**EECE 343 Computer Interface Circuits**

**Lab 6**

**9-Bit Sequence Detector**

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**Objectives**

The purpose of this exercise is to learn how to design a 9-Bit Sequence Detectorusing finite state machine. We will use the dip switches or de-bounced switches on the DE2 board as inputs to the circuit, and outputs to LEDs, Seven Segment Display, and LCD Display.

**Project**

# Please design a 9-Bit Sequence Detector with VHDL programming and implement the design with the DE 2 board for a sequence of code, 110110101.

# The minimum requirements of the 9-Bit Sequence Detector are

# A parallel-in 9-bit shift register controlled by a load pin

# A start key to recognize the displayed by 9 LEDs and 3 Seven-Segment Displays and LCD Display

# Display for failure or success of the recognition.

**Procedure**

Perform the following steps to implement a circuit for the project on the DE2 board.

1. Create a new Quartus II project for your circuit. If using the Altera DE2 board, select Cyclone II EP2C35F672C6 as the target chip, which is its FPGA chip.
2. Create a VHDL entity for the code of the lab project.
3. Include in your project the required pin assignments for the DE2-series board, as discussed above. Compile the project.
4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit.
5. Turn in your lab report on the day you demonstrate your project in class.