**EECE 343 Computer Interface Circuits**

**Lab 9**

**Slot Machine**

Dr. Hede Ma

**Objectives**

The purpose of this exercise is to learn how to design a Slot Machineusing finite state machine. We will use the dip switches or de-bounced switches on the DE2 board as inputs to the circuit, and outputs to LEDs, Seven Segment Display, LCD Display, and VGA Monitor.

**Project**

# The key part of a slot machine is a pseudorandom number generator. Please design a state machine to produce a three-digit pseudorandom numbers for per deposited coin (hint: three counters designed with different sequences, respectively, can do the job). Design a winning number mechanism that determines the winning numbers following a certain probability, which should not be too tough or too easy. If too tough, no one will play the machine. If too easy, you will lose money. Please verify your design using VHDL with Altera Quartus II and implement the circuit with the DE 2 board. The three-digit pseudorandom numbers shall be displayed by three seven-segments, and the result shall be displayed by LCD and VGA Monitor for win or losing. Extra credit will be given if the three-digit pseudorandom numbers can be dynamically displayed by the VGA Monitor, too.

**Procedure**

Perform the following steps to implement a circuit for the project on the DE2 board.

1. Create a new Quartus II project for your circuit. If using the Altera DE2 board, select Cyclone II EP2C35F672C6 as the target chip, which is its FPGA chip.
2. Create a VHDL entity for the code of the lab project.
3. Include in your project the required pin assignments for the DE2-series board, as discussed above. Compile the project.
4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit.
5. Turn in your lab report on the day you demonstrate your project in class.