

Unit-2

Digital logic families

Definition: → group of compatible ICs with same logic level & supply voltages for performing various logic functions. which have been fabricated using specified configuration, this is referred to as Digital logic families.

Digital logic families

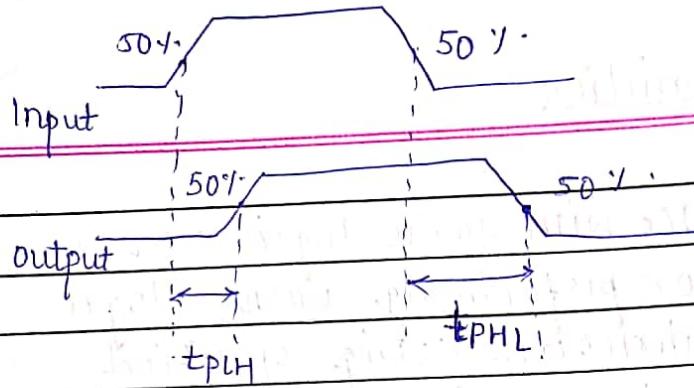
↳ Bipolar logic families

↳ Unipolar logic families

saturated mode	unsaturated mode	Pchannel metal oxide semiconductor - PMOS
- RTL: Register Transistor Logic	- DTL: Diode Transistor Logic	- N MOS
- DCTL: Direct Coupled Transistor logic	- TTL: Transistor Transistor Logic	- CMOS
- HTL: High Threshold logic	- ECL: Emitter coupled logic	complimentarity Metal oxide semiconductor
- I ² L: Integrated injection logic		

Characteristics of Digital ICs

- 1) Speed of operation: → speed of digital IC is expressed in terms of propagation delay. When we apply input on logic gate output occurs after some time & this is



called propagation delay.

② Current and voltage parameter :-

(i) $V_{IH}(\text{min})$

\therefore If it is high level input voltage it is min. voltage level required for logic one as an input below this minimum level it will not be expected as HIGH by logic gate circuit.

(ii) $V_{IL}(\text{max})$:- it is low level input voltage it is maximum voltage level required for logic zero at input. Any voltage above this level will be considered as HIGH input.

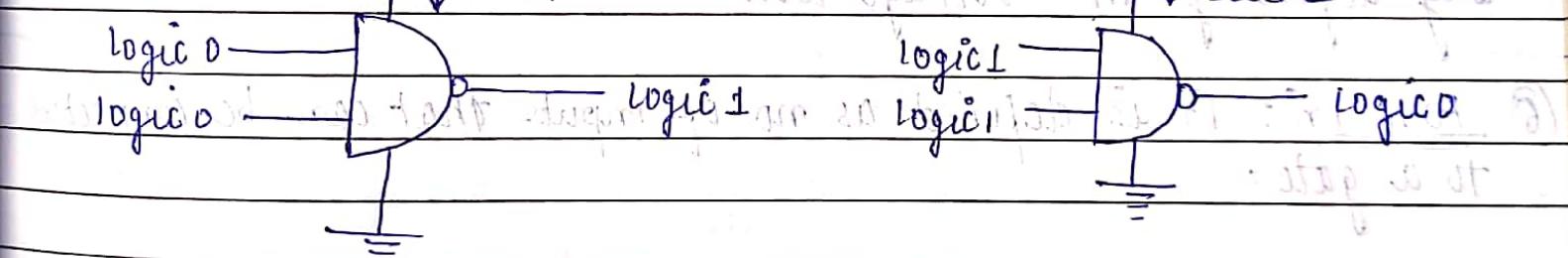
(iii) $I_{OL}(\text{min})$:- it is low level output current it is the max. current level at the a logic ckt Output is in logical zero state under the defined load condition.

(iv) $I_{IH}(\text{min})$:- it is high level input current it is the current that flows into an input when a specified high level voltage is applied to that input.

- (v) $I_{IL(\max)}$:- It is low level input current. It is the current that flows into an input when a specified low level voltage is applied to that input.
- (vi) I_{OH} :- High level output current. It is the current that flows from output in the logic one state under specified load conditions.
- (vii) I_{OL} :- It is low level output current. It is the current that flows from an output in logic 0 state under specified load condition.

③ Power dissipation :-

$I_{CC(H)} + V_{CC} \times I_{CC(L)}$



$$I_{CC(H)} \quad I_{CC(\text{avg})} = I_{CC(H)} + I_{CC(L)}$$

$$P_{\text{avg}} = V_{CC} \times I_{CC(\text{avg})} \\ = V_{CC} \left[\frac{I_{CC(H)} + I_{CC(L)}}{2} \right]$$

IC requires some power for operation & this is called power dissipation. When gate is in high output the current drawn by gate is represented by I_{CCH} .

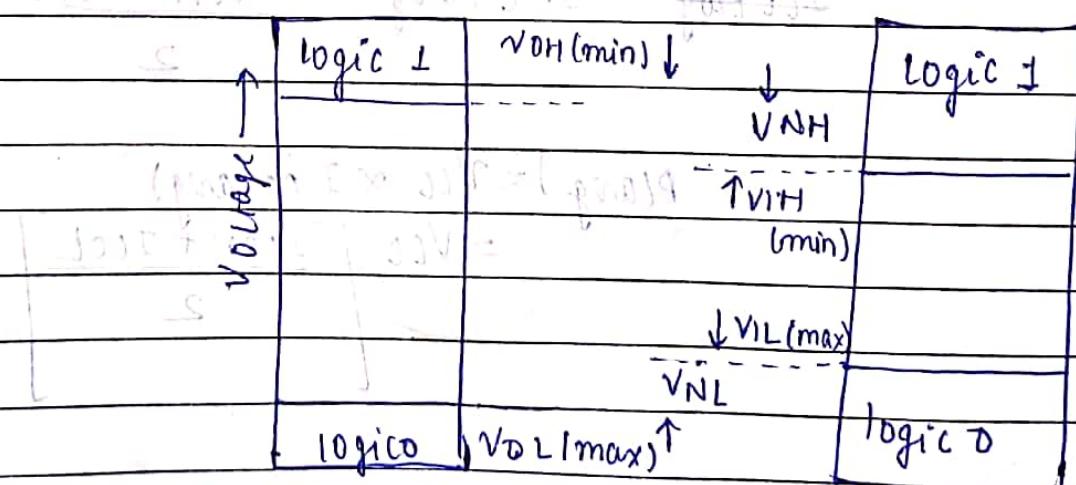
When gate is in low output current drawn by gate is represented by I_{CL} .

(4) Figure of Merit : \rightarrow Figure of Merit = power \times propagation delay.

(5) Fan out: It is also called loading factor. It is maximum no. of similar logic gate that a gate can drive without any degrading in voltage level.

(6) Fan in: It is defined as no. of inputs that can be connected to a gate.

(7) Noise immunity:-



state L Noise Margin = $V_{OH} - V_{IH}$

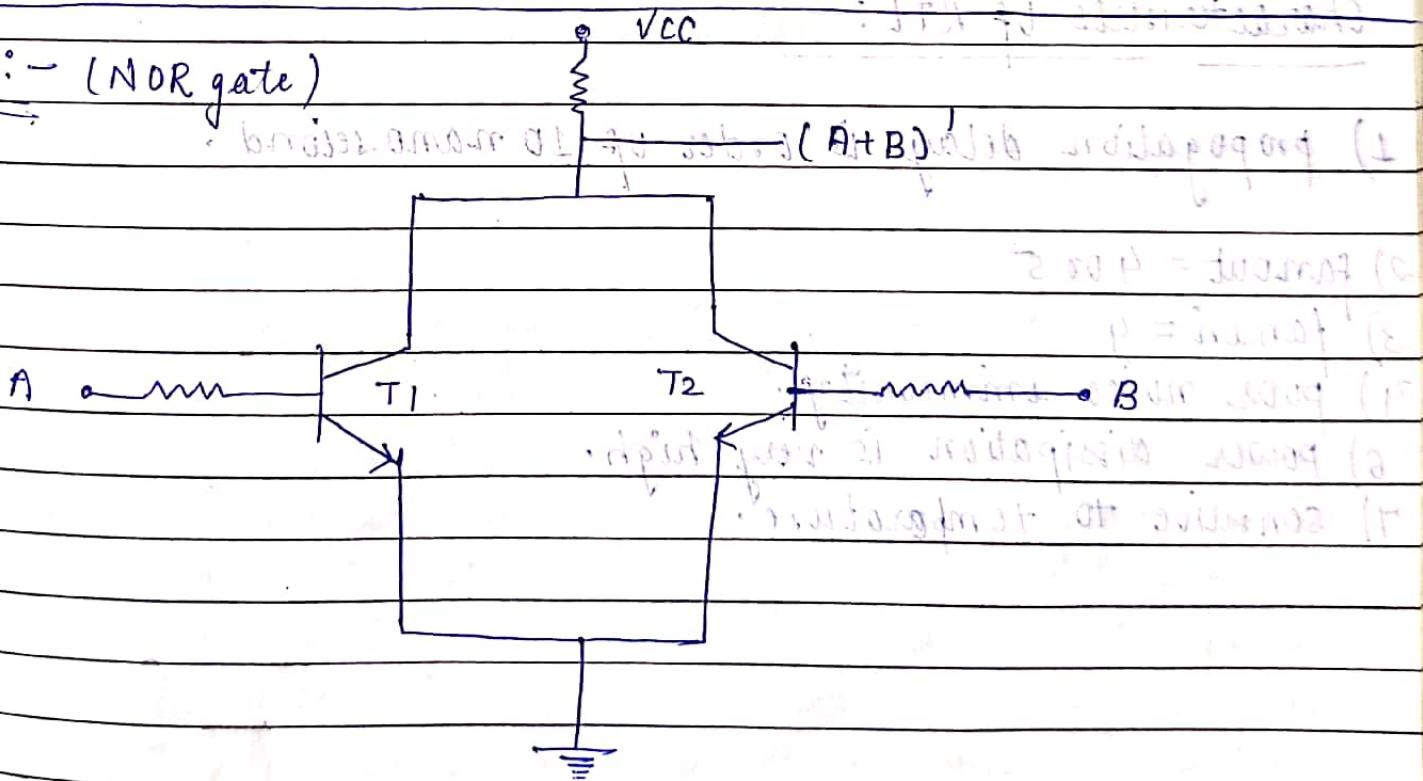
state H Noise Margin = $V_{IL} - V_{OL}$

The input & output level of digital ckt is specified by voltage level. Some unwanted voltage might induced may cause voltage at input of logical ckt to draw below V_{IH} and rise above V_{IL} and may produce undesired operation.

Noise immunity is the max. noise voltage at input of logic ckt without changing logic state of its output.

⑧ Operating Temperature: It ranges from 0°C to $+70^{\circ}\text{C}$ for consumer and industrial application. For military application it ranges from -55°C to $+125^{\circ}\text{C}$.

RTL :- (NOR gate)



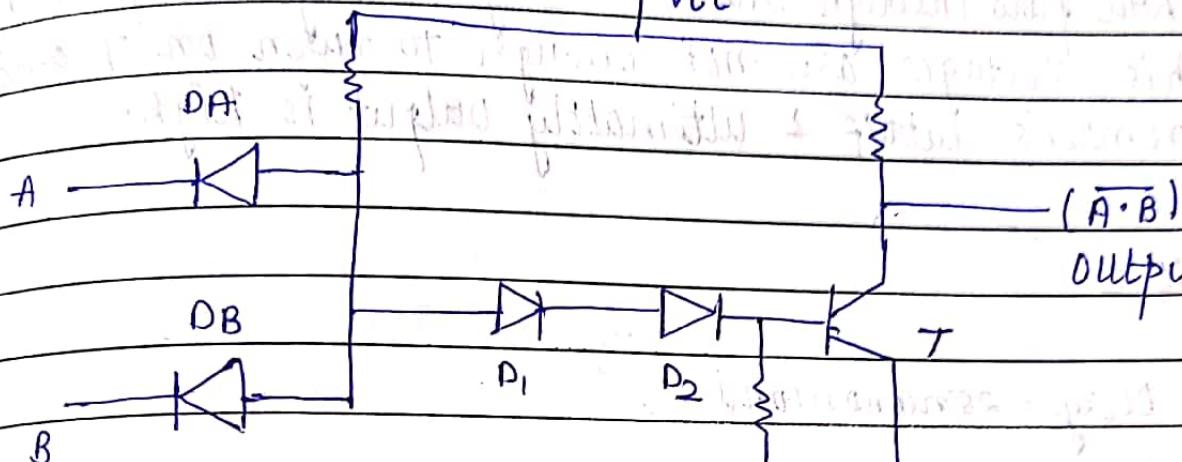
Inputs.	Transistors		Output	
A	B	T ₁	T ₂	Y
L L	OFF	OFF	H	High as both transistors are off
L H	OFF	ON	L	Low as T ₁ is off & T ₂ is on
H L	ON	OFF	L	Low as T ₁ is on & T ₂ is off
H H	ON	ON	L	Low as both T ₁ & T ₂ are on

The basic ckt of an RTL digital logic family using NOR gate is shown in the figure. It was one of the earliest technology of Digital IC and is not used now a days. When both inputs are low (t_1 and t_2 are cutoff) & output is high. A high level on any input drives the corresponding transistor to saturation causing output to low (expands t_1 & t_2).

Characteristics of RTL:-

- 1) propagation delay is order of 10 nano-second.
- 2) fanout = 4 or 5
- 3) fanin = 4
- 4) poor noise immunity.
- 5) power dissipation is very high.
- 6) sensitive to temperature.

DTL



Inputs	Diode	Transistor	Output
A B	D _A D _B D ₁ D ₂	T ₁ T ₂ T ₃	Out = (A·B) JTF
L L	F _B F _B OFF OFF	OFF OFF	H
L H	F _B R _B OFF OFF	OFF OFF	H
H L	R _B F _B OFF OFF	OFF OFF	H
H H	R _B R _B ON ON	ON OFF	L
			JTF high level (L)
			JTF low level (S)
			JTF high input (S)

Figure shows a 2 input NAND gate using diode-transistor logic. This logic uses a transistor and diode. Two diodes D_A and D_B performs logic AND operation followed by a transistor inverter which results in a NAND gate. When both the inputs are logic High level the diodes D_A and D_B are RB^{if}. D_A and diode D₁ & D₂ & transistor are switched on hence output is low. If any of input drop to ground potential the corresponding input diode will conduct &

current will flow through diode causing voltage drop at input of D_1 . These voltages are not enough to turn on T and hence T remains cut-off & ultimately output is high.

Characteristics

propagation Delay = 25 nanosecond

fanout = 8

noise margin = 0.8 V when output is low

= 3.4 V when output is high

IMP TTL :- It has been used for several years because of its good performance. It has more speed than DTL. It is a variable from several manufacturers & it is easily interconnected & interface with other digital circuitry.

The sub family of TTL are as follows:-

1) Basic / standard TTL

2) Low power TTL

3) High speed TTL

4) Schottky TTL with Schottky diodes & zener diodes

5) Adv. Schottky TTL (Fast switching speed)

6) Adv. low power Schottky TTL (low current draw)

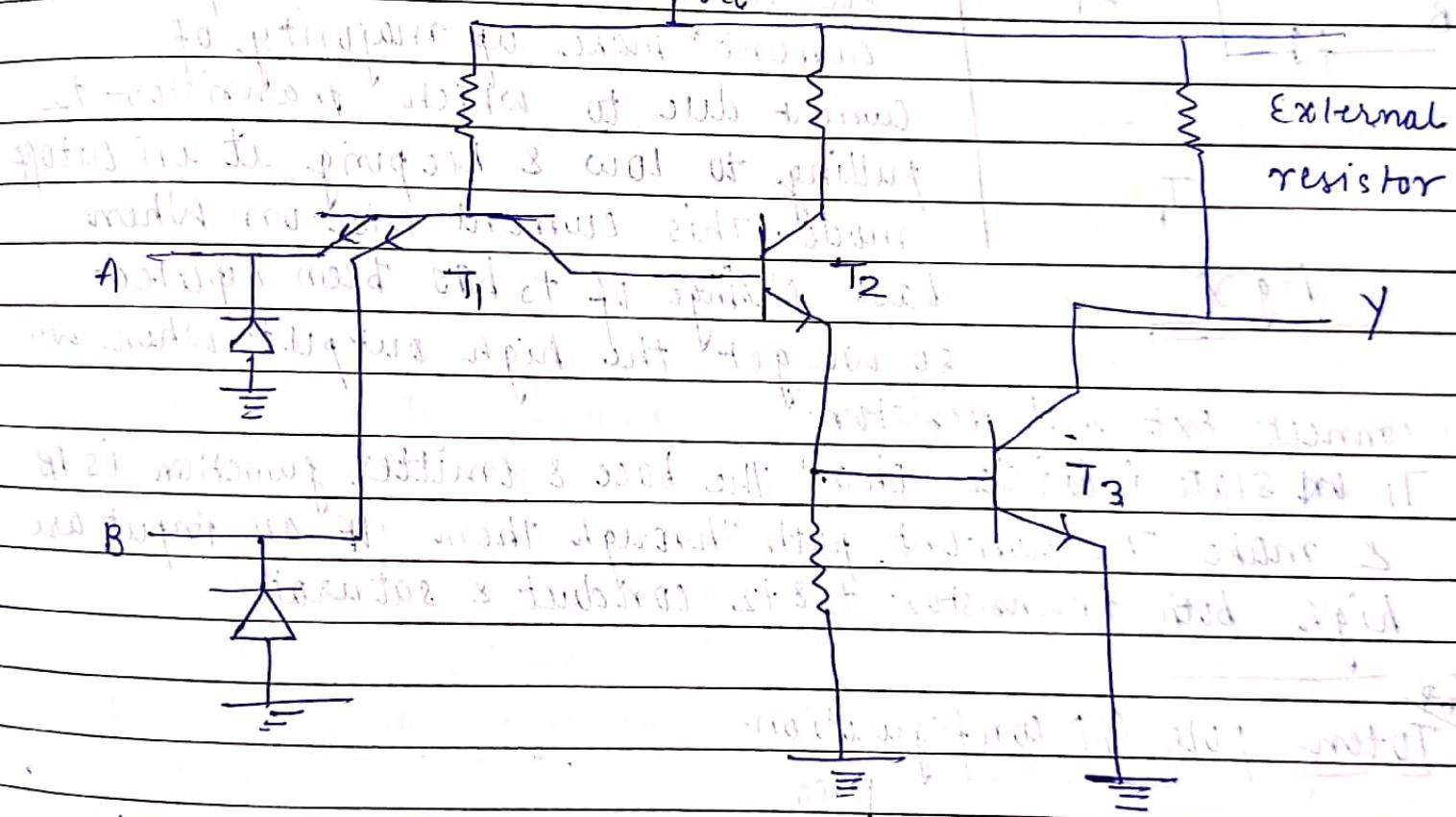
7) Fast TTL (Fast switching speed)

TTL gates in all available series come in 3 diff. types of output configurations.

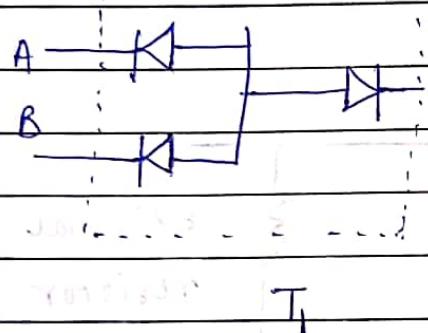
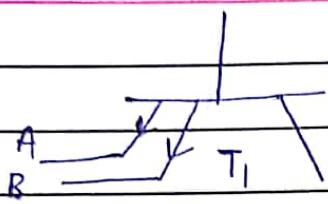
1) Open collector output which provides open collector output with saturation.

- 1) Open collector O/p configuration
- 2) Totem pole O/p
- 3) Three state (Tri-state O/p configuration)

- 1) Open collector O/p configuration



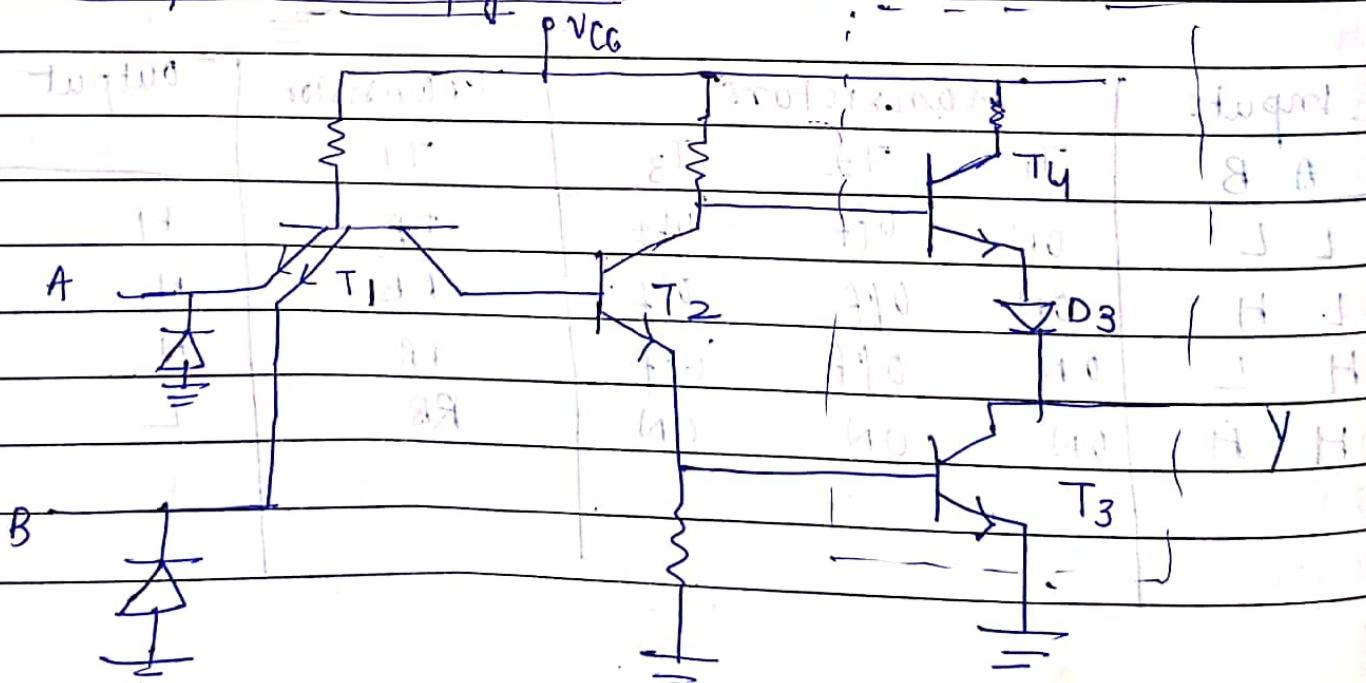
Inputs	Transistors T1, T2	Transistor T3	Transistor T4	Output
A B	ON OFF	OFF	OFF	Open
L L	ON OFF	OFF	ON	H
L H	ON OFF	OFF	ON	A
H L	OFF ON	OFF	ON	H
H H	OFF ON	ON	ON	L

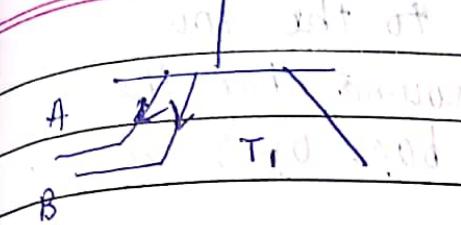
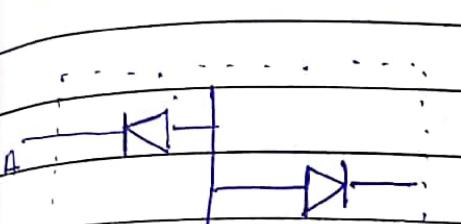
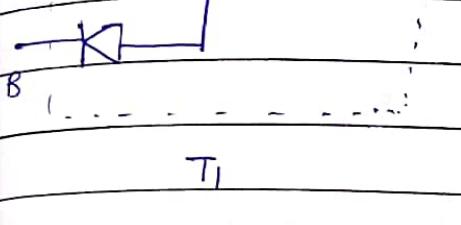
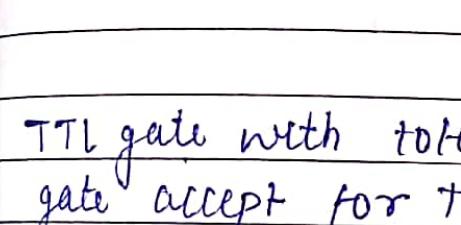


The transistor T_1 can be treated as diode equivalent as shown in fig. X. When the TTL inputs are low the base-emitter junction of T_1 act as FB diode, creating a current path from V_{cc} to ground via this input. This current makes up majority of current due to which transistor T_2 pulls to low & keeping it in cutoff mode. This current exists when base change of T_3 has been depleted so we get the high output when we connect external resistor.

T_1 off state indicates that the base & emitter junction is FB & make the current path through them. If all inputs are high both transistor T_1 & T_2 conduct & saturate.

Totem pole O/P configuration-



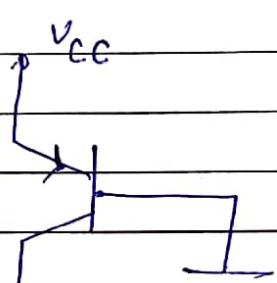
	Inputs	Transistors	Transistor	Output
	A, B	T ₁ , T ₂ , T ₃		
	L L	ON OFF OFF	ON	H
	L H	ON OFF OFF	ON	H
	H L	ON OFF OFF	ON	H
	H H	OFF ON ON	OFF	L

Outputs

TTL gate with totem pole output is same as the open collector gate except for the transistor T₄ and the diode D₂-D₃ as shown in fig. It has separate transistor T₀ to switch the output to the high state T₀ & the low state (T₃). These transistors are switched by T₂; phase splitter ensures one of them is ON at a time. The main advantage of totem pole output over the open collector output is that it can change state faster. When both inputs are high, the base-emitter junction T₁ is RB & base-collector junction is FB. This condition permits current through resistor R_B & base-collector junction of T₁ into base of T₂ thus driving T₂ to saturation. As a result T₃ is turned on by T₂ & its collector voltage which is the output is near ground potential (low). When one or more inputs are low, the base-emitter junction of T₁ is FB & base-collector junction is RB. There is current through

Resistor and base emitter junction of T_1 , to the low inputs. A low level provides path to ground for the current. There is no current into the base of T_2 so it is OFF.

I²SL



+ V_{CC}

output?

realization with NMOS has a turned off transistor also if input A is high both NMOS transistors will not conduct due to the fact that the current through each NMOS is proportional to the width of the channel. If one NMOS is turned off then the other NMOS will conduct. In this case the output voltage will be high. So the output voltage is dependent on which NMOS is turned off.

A and B | Q₂ | Output | monolithic structure no resistor are employed which occupy sufficient space on the chip in case of other logic family so very high densities of integration are possible; nearly 10 times that of DTL. It consumes very low supply current this technology has been employed for producing different devices.

Complex LSI & VLSI functions like that of microprocessor Fig. shows I^2L NAND gate. The NAND gate is simply an inverter to that inputs connected directly together at inverter. When either or both inputs are low Q_2 is off. When both input is high Q_2 is turned on making the output low.

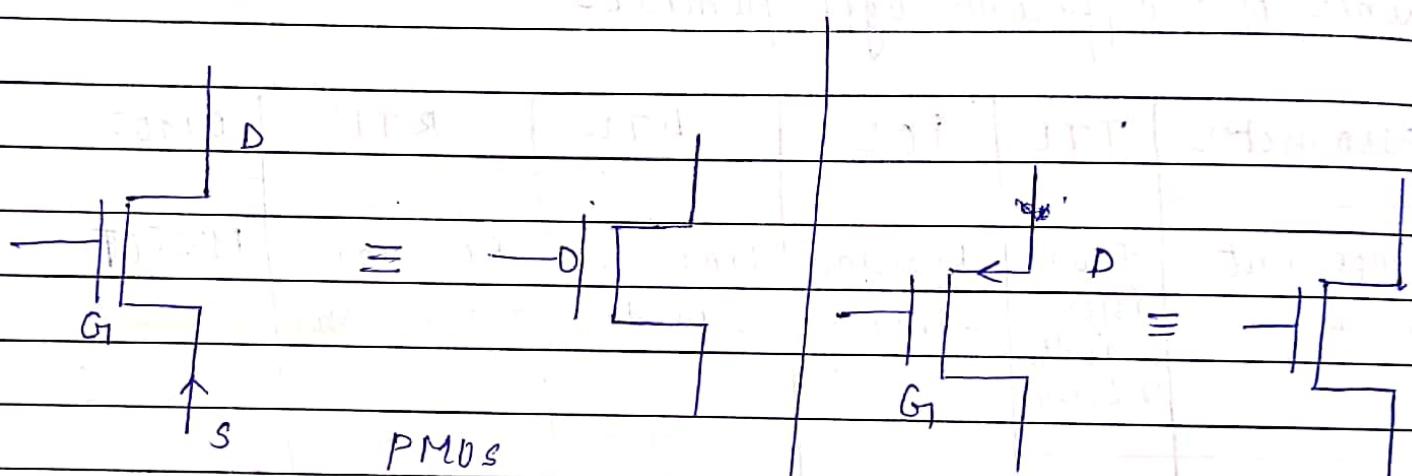
Difference b/w different logic families

no.	Parameter	TTL	ECL	DTL	RTL	CMOS
1.	component used	Transistor, diode, resistor	Resistor & Transistor	Transistor & Diode	Resistor & Transistor	MOSFET
2.	fanout	Moderate	High	Low	Low	Highest
3.	propagation delay	10 ns	2 ns	10 ns	12 ns	70 nano seconds
4.	Noise Margin	Moderate	Low	poor low	Poor	High
5.	Power dissipation per gate	10 milliwatt	40-50 milliwatt	30 milli watt	30 milliwatt	0.1 milliwatt
6.	CKT complexity	complex	complex	Not complex	Not complex	Moderately complex
7.	Application	Lab & demonstration	High speed switching	not used	not used	Portable equipment
	Equipment		application			

Most used

MOSFET: (Metal oxide semiconductor field effect transistor)

Simplest to fabricate & occupy very less space because it requires only N-MOS and P-MOS transistors. It does not require resistor & diode which require large space. Power dissipation is low, operating speed is less than TTL. It is used in calculator chip, large microprocessor etc.

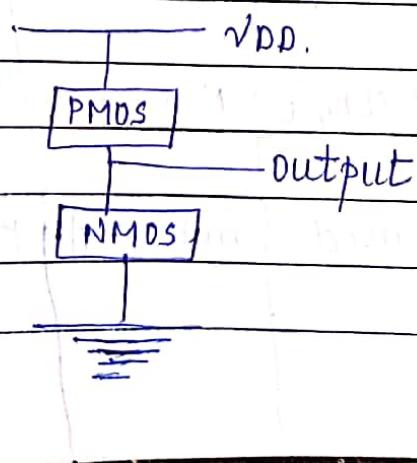


Current Flows from source
to drain

NMOS
current flows from Drain
to source.

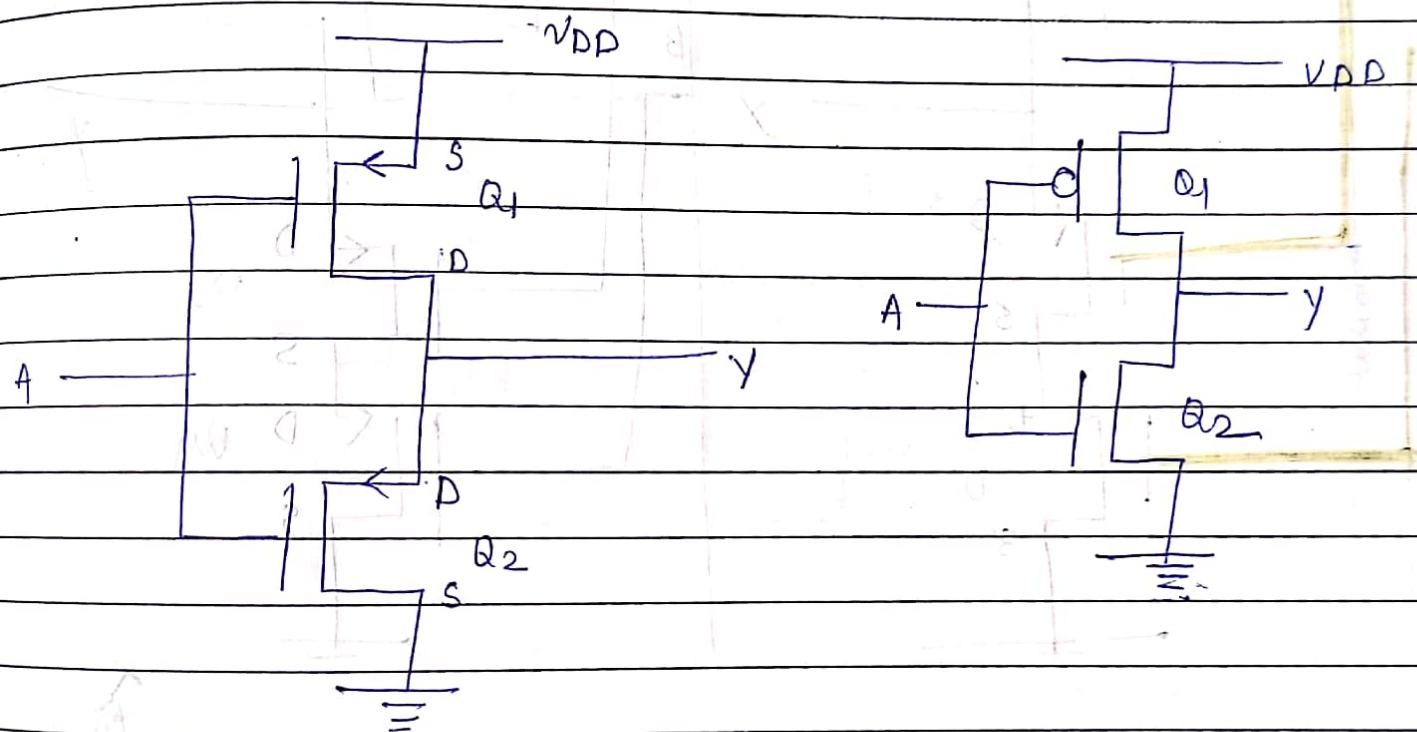
Imp**

CMOS: (complementary metal oxide semiconductor)



It uses both p channel & n channel MOSFETs in same ckt
 it is faster & consume less power than other MOS family

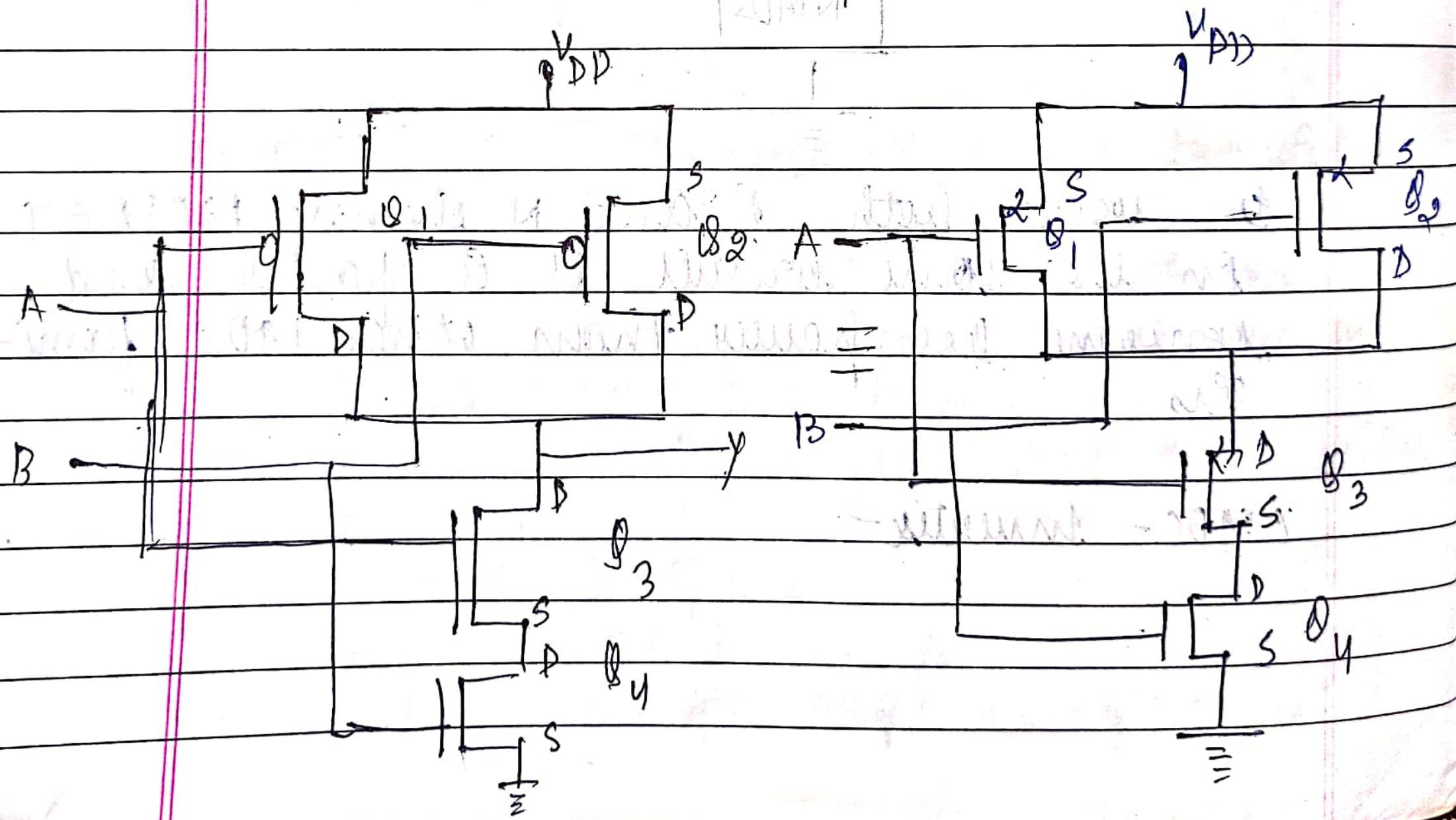
CMOS Inverter



Description:-

Input	Transistor	Output
A	Q ₁ Q ₂	Y
L	ON OFF	H
H	OFF ON	L

Lⁱg_o CMOS NAND Gate



P Mos - parallel.
N Mos - series

Inputs

A B

Resistors

Ω_1 Ω_2 Ω_3 Ω_y

Output -

y

L L

ON ON OFF OFF

H.

L H

ON OFF OFF ON

H

H L

OFF ON ON OFF

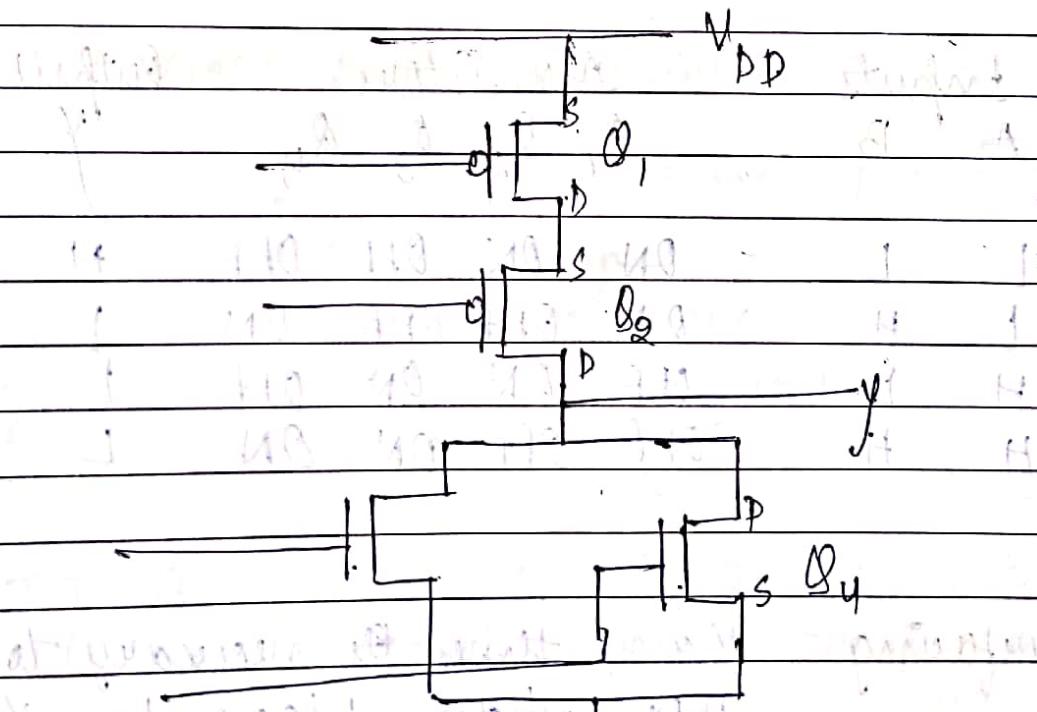
H

H H

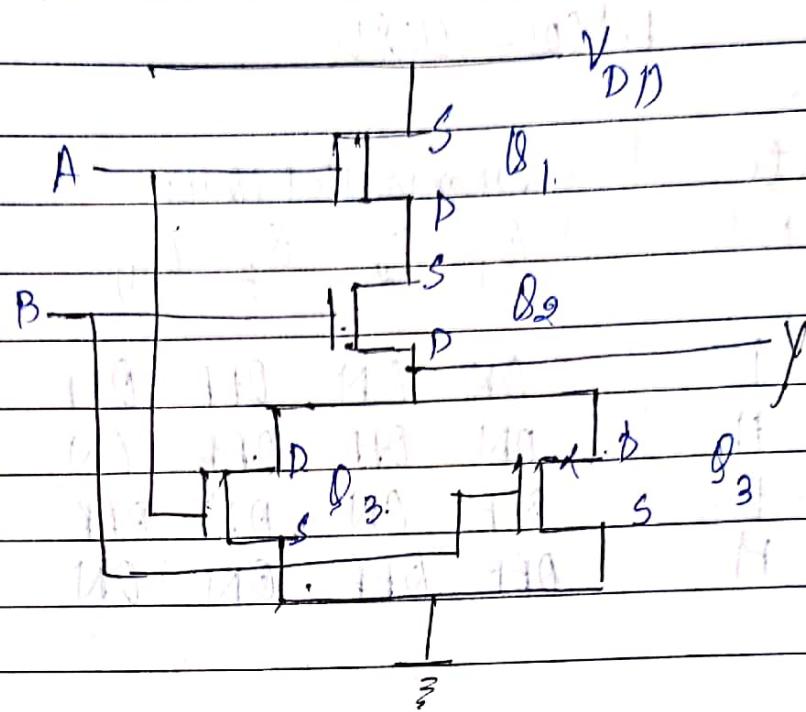
OFF OFF ON ON

L.

C MOS AND GATE



N MOS - Parallel. P-MOS - Series.



Truth Table -

Inputs Transistors Output
A B Q₁, Q₂, Q₃, Q₄ Y

L	L	-	ON	ON	OFF	OFF	H.
L	H		ON	OFF	OFF	DN	I
H.	L		OFF	ON	ON	OFF	L
H	H.		OFF	OFF	ON	ON	L

17-10-19 Interfacing - Many times it is necessary to use more than 1 logic family in a digital circuit. When gate from 1 family is feeding gate from another family, it is necessary to ensure that gate from one family is matching the other. This is interfacing.

Interfacing

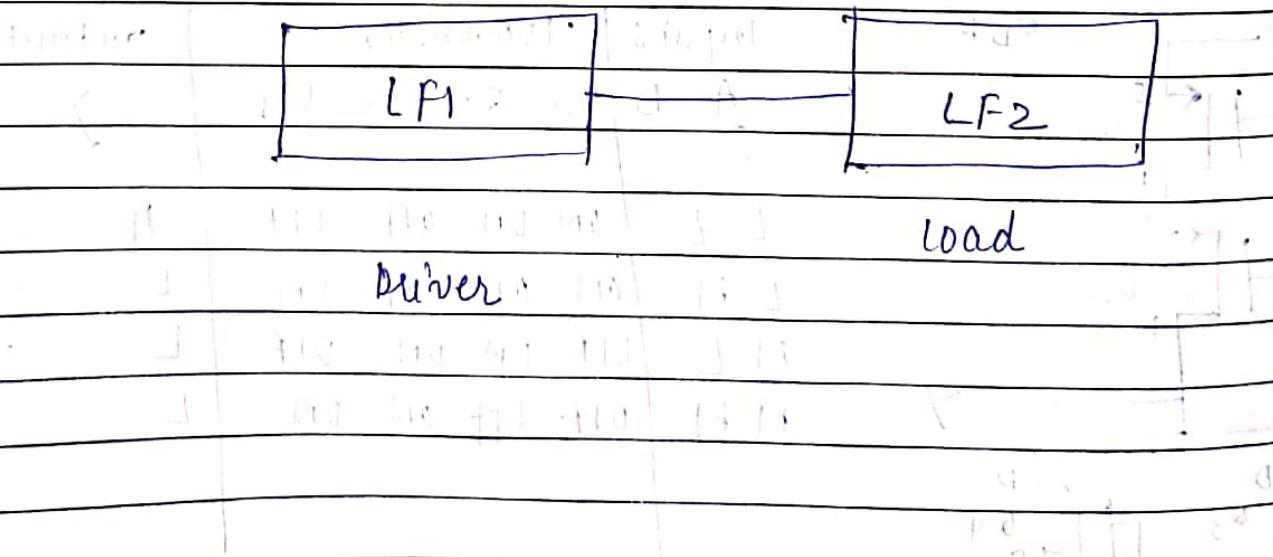
Many times it is necessary to use more than one logic family in a digital ckt. When gate of one family is feeding gate of other family it is necessary to ensure that there are matching voltage & current.

Interfacing means conn. O/p of one ckt or system to I/p of other ckt or system that may have different electrical characteristic. When 2 ckt have diff. electrical characteristic direct connection cannot be build.

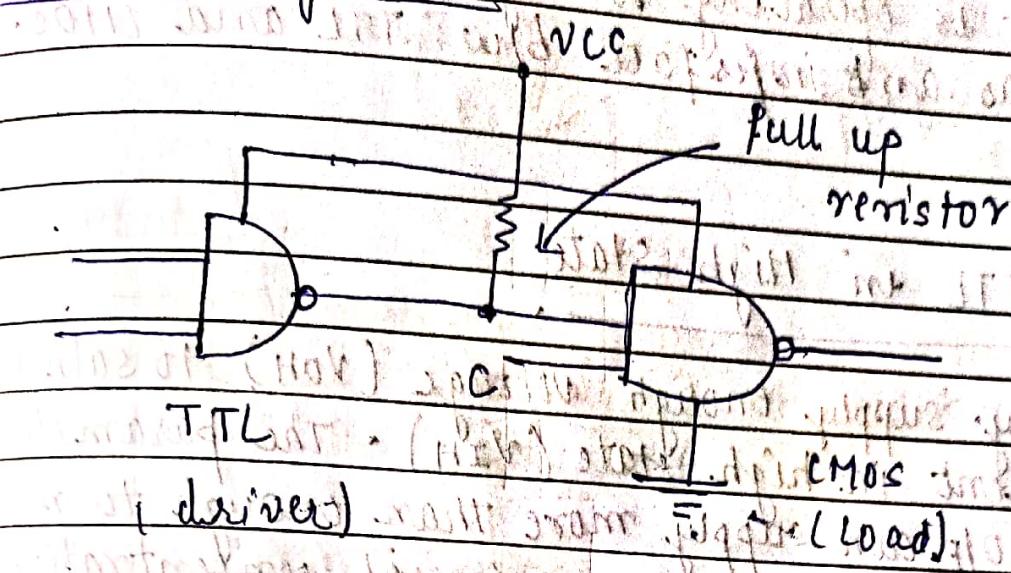
Its function is to take the driver O/p signal & condition it so that it is compatible with requirement of load.

Measure & category of interfacing are:-

- 1) TTL - CMOS interfacing
- 2) CMOS - TTL interfacing.

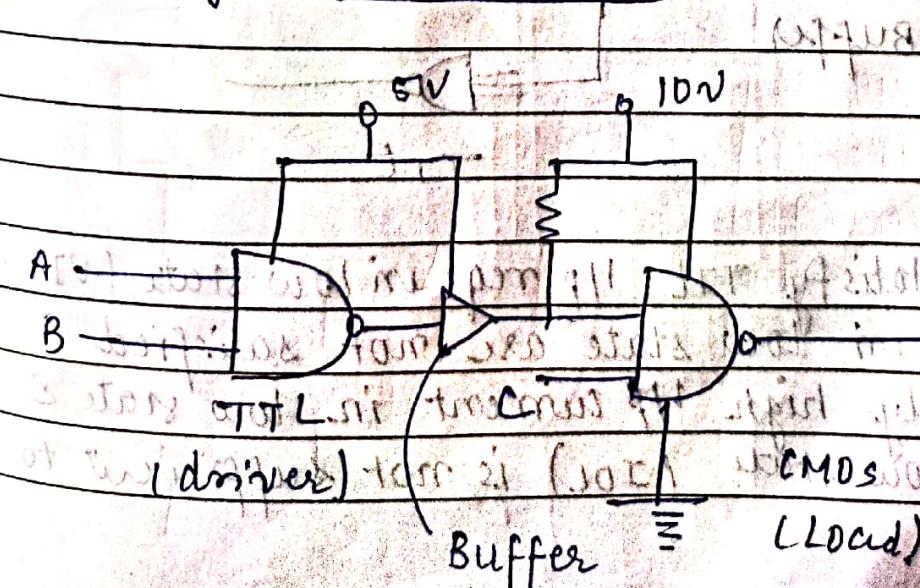


1) TTL driving CMOS



I/P current value for CMOS are extremely low compared with O/P current capacity of any TTL series thus TTL has no problem in meeting the CMOS I/P current requirement but V_{OH(min)} for TTL is very very less than V_{IH(min)} for CMOS in this situation TTL output must be raised to an acceptable level for CMOS. This can be done by conn. pull up resistor at O/P of TTL as shown in Fig.

TTL driving High level CMOS

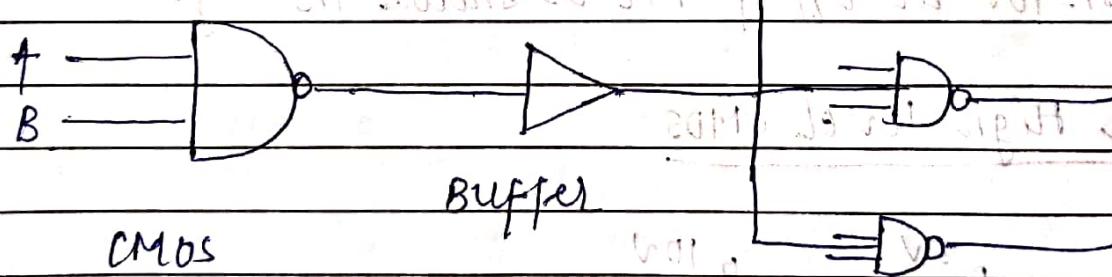


When O/P CMOS CKT is operating with greater than 5V then buffer is used as an interface b/w TTL and CMOS.

2) CMOS driving TTL in High state

CMOS O/P can easily supply enough voltage (V_{OH}) to satisfy TTL I/O requirement in high state (V_{IH}). The parameters shows that CMOS O/P can supply more than enough to meet TTL I/O current requirement thus no special concentration consideration is required for CMOS driving TTL in High state.

CMOS driving TTL in low state with sink capability see load driver



CMOS O/P voltage V_{OL} satisfy TTL I/O req. in low state (V_{IL}) However current req. in low state are not satisfied as TTL I/O has relatively high I/O current in low state & CMOS O/P current in low state (I_{OL}) is not sufficient to

drive even one I/O of TTL in such situation Buffer is used as an interfacing CRT.

Assignment

Q1. TTL to ECL interfacing } Anand Kumar
Q2. ECL to TTL interface }

Q3 Design & Implement ECL

Q4 Write a short note on schottkey TTL.

Q5 Describe 3 state (Tri-state O/P config. of TTL)