Zebu Basic Training

September 16 - 20, 2013

This training is for Verification ACs and CAEs. The prerequisite is to have knowledge of Verilog and C++ language and generic design verification.

Day 1 Recorded Training: http://us01-webcast-04/Webcast_On-Demand/Zebu_Basic_Training_9-16-13	**Agenda:** • Overview
Day 2 Recorded Training: http://us01-webcast-04/Webcast_On-Demand/ZeBu_Basic_Training_9-17-13	**Agenda:** • Synthesis • Compilation
Day 3 Recorded Training: http://us01-webcast-04/Webcast_On-Demand/Zebu_Basic_Training_9-18-13	**Agenda:** • Runtime • HDL Co-Simulation
Day 4 Recorded Training: http://us01-webcast-04/Webcast_On-Demand/Zebu_Basic_Training_9-19-13	**Agenda:** • C/C++ Co-simulation
Day 5 Recorded Training: http://us01-webcast-04/Webcast_On-Demand/Zebu_Basic_Training_9-20-13	**Agenda:** • Using Transactors • Designing zcei Transactors