EXPERIMENT 7

AIM: To design and implement 4-bit common bus using 4*1 multiplexers

PLATFORM USED: Circuit verse

THEORY:

BUS TRANSFER

There should be a path to process data transfers between registers/memory. These paths are basically group of wires, which is referred as common bus system. The bus structure is basically a set of common lines one for each bit of a register. There are control signals to decide which register is selected by bus and for each register transfer.

COMMON BUS TRANSFER

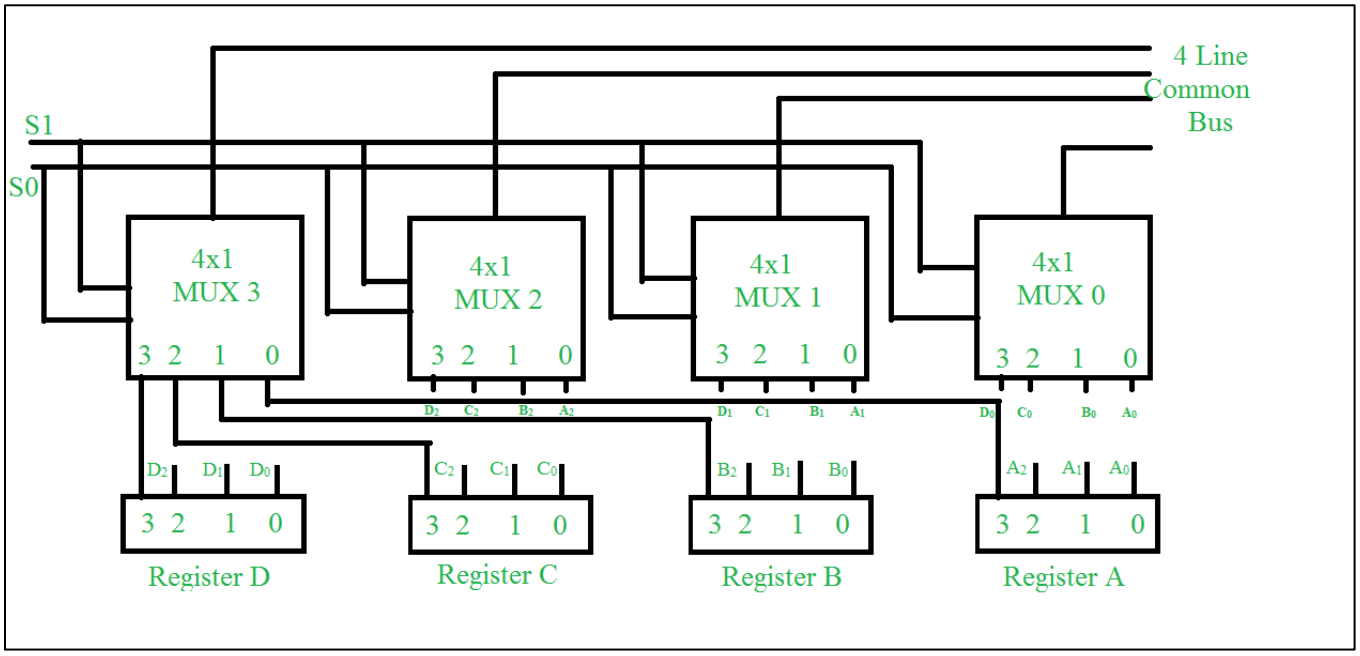
To transfer information from one register to another and between memory and registers, paths are required. If individual and separate connections are made between the outputs of each register and the inputs of the other registers, the system will become complex and messy. A more efficient scheme for transferring information in a system with many registers is to use a common bus. The connection of the registers and memory of the basic computer to a common bus system is done by multiplexers or three-state buffer gates.

COMMON BUS THROUGH MULTIPLEXER

The multiplexers select the source register whose binary information is then placed on the bus. Each register has four bits, numbered 0 through 3. The bus consists of four 4 x 1 multiplexers each having four data inputs, 0 through 3, and two selection inputs, S1 and SO. In order not to complicate the diagram with 16 lines crossing each other, labels are used to show the connections from the outputs of the registers to the inputs of the multiplexers. The multiplexers select the source register whose

binary information is then placed on the bus. Each register has four bits, numbered 0 through 3.

The selection lines S1 and SO decides which register data must be transferred on common bus. The multiplexers select the source register whose binary information is then placed on the bus. Each register has four bits, numbered 0 through 3. The bus consists of four 4 x 1 multiplexers each having four data inputs, 0 through 3, and two selection inputs, S1 and SO. In order not to complicate the diagram with 16 lines crossing each other, labels are used to show the connections from the outputs of the registers to the inputs of the multiplexers.

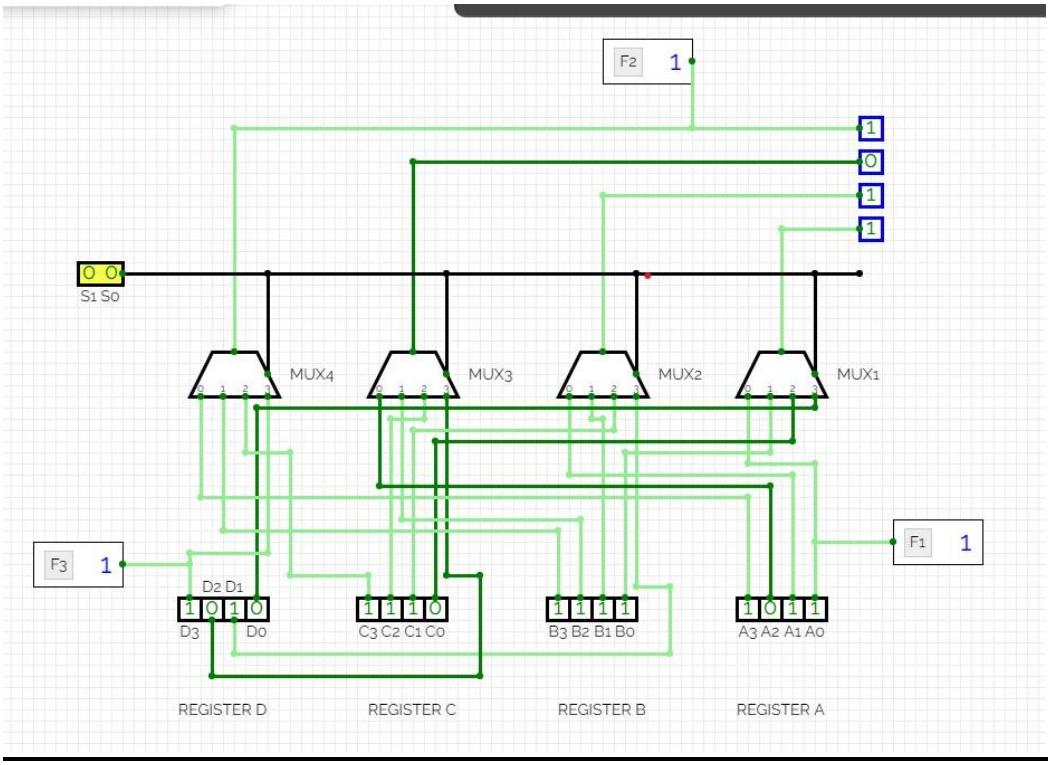


4-bit common bus

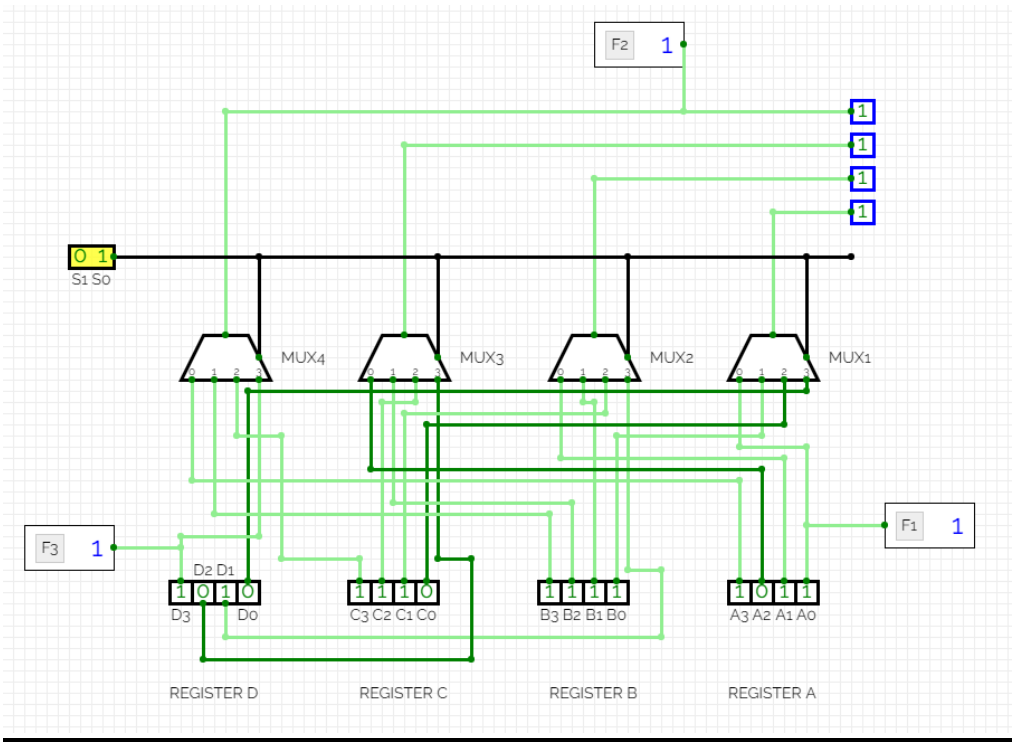
Select Lines combination S1S0	Register Selected
00	Register A
01	Register B
10	Register C
11	Register D

OUTPUT

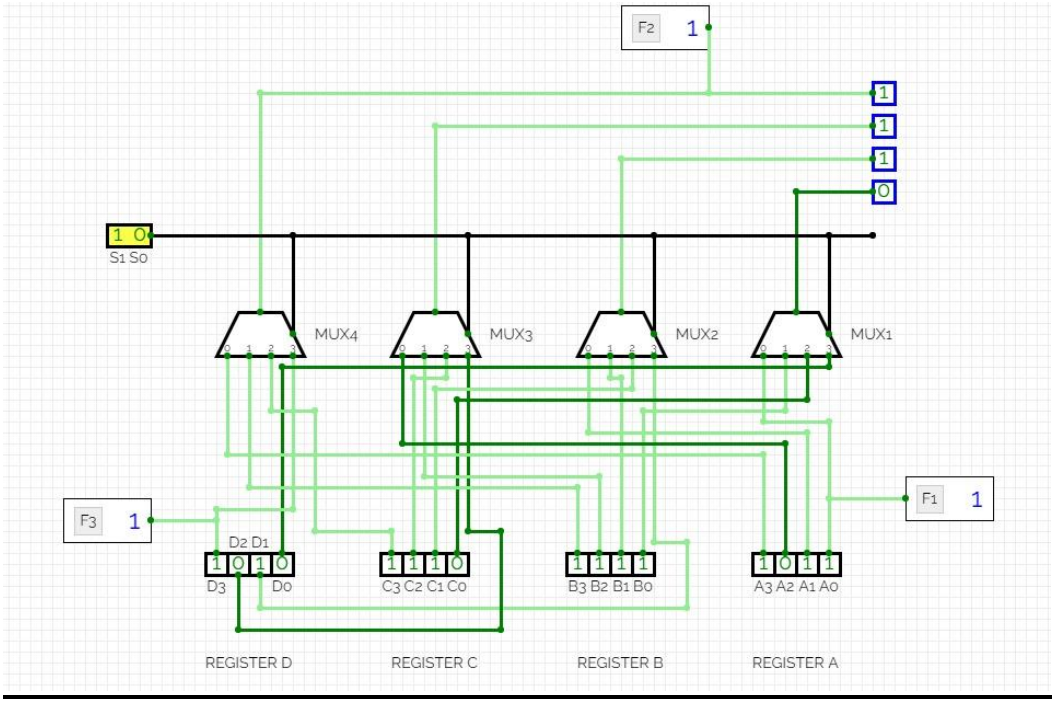
Register A



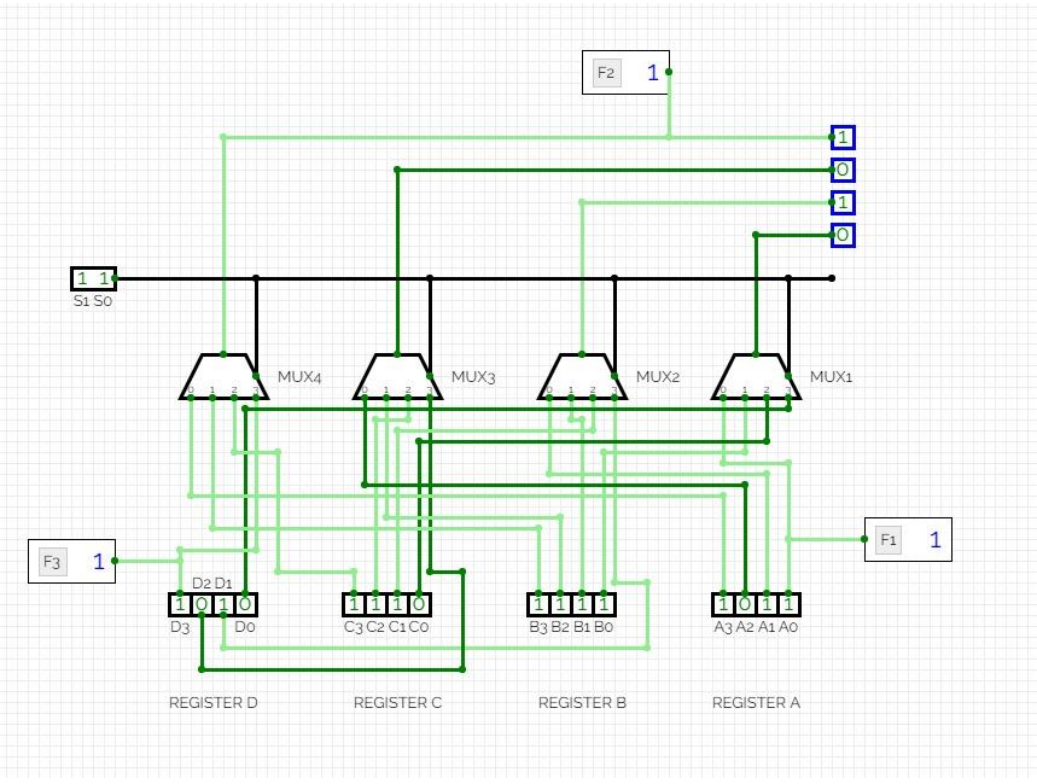
Register B



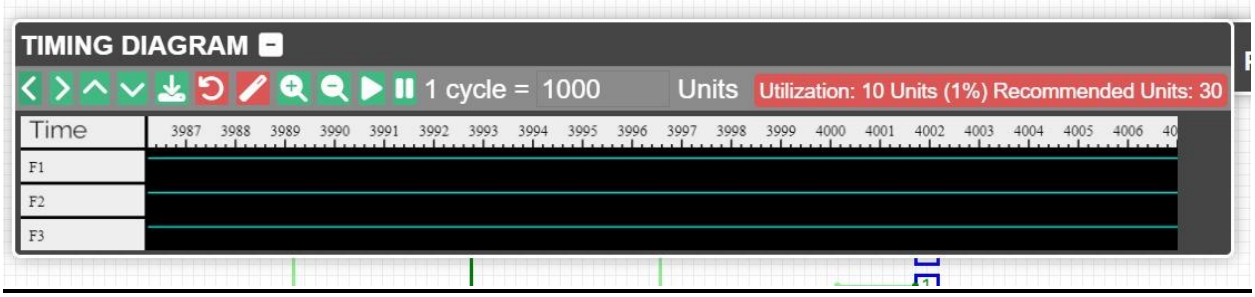
Register C



Register D



TIMING DIAGRAM



RESULT

4-bit common bus using 4*1 multiplexers has been designed and implemented.

Criteria	Total Marks	Marks Obtained	Comments
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		