

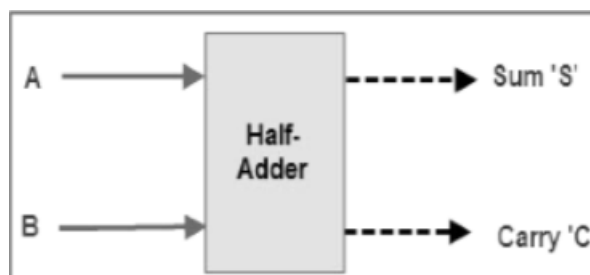
## EXPERIMENT-2

**AIM:** To design a half-adder circuit using

- i. Logic Gates
- ii. NAND gate only

**TOOL USED:** Circuit Verse

**THEORY:** Half adder is a combinational circuit that simply adds two binary numbers. If we assume A and B as the two bits whose addition is to be performed, the block diagram and a truth table for half adder with A, B as inputs and Sum, Carry as outputs can be tabulated as follows.



**Block Diagram**

**Truth Table**

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The sum output of the binary addition carried out above is similar to that of an Ex-OR operation while the carry output is similar to that of an AND operation. The same can be verified with the help of Karnaugh Map.

The K Map simplification and logic diagram for sum output is shown below.

A \ B	0	1
0	0	1
1	1	0

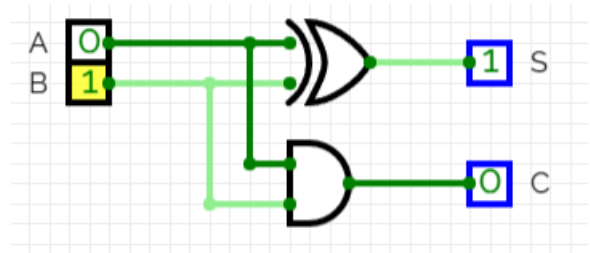
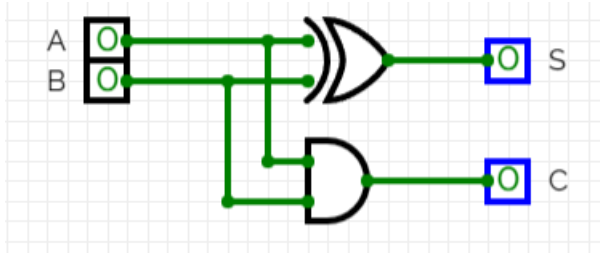
**K-Map for Carry**

A \ B	0	1
0	0	0
1	0	1

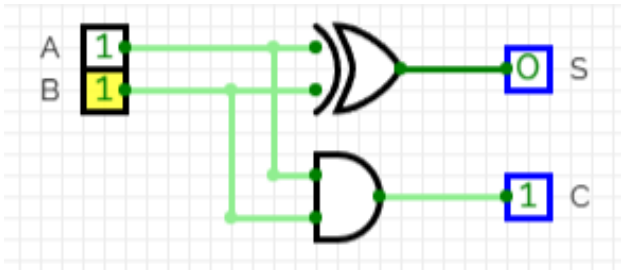
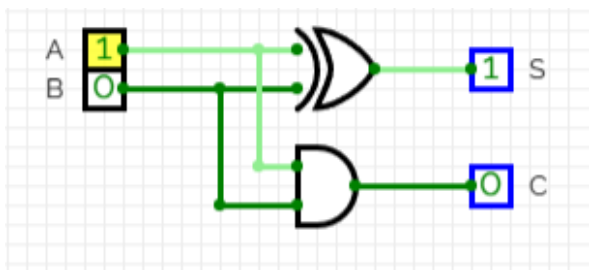
**K-Map for Sum**

**OBSERVATIONS:**

- i. Logic Gates  
 $S = AB' + A'B$   
 $C = A.B$

[illegible]

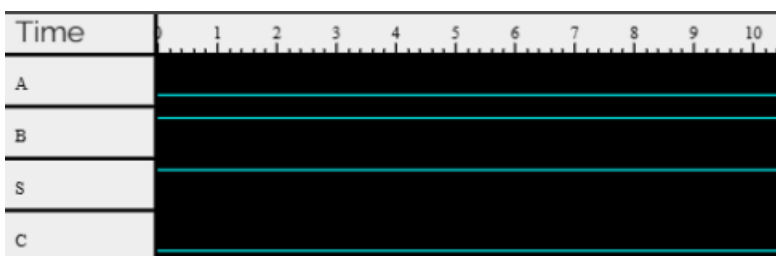
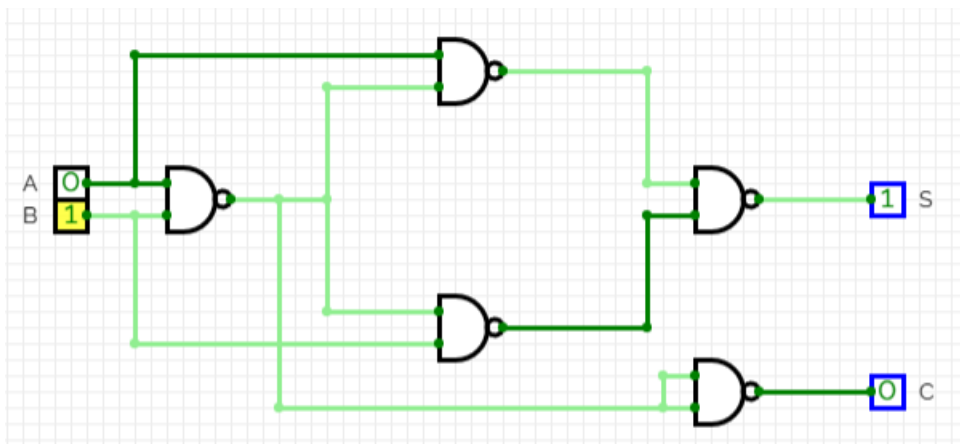
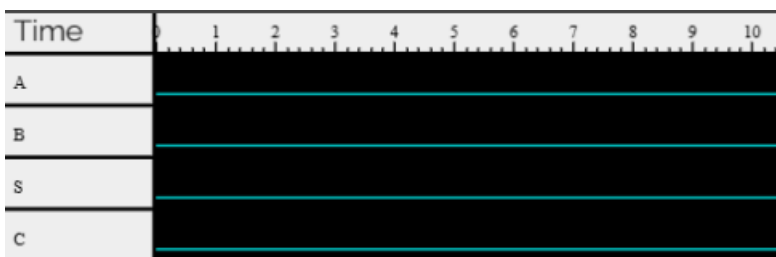
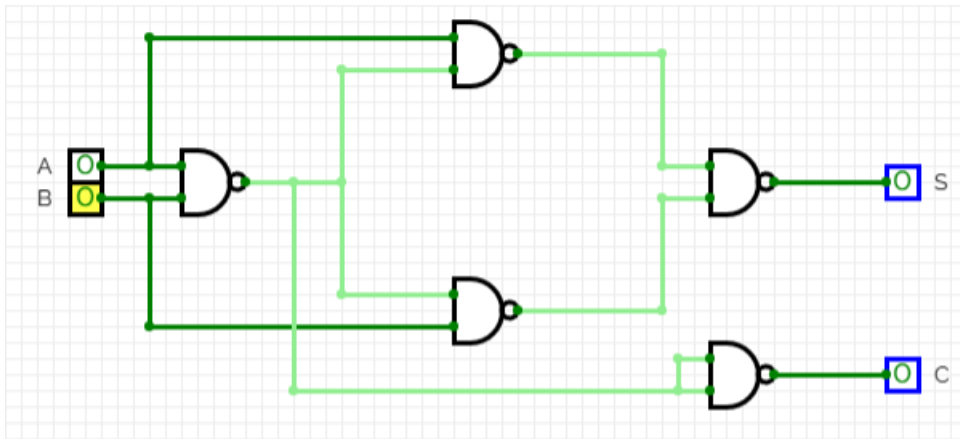
Time	0	1	2	3	4	5	6	7	8	9	10
F1											
F1											
F1											
F1											

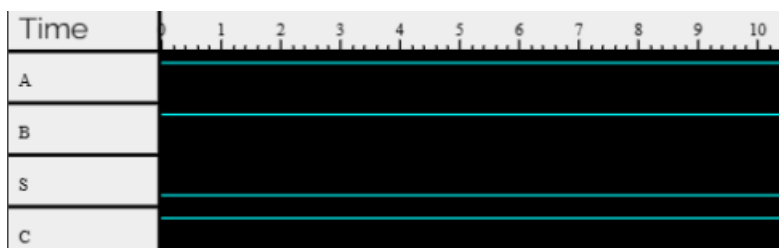
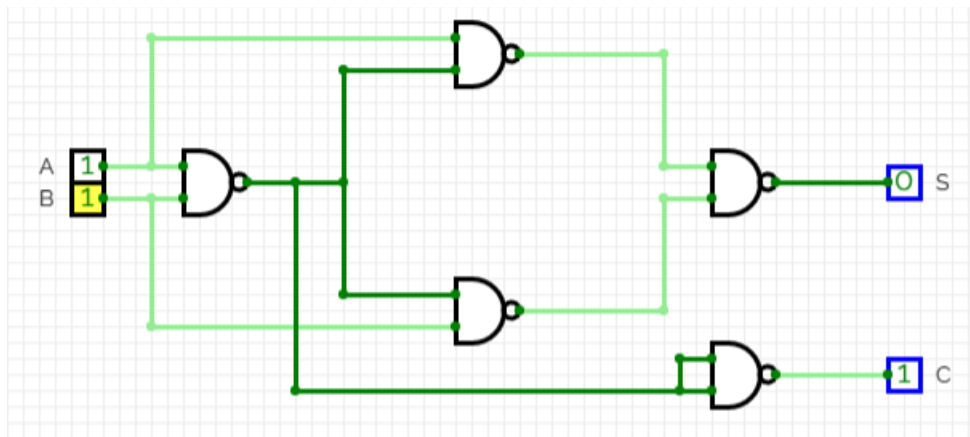
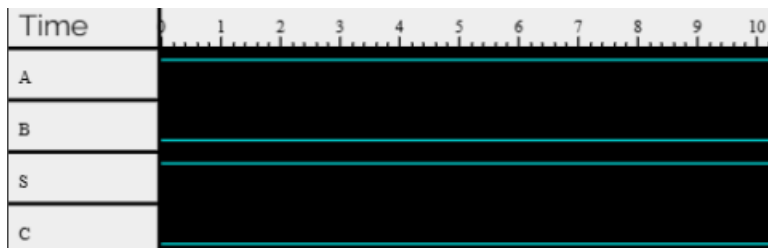
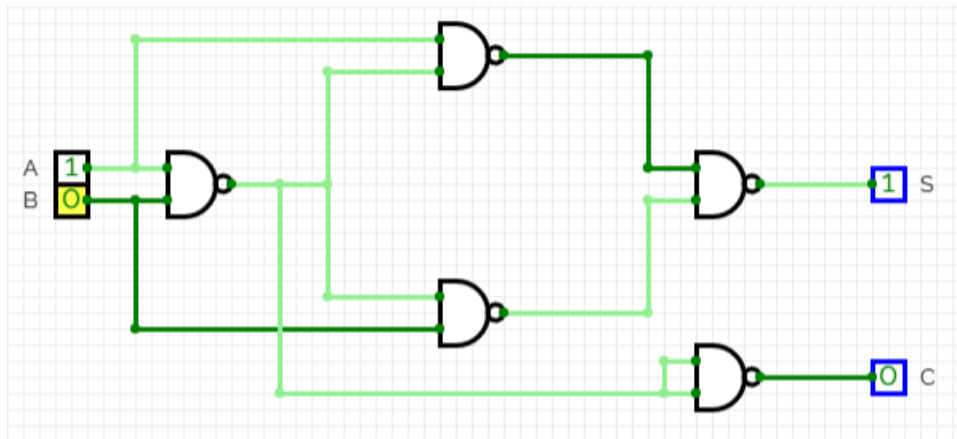


The image shows a software interface for data analysis. At the top, there is a horizontal time scale labeled 'Time' with major tick marks from 1 to 10. Below this scale are four horizontal tracks, each labeled 'F1' on the left. The tracks are currently empty, with only a thin blue line visible at the bottom of the first track.

Time	0	1	2	3	4	5	6	7	8	9	10
F1											
F1											
F1											
F1											

ii. NAND gate only





**RESULT:** The Half Adder is successfully designed and verified.