EXPERIMENT-6

AIM - To design the logical part of an ALU using MUX and decoder and study its working.

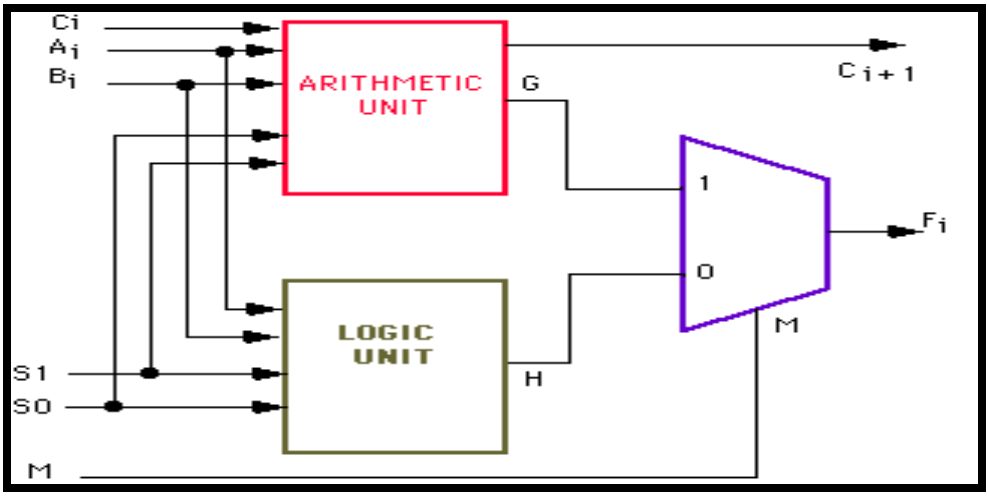
TOOLS USED - Circuitverse

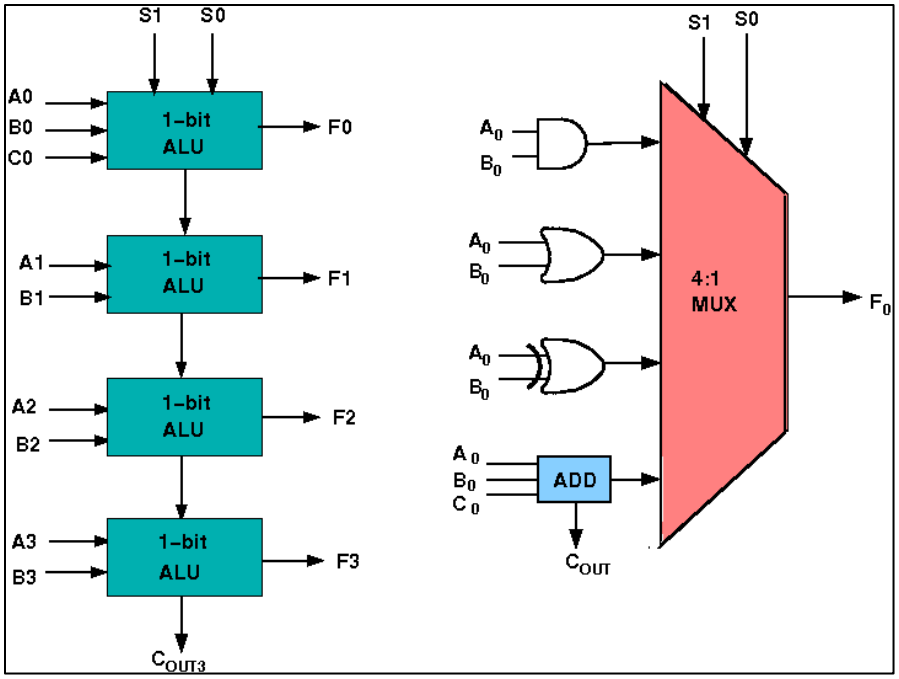
THEORY –

In computing, an arithmetic logic unit (ALU) is a digital circuit that performs arithmetic and logical operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain several ALUs. Mathematician John von Neumann proposed the ALU concept in 1945.

The ALU is divided into two units: an arithmetic unit (AU) and a logic unit (LU).

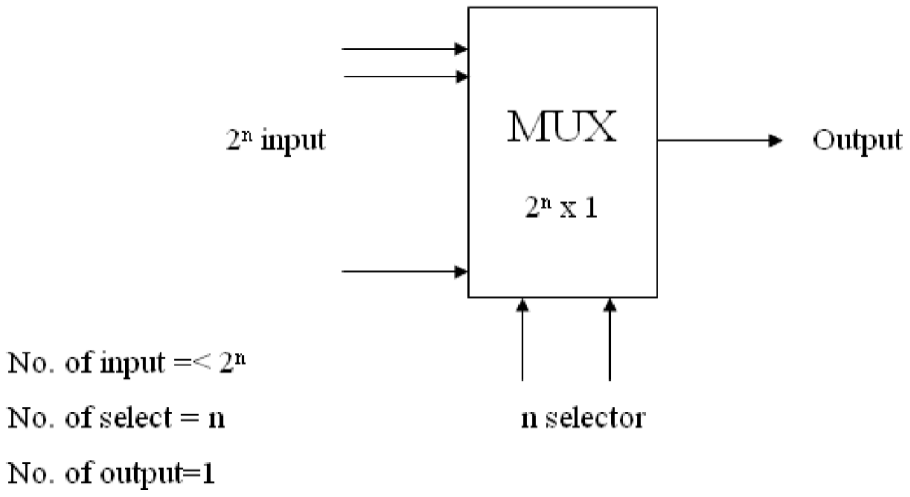
Below is a block diagram for an ALU:





MULTIPLEXER -

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. A multiplexer or MUX is a combinational circuit with more than one input line, one output line and more than one selection line. It selects any one of the many input lines an directs it to the output line which is controlled by selection/control lines.



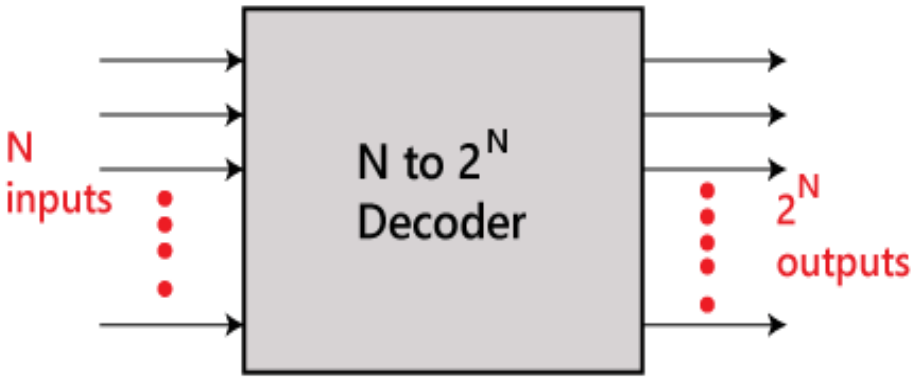
For N input lines, log n (base2) selection lines, or 2^n input lines, n selection lines are required

Multiplexers are classified into four types

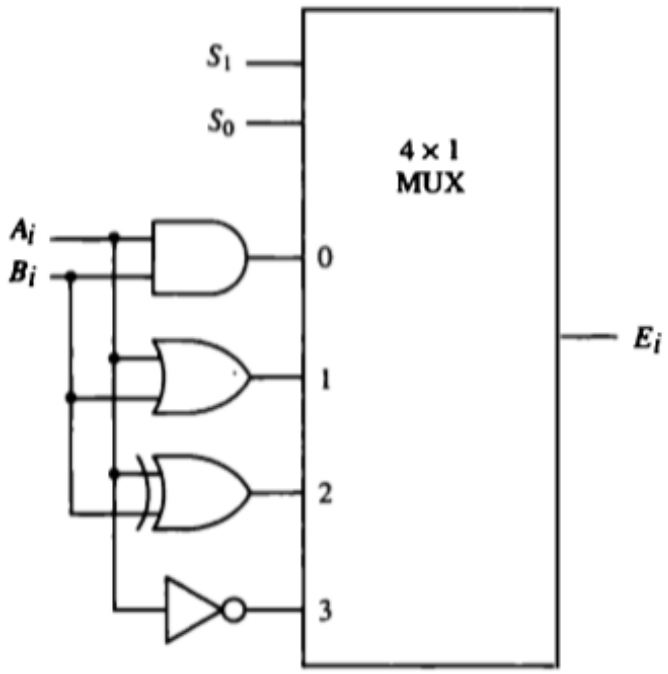
- 2:1 Mux
- 4:1 Mux
- 8:1 Mux
- 16:1 Mux

DECODER -

The combinational circuit that changes the binary information into 2N output lines is known as Decoders. The binary information is passed in the form of N input lines. The output lines define the 2N-bit code for the binary information. In simple words, the Decoder performs the reverse operation of the Encoder. At a time, only one input line is activated for simplicity. The produced 2N-bit output code is equivalent to the binary information.



Implementation of ALU using multiplexers -

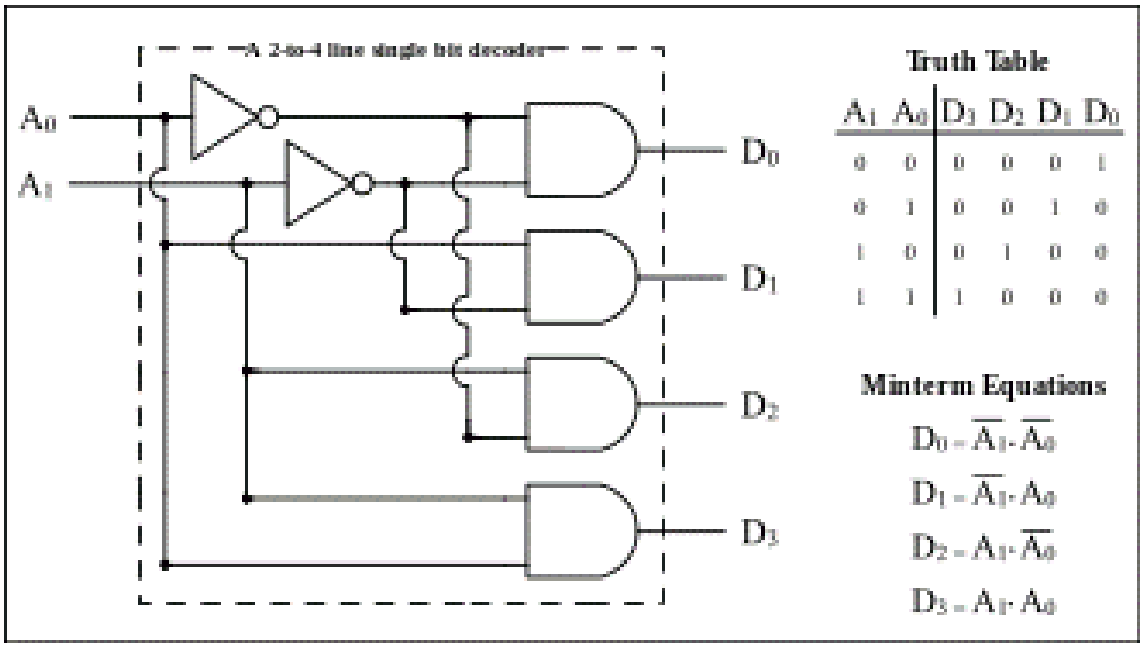


(a) Logic diagram

S_1	S_0	Output	Operation
0	0	$E = A \wedge B$	AND
0	1	$E = A \vee B$	OR
1	0	$E = A \oplus B$	XOR
1	1	$E = \overline{A}$	Complement

(b) Function table

Implementation of ALU using Decoder -



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$D_0 = \overline{A_1} \cdot \overline{A_0}$

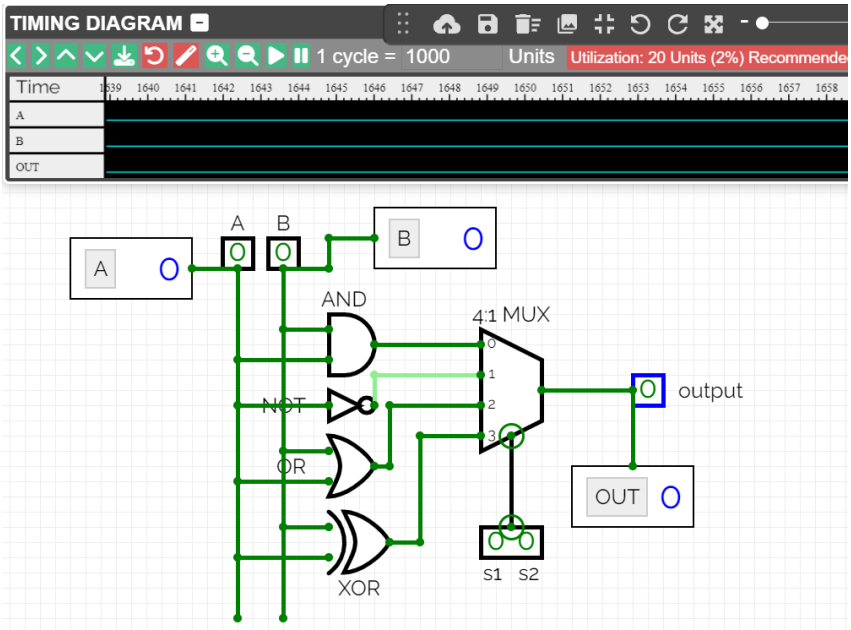
$D_1 = \overline{A_1} \cdot A_0$

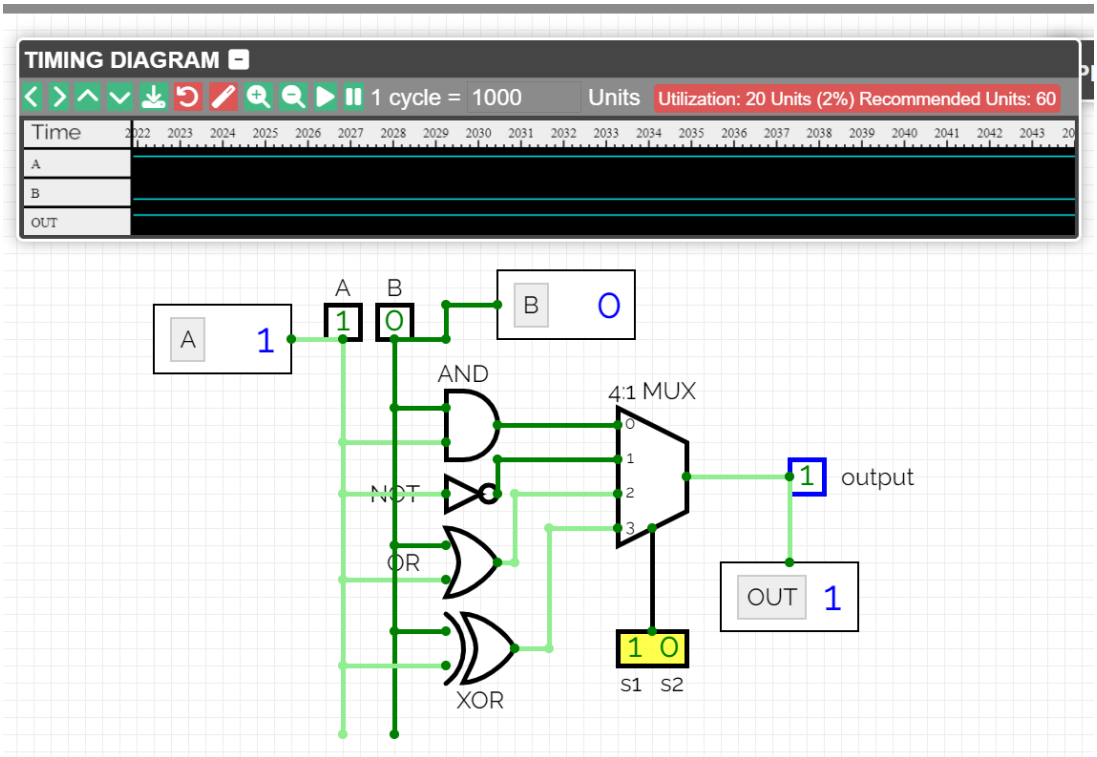
$D_2 = A_1 \cdot \overline{A_0}$

$D_3 = A_1 \cdot A_0$

OBSERVATIONS

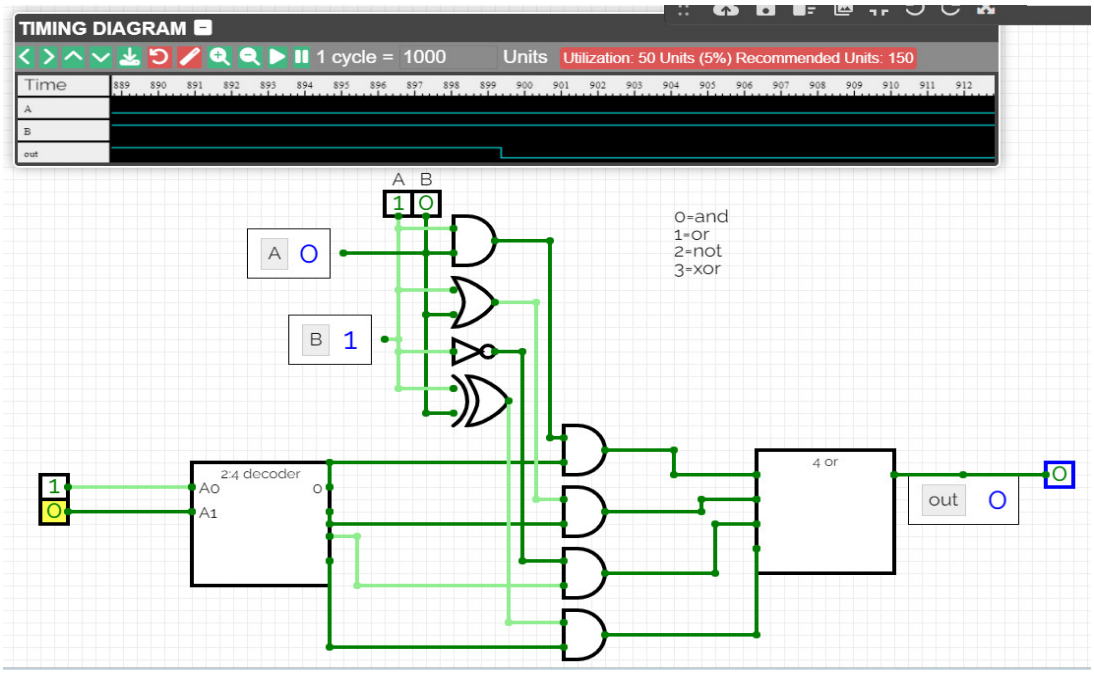
1) Using MUX



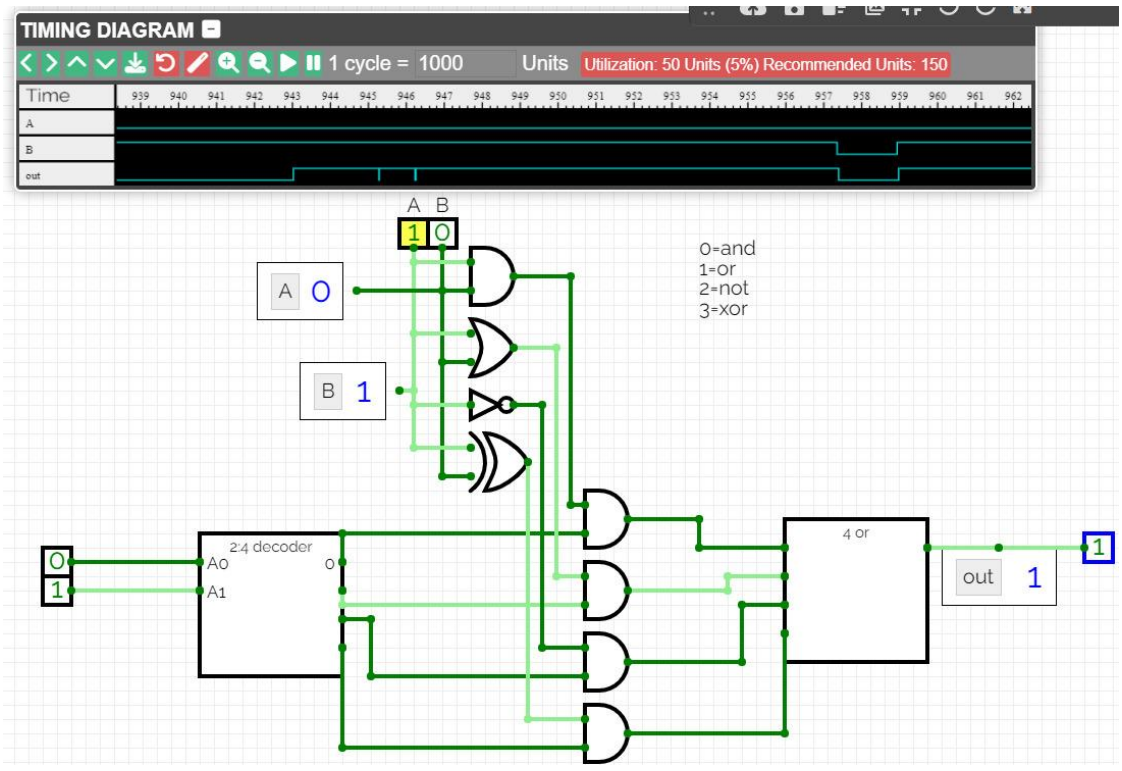


2) Using Decoder

- Not of A



- A or B



RESULT - Logical part of an ALU is designed and verified

Criteria	Total Marks	Marks Obtained	Comments
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		