Experiment 3

Aim - To verify the truth table of full adder by using XOR and NAND gates

Tools Used – Circuitverse

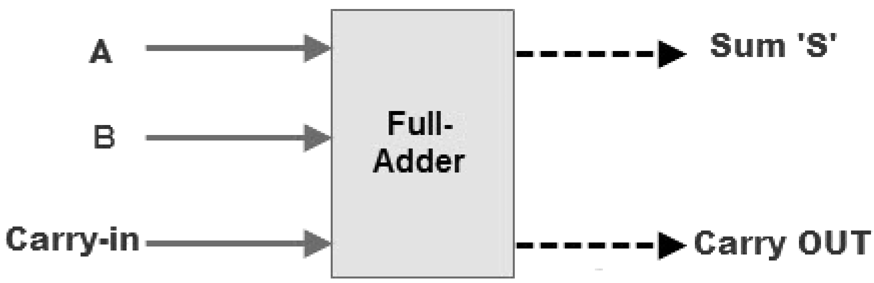
Theory

Adders are digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BCD), Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc.

Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

1)Full Adder

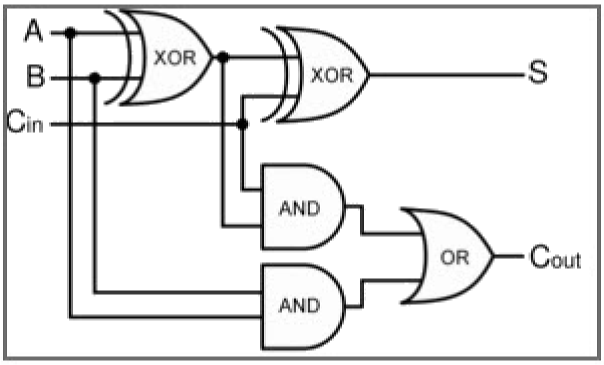
Full adder is a digital circuit used to calculate the sum of three binary bits. Full adders are complex and difficult to implement when compared to half adders. Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called 'Carry' – in generally represented by CIN. It calculates the sum of three bits along with the carry. The output carry is called Carry – out and is represented by Carry OUT. The block diagram of a full adder with A, B and CIN as inputs and S, Carry OUT as outputs is shown below.



Full Adder Block Diagram

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder Truth Table



Full Adder Logic Diagram

Based on the truth table, the Boolean functions for Sum (S) and Carry – out (COUT) can be derived using K – Map.

A \ BC_{IN}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

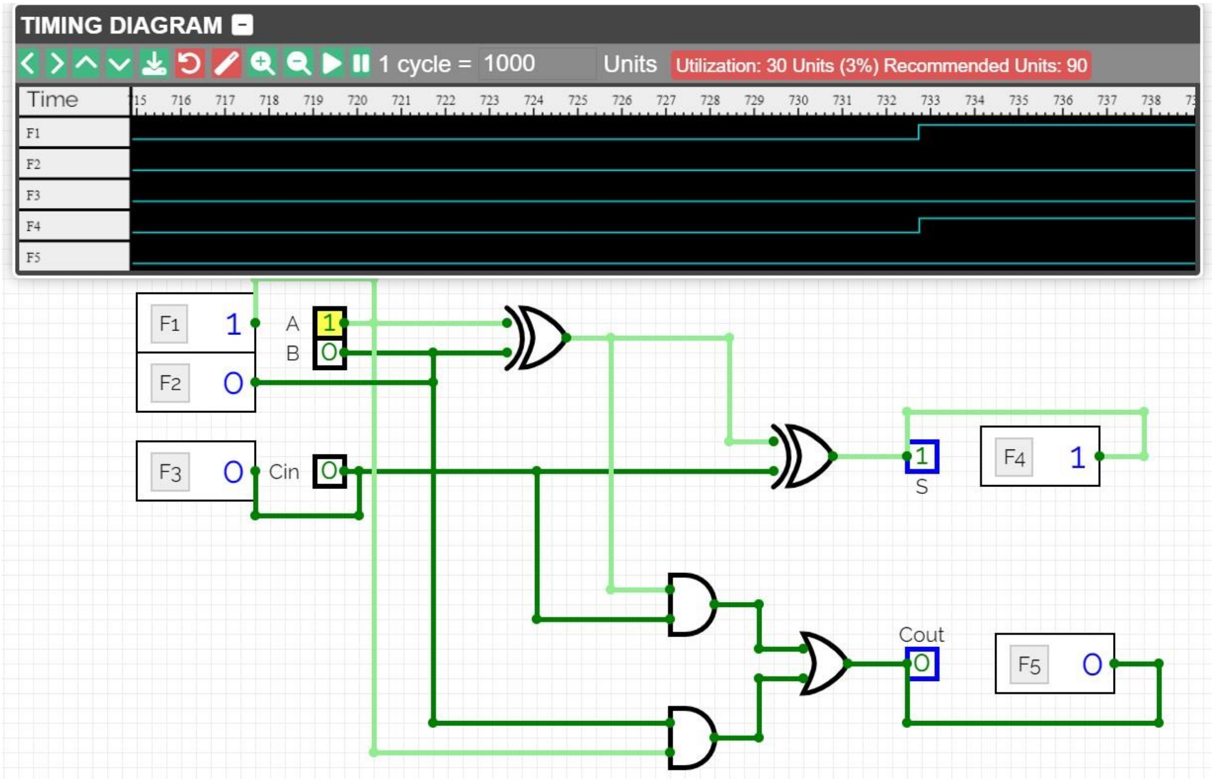
The K-Map simplified equation for sum is S = A'B'Cin + A'BCin' + ABCin

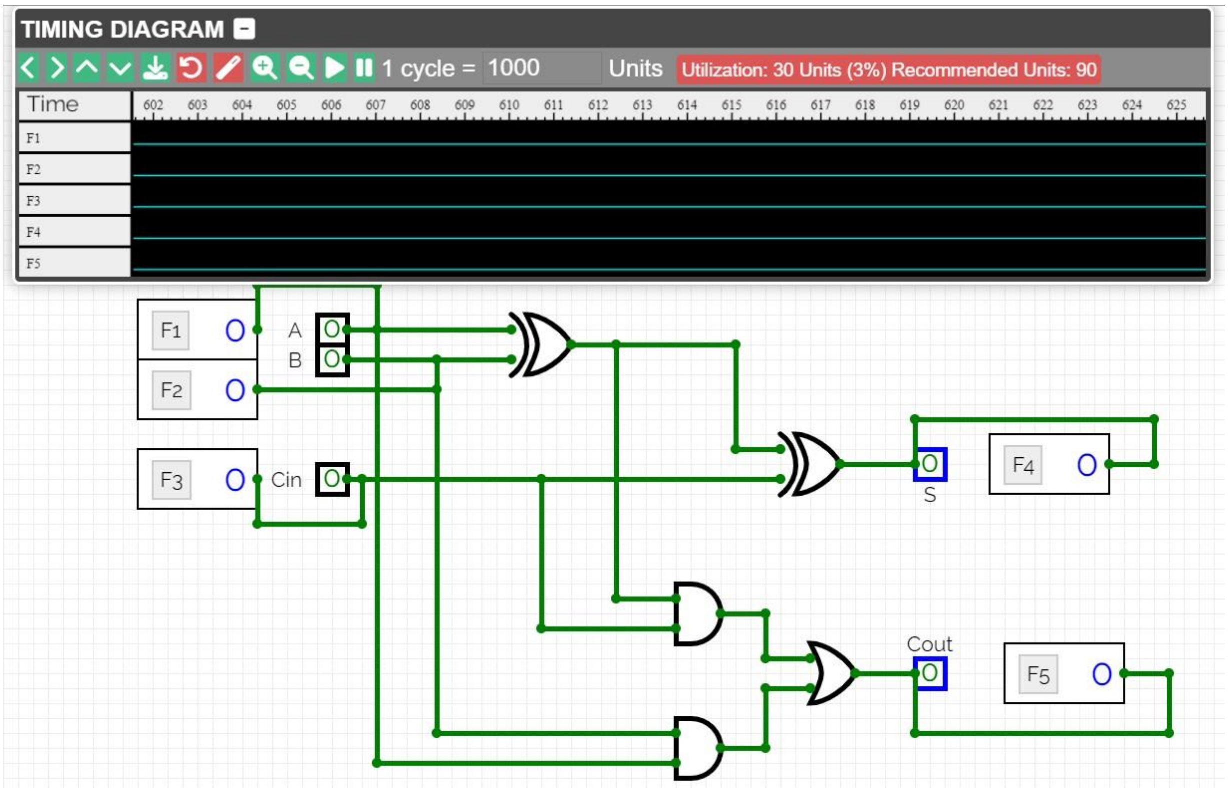
A \ BC_{IN}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

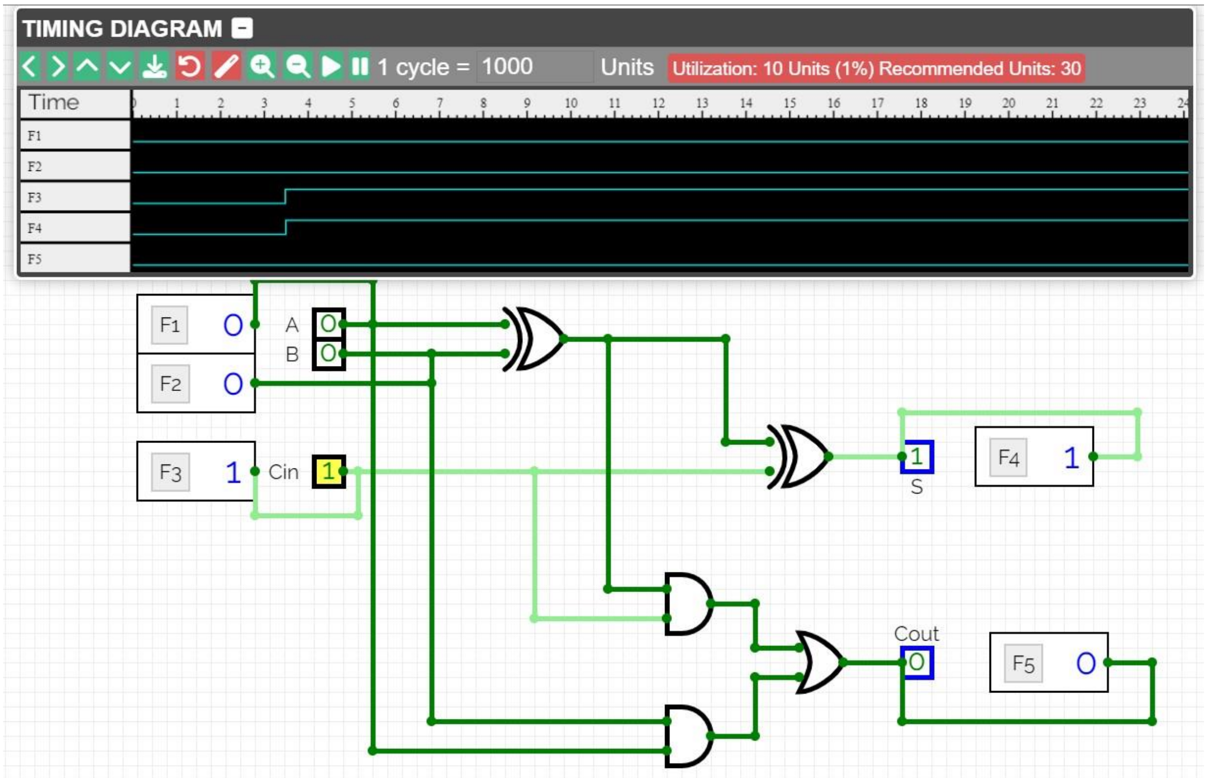
The K-Map simplified equation for COUT is COUT = AB + ACIN + BCIN

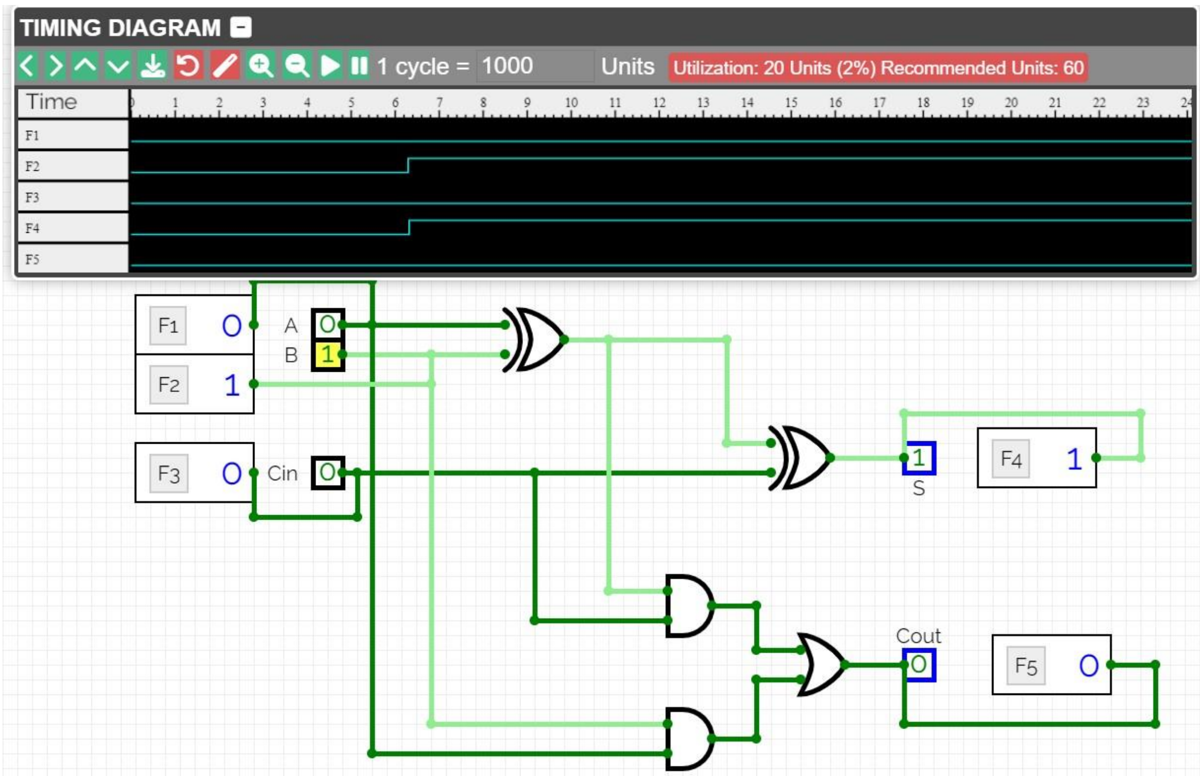
In order to implement a combinational circuit for full adder, it is clear from the equations derived above, that we need four 3-input AND gates and one 4-input OR gates for Sum and three 2-input AND gates and one 3-input OR gate for Carry – out.

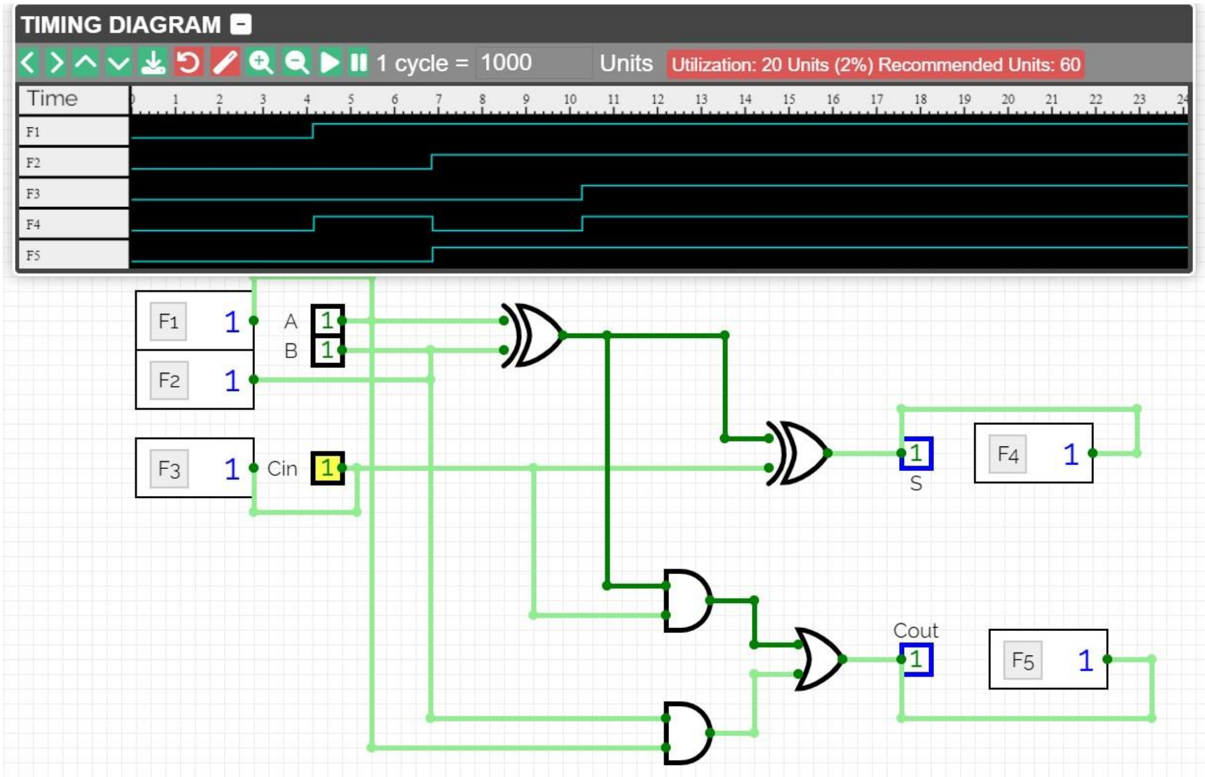
Observations

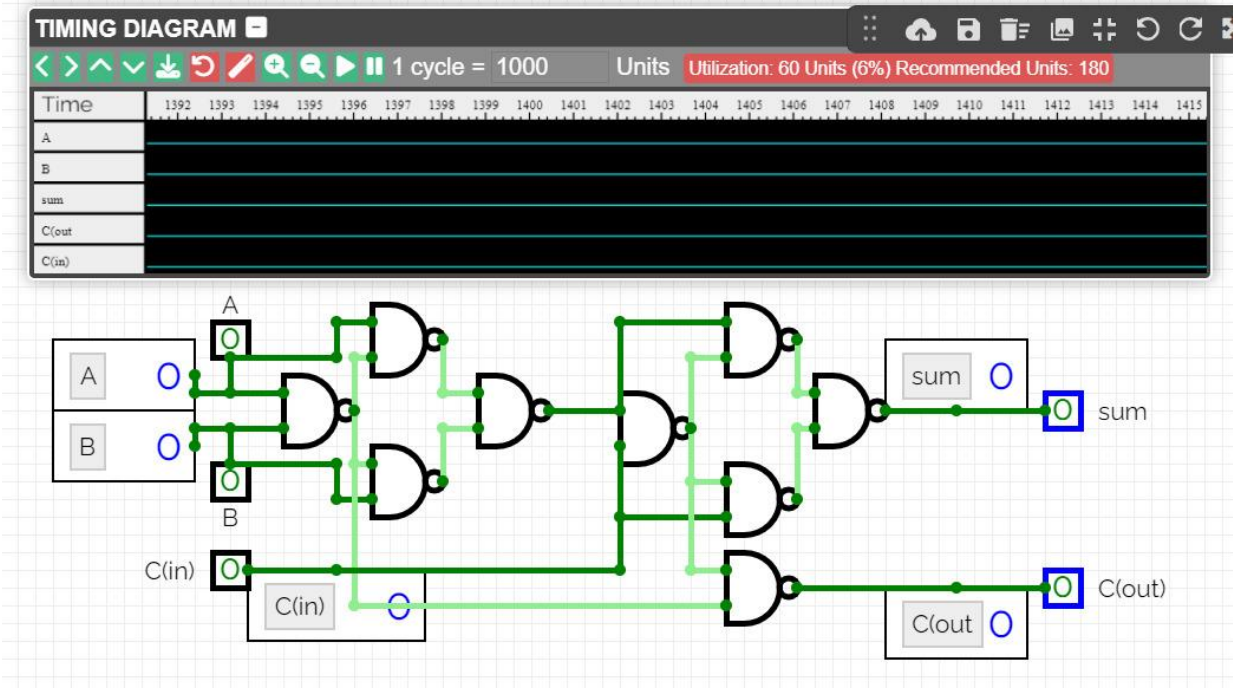


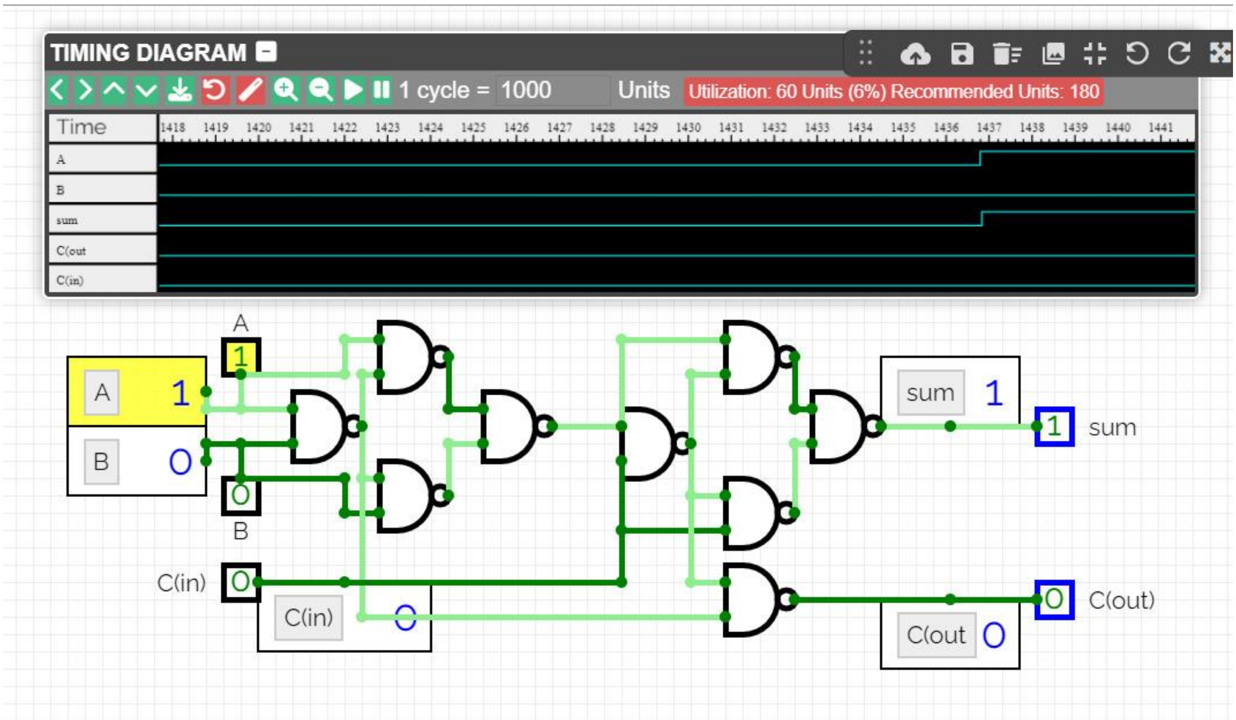


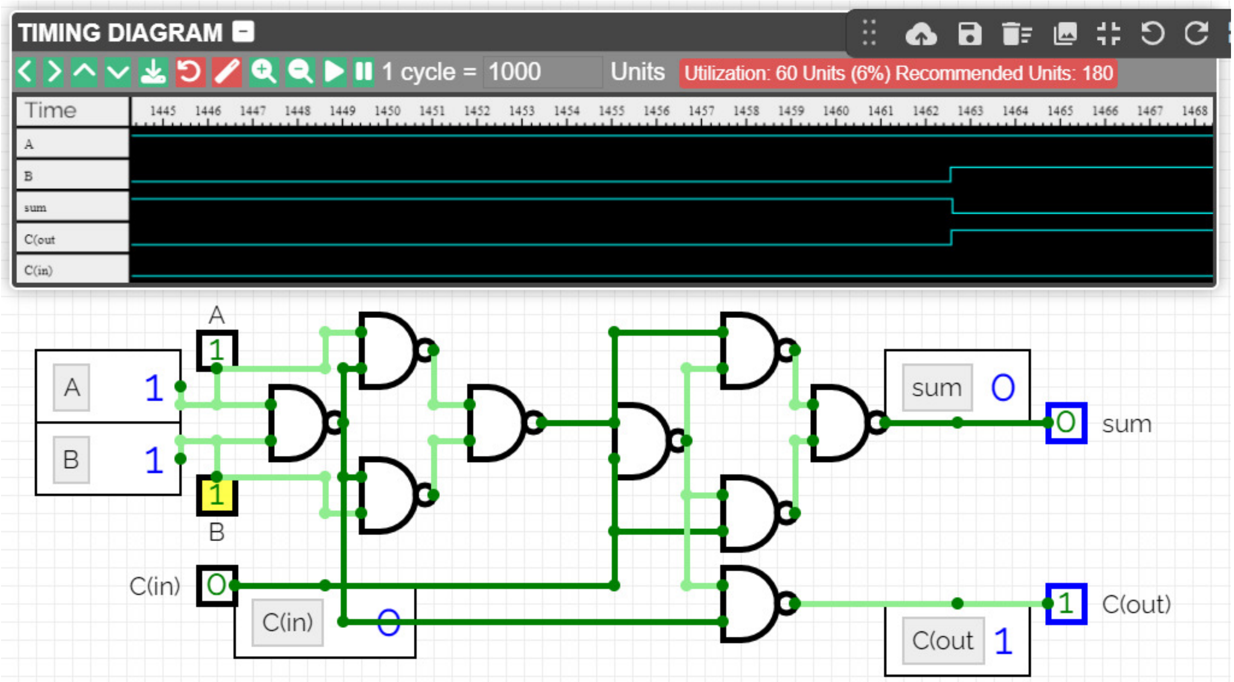

TIMING DIAGRAM
1 cycle = 1000 Units
Utilization: 10 Units (1%) Recommended Units: 30
Time
F1
F2
F3
F4
F5
F1 0
F2 0
F3 1
A
B
Cin
S
F4 1
Cout
F5 0

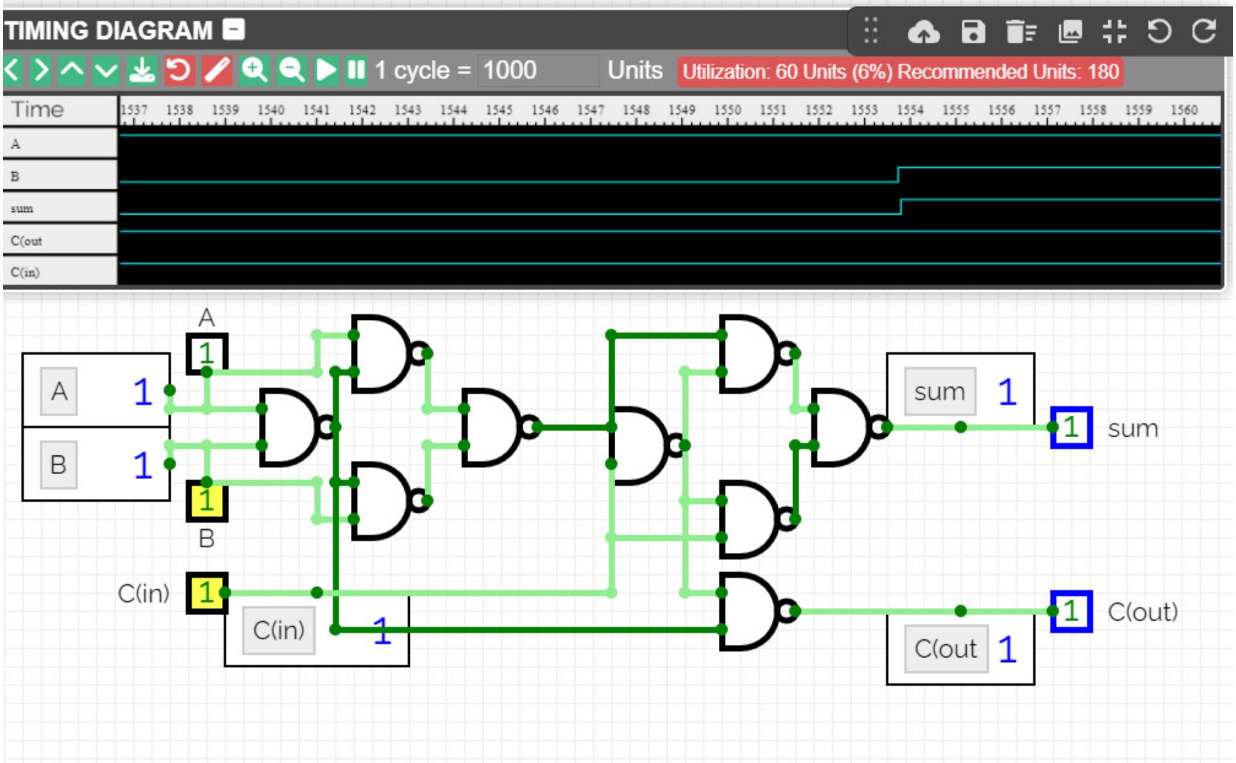

TIMING DIAGRAM
1 cycle = 1000 Units
Utilization: 20 Units (2%) Recommended Units: 60
Time
F1
F2
F3
F4
F5
F1 0
F2 1
F3 0
A
B
Cin
S
F4 1
Cout
F5 0


TIMING DIAGRAM
1 cycle = 1000
Units
Utilization: 20 Units (2%) Recommended Units: 60
Time
F1
F2
F3
F4
F5
A
B
Cin
S
Cout


TIMING DIAGRAM
1 cycle = 1000
Units
Utilization: 60 Units (6%) Recommended Units: 180
Time
A
B
sum
C(out
C(in)
C(in)
sum
C(out)


TIMING DIAGRAM
1 cycle = 1000 Units
Utilization: 60 Units (6%) Recommended Units: 180
Time
A
B
sum
C(out
C(in)
A 1
B 0
C(in) 0
sum 1
C(out 0
sum
C(out)


TIMING DIAGRAM
1 cycle = 1000 Units
Utilization: 60 Units (6%) Recommended Units: 180
Time
A
B
sum
C(out
C(in)
A 1
B 1
C(in) 0
sum 0
C(out 1
sum
C(out)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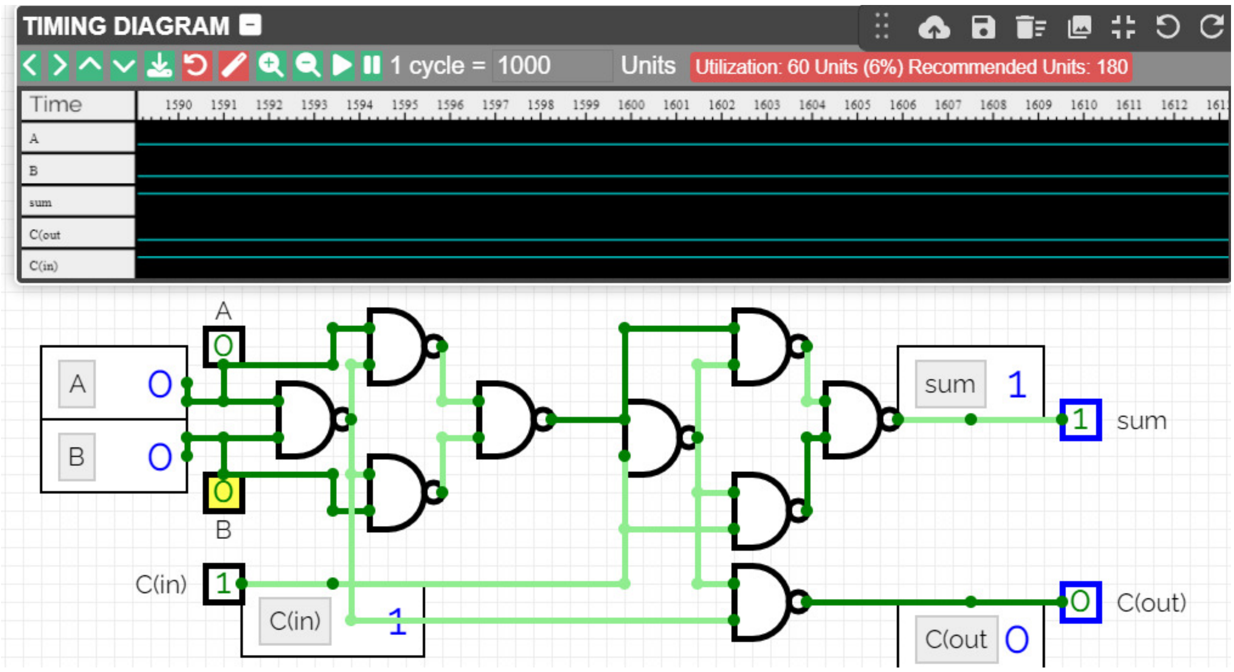
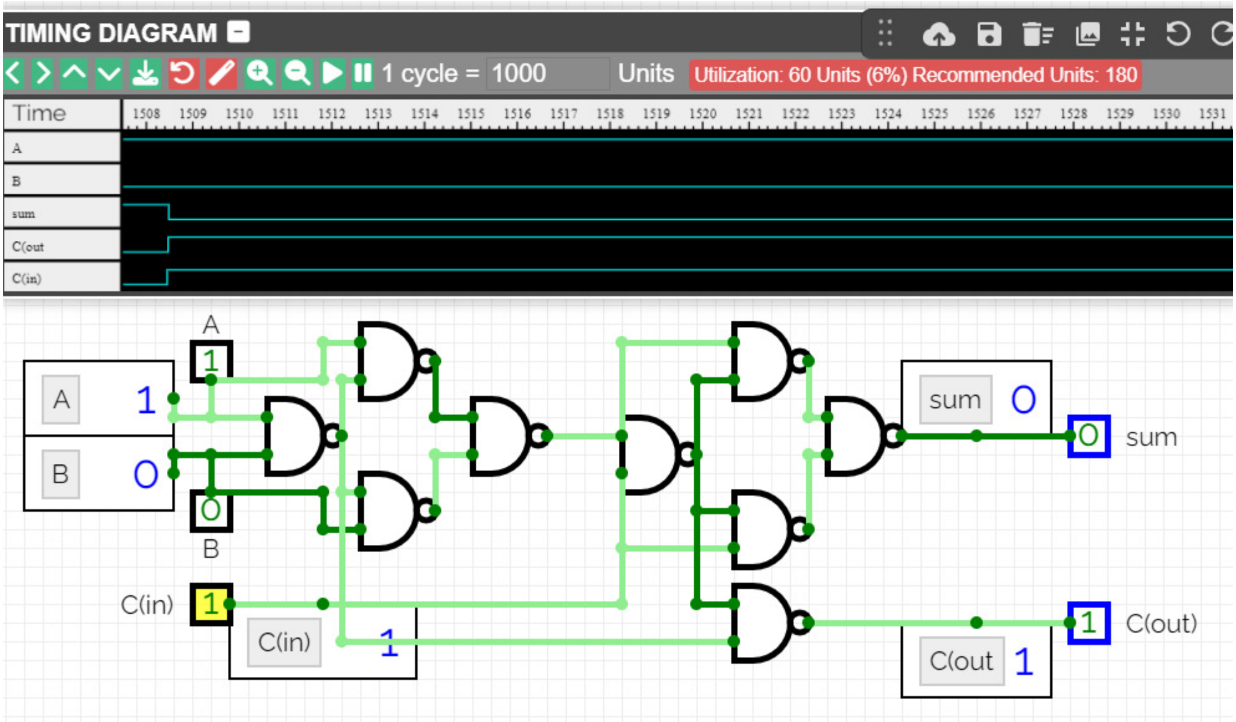
Utilization: 60 Units (6%) Recommended Units: 180
Time
A
B
sum
C(out
C(in)
A 1
B 1
C(in)
sum 1
sum
C(out)
C(out 1


TIMING DIAGRAM
1 cycle = 1000 Units
Utilization: 60 Units (6%) Recommended Units: 180
Time
A
B
sum
C(out
C(in)
A 0
B 0
C(in)
sum 1
sum
C(out)
C(out 0



Result – Full adder are successfully constructed and verified