EXPERIMENT-5

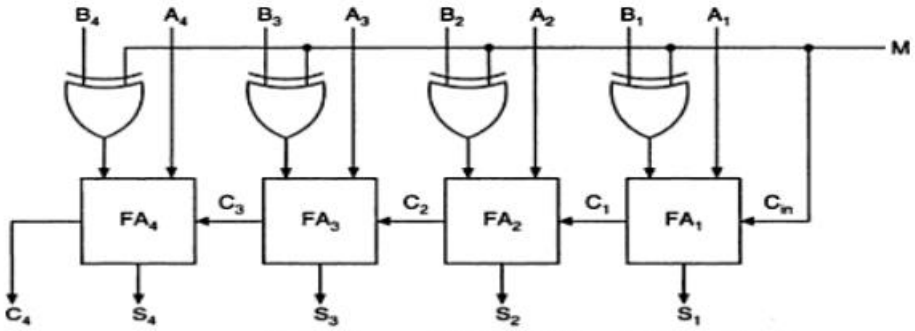
AIM: To design a parallel Adder-Subtractor.

TOOL USED: Circuit Verse

THEORY: In a 4-bit adder-subtractor, the addition and subtraction operations are combined into one circuit with one common binary adder. This is done by including an X-OR gate with each Full-Adder. The mode input M controls the operation. When M=0, the circuit is an adder, and when M=1, the circuit becomes a subtractor. Each X-OR gate receives input M and one of the inputs B.

When M=0, $B \oplus 0 = B$ the Full-Adder receives the value of B, the input carry is 0 and the circuit performs A+B.

When $B \oplus 1 = B'$ and C1=1, the B inputs are complemented and a 1 is through the input carry. The circuit performs operation A plus the 2‘s complement of B.



Logic diagram of a 4-bit binary adder-subtractor.

Example of Binary Subtraction:

0111-0101 (7-5)

=1101 (2)

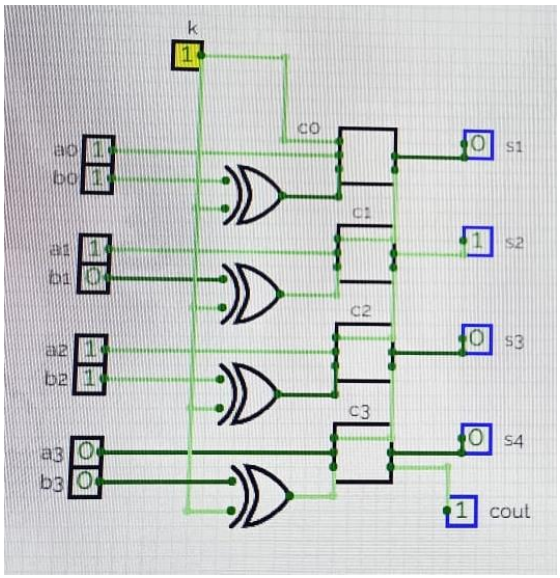
Example of Binary Addition:

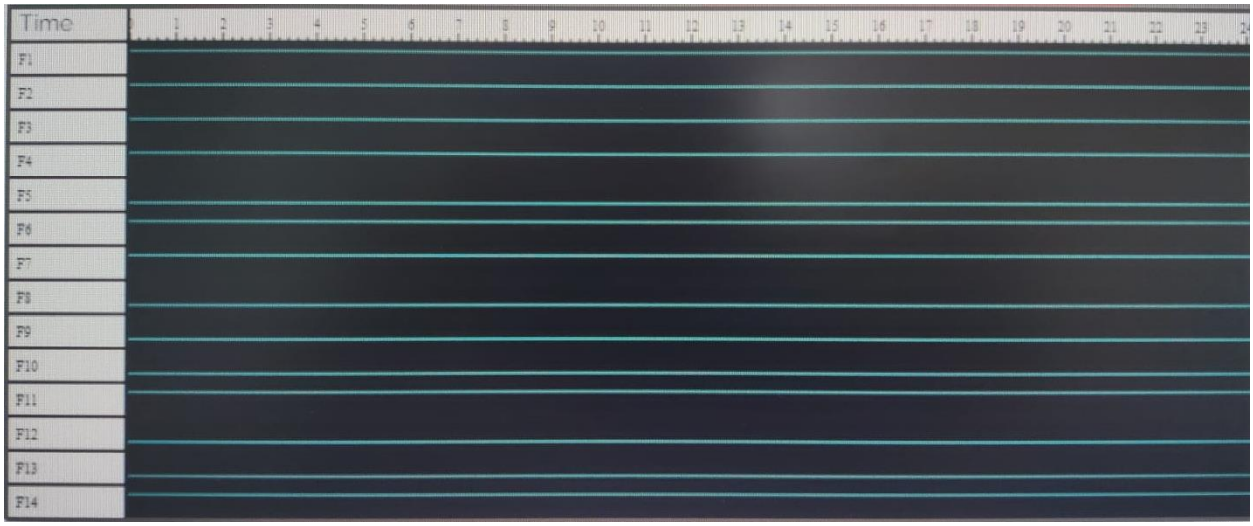
0111+0101 (7+5)

=1100 (12)

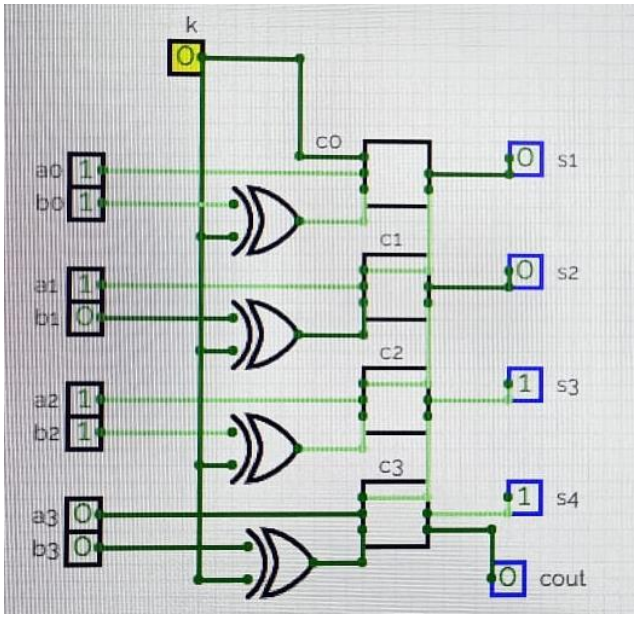
OBSERVATIONS:

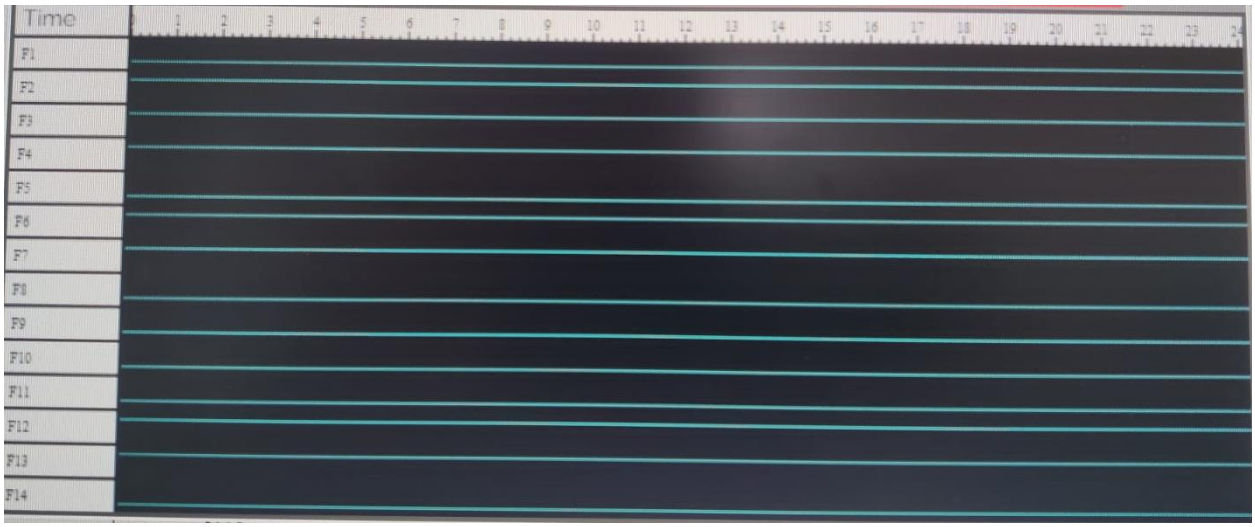
a) For Subtraction –





b) For Addition –





RESULT: The Parallel Adder-Subtractor is successfully designed and verified.

Criteria	Total Marks	Marks Obtained	Comments
Concept (A)	2		
Implementation (B)	2		
Performance (C)	2		
Total	6		