Lab Report

Min Han

06.02.2024

CPE 324-03

Laboratory #3

Introduction

: The goal in this lab experiment is to investigate digital hardware prototyping using the Terasic DE2-115 FPGA board and solderless breadboarding techniques. The area of expertise is the design and validation of digital systems. Using Small Scale Integration (SSI) integrated circuits (ICs) for combinational logic, we progress to sequential designs using MSI ICs. The experiment teaches basic breadboarding techniques, how to interface external digital components with the DE2-115 board, and the important distinctions between synchronous and asynchronous control signals.

<Experiment 1>

Experiment Description:

The first experiment in the lab guide measures the voltage levels of digital circuits, with a particular emphasis on the distinctions between the complementary metal-oxide-semiconductor (CMOS) and transistor-transistor (TTL) logic families. In order to demonstrate the unique electrical properties of both logic families and the implications for digital design, this experiment walks us through the process of measuring and comparing the High and Low voltage levels of each logic family using a digital multimeter. The goal is to comprehend the voltage thresholds in TTL and CMOS circuits that define the logical states of High (1) and Low (0), as this will lay the groundwork for developing and debugging digital systems.

Results:

Record the measurement: DE-155 supplied from the 5v pin = 5.1 v

Record the measurement: DE-155 supplied from the 3v3 pin = 3.3 v

<Experiment 2>

Experiment Description:

The second experiment is devoted to assessing the timing properties of digital circuits. This entails measuring the propagation delay periods of TTL and CMOS logic gates using an oscilloscope. By timing the time it takes for a signal to go from input to output, the experiment seeks to illustrate how quickly these gates can function. This emphasizes the significance of timing concerns in the design and analysis of digital systems, which is essential for comprehending the constraints and functionality of digital circuits in real-world applications.

Results:

1) Voltages comes from the DE2-115 Switch SW0

when SW0 is down

voltage =0, Logic Probe reported logic level = 0

when SW0 is up

voltage =5, Logic Probe reported logic level = 1

2) Voltages comes from the selected 74LS04 inverter

When SW0 is down

74LS04 Output Voltage = 5v, LED light (on/off) = 0n

When SW0 is up

74LS04 Output Voltage = 0v, LED light (on/off) = Off

In your laboratory report, comment on these voltage levels. For a given Logic High or Low are the voltage levels from outputs of the DE2-115 the same as those for the TTL logic? Does TTL logic use positive or negative logic? Explain.

: The DE2-115 board, which makes use of FPGAs, may not have output voltage levels that precisely match those of conventional TTL logic circuits. Transistor-Transistor logic, or TTL logic for short, uses positive logic in which a logical "1" (true) is represented by a high voltage level (usually around 5V) and a logical "0" (false) by a low voltage level (0V).

<Experiment 3>

Experiment Description:

The purpose of Experiment #3 is to examine signal integrity, with particular attention to problems like ringing and reflections. This experiment examines the effects of overshoot, undershoot, and reflections on signal transitions in digital circuits using an oscilloscope, with a focus on high-speed digital designs. We will learn how to use an oscilloscope to detect these problems and comprehend how they affect the quality of digital signals, highlighting the significance of appropriate circuit design and termination methods for dependable digital communication.

Results:

Logic Probe Mode	VIL	VIH
TTL	0.7 V	2.3 V
CMOS	1.69 V	3.41 V

In your report comment on whether the DE2-115 VLTTL output voltage values fall within the acceptable region for a TTL to interpret it as a logic high or a logic low. Also in your report review the complete data sheet on the 74LS04 and compare the readings you obtained with those that are expected

DE2-115 FPGA VLTTL Output Voltage Levels: The FPGA on the DE2-115 board can be set up for different logic level standards, such as Low Voltage TTL (LVTTL). Typically, a logic high is at 3.3V and a logic low is at 0V for LVTTL levels.

TTL Logic High and Low Levels: Voltages above roughly 2V are interpreted as high (logic 1) in traditional TTL logic, and voltages below approximately 0.8V are interpreted as low (logic 0).

74LS04 Hex Inverter Specifications: A hex inverter chip with TTL logic levels of operation is the 74LS04. The minimum voltage recognized as a high input (V_IH) and the maximum voltage recognized as a low input (V_IL), which are crucial for guaranteeing compatibility, are specified in its datasheet.

A TTL logic, like the 74LS04, would interpret the FPGA's output, which is configured for LVTTL levels (3.3V high, 0V low), as comfortably falling within this range.

<Experiment 4>

Experiment Description:

The fourth experiment explores crosstalk and how it affects digital circuits. We must watch and examine how signals in one circuit can unintentionally affect those in adjacent circuits, resulting in "crosstalk," or unintentional interactions. We gain an understanding of the significance of circuit layout and shielding techniques in minimizing these undesirable effects, particularly in environments with dense electronic packaging or high-speed digital signals, by conducting experiments that demonstrate the conditions under which crosstalk occurs and its impact on signal integrity.

Results:

Inputs		Measured Voltage	LP-560 Logic Probe Indicated TTL logic Level
SW1	SW0		
0	0	5V	1
0	1	0V	0
1	0	0V	0
1	1	0V	0

Are there any voltage levels that are in the so called forbidden region where the voltage present at the input of the logic probe has a value that is in between the range interpreted as a valid logic high or a logic low for TTL logic? If so indicate the cases where these occur. Why do you think that in most cases it is not wise to connect outputs together.

: The term "forbidden region" in TTL logic describes voltage levels that are not easily distinguished as either a logical high or logical low. This region usually falls between 0.8V and 2.0V for TTL. This range of voltages is confusing and can result in incorrect logic state interpretations. When outputs from various TTL devices are connected directly to one another without the necessary interfacing, this situation may arise. If the outputs are not precisely synchronized, or if one device tries to drive the line high while another tries to drive it low, there may be potential conflicts or undefinable states.

In general, output connections should be avoided as they may cause short circuits or harm to the devices if the logic states of the devices disagree. It may also result in the combined output.

<Experiment 5>

Experiment Description:

The fifth experiment investigates the reduction of electromagnetic interference (EMI) in digital circuits. With the aid of an oscilloscope and an AM radio, this experiment aims to locate EMI sources and quantify the impact they have on electrical equipment. The intention is to illustrate the significance of electromagnetic compatibility (EMC) design principles, including the use of EMI filters, shielding, and grounding.

Results:

Inputs		Measured Voltage	LP-560 Logic Probe Indicated TTL logic Level
SW1	SW0		
0	0	5V	1
0	1	0V	0
1	0	0V	0
1	1	0V	0

Are there any voltage levels that are in the forbidden TTL region? If so indicate the cases where these occur. What is the logic function that can be expressed by the table above if we assume positive logic? If TTL logic was negative logic instead of positive logic what logic function would this truth table represent?

: Voltages in the "forbidden region," or between 0.8V and 2.0V in TTL logic, can lead to ambiguity when interpreting signals. In an ideal world, the outputs of the DE2-115 would stay outside of this range to guarantee distinct logic levels. In positive logic, logical operations (like AND and OR) are defined by a truth table according to high and low voltages; in negative logic, however, these interpretations and their corresponding functions are reversed.

<Experiment 6>

Experiment Description:

Completing a table for the 74LS125 circuit is the sixth experiment, which shows an uncommon scenario in which outputs may be connected. Understanding the operation and uses of tri-state logic devices in digital circuits—particularly in CPU memory architectures—is made possible by this experiment. It highlights the special capacity of tri-state devices to exist in a high, low, or high-impedance state by contrasting the tri-state logic with open-collector and open-drain topologies.

Results:

Inputs				Measured Voltage	LP-560 Logic Probe Indicated TTL logic Level
SW3	SW2	SW1	SW0		
0	0	0	0	x	x
0	0	0	1	0V	0
0	0	1	1	5V	1
1	0	0	1	0V	0
0	1	0	0	5V	1
1	1	0	0	0V	0
0	1	1	0	5V	1

Inputs				Measured Voltage	LP-560 Logic Probe Indicated TTL logic Level
SW3	SW2	SW1	SW0		
0	1	0	1	Hi-z	x
1	1	1	0	0V	0
1	1	1	1	5V	1
1	0	1	1	Hi-z	x
1	0	1	0	5V	1

Report on how tri-state differs from open-collector or open-drain configurations. Where and how are tri-state devices used in many CPU memory architectures?

: In contrast to open-collector or open-drain configurations, tri-state devices offer three different output states: high, low, and high-impedance (Z). In contrast, open-collector/drain configurations only provide two output states: active low and high-impedance. Tri-state devices, which enable numerous devices to share a single bus without interfering with one another, are commonly used in CPU memory architectures for bus management. One way to effectively disconnect a device from the bus when not in use is to set its output to high impedance, which allows another device to communicate with it without interference. This makes it easier for complex digital systems to manage peripherals and transfer data efficiently.

<Experiment 7>

Experiment Description:

Experiment #7 looks at signal integrity in synchronous designs on crosstalk and electromagnetic radiation problems. It entails watching clock signals produced by the DE2-115 platform and analyzing signal forms, frequencies, and electromagnetic interference with an oscilloscope, an amplified speaker, and an AM radio. The objective is to comprehend how parasitic effects cause high-speed signals to diverge from ideal circumstances and how noise and radiation can be introduced into a circuit via conductive channels that are physically adjacent to one another, hence impacting circuit performance.

Results:

<Case1>

Oscilloscope Settings

Volts per division: 1 V

Time per division: 100ms

Measured

Peak-to-peak Voltage: 0~5 V

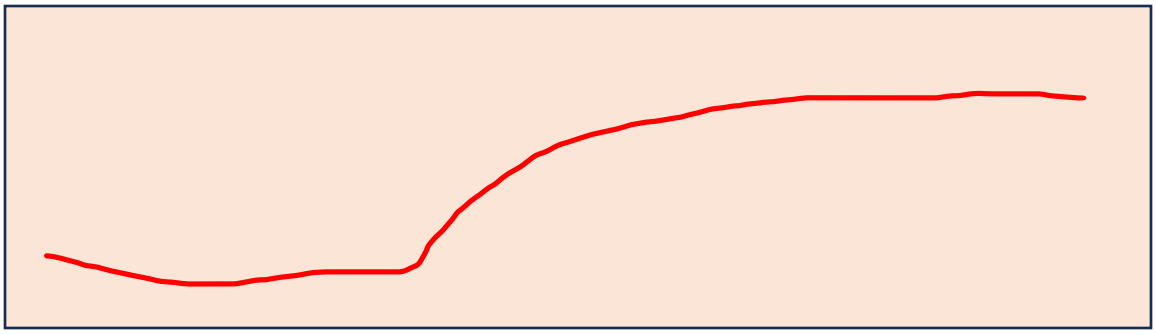
Frequency: very low

Speaker Observation: Extremely low sound

DE2-115 HEX6 7seg LED Observation: Pattern changes with each clock pulse

Electromagnetic Transmission Observations: electromagnetic emissions was less pronounced at very low frequencies.

Wavefrom Observations: The amplitude is almost nonexistent and the line is uniform.



<Case2>

Oscilloscope Settings

Volts per division: 1V~ 2V

Time per division: 30ms

Measured

Peak-to-peak Voltage: 5V

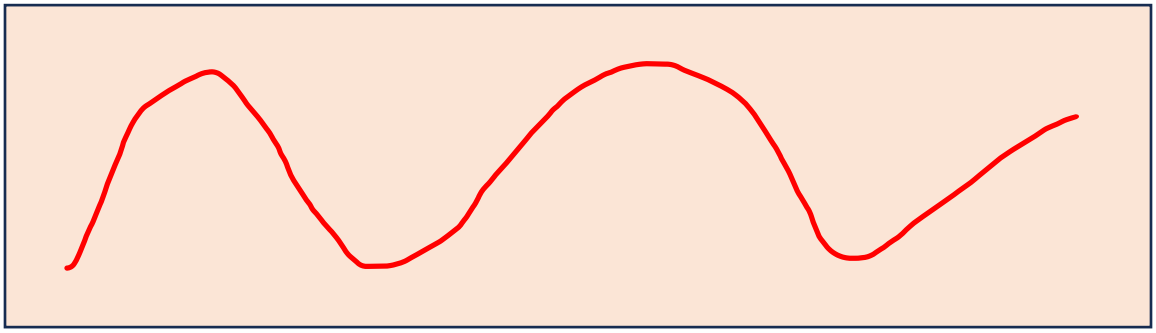
Frequency: uniformed amplitude

Speaker Observation: infrequent

DE2-115 HEX6 7seg LED Observation: shows a little faster binary count

Electromagnetic Transmission Observations: more noticeable interference effects

Wavefrom Observations: uniformed amplitude



<Case3>

Oscilloscope Settings

Volts per division: 2V

Time per division: 5ms

Measured

Peak-to-peak Voltage: 5.5 V

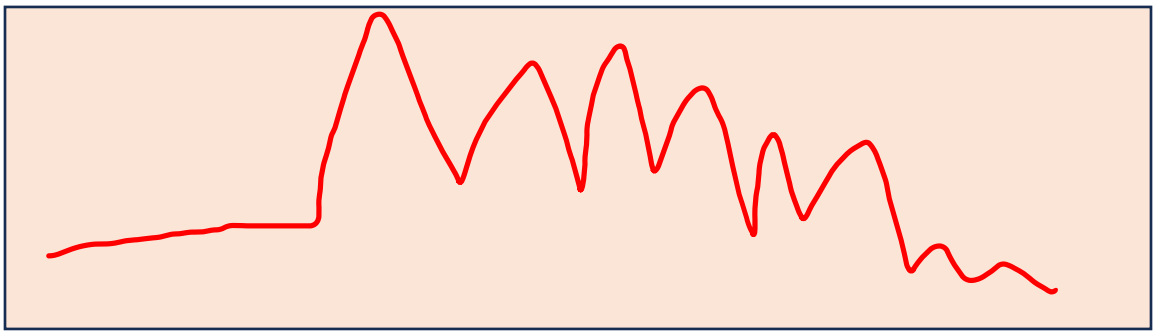
Frequency: Higher frequency

Speaker Observation: Sounds regular beeps.

DE2-115 HEX6 7seg LED Observation: Fast binary count

Electromagnetic Transmission Observations: electromagnetic emissions and potential interference become more pronounced.

Wavefrom Observations: The graph keeps bounces.



<Case4>

Oscilloscope Settings

Volts per division: 1V

Time per division: 500 us

Measured

Peak-to-peak Voltage: 5 V

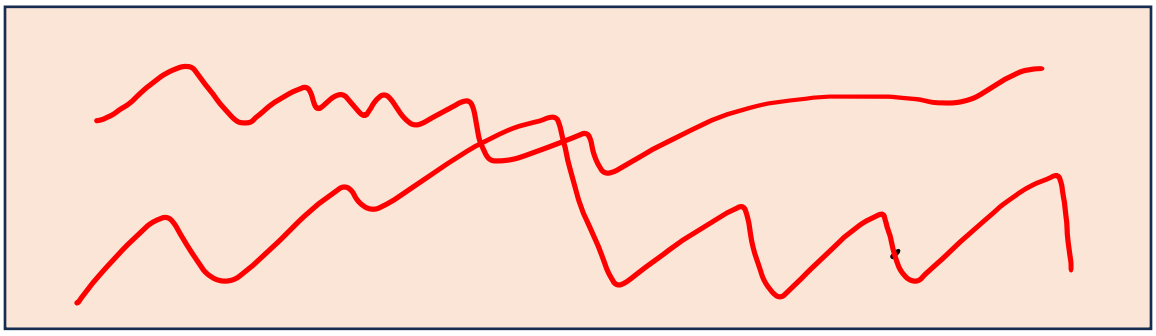
Frequency: Fast

Speaker Observation: Too fast and cant even hear well

DE2-115 HEX6 7seg LED Observation: Super Fast binary count

Electromagnetic Transmission Observations: More electromagnetic emissions and potential interference become more pronounced.

Wavefrom Observations: The graph keeps vibrates and moving so fast.



Conclusion:

In conclusion, Lab 3 provided valuable insights into the electrical and timing characteristics of digital circuits, focusing on the behavior of TTL logic levels and the functionality of tri-state, open-collector, and open-drain configurations. Through hands-on experimentation, the lab reinforced the importance of understanding voltage levels, signal integrity, and the role of these configurations in CPU memory architectures.