

Features

- **Stable 3.8 MHz GBWP Over Temperature Range**
- **Stable 3.8 MHz GBWP in V_{CM} from 0-V to V_{DD}**
- **Very Low Supply Current: 130 μ A per Amplifier**
- **Unity Gain Stable for Any Capacitive Load**
- **Offset Voltage: 3.0 mV Maximum**
- **Offset Voltage Temperature Drift: 0.6 μ V/°C**
- **Input Bias Current: 1 pA Typical**
- **THD+Noise: -115 dB at 1kHz, -99 dB at 10kHz**
- **High CMRR/PSRR: 120 dB**
- **Beyond the Rails Input Common-Mode Range**
- **Outputs Swing to within 5 mV of Each Rail**
- **No Phase Reversal for Overdriven Inputs**
- **Drives 2 k Ω Resistive Loads**
- **Shutdown Current: 0.2 μ A (TP1561N)**
- **Supply Voltage Range:**
 - Single +2.1 V to +6.0 V Supply
 - Or Dual ± 1.05 V to ± 3.0 V Supplies
- **-40°C to 125°C Operation Temperature Range**
- **ESD Rating: 8KV – HBM, 2KV–CDM and 500V–MM**
- **Green, Popular Type Package**

Applications


- Multimedia Audio
- Headphone Drivers
- LCD Drivers
- Photo Diode Pre-amp
- Medical Equipments
- Portable Devices
- ASIC Input or Output
- Sensor Interfaces

Description

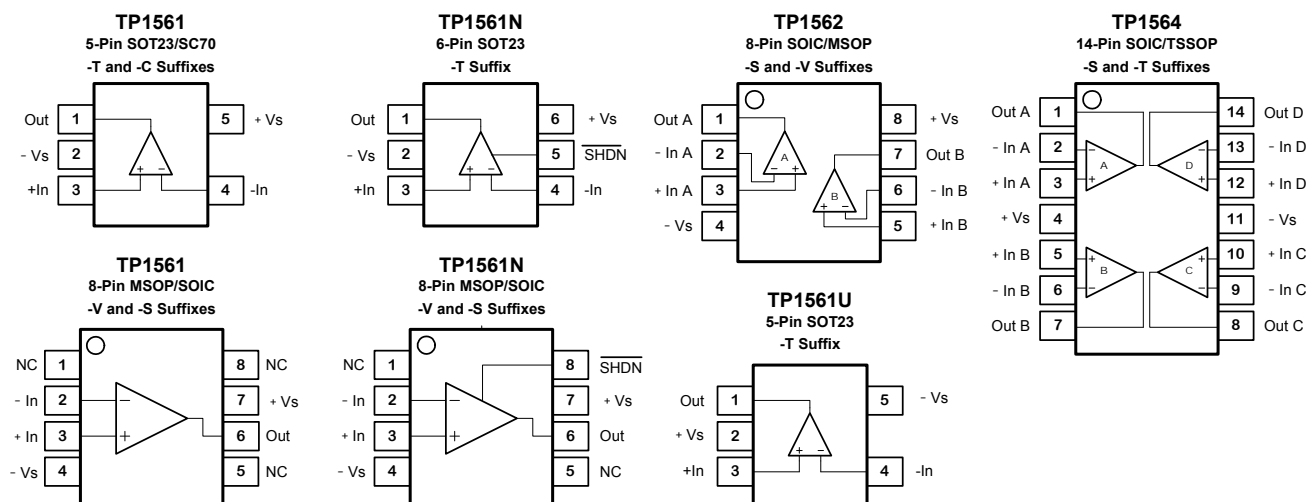
The TP156x series are CMOS single, dual, and quad RRIO op-amps with low offset, low power and stable high frequency response. They incorporate 3PEAK's proprietary and patented design techniques to achieve very good AC performance with 3.8MHz bandwidth, 3.6V/ μ s slew rate and low distortion while drawing only 130 μ A of quiescent current per amplifier. The input common-mode voltage range extends 300mV beyond V^- and V^+ , and the outputs swing rail-to-rail. The TP156x family can be used as plug-in replacements for many commercially available op-amps to reduce power and improve input/output range and performance.

The TP156x Op-amps are unity gain stable with any capacitive load. They operate from either single +2.1V to +6.0V supply or dual ± 1.05 V to ± 3.0 V supplies. Analog trim and calibration routine reduce input offset voltage to below 3.0mV, and proprietary precision temperature compensation technique makes offset voltage temperature drift at 0.6 μ V/°C. Adaptive biasing and dynamic compensation enables the TP156x to achieve 'THD +Noise' for 1kHz/10kHz 2V_{PP} signal at -115dB/ -99dB. Beyond the rails input and rail-to-rail output characteristics allow the full power-supply voltage to be used for signal range.

The combination of features makes the TP156x ideal choices for audio amplification of computers, sound ports, and other consumer Audio. The TP156x Op-amp is very stable, and it is capable of driving heavy capacitive loads such as those found in LCDs. The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

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Pin Configuration (Top View)



Absolute Maximum Ratings ^{Note 1}

Supply Voltage: $V^+ - V^-$	7.5V	Output Short-Circuit Duration ^{Note 3}	Indefinite
Input Voltage.....	$V^- - 0.5$ to $V^+ + 0.5$	Operating Temperature Range.....	-40°C to 125°C
Input Current: +IN, -IN, SHDN ^{Note 2}	±10mA	Maximum Junction Temperature.....	150°C
SHDN Pin Voltage.....	V^- to V^+	Storage Temperature Range.....	-65°C to 150°C
Output Current: OUT.....	±45mA	Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	500	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP1561	TP1561-TR	5-Pin SOT23	Tape and Reel, 3000	A6TYW ⁽¹⁾
	TP1561-CR	5-Pin SC70	Tape and Reel, 3000	A6CYW ⁽¹⁾
	TP1561-VR	8-Pin MSOP	Tape and Reel, 3000	A61V
	TP1561-SR	8-Pin SOIC	Tape and Reel, 4000	A61S
TP1561U	TP1561U-TR	5-Pin SOT23	Tape and Reel, 3000	A6UYW ⁽¹⁾
TP1561N	TP1561N-TR	6-Pin SOT23	Tape and Reel, 3000	A6NYW ⁽¹⁾
	TP1561N-SR	8-Pin SOIC	Tape and Reel, 4000	A61NS
	TP1561N-VR	8-Pin MSOP	Tape and Reel, 3000	A61NV
TP1562	TP1562-SR	8-Pin SOIC	Tape and Reel, 4000	A62S
	TP1562-VR	8-Pin MSOP	Tape and Reel, 3000	A62V
TP1564	TP1564-SR	14-Pin SOIC	Tape and Reel, 2500	A64S
	TP1564-TR	14-Pin TSSOP	Tape and Reel, 3000	A64T

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

5V Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 27^\circ\text{C}$.
 $V_{\text{SUPPLY}} = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{SUPPLY}}/2$, $R_L = 100\text{k}\Omega$, $C_L = 100\text{pF}$, V_{SHDN} is unconnected.

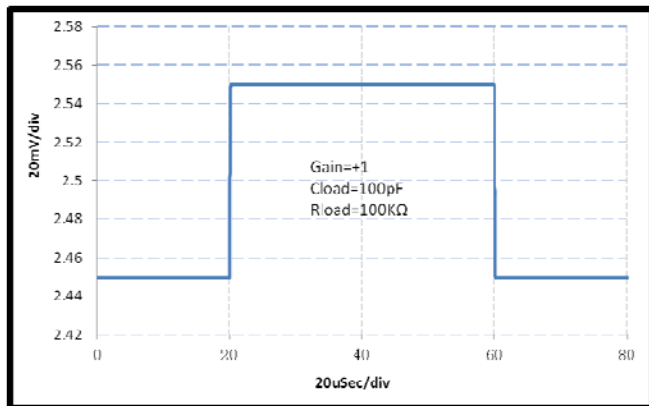
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V_{\text{DD}}/2$	● -3.0	± 0.1	+3.0	mV
$V_{\text{OS TC}}$	Input Offset Voltage Drift			0.6		$\mu\text{V}/^\circ\text{C}$
I_{B}	Input Bias Current			1.0		pA
I_{OS}	Input Offset Current			1.0		pA
V_{n}	Input Voltage Noise	$f = 0.1\text{Hz to } 10\text{Hz}$		2.4		$\mu\text{V}_{\text{P-P}}$
e_{n}	Input Voltage Noise Density	$f = 1\text{kHz}$ $f = 10\text{kHz}$		27 14		$\text{nV}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance			> 100		G Ω
C_{IN}	Input Capacitance	Differential Common Mode		2.0 3.5		pF
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = 0.1\text{V to } 4.9\text{V}$	● 80	120		dB
V_{CM}	Common-mode Input Voltage Range		● $V^- - 0.3$		$V^+ + 0.3$	V
PSRR	Power Supply Rejection Ratio		● 80	120		dB
A_{VOL}	Open-Loop Large Signal Gain	$V_{\text{OUT}} = 2.5\text{V}$, $R_{\text{LOAD}} = 100\text{k}\Omega$	● 80	110		dB
		$V_{\text{OUT}} = 0.1\text{V to } 4.9\text{V}$, $R_{\text{LOAD}} = 100\text{k}\Omega$	● 72	102		dB
$V_{\text{OL}}, V_{\text{OH}}$	Output Swing from Supply Rail	$R_{\text{LOAD}} = 100\text{k}\Omega$		5		mV
R_{OUT}	Closed-Loop Output Impedance	$G = 1$, $f = 1\text{kHz}$, $I_{\text{OUT}} = 0$		0.4		Ω
R_{O}	Open-Loop Output Impedance	$f = 100\text{kHz}$, $I_{\text{OUT}} = 0$		2.6		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current		45		mA
V_{DD}	Supply Voltage		2.1		6.0	V
I_{Q}	Quiescent Current per Amplifier		●	130	190	μA
$I_{\text{Q(off)}}$	Supply Current in Shutdown ^{Note 1}			0.2		μA
I_{SHDN}	Shutdown Pin Current ^{Note 1}	$V_{\text{SHDN}} = 0.5\text{V}$		-0.15		μA
		$V_{\text{SHDN}} = 1.5\text{V}$		-0.15		μA
I_{LEAK}	Output Leakage Current in Shutdown ^{Note 1}	$V_{\text{SHDN}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$ $V_{\text{SHDN}} = 0\text{V}$, $V_{\text{OUT}} = 5\text{V}$		-20 20		pA
V_{IL}	SHDN Input Low Voltage ^{Note 1}	Disable	●		0.5	V
V_{IH}	SHDN Input High Voltage ^{Note 1}	Enable	● 1.0			V
t_{ON}	Turn-On Time ^{Note 1}	SHDN Toggle from 0V to 5V		20		μs
t_{OFF}	Turn-Off Time ^{Note 1}	SHDN Toggle from 5V to 0V		20		μs
PM	Phase Margin	$R_{\text{LOAD}} = 100\text{k}\Omega$, $C_{\text{LOAD}} = 100\text{pF}$		66		$^\circ$
GM	Gain Margin	$R_{\text{LOAD}} = 100\text{k}\Omega$, $C_{\text{LOAD}} = 100\text{pF}$		-15		dB
GBWP	Gain-Bandwidth Product	$f = 1\text{kHz}$		3.8		MHz
t_{s}	Settling Time, 1.5V to 3.5V, Unity Gain Settling Time, 2.45V to 2.55V, Unity Gain	0.1%		0.7		μs
		0.01%		0.8		
		0.1%		0.1		
		0.01%		0.2		
SR	Slew Rate	$A_{\text{V}} = 1$, $V_{\text{OUT}} = 1.5\text{V to } 3.5\text{V}$, $C_{\text{LOAD}} = 100\text{pF}$, $R_{\text{LOAD}} = 100\text{k}\Omega$		3.6		V/ μs
FPBW	Full Power Bandwidth ^{Note 2}	$2V_{\text{P-P}}$		500		kHz
THD+N	Total Harmonic Distortion and Noise	$f=1\text{kHz}$, $A_{\text{V}}=1$, $R_L=100\text{k}\Omega$, $V_{\text{OUT}} = 2V_{\text{PP}}$		-115		dB
		$f=10\text{kHz}$, $A_{\text{V}}=1$, $R_L=100\text{k}\Omega$, $V_{\text{OUT}} = 2V_{\text{PP}}$		-99		

Note 1: Specifications apply to the TP1561N with shutdown.

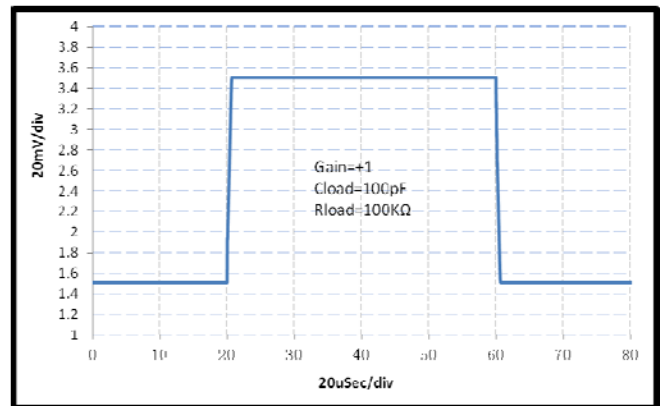
Note 2: Full power bandwidth is calculated from the slew rate $\text{FPBW} = \text{SR}/\pi \cdot V_{\text{P-P}}$.

Typical Performance Characteristics

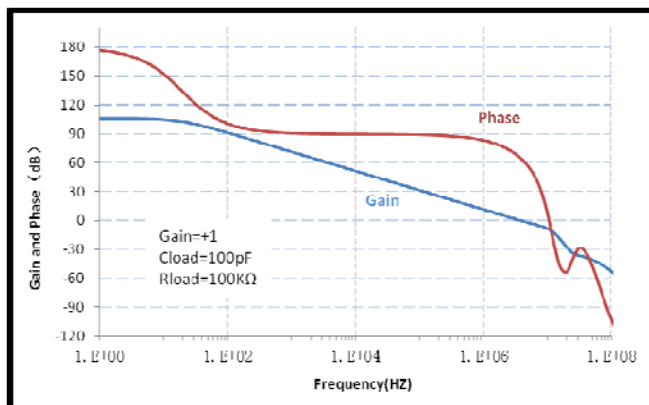
Small-Signal Step Response, 100mV Step



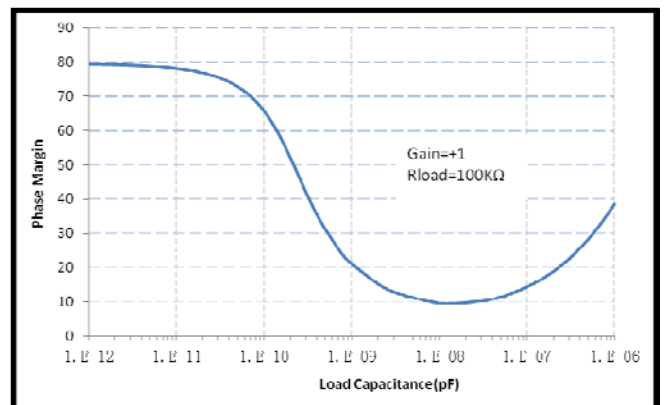
Large-Signal Step Response, 2V Step



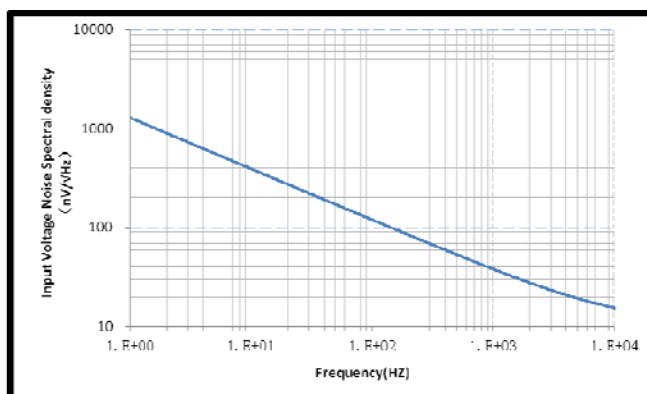
Open-Loop Gain and Phase



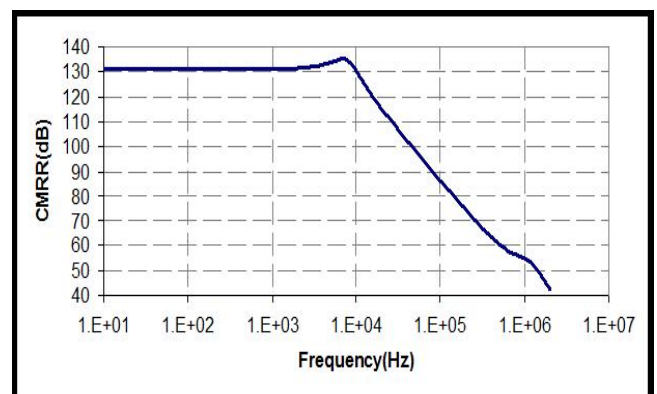
Phase Margin vs. C_{LOAD} (Stable for Any C_{LOAD})



Input Voltage Noise Spectral Density

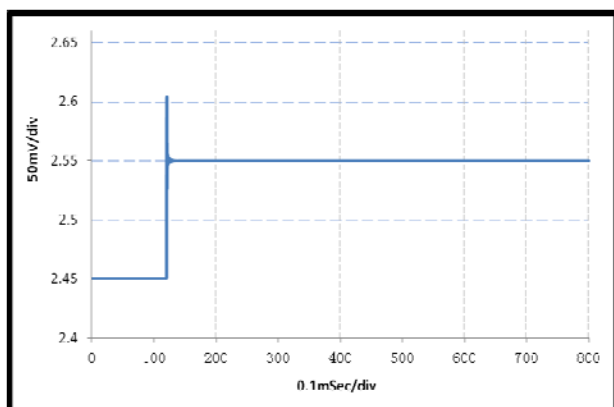


Common-Mode Rejection Ratio

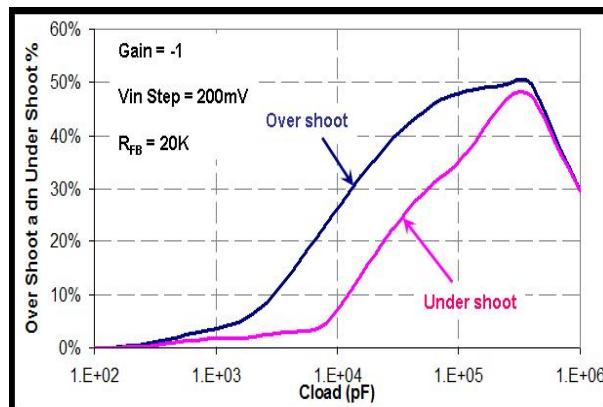


Typical Performance Characteristics

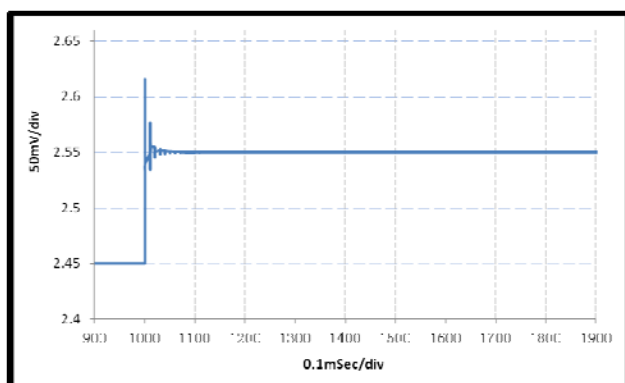
Over-Shoot Voltage, $C_{LOAD} = 40nF$, Gain = +1



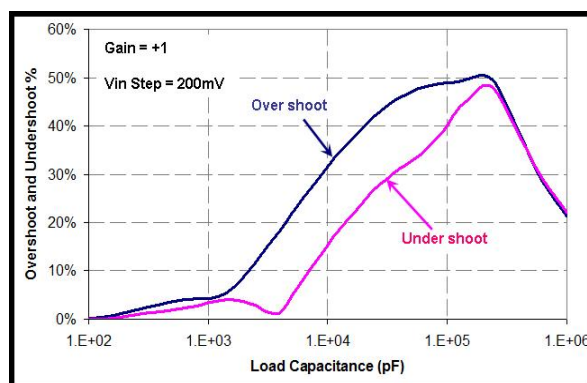
Over-Shoot % vs. C_{LOAD} , Gain = -1, $R_{FB} = 20k\Omega$



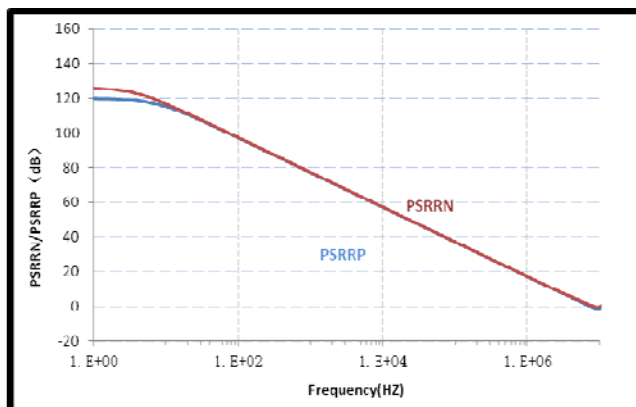
Over-Shoot Voltage, $C_{LOAD}=40nF$, Gain= -1, $R_{FB}=100k\Omega$



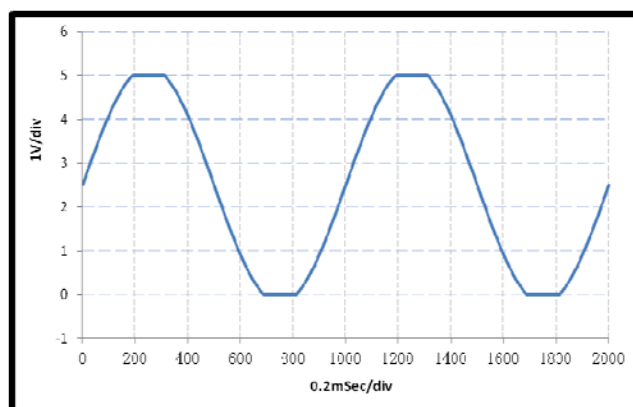
Small-Signal Over-Shoot % vs. C_{LOAD} , Gain = +1



Power-Supply Rejection Ratio

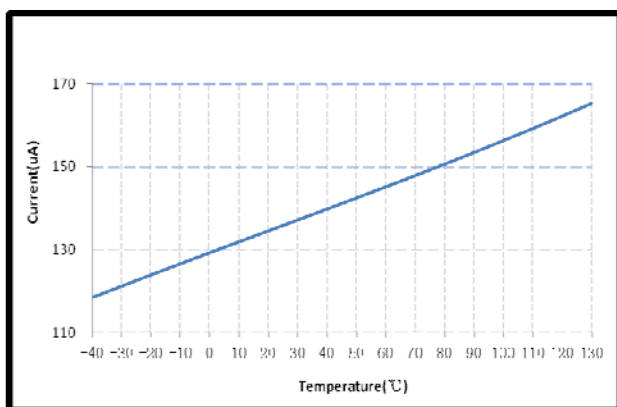


$V_{IN} = -0.2V$ to $5.7V$, No Phase Reversal

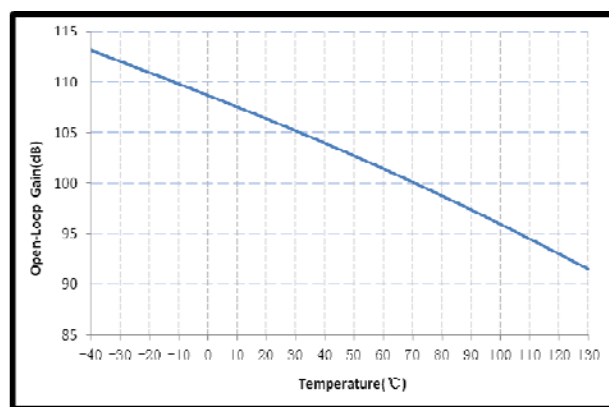


Typical Performance Characteristics

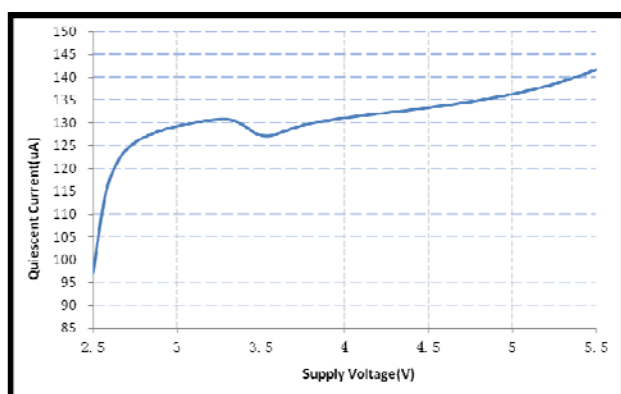
Quiescent Supply Current vs. Temperature



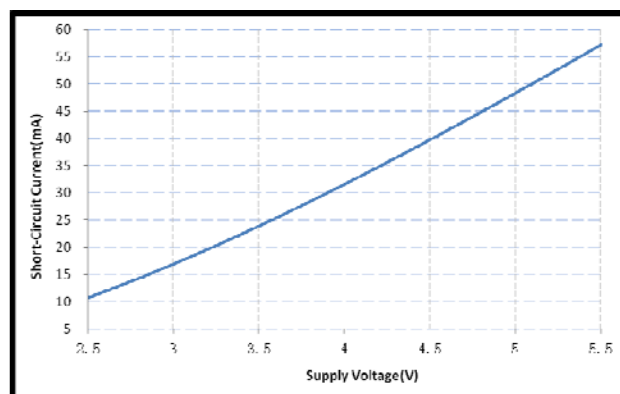
Open-Loop Gain vs. Temperature



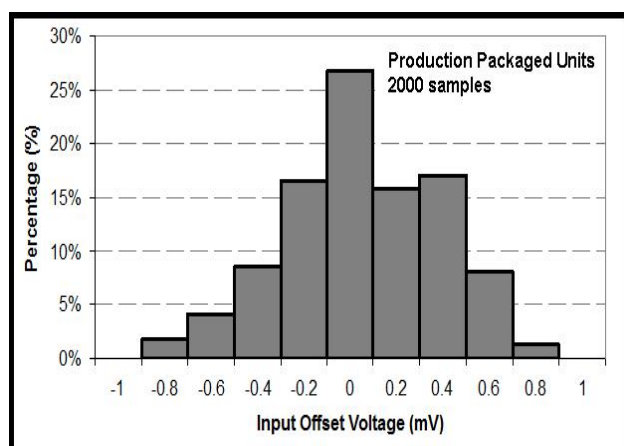
Quiescent Supply Current vs. Supply Voltage



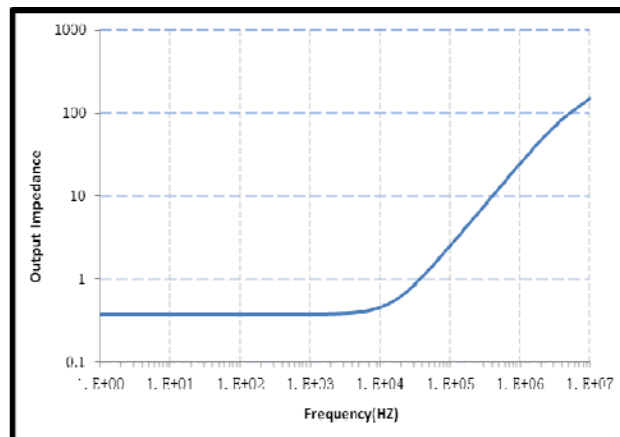
Short-Circuit Current vs. Supply Voltage



Input Offset Voltage Distribution



Closed-Loop Output Impedance vs. Frequency



Pin Functions

–IN: Inverting Input of the Amplifier. Voltage range of this pin can go from $V^- - 0.3V$ to $V^+ + 0.3V$.

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

+V_S: Positive Power Supply. Typically the voltage is from 2.1V to 5.25V. Split supplies are possible as long as the voltage between V+ and V– is between 2.1V and 5.25V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

N/C: No Connection.

–V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V+ and V– is from 2.1V to 5.25V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

SHDN: Active Low Shutdown. Shutdown threshold is 1.0V above negative supply rail. If unconnected, the amplifier is automatically enabled.

OUT: Amplifier Output. The voltage range extends to within millivolts of each supply rail.

Operation

The TP156x family input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is comprised of two CMOS differential amplifiers, a PMOS stage and NMOS stage that are active over different ranges of common mode input voltage. The

Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Low Supply Voltage and Low Power Consumption

The TP156x family of operational amplifiers can operate with power supply voltages from 2.1 V to 6.0 V. Each amplifier draws only 130 µA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding high capacitive load driving capability and stable wide bandwidth. The TP156x family is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for any capacitive load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Low Input Referred Noise

The TP156x family provides a low input referred noise density of 27 nV/√Hz at 1 kHz. The voltage noise will grow slowly with the frequency in wideband range, and the input voltage noise is typically 2.4 µV_{P-P} at the frequency of 0.1 Hz to 10 Hz.

Low Input Offset Voltage

The TP156x family has a low offset voltage of 3.0 mV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirement.

Low Input Bias Current

The TP156x family is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12} \Omega$. A 5 V difference would cause 5 pA of current to flow, which is greater than the TP156x OPA's input bias current at +27°C (± 1 pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

- Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
- Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

- Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_{DD}/2$ or ground).
- Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

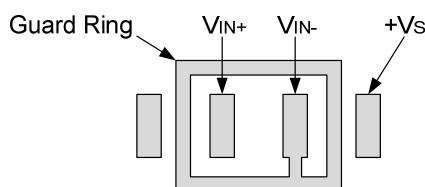


Figure 1

Ground Sensing and Rail to Rail Output

The TP156x family has excellent output drive capability, delivering over 10 mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300 mV beyond either rail, the op-amp can easily perform 'true ground' sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP156x family has reverse-biased ESD protection diodes on all inputs and output. Input and out pins can not be biased more than 300 mV beyond either supply rail.

Feedback Components and Suppression of Ringing

Care should be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration with gain and feedback resistors of 10k, a poorly designed circuit board layout with parasitic capacitance of 5 pF (part +PC board) at the amplifier's inverting input will cause the amplifier to ring due to a pole formed at 3.2 MHz. An additional capacitor of 5 pF across the feedback resistor as shown in Figure 2 will eliminate any ringing.

Careful layout is extremely important because low power signal conditioning applications demand high-impedance circuits. The layout should also minimize stray capacitance at the OPA's inputs. However some stray capacitance may be unavoidable and it may be necessary to add a 2 pF to 10 pF capacitor across the feedback resistor. Select the smallest capacitor value that ensures stability.

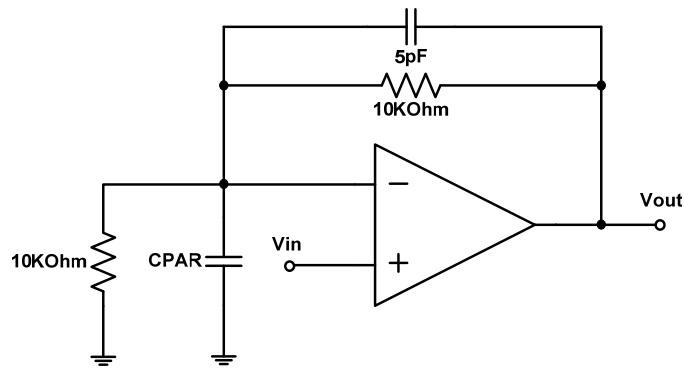


Figure 2

Shut-down

The single channel OPA versions have SHDN pins that can shut down the amplifier to less than 0.2 μ A supply current. The SHDN pin voltage needs to be within 0.5 V of V_{-} for the amplifier to shut down. During shutdown, the output will be in high output resistance state, which is suitable for multiplexer applications. When left floating, the SHDN pin is internally pulled up to the positive supply and the amplifier remains enabled.

Driving Large Capacitive Load

The TP156x family of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for “Phase Margin vs. Load Capacitance”. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop’s phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer ($G = +1V/V$) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP156x OPA family (e.g., > 200 pF when $G = +1V/V$), a small series resistor at the output (R_{ISO} in Figure 3) improves the feedback loop’s phase margin and stability by making the output load resistive at higher frequencies.

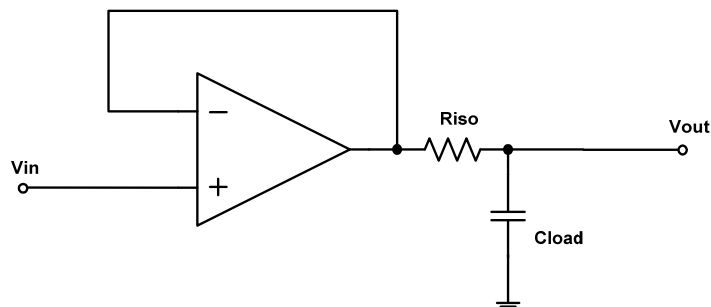


Figure 3

Power Supply Layout and Bypass

The TP156x OPA’s power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 μ F to 0.1 μ F) within 2 mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1 μ F or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA’s inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps’ pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Stable 3.8MHz, 130µA, RRIO, EveryCap™ Op Amps

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Instrumentation Amplifier

The TP156x op-amp series is well suited for conditioning sensor signals in battery-powered applications. Figure 4 shows a two op-amp instrumentation amplifier, using the TP156x op-amps.

The circuit works well for applications requiring rejection of Common Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, V_{REF} is typically $V_{DD}/2$.

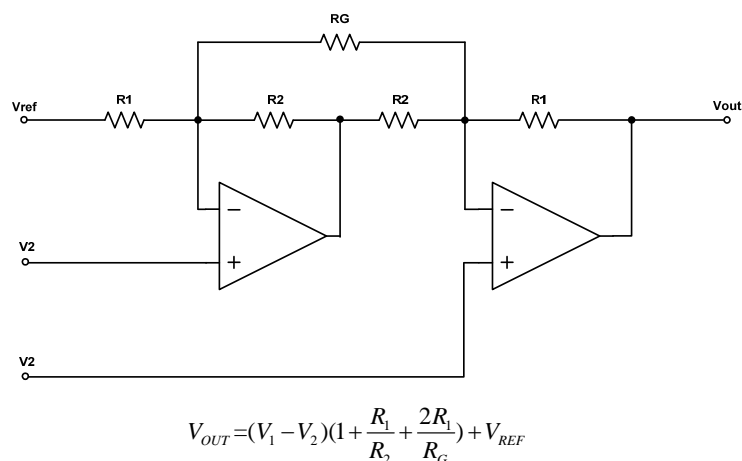


Figure 4

Gain-of-100 Amplifier Circuit

Figure 5 shows a Gain-of-100 amplifier circuit using two TP156x op-amps. It draws 74 µA total current from supply rail, and has a -3dB frequency at 100kHz.

Figure 6 shows the small signal frequency response of the circuit.

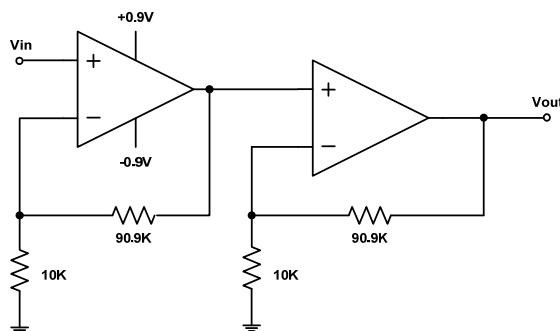


Figure 5: 100kHz, 74µA Gain-of-100 Amplifier

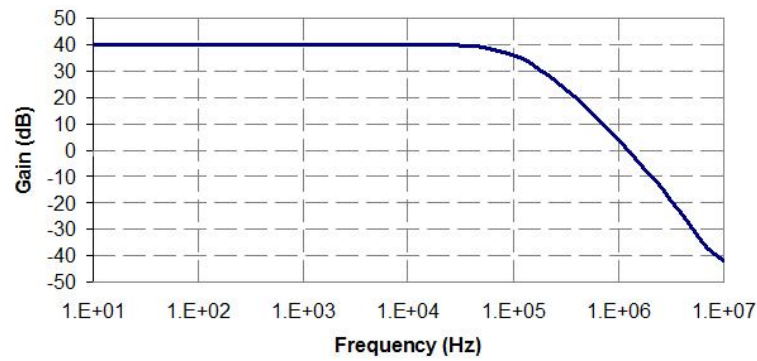


Figure 6: Frequency response of 100kHz, 74uA Gain-of-100 Amplifier

Buffered Chemical Sensor (pH) Probe

The TP156x op-amp has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors such as pH probe. As an example, the circuit in Figure 7 eliminates expansive low-leakage cables that that is required to connect pH probe to metering ICs such as ADC, AFE and/or MCU. A TP156x op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry OPA's output signal to subsequent ICs for pH reading.

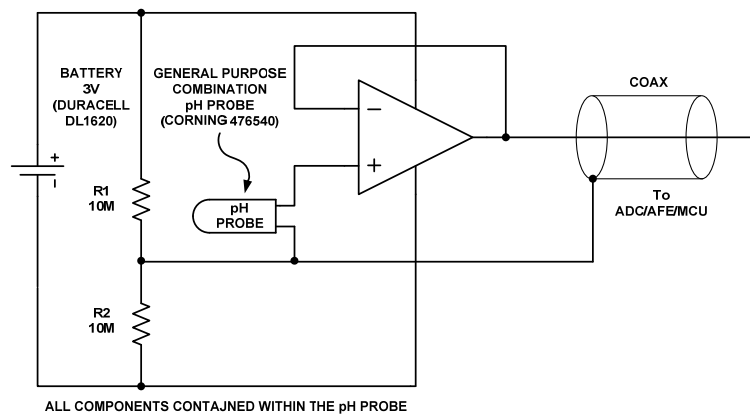


Figure 7: Buffer pH Probe

Two-Pole Micro-power Sallen-Key Low-Pass Filter

Figure 8 shows a micro-power two-pole Sallen-Key Low-Pass Filter with 400Hz cut-off frequency. For best results, the filter's cut-off frequency should be 8 to 10 times lower than the OPA's crossover frequency. Additional OPA's phase margin shift can be avoided if the OPA's bandwidth-to-signal ratio is greater than 8. The design equations for the 2-pole Sallen-Key low-pass filter are given below with component values selected to set a 400Hz low-pass filter cutoff frequency:

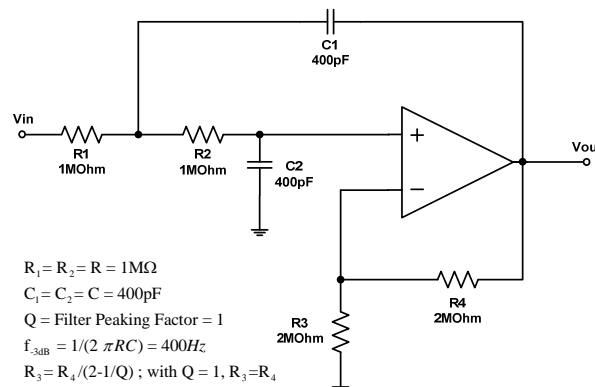


Figure 8

Portable Gas Sensor Amplifier

Gas sensors are used in many different industrial and medical applications. Gas sensors generate a current that is proportional to the percentage of a particular gas concentration sensed in an air sample. This output current flows through a load resistor and the resultant voltage drop is amplified. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the range of tens of microamperes to a few milli-amperes. Gas sensor datasheets often specify a recommended load resistor value or a range of load resistors from which to choose.

There are two main applications for oxygen sensors – applications which sense oxygen when it is abundantly present (that is, in air or near an oxygen tank) and those which detect traces of oxygen in parts-per-million concentration. In medical applications, oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. In fresh air, the concentration of oxygen is 20.9% and air samples containing less than 18% oxygen are considered dangerous. In industrial applications, oxygen sensors are used to detect the absence of oxygen; for example, vacuum-packaging of food products.

The circuit in Figure 9 illustrates a typical implementation used to amplify the output of an oxygen detector. With the components shown in the figure, the circuit consumes less than 37 μ A of supply current ensuring that small form-factor single- or button-cell batteries (exhibiting low mAh charge ratings) could last beyond the operating life of the oxygen sensor. The precision specifications of these amplifiers, such as their low offset voltage, low TC- V_{OS} , low input bias current, high CMRR, and high PSRR are other factors which make these amplifiers excellent choices for this application.

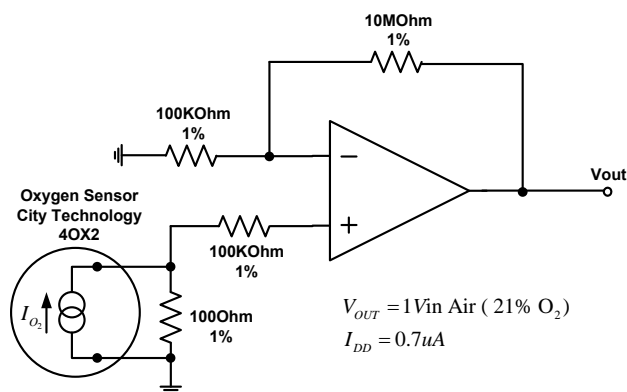
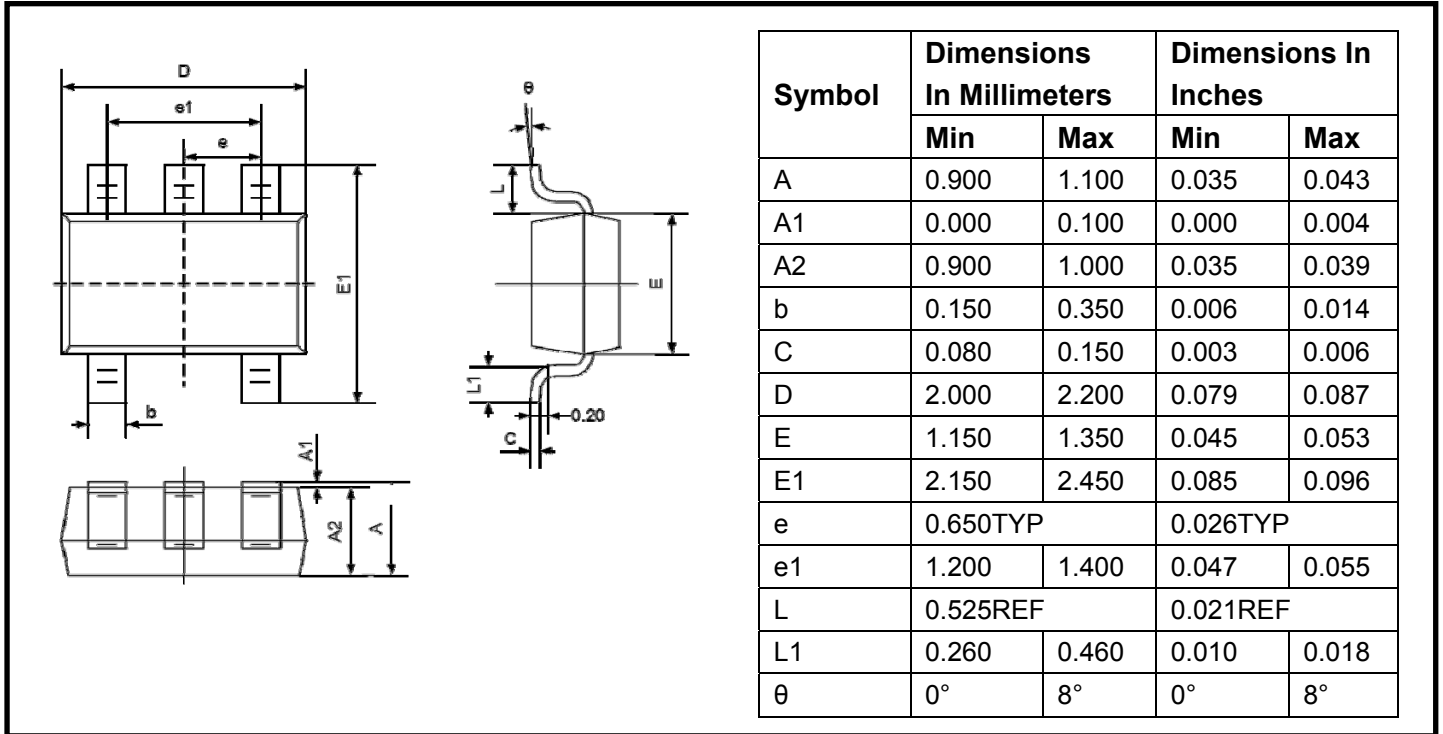


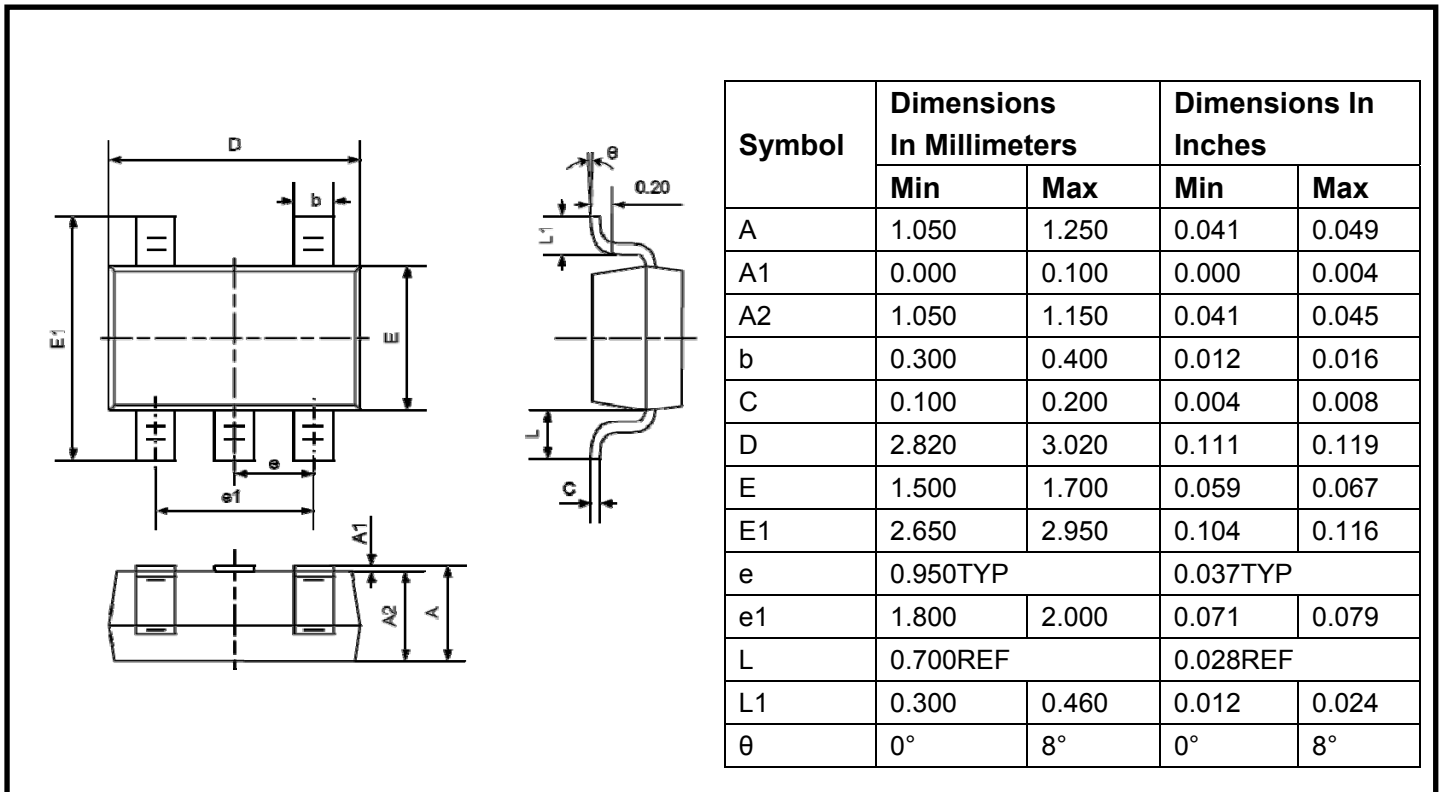
Figure 9

Package Outline Dimensions

SC70-5 /SOT-353

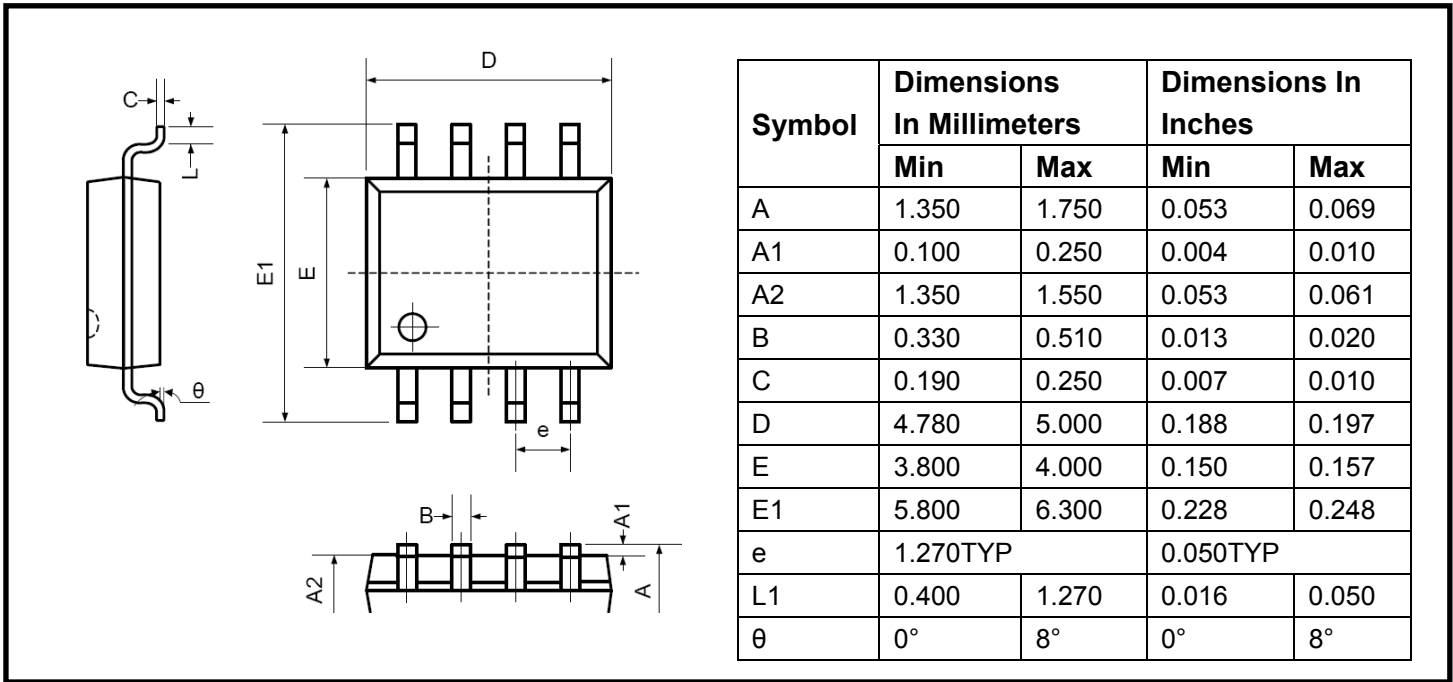


SOT23-5 (SOT23-6)

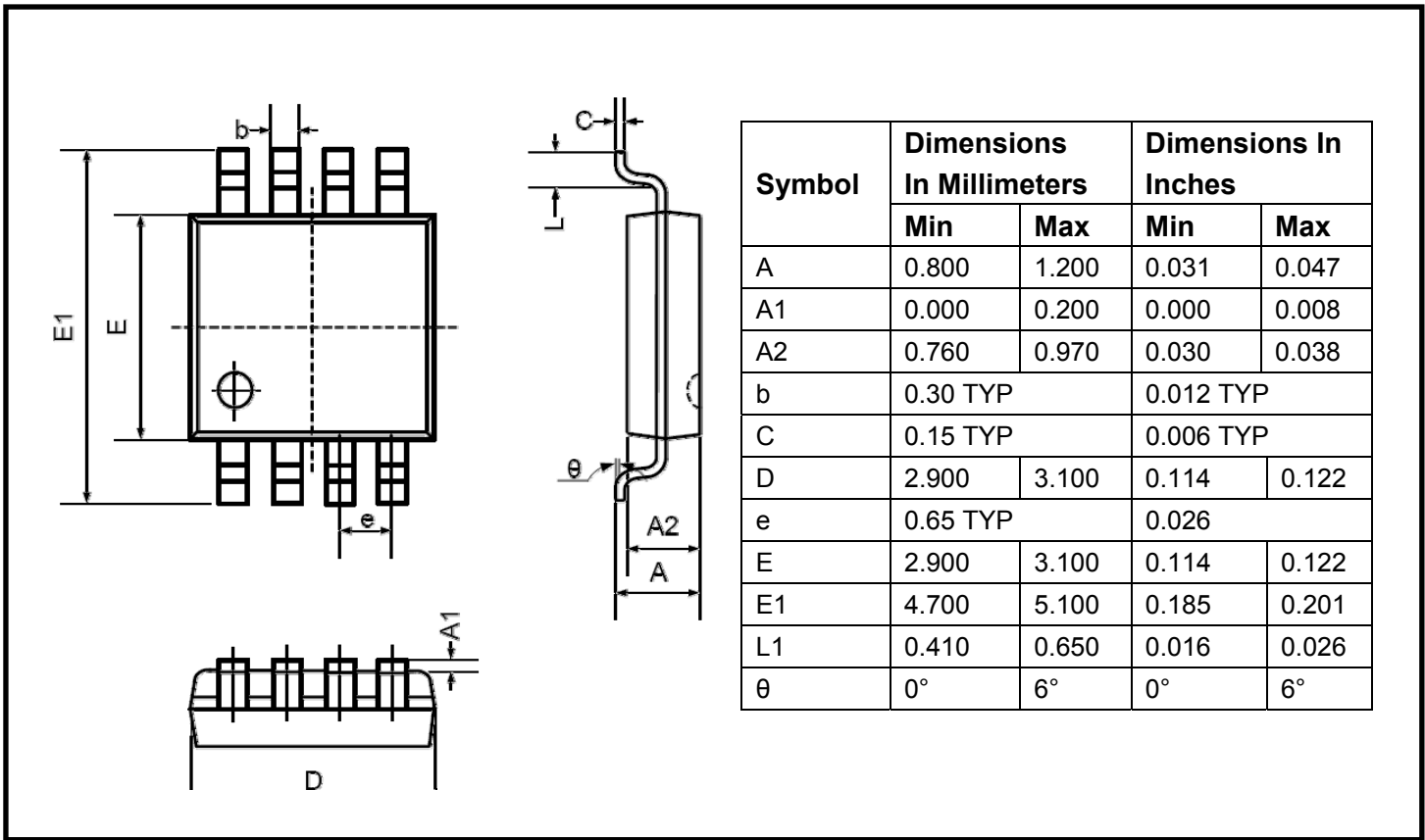


Package Outline Dimensions

SO-8

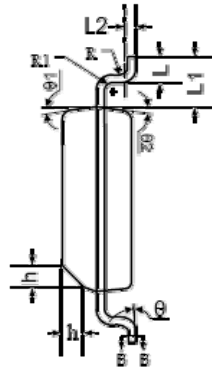
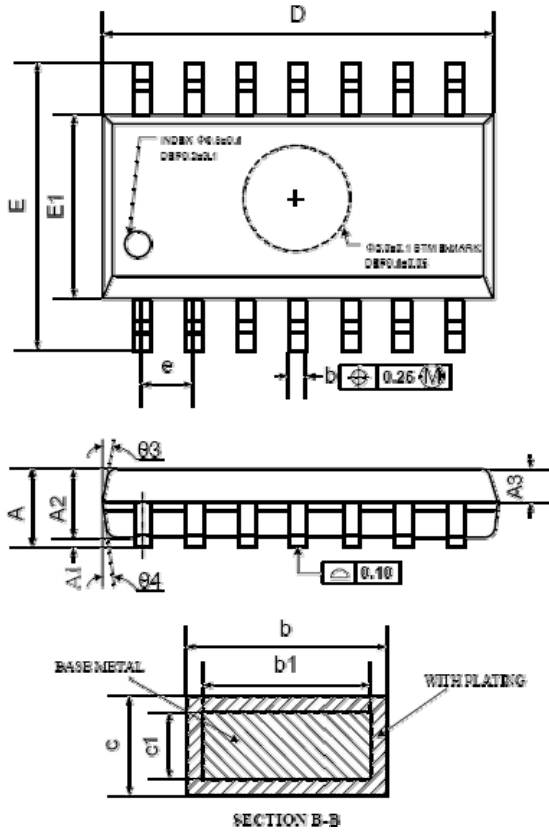


MSOP-8



Package Outline Dimensions

SO-14



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36		0.49
b1	0.35	0.40	0.45
c	0.16		0.25
c1	0.15	0.20	0.25
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30	0.40	0.50
θ	0°		8°
$\theta 1$	6°	8°	10°
$\theta 2$	6°	8°	10°
$\theta 3$	5°	7°	9°
$\theta 4$	5°	7°	9°

Package Outline Dimensions

TSSOP-14

