8Mbit Asynchronous Fast Static RAM

Features

- Fast Access Time : 8, 10, 12, 15ns
- CMOS Low Power Dissipation
  Standby (TTL) : 25mA (Max.)
  (CMOS) : 15mA (Max.)
  Operating : 80mA (8ns, Max.)
  70mA (10ns, Max.)
- 5.0V,3.3V or 1.8V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)
  LB : I/O0~ I/O7, UB : I/O8~ I/O15
- Standard 48FBGA and 44TSOP2 Package type
- ROHS compliant
- Industrial Temperature

Description

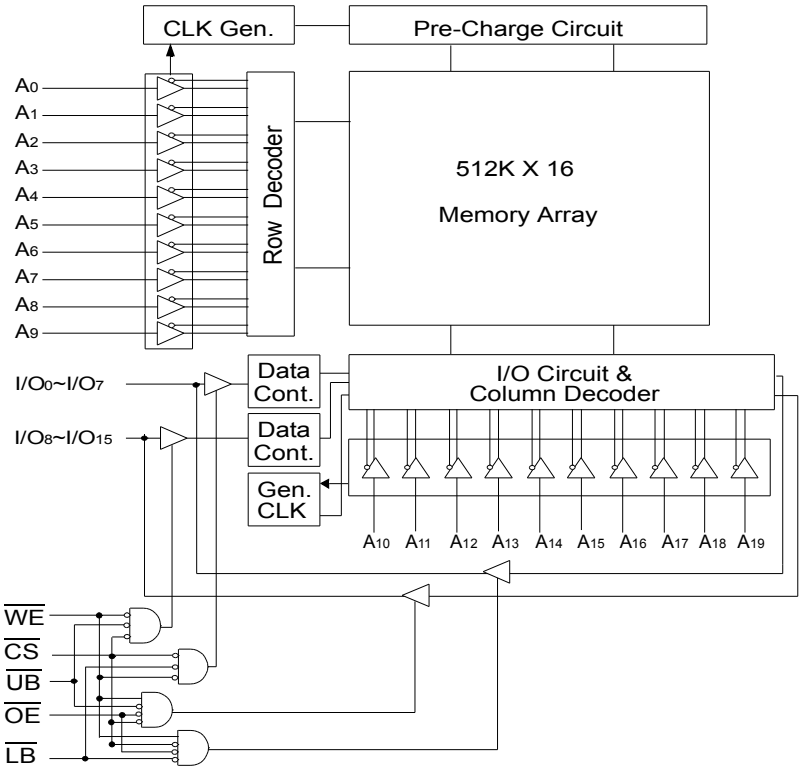
The VTI508(H/N/L)16T(L) and VTI508(H/N/L)08T(L) is a 8,388,608-bit high-speed Static Random Access Memory organized as 512K(1M) words by 16(8) bits.
The device uses 16(8) common input and out-put lines and have an output enable pin which operates faster than address access time at read cycle.

The device is fabricated using advanced CMOS process,6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

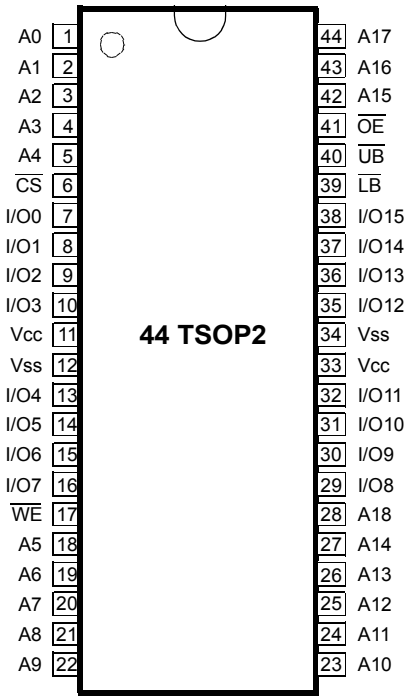
Ordering Information

Density	Org.	Part Number	Vcc (V)	tAA(ns)	Package	Temp.
8Mbit	512Kb x 16bit	VTI508HF16VM-10I	5.0	10	44 TSOP2	-40℃ to 85℃
		VTI508NF16VM-10I	3.3	10	44 TSOP2	
		VTI508LF16VM-10I	1.8	15	44 TSOP2	
		VTI508HF16LM-10I	5.0	10	48 FBGA	
		VTI508NF16LM-10I	3.3	10	48 FBGA	
		VTI508LF16LM-10I	1.8	15	48 FBGA	
	1Mb x 8bit	VTI508HF08VM-10I	5.0	10	44 TSOP2	
		VTI508NF08VM-10I	3.3	10	44 TSOP2	
		VTI508LF08VM-10I	1.8	15	44 TSOP2	
		VTI508HF08LM-10I	5.0	10	48 FBGA	
		VTI508NF08LM-10I	3.3	10	48 FBGA	
		VTI508LF08LM-10I	1.8	15	48 FBGA	

Logic Block Diagram - 512K x 16



PKG Pin Configurations - 512K x 16

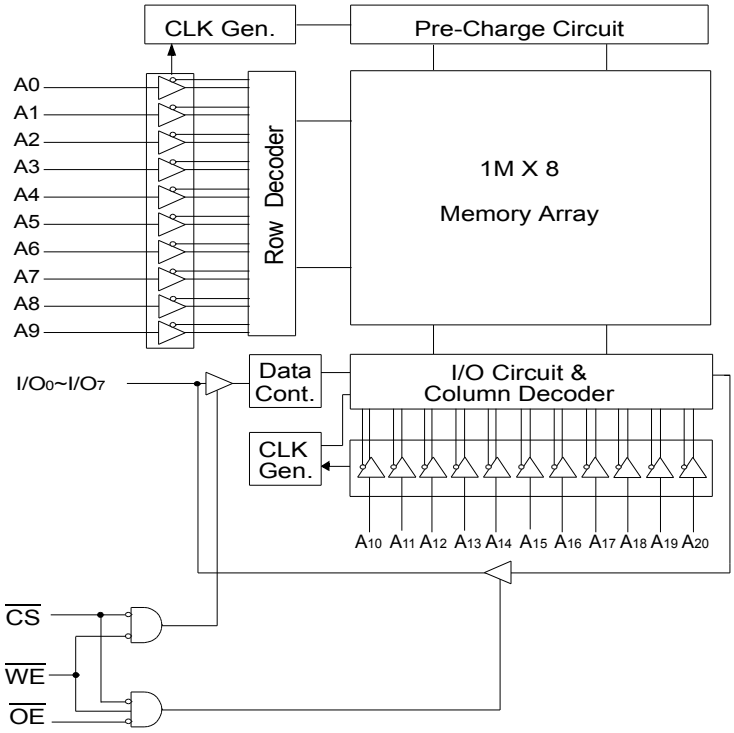


48FBGA

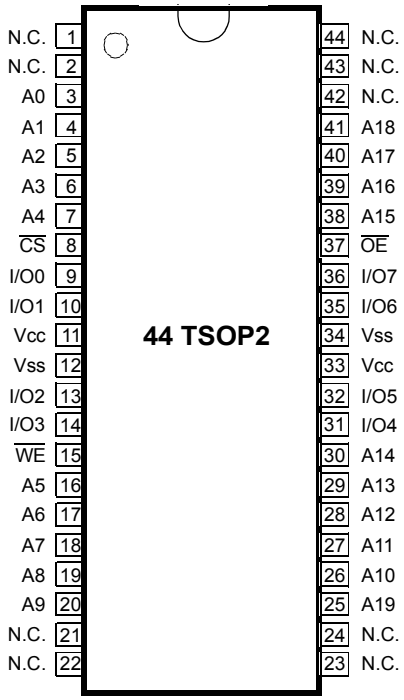
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CS}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	Vss	I/O_{11}	A_{17}	A_7	I/O_3	Vcc
E	Vcc	I/O_{12}	NC	A_{16}	I/O_4	Vss
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

Pin Name	Pin Function
A_0 - A_{18}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O_0~I/O_7)
$\overline{UB}$	Upper-byte Control(I/O_8~I/O_{15})
I/O_0 ~ I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
N.C	No Connection

Logic Block Diagram - 1M x 8



PKG Pin Configurations - 1M x 8



48FBGA

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A_0	A_1	A_2	NC
B	NC	NC	A_3	A_4	$\overline{CS}$	I/O_0
C	NC	NC	A_5	A_6	I/O_1	I/O_2
D	Vss	NC	A_{17}	A_7	I/O_3	Vcc
E	Vcc	NC	NC	A_{16}	I/O_4	Vss
F	NC	NC	A_{14}	A_{15}	I/O_5	I/O_6
G	NC	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{19}

Pin Name	Pin Function
A_0 - A_{19}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_0 ~ I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
N.C	No Connection

Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to VSS	1.8V Product	V_{IN}, V_{OUT}	-0.5 to Vcc+0.5V	V
	3.3V Product			
	5.0V Product			
Voltage on Vcc Supply Relative to VSS	1.8V Product	V_{IN}, V_{OUT}	-0.5 to 4.6	V
	3.3V Product			
	5.0V Product		-0.5 to 7.0	
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Industrial	T_A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions* (T_A=0 to 70°C)

Parameter	Operating Vcc(V)	Symbol	Min	Typ	Max	Unit
Supply Voltage	5.0	V_{CC}	4.5	5.0	5.5	V
	3.3	V_{CC}	2.4	3.3	3.6	
	1.8	V_{CC}	1.65	1.8	2.2	
Ground		V_{SS}	0	0	0	V
Input High Voltage	5.0	V_{IH}	2.2	-	V_{CC}+0.5	V
	3.3	V_{IH}	2.0	-	V_{CC}+0.3	
	1.8	V_{IH}	1.4	-	V_{CC}+0.2	
Input Low Voltage	5.0	V_{IL}	-0.3	-	0.8	V
	3.3	V_{IL}	-0.3	-	0.7	
	1.8	V_{IL}	-0.2	-	0.4	

* The above parameters are also guaranteed for industrial temperature range.

DC and Operating Characteristics*(T_A=0 to 70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}		-2	2	µA
Operating Current**	I_{CC}	Min. Cycle, 100% Duty CS=VIL, VIN=VIH or VIL, IOUT=0mA	8ns	-	80	mA
			10ns	-	70	
			12ns	-	65	
			15ns	-	60	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	25	mA
	I_{SB1}	f=0MHz, $\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V		-	15	
Output Low Voltage Level	V_{OL}	Vcc=4.5V, I_{OL}=8mA, 5.0V Product		-	0.4	V
		Vcc=3.0V, I_{OL}=8mA, 3.3V & Wide Vcc** Product		-	0.4	
		Vcc=1.65V, I_{OL}=0.1mA, Wide Vcc** Product		-	0.2	
Output High Voltage Level	V_{OH}	Vcc=4.5V, I_{OH}=-4mA, 5.0V Product		2.4	-	V
		Vcc=3.0V, I_{OH}=-4mA, 3.3V & Wide Vcc** Product		2.4	-	
		Vcc=1.65V, I_{OH}=-0.1mA, Wide Vcc** Product		1.4	-	

* The above parameters are also guaranteed for industrial temperature range.

Capacitance*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

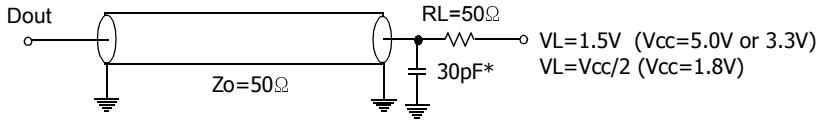
* Capacitance is sampled and not 100% tested.

Test Conditions*

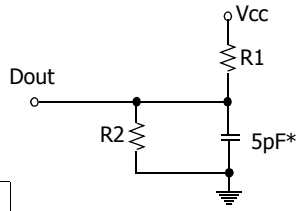
Parameter	Value
Input Pulse Level	0 to 3.0V (Vcc=3.3V or 5.0V)
	0 to 1.8V (Vcc=1.8V)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V (Vcc=3.3V or 5.0V)
	1/2Vcc (Vcc= 1.8V)
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.

Output Load(A)



Output Load(B)
(for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OLZ} & t_{OHZ})

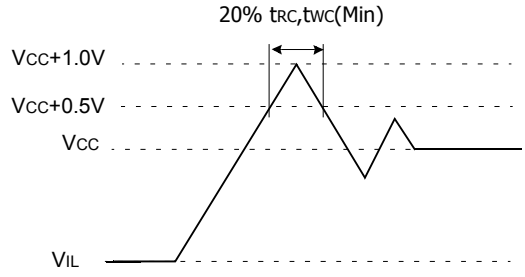


Vcc	5.0V	3.3V	1.8V
R1	480Ω	319Ω	13500Ω
R2	255Ω	353Ω	10800Ω

* Including Scope and Jig Capacitance

Fig. 1

Overshoot Timing



Undershoot Timing

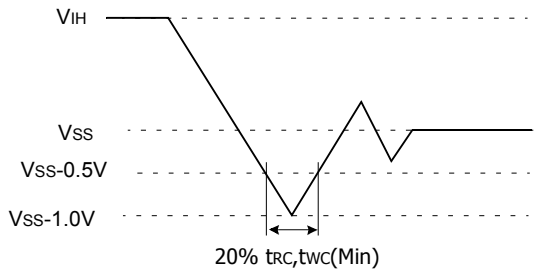


Fig. 2

Functional Description (x8 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* X means Don´t Care.

Functional Description (x16 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_0~I/O_7	I/O_8~I/O_{15}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* X means Don't Care.

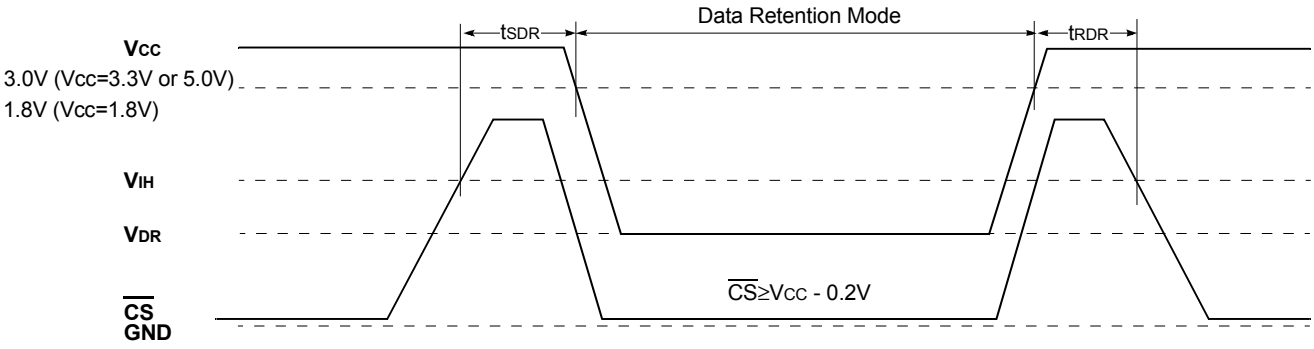
Data Retention Characteristics* (T_A=0 to 70°C)

Parameter	Product	Operating Vcc(V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	5.0V Product	5.0	V_{DR}	$\overline{CS}$ ≥V_{CC} - 0.2V	2.0	-	5.5	V
	3.3V Product	3.3			2.0	-	3.6	
	1.8V Product	1.8			1.5	-	3.6	
Data Retention Current	5.0V Product	5.0	I_{DR}	V_{CC}=2.0V $\overline{CS}$≥V_{CC} - 0.2V V_{IN}≥V_{CC} - 0.2V or V_{IN}≤0.2V	-	-	15	mA
	3.3V Product	3.3			-	-	15	
	1.8V Product	1.8		V_{CC}=1.5V $\overline{CS}$≥V_{CC} - 0.2V V_{IN}≥V_{CC} - 0.2V or V_{IN}≤0.2V	-	-	15	
Data Retention Set-Up Time			t_{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time			t_{RDR}		5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.

Data Retention Wave Form

$\overline{CS}$ controlled



Read Cycle

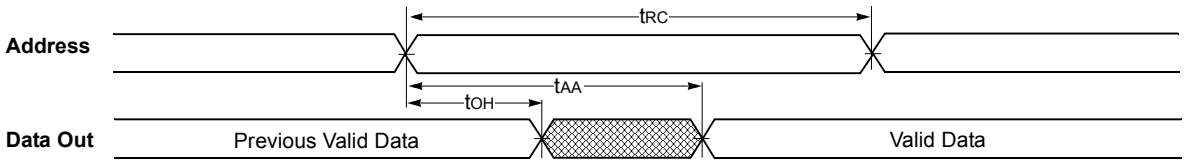
Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	-	7	ns
$\overline{UB}$, $\overline{LB}$ Access Time **	t_{BA}	-	4	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output **	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output **	t_{BHZ}	0	4	0	5	0	6	0	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	t_{PD}	-	8	-	10	-	12	-	15	ns

Write Cycle

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	9	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	9	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	6	-	7	-	9	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	8	-	10	-	12	-	15	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write **	t_{BW}	6	-	7	-	9	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	0	6	0	7	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	7		8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

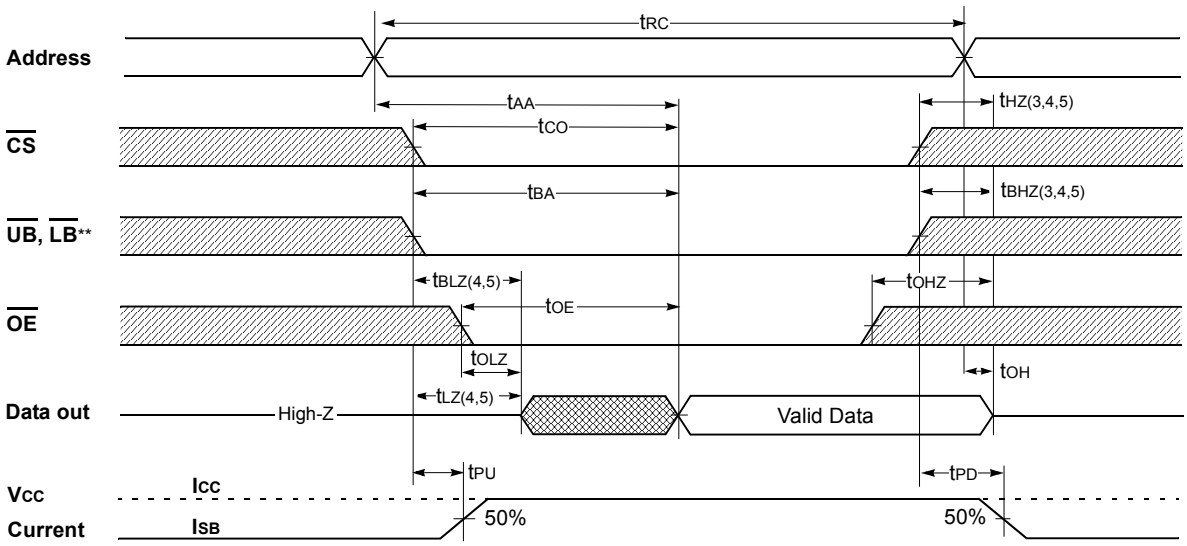
Timing Diagrams

Timing Waveform Of Read Cycle(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$, $\overline{LB}$=V_{IL} **)



** Those parameters are applied for x16 mode only.

Timing Waveform Of Read Cycle(2) ($\overline{WE}$=V_{IH})

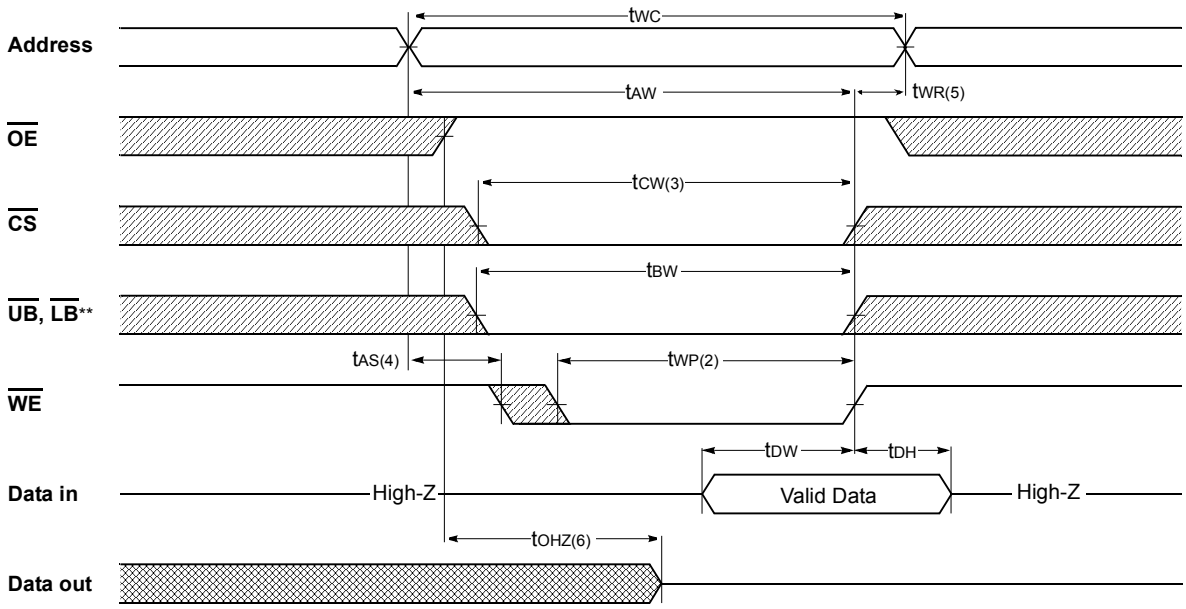


NOTES(Read Cycle)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

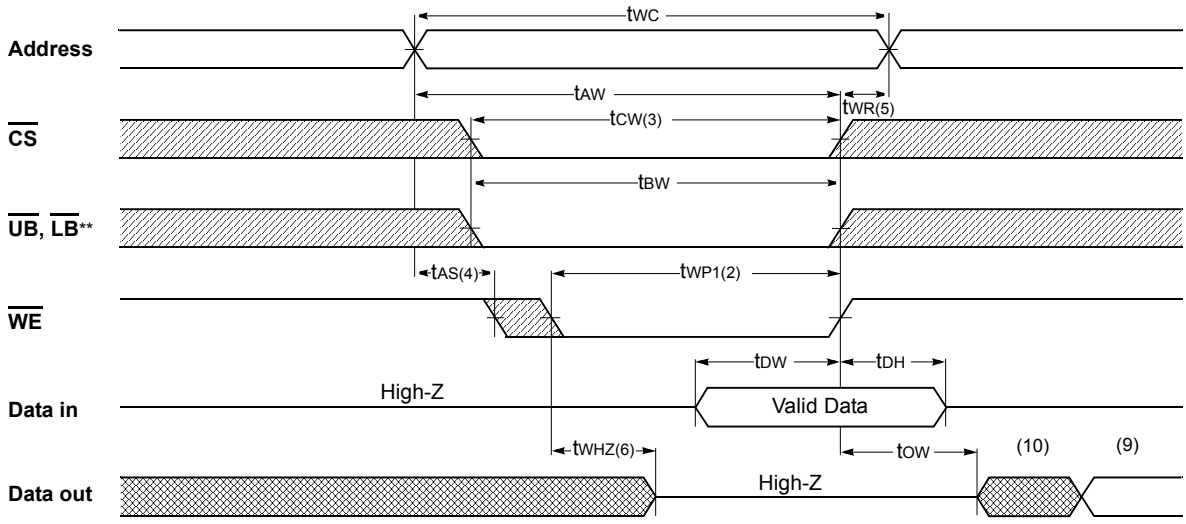
** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(1) ($\overline{OE}$ Clock)



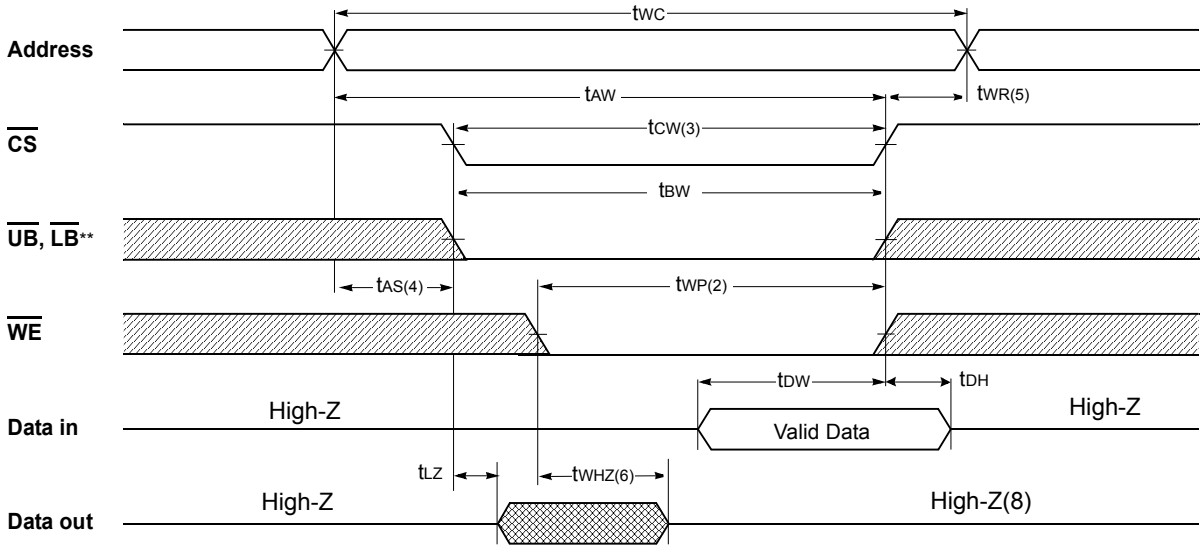
** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(2) ($\overline{OE}$=Low fixed)



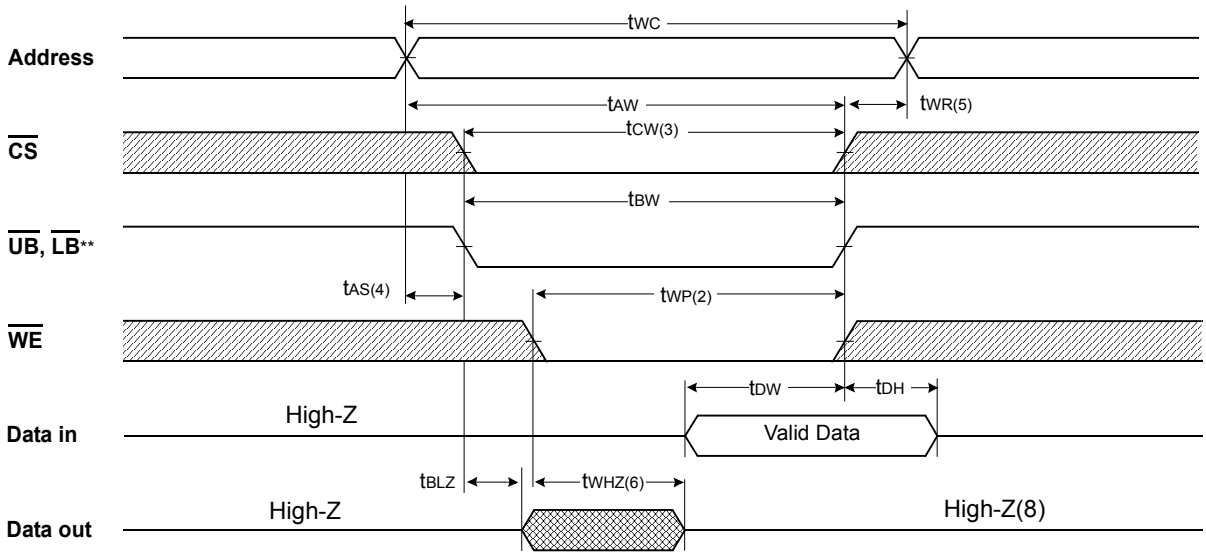
** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(3) ($\overline{CS}$=Controlled)



** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(Write Cycle)

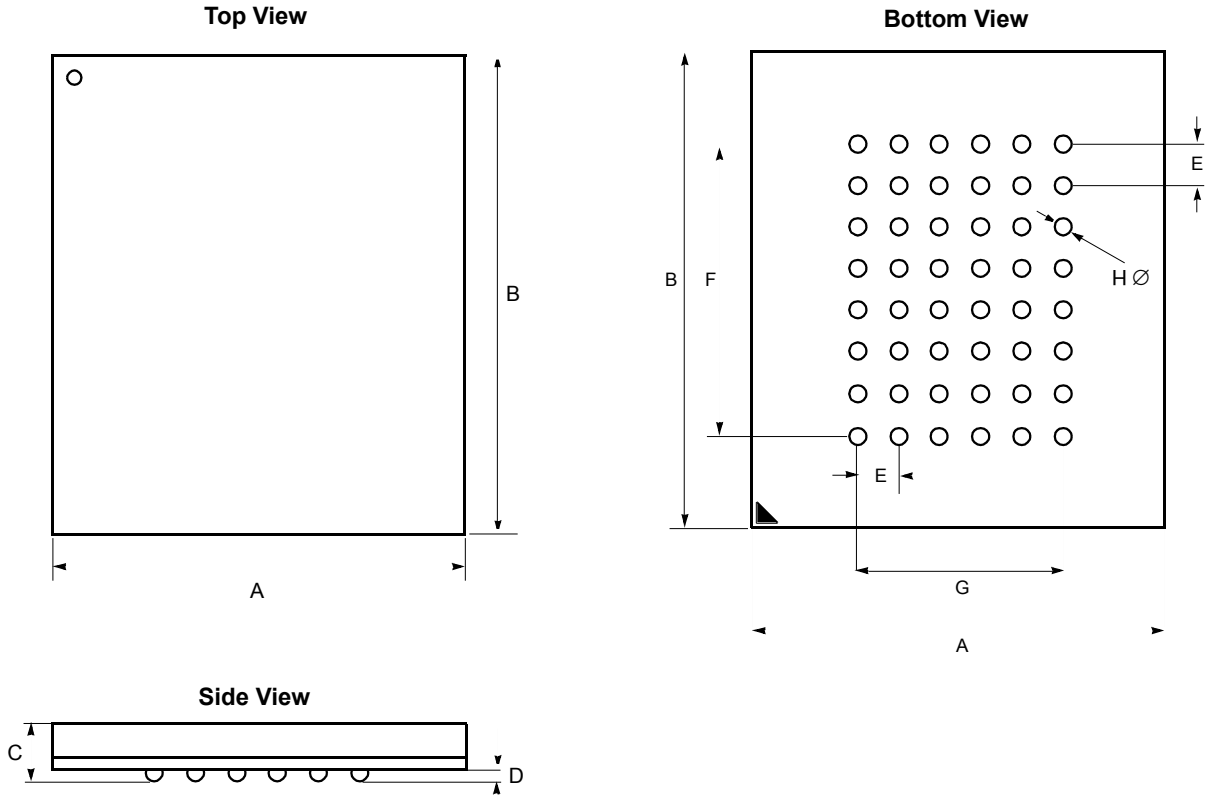
1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not . be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only.

Package Dimensions

48-FBGA

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array

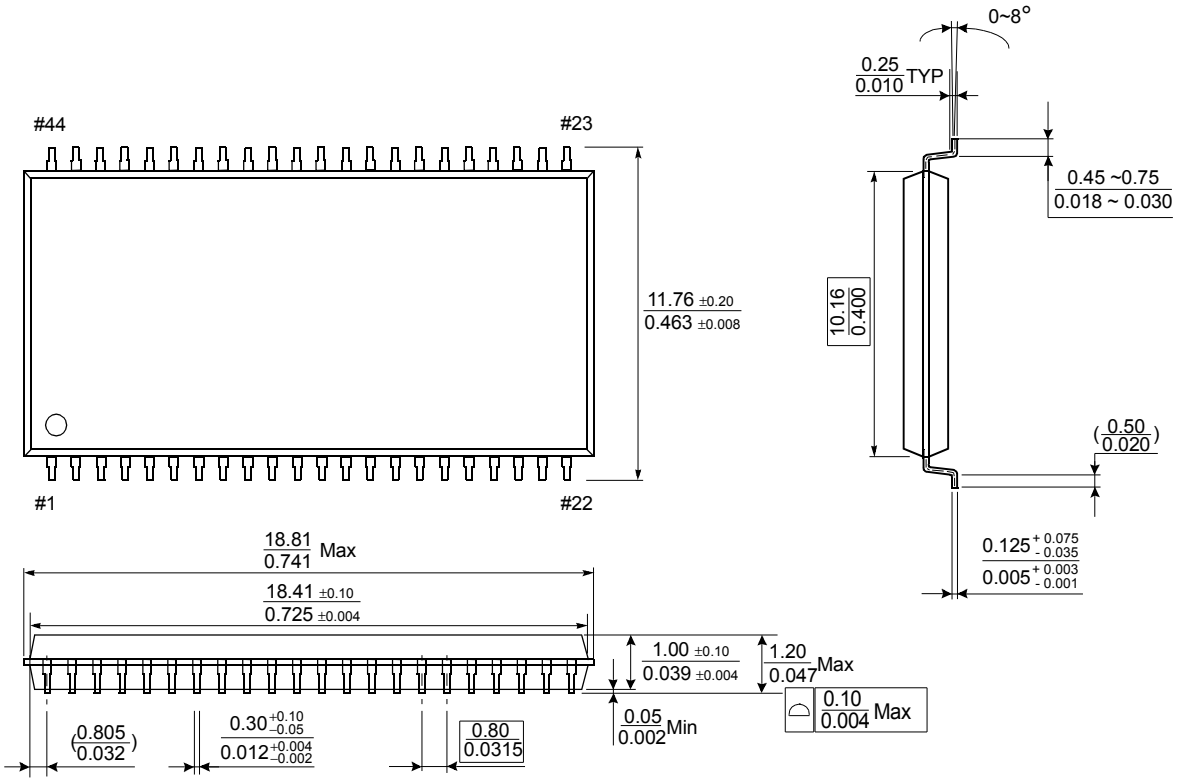


Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	6 ± 0.1	mm		**E**	0.75	mm	
B	8 ± 0.1	mm		**F**	5.25	mm	
C	1.1 ± 0.1	mm		**G**	3.75	mm	
D	0.25 ± 0.05	mm		**H**	0.35 ± 0.05	mm	

Package Dimensions

44-TSOP2-400BF

Units:millimeters/Inches



Code Informations

V	T	I	X	X	X	X	X	X	X	X	X	-	X	X	X	X	X	X
1	2	3	4	5	6	7	8	9	10	11	12		13	14	15	16	17	18

Digit-No.	Remark		Code
1,2,3	Vilsion Technology Inc. Product		VTI
4	Asynchronous SRAM		5
5,6	Density	1Mb	01
		2Mb	02
		4Mb	04
		8Mb	08
		16Mb	16
		32Mb	32
7	Vcc	1.8V	L
		3.3V	N
		5.0V	H
		1.65V~3.6V	W
8	Product type	Low Power(1 C/S)	L
		Low Power(2C/S)	B
		Fast	F
9 10	Organization	8bit	08
		16bit	16
11	Package	36 BGA	N
		48 BGA	L
		48 TSOP1	T
		44 TSOPII	V
		32 TSOP1	S
		32 sTSOP1	W
		32 TSOPII	Y
		32 SOP	P
12	Die Version	Monther Die	M
		2nd Generation	A
		3rd Generation	B
13,14	Speed	8ns	08
		10ns	10
		12ns	12
		45ns	45
		55ns	55
15	Temperature range	-40℃ to 85℃	I
		-40℃ to 105℃	A
16	Packing type	Tray	Blank
		Tape and Reel	T
17，18	Special function	TBD	TBD

Document History

Rev.	Date	Description of Change
0	Oct. 2015	Initial Advanced Information Release
1	Jan. 2016	Final