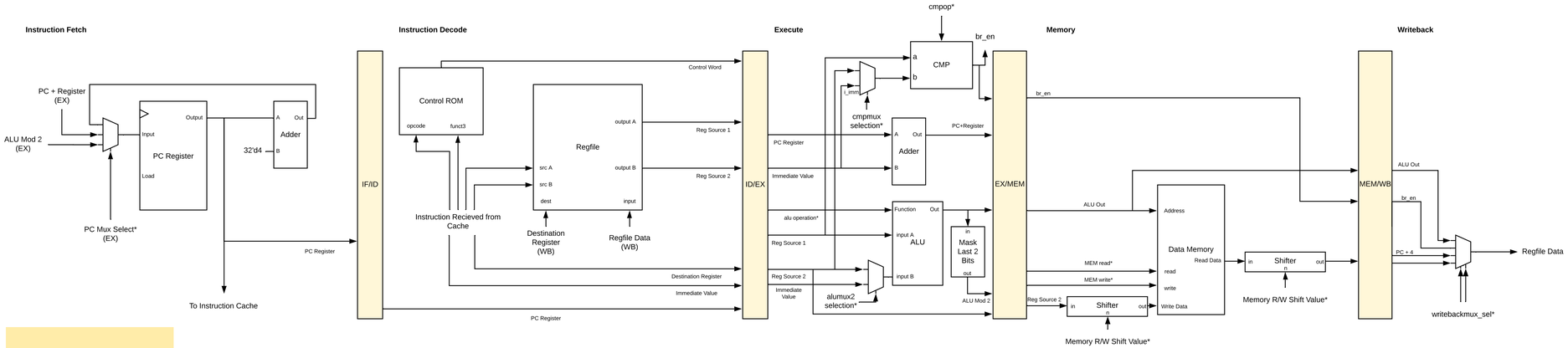

Note:
1. Signal with a * comes from the control ROM

2. Signal with a (stage) specifies where it's retrieved from. For example, br_en(EX) in IF means this br_en is avaliable from EX/MEM stage 2 cycles later

MEMORY

Unlike other state modules, MEM stage contains no sub-modules, therefore it is challenging to describe it visually. This module considers inputs and based on its considerations, set outputs.

If (mem_read == 1) && (mem_write == 0)
pmem_write = 0, pmem_read = 1,(of course), wdata = 32'h___, pmem_rdata = rdata_out.

Else If (mem_write == 1) && (mem_read == 0)
pmem_write = 1, pmem_read = 1, wdata = pmem_wdata, rdata_out = 32'h___.

Default: pmem_write = 0, pmem_read = 0, wdata = 32'h___, rdata_out = 32'h___.

Always pmem_address = mem_addr.

Basically dealing with all memory signals and generating physical memory signals for actual physical memory. It is the fourth stage of pipelining datapath so that it communicates with the actual memory.
For the checkpoint purpose, we consdier to set mem_resp is ALWAYS set to be high so that we do not have to handle cache misses or memory stalls at all. (Not sure this is right though)