# Technology Independent Analog Circuit Design with $g_m/I_D$ Methodology

**Master Thesis Report**
Master in the department of Electrical Engineering and Information Technology
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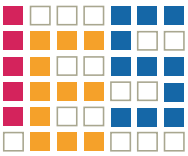

Integrated Electronic Systems

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# Abstract

This thesis investigates the design of analog circuits in UMC 65nm and GF 22nm CMOS submicron technologies, with a focus on low-power applications. The scaling of transistors introduces challenges such as reduced supply voltage, lower intrinsic gain, and limited dynamic range, making analog circuit design increasingly complex and time-intensive. To address these issues, the $g_m/I_D$ methodology is employed as a systematic approach to optimize transistor operation and streamline the design process. A Python-based tool was developed to generate Look-Up Tables (LUTs) from Cadence Spectre simulation data, enabling efficient and accurate transistor sizing while enhancing circuit performance predictions. This methodology is applied to the design of three analog blocks: a two-stage Miller operational amplifier, a latched comparator, and a telescopic amplifier. The latched comparator demonstrates strong inversion operation, while the operational amplifiers explore moderate and weak inversion regimes. This work provides a robust framework for designing high-performance, low-power analog circuits, bridging theoretical methodology with practical implementation in advanced submicron technologies.

# List of Abbreviations

| | |
|---|---|
| $A_{DC}$ | DC Gain |
| **CMRR** | Common Mode Rejection Ratio |
| $C_c$ | Compensation Capacitor |
| $C_{gb}$ | Gate-to-Bulk Capacitance |
| $C_{gg}$ | Gate-to-Gate Capacitance |
| $C_{gs}$ | Gate-to-Source Capacitance |
| $C_L$ | Load Capacitance |
| $C_{ox}$ | Oxide Capacitance |
| **EKV** | Enz, Krumenacher and Vittoz compact model |
| $f_u$ | Unity Gain Frequency |
| $f_T$ | Transit Frequency |
| $f_{CLK}$ | Clock Frequency |
| **GBW** | Gain Bandwidth Product |
| **GF** | GlobalFoundries |
| $g_m$ | Transconductance |
| $g_m/I_D$ | Transconductance Efficiency |
| $g_{ds}$ | Output Conductance |
| **GUI** | Graphical User Interface |
| $I_{bias}$ | Biasing Current |
| $I_D$ | Drain Current |
| $I_D/W$ | Current Density |
| $J_D$ | Current Density |
| $L$ | Transistor Length |
| $L_{min}$ | Minimum Length |
| **LUT** | Lookup Table |
| **MOS** | Metal-Oxide-Semiconductor |
| **MOSFET** | Metal-Oxide-Semiconductor Field-Effect-Transistor |
| **OTA** | Operational Transconductance Amplifier |

| | |
|---|---|
| **OpAmp** | Operational Amplifier |
| $P_{avg}$ | Average Power Consumption |
| **PDP** | Power Delay Product |
| **PM** | Phase Margin |
| $R_n$ | Nulling Resistor |
| **SR** | Slew Rate |
| **SPICE** | Simulation Program with Integrated Circuit Emphasis |
| **UMC** | United Microelectronics Corporation |
| $U_T$ | Thermal Voltage |
| $V_{Dsat}$ | Drain Saturation Voltage |
| $V_{GS}$, $V_{DS}$ | Gate and Drain Voltage with respect to the source (DC) |
| $\mathbf{V_{DD}}$ | Supply Voltage |
| $V_{ov}$ | Gate Overdrive Voltage, VGS - VT |
| $V_{SB}$ | Source-to-Bulk Voltage |
| $V_{TH}$ | Threshold Voltage |
| $\mu$ | Carrier Mobility |
| $\omega$ | Angular Frequency |
| $W$ | Transistor Width |

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# 1 Introduction

Advancements in fabrication processes have spurred the rapid development of semiconductor technology, resulting in a substantial decrease in transistor sizes. This trend towards miniaturization has markedly enhanced digital circuit performance by increasing transistor density and reducing chip area. However, this same trend presents several challenges for analog circuit design. Decreased gain, reduced dynamic range, and diminished supply voltage headroom are all consequences of the ongoing miniaturization of transistor dimensions [1]. As a result, conventional long-channel models employed in analog design are increasingly inaccurate, prompting the need for new design approaches to tackle these evolving challenges [2].

In response to these issues, the $g_m/I_D$ methodology has emerged as a crucial strategy for analog circuit design. Initially introduced by Silveira et al. in 1996, this approach leverages the ratio of transconductance ($g_m$) to drain current ($I_D$) as a key parameter for transistor sizing and circuit design [2]. The $g_m/I_D$ methodology offers a systematic framework for designing analog circuits by employing approximated data and pre-computed lookup tables (LUTs), which account for various operating regions and transistor inversion modes [1]. This method becomes increasingly important as MOSFETs are miniaturized, where short-channel effects like mobility degradation and drain-induced barrier lowering have a pronounced effect on device performance [3].

Recent advancements in the $g_m/I_D$ methodology have refined its application further. For instance, Jespers and Murmann's 2017 work provides a comprehensive overview of systematic design techniques and the utilization of LUTs to optimize circuit performance [1]. Additionally, the practical use of $g_m/I_D$ in various analog circuits has been showcased. Notably, Sabry et al. (2018) examined the methodical development and enhancement of OTAs utilizing this technique [4]. Kumar et al. (2019) presented design automation techniques for OTAs, showcasing the relevance of the methodology in contemporary design contexts [3]. Furthermore, Martins et al. (2022) introduced a temperature-aware

design methodology using the $g_m/I_D$ approach in 180 nm CMOS technology, extending its applicability to high-temperature environments up to 250°C [5].

The primary objective of this thesis is to develop a comprehensive and user-friendly tool that leverages the $g_m/I_D$ methodology for analog circuit design in submicron technologies. This involves generating LUTs in Python using Cadence Spectre as an interface to facilitate the efficient calculation of transistor widths. This implementation offers significant advantages over MATLAB, including cost-effectiveness and flexibility, as MATLAB typically requires additional licensing. The tool will integrate data from the generated plots and apply it to advanced circuit designs, thereby demonstrating the effectiveness and efficiency of the $g_m/I_D$ methodology. This approach not only simplifies the design process but also enhances the accuracy and performance of modern analog circuits.

The following chapters of the thesis are organized as follows: **Chapter 2** reviews various design methodologies and emphasizes the advantages of the $g_m/I_D$ approach. **Chapter 3** provides an in-depth analysis of the $g_m/I_D$ methodology, including its operating regions and inversion mode selection tailored to design specifications. **Chapter 4** covers the generation of Look-Up Tables (LUTs) and the implementation of the $g_m/I_D$ design tool using Python. **Chapter 5** demonstrates the application of the $g_m/I_D$ methodology through the design of a two-stage Miller OpAmp, a latched comparator, and a telescopic OTA. Finally, **Chapter 6** summarizes the findings and implications of this thesis work.

# 2 Overview of Methodologies

This chapter introduces key methodologies and models used in CMOS analog circuit design, focusing on transistor sizing and the impact of short-channel effects. It covers traditional hand-calculation approaches, advanced models like the EKV model and $g_m/I_D$ methodology, and reviews various models developed to address challenges in deep submicron technologies. The goal is to provide a clear understanding of how these methodologies balance simplicity and accuracy in modern design practices.

Designing CMOS analog circuits begins with the critical step of transistor sizing, which is typically accomplished using hand-calculation equations. This initial sizing is foundational, as it influences the entire design process of the circuit. Understanding the initial sizing is fundamental to the overall design process. Accurate models are necessary as they ensure that the design parameters meet the required specifications. They also provide designers with valuable insights into transistor sizing, bias voltages, $g_m$, and $I_D$ [6, 7].

These models accurately represent behavior in moderate inversion and account for short-channel effects, which are critical in submicron technologies [7, 8]. Traditional design approaches often rely on threshold voltage-based models. Although widely used, these models tend to lose accuracy, particularly when sizing transistors that operate in the moderate inversion region. Incorporating short-channel effects into these models often leads to highly complex equations, making them impractical for manual calculations [9].

Analog designers must navigate the challenge of selecting transistor models and design strategies that strike a balance between simplicity and accuracy throughout various operating regions, by incorporating short-channel effects. The EKV model and the $g_m/I_D$ methodology are two approaches that effectively address these requirements [6, 10].

**The EKV Model**

Version 2.6 of the EKV model (level 5) is widely used in analog design, while the most recent version 3.0 also supports RF circuit design [11]. The model introduces the inversion

factor as a parameter and preserves the intrinsic symmetry between the source and drain, delivering an in-depth understanding of transistor behavior across the different regions of operations. However, like threshold voltage-based models, the integration of short-channel effects into the EKV model leads to complex analytical expressions, reducing its practicality for hand calculations [11].

### The $g_m/I_D$ Methodology

The sizing of transistors across all operating regions can be achieved using the semi-empirical $g_m/I_D$ methodology. This approach also incorporates short-channel effects. It relies on pre-computed values of the drain current at various voltage potentials for transistors with specific channel dimensions. These values can be stored in LUTs, simplifying the process for designers to determine the drain current for any transistor in the circuit, based on its length and the voltages at the gate, source, and drain. This approach strikes a balance between simplicity and accuracy, making it highly practical for modern CMOS analog circuit design [6, 10].

Over the years, various models have been developed to address the complexities of CMOS transistor behaviour, particularly as device dimensions have scaled down to deep submicron levels. Some of the prominent models include:

- **SPICE Models:** SPICE models are among the earliest models used in transistor-level circuit design. However, they have become obsolete for submicron technologies due to their inaccuracy and discontinuities in current derivatives [6, 7].
- **PHILIPS Model:**MOS Model 11, part of the PHILIPS series, is a compact model that utilizes surface potential concepts. It is designed to be applicable in the design of digital, analog, and RF circuits. While it captures short-channel effects, its surface potential-based nature leads to complex equations, making it less practical for hand calculations [12].
- **SP Model:** This model, based on surface potential, offers accurate representation of the $g_m/I_D$ ratio and incorporates most short-channel effects [11].
- **PSP Model:** This model merges the strengths of both the SP and PHILIPS MOS models, offering enhanced precision and suitability for modern designs, along with superior computational performance. However, its main drawback is its greater complexity [13].

The $g_m/I_D$ methodology is preferred because it offers simplicity, flexibility, and practicality, making it ideal for efficient and fast design processes. It allows designers to achieve good results with less complexity, enabling quicker iterations and easier adjustments. In contrast, the EKV model and other models discussed above, although precise, are more complex and require a higher number of iterations, making it less efficient for rapid design tasks. Therefore, $g_m/I_D$ is often chosen for its balance of ease and effectiveness in design.

# 3 $g_m/I_D$ Methodology

$g_m/I_D$ methodology, which is essential for optimizing MOSFET performance in analog circuit design. It begins with an understanding of the MOSFET operating regions - weak, moderate, and strong inversion and their impact on transconductance efficiency and circuit behaviour [10]. This strategic approach explained in detail in this chapter, aids in determining the optimal transistor size and operating conditions to enhance circuit performance across different semiconductor technologies [1].

## Operation Regions of MOSFETs

MOSFETs operate in three major regions: weak inversion, moderate inversion, and strong inversion. Each of these regions exhibits unique relationships between the drain current $I_D$ and the gate-source voltage $V_{GS}$, which affect $g_m/I_D$ and overall design performance.

**Weak Inversion (Sub-Threshold Region)**

In the weak inversion or sub-threshold region, the gate-source voltage $V_{GS}$ is below the threshold voltage $V_{TH}$, resulting in a partially inverted channel [10]. The current $I_D$ is dominated by diffusion, flowing due to minority carriers, with an exponential current-voltage relationship similar to that in a BJT. The transconductance efficiency $g_m/I_D$ is maximized, expressed as:

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \tag{3.1}$$

where $n$ is the subthreshold slope factor, and $U_T$ is the thermal voltage. This high efficiency makes weak inversion suitable for ultra-low-power circuits, though the low drain current requires large device dimensions, increasing gate capacitance and reducing bandwidth. It is ideal for power-critical applications but with trade-offs in speed and silicon area [10].

**Moderate Inversion**

Moderate inversion represents a transition between the strong and weak inversion regions. In this state, both diffusion and drift currents contribute to the drain current. Here, $V_{GS}$ is closer to $V_{TH}$, offering a balance between high efficiency and higher current levels. Modeling is complex, often relying on simulations. This region is preferred for low-power designs needing more speed than weak inversion can provide but with less power consumption than strong inversion [10].

**Strong Inversion**

In strong inversion, $V_{GS}$ significantly exceeds $V_{TH}$, fully inverting the channel [10]. In long-channel devices, the drain current is primarily governed by drift, following a quadratic relationship.

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{3.2}$$

where $\mu$ is carrier mobility, $C_{ox}$ is the oxide capacitance per unit area, $W$ is the channel width, and $L$ is the channel length. Short-channel effects like velocity saturation cause deviations from this model. $g_m/I_D$ decreases as $V_{GS}$ increases [10]. Strong inversion is used in high-speed circuits, with design trade-offs needed for power consumption.

Designers can efficiently size transistors and ensure they operate in the desired region weak, moderate, or strong inversion using this methodology, as summarized in Table 3.1 and the trade-offs are explained in detail at the end of this chapter in Table 3.2.

| **Operating Region** | **Transistor Efficiency ($g_m/I_D$)** |
|---|---|
| Strong | $< 10$ |
| Moderate | $22 > g_m/I_D > 10$ |
| Weak | $> 22$ |

Table 3.1: Operating Regions per Interval [14]

## Transistor Figures of Merit

The performance of analog circuits is influenced by various parameters such as current $I_D$, transconductance $g_m$, and intrinsic capacitances. The key figures of merit derived from

the Square law model include transconductance efficiency, transit frequency, and intrinsic gain [1]:

- **Transconductance Efficiency** ($g_{\mathrm{m}}/I_{\mathrm{D}}$)

$$\text{Transconductance efficiency} = \frac{g_m}{I_D} = \frac{2}{V_{ov}} \tag{3.3}$$

- **Transit Frequency** ($f_{\mathrm{T}}$)

$$\text{Transit frequency} = \frac{g_m}{C_{gg}} = \frac{3\mu V_{ov}}{2L^2} \tag{3.4}$$

- **Intrinsic Gain** ($A_{\mathrm{v}}$)

$$\text{Intrinsic gain} = \frac{g_m}{g_{ds}} = \frac{2}{\lambda V_{ov}} \tag{3.5}$$

These figures of merit are essential for optimizing transistor performance in analog circuits, and balancing power dissipation, speed, and gain.

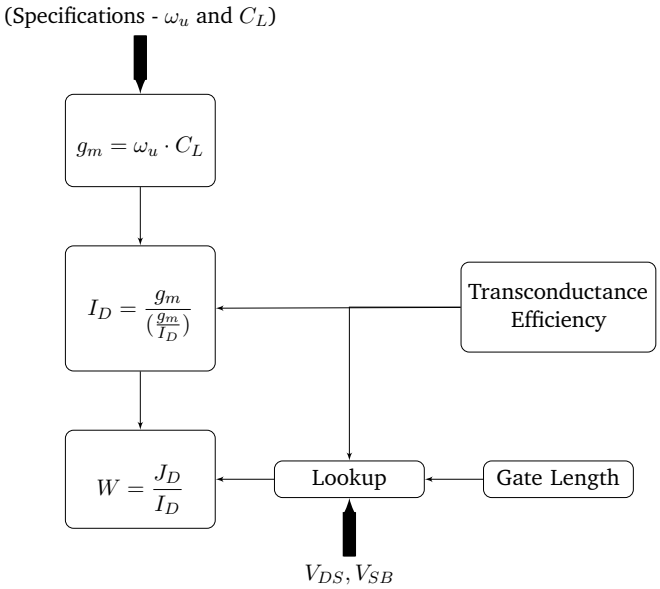


Figure 3.1: Flow of design [1]

## Design Flow

To design a MOSFET circuit for a specified unity-gain frequency ($f_u$) and load capacitance ($C_L$), first determine the desired $g_m$ according to the design specifications. Next, choose $L$, opting for a shorter length if higher speed and reduced area are priorities, or a longer length for increased gain and better matching. Then, select the $g_m/I_D$ ratio based on required specifications using Table 3.2.

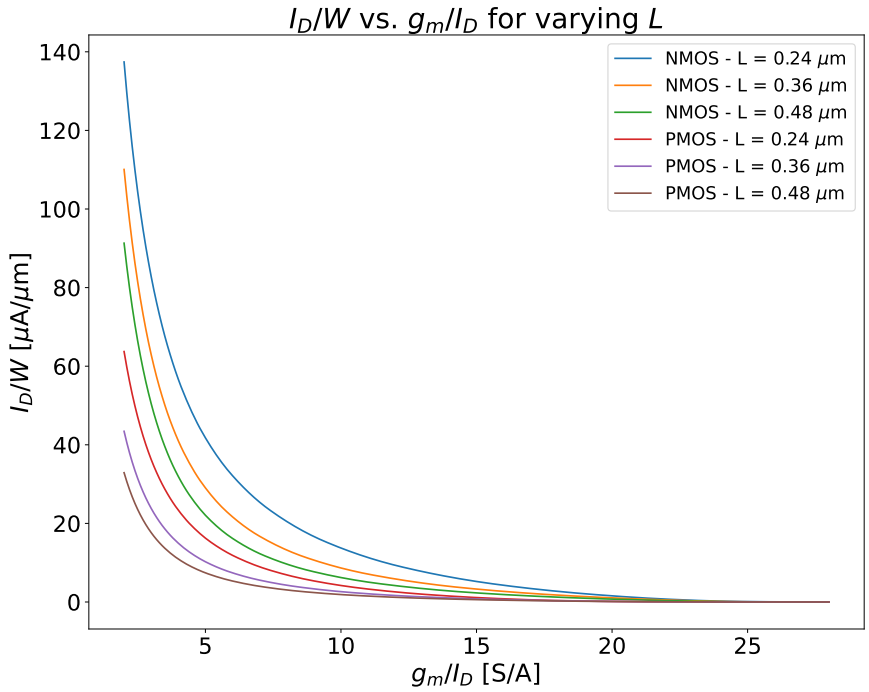


Figure 3.2: $I_D/W$ vs. $g_m/I_D$ Methodology

Calculate the drain current using the relationship between these parameters:

$$I_D = \frac{g_m}{\left(\frac{g_m}{I_D}\right)} \tag{3.6}$$

The current density can be known by using plots from $g_m/I_D$ versus $I_D/(W/L)$ as shown in Figure 4.3. Once the desired $I_D$ and $I_D/W$ are known, the transistor width $W$ can be calculated using:

$$W = \frac{I_D}{\left(\frac{I_D}{W}\right)} \tag{3.7}$$

This approach ensures the MOSFET meets the target unity-gain frequency and performance criteria. These plots give insight into the optimization of performance across different regions not only for widths but also for output resistance and capacitances. The relationship between $g_m/I_D$ and $I_D/(W/L)$ is independent of the Width of the transistor [2], thereby serving as a distinctive feature common to all transistors of the same type (NMOS or PMOS) across various CMOS fabrication technologies [10]. This study, analyzed NMOS and PMOS transistors across various channel lengths using UMC 65nm and GF 22nm technologies, with the characteristic curves being obtained for these transistors.

| **Parameter** | **Weak Inversion** | **Strong Inversion** |
|---|---|---|
| Transconductance | High | Low |
| $g_m/I_D$ value | High | Low |
| Power Consumption | Low | High |
| Gain | High | Low |
| Capacitance | High | Low |
| Transit Frequency (Speed) | Low | High |
| Output Signal Swing | High | Very Low |
| Transistor Size | Large | Small |
| Early Voltage ($V_A$) | Small | Large |
| Flicker Noise | Low (Large $W$) | High |

Table 3.2: Performance Parameters in Weak and Strong Inversion Regions [1, 10, 15]

The comparative analysis of key performance parameters for transistors operating in weak versus strong inversion regions, as summarized in Table 3.2, reveals distinct advantages and trade-offs associated with each region of inversion. In weak inversion, transistors exhibit high transconductance, gain, and $g_m/I_D$ value, resulting in lower power consumption and enhanced signal swing. These benefits, however, come at the cost of increased capacitance, slower transient frequency, and a smaller output voltage range.

Conversely, strong inversion operation is characterized by lower transconductance and gain but offers advantages such as higher speed, reduced transistor size, and a larger Early voltage, which is beneficial in high-speed applications. The trade-offs for strong inversion include higher power consumption, reduced signal swing, and elevated flicker noise, highlighting the different suitability of each regime depending on the specific performance requirements of the application.

# 4 LUT generation and Implementation of $g_m/I_D$ methodology tool in Python

This chapter presents the generation and implementation of a Python tool for $g_m/I_D$ methodology. It outlines the process of creating LUTs through four-dimensional sweeps using Cadence Spectre, optimizing simulation efficiency. Key topics include parameter setup, handling process corners, and temperature variations. The chapter also details the development of a graphical user interface (GUI) tool, which facilitates transistor design by enabling file uploads, plot generation, and width calculations, thereby supporting effective analysis and design.

## 4.1 Generation of Lookup Tables in Python

### Key Considerations for LUT generation

**1. Proportionality of $I_D$ to $W$:**

Recognizing that the drain current ($I_D$) is directly proportional to the transistor width ($W$) simplifies the design process. Consequently, parameters proportional to $I_D$—such as transconductance ($g_m$), output conductance ($g_{ds}$), and capacitances ($c_{gb}$, $c_{sb}$, $c_{db}$)—also scale with $W$. Noise parameters, including thermal and flicker noise, likewise increase with $W$ [10].

This proportionality assumes that $I_D$ scales directly with $W$, which is valid when the transistor is sufficiently large to negate narrow-width effects, a condition typically met in most analog circuits. While this model is well-suited for MOSFETs, it is less effective for other transistor types or more complex circuits, highlighting a limitation of this methodology.

**2. Independence of Parameter Ratios from $W$:**

The ratios of these parameters (e.g., $g_m/I_D$, $g_m{\cdot}r_o$, and Early voltage ($V_A$)) are independent of $W$. This independence allows for the storage of these parameters for a reference device width, facilitating later calculations for new design problems via cross-multiplication. Consequently, it suffices to characterize only a single reference width device while varying the length for each design [10, 16].

As technology scales down, increased variability and second-order effects make these assumptions more challenging to apply. Given that there is a one-to-one relationship between transconductance efficiency and current density for a specific $L$, $V_{DS}$, and $V_{SB}$, $J_D$ can be determined using the LUT data for this technology, thereby completing the sizing process [1].

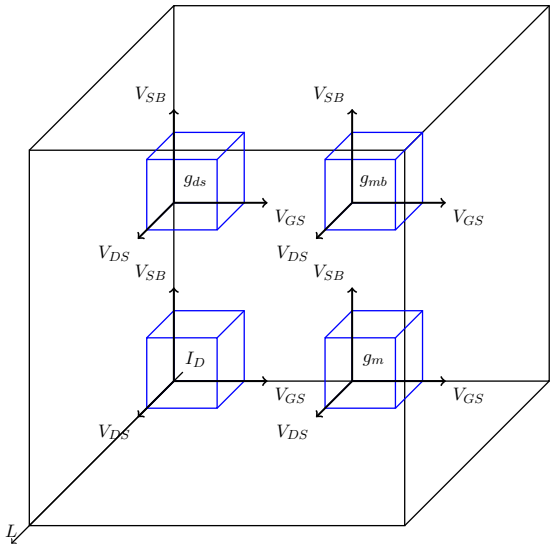


Figure 4.1: 4-Dimensional block of LUTs [10]

### Generation Process Flow

The LUTs used in this work are generated through four-dimensional ($L$, $V_{DS}$, $V_{GS}$, and $V_{SB}$) DC sweeps and noise analyses performed in Python using the Cadence Spectre circuit simulator Figure 4.1. The LUT generation process flow and the associated code are

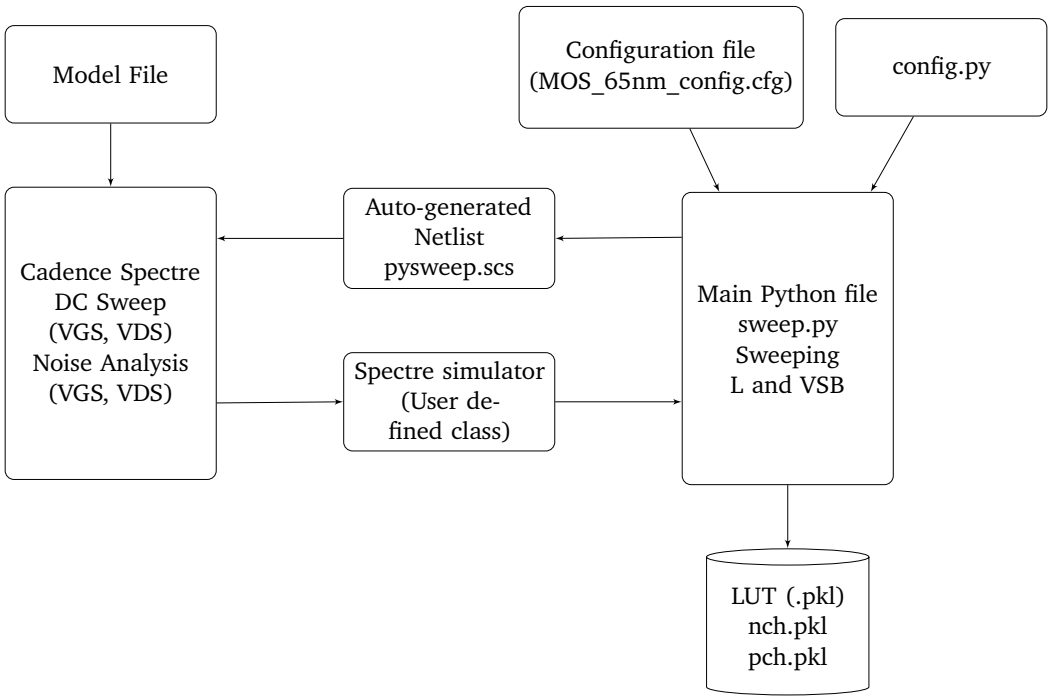


Figure 4.2: LUT generation using $g_m/I_D$ methodology adapted from [1]

adapted from Murmann's MATLAB code in [17] and referenced from Donnell's Pygmid code[18].

**Lookup Table Extraction from Simulation**

Although many simulators can execute four-dimensional sweeps, the workflow developed here in Figure 4.2 optimizes memory usage by handling two of the four dimensions through for-loops in the main block. This approach greatly reduces the risk of simulator memory overuse [1].

- **Primary Sweep:** Perform a sweep over $V_{GS}$, with $V_{DS}$ and $V_{SB}$ set to fixed values.
- **Length Sweep:** Sweep the length ($L$) over a few steps, with $W$ set to the reference value (Here 8 $\mu$m is taken).
- **Simulation:** Execute DC and noise sweeps, storing large signal and small signal parameters in arrays.

To achieve accurate results, the dependencies on $V_{DS}$ and $V_{SB}$ must be accounted for.

This necessitates sweeping these variables as well, resulting in a four-dimensional array. Once this process is completed, a 4D LUT for each parameter is obtained as shown in Figure 4.2.

After all simulation runs are completed, the data for each transistor is stored in LUT output files (65nch.pkl and 65pch.pkl). The pickle (.pkl) format is chosen for its storage efficiency compared to .csv and its simplicity relative to .h5 or others, while still offering a structured bit stream.

### Lookup Table Configuration and Output Variables

The configuration of output variables, parameter setup, and simulation environment settings are essential steps for generating LUTs. These configurations are crucial for extracting meaningful data from simulation results and tailoring the simulation setup to specific process corners and technology nodes.

**Output Variables, Parameter Definitions, and Sweep Setup**

- **Output Variables and Parameter Definitions**: The tool defines a list of output variables, such as `ID`, `VT`, `IGD`, etc., extracted from the simulation results. Each parameter is assigned a unique identifier and type, with corresponding weights determining its impact on the output variables. The parameters and their associated weights are stored in a dictionary under the key `n` [10].

Listing 4.1: Configuration of Output Variables and Parameters [10]

```
# output variables List
config['outvars'] = ['ID', 'VT', 'IGD', 'IGS', 'GM', 'GMB', '
   GDS', 'CGG', 'CGS', 'CSG', 'CGD', 'CDG', 'CGB', 'CDD', 'CSS'
   ]

# Definition of parameters
n = []
n.append(['mn:ids', 'A', [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0]])
n.append(['mn:vth', 'V', [0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0]])
# More parameters...
config['n'] = n
```

Above listing is the sample code snippet illustrating the configuration of output variables and parameters.

- **Sweep Parameters Setup**: The range for key parameters like `VGS`, `VDS`, `VSB`, and `Length` is configured in the associated configuration file, defining the sweep parameters for simulations.

Below is the code snippet illustrating the sweep setup:

Listing 4.2: Example Configuration for GPDK

```
temp = 300 #Nominal case
# Sweep parameters
#  (start,step,stop)
VGS = (0,0.1,1.8)
VDS = (0,0.1,1.8)
VSB = (0,0.1,0.7)
LENGTH = [(0.24,0.1,0.48)]
WIDTH = 8
NFING = 4
```

**Desiging for Process Corners**

The configuration settings are related to temperature and process corners, which are critical for simulating different operating conditions.

- **Temperature Configuration**: The `temp` parameter in the configuration file can be adjusted to generate LUTs for different temperature corners. For example:
  - `temp = 358 Kelvin` for high temperature.
  - `temp = 300 Kelvin` for nominal temperature.
  - `temp = 248 Kelvin` for low temperature.
- **Process Corner Selection**: To select a specific process corner (e.g., `ff`, `tt`, `ss`, `fs`, or `sf`), the corresponding section in the model library need to be referenced.

The $g_m/I_D$ design methodology assists designers in systematically addressing corner variations. By determining the worst-case deviations of $g_m/I_D$, $f_T$, $g_m/g_{ds}$, designers can typically adjust the design specifications in advance to ensure that the circuit meets the required margins across different corners [10].

However, it is crucial to emphasize that this methodology does not eliminate the need for SPICE verification across all corners, which remains essential before chip tape-out. Designers must still dedicate time to these verifications, as there are no shortcuts to this critical process [10].

**Generating Lookup Tables for New Technologies**

When working with new devices, such as HV transistors or RF transistors, or when using new technologies like BCD 130nm, it is essential to create and modify configuration files (.cfg). These files guide the simulation process, ensuring that the correct parameters are extracted for LUT generation.

**Utilizing Generated Lookup Tables**

Once the LUTs are generated using the modified configuration, they can be employed for subsequent simulations and analyses until new parameters need to be recalculated. This process ensures continuous adaptation and optimization of the simulation environment as new technologies and device types are introduced.

For both UMC 65nm and GF 22nm technologies, the resulting plots from the LUTs are validated using the basic NMOS and PMOS configurations. The curves generated by the GUI are in alignment with those obtained from Cadence SPECTRE.

## 4.2 Implementation of Graphical User Interface for $g_m/I_D$

The development of a GUI tool for the $g_m/I_D$ methodology in Python addresses the need for a more intuitive and efficient design process in analog circuit design. This tool simplifies complex calculations, such as plotting characteristic curves and determining transistor widths, by providing an accessible and user-friendly interface. It enhances visualization, streamlines the design workflow by automating repetitive tasks, and ensures consistency across different design projects. Additionally, the GUI serves as an educational resource, allowing users to explore the $g_m/I_D$ methodology interactively, thereby improving understanding and reducing the likelihood of errors. The primary features of the tool are mentioned hereafter in this section.

### File Upload and Transistor Type Selection

The GUI allows users to upload data files in either .pkl format (generated by Python) or .mat format (generated by MATLAB). It is important to note that .mat files converted from .pkl files are not supported, as this may lead to compatibility issues. Additionally, the interface includes a dropdown menu for selecting the transistor type, either PMOS or NMOS, which is crucial for subsequent analyses and plot generation.

### Circuit Selection and $g_m/I_D$ Values

The GUI offers a circuit selection feature, allowing users to determine verified $g_m/I_D$ values for their specific circuit configurations which are designed in this work. This ensures that transistor sizing aligns with the desired circuit specifications, optimizing overall performance.

### Input Parameters

The tool offers a variety of input parameters essential for conducting $g_m/I_D$ analysis, including:

- **nf:** Number of fingers
- **L:** Channel length (in $\mu$m)
- **VGS:** Gate-source voltage (in V)
- **VDS:** Drain-source voltage (in V)
- **VSB:** Source-bulk voltage (in V)
- $g_m/I_D$**:** Start, stop, and step values for the transconductance over drain current ratio (in S/A)

These input fields allow for the exploration of various transistor behaviors, with the capability to handle multiple values for $L$, $VGS$, $VDS$, and $VSB$, enabling users to generate plots that reflect different design scenarios. Figure 4.4 shows some of the plots from GUI. From GUI, plots of the following are obtained:

- $I_D/W$ *vs.* $g_m/I_D$ *for varying* $L$

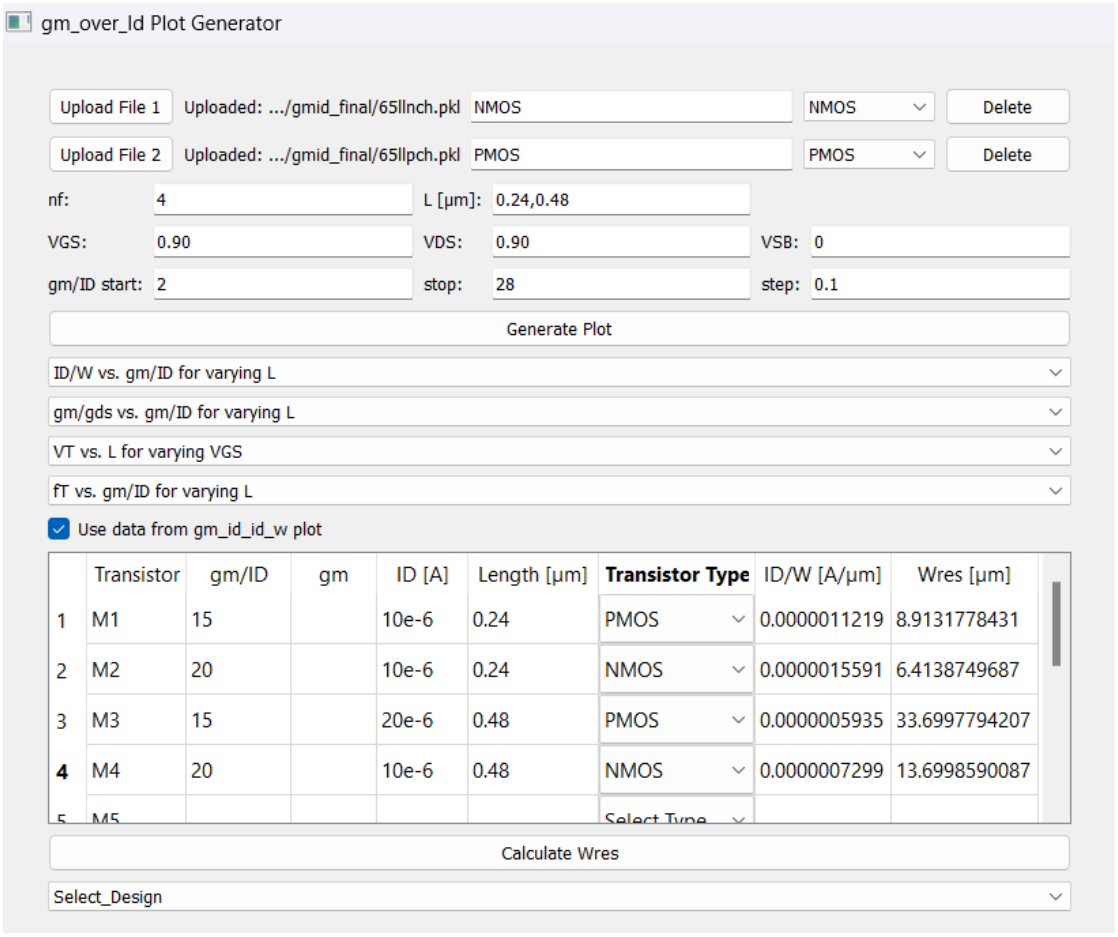


Figure 4.3: GUI for $g_m/I_D$ Methodology

- *$V_T$ vs. $L$ for varying $V_{GS}$*
- *$V_T$ vs. $V_{SB}$ for varying $V_{GS}$*
- *$f_T$ vs. $g_m/I_D$ for varying $L$*
- *$g_m/g_{ds}$ vs. $g_m/I_D$ for varying $L$*
- *$g_m/g_{ds}$ vs. $V_{DS}$ for varying $L$*
- *$g_{ds}$ vs. $V_{GS}$ for varying $L$*

- $g_{ds}$ *vs.* $V_{DS}$ *for varying* $V_{SB}$

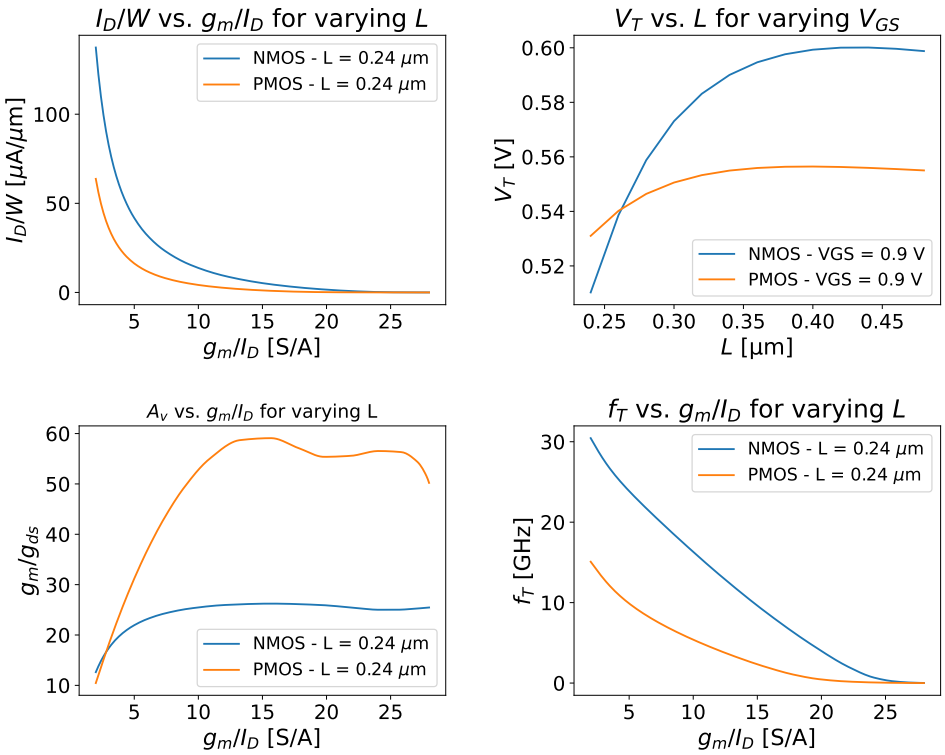


Figure 4.4: Plots from GUI for 240 nm and 480 nm Lengths in UMC 65nm

## Transistor Width Calculation using plot data

The tool includes a feature for calculating transistor widths, leveraging data from the $g_m/I_D$ vs. $I_D/W$ plot. Users can choose to calculate widths using the values from this plot, along with specified transistor type, $I_D$, and $L$ values. Alternatively, if the plot data is not used, the widths are calculated using provided $g_m$ or $I_D$ values and $I_D/W$, following

the modified formula mentioned in (3.7):

$$W = \frac{I_D}{(I_D/W)} \tag{4.1}$$

To enhance user experience, the tool provides a built-in troubleshooting guide and a readme button. These resources offer step-by-step instructions for resolving common issues, as well as detailed explanations of the tool's features and guidance on interpreting generated plots and calculated values.

# 5 Advanced Analog Circuit Design Using $g_m/I_D$ methodology

This chapter presents a detailed design and analysis of three fundamental analog circuits: the two-stage Miller operational amplifier (OpAmp), the latched comparator, and the telescopic operational transconductance amplifier (OTA). Each of these circuits is crucial for various analog applications, from amplification to precise signal comparison. The designs leverage the $g_m/I_D$ methodology, which optimizes transistor sizing to achieve superior performance and efficiency. The two-stage Miller OpAmp is designed based on the principles articulated by Arzate [14], while the latched comparator design is influenced by Vinoth's techniques [15] and considering Razavi's modified StrongARM Latch [19]. The telescopic OTA, known for its high-speed and power-efficient operation, follows the methodologies detailed in Angulo's work [20] and Gulati's studies [21]. By strategically selecting different transistor inversion regions, these designs not only simplify the implementation but also enhance performance in specific areas compared to the reference designs. This approach results in improved specifications, such as gain-bandwidth product and common-mode rejection ratio, thereby achieving more effective and efficient analog circuit solutions.

## 5.1 Two Stage Miller OpAmp Design

This section presents the design of a two-stage Miller amplifier using a step-by-step design approach. The op-amp is systematically divided into its components, and by using the $g_m/I_D$ method the transistor dimensions are determined to achieve the desired target specifications [14].

The two-stage Miller OpAmp, depicted in Figure 5.1, comprises a differential input stage followed by a common-source gain stage. The differential amplifier sets key performance

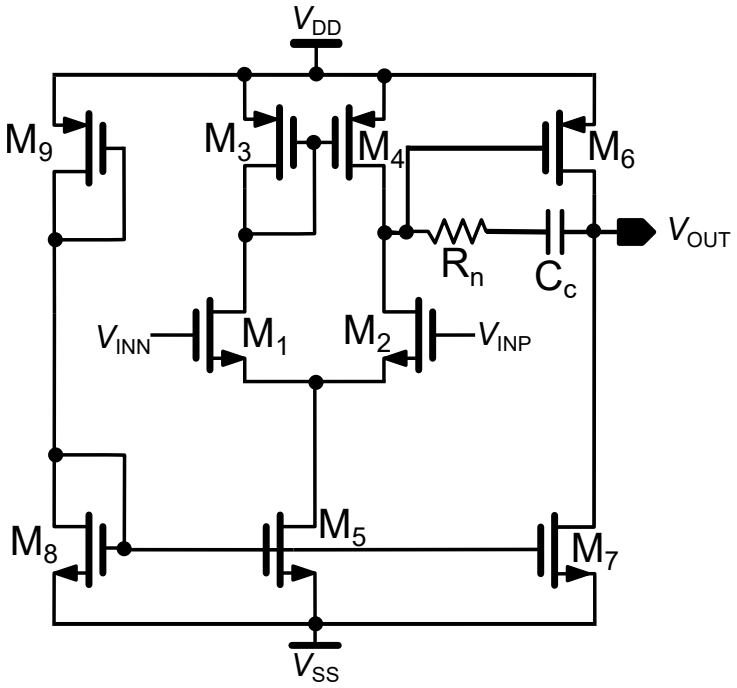


Figure 5.1: Two-Stage Miller Op-amp

parameters such as the CMRR and SR, while the second stage enhances the voltage gain. Between these stages, an RC network is present, depending on certain conditions.

To have proper stability of the design, especially when handling a capacitive load $C_L$, a $C_c$ is employed to adjust the phase margin via the Miller effect [22]. To counteract this, a cancellation resistor $R_n$ can be added in series with $C_c$ to remove the zero [23]. However, the effectiveness of $R_n$ in all cases can vary [14], necessitating careful design to balance stability and performance. The Cc affects the dominant pole by shifting it to lower frequencies, a phenomenon known as pole-splitting, while the non-dominant pole is pushed to higher frequencies. However, the presence of $C_c$ introduces a feedforward path that may result in a zero, which could adversely impact the phase margin and thus the stability of the system. In a Bode plot, this zero typically appears between the poles of the system [23]. To counteract this, a cancellation resistor Rn can be placed in series with $C_c$, which helps to eliminate the zero a $C_c$ is placed to ensure stability while handling $C_L$. This gives better PM via the Miller effect. Rn is added in series with cc to remove the zero [14].

$$\text{GBW} = \frac{g_{m1}}{C_c} \tag{5.1}$$

$$f_{\text{GBW}} = \frac{g_{m1}}{2\pi C_L} \tag{5.2}$$

$$\text{PM} \approx 90^\circ - \tan^{-1}\left(\frac{GBW}{\omega_{s2}}\right) \tag{5.3}$$

$$\text{SR} = \frac{I_{bias}}{C_c} \tag{5.4}$$

$$C_c \geq 0.22 * C_L \tag{5.5}$$

where $I_{bias}$ is the bias curent and the set equations (5.1 - 5.5) are required to design the Miller amplifier by taking into account design specifications shown in Table 5.3.

Using the above 3 equations the GBW, PM and SR can be calculated [22, 23].

These equations are essential for achieving the required performance.

| **Parameter** | **UMC 65nm** | **GF 22nm** |
|---|---|---|
| Supply Voltage [V] | 1.8 | 0.8 |
| Load Capacitor $C_L$ [pF] | 2 | 2 |
| Compensation Capacitor $C_c$ [pF] | 0.581 | 0.500 |
| Nulling Resistor $R_n$ [kOhms] | 5.13 | 5 |
| Biasing current $I_{bias}$ [µA] | 30 | 20 |

Table 5.1: Parameters for UMC 65nm and GF 22nm Technologies

### 5.1.1 Design using $g_m/I_D$ Methodology

The design process for the two-stage Miller OpAmp begins with defining the $C_c$ and the desired specifications. For this design, considering $C_L$ is 2 pF, using eq. 5.5 $C_c$ is set to 500 fF to ensure stability with a phase margin greater than 60° [14].

| UMC 65nm technology | | | | GF 22nm technology | | | |
|---|---|---|---|---|---|---|---|
| **Transistor** | **$g_m/I_D$** | **W [µm]** | **L [µm]** | **Transistor** | **$g_m/I_D$** | **W [µm]** | **L [µm]** |
| $M_{1/2}$ | 20 | 20.54 | 0.48 | $M_{1/2}$ | 25 | 2.63 | 0.08 |
| $M_{3/4}$ | 15 | 25.27 | 0.48 | $M_{3/4}$ | 22 | 4.35 | 0.08 |
| $M_{5/8}$ | 10 | 4.82 | 0.48 | $M_{5/8}$ | 10 | 0.296 | 0.08 |
| $M_6$ | 10 | 47.63 | 0.48 | $M_6$ | 20 | 8.15 | 0.08 |
| $M_7$ | 10 | 14.67 | 0.48 | $M_7$ | 15 | 1.266 | 0.08 |
| $M_9$ (bias) | 3.7 | 2.47 | 0.48 | $M_9$ (bias) | 26.3 | 170 | 0.02 |

Table 5.2: Sizing of transistors in UMC 65nm and GF 22nm Technology for two-stage Miller Amplifier

### Transistor Sizing Methodology for UMC 65nm

The design of the two-stage Miller op-amp is based on the $g_m/I_D$ methodology, which allows for systematic transistor sizing to meet specific performance targets. The transistor length $L$ is chosen according to the criterion $L \geq 2 \times L_{min}$, where $L_{min}$ represents the minimum length permissible in this technology.

**Calculation of Transconductance $g_m$ for Differential Pair:**

For transistors $M_{1,2}$ (the NMOS differential pair), the transconductance $g_{m1,2}$ is determined using the equation:

$$g_{m1,2} = 2\pi f_T C_c \tag{5.6}$$

Given that $f_T = 100\,\text{MHz}$ and $C_c = 500\,\text{fF}$, the calculated value is:

$$g_{m1,2} = 314.15\,\mu\text{S}$$

**Bias Current and $g_m/I_D$ Ratio:**

The bias current $I_{bias}$ is set to $30\,\mu\text{A}$, yielding a drain current $I_{D1,2} = 15\,\mu\text{A}$ for each transistor. The resulting $g_m/I_D$ ratio is:

$$\frac{g_{m1,2}}{I_{D1,2}} = 20.9\,\text{S/A}$$

This value, approximated to 20, indicates that the transistors are operating in the moderate inversion region (with $10 < g_m/I_D < 22$).

**Width Calculation for $M_{1,2}$:**

Using the chosen $g_m/I_D$ and the drain current $I_D$, the width $W$ of $M_{1,2}$ is calculated as:

$$W_{1,2} = 20.54\,\mu\text{m}$$

**Sizing of Current Mirror and Other Transistors:**

The current mirror transistors are operated in moderate inversion to ensure good matching and low noise. Other transistors in the design are sized to ensure operation within the moderate inversion region, achieving a balance between gain, power consumption, and speed [24].

**Sizing of $M_6$ (NMOS Gain Stage):**

From the analysis of the Miller amplifier, the transconductance $g_{m6}$ is set to three times $g_{m2}$, resulting in:

$$g_{m6} = 0.942\,\text{mS}$$

A $g_m/I_D$ ratio of 10 is chosen for $M_6$, leading to a current $I_{D6} = 94.2\,\mu$A and a width $W_6 = 47.63\,\mu$m.

**Summary of Current Values:**

All transistors are placed in the moderate inversion region to maintain a good balance between power and gain. This results in the following currents:

- $I_{D3,4} = I_{D1,2} = 15\,\mu$A
- $I_{D5} = I_{D8} = I_{bias} = 30\,\mu$A
- $I_{D5} = I_{D6} = 90\,\mu$A

### Transistor Sizing Methodology for GF22nm

A similar design procedure is followed for GF 22nm technology, with adjustments to account for technology scaling. The length $L$ is selected as $0.08\,\mu$m, which is more than twice the minimum length $L_{min}$ for this technology.

**Transconductance and $g_m/I_D$ Ratio for Differential Pair:**

For the differential pair $M_{1,2}$, operation in the weak inversion region is chosen to optimize power efficiency. The initial $g_m/I_D$ ratio is calculated as:

$$\frac{g_{m1,2}}{I_{D1,2}} = 31\,\text{S/A}$$

Given the extreme $g_m/I_D$ value of 30 for this technology, the design is fine-tuned to a more practical value of $g_m/I_D = 25$, which improves the Common-Mode Rejection Ratio (CMRR) while maintaining balance among other performance metrics.

**Bias Current and Width Calculation:**

The bias current $I_{bias}$ is set to $20\,\mu$A, leading to a drain current $I_{D1,2} = 10\,\mu$A. The width $W_{1,2}$ is determined as:

$$W_{1,2} = 2.63\,\mu\text{m}$$

**Sizing of $M_6$ (NMOS Gain Stage):**

The $g_{m6}$ value is calculated similarly, with $g_m/I_D = 20$ chosen to achieve a higher bandwidth. This results in:

$$W_6 = 8.15\,\mu\text{m}, \quad I_{D6} = 60\,\mu\text{A}$$

**Summary of Current Values:**

All transistors are placed in moderate inversion to maintain a balance between power and gain. This results in the following currents:

- $I_{D3,4} = I_{D1,2} = 10\,\mu$A
- $I_{D5} = I_{D8} = I_{bias} = 20\,\mu$A
- $I_{D5} = I_{D6} = 60\,\mu$A

### 5.1.2 Simulation Results and Discussion

The transistor dimensions are initially determined based on the design methodology described earlier, with adjustments made to optimize performance metrics. The specifications taken from the [25] for an ideal two-stage miller opamp.

| Parameter | Specification | Achieved Results | |
|---|---|---|---|
| | | **UMC 65nm** | **GF 22nm** |
| DC Gain [dB] | $> 50$ | 58.36 | 61.06 |
| GBW [MHz] | $\geq 20$ | 59.28 | 94.21 |
| Phase Margin [°] | $\geq 55$ | 72.6 | 69.56 |
| CMRR [dB] | $> 60$ | 68.24 | 68.12 |
| Slew Rate (+ve) [V/µs] | $\geq 15$ | 46.19 | 44.34 |
| Slew Rate (-ve) [V/µs] | $\geq 15$ | 45.24 | 44.42 |
| Settling Time (high) @5% error [ns] | $\leq 500$ | 12.97 | 4.815 |
| Settling Time (low) @5% error [ns] | $\leq 500$ | 17.84 | 10.75 |
| ICMR [V] (for UMC 65nm) | 0.5 … 1.3 | 0.414 … 1.398 | - |
| ICMR [V] (for GF 22nm) | 0.3 … 0.6 | - | 0.231 … 0.691 |
| Input Offset [mV] | $\leq 5$ | 0.648 | 2.645 |
| Input Referred Noise @20 kHz [nV/$\sqrt{\text{Hz}}$] | $\leq 55$ | 46.59 | 101 |
| Power [mW] | $\leq 0.6$ | 0.241 | 0.087 |

Table 5.3: Comparison of Specifications [14, 25] and Schematic Results for UMC 65nm and GF 22nm Technologies

For the design of a bias transistor, it is done by adjustment to get the required bias current. The open-loop frequency response of the amplifier, as shown in Figure 4, demonstrates a DC gain of approx $A_{DC,0} = 60\,\text{dB}$, and a phase margin of approx $PM = 70°$. It is important to note that if the resistor $R_n$ is removed from the circuit, the zero in the frequency response shifts to lower frequencies, which can cause phase margin degradation and potentially lead to instability. To prevent this, $R_n$ is utilized to shift the zero to frequencies higher than $f_T$, ensuring that the circuit behaves like a first-order system within the bandwidth of interest, up to $f_T$ [14].

Table 5.3 summarizes the performance metrics achieved for both the UMC 65nm and GF 22nm technologies. The results indicate that the designed amplifier meets or exceeds the specified targets for key parameters such as DC gain, gain-bandwidth product (GBW), phase margin, and power consumption. The GF 22nm technology, in particular, demonstrates a higher GBW and lower power consumption due to the smaller transistor sizes and optimized bias currents. Though it is considered the differential pair and current mirror

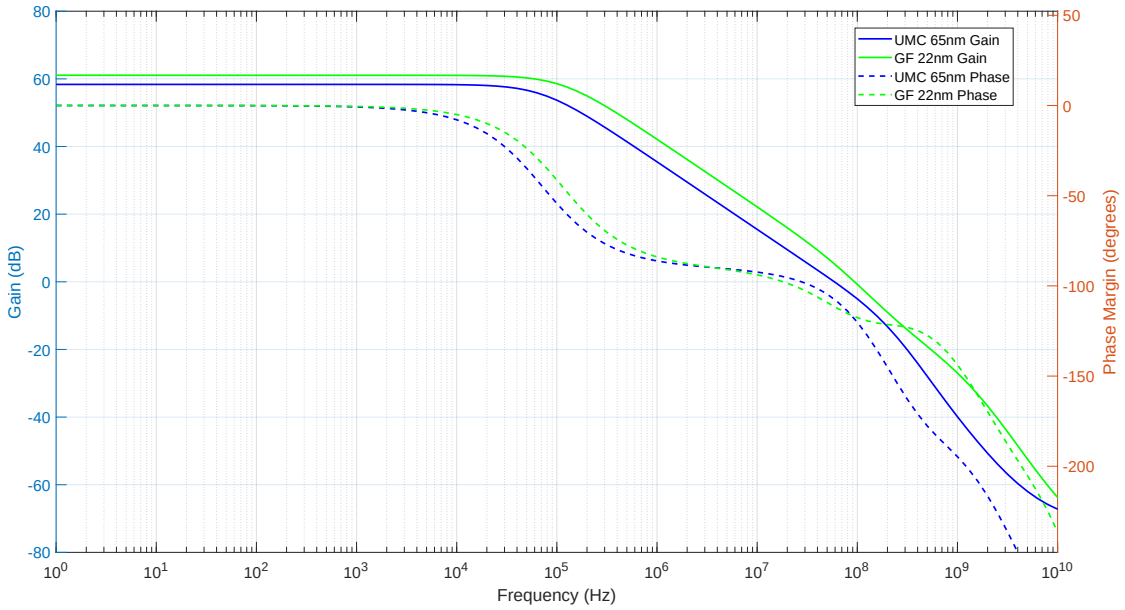


Figure 5.2: Gain and Phase plots of Two-Stage Miller OpAmp

more than 22, because of the same Cc, in (5.1) it is assumed that taking higher gm1 for GF 22nm leads to higher GBW. The main goal in this design is to show the results of 2stage OpAmp in moderate inversion region [14].

## 5.2 Design of High-Speed Latched Comparator

The design of analog circuits for high-speed applications involves several essential factors, including the choice of design methodology, accurate modeling, and thorough technology characterization [15]. This section presents the development of a high-speed latched comparator, optimized for low power consumption, leveraging the StrongARM latch topology. This topology is particularly suited for Analog-to-Digital Converters (ADCs) within System-on-Chip (SoC) environments due to its efficient power usage and robust performance. The StrongARM latch, first introduced by Kobayashi et al. [26] and later popularized due to its use in the StrongARM microprocessor, offers significant advantages such as zero static power dissipation, full rail-to-rail output swing, and a minimized

input-referred offset due to a simple differential pair design [19]. These features make it an ideal choice for low-power, high-speed circuit applications. This design, which is implemented in both UMC 65nm and 22nm CMOS technologies, employs the $g_m/I_D$ design methodology to optimally size the transistors, ensuring enhanced performance across different operating conditions [15].

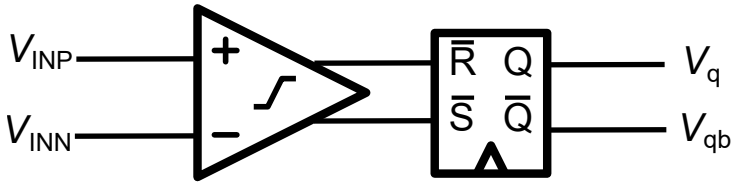


Figure 5.3: Latched comparator block diagram

### StrongARM Latch Circuit Operation

The StrongARM latch, a well-established topology, forms the core of the comparator design. The latch comprises an NMOS differential pair $M_{1/2}$ , cross-coupled inverters $M_3 - M_6$, a tail current source $M_7$, and pre-charge transistors $M_9 - M_{12}$. The operation of the StrongARM latch can be divided into two main phases: pre-charge and amplification.

During the *pre-charge phase*, when the clock (CLK) is low, the pre-charge switches $M_9 - M_{12}$ are turned on, charging the critical nodes (X and Y) to the supply voltage ($V_{DD}$). This ensures that the NMOS pairs $M_3 - M_4$ turn on, and the nodes P and Q are also precharged to $V_{DD}$. The common node between $M_1$, $M_2$, and $M_7$ is precharged to $V_{DD}$-$V_{tn}$, preparing all capacitances for the next evaluation [15].

In the *amplification phase*, as CLK goes high, the pre-charge switches are turned off, and $M_1$ and $M_2$ are turned on, drawing a differential current proportional to the applied potential difference ($V_{INP}$-$V_{INN}$). This current discharges the nodes X and Y through the NMOS transistors ($M_3$, $M_1$, $M_7$ for X, and $M_4$, $M_2$, $M_7$ for Y), resulting in a growing differential voltage $|V_X$-$V_Y|$ that exceeds the input difference $|V_{INP}$-$V_{INN}|$. This phase provides differential gain, critical for the comparison process. As the voltage at X and Y continues to drop, either $M_5$ or $M_6$ turns on, leading to one of the nodes falling to zero while the other reaches $V_{DD}$, thus completing the comparison [19, 15].

The transistors $M_3 - M_4$ cut off the DC path to ground at the end of this phase, preventing static power drain, while $M_5 - M_6$ restore the output nodes to $V_{DD}$, ensuring rail-to-

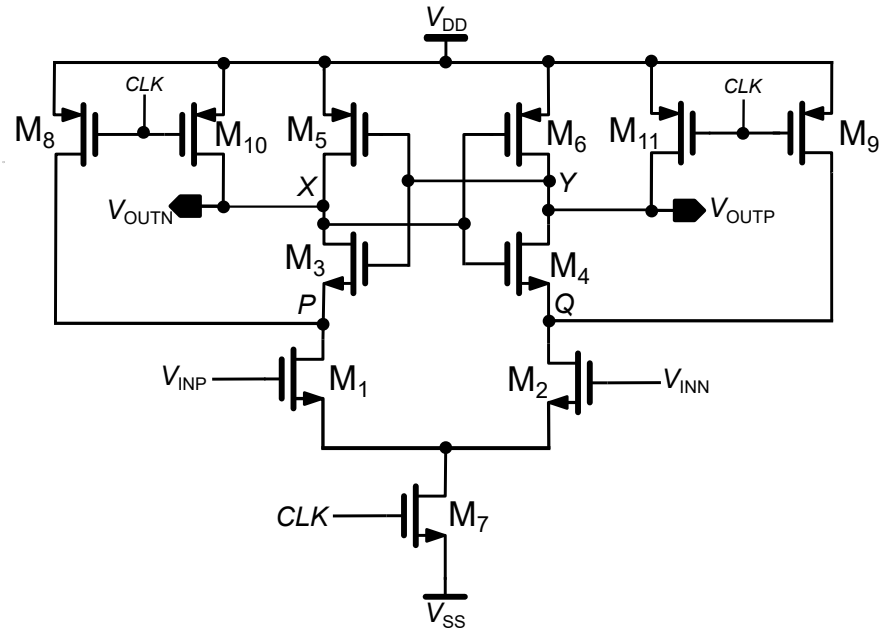


Figure 5.4: Modified Strong ARM Latch [19]

rail output swing. The pre-charge switches also reset the output nodes for every clock cycle, clearing previous values and establishing an initial voltage of $V_{DD}$ at nodes X and Y, ensuring that $M_5 - M_6$ remain off before amplification [19, 15].

### Data Holding using RS Latch

Since the StrongARM latch provides valid outputs only during a specific segment of the clock cycle, an RS latch is utilized to preserve the output value until the subsequent comparison cycle.

Traditional RS latches often exhibit output asymmetry, where one output is consistently delayed relative to the other. To address this issue, a modified RS latch as described by [2] is used, in which the outputs $V_{\mathrm{q}}$ and $V_{\mathrm{qb}}$ are made independent of each other through logical expressions involving solely the inputs and current states. This approach minimizes the number of P-type transistors required and ensures that both outputs experience the same delay [15].

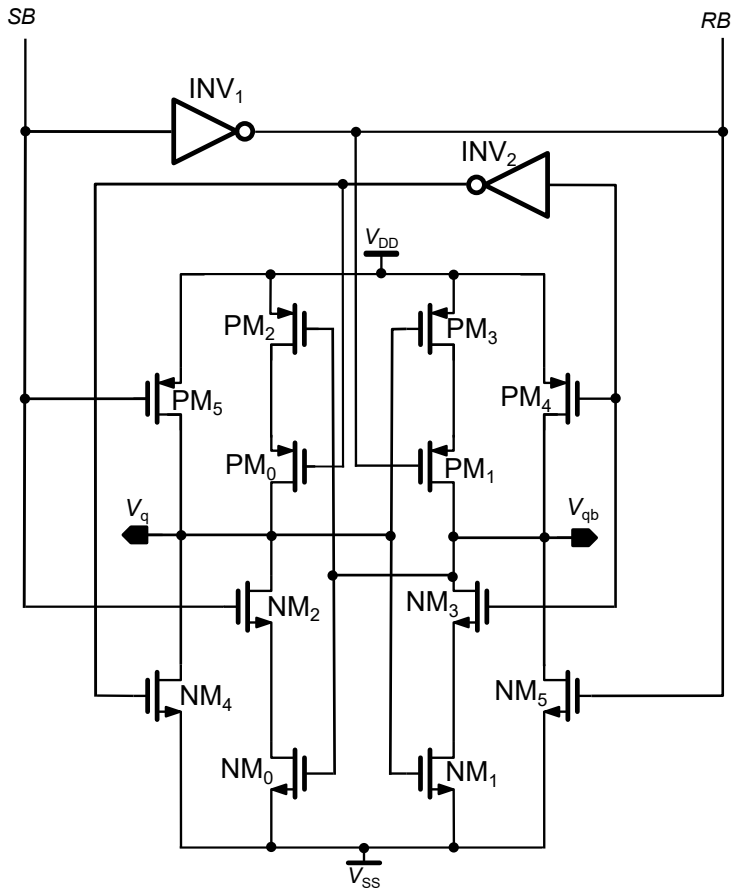


Figure 5.5: RS Latch

Define $Q(n)$ and $\overline{Q}(n)$ as the current state outputs. The next states $Q(n+1)$ and $\overline{Q}(n+1)$ are represented as follows:

$$Q(n+1) = S + \overline{R} \cdot Q(n) \tag{5.7}$$

$$\overline{Q}(n+1) = R + \overline{S} \cdot \overline{Q}(n) \tag{5.8}$$

These equations are realized using an AND-OR configuration, with $S$ forming an OR

branch. This design minimizes the number of P-type transistors responsible for switching from 0 to 1 [15].

Maintaining symmetry is essential for preserving the accuracy of the digital output signal, particularly at high speeds [19]. The symmetrical design allows the use of small keeper transistors, which rapidly turn off during state transitions, thus enabling the driver transistors ($NM_4$, $PM_5$, $PM_4$, $PM_5$) to effectively alter the latch state and drive the load [19].

### 5.2.1 Design Using $g_m/I_D$ Methodology

In the design of the StrongARM latch, the $g_m/I_D$ methodology is employed to size the transistors for optimal performance under given constraints. The inversion region of the transistors is carefully chosen based on the guidelines provided in [15], which served as a critical reference point in determining the appropriate dimensions to achieve the desired performance metrics.

Considering the Table 3.2, here for StrongARM latch the most critical parameters are Transient Frequency (Speed), Signal Swing, and Gain. Strong inversion is usually preferred despite its lower transconductance, signal swing, and gain, because it provides the necessary speed and lower capacitance required for the high-speed operation of latched comparators.

To calculate the average power dissipation from the supply voltage over a single comparison period, the following equation is employed [27]:

$$P_{\text{avg}} = \frac{1}{T} \int_0^T V_{DD} \cdot I_D \, dt \tag{5.9}$$

where $T$ denotes the duration of the comparator's clock cycle, and $I_D$ represents the total current drawn from the supply voltage. This equation can alternatively be expressed as:

$$P_{\text{avg}} = f_{\text{CLK}} \cdot \int_0^T V_{DD} \cdot I_D \, dt = f_{\text{CLK}} \cdot V_{DD} \cdot \int_0^T I_D \, dt \tag{5.10}$$

To achieve high gain during the amplification phase while keeping power consumption controlled, the strong to moderate inversion region is where the differential pair transistors are operated. The increase in transistor sizes leads to larger precharge capacitances in

| UMC 65nm technology | | | | GF 22nm technology | | | |
|---|---|---|---|---|---|---|---|
| **Transistor** | **$g_m/I_D$** | **W [µm]** | **L [µm]** | **Transistor** | **$g_m/I_D$** | **W [µm]** | **L [µm]** |
| $M_{1/2}$ | 15 | 9.5 | 0.24 | $M_{1/2}$ | 12 | 0.726 | 0.04 |
| $M_{3/4}$ | 8 | 2.44 | 0.24 | $M_{3/4}$ | 8 | 0.306 | 0.04 |
| $M_{5/6}$ | 8 | 7.25 | 0.24 | $M_{5/6}$ | 8 | 0.632 | 0.04 |
| $M_7$ | 12 | 10.7 | 0.24 | $M_7$ | 12 | 1.45 | 0.04 |
| $M_{8/9}$ | 8 | 8.71 | 0.24 | $M_{8/9}$ | 8 | 0.759 | 0.04 |
| $M_{10/11}$ | 8 | 8.71 | 0.24 | $M_{10/11}$ | 8 | 0.759 | 0.04 |

Table 5.4: Sizing of transistors in UMC 65nm and 22nm Technology for StrongARM Latch

the StrongARM circuit, which subsequently results in higher power consumption [15]. To manage this issue, a $(g_m/I_D)$ ratio of 15 is selected for UMC 65nm technology and 12 for GF 22nm technology for the transistors $(g_m/I_D)_1$ and $(g_m/I_D)_2$.

The effective discharge of the main differential pairs is the responsibility of the tail current source transistor $M_7$. To ensure that the tail current source remains in saturation, a $(g_m/I_D)$ ratio less than 10 is chosen for $(g_m/I_D)_7$. Similarly, the operating regions of other transistors dictate their respective $(g_m/I_D)$ ratios [15]. Speed is prioritized for the StrongARM latch, leading to the choice of a $(g_m/I_D)$ ratio of 8 for both technologies. The $(W/L)$ ratios for the transistors are approximated based on $(g_m/I_D)$ curves, and transistor sizes are refined through simulations to meet the desired specifications. Table 5.4 displays the widths and lengths of the transistors used in these simulations. Fernando's analysis showed that traditional approaches tend to overestimate power dissipation and require larger transistors to achieve comparable gain [24].

Sizing adjustments for the driving transistors are made according to the load of the subsequent stage, as outlined in Table 5.5. In this modified RS latch design, equal drive strength and delay are ensured for both the true and complementary outputs. This balance is essential for effective latched comparator operation [15].

### 5.2.2 Simulation Results and Discussion

The performance of the Latched Comparator is evaluated through simulations conducted in both UMC 65nm and GF 22nm technologies. The circuit is operated with a supply voltage of 1.8 V for the UMC 65nm technology and 0.8 V for the GF 22nm technology,

| RS Latch Transistor Sizes | | |
|---|---|---|
| **Technology** | **Transistor** | **Size (W/L)** |
| **UMC 65nm** | $NM_{0/1/2/3}$ | 2.2 µm / 240 nm |
| | $PM_{0/1/2/3}$ | 4.29 µm / 240 nm |
| | $NM_{4/5}$ | 6 µm / 240 nm |
| | $PM_{4/5}$ | 9 µm / 240 nm |
| **GF 22nm** | $NM_{0/1/2/3}$ | 240 nm / 40 nm |
| | $PM_{0/1/2/3}$ | 240 nm / 40 nm |
| | $NM_{4/5}$ | 600 nm / 40 nm |
| | $PM_{4/5}$ | 500 nm / 40 nm |

Table 5.5: Transistor sizes for RS Latch in UMC 65nm and GF 22nm technologies

with a capacitive load of 20 fF applied to both outputs. The clock frequencies used are 909 MHz for the UMC 65nm technology and 2 GHz for the 22nm technology. The key performance metrics, including delay, power consumption, and power delay product (PDP), are summarized in Table 5.6.

| **Parameter** | **Vcm = 0.8 V UMC 65nm** | **Vcm = 0.5 V GF 22nm** |
|---|---|---|
| Supply (V) | 1.8 | 0.8 |
| Load Capacitance (fF) | 20 | 20.2 |
| Operating frequency (GHz) | 0.909 | 2 |
| Average Delay (ps) | 521 | 154 |
| Power (mW) | 0.437 | 0.011 |
| PDP (pJ) | 0.227 | 0.00169 |
| Output Swing (V) | -0.101 to 1.857 | -0.003 to 0.809 |

Table 5.6: Simulation Results for UMC 65nm and 22nm Technology

For the UMC 65nm technology, using the data from plot 5.7, the average delay is calculated to be 0.521 ns. This value reflects the overall time delay experienced in the circuit, providing a crucial metric for evaluating the speed and efficiency of the design within this technology node. The relatively low average delay underscores the effectiveness of the transistor sizing and the design choices made during the implementation process.

For the GF 22nm technology, using the plot 5.9 the average delay is

$$\text{Average Delay} = 0.15454 \text{ ns}$$

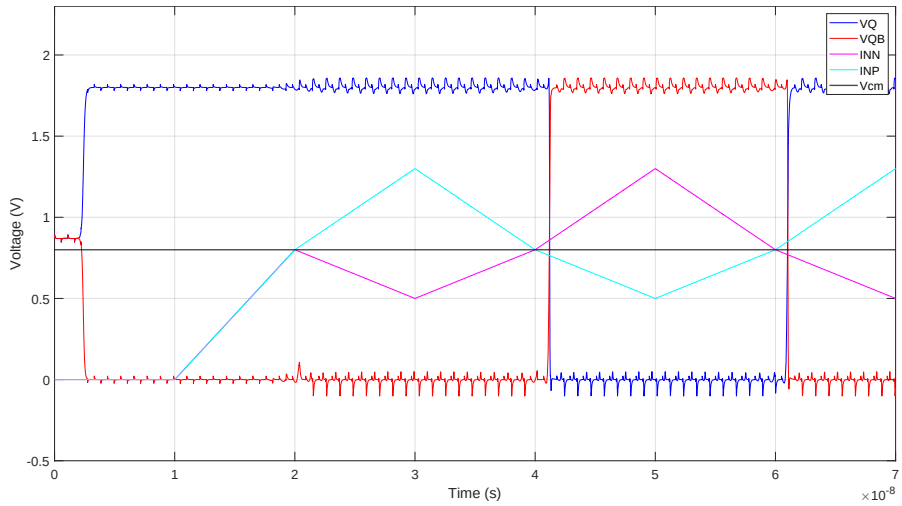


Figure 5.6: Output of Comparator at 909 MHz Clock in UMC 65nm

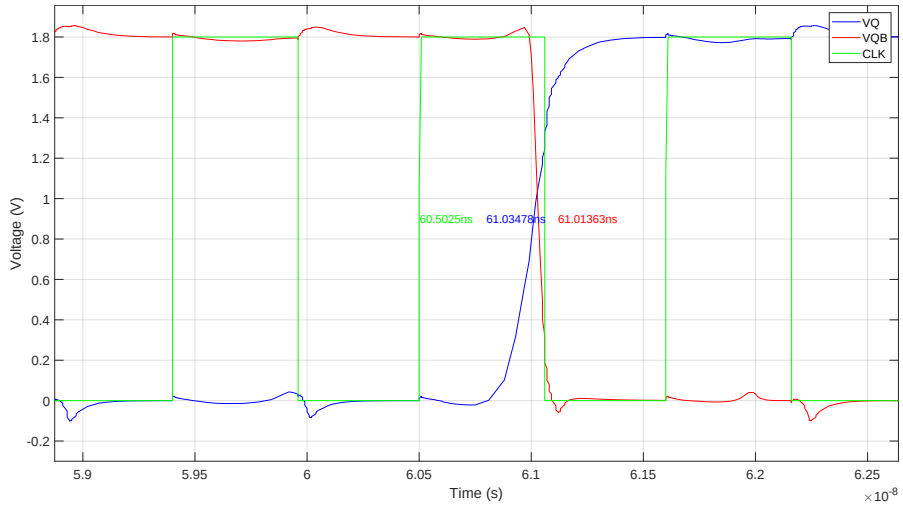


Figure 5.7: Delay measurement of Latched Comparator in UMC 65nm

The delay measurement and output waveforms for the UMC 65nm technology are shown in Figures 5.6 and 5.7, respectively. The delay measurement and output waveform for the 22nm technology are depicted in Figures 5.8 and 5.9, respectively.

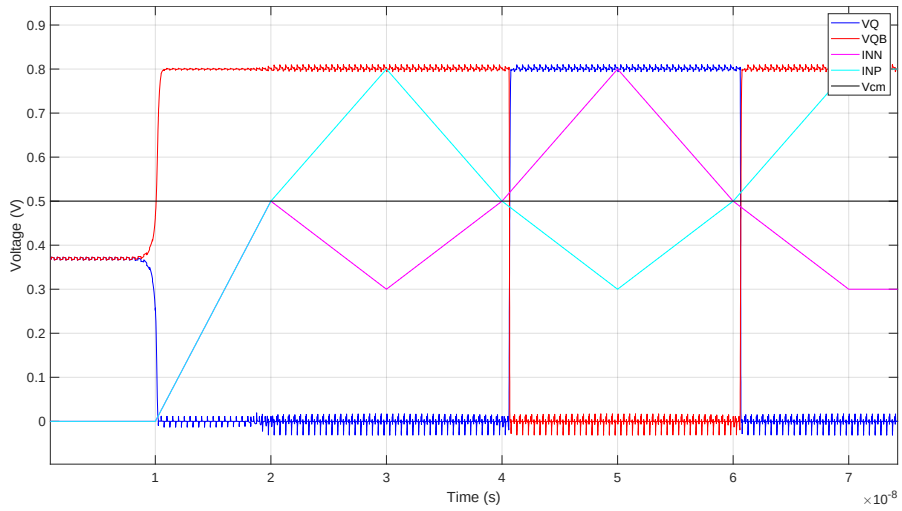


Figure 5.8: Output of Comparator at 2 GHz Clock in GF 22nm

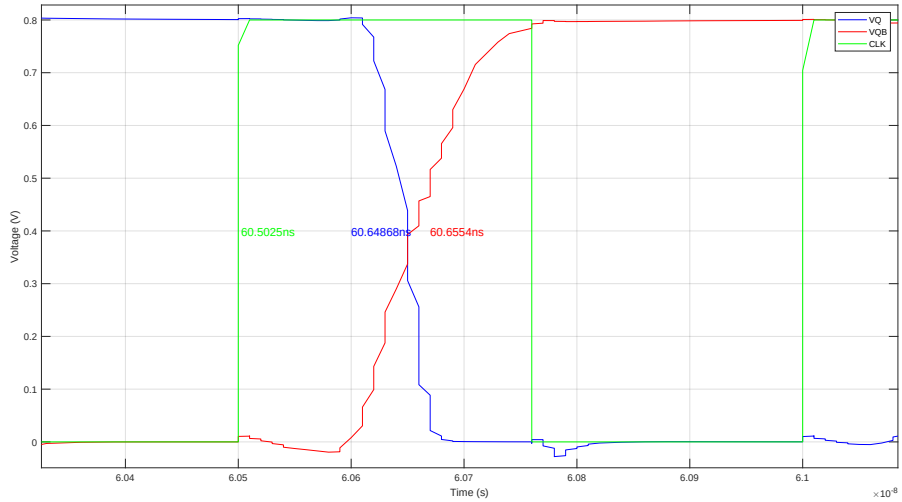


Figure 5.9: Delay measurement of Latched Comparator in GF 22nm

The results, including delay, power consumption, and power delay product (PDP) for both technologies, are detailed in Table 5.6. The plots provide visual confirmation of the comparator's performance at different clock frequencies, demonstrating the efficiency improvements achieved with the GF 22nm technology compared to the UMC 65nm

technology.

Overall, the StrongARM latch design predominantly operates in strong inversion, except for the differential pair, which functions in moderate inversion. This design choice optimizes performance characteristics such as gain and power consumption. In contrast to [15], where all transistors are designed to operate in strong inversion, this approach, after a few iterations, demonstrates improved delay and operating frequency by taking moderate inversion for the differential pair. Although the delay and operating frequency achieved for UMC 65nm in this thesis are not as high as those in [15], the area, power, and power-delay product (PDP) have been significantly reduced, resulting in a more efficient design.

## 5.3 Design of Telescopic OTA

The telescopic Operational Transconductance Amplifier (OTA) is chosen due to its simplicity, which facilitates higher-speed operation compared to other architectures.

Contrasting a folded-cascode design which features an input differential pair and separate current branches for differential outputs, the telescopic design integrates both the input differential pair and the output onto the same two current branches [21]. This integration eliminates noise issues associated with current mirrors and provides a more direct signal path, thereby enabling higher speed. Additionally, the telescopic architecture is more power-efficient, utilizing only half the bias current of a folded-cascode design because it requires fewer current branches.

The telescopic OTA is favoured for its compact structure, high voltage swing, substantial voltage gain, and overall efficiency [20]. Despite potential degradations in differential gain, common-mode rejection ratio (CMRR), and other amplifier characteristics, these can be effectively mitigated using techniques such as regulated cascode differential gain enhancement and replica-tail feedback [21]. The biasing voltages, supply voltages, and biasing currents are set as shown in Table 5.7.

The telescopic cascode OTA enhances power efficiency by achieving a high open-loop gain ($A_o$) and output resistance ($r_{out}$) without requiring an additional stage.

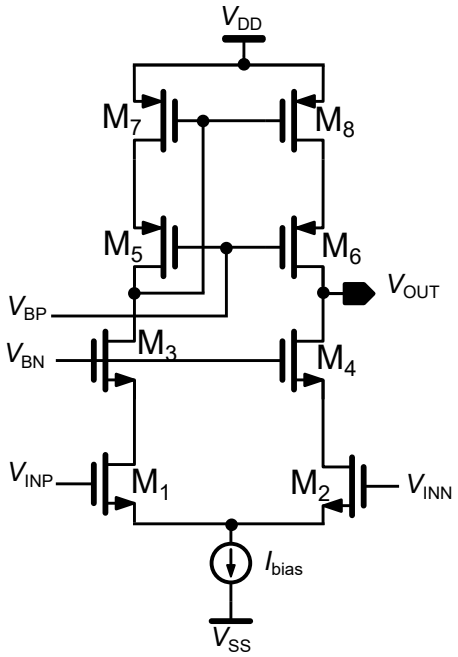


Figure 5.10: Telescopic amplifier

| Parameter | 65nm Technology | 22nm Technology |
|---|---|---|
| $V_{DD}$ (Supply Voltage) | 1.8 V | 1.2 V |
| $V_{BN}$ (NMOS Bias Voltage) | 1.12 V | 670 mV |
| $V_{BP}$ (PMOS Bias Voltage) | 1.12 V | 670 mV |
| $I_{bias}$ (Biasing Current) | 20 µA | 20 µA |
| $C_L$ (Load capacitance) | 1 pF | 1 pF |

Table 5.7: Biasing and Supply Parameters for UMC 65nm and 22nm Technologies

### 5.3.1 Design Methodology and Transistor Sizing

The design methodology for the telescopic OTA involved the strategic application of the $g_m/I_D$ methodology to optimize transistor sizing in both UMC 65nm and GF 22nm technologies. This approach allowed for the precise adjustment of transistor dimensions to achieve desired performance characteristics while maintaining efficiency.

In this design, key parameters include the $I_{\text{bias}}$, $C_L$, and supply voltages, as detailed in

| UMC 65nm technology | | | |
|---|---|---|---|
| Transistors | $g_m/I_D$ | W [µm] | L [µm] |
| $M_{1/2}$ | 10 | 1.15 | 0.36 |
| $M_{3/4}$ | 24.5 | 117 | 0.36 |
| $M_{5/6}$ | 15 | 12.58 | 0.36 |
| $M_{7/8}$ | 15 | 12.58 | 0.36 |

Table 5.8: Sizing of transistors in 65nm Technology for Telescopic Amplifier Design

| GF 22nm technology | | | |
|---|---|---|---|
| Transistors | $g_m/I_D$ | W [µm] | L [µm] |
| $M_{1/2}$ | 10 | 0.78 | 0.5 |
| $M_{3/4}$ | 24.5 | 13.07 | 0.5 |
| $M_{5/6}$ | 15 | 4.24 | 0.5 |
| $M_{7/8}$ | 15 | 4.24 | 0.5 |

| GF 22nm technology - Alternate Sizing | | | |
|---|---|---|---|
| Transistors | $g_m/I_D$ | W [µm] | L [µm] |
| $M_{1/2}$ | 11 | 0.6 | 0.3 |
| $M_{3/4}$ | 24.5 | 1.91 | 0.06 |
| $M_{5/6}$ | 15 | 0.704 | 0.06 |
| $M_{7/8}$ | 15 | 0.704 | 0.06 |

Table 5.9: Sizing of transistors in 22nm Technology for Telescopic Amplifier Design

Table 5.7. The $I_{\text{bias}}$ is set at 20 µA for both technology nodes, and the $C_L$ is maintained at 1 pF. These parameters are chosen to balance the trade-offs between speed, stability, and power consumption.

The GBW of the OTA is a critical performance metric and is calculated using the formula:

$$f_{\text{GBW}} = \frac{g_{m1}}{2\pi C_L} \tag{5.11}$$

$$g_{m1} = 2\pi C_L \cdot f_{\text{GBW}} \tag{5.12}$$

For this design, $g_{m1}$ is determined based on the desired GBW and the $C_L$, ensuring that the amplifier meets the required frequency response specifications $g_{m1} = g_{m2}$

The slew rate (SR) is another important parameter and is given by:

$$SR = \frac{I_{bias}}{C_L} \tag{5.13}$$

$$I_{bias} = SR \cdot C_L \tag{5.14}$$

This relationship ensures that the amplifier can respond quickly to input signal changes, with the biasing current ($I_{\text{bias}}$) set to support the desired slew rate while optimizing power consumption. Since the bias current is 20 µA, it is divided equally between the differential pair, resulting in all transistors in the circuit carrying a current of 10 µA.

The transistors are sized according to their $g_m/I_D$ ratios to achieve optimal performance:

- **Differential Pair ($M_{1/2}$):** A $g_m/I_D$ of 10 is selected for the differential pair transistors, placing them in moderate inversion. This choice balances speed and power consumption, providing the high transconductance efficiency necessary for achieving the desired gain and bandwidth. Although weak inversion ideally provides higher gain, a $g_m/I_D$ of 10 is chosen to optimize the area. The transistor dimensions for the 65nm and 22nm technologies are listed in Table 5.8 and Table 5.9.
- **NMOS Biasing Transistors ($M_{3/4}$):** With a $g_m/I_D$ of 24.5, the NMOS biasing transistors are designed to operate in weak inversion. This design choice enhances transconductance efficiency and improves the CMRR, contributing to higher overall gain and lower power consumption.
- **PMOS Transistors ($M_{5/6}$, $M_{7/8}$):** These transistors are designed with a $g_m/I_D$ of 15, operating in moderate inversion. This choice ensures a balance between speed and power dissipation and provides the necessary drive strength for the current mirror without excessively increasing power usage.

The widths (W) of the transistors are determined based on the $g_m/I_D$ values, ensuring that the design meets the required performance specifications while optimizing for power and area. This sizing approach, combined with the specified biasing current and load capacitance, allowed for the achievement of high performance in both the 65nm and 22nm technology nodes, as summarized in Tables 5.8 and 5.9.

### 5.3.2 Simulation Results and Discussion

For both technology nodes, the moderate inversion operation of the differential pair and PMOS transistors enabled a favourable balance between gain and power efficiency. The achieved DC gains and gain-bandwidth products are detailed in Table 5.10. Specifically, the 65nm design attained a DC gain of 44.64 dB and a gain-bandwidth product (GBW) of 13.8 MHz. In comparison, the 22nm technology demonstrated even higher performance, with an increased DC gain and GBW, attributable to the enhanced transistor characteristics at smaller nodes. Here specifications are taken from [25] with minor modifications such

as DC Gain, GBW and SR. Due to the single-stage design here, a DC gain of only 40 and GBW of 10 is chosen.

| Parameter | Specification | GF 22nm Technology | | UMC 65nm Technology Achieved Results |
|---|---|---|---|---|
| | | L = 0.5 µm | Alternate L | |
| DC Gain [dB] | > 40 | 45.49 | 40.47 | 44.64 |
| GBW [MHz] | $\geq$ 10 | 14.52 | 18.14 | 13.8 |
| Phase Margin [°] | $\geq$ 55 | 86.21 | 90.73 | 82.14 |
| CMRR [dB] | > 60 | 60.08 | 60.71 | 65.42 |
| Slew Rate (+ve) [V/µs] | $\geq$ 10 | 10.18 | 9.393 | 14.68 |
| Slew Rate (-ve) [V/µs] | $\geq$ 10 | 10.19 | 9.372 | 14.67 |
| Settling Time (high) @5% error [ns] | $\leq$ 500 | 33.78 | 31.05 | 35.37 |
| Settling Time (low) @5% error [ns] | $\leq$ 500 | 30.34 | 27.97 | 34.12 |
| ICMR [V] (UMC 65nm) | 0.5 ... 1.2 | - | - | 0.402 ... 1.352 |
| ICMR [V] (GF 22nm) | 0.3 ... 0.9 | 0.103 ... 0.992 | 0.104 ... 0.945 | - |
| Input Offset [mV] | $\leq$ 10 | -0.272 | -0.8905 | -1.455 |
| Power [mW] | $\leq$ 0.6 | 0.024 | 0.024 | 0.037 |

Table 5.10: Comparison of Specifications[25] and Achieved Results for UMC 65nm and GF 22nm Technologies.

The phase margin, critical for stability, is measured at 82.14° for the UMC 65nm design, as shown in the gain and phase margin plot. This plot highlights the OTA's stability under various conditions. The GF 22nm design also showed an improved phase margin, reinforcing the stability and robustness of the amplifier. The phase margin improvements can be observed in the corresponding phase margin plot Figure 5.11, which illustrates the enhanced stability achieved with the 22nm technology.

The NMOS biasing transistors ($M_{3/4}$), operating in the weak inversion region, are chosen to maximize transconductance efficiency and improve CMRR. This design choice resulted in a CMRR of 65.42 dB for the UMC 65nm technology, with similar enhancements in the GF 22nm technology. The improved CMRR, as depicted in the CMRR performance plots, demonstrates the effectiveness of the weak inversion operation in achieving superior differential signal processing.

The comparison of transistor inversion regions with the obtained results validates the design strategy. The moderate inversion regions of the differential pair and PMOS transistors provided the required gain and stability, while the weak inversion for NMOS biasing transistors significantly enhanced the CMRR. The gain and phase margin plots, along with the performance metrics, confirm that the design choices effectively achieved the desired amplifier characteristics, including high gain, stability, and efficient common-mode rejection.

The presented designs demonstrate that there is no specific inversion region for a particular design or set of transistors. As evidenced in Tables 5.2, 5.4, and 5.8, the differential pair can operate in weak inversion, moderate inversion, or strong inversion depending on the primary objective of the design. For instance, if speed is the priority, it is advisable to begin in strong inversion and then move toward moderate inversion. Conversely, if power efficiency is the main concern, starting in weak inversion and progressing toward moderate inversion is more appropriate. The optimal region, however, is determined by the initial calculations of bias current, transconductance ($g_m$), and other design parameters such as load capacitance, gain-bandwidth product, and slew rate equations.

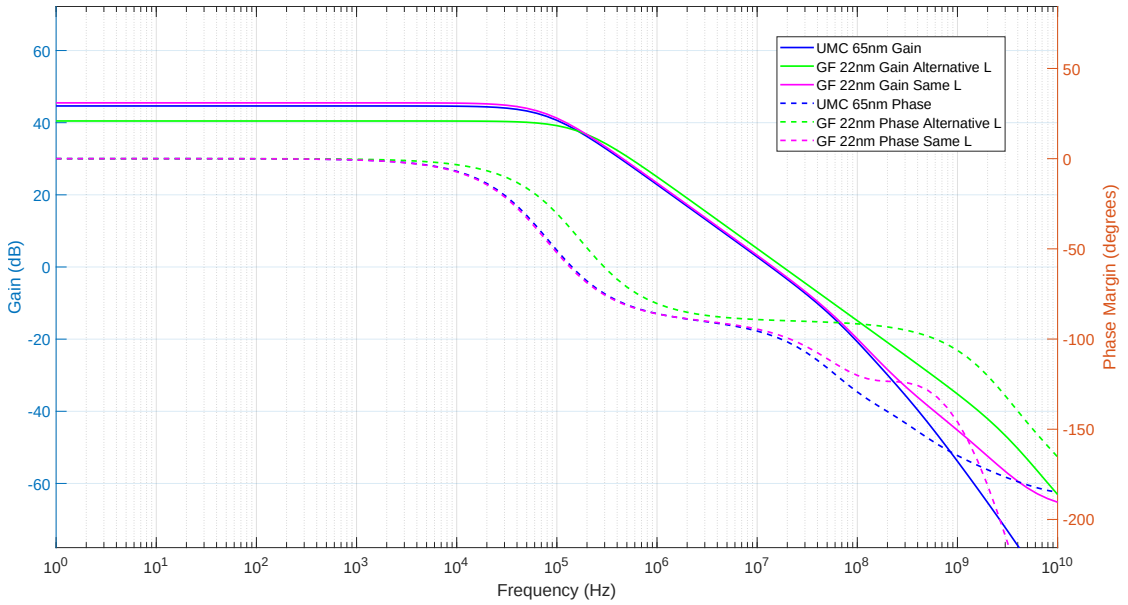


Figure 5.11: Gain and Phase plots of Telescopic Amplifier in UMC 65nm and GF 22nm

## 5.4 Optimization for Common-Mode Rejection Ratio

During the design process in GF 22nm technology, it is observed that the circuit met the required specifications at lower transistor lengths like in Table 5.9. Alternate Sizing, particularly at 60nm, is unable to achieve the desired CMRR. Achieving a high CMRR is crucial for minimizing the influence of common-mode signals and improving the overall

accuracy and performance of the amplifier. So, either higher lengths must be used, as shown in the first part of Table 5.9 by using a length of 500 nm for all transistors, or a varying length should be chosen for the differential pair, as it is the major reason for the degradation of CMRR.

Rather than incorporating additional circuitry, such as common-mode feedback or complex biasing circuits, which could complicate the design and increase power consumption, a decision is made to iterate the design with higher transistor lengths. By increasing the lengths of the transistors, the mismatch effects are reduced, which in turn improves the CMRR. This approach allowed for a simpler and more power-efficient design while still meeting the required CMRR specifications. The same approach has been followed for the design of a two-stage Miller OpAmp to have a smaller size for the biasing transistor. The iterative process of adjusting the transistor lengths proved effective, ensuring that the final design not only met the CMRR requirements but also maintained overall circuit simplicity and efficiency.

## 5.5 Design Methodology for Dynamic Output Resistance Driver Circuit

The design methodology is applied to the development of a dynamic output resistance driver circuit for a DDR4 receiver circuit using GF 22nm technology. The design approach is primarily based on the methodology described in [28], which involves designing both the pull-up and pull-down blocks for the output driver. This section aims to verify the methodology from a different perspective, facilitating the decision-making process for sizing the pull-up and pull-down blocks.

Building on previous work where the methodology is successfully applied to three different circuits, this design extends the methodology's application to a dynamic output resistance driver circuit specifically for output resistance driver circuits. The goal is to assess the methodology's adaptability and effectiveness in this new context.

In [28], the output driver design employs binary-weighted transistors, and calibration is performed with codes ranging from 0 to 128. The drain current through the pull-up and pull-down blocks with NMOS transistors in parallel is set to 1.25 mA to achieve a constant output of $(V_{dd}/2)$ with an effective resistance of 240 Ohms. With this approach, all transistors operate in strong inversion, characterized by a $(g_m/I_D)$ ratio of less than

10. Operating in this region ensures predictable and stable transistor behaviour with high speed, crucial for achieving the desired output resistance characteristics [10].

The GUI plots generated from the proposed design flow facilitate the examination of the relationship between $g_{ds}$, the inverse of output resistance, and transistor width. These plots are essential for determining the transistor dimensions required to achieve a specific drain current ($I_D$) for a given gate-source ($V_{GS}$) and drain-source ($V_{DS}$) voltages in the circuit. The relevant curves are:

- $(g_m/I_D)$ vs $(g_m/g_{ds})$
- $(g_m/I_D)$ vs $(I_D/W)$

To achieve high speed and low resistance of 240 Ohms, the design procedure begins by selecting all transistors in Strong Inversion with $(g_m/I_D) = 10$.

The output impedance ($Z_{out}$) can be calculated using:

$$Z_{out} = \frac{1}{g_{ds,total}} \tag{5.15}$$

where $g_{ds}$ is the total drain-source conductance. Therefore, the total $g_{ds}$ can be expressed as:

$$g_{ds,\text{total}} = \frac{1}{Z_{out,total}} \tag{5.16}$$

From the $(g_m/I_D)$ vs $(g_m/g_{ds})$ plot, the value of $(g_m/g_{ds})$ can be determined. Given the required $g_{ds}$, $g_m$ can be found. With $g_m$, $g_{ds}$, and $I_D$ known, the $I_D/W$ can be determined from the $(g_m/I_D)$ vs $(I_D/W)$ plot, which then allows calculation of the transistor width.

While choosing $g_{ds}$, one has the option of linear or binary-weighted configurations. For an output driver circuit, binary-weighted transistors are preferred due to their linear response and improved DAC conversion.

The proposed method ensures an efficient design process, enabling dynamic adjustment of the output resistance to meet the stringent requirements of DDR4 memory interfaces. This verification of the methodology confirms its applicability and effectiveness in DDR4 receiver circuit design, further demonstrating its robustness across various circuit designs.

# 6 Conclusion and Future Work

The $g_m/I_D$ methodology significantly reduces design time in analog circuits by maintaining a structured design approach, renowned for its simplicity and compatibility with submicron technologies. This methodology is demonstrated through a comprehensive approach to transistor sizing across three distinct analog design blocks. This process not only simplifies the design workflow but also validates physical principles through SPICE simulations and supports thorough exploration of the design space.

LUTs for PMOS and NMOS transistors are generated in Python using Spectre as a simulator and validated with results from the Cadence Spectre test setup. To streamline the calculation process, a GUI has been developed that allows users to plot various characteristics across multiple files, enabling easier comparison and deeper understanding of the devices. This GUI accepts LUT files in .pkl format and inputs such as Length, VGS, VDS, and VSB, and it calculates the width for up to 10 transistors simultaneously.

In the design of the two-stage Miller OpAmp, good performance is achieved in moderate inversion for both UMC 65nm and GF 22nm technologies. Both designs met the required specifications, with the UMC 65nm design achieving a GBW of 59.28 MHz compared to 94.21 MHz in the GF 22nm design. However, the use of shorter transistor lengths resulted in increased noise, which can be mitigated at the expense of increased area and reduced CMRR.

For the design of the latched comparator, consisting of a StrongARM latch and an RS latch, the entire design is implemented in strong inversion to enhance speed. The UMC 65nm design achieved an operating frequency of 0.909 GHz, while the GF 22nm design reached 2 GHz, where GF 22nm has a lesser delay of 154 ps than UMC 65nm.

In the design of the telescopic OTA, the GF 22nm technology is tested using both uniform and varying transistor lengths. Both approaches yielded similar output results, but the alternative sizing consumed significantly less area, although with a higher offset voltage of -0.89 mV.

Overall, the results indicate that the $g_m/I_D$ value remains relatively consistent across different technologies. While some studies, such as those by Fernando[24] and Vinoth [15], explore the use of varying transistor lengths, in this thesis, a uniform transistor length across all devices is opted for. This approach simplifies the design process while still meeting the desired performance outcomes.

The tool developed in this thesis is designed to be semi-automatic and generic, suitable for a wide range of designs. Future work could involve creating a fully automated tool tailored for specific designs, building upon the code developed here. Additionally, while this work focuses on nominal temperature conditions, there is potential to extend the tool's capabilities to include temperature sweeps for corner simulations, despite the increased computational resources required. As technology advances, it would also be advantageous to apply the $g_m/I_D$ methodology to smaller technology nodes, such as 5nm or 3nm, to assess its effectiveness and adaptability in the latest semiconductor processes.

# Bibliography


[1] Paul G. A. Jespers and Boris Murmann. *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. 2017. ISBN: 9781107192256.

[2] F. Silveira, D. Flandre, and P.G.A. Jespers. "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA". In: *IEEE Journal of Solid-State Circuits* 31.9 (1996), pp. 1314–1319. DOI: 10.1109/4.535416.

[3] Gaurav Sharma, Bharat Kumar, Arun Johar, Deep Gupta, Dharmendar Boolchandani, and Sougata Kar. "Design Automation of 5-T OTA using gm/ID methodology". In: *2019 IEEE 5th International Conference on Computational Intelligence and Communication Technology (CICT)*. 2019. DOI: 10.1109/CICT48419.2019.9066119.

[4] Nagwa Sabry, Hesham Omran, and Mohamed Dessouky. "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology". In: *Microelectronics Journal* 75 (2018), pp. 87–96. DOI: 10.1016/j.mejo.2018.02.002.

[5] Joao Raposo, Francisco Alves, and Pietro Ferreira. "A General gm/Id Temperature-Aware Design Methodology Using 180 nm CMOS up to 250 °C". In: *Journal of Integrated Circuits and Systems* 17.1 (2022), pp. 1–9. DOI: 10.29292/jics.v17i1.552.

[6] Aleksandar Radev. "Overview of Methodologies for Initial Design of CMOS Integrated Circuits in Deep Submicron Processes in Different Regions of Inversion". In: *2023 19th International Conference on Electrical, Computer, and Communication Technologies (ICECCT)*. 2023, pp. 1–6. DOI: 10.1109/ET59121.2023.10278653.

[7] A. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout. "Analog Circuits in Ultra-Deep-Submicron CMOS". In: *IEEE Journal of Solid-State Circuits* 40.1 (2005), pp. 132–143.

[8] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin. "Analog Circuit Design in Nanoscale CMOS Technologies". In: *Proceedings of the IEEE* 97.10 (2009), pp. 1687–1714.

[9] D. M. Binkley. *Tradeoffs and Optimization in Analog CMOS Design*. John Wiley & Sons, Ltd, 2008.

[10] P. Jespers. *The Gm/ID Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits: The Semi-Empirical and Compact Model Approaches*. Springer Publishing Company, Inc., 2009.

[11] C. Enz, F. Krummenacher, and E. A. Vittoz. "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications". In: *IEEE Journal of Solid-State Circuits* 30.1 (1995), pp. 33–43.

[12] A. J. Scholten, X. Jin, R. Van Langevelde, G. C. M. Meijer, D. B. M. Klaassen, and R. J. E. Hueting. "MOS Model 11: An Advanced Compact Model for Deep-Submicron MOS Transistor Design". In: *IEEE Transactions on Electron Devices* 46.9 (1999), pp. 1778–1787.

[13] A. J. Scholten, R. van Langevelde, D. B. M. Klaassen, and R. J. E. Hueting. "Accurate Compact Modeling of MOSFETs Down to Deep-Submicron Dimensions". In: *IEEE Transactions on Electron Devices* 50.1 (2003), pp. 177–182.

[14] Victor Arzate and Federico Sandoval-Ibarra. "Design of a Miller Amplifier using gm/ID based on A First-order Building Block Approximation". In: *2023 International Symposium on Advanced Topics in Electrical Engineering (ATEE)*. 2023, pp. 1–4. DOI: 10.1109/ATEE58038.2023.10108237.

[15] Ramesh Vinoth and Ramasamy Srinivasn. "Design and Implementation of High-Speed Latched Comparator Using gm/Id Sizing Method". In: *ICTACT Journal on Microelectronics* 2 (2017), pp. 300–304. DOI: 10.21917/ijme.2017.0052.

[16] Sandar M. *Gm_over_Id_methodology*. 2022. URL: https://github.com/sandarm-1/Gm_over_Id_methodology.

[17] Bmurmann. *GitHub - bmurmann/Book-on-gm-ID-design: Ancillary Material for the book "Systematic Design of Analog CMOS Circuits"*. URL: https://github.com/bmurmann/Book-on-gm-ID-design.

[18] Cian O'Donnell, Daniel O'Hare, and Tiarnach Reidy. *PyGMID*.

[19] Behzad Razavi. "The Strong ARM Latch: A Circuit for all Seasons". In: *IEEE Solid-State Circuits Magazine* 7.2 (2015), pp. 12–17.

[20] Jaime Ramiírez Angulo, Milind Sawant, Antonio Lopez Martin, and Ramon G. Carvajal. "A Power Efficient and Simple Scheme for Dynamically Biasing Cascode Amplifiers and Telescopic Op-Amps". In: *VLSI Journal* 41 (2009), pp. 239–243.

[21] Kush Gulati and Hae-Seung Lee. “A High-Swing CMOS Telescopic Operational Amplifier”. In: *IEEE Journal of Solid-State Circuits* 33.12 (1998), pp. 2010–2019.

[22] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2005.

[23] R. J. Baker. *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2019.

[24] Fernando Cortes, Eric Fabris, and Sergio Bampi. “Analysis and design of amplifiers and comparators in CMOS 0.35 m technology”. In: *Microelectronics Reliability* 44 (2004), pp. 657–664. DOI: 10.1016/j.microrel.2003.10.014.

[25] Prof. Dr.-Ing Klaus Hofmann and Markus Graber. “Opamp Design Simulation”. In: *Advanced Integrated Circuit Design Lab, Technical University of Darmstadt* (2021).

[26] Tsuguo Kobayashi, Kazutaka Nogami, T. Shirotori, and Y. Fujimoto. “A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture”. In: *IEEE Journal of Solid-State Circuits* 28 (1993), pp. 523–527. URL: https://api.semanticscholar.org/CorpusID:56929187.

[27] Sounak Dutta. “Design of a Strong-Arm Dynamic-Latch based comparator with high speed, low power and low offset for SAR-ADC”. In: (Sept. 2022). DOI: 10.36227/techrxiv.21114433.v1.

[28] Madhushree Bapuraya Patil. *Design and Verification of a LPDDR4X DQ Driver in 22nm FDSOI Technology*. 2024.