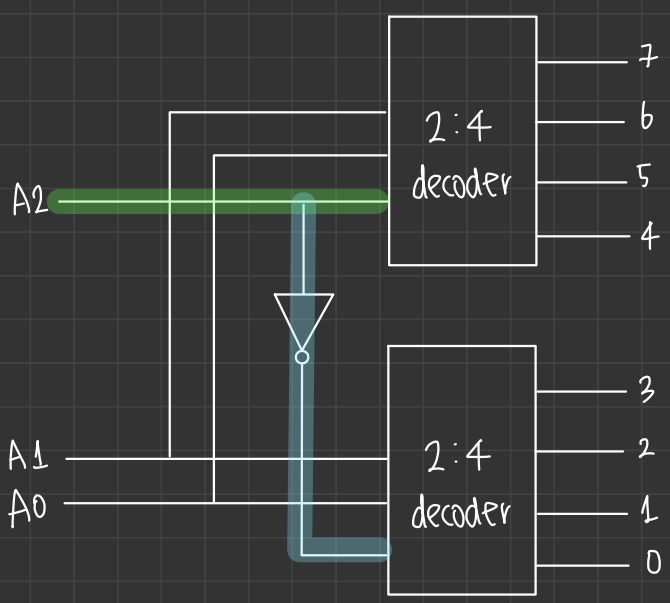
3 : 8 Decoder

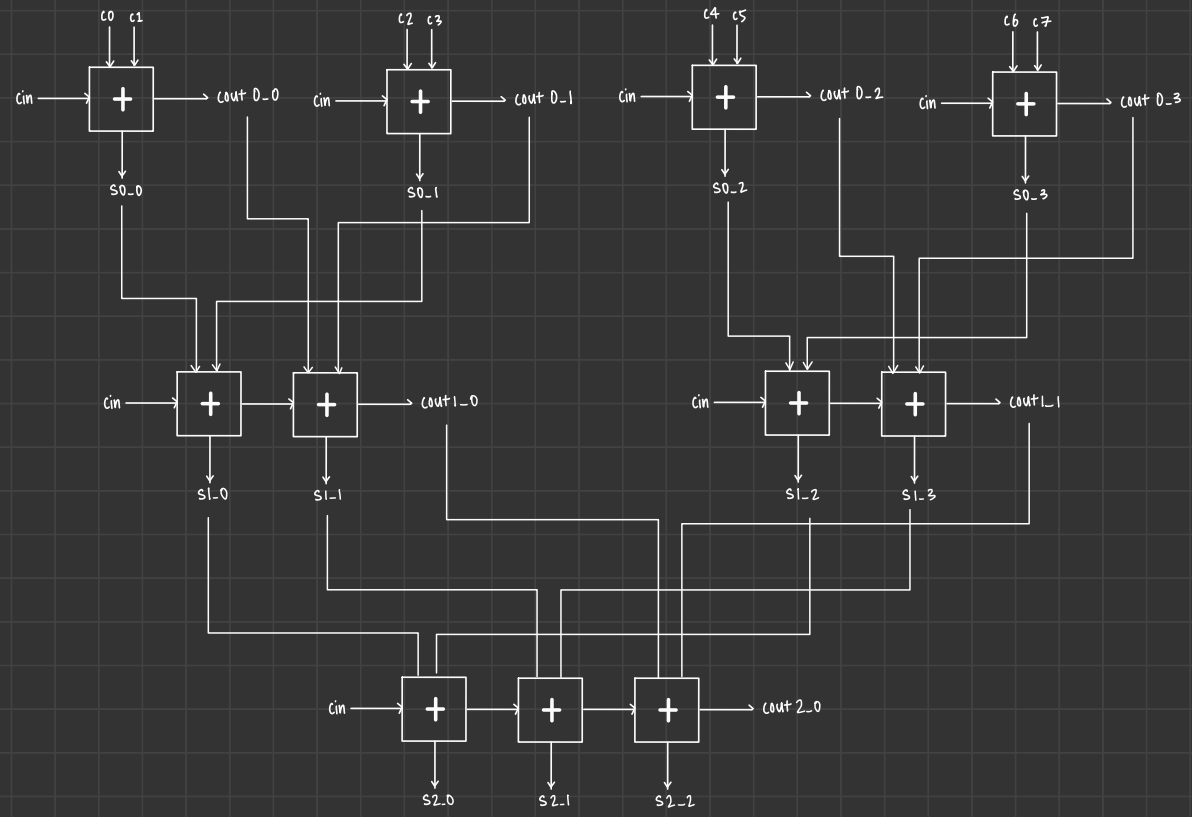
TRUTH TABLE

ena	in[2:0]			out[7:0]							
0	X	X	X								
1	0	0	0	0	0	0	0	0	0	0	1
	0	0	1	0	0	0	0	0	0	1	0
	0	1	0	0	0	0	0	0	1	0	0
	0	1	1	0	0	0	0	1	0	0	0
	1	0	0	0	0	0	1	0	0	0	0
	1	0	1	0	0	1	0	0	0	0	0
	1	1	0	0	1	0	0	0	0	0	0
	1	1	1	1	0	0	0	0	0	0	0

SCHEMATIC



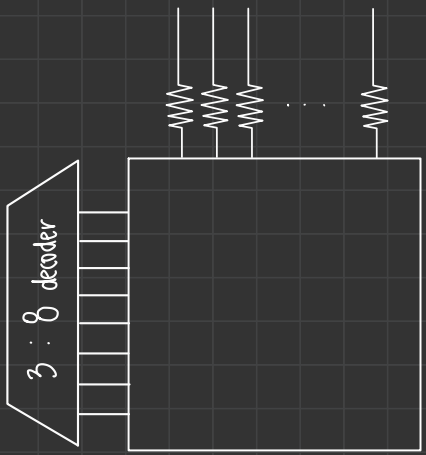
N-bit Adder

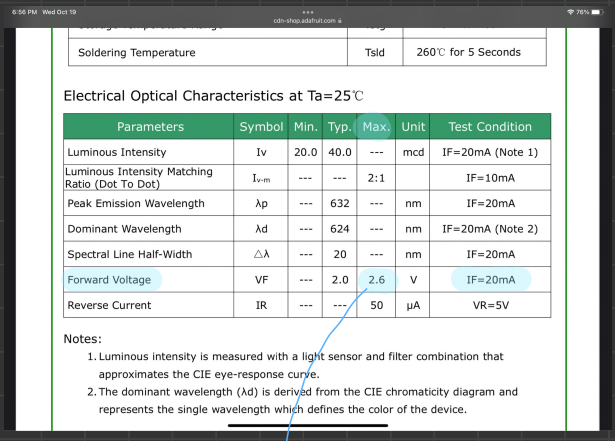

c0
c1
cin
cout 0_0
s0_0
c2
c3
cin
cout 0_1
s0_1
c4
c5
cin
cout 0_2
s0_2
c6
c7
cin
cout 0_3
s0_3
cin
cout1_0
s1_0
s1_1
cin
cout1_1
s1_2
s1_3
cin
cout 2_0
s2_0
s2_1
s2_2

FPGA Wiring

MODEL

ROW 1	PIN1	PIN16	COL 5
2	2	15	6
3	3	14	7
4	4	13	8
COL 1	5	12	ROW 5
2	6	11	6
3	7	10	7
4	PIN8	PIN9	8





Soldering Temperature	Tsld	260℃ for 5 Seconds

Electrical Optical Characteristics at Ta=25℃

Parameters	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Luminous Intensity	Iv	20.0	40.0	---	mcd	IF=20mA (Note 1)
Luminous Intensity Matching Ratio (Dot To Dot)	$I_{v\text{-}m}$	---	---	2:1		IF=10mA
Peak Emission Wavelength	λp	---	632	---	nm	IF=20mA
Dominant Wavelength	λd	---	624	---	nm	IF=20mA (Note 2)
Spectral Line Half-Width	△λ	---	20	---	nm	IF=20mA
Forward Voltage	VF	---	2.0	2.6	V	IF=20mA
Reverse Current	IR	---	---	50	μA	VR=5V

Notes:

1. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE eye-response curve.
2. The dominant wavelength (λd) is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

FPGA Voltage Supply

$$\frac{3.3V - 2.6V}{20\,mA} = \frac{0.7V}{0.02A} = 35\,\Omega$$ (Resistor values for LEDs)