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VESA Proposed DisplayPort (DP) Standard

Version 1.4 d1

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www.vesa.org

Purpose

The purpose of this document is to define a flexible system and apparatus capable of transporting video, audio and other data between a Source device and a Sink device over a digital communications interface.

Summary

The DisplayPort™ standard specifies an open digital communications interface for use in both internal connections, such as interfaces within a PC or monitor, and external display connections. Suitable external display connections include interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display.

DP v1.1a was revised to correct errata items and add clarifications to *DP v1.1*.

DP v1.2 was revised to add enhancements including higher speed operation, more flexible topology management, multiple streams on a single connection, higher speed Auxiliary Channel communications, improved support for audio, and a new smaller connector. It also corrected errors and added clarifications to *DP v1.1a*. This version corrects errors and adds clarification to *DP v1.2*. Furthermore, this version adds DP_PWR voltage level options to a downstream DisplayPort device.

DP v1.2a was revised to correct errata items and add clarifications to DP v1.2.

DP v1.3 was revised to add 8.1Gbps/lane link rate and living-room friendliness improvement, both for direct connection to a living room display and through DP-to-HDMI converter.

DP v1.4 was revised to add VESA Display Stream Compression (DSC) transport support for visually lossless 8Kp/10Kp60Hz video along with full extension of audio transport up to 32-channel LPCM audio at 192kHz and HBR 8-channel audio up to 1536kHz. For visual glitch-free DSC bitstream transport, Reed Solomon (254, 250) Forward Error Correction (FEC) was added. In addition to the sheer video and audio transport bandwidth increase, *DP v1.4* incorporates metadata transport for both static and dynamic High Dynamic Range (HDR). Furthermore, *DP v1.4* enhances the Multi-stream Transport (MST) feature to better enable multi-function.

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Preface

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The following holders of this IPR have assured VESA that they are willing to license the IPR on Reasonable And Non-Discriminatory (RAND) terms. The statement of the holder of this IPR is registered with VESA.

Table 1: Patents

Holder Name	Contact Information	Claims Known
Advanced Micro Devices, Inc. 1 Commerce Valley Drive East Markham, ON L3T 7X6 Canada	Raymond Li (raymond.li@amd.com)	**US Patent Applications** 11/678,825 11/678,819 11/010,159
Apple, Inc. 1 Infinite Loop MS 169-3IPL Cupertino, CA 95014 408-783-5093	Jonathan Brown Senior Standards Counsel (jbrown1@apple.com)	**US Patents** US 20130050216 US 20130094557 US 61/914,312 US 61/914,322 US 61/954,498 **Foreign Counterparts Related to the Patents Identified Above** WO2013055510
Dell, Inc. One Dell Way Round Rock, TX 78682	Tom Lanzoni (tom_lanzoni@dell.com)	11/458130 11/769803 11/458138 12/029013 11/543574 12/12334 11/678838 12/148668

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Table 1: Patents (Continued)

Holder Name	Contact Information	Claims Known
Genesis Microchip, Inc. 750 Canyon Drive Coppell, TX 75019	Robert Krysiak (bob.krysiak@st.com)	**US Patents** 6,992,987 7,424,558 7,733,915 7,068,686 7,567,592 8,059,673 7,088,741 7,620,062 8,068,485 7,177,329 **US Patent Applications** 10/726,350 10/726,441 11/742,222 10/726,362 10/726,794 12/248,822 **China Patents** ZL200410038432.8 ZL200410071497.2 ZL200410047784.X ZL200410038545.8 ZL200410044503.5 ZL200810128376.5 **China Patent Applications** 20041038545 20041044503 20081095571 20041038546 20041045686 20081099136 20041043412 20041071497 20081128376 20041043419 20041071498 **EPO Patent Applications** 04251581.7 04252057.7 04252205.2 04251582.5 04252202.9 08153724.3 04252054.4 04252203.7 08153726.8 04252055.1 04252204.5 08155262.2 04252056.9 **Japan Patent Applications** 2004127749 2004130804 20040132494 2004127757 2004130812 20040135520 2004129464 2004133593 20040135542 2004129479 2008116510 20080125185 **Korea Patent Applications** 20040026008 20040026013 20040026486 20040026009 20040026483 20080039968 20040026010 20040026484 20080063251 20040026011 20040026485 20080043714 20040026012 **Singapore Patent Applications** 2008027534 20040001975 20040002060 20040001154 20040001979 20040002061 20040001166 20040002054 20080002448 20040001969 20040002057 20080002449 20040001973 **Taiwan Patent Applications** 93106707 93109757 93110863 93106751 93110851 97115572 93109369 93110857 97111673 93109370 93110861 97111674 93109747

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Table 1: Patents (Continued)

Holder Name	Contact Information	Claims Known
Intel Corporation 2111 NE 25th Avenue Hillsboro, OR 97124	Srikanth Kambhatla (srikanth.kambhatla@intel.com)	11/648367 Sink device addressing mechanism 61/1298,936, Title: Audio/video streaming audio in a topology of devices. 12/774,023 (claims priority to P33959Z), Title: Audio/video streaming audio in a topology of devices. 12/782,040 (claims priority to P33959Z), Title: Binding for audio/video streaming in a topology of devices. 12/821,306 (claims priority to P33959Z), Title: Message passing framework for audio/video in a topology of devices. 12/789,893 (claims priority to P33959Z), Title: Identifying devices in a topology of devices for audio/video streaming.
Molex, Inc. 2222 Wellington Court Lisle, IL 60532	Stephen L. Sheldon IP Counsel (slsheldon@molex.com)	**US Patents** US 6,280,209, claim 1 US 6,457,983, claims 1 and 23 US 6,575,789, claim 1 US 6,945,796, claims 5 and 13 US 7,165,981
Parade Technologies, Ltd. 2890 Zanker Road, Suite 102 San Jose, CA 95134	Craig Wiley (craig.wiley@paradetech.com)	**US Patents** 7,397,383, Title: Digital AV Transmission PHY Signaling Format Conversion, Multiplexing & De-multiplexing. 8,094,684, Title: Link Training Scheme for DisplayPort Repeaters **US Patent Applications** 11/467,528 11/537,377 12/118,508
Silicon Image, Inc. 1140 East Arques Avenue Sunnyvale, CA 94085	Roger Isaac (roger.isaac@siliconimage.com)	**US Patents** US 6151334 US 6857525 US 6914637 US 7088398 US 7599439
STMicroelectronics, Inc. 750 Canyon Drive Coppell, TX 75019	Robert Krysiak (bob.krysiak@st.com)	**US Patent Applications** 12/365,678 12/423,724 12/484,796
Synaptics, Inc. 1251 McKay Drive San Jose, CA 95131	Wendy Cheng (wcheng@synaptics.com)	US 8,686,759, Title: Link-Train tunable PHY electrical repeater

Attention is drawn to the possibility that some of the elements of this VESA Standard might be the subject of IPR other than those identified above. VESA shall not be held responsible for identifying any or all such IPR, and has made no inquiry into the possible existence of any such IPR.

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Clarifications and application notes to support this standard might be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates DisplayPort, ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you might require. Submit all comments to support@vesa.org.

Acknowledgements

This document would not have been possible without the efforts of VESA's DisplayPort Task Group. In particular, Table 2 lists the individuals and their companies that contributed significant time and knowledge to this version of the Standard.

Table 2: Main Contributors to *DP v1.4 (To be updated)*

Company	Name	Contribution
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	Sree Raman	Technical Content
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Revision History

Table 3: Revision History

Date	Version	Description

November 3, 2015	v1.4 d1	• DP1.4 draft documents that have gone through TGR
		  • DP1.4 Update on MSA Video Horizontal Expansion Option d3 TGR-PostTGR Coms Addressed
		  • DP1.4 Secs 2.2.5 on InfoFrame SDP, VSC_EXT, and Split SDP in SST d5 TGR-PostTGR Coms Addressed
		  • DP1.4 Audio Secs Update d11 TGR-PostTGR Coms Addressed
		  • DP1.4 Add of Sec 2.6.1.1 on Multi-Function MST Branch Enumeration d6 TGR-PostTGR Coms Addressed
		  • DP1.4 Add DSC Transport Sec 2.6a d5 TGR_Post TGR Coms Addressed
		  • DP1.4 Updates on FEC d 7 TGR-PostTGR Coms Addressed 151029
		• DP Link Training policy update draft document
		  • DP1.4 Updated to Link Training in Sec 3.5.1.2 D2
		• Adopted DP1. 3 SCR documents
		  • DP to VGA sink_source behavior v3
		  • DP1.3 Adaptive-Sync v3
		  • DP1.3 HBR EYE Mask Typo Errors v1
		  • DP1 3 TPS4 Symbol Sequence Info Correction SCR v 1
		• TGR-completed DP1.3 SCR draft documents
		  • DP1.3 BT2020 color gamut for RGB
		  • DP1.3 HDMI Protocol Conv Source Control v4
		  • DP1.3 LT Tunable PHY Repeater Use Case
		  • DP1.3 TRAINING LANEx Set v2 clean
		• Corrected Wireless DFP Byte 1 name at DPCD Address 000081h
		• Corrected SINK_COUNT field in DPCD Address 02002h references to include bit 7.
		• Corrected range RESERVED for Protocol Converter Extension to start at 3035h (instead of 3034h)
		• Table 1-3 – Updated to include additional documents mentioned throughout the Standard
		• Table 3-8 – Corrected TPS4 “Name” column text
		• Applied minor edits and started applying VESA template style changes

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Table 3: Revision History (Continued)

Date	Version	Description

September 2014	1.3	• Updated DPCD address mapping to include GTC-related registers that were added in DPv1.2a at DPCD Addresses 0005Ah and 0005Bh (Table 2-155), 00115h, 0015Ah, and 0015Bh (Table 2-156), and 02004h bit 1 (Table 2-164).
		• Added register at DPCD Address 0025Bh.
		• Added missing names for Byte 1 (bits 7:0), and Byte 2 (bits 7:2 RESERVED) of DPCD Addresses 00080h through 0008Fh, when DETAILED_CAP_INFO_AVAILABLE = 1.
		• 2.8.4.5.1 (was 2.9.3.6.1) – Corrected field reference from 00102h bits 3:2 to 0010Bh through 0010Eh bits 2:0.
		• 2.12.1.3.2.2 (previously not numbered), 2nd pg – Corrected bit reference from 00058h bit 0 to bit 1.
		• Corrected SINK_COUNT field in DPCD Address 00200h references to include bit 7.
		• Corrected DFP_COUNT field in DPCD Address 00007h references to include bit 3.
		• Appended "_ESI" to DPCD Address 0200Ch register name.
		• Standardized spelling of register names – DPCD Addresses 00005h, 0000Fh, and 001A0h.
		• Combined DPCD Addresses 00054h through 00058h into a single register with multiple bytes.
		• Deprecated FAUX, Post Cursor2, and Default Framing mode.
		• Applied global updates to bring standard parallel with DPCD-related content in VESA eDP, DockPort, and MyDP standards.
		• Renamed terms:
		  • downstream port –> downstream-facing port (DFP)
		  • upstream port – upstream-facing port (UFP)
		  • M and N timestamps -> Mvid and Nvid time stamps
		  • AUX CH -> AUX CH or AUX transactions, depending on use
		  • uPacket receiver, DP receiver -> DPRX
		  • uPacket transmitter, DP transmitter -> DPTX
		• Revised miscellaneous bit names to better identify their function.
		• Updated Acronym and Glossary lists to include new terms and expanded and/or corrected definitions.
		• Updated (preliminary updated) reference document table to include additional reference documents supported by this Standard.
		• Added "living-room friendliness" objective; both (1) DP directly to a living-room large screen display and (2) through active transport protocol conversion from DP to HDMI.
		• Global – Added 8.1Gbps/lane speed, and support for MyDP 6.75Gbps/lane speed.
		• Global – Added support for YCbCr420 and RAW.
		• 2.1 – Clarified terminology/device types (DP Source/Sink/Branch/PHY Repeater).
		• 2.1.4 – Updated SST Branch device EDID and DPCD access handling requirement.

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Table 3: Revision History (Continued)

Date	Version	Description

September 2014	1.3	**Continued:**
		• 2.2.1 – Added Camera RAW mapping to Main-Link symbols. Incorporate "End of active line TU clarification" SCR.
		• 2.2.4 – Incorporated "Extend MS Timing Parameters Ignore Option" SCR (Active-Sync enabler); added MISC 1 bit 6 support (support added globally)
		• 2.2.5 – VSC SDP extension for Pixel Encoding/Colorimetry Format (globally added support).
		• 2.2.5 – Added Camera SDP.
		• 2.8 – Added comprehensive DPCD Address Mapping table covering all published DP-related standards:
		  • New Extended Receiver Capability field for DPCD r1.4 (and higher)
		  • HDMI2.0 SCDC abstraction
		  • Metadata extension:
		  DVI/HDMI1.4b/HDMI2.0 mode selection
		  Pixel encoding conversion within active transport protocol converter (e.g., YCbCr444 to YCbCr420)
		  Colorimetry format
		  • BT2020
		  • Full-range YCbCr601/701:
		  Content type
		  • Game/video/still image:
		  CEC-Tunneling-over-AUX
		  HDCP2.2-for-DP (DPCD 69xxxh)
		  • Incorporated eDP, MyDP, and DockPort DPCD register address mapping.
		• 2.11 – Added Intel SCR concerning ENUM_PATH_RESOURCES message transaction extension.
		• 3.4.2 – Added edge rate restriction of AUX CH electrical sub-block for supporting HBR3.
		• 3.5.1 – Added HBR3, TPS4, Post LT ADJ REQ.
		• 3.5.2 – Added HBR3, updated jitter budget, Reference DFE, Enhanced HBR Reference CTLE.
		• 3.6 – Added new Link Training-tunable PHY Repeater section.
		• 5.3.2 – Added link rate/lane count configuration flexibility between UFP and DFP.
		• 5.3.3 – Expanded DP-to-HDMI transport protocol converter section to comprehend protocol conversion to HDMI2.0.
		• 5.3.3 – Added CEC-Tunneling-over-AUX.
		• Figure G-3 – Replaced.

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Table 3: Revision History (Continued)

Date	Version	Description
May 2013	1.2a	• Reformatted document into new style template. • Tabled or bulleted/numbered paragraphical data, as needed, and fixed typos. Other minor edits have also been applied as part of the changes listed below. • Corrected table or figure cross-references in 2.2.1.2, 2.2.1.3, 2.2.5.3.3, 2.6.5, 3.4.1.3.1, 3.4.2.7, and D.1.1.4. • Standardized mention of register-related information (bits, fields, registers, addresses, etc.) Hyperlinked register and state-related information, as well as some packet-related information. Edited text surrounding the newly hyperlinked text, as needed. • Corrected figure cross-references in 2.2.5.3.3 and 2.6.6 (was 2.6.5). • Organized registers into individual address mapping tables by DPCD field, with all master copies residing in Section 2. • Relabeled appendices alphabetically, with no numbers in their titles. • Corrected register name for DPCD Address 00114h.

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Table 3: Revision History (Continued)

Date	Version	Description
May 2012	1.2a	• Patent information for Genesis Microchip, Intel, STMicrosystems and Parade added. • FAUX bit rate changed from 720Mbps to 675Mbps throughout the document. • 2.3.1.1 Rules of DP_PWR State for a Source Device: Added text. • 2.2.5.6 VSC Packet: Added text regarding PSR function defined in eDP v1.3. • 2.2.5.6.1 VSC Packet Header, Table 2-55: Added text for VSC packets. • 2.2.5.6.2 VSC Packet Payload: Added text describing Table 2-56. • 2.3.3.2 Relative Address (RAD): Corrected port numbers. • 2.7.7.1.5.3 Upon I2C_DEFER|AUX Reply with MOT Bit in Request Transaction Set to 0 or 1: Added text. • 2.7.7.1.5.6 Upon Receiving AUX_DEFER Reply to Request Transaction with MOT Bit Set to 0 or 1: Added text, table, and sub-section. • 2.7.7.1.6.3 Upon I2C_DEFER|AUX_ACK Reply to a Request Transaction with MOT Bit Set to 0 or 1: Added text. • 2.7.7.1.6.6 Upon Receiving AUX_DEFER Reply to Request Transaction with MOT Bit Set to 0 or 1: Changed and added text, table, and sub-section. • 2.9.3 AUX Link Services: Added text regarding EDID Read requirements. • 2.9.3.1 Address Mapping for Link Configuration Management, Table 2-75: Added missing information to Read/Write over AUX column and requirement for Downstream device in area 0010Fh of table, changed rows. Also added new bit in DPCD and updated address entries for 00005h and 00080h-0008fh. Added entries from 00271h to 0027Ah. • 2.11 Messaging AUX Client: Replaced & renumbered sections 2.11.9.5.9 and 2.11.9.5.10. Corrected field names in Table 2-85. Resolved errors in Tables 2-81, 2-85. Corrected syntax in Tables 2-89, 2-90, 2-91, 2-94, 2-95, 2-96, 2-97, 2-98, 2-99, 2-100, 2-101, 2-103. Added new fields to Tables 2-81, 2-85. • 2.11.2.4 Handling of Multiple Message Transaction Requests: Removed Message Transaction requirement. • 2.11.3.1.4 Sideband_MSG_Body_Length: Corrected field description text. • 2.11.3.1.5 Start_Of_Message Transaction: Changed text, clarified bit definition. • 2.11.3.2 Sideband_MSG_Body: Corrected table number referenced. • 2.11.4.1.1 MST_CAP Bit of MSTM_CAP DPCD Location: Removed device requirement. • 2.11.4.1.5 DOWN_REQ Sideband MSG Buffer: Corrected writing into message buffer, 2.11.4.1.6 UP_REP Sideband MSG Buffer: Corrected writing into message buffer, 2.11.4.1.7 DOWN_REP Sideband MSG Buffer: Corrected writing into message buffer. • 2.11.9.1.3 Payload_Bandwidth_Number: Removed last sentence. • 2.11.9.1.4 Allocated_Payload_Bandwidth_Number: Added this new section. • 2.11.9.4.1 This sub-section added covering Full Payload Bandwidth Number.

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Table 3: Revision History (Continued)

Date	Version	Description
May 2012	1.2a	**Continued:** • 2.11.9.4.2 This sub-section number changed from 2.11.9,4.1 to 2.11.9.4.1 due to the addition of new Section 2.11.9.4.1 and change the section title to "Available Payload Bandwidth Number." • 2.11.9.4.3 Port Number: Section number has changed. • 2.11.9.10.7 Global_Unique_Identifier sub-section • 2.11.9.15 QUERY_STREAM_ENCRYPTION_STATUS: Updated text. • 2.13 Global Time Code and Audio Inter-channel Sync: Amended and added significant text. Added new table (Table 2-104). • 3.2 DP_PWR for Box-to-Box DisplayPort Connection: Added active cable assembly to list of device types, changed power pin voltage, removed some text in Table 3-3, column two. Text additions and footnote. • 3.1.3.1 DP_PWR/DP_PWR_RETURN: Added text and footnote. • 3.2 DP_PWR specification for a downstream device updated. • 3.2.1 DP_PWR User Detection Method: Added text regarding resistor requirements for CONFIG1 and 2. • 3.2.3 Inrush Energy: Changed peak current. • 3.4.2 AUX Channel Electrical Sub-block: Tables (3-6, 3-8, 3-9) and Figures (3-29, 3-30) were replaced to redefine eye vertices and bring Standard in line with CTS document(s). • 3.5.1 Transmitter and Receiver Electrical Parameters: Added to and amended Table 3-17, 3-20. • 3.5.1.2 Link Training: Added text defining transmitter response related to Post Cursor2 level. • 3.5.1.2.1 Clock Recovery (CR) Sequence: Added text regarding Downstream device. • 3.5.3.7.2 Differential Noise Budget: Added to and/or amended Tables 3-6, 3-7, and 3-23. • 3.5.3.8 Differential Voltage/Timing EYE Diagram: Changed and added to CTLES, replaced Tables 3-40 and 3-41. • 4.1.1 Cable-Connector Assembly Definition: Added text to very end of section (before sub-section 4.1.1.1). • 4.1.3.1 Impedance Profile through DP Connector: Changed information in Tables 4-1, 4-2, replaced Fig 4-9. • 4.1.5.4.2 Inter-Pair Skew: Amended text. • 4.4.6.4 Intra- and Inter-Pair Skew: Restructured and added sub-section for Inter-Pair Skew. • 5.1.2.1 Source Device Link Requirement when Other Interfaces are Supported: New sub-section. • 5.1.6 Transferred requirements for Source treatment of Branch devices from Interop Guide.

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Table 3: Revision History (Continued)

Date	Version	Description

May 2012	1.2a	**Continued:**
		• 5.2.2.1 Sink Device Link Requirement when Other Interfaces are Supported: New sub-section.
		• 5.3 Transferred requirements for protocol converting Branch devices and treatment by Sources from Interop Guide.
		• 5.3.2 Branch Device Link Configuration Requirements: Added info to address 0003h field.
		• 5.5.5 Sink Device uPacket RX Power-Save Mode, Figure 5-2: Added text to table and to STATE 1: ACTIVE section following figure.
		• 5.7.3 Active Cable Assembly, 5.7.3.1 Active Cable Assembly Electrical Parameters, 5.7.3.2 Active Cable Assembly DP_PWR Requirements: New sections added.
		• Appendix D: Amended Table 9-8.
		• Appendix H
		  • 13.1.2.1 VSC Packet Header, Table 13-1: Added text to table.
		  • 13.1.2.2 VSC Packet Payload: Added descriptive text.
		  • 13.3 Added section/sub-sections and table related to stereo 3D.
		• Appendix I, 14.3 QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling: Updated text, modified Tables 14-1, 14-2 and added text regarding L parameters in sub-sections. Removed path-message description.
		• Appendix J: Original was deleted and replaced with another appendix.
		• Other general edits and clarifications have also been made.

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Table 3: Revision History (Continued)

Date	Version	Description
January 2010	1.2	While maintaining full backward-compatibility with Version 1.1a, Version 1.2 added the following major features: • A new link rate, 5.4Gbps/lane, called HBR2 (or High Bit Rate 2). • Enhanced 3D stereo transport capability. • Color consistency/accuracy improvement support for wide color gamut contents and displays. • Multi-stream transport (MST) format supporting the transmission of up to 63 independent AV streams from a single DP connector, taking full advantage of the micro-packet transport architecture. • Enhanced topology management via message transactions over sideband channel (i.e., AUX CH and Hot Plug Detect) so that a stream Source device has full knowledge of the devices and their capabilities in the topology. • High data rate audio, audio-to-video lip synchronization and audio inter-channel synchronization enablement. • Fast AUX transaction at the raw bit rate of 720Mbps, or application bit rate of 576Mbps, for enabling applications such as USB2.0 transport over AUX CH. • Incorporated Mini DisplayPort Connector Standard. • Highlighted the difference between DisplayPort Standard and Embedded DisplayPort (eDP) Standard. • Various clarifications and errata corrections to Version 1.1a were also made in this revision.
December 2007	1.1a	Revised to correct errata items and improve clarification.
March 2007	1.1	Revised to clarify details; introduce the class of “hybrid device”; extend support for content protection schemes to include HDCP; and change requirements for power at DisplayPort connectors.
May 2006	1.0	Initial release of the Standard.

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1 Introduction

DisplayPort (DP) is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and CE industries. It consolidates internal and external connection methods to reduce device complexity, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

1.1 DisplayPort Standard Organization

The DP Standard is organized into the following sections that define the overall architecture and structure of the display interface:

- Section 1 – Introduction

  The introduction section defines the high-level industry needs for DisplayPort, and the resulting technical objectives that the protocol, electrical, and mechanical sections are intended to satisfy. This section also includes a glossary of terms for the overall Standard, references, and overview of DP architecture.

- Section 2 – Link Layer

  The Link Layer section describes the protocol for configuring and managing the topology and the flow of data over both the forward (host to display) transport channel and the auxiliary bidirectional channel. Both SST (Single Stream Transport) mode and MST (Multi-Stream Transport) mode are covered.

- Section 3 – PHY Layer

  The Physical (PHY) Layer section describes the electrical requirements of the DPTX and DPRX implementations. It also defines the required circuitry and encoding methodology for transmitting data to and from the DP Link Layer over a cable or circuit board traces.

- Section 4 – Mechanical

  The mechanical section defines the connector and cable requirements for both internal and external DisplayPort connectors used to convey the electrical signals defined by the DP PHY Layer.

- Section 5 – Source/Sink/Branch Device Policy Requirements for Interoperability

  The device and link media requirements section describes the policy requirements for Source, Sink, and Branch devices to support interoperability among devices that implement DisplayPort connections.

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1.2 DisplayPort Objectives

This Standard defines a scalable digital display interface with optional audio and content protection capability for broad application within PC and consumer electronic (CE) devices. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. Potential internal chip-to-chip applications include usage within a notebook PC for driving a panel from a graphics controller, and usage within a monitor or TV for driving the display component from a display controller. Examples of box-to-box applications for DisplayPort include display connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high-definition optical disc players, set top boxes, and television displays.

DisplayPort is designed to meet several key needs within the PC and CE industries as defined in Section 1.2.1. These industry needs are expanded into a set of technical objectives in Section 1.2.2 of the DisplayPort Standard to ensure that the display interface can support current and future industry requirements.

Specific objectives for external and internal display connections are defined in Section 1.2.3 and Section 1.2.4 respectively of the DisplayPort Standard. Section 1.2.5 defines the additional objectives for CE devices applications.

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1.2.1 Key Industry Needs for DisplayPort

The following PC and CE industry needs were considered in the development of the DisplayPort architecture and resulting interface Standard:

- Drive maximum application and re-use of digital technology to enable reduced device costs associated with implementing a digital display connection.
- Enable a common signaling methodology for both internal and external display connections to reduce device complexity and promote commoditization.
- Enable an extensible architecture that supports an optional robust content protection capability that may be economically implemented.
- Enable high-quality optional digital audio transmission capability.
- Enable higher levels of silicon integration and innovation within rendering and display devices to reduce device complexity and enable digital interface commoditization.
  Examples of potential DisplayPort integration capability include transmitter integration within a graphics or display controller, and receiver integration within a timing controller on a module.
- Simplify cabling for internal and external digital display connections.
- Address performance concerns with existing technologies by providing higher bandwidth over fewer wires.
- Apply embedded clock architecture to reduce electromagnetic interference (EMI) susceptibility and physical wire count.
- Provide a small form factor connector that can be plugged in by feel, and a design that will enable four connectors to be placed on a full height Peripheral Component Interconnect (PCI) card bracket.
- Enable broad PC and CE industry via an open and extensible industry standard.

DisplayPort addresses these industry needs by defining an electrical and protocol specification that may be readily implemented in module timing controllers, graphics processors, media processors, and display controllers.

A forward drive channel is defined that is scalable from one to four lanes, and implements a Micro-Packet architecture that supports variable color depths, refresh rates, and display pixel formats. A bidirectional auxiliary channel is defined that also implements micro-packet architecture for flexible delivery of control and status information.

DisplayPort includes a mechanical specification that defines a small, user-friendly external connector that is optimized for use on thin profile notebooks in addition to allowing up to four connectors on a graphics card. A standard module connector for internal applications is also defined in the mechanical section of this Standard.

1.2.2 DisplayPort Technical Objectives

The cross-industry needs defined above for DisplayPort may be translated into specific technical objectives. These technical objectives for DisplayPort are to:

- Provide a high bandwidth forward transmission link channel, with a bidirectional auxiliary channel capability.

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- Provide application support for up to 32.4Gbps (gigabits per second) forward link channel throughput to address long-term PC industry needs to support greater than QXGA (2048x1536) pixel format and greater than 24-bit color depths.
- Provide application support for 1Mbps (megabits per second) auxiliary channel (AUX CH) throughput with a maximum latency of 500us (except for a topology with cascaded PHY Repeaters between DPTX and DPRX, as described in Section 3.6).
- Support variable color depth transmission of 6, 8, 10, 12, or 16 bits per component.
- Support EMI compliance to FCC/CISPR B standard with a margin of at least 6dB.
- Support existing VESA and CEA standards where applicable.
- Architecture that does not preclude legacy transmission support (e.g., DVI and LVDS) to and from DisplayPort components.
- Support hot plug and unplug detection and link status failure detection.
- Support full bandwidth transmission via direct drive over a 2m cable.
- Support reduced bandwidth transmission via direct drive over a 15m cable. DisplayPort supports a minimum of 1080p lines at 24bpp, 50/60Hz over four lanes at 15m.
- Support audio skew of less than 1ms.
- Support a bit error rate of 10^{-9} for raw transport per lane, and 10^{-12} symbol error rate for audio and control data after ECC encoding/decoding.
- Support sub 65nm (0.065 micron) process technologies for integration in Source devices, and supports 0.35 micron process technologies for integration in Sink devices.

1.2.3 DisplayPort External Connection Objectives

For external connections between a Source device and a Sink device, this Standard is designed to achieve the following technical objectives:

- Support reading of the display EDID (Extended Display Identification Data) whenever the display is connected to power, even trickle AC power.
- Support DDC/CI (Display Data Channel/Command Interface) and MCCS (Monitor Command and Controls Set) command transmission.
- Support external display configurations that do not include scaling, a discrete display controller, or on screen display (OSD) functions, enabling low cost, digital monitors.
- For external notebook PC applications, DisplayPort allows support for direct drive through a docking connector configuration. A repeater function in the dock is strongly recommended.
- The external DP connector is identical for all display applications and provides support for four lanes. Captive cables may support one, two or four lanes to reduce cost.
- The external DP connector includes a multi-purpose power pin.
- The external DP connector is symmetrical such that the same connector may be used on both source and Sink devices.
- The external DisplayPort connector supports connection without the need for visual alignment.
- The external DisplayPort connector is sized to allow four connectors to fit on a standard full height ATX/BTX bracket opening for PCI, AGP (Accelerated Graphics Port), and PCI-Express add-in cards.

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1.2.4 DisplayPort Internal Connection Objectives

For internal connections such as within a notebook PC or display, this Standard is designed to achieve the following technical objectives:

- DisplayPort defines a common module connector to simplify internal device connections.
- The number of lanes in the internal cable is implementation-dependent, and may be one, two, or four.
- Internal DisplayPort connections may support both maximum and reduced link bandwidths.
- Internal DisplayPort connections support low link power modes.
- Hot Plug support for internal DisplayPort connections is implementation-dependent.

1.2.5 DisplayPort CE Connection Objectives

For application to CE devices, this Standard is designed to address the following technical objectives:

- DisplayPort optionally delivers digital audio data concurrent with display data.
- Support for maintaining synchronization for delivery of audio and video data to within ±1ms.
- DisplayPort architecture supports an optional robust content protection capability that may be economically implemented.
- DisplayPort supports equivalent functionality to the feature sets defined in *CEA-861-F* for transmission of high quality uncompressed audio-video content, and *CEA-931-B* for the transport of remote control commands between Sink and Source devices.
- DisplayPort supports variable audio formats, audio coding types, sample frequencies, sample sizes, and audio channel configurations. DisplayPort supports up to 32 channels of Linear Pulse Code Modulation (LPCM) audio at 192kHz with a 24-bit sample size, High Bit Rate (HBR) audio from 256 kHz to 1536 kHz, and up to eight channels of One Bit audio and DST audio.
- DisplayPort supports variable video formats based on flexible aspect, pixel format, and refresh rate combinations based on *DMT v1 r13* and *CVT v1.2* timing standards and those timing modes listed in *CEA-861-F*. DisplayPort also allows a Source device to indicate content types (i.e., games, video, and still image).
- DisplayPort supports industry-standard pixel encoding formats including RGB, YCbCr4:4:4, YCbCr4:2:2, and YCbCr4:2:0 with component bit depth up to 16 bits per component.
- DisplayPort supports colorimetry specifications such as BT601, BT709, BT2020, and Adobe RGB.
- DisplayPort supports transport protocol conversion, including DVI/HDMI1.4b/HDMI2.0, as well as analog VGA. For conversion to HDMI, DisplayPort also supports CEC message tunneling over AUX CH.
- DisplayPort supports VESA Display Stream Compression (DSC) transport for visually lossless 8Kp/10Kp60Hz video. For visual glitch-free DSC bitstream transport, DisplayPort also supports Reed Solomon (254, 250) Forward Error Correction (FEC).
- DisplayPort supports multi-function Multi-stream Transport (MST) dock with DP Alt Mode on USB Type-C capability.

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1.2.6 Content Protection for DisplayPort

For implementations of the DP interface where content protection is desired, it is recommended that HDCP Versions 1.3 and 2.2 be used. This is recommended to minimize incompatibilities between DisplayPort devices in the market.

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1.3 Acronyms, Initializations, and Abbreviations

Table 1-1: Acronyms, Initializations, and Abbreviations

Acronym	Stands for
ACT	Allocation Change Trigger
API	Application Programming Interface
AUX	Auxiliary transaction
AUX CH	Auxiliary CHannel
BER	Bit Error Rate
bpc	bits per component
bpp	bits per pixel
BE	Blanking End
BS	Blanking Start
BU	Branching Unit
CDF	Cumulative Distribution Function
CDR	Clock and Data Recovery
CEA	Consumer Electronics Association
CCS	Current Capabilities Structure
CD_ADJ	Current Disparity ADJust
CEC	Consumer Electronics Channel
CH	Channel
CP	Content Protection
CR	Clock Recovery
CSN	Connection Status Notify
CTLE	Continuous Time Linear Equalizer
CVT	Coordinated Video Timings (VESA)
DB	Data Byte
DDC/CI	Display Data Channel/Command Interface (VESA)
DE	Display Enable
DEM	Downstream Event Monitor
DFE	Decision Feedback Equalizer
DFP	Downstream-Facing Port
DisplayID	Display Identification Data
DJ	Deterministic Jitter
DMT	Discrete Monitor Timing (VESA)
DP	DisplayPort (VESA)
DPCD	DisplayPort Configuration Data
DP_PWR	DP Power
DPRX	DisplayPort receiver
DPRX_PHY	DPRX PHY Layer circuit

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Table 1-1: Acronyms, Initializations, and Abbreviations (Continued)

Acronym	Stands for
DPTX	DisplayPort transmitter
DPTX_PHY	DPTX PHY Layer circuit
DSC	Display Stream Compression
DST	Direct Stream Transfer
DTD	Display Timing Data
DVI	Digital Visual Interface
eDP	Embedded DisplayPort (VESA)
ECC	Error Correcting Code
ECF	Encryption Control Field
E-DDC	Enhanced Display Data Channel (VESA)
EDID	Extended Display Identification Data (VESA)
EMT	End_Of_Message_Transaction
EOC	End Of Chunk
EOM	End Of Message
EOS	Electrical Over-Stress
EQ	Equalization
ESD	Electro Static Discharge
ESI	Event Status Indicator
FEC	Forward Error Correction
fs	Pre-defined sample frequency
GPU	Graphics Processor Unit
GTC	Global Time Code
GUID	Globally Unique ID
HA	Horizontal Active height
HB	Header Byte
HBR	High Bit Rate (2.7Gbps/lane)
HBR2	High Bit Rate 2 (5.4Gbps/lane)
HBR3	High Bit Rate 3 (8.1Gbps/lane)
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
HSP	HSync Polarity
HSW	HSync Width
I^2C	Inter-Integrated Circuit
IRQ	Interrupt Request
ISI	Inter-Symbol Interference
LFSR	Linear Feedback Shift Register
LL	Link Layer

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Table 1-1: Acronyms, Initializations, and Abbreviations (Continued)

Acronym	Stands for
lsb	least significant bit
LSB	Least Significant Byte
LPCM	Linear Pulse Code Modulation
LT	Link Training
LVP	Link Verification Pattern
Maud	Maud value for audio
MBps	Megabytes/second
MCCS	Monitor Control Command Set (VESA)
mDP	Mini DisplayPort
MP/s	Megapixel/second
msb	most significant bit
MSB	Most Significant Byte
MOT	Middle Of Transaction
MST	Multi-Stream Transport
MTP	Multi-stream Transport Packet
MTPH	Multi-stream Transport Packet Header
Mvid	Mvid value for video
Naud	Naud value for audio
nb	Nibble
Nvid	Nvid value for video
NORP	Number Of Receiver Ports
OCP	Over Current Protection
OUI	Organizational Unique ID
PB	Parity Byte
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PH	Place Holder
PHY	Physical (used with “PHY Layer”)
PLL	Phase-Locked Loop
PM	Parity Marker
PoS	Point of Sync
ppr	peak pixel rate
PPS	Picture Parameter Set
PRBS	Pseudo Random Bit Sequence
PSR	Panel Self Refresh
PSR2	Panel Self Refresh, Version 2

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Table 1-1: Acronyms, Initializations, and Abbreviations (Continued)

Acronym	Stands for
RAD	Relative Address
RBR	Reduced Bit Rate
RC	Rate Control
RD	Running Disparity
RG	Rate Governing
RGB	Red Green Blue
RJ	Random Jitter
ROO	Region Of Overlap
RS	Reed-Solomon
RSN	Resource Status Notify
RT	Retimer
RTL	Register Transfer Level
RX	Receiver
SCMS	Serial Copy Management System (ANSI)
SDP	Secondary-Data Packet
SE	SDP End
SF	Stream Fill
SMT	Start_Of_Message_Transaction
SR	Scrambler Reset
SS	SDP Start
SSC	Spread-Spectrum Clock
SST	Single-Stream Transport
TBC	Time Base Converter
TBR	Time Base Recovery unit
TCON	Timing Controller
TDR	Time Domain Reflectometry
TG	Timing Generator
TIA	Timing Interval Analyzer
TIE	Timing Interval Error
TJ	Total Jitter
TMDS	Transition Minimized Differential Signaling
TU	Transfer Unit
TX	Transmitter
UFP	Upstream-Facing Port
UI	Unit Interval
VA	Vertical Active height
VB-ID	Vertical Blanking ID
VBL	Vertical Blank

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Table 1-1: Acronyms, Initializations, and Abbreviations (Continued)

Acronym	Stands for
VBP	Vertical Back Porch
VC	Virtual Channel
VCO	Voltage Controlled Oscillator
VCPF	Virtual Channel Payload Fill
VESA	Video Electronics Standards Association
VEV	Vertical Eye View
VFP	Vertical Front Porch
VHDL	Very high speed integrated circuit Hardware Description Language
VS	Vertical Sync
VSP	VSync Polarity
VSR	Vertical Space Region
VSW	VSync Width

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1.4 Glossary

Table 1-2: Glossary of Terms

Terminology	Definition
ANSI 8b/10b	Channel coding specification as specified in ANSI X3.230-1994, Clause 11.
Auxiliary channel	AUX CH. Physical property (pins and signal traces) over which AUX transaction traffic is routed. Half-duplex, bidirectional channel between a DPTX and DPRX. Consists of 1 differential pair transporting data. An upstream DP device is the master (also referred to as AUX requester) that initiates an AUX transaction. A downstream DP device is the slave (also referred to as AUX replier) that replies to the AUX transaction initiated by the requester.
Back channel	See the definition in Directionality terminology.
Box-to-box connection	DisplayPort link between two boxes that is detachable by an end-user. A DP cable-connector assembly for the box-to-box connection shall have four Main-Link lanes.
bits per component	bpc. Number of bits for each of R, G, B or Y, Cb, and Cr.
bits per pixel	bpp. Number of bits for each pixel: • For RGB and YCbCr 4:4:4, the bpp value is three times the bpc value. • For YCbCr 4:2:2, the bpp value is two times the bpc value. • For YCbCr 4:2:0, the bpp value is 1.5 times the bpc value. • For Y-only, the bpp value is equal to the bpc value.
Branch Device	See DP Branch device.
Captive cable	DP cable that is attached to Sink device and cannot be detached by an end-user. Captive DP cable may have one, two, or four Main-Link lanes, while an end-user-detachable cable is required to have four Main-Link lanes.
CEA range	Nominal zero luminance intensity level: • 16 for 24bpp • 64 for 30bpp • 256 for 36bpp • 1024 for 48bpp Maximum luminance intensity level at maximum code value allowed for bit depth: • 235 for 24bpp RGB • 940 for 30bpp RGB • 3760 for 36bpp RGB • 15040 for 48bpp RGB ***Note:*** *The RGB CEA range is defined for 24, 30, 36, and 48bpp RGB only.*
Chunk	Portion of the bitstream that comprises a set of data bytes. For each slice, there are the same number of Chunks as lines within a slice. Every Chunk is the same size because *DP v1.4* assumes a constant bit rate bitstream. (See *DSC v1.2* for further details.)
De-bouncing timer	A timer that counts the "de-bouncing period" to elapse after a mechanical contact (e.g., plugging in a cable-connector assembly to a receptacle connector) to give the signals on the connectors time to settle.
De-spreading	An operation by a Sink device for getting rid of down-spread of the stream clock when the clock is regenerated from the down-spread link symbol clock.

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Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
Directionality terminology (Downstream-facing port, downstream link, downstream device, upstream-facing port, upstream link, upstream device, Downward/Upward Message Transactions, Forward/Back Channel)	A link through which data is transmitted by the DPTX of a DP device (either DP Source or DP Branch device) is called a "downstream link" of the DP device and the port through which the link is driven is a "downstream-facing port" (DFP). A link through which data is received by the DPRX of a DP device (either DP Branch or DP Sink device) is called an "upstream link" of the DP device and the port through which the link is receiving data is an "upstream-facing port." (UFP). From the point of view of the device that transmits Main-Link data, device at the other end of link that receives the data is its downstream device. From the point of view of the device that receives Main-Link data, device at the other end of link that transmits the data is its upstream device. As for Sideband MSG and Message Transaction, a request Message Transaction (consisting of one or multiple request Sideband MSGs) originated by a DP device toward the downstream devices is called a downward-going request, or DOWN_REQ_MSG. A reply to the downward-going request is called an upward going reply, or UP_REP_MSG. A request Message Transaction originated by a DP device toward upstream devices is called an upward-going request, or UP_REQ_msg. A reply to the upward-going request is called a downward going reply, or DOWN_REP_MSG. For AUX transactions, the channel from upstream device to downstream device (used for request transactions) is the Forward channel and the channel from downstream device to upstream device (used for reply transactions) Back channel.
Display Line	Single row of active pixels across a display.
DisplayPort receiver	DPRX. Circuitry that receives the incoming DisplayPort Main-Link data. It also contains the transceiver circuit for AUX CH. Performs both PHY and Link Layer functions. Part of a DP downstream device (i.e., DP Sink device and DP Branch device).
DisplayPort transmitter	DPTX. Circuitry that transmits the DisplayPort Main-Link data. Also contains the transceiver circuit for AUX CH. Performs both PHY and Link Layer functions. Part of a DisplayPort upstream device (i.e., DP Sink device and DP Branch device).
DisplayPort Configuration Data (DPCD)	DPCD registers are mapped to the 20-bit address space of the DPRX. Each register is 8 bits wide. DPCD registers are used by the DPRX to declare its capabilities and status, and by DPTX to configure the DPRX by way of AUX transactions.
Down-spread	Spreading a clock frequency downward from a peak frequency. As compared to "center-spread", avoids exceeding the peak frequency specification.
Downstream-facing port	See the definition in Directionality terminology.
Downstream link	See the definition in Directionality terminology.
Downstream device	See the definition in Directionality terminology.
DP Branch device	Device containing DPRX and either DPTX or transmitter of another AV transport interface ("legacy interface"). DP PHY Repeater, having only PHY Layer portions of a DPTX and DPRX, is not a DP Branch device. Also referred to as a "Branch device" within this Standard.
DP PHY Repeater	Consists of the DPTX_PHY and DPRX_PHY.
DP Sink	Contains the DPRX and at least one stream sink.
DP Sink device	Device containing the DP Sink. Leaf device of DP topology. Also referred to as a "Sink device" within this Standard.
DP Source	Contains the DPTX and at least one stream source.
DP Source device	Device containing the DP Source. Root device of DP topology. Also referred to as a "Source device" within this Standard.

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Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
DST audio	***TBD***
embedded DisplayPort	eDP. Embedded connection, as specified in the VESA Embedded DisplayPort Standard.
Embedded Connection	DisplayPort link within a box that is not to be detached by an end-user. DisplayPort cable for the embedded connection may have one, two, or four Main-Link lanes.
Forward Channel	See the definition in Directionality terminology.
Gen-lock	Locking the output timing of a circuit to the input timing. For example, the DPRX may Gen-lock its Display Enable (DE) output timing to the timing of DE signal it receives from a transmitter on the other end of the link.
High-bandwidth Digital Content Protection	HDCP. One of the content protection system options for the DisplayPort link. ***Note:*** *HDCP is not part of the DP Standard.*
HPD pulse	There are two kinds of HPD (Hot Plug Detect) pulse, depending on the duration: • A Sink device, when issuing an IRQ (Interrupt ReQuest) to the Source device, must generate a low-going HPD pulse of 0.5ms through 1ms in duration. Upon detecting this "IRQ_HPD pulse", the Source device must read the DPCD Link/Sink Device Status registers and take corrective action. • When a Source device detects a low-going HPD pulse longer than 2ms in duration, it must be regarded as a hot plug event HPD pulse. Upon detecting this hot plug event HPD pulse, the Source device must read the DPCD Receiver Capability and Link/Sink Device Status registers and take corrective action.
Hybrid device	Either a Branch device or PHY Repeater device responsible for transporting data between a Source device and Sink device by means other than that provided for by PHY Layer, as defined in Section 3, and mechanical, cable-connector assembly specifications, as defined in Section 4.1. A Hybrid device may use alternative wired or wire-free means including optical or radio technology.
Idle Pattern	Main-Link Symbol pattern sent over the link when the link is active with no stream data being transmitted.
Leaf device	Sink device, located at a leaf in a DisplayPort tree topology.
Link clock recovery	Operation of recovering the link clock from the link serial bitstream.
Link Layer	Layer that handles the mapping between upper layer data and link symbols for the Main-Link and AUX CH.
Link Policy Maker	Manages the link and is responsible for keeping the link synchronized. All DisplayPort devices must have a Link Policy Maker.
Main-Link	Unidirectional channel for isochronous stream transport from DPTX to DPRX. Consists of one, two, or four lanes, or differential pairs. Supports four bit rates: • 8.1Gbps/lane (referred to as "high bit rate 3") • 5.4Gbps/lane (referred to as "high bit rate 2") • 2.7Gbps/lane (referred to as "high bit rate") • 1.62Gbps/lane (referred to as "low bit rate" or "reduced bit rate") ***Note:*** *6.75Gbps/lane link rate is supported between a MyDP DPTX and MyDP DPRX.*

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Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
Main-Link Symbol	Symbol types can be data or control: • Data symbols contain 8 bits of data and are encoded into 10-bit data characters by way of channel coding, as specified in ANSI X3.230-1994, Clause 11 (referred to as "ANSI 8b/10b" within this Standard) before being transmitted over a link. • DisplayPort also defines control symbols used to frame data symbols. Control symbols are encoded into 10-bit special characters of ANSI 8b/10b (called k-codes).
Main-Link Symbol clock	Clock with which Main-Link Symbols are transferred within PHY and Link Layer circuits of either DPTX or DPRX for Main-Link transport. The clock frequency is as follows: • 810MHz for 8.1Gbps/lane (high bit rate 3, HBR3) • 540MHz for 5.4Gbps/lane (high bit rate 2, HBR2) • 270MHz for 2.7Gbps/lane (high bit rate, HBR) • 162MHz for 1.62Gbps/lane (low bit rate, RBR)
Main Stream Attributes	Attributes describing the main video stream format in terms of geometry and color format. Inserted once per video frame during the video blanking period. Used by the DisplayPort receiver in reconstructing the stream.
Manchester transaction	AUX transaction using Manchester II encoding used for transfers at 1Mbps on the AUX CH.
Micro-packet	Vessel used for transporting data over a DP link.
Multi-stream Transport	MST. Format used for transporting multiple main video streams, each of which is enclosed in a VC Payload and may have a Secondary-Data Packet (SDP) stream, such as an audio stream (or SDP stream only without main video stream). Uses MTP (Multi-stream Transport Packet) as the unit of micro-packet. See also Single-stream Transport.
One Bit audio	***TBD***
Peak Pixel Rate	ppr. Maximum data rate in megapixels per second (MP/s) reported by the DSC decoder(s) in a DP DSC Sink device that a display requires for a given display mode (resolution and refresh).
Physical Layer	PHY Layer. Consists of logical and electrical sub-blocks. Handles channel encoding from/ decoding to link symbols, serialization/de-serialization, and serial bit stream transmission/ reception.

PRBS7	7-bit pseudo random bit sequence according to ITU-T Recommendation O.150, "General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment," May 1996.
	$G(x) = x^7 + x^6 + 1$ (non-inverted signal)
	Length of sequence = 127 bits
	The actual sequence must be:
	`----- direction ---→`
	`0010000011000010100`
	`0111100100010110011101010 01`
	`1111010000111000100100110 11`
	`0101101111011000110100101 11`
	`0111001100101010111111100 00`
	Note: *Upper left transmitted first and lower right transmitted last.*

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Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
Rendering function	Function of displaying/processing the stream data in devices such as video displays, speakers, and image format converters.
Root device	DP Source device, located at a root in a DisplayPort tree topology.
Secondary-data	Data transported over the Main-Link which is not main video stream data, such as audio data and INFOFRAME SDPs.
Single-stream Transport	SST. Format used for transporting a single main video stream which may have a Secondary-Data Packet stream, such as an audio stream (or an SDP stream only without main video stream). Uses TU (Transfer Unit) as the unit of micro-packet. See also Multi-stream Transport.
slice	Independently decodable set of compressed bits that represent a specified set of samples. The set of samples forms a rectangle in the horizontal and vertical dimensions. Decoding of any one slice does not depend on the decoded result or availability of another slice.
Stream Clock	Used for transferring stream data into a DPTX within a DP Source device or from a DPRX within a DP Sink device. Video and audio (optional) are likely to have separate stream clocks.
Stream Clock Regeneration	Operation of regenerating the stream clock from the Main-Link Symbol clock.
Stream Policy Maker	Manages transportation of an isochronous stream.
Timing Controller	TCON. Circuit that outputs control and data signals to driver electronics of a display device.
Time Stamp	A value used by a clock circuit to keep two systems synchronized.
Transfer Unit	TU. Used to carry main video stream data during its horizontal active period. TU has 32 to 64 symbols per lane (except at the end of the horizontal active period), each consisting of active data symbols and fill symbols.
Trickle Power	Power for Sink device that is sufficient to let the Source device read EDID via the AUX CH, but insufficient to enable Main-Link and other Sink device functions. For Sink device to drive the HPD signal high, at least the trickle power must be present. The amount of power needed for the trickle power is Sink device implementation-specific.
Upstream-facing port	See the definition in Directionality terminology.
Upstream link	See the definition in Directionality terminology.
Upstream device	See the definition in Directionality terminology.
Vertical Blanking ID	VB-ID. Data symbol sent immediately following a BS symbol sequence, indicating the AV stream transport status (e.g., vertical blanking interval or not, audio to be muted or not). Also used for content protection synchronization detection by the DPRX.
VESA range	Nominal zero luminance intensity level at code value zero. Maximum luminance intensity level is the maximum code value allowed for the bit depth: • 63 for 18bpp RGB • 255 for 24bpp RGB • 1023 for 30bpp RGB • 4095 for 36bpp RGB • 65535 for 48bpp RGB

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Table 1-2: Glossary of Terms (Continued)

Terminology	Definition
via	Cross-over between layers of a multi-layer PCB (printed circuit board).
Video Horizontal Timing	Horizontal timing means video line timing. For example, horizontal period and horizontal synchronization pulse mean line period and line synchronization pulse, respectively. The term “horizontal” does not necessarily correspond to the physical orientation of the display device. For instance, a line may be oriented vertically on a “portrait” display.
Video Vertical Timing	Vertical timing means video frame (or field) timing. For example, vertical period and vertical synchronization pulse mean a frame (or field) period and a frame synchronization pulse, respectively. The term “vertical” does not necessarily correspond to the physical orientation of the display device. For instance, a line may be oriented horizontally on a “portrait” display.

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1.5 Reference Documents

Table 1-3: Reference Documents

Document	Version/ Revision	Referenced As	Date
ANSI IEC 14496-3, Information Technology – Coding of Audio-Visual Objects – Part 3: Audio – see global.ihs.com	Edition 4.0	*IEC 14496-3*	August 1, 2015
ANSI IEC 60958 SET, Digital Audio Interface – All Parts – see global.ihs.com	Edition 1.0 en:2015	*IEC 60958*	2015
ANSI IEC 60958-1, Digital Audio Interface – Part 1, General – see global.ihs.com	Edition 3.0 b:2014	*IEC 60958-1*	April 1, 2014
ANSI IEC 60958-3, Digital Audio Interface – Part 3, Consumer Applications – see global.ihs.com	Edition 3.2 en:2015	*IEC 60958-3*	June 1, 2015
ANSI IEC 61937 SET, Digital Audio – Interface for Non-linear PCM Encoded Audio Bitstreams Applying IEC 60958 – All Parts – see global.ihs.com	Edition 1.0 b:2013	*IEC 61937*	2013
ANSI INCITS 230-1994, FibreChannel – Physical and Signaling Interface (FC-PH) – see global.ihs.com			1994
ANSI/EIA-364-09C, Durability Test Procedure for Electrical Connectors and Contacts – see global.ihs.com			June 1999
ANSI/EIA-364-13B, Mating and Unmating Forces Test Procedure for Electrical Connectors – see global.ihs.com			December 1998
ANSI/EIA-364-17B, Temperature Life with or without Electrical Load Test Procedure for Electrical Connectors and Sockets – see global.ihs.com			June 1999
ANSI/EIA-364-20C, Withstanding Voltage Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts – see global.ihs.com			June 2004
ANSI/EIA-364-21C, Insulation Resistance Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts – see global.ihs.com			May 2000
ANSI/EIA-364-23B, Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets – see global.ihs.com			December 2000
ANSI/EIA-364-27B, Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors – see global.ihs.com			May 1996
ANSI/EIA-364-28D, Vibration Test Procedure for Electrical Connectors and Sockets – see global.ihs.com			July 1999
ANSI/EIA-364-31B, Humidity Test Procedure for Electrical Connectors – see global.ihs.com			May 2000

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Table 1-3: Reference Documents (Continued)

Document	Version/ Revision	Referenced As	Date
ANSI/EIA-364-32C, Thermal Shock (Temperature Cycling) Test Procedure for Electrical Connectors and Sockets – see global.ihs.com			May 2000
ANSI/EIA-364-41C, Cable Flexing Test Procedure for Electrical Connectors – see global.ihs.com			June 1999
ANSI/EIA-364-70, Temperature Rise Versus Current Test Procedure for Electrical Connector and Sockets – see global.ihs.com			May 1998
ANSI/EIA-364-98, Housing Locking Mechanism Strength Test Procedure for Electrical Connectors – see global.ihs.com			June 1997
CEA-861.2, Advanced Audio Extensions – see global.ihs.com		*CEA-861.2*	August 1, 2015
CEA-861.3, HDR Static Metadata Extensions – see global.ihs.com		*CEA-861.3*	January 30, 2015
CEA-861-F, A DTV Profile for Uncompressed High Speed Digital Interface – see global.ihs.com		*CEA-861-F*	August 2013
CEA-931-B, Remote Control Command Pass-Through Standard for Home Networking – see global.ihs.com		*CEA-931-B*	September 2003
Digital Visual Interface (DVI)	1.0	*DVI r1.0*	April 2, 1999
High-Bandwidth Digital Content Protection System, Amendment for DisplayPort – see www.digital-cp.com	1.3/1.1		December 2009
High-Bandwidth Digital Content Protection System, Mapping HDCP to DisplayPort – see www.digital-cp.com	2.2		December 2012
High-Definition Multimedia Interface Specification – see www.hdmi.org	1.4b		October 2011
High-Definition Multimedia Interface Specification – see www.hdmi.org	2.0		September 2013
IEC 61000-4-2, Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test – see webstore.iec.ch	2.0		December 2008
IETF 4122, A Universally Unique IDentifier (UUID) URN Namespace – see www.ietf.org/rfc/rfc4122.txt			July 2005
ITU-R BT.2020, Parameter values for ultra-high definition television systems for production and international programme exchange – see www.itu.int/rec/R-REC-BT.2020/en			August 2012
ITU-R BT.601-6, Studio Encoding Parameters of Digital Television for Standard 4:3 and Wide Screen 14:9 Aspect Ratio – see www.itu.int/publications			January 2007

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Table 1-3: Reference Documents (Continued)

Document	Version/ Revision	Referenced As	Date
ITU-R BT.709-5, Parameter Values for the HDTV Standards for Production and International Programme Exchange – see www.itu.int/publications			April 2002
JEDEC JESD22-A114FElectrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) – see www.jedec.org/standards-documents			December 2008
VESA Glossary of Terms – see www.vesa.org	Current		Current
VESA Intellectual Property Rights (IPR) Policy – see www.vesa.org/wp-content/uploads/2014/04/VP-200C.pdf	200C		April 2014
VESA Coordinated Video Timings Standard	Version 1.2	*CVT v1.2*	***TBD***
VESA Display Data Channel Command Interface (DDC/CI) Standard	Version 1, Revision 1		October 2004
VESA DisplayPort Alt Mode on USB Type-C Standard	Version 1.0a	*DP Alt Mode on USB Type-C v1.0a*	August 5, 2015
VESA DisplayPort EDID Compliance Test Standard	Version 1.2	*DP EDID CTS v1.2*	***TBD***
VESA DisplayPort Panel Connector Standard	Version 1.1a		May 2009
VESA DisplayPort PHY Compliance Test Standard (PHY CTS)	Version 1.2b		November 26, 2012
VESA Display Stream Compression (DSC) Standard	Version 1.2	*DSC v1.2*	***TBD***
VESA Embedded DisplayPort (eDP) Standard	Version 1.4b	*eDP v1.4b*	October 23, 2015
VESA Enhanced Display Data Channel (E-DDC) Standard	Version 1, Revision 1		March 2004
VESA Enhanced Extended Display Identification Data (E-EDID) Standard	Release A, Revision 2		September 2006
VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT)	Version 1, Revision 13	*DMT v1 r13*	March 3, 2013
VESA Display Identification Data (DisplayID) Structure Standard	Version 1, Revision3		July 2013
VESA DockPort Standard	Version 1.0a	*DockPort v1.0a*	December 22, 2014
VESA Mini DisplayPort Connector (mDP) Standard	Version 1		October 2009
VESA Monitor Control Command Set (MCCS) Standard	Version 2, Revision 2		January 2009
VESA MST Use Case Example	Version 1		September 2011
VESA MyDP Standard	Version 1		October 2012
DVD Specifications for Read-Only Disc, Part 4: Audio Specification, Version 1.2	***TBD***		***TBD***

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1.6 Nomenclature for Bit and Byte Ordering

This section describes the bit and byte ordering of the Main-Link and AUX CH.

1.6.1 Bit Ordering

1.6.1.1 Parallel Bit Ordering

- Main-Link
  - Within a byte, bit 0 is the least significant bit (lsb) and bit 7 is the most significant bit (msb).

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

  - For 8 bits per component (bpc), red bit 7 (R7) is placed at bit 7 and red bit 0 (R0) is placed at bit 0

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R7	R6	R5	R4	R3	R2	R1	R0

  - For 6bpc, red bit 5 is placed at bit 7 (R5) and green bit 4 (G4) is placed at bit 0

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R5	R4	R3	R2	R1	R0	G5	G4

- AUX CH
  - Within a byte, bit 0 is the least significant bit while bit 7 is the most significant bit

1.6.1.2 Serial Bit Ordering after Channel Encoding

- Main-Link (ANSI 8b/10b)
  - The least significant bit is transmitted first and the most significant bit last.
- AUX CH (Manchester-II)
  - The most significant bit is transmitted first and the least significant bit last.

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1.6.2 Byte Ordering

- Main-Link, main stream
  - The most significant byte is transmitted first.
    For example, if the color bit depth of an RGB pixel is 16bpc, R15:8 (red bits 15:8) is transmitted first and is followed by R7:0 (Red bits 7:0).

R15:8
R7:0

  - When certain parameters of the main stream attribute packet have multiple bytes, the most significant byte is transmitted first.
    For example, Mvid23:16 is transmitted first, followed by Mvid15:8, and then by Mvid7:0.

Mvid23:16
Mvid15:8
Mvid7:0

  - Main-Link, Secondary-Data Packet (SDP)
  - The least significant byte is transmitted first as shown in the audio sample data example below.

Audio sample0 channel0 byte 0
Audio sample0 channel0 byte 1
Audio sample0 channel0 byte 2
Audio sample0 channel0 byte 3

- AUX CH
  - In burst write/read operations over the AUX CH, the address is increased by one after each data byte. For the DPCD fields that have multiple bytes, the least significant byte is stored at the lowest address, unless otherwise explicitly stated in the DPCD Address Mapping table (e.g., in DPCD Addresses 00222h through 00231h, the least significant byte is stored at the upper address). During the burst operation of an AUX transaction, therefore, the least significant byte is transported first.

Source IEEE OUI first two hex digits (DPCD Address 00300h)
Source IEEE OUI second two hex digits (DPCD Address 00301h)
Source IEEE OUI third two hex digits (DPCD Address 00302h)

Note: *As specified in Section 1.6.1, the most significant bit is transported first, and the least significant last over the AUX CH.*

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1.7 Overview of DisplayPort

A DisplayPort link is comprised of the following:

- Main-Link

  The Main-Link is a unidirectional, high-bandwidth, low-latency channel that is used to transport isochronous data streams, such as uncompressed video and audio.

- Auxiliary channel (AUX CH)

  The AUX CH is a half-duplex, bidirectional channel that is used for link management and device control.

- Hot Plug Detect (HPD) signal line

  The HPD signal also serves as an interrupt request by the Sink device.

In addition, the DP connector for a box-to-box connection has a power pin for powering a local device.

Figure 1-1: DisplayPort Data Transport Channels

1.7.1 Makeup of the Main-Link

The Main-Link consists of one, two, or four AC-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration because the DPTX and DPRX may have different common mode voltages.

Four link rates are supported – 8.1, 5.4, 2.7, and 1.62Gbps/lane. All enabled lanes must be operating at the same link rate. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values Mvid and Nvid. The capabilities of the DPTX and DPRX, and the quality of the channel (or a cable) will determine whether the link rate is set to 8.1, 5.4, 2.7, or 1.62Gbps/lane.

Note: *6.75Gbps link rate is supported between a MyDP DPTX and MyDP DPRX.*

The number of lanes of Main-Link is one, two, or four lanes. The number of lanes is decoupled from the pixel bit depth (bits per pixel, or bpp) and component bit depth (bits per component, or bpc). Component bit depths of 6, 8, 10, 12, and 16 are supported with the pixel encoding formats of RGB, YCbCr 4:4:4 / 4:2:2 / 4:2:0 Y-only in DisplayPort, regardless of the number of Main-Link lanes. For RAW pixel encoding format, bit depths of 6, 7, 8, 10, 12, 14, and 16 bits per pixel are supported.

All lanes carry data. There is no dedicated clock channel. The clock is extracted from the data stream itself that is encoded with ANSI 8b/10b coding rule. (Channel coding is specified in ANSI X3.230-1994, Clause 11.)

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Source and Sink devices are allowed to support the minimum number of lanes required for their needs. The devices that support two lanes are required to support both one and two lanes, while those that support four lanes are required to support one, two and four lanes. An external cable that is detachable by an end-user is required to support four lanes to maximize the interoperability between Source and Sink devices.

Excluding the 20% channel coding overhead, the DisplayPort Main-Link provides for the application bandwidth (also called the link symbol rate) listed in Table 1-4.

Table 1-4: DP Main-Link Application Bandwidth

Link Rate (Gbps)	# of Lanes	Application Bandwidth (MBps)
8.1	One	810
	Two	1620
	Four	3240
6.75[a]	One	675
5.4	One	540
	Two	1080
	Four	2160
2.7	One	270
	Two	540
	Four	1080
1.62	One	162
	Two	324
	Four	648

a. 6.75Gbps link rate is supported between a MyDP DPTX and MyDP DPRX.

DisplayPort devices may freely trade pixel bit depth with pixel format and the frame rate of a stream within the available bandwidth.

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The data mapping of a stream to the Main-Link is devised to facilitate the support of various lane counts. For example, the pixel data is packed and mapped over a 4-lane Main-Link, as listed in Table 1-5, regardless of the pixel bit depth and colorimetry format.

Table 1-5: Pixel Data Mapping over 4-lane Main-Link

Pixels	Lane #
0, 4	0
1, 5	1
2, 6	2
3, 7	3

The stream data is packed into "micro-packets" which are called "transfer units" in SST (Single Stream Transport) mode and MTP (Multi-stream Transport Packet) in MST (Multi-Stream Transport) mode. After the stream data is packed and mapped to the Main-Link, the packed stream data rate will be equal to or smaller than the link symbol rate of the Main-Link. When it is smaller, stuffing symbols are inserted.

1.7.2 Makeup of AUX CH

AUX CH consists of an AC-coupled, doubly-terminated differential pair. Manchester-II coding is used as the channel coding for AUX transaction over AUX CH. As is the case with Main-Link, the clock is extracted from the data stream.

AUX CH has a half-duplex, bidirectional PHY Layer. The Source device is the master and the Sink device the slave. A Sink device may toggle the HPD signal to prompt the Source device to initiate an AUX request transaction to read DPCD Link/Sink status register bits, including the IRQ_HPD Vector register bits.

AUX CH provides a data rate of 1Mbps over the supported cable lengths of up to 15m and longer. Each transaction takes no more than 500us with a maximum burst data size of 16 bytes. This avoids AUX CH contention problems by one application starving other applications.

1.7.3 Link Configuration and Management

Upon an HPD event, the Source device configures the link through link training. The correct number of lanes is enabled at the correct link rate with the correct drive current and equalization level through AUX transactions between a DPTX and DPRX over AUX CH.

During normal operation following link training, the Sink device may notify a link status change, for example, loss of synchronization, by toggling the HPD signal for interrupt request signaling. The Source device then checks the DPCD Link/Sink Device Status registers using AUX transactions and then takes corrective action. This closed-loop operation enhances the robustness and interoperability between the Source and Sink devices.

Because the link rate is decoupled from the stream rate, the DisplayPort link may stay active and stable, even when the timing of a transported AV stream changes.

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1.7.4 Layered Modular Architecture

Figure 1-2 shows the layered architecture of DisplayPort.

Figure 1-2: Layered Architecture

In Figure 1-2, DisplayPort Configuration Data (DPCD) in the Sink device describes the capability of the DPRX, just as EDID describes that of the stream sink. Link and Stream Policy Makers manage the link and stream, respectively. Details (state machine, firmware, or system software) are implementation-specific.

Note: *At some future time, the PHY Layer may be replaced while the Link Layer remains unchanged. This allows this Standard to evolve along with the technology, to maintain its cost and performance position.*

Also, the micro-packet-based data transport enables a seamless extension of this Standard toward supporting multiple audio-visual streams and other data types. Switches and hubs may be used to route streams among multiple Source and Sink devices.

When content protection is required, it is recommended that HDCP Version 1.3 Amendment for DisplayPort Revision 1.1 and HDCP Version 2.2 for DisplayPort be used.

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2 Link Layer

2.1 SST Mode Introduction

This section describes the services provided by the Link Layer of DisplayPort in Single-stream Transport (SST) mode. (Sub-sections within this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles.) These services are:

- Isochronous transport services over the Main-Link

  The isochronous transport services, based on a micro-packet architecture, maps the video and audio streams onto the Main-Link Symbols with a set of rules (explained in Section 2.2), so that the streams can be correctly re-constructed into the original format and time base in the Sink device.

- Link and device management services over the AUX CH

  Link services are used for discovering, configuring, and maintaining the link. The AUX transaction to access the DisplayPort Configuration Data (DPCD) address is used for these purposes. Device services support device-level applications, such as EDID read and MCCS control. In addition, AUX transactions may be used for optional content protection.

In conjunction with the description of these services, AUX states/arbitration and transaction syntax are also covered in this section.

Figure 2-1: Overview of Link Layer Services

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The Link Layer provides services as instructed or requested by the Stream/Link Policy Makers (Figure 2-1). The Stream Policy Maker manages the transport of the stream. The Link Policy Maker manages the link and is responsible for keeping the link synchronized.

In this section (and in the entire Standard), only the interactions between the policy makers and Link Layer are described. The syntax for these interactions (i.e., the API) is implementation-specific and beyond the scope of this Standard.

2.1.1 Number of Lanes and Per-lane Data Rate (Applicable in both SST and MST Modes)

DisplayPort supports three options for the number of Main-Link lanes and four options for Main-Link data rate per lane, as follows:

- 4-, 2-, or 1-lane
- 8.1, 5.4, 2.7, or 1.62Gbps/lane

Note: *6.75Gbps link rate is supported between a MyDP DPTX and DPRX.*

The stream data to Main-Link Symbols mapping is defined to facilitate the support of these lane count options.

The per-lane data rate is determined not only by the PHY Layer capabilities of DPTX and DPRX, but also by the quality of a channel consisting of PCB traces and/or a cable connector assembly.

A DP device with a DPRX must indicate its receiver capability in the Receiver Capability registers (DPCD Addresses 00000h through 000FFh; see Table 2-155) and Extended Receiver Capability registers (DPCD Addresses 02200h through 022FFh; see Table 2-165), as described.

After reading the receiver capability, a DP device with a DPTX must configure the link by writing to the Link Configuration field (DPCD Addresses 00100h through 001FFh; see Table 2-156) of the DPRX of the downstream device, and then running link training.

Through this process of receiver capability discovery and link training, the upstream DP device and the downstream DP device are able to negotiate for the optimal lane count and per-lane data rate for a given connection.

2.1.2 Number of Main, Uncompressed Video Streams in SST Mode

The scope of this Standard is limited to the transport of a single, uncompressed video stream as the main stream, with the optional insertion of SDPs such as an Audio Stream SDP.

2.1.3 Basic Functions (Applicable in both SST and MST Modes)

The basic functions of DP devices are as follows:

- **DPTX function** – Transmitter of Main-Link Symbols
- **DPRX function** – Receiver of Main-Link Symbols
- **Stream source function** – Sourcing of stream data
- **Stream sink function** – Sinking (i.e., consuming) of stream data

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2.1.4 DisplayPort Device Types and Link Topology in SST Mode

A device contains at least one DP function, as well as other functions such as a stream source, display, speakers, recording device, or even an entire computer.

Table 2-1 lists the device types covered by this Standard.

Table 2-1: Device Types Covered by this Standard

Device Type		Description
Source		Device that contains one or more stream source functions and DPTX functions and is a root in a DP tree topology.
Sink		Device that contains one or more DPRX functions and one or more stream sink functions and is a leaf in a DP topology.
Branch	DP Repeater (one input, one output)	Branch device that contains one DPRX and one DPTX.
	Legacy-to-DP Converter (one input, one output)	Branch device that contains one legacy RX and one DPTX. From the point of view of a DP topology, appears as a DP Source device.
	DP-to-Legacy Converter (one input, one output)	Branch device that contains one DPRX and one legacy TX.
	DP Replicator (one DPRX and *k* DPTXs, where *k* is a positive integer > 1)	Branch device that may include one or more legacy converter TXs.
	Output Switch (one DPRX and *k* DPTXs legacy TXs, where *k* is a positive integer > 1)	Branch device. Unlike a DP Replicator, only one DPTX (or legacy TX) is selected at a time. After one TX is selected, operates either as a DP Repeater or DP-to-Legacy Converter.
	Input Switch (*k* DPRXs and one DPTX, where *k* is a positive integer >1)	Branch device that operates as a DP Repeater after a single DPRX is selected.
	DP Composite Sink	Branch device with a stream sink function. For example, a display that has one or more downstream-facing ports (DFPs). A stream format converter that alters the stream format is regarded as a Composite Sink device.

DP devices with a DPTX and/or DPRX must have a Link Policy Maker. A Source device that originates or processes (e.g., stream format conversion) the stream data and Sink devices must also have a Stream Policy Maker.

Note: *A device containing the PHY Layer of a DPRX and DPTX only (i.e., DPRX_PHY and DPTX_PHY) is called a PHY Repeater, which is also referred to as a Cable Extender. Hybrid devices that perform the interface media converter (e.g., between electrical and optical) are typically built as Cable Extender devices.*

DP devices with a DPRX must have DPCD registers. Sink devices and Composite Sink devices must also have EDID.

Using the device types listed in Table 2-1, DP networks consisting of a single link or multiple links (daisy chain or tree) may be configured.

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From the perspective of the device location within a link, the devices are categorized as listed in Table 2-2.

Table 2-2: Topological Device Categories

Device Category	Device Type
Root	Source
Leaf	Sink
Intermediate	Branch devices listed in Table 2-1

The Source device needs to read the receiver capability (DPCD RX Capability registers), the stream sink capability (EDID), and speaker presence (MCCS) from its downstream device to source a stream accordingly.

Figure 2-3 through Figure 2-7 show examples of DP link topologies.

Figure 2-2: Single DP Link

Figure 2-3: DP Source Device-to-DP Sink Device via a DP Repeater

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Figure 2-4: DP Source Device-to-Legacy Sink via DP-to-Legacy Converter

Figure 2-5: Legacy Source Device-to-DP Sink Device via a Legacy-to-DP Converter

Figure 2-6: Multiple DP Source Devices-to-DP Sink Device via an Input Switch

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When only one DPTX is selected at a given time, a Replicator device (as shown in Figure 2-7) becomes an Output Switch device.

Figure 2-7: DP Source Device to Multiple DP Sink Devices via a DP Replicator

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2.1.4.1 EDID and DPCD Access Handling by SST-only Mode Branch Devices

Upon an EDID read by the DP Source device, a Branch device must reply with the EDID of the downstream DP Sink device.

The DP Repeater must update the MAX_LINK_RATE and MAX_LANE_COUNT register (DPCD Addresses 00001h and 00002h, respectively) values to those of the downstream device's DPRX when the following two conditions are met:

- DP Repeater is incapable of changing the link rate and lane count from the upstream link to the downstream link
- MAX_LINK_RATE and MAX_LANE_COUNT register values of the downstream device's DPRX are smaller than those of the DP Repeater's DPRX

In case the DP Repeater is capable of setting the link rate and lane count of the DFP independent of those of the upstream-facing port (UFP), and the downstream device is a DP Sink device, the DP Branch device does not need to update the Receiver Capability field registers (DPCD Addresses 00000h through 000FFh; see Table 2-155).

The description of the following two cases explains the rationale behind the above.

- **Case A – Maximum link bandwidth of the DP Branch device's DPRX is greater than or equal to that of the downstream DP Sink device's DPRX**

  The DP Sink device is required to have the maximum link bandwidth that covers all the video timing formats that are declared in its EDID. As the DP Source device selects the video timing format from those listed in the EDID, the maximum link bandwidth of the DP Sink device's DPRX does not gate the transmission of the video stream.

- **Case B – Maximum link bandwidth of the DP Branch device's DPRX is less than or equal to that of the downstream DP Sink device's DPRX**

  The DP Source device is required to select the video timing format whose stream bandwidth fits within the maximum link bandwidth of the DP Branch device's DPRX

In case the DP Repeater is capable of setting the link rate and lane count of the DFP independent of those of the UFP, but its downstream device is a DP-to-legacy downstream device, the DP Repeater must update the following DFP Capability registers:

- DOWN_STREAM_PORT_PRESENT register(s) (DPCD Addresses 00005h and 02205h)
- Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh), including the maximum pixel clock rate and pixel bit depth of the downstream legacy transmitter

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The reason is that when the following two conditions are met, a DP Source device can choose to send a video stream whose stream bandwidth exceeds that of the DP-to-legacy converter DPRX's maximum link bandwidth:

- MAX_LINK_RATE and MAX_LANE_COUNT register values of the DP Repeater's DPRX are larger than those of the DP-to-legacy converter's DPRX
- EDID of a legacy Sink device plugged into the DP-to-legacy converter declaring support for video formats whose stream bandwidth requirements exceed the link bandwidth of the DP-to-legacy converter's DPRX

A DP-to-legacy converter is required to report the maximum pixel clock and pixel bit depth of the DFP legacy transmitter that fit within the link bandwidth of its DPRX. By the DP Repeater's copying the DP-to-legacy converter's DFP capability registers, the stream bandwidth transmitted by the DP Source device is kept within the DP-to-legacy converter's DPRX link bandwidth limit.

2.1.4.1.1 EDID and DPCD Access Handling by SST-only Replicator Device

A DP Replicator device must use the EDID and DPCD of the lowest DFP number that has the connected downstream device.

2.1.4.1.2 EDID and DPCD Access Handling by SST-only Composite Sink Device (Informative)

Handling of EDID and DPCD access by a composite device is implementation-specific. For example, it may reply with the EDID of its own Sink device and may choose not to comprehend the DPCD of its downstream link.

Note: *In SST mode, this Standard does not currently define a mechanism through which the upstream device can read multiple EDIDs of Sink devices connected to Branch device(s).*

2.1.4.2 Docking Station (Informative)

A docking station is either a Replicator device or a Composite Sink device (with format converting function) embedded in a Source device. Because it is embedded, the management policy is implementation-specific and beyond the scope of this Standard.

2.2 Isochronous Transport Services in SST Mode

The isochronous transport services of the Link Layer provide the following:

- Mapping of stream data to and from the Main-Link lanes
  - Packing and unpacking
  - Stuffing and unstuffing
  - Framing and unframing
  - Inter-lane skewing and de-skewing
- Stream clock regeneration
- Insertion of main stream attributes data
- Optional insertion Secondary-Data Packet (SDP) with ECC
  - Audio_Stream SDP
  - *CEA-861-F* INFOFRAME SDP

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2.2.1 Main Stream to Main-Link Lane Mapping in the Source Device

The Main-Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with SDP and inter-lane skewed before it is handed over to the PHY Layer after the Link Layer data mapping for transport over the Main-Link. The stream data must enter the Link Layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY Layer at the LS_Clk rate after this mapping.

Figure 2-8 and Figure 2-9 show the data mapping in Source (DPTX) and Sink (DPRX) devices, respectively.

Figure 2-8: High-Level Block Diagram of DPTX Main-Link Data Path

Notes: *Logical block diagram. Actual implementation may vary.*

The ECC and CP encryption blocks are both optional. To support SDPs, however, ECC is required.

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Figure 2-9: High-Level Block Diagram of DPRX Main-Link Data Path

Notes: *Logical block diagram. Actual implementation may vary.*

The ECC and CP decryption blocks are both optional. To support SDPs, however, ECC is required except for the extension Secondary packet (Section 2.2.5.4).

Main-Link data mapping must take place in the following order:

- Main stream data packing, stuffing, and framing
- Optional secondary-data framing and multiplexing

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2.2.1.1 Default Framing Mode Control Symbols

The use of Default Framing mode is deprecated. Table 2-3 lists the Default Framing symbols for the sake of completeness only.

Table 2-3: Control Symbols for Default Framing Mode

Symbol	Name	Description
BS	Blanking Start	For DPRX with a DPCD Revision of 1.2 or higher, the Enhanced Framing mode described in Section 2.2.1.2 must be used when running in SST mode. An upstream device interoperating with a downstream device with DPCD Revision of 1.2 or higher must enable Enhanced Framing mode. Blanking Start consists of a 4-symbol sequence on each lane: • Inserted after the last active pixel during the vertical display period. • Inserted at the same symbol time during vertical blanking period as during vertical display. • This framing symbol must be periodically (every 2^{13} or 8192 symbols) inserted for active links with no main video stream data to send. In this condition, the BS symbol is immediately followed by the NoVideoStream_Flag bit in the VB-ID (bit 3) set to 1. (For more information on VB-ID, see Section 2.2.1.) This link symbol pattern is referred to as the "Idle Pattern."
BE	Blanking End	Inserted immediately before the first active pixel of a line only during the vertical display period.
FS	Fill Start	• Inserted at the beginning of stuffing symbols in the transfer unit. • Omitted when there is only one stuffing symbol. In this case, FE (Fill End) is inserted without FS. • FS and FE are inserted with no stuffing data symbols in between when there are only two stuffing symbols. ***Note:*** *Transfer unit is described in Section 2.2.1.4.1.*
FE	Fill End	Inserted at the end of stuffing symbols within transfer unit.
SS	Secondary-data Start	Inserted at the beginning of secondary-data.
SE	Secondary-data End	Inserted at the end of secondary-data.
SR	Scrambler Reset	For DPRX with a DPCD Rev. of 1.2 or higher, the Enhanced Framing mode described in Section 2.2.1.2 must be used when running in SST mode. An upstream device interoperating with a downstream device whose DPCD Rev. is 1.2 or higher must enable Enhanced Framing mode. In Enhanced Framing Mode, the Scrambler Reset consists of four symbol sequence on each lane. Every 512th BS symbol must be replaced with an SR symbol by a DPTX to reset the LFSR of the scrambler.

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Table 2-3: Control Symbols for Default Framing Mode (Continued)

Symbol	Name	Description
CPBS	Content Protection BS	For DPRX with a DPCD Rev. of 1.2 or higher, the Enhanced Framing mode described in Section 2.2.1.2 must be used when running in SST mode. An upstream device interoperating with a downstream device whose DPCD Revision is 1.2 or higher must enable Enhanced Framing mode. In Enhanced Framing mode, the Content Protection BS consists of a 4-symbol sequence on each lane. Used by a CP system. Called "CP" symbol in the Enhanced Framing mode described in Section 2.2.1.2.
CPSR	Content Protection SR	For DPRX with a DPCD Rev. of 1.2 or higher, the Enhanced Framing mode described in Section 2.2.1.2 must be used when running in SST mode. An upstream device interoperating with a downstream device whose DPCD Rev. is 1.2 or higher must enable Enhanced Framing mode. In Enhanced Framing mode, the Content Protection SR consists of a 4-symbol sequence on each lane. Used by a CP system. CPSR resets the LFSR of the scrambler just as SR does. Called "BF" symbol in the Enhanced Framing mode described in Section 2.2.1.2.

These control symbols must be inserted in all lanes in the same LS_Clk cycle (before they get inter-lane skewed by 2 LS_Clk cycles just before going to the PHY Layer). The Link Layer must distinguish these control symbols from data symbols so that the PHY Layer can properly encode these control symbols using "special characters."

For example, the Link Layer may use the ninth bit to indicate whether the accompanying 8-bit data represents control symbols or data symbols. There are many ways for the Link Layer to implement this distinction, the method used is implementation-specific and beyond the scope of this Standard.

2.2.1.2 Enhanced Framing Mode Control Symbols

Table 2-4 lists the Control Symbols used for Enhanced Framing mode. (See Table 2-3 for descriptions of the framing symbols.) A DPRX must support Enhanced Framing mode, and therefore must set the ENHANCED_FRAME_CAP bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 7). A DPTX must always enable Enhanced Framing mode by writing 1 to the ENHANCED_FRAME_EN bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 7).

These control symbols must be inserted in all lanes in the same LS_Clk cycle (before they are inter-lane skewed by 2 LS_Clk cycles just before going to the PHY Layer). The Link Layer must distinguish these control symbols from data symbols so that the PHY Layer can properly encode these control symbols using "special characters."

For example, the Link Layer can use the ninth bit to indicate whether the accompanying 8-bit data represents control symbols or data symbols. There are many ways for the Link Layer to implement this distinction – the method used is implementation-specific and beyond the scope of this Standard.

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Table 2-4: Enhanced Framing Mode Control Symbols

Default Framing Mode Symbols (Deprecated)	Enhanced Framing Mode Symbols
BS	BS + BF + BF + BS
SR	SR + BF + BF + SR
CPBS (called CP symbol in Enhanced Framing Mode)	BS + CP + CP + BS
CPSR (called BF symbol in Enhanced Framing Mode)	SR + CP + CP + SR
BE	BE (no change)
FS	FS (no change)
FE	FE (no change)
SS	SS (no change)
SE	SE (no change)

The mapping of these control symbols to ANSI 8b/10b special characters is described in Section 3.

When a DPTX is transmitting the Idle Pattern, the DPTX must insert the 4-symbol sequence of BS (or SR) every 2^{13} or 8192 symbols. In other words, there must be 8188 symbols between the last (fourth) symbol of the 4-symbol sequence for BS (or SR) and the first symbol of the next 4-symbol sequence.

Every 512th BS symbol sequence must be replaced with SR symbol sequence. The last symbol of the 4-symbol sequence for SR must be used to reset the scrambler.

When switching between the Idle Pattern transmission and a stream transmission, the Source device must avoid any overlap of the four symbols for BS and SR.

2.2.1.3 Main Video Stream Data Packing

The Link Layer must first steer pixel data in a pixel-within-lane manner, as shown in Table 2-5.

Table 2-5: Pixel Steering into Main-Link Lanes

# of Lanes	Pixel Steering[a]
One	All pixels to Lane 0
Two	Pixel 2*N* to Lane 0 Pixel 2*N* + 1 to Lane 1
Four	Pixel 4*N* to Lane 0 Pixel 4*N* + 1 to Lane 1 Pixel 4*N* + 2 to Lane 2 Pixel 4*N* + 3 to Lane 3

a. N is 0 or a positive integer.

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These rules apply regardless of the color space/pixel bit depth of the video stream. As shown in Figure 2-10, the first set of active partial pixel data of a line must follow the control symbol, BE.

Figure 2-10: Main Video Stream Data Packing Example for a 4-Lane Main-Link

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When there is no audio stream transported, Maud7:0 must be cleared to 00h. When there is no video stream transported, Mvid7:0 must be cleared to 00h.

During the last symbol time for a line of pixel data, there may be insufficient pixel data to provide data on all lanes of the link. The DPTX must send 0s for those bits (zero-padded bits).

Immediately following the last symbol period of a line of data the control symbol sequence, namely, BS symbol sequence, must be inserted on all lanes of the link.

The Sink device, knowing the number of active pixels per horizontal line (from the main stream attribute), must discard zero-padded bits as "don't care." Figure 2-10 shows that a new line must always start with pixel 0 on Lane 0 following BE.

The BS must be followed on all lanes by VB-ID, Mvid7:0, and Maud7:0:

- VB-ID must carry the following information:
  - Whether the main video stream is in the vertical display period or the vertical blanking period.
  - Whether the main video stream is in the odd field or the even field for interlaced video.
  - Whether the main video stream is interlaced or non-interlaced (progressive).
  - Whether the BS is inserted while no video stream is being transported. The symbols transmitted over the Main-Link when no video stream is active are shown in Table 2-6.
  - Whether to mute the audio.
- **Mvid7:0**

  The least significant eight bits of the time stamp value Mvid for the video stream. When there is no video stream transported, these bits must be cleared to 00h. The DP Sink device must use the time stamp as a hint for pixel clock recovery.
- **Maud7:0**

  The least significant eight bits of the time stamp value Maud for the audio stream. When there is no audio stream transported, these bits must be cleared to 00h. The DP Sink device must use the time stamp as a hint for audio clock recovery.

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Table 2-6: VB-ID Bit Definition

VB-ID Bit #	Bit Definition
0	**VerticalBlanking_Flag** Must be set to 1 at the end of the last active line of a video frame and remain set to 1 during the vertical blanking period. A Source device may clear this bit in the VB-ID either immediately prior to the first active line of a video frame (i.e., the first BE of a video frame) or immediately after the first active line (i.e., the first BS ending the first active line of a video frame). A Sink device must be able to handle either case. This bit is also set to 1 when there is no video stream (as indicated by bit 3 being set to 1).
1	**FieldID_Flag** This bit must be set to: • 0 right after the last active line in the top field • 1 right after the last active line of the bottom field See Section 2.2.4.2 for definitions of the top and bottom fields. For progressive (non-interlaced) video, there is no bottom video and this bit remains cleared to 0.
2	**Interlace_Flag** Must be set to 1 when the main stream is an interlaced video. For non-interlaced video or no video, this bit must remain cleared to 0.
3	**NoVideoStream_Flag** Must be set to 1 when preceding BS is inserted while no video stream is transported. When this bit is set to 1, the Mvid7:0 value must be "don't care." ***Note:*** *An audio stream may be transported even when no main video stream is being transported.*
4	**AudioMute_Flag** Must be set to 1 when the audio is to be muted.
5	**HDCP SYNC DETECT** Used by HDCP-capable DPRXs to detect CP lock status. See HDCP Specification 1.3 – Amendment for DisplayPort and HDCP on DisplayPort Specification 2.2.
6	**CompressedStream_Flag** New to *DP v1.4* to support Display Stream Compression (DSC).
7	**RESERVED** Read 0.

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Figure 2-11: Link Symbols over the Main-Link without Main Video Stream

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The VB-ID, Mvid7:0, and Maud7:0 must be transported four times, regardless of the number of lanes in the Main-Link, as shown in Figure 2-12.

Figure 2-12: VB-ID, Mvid7:0, and Maud7:0 Packing over the Main-Link

If there is no audio stream, Maud7:0 must be cleared to 00h.

If there is no video stream, Mvid7:0 must be cleared to 00h.

Table 2-7 is an example of how a video stream with pixel format of 1366x768 and 10 bits per component (bpc) (= 30 bits per pixel (bpp)) RGB pixels are mapped to a 4-lane Main-Link.

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Table 2-7: 10bpc RGB (30 bits per pixel)
1366x768 Packing to a 4-Lane Main-Link[a, b]

Lane 0		Lane 1		Lane 2		Lane 3		
BE		BE		BE		BE		
R0-9:2		R1-9:2		R2-9:2		R3-9:2		<-- Start of Active Pixel
R0-1:0	G0-9:4	R1-1:0	G1-9:4	R2-1:0	G2-9:4	R3-1:0	G3-9:4	
G0-3:0	B0-9:6	G1-3:0	B1-9:6	G2-3:0	B2-9:6	G3-3:0	B3-9:6	
B0-5:0	R4-9:8	B1-5:0	R5-9:8	B2-5:0	R6-9:8	B3-5:0	R7-9:8	
R4-7:0		R5-7:0		R6-7:0		R7-7:0		
G4-9:2		G5-9:2		G6-9:2		G7-9:2		
G4-1:0	B4-9:4	G5-1:0	B5-9:4	G6-1:0	B6-9:4	G7-1:0	B7-9:4	
B4-3:0	R8-9:6	B5-3:0	R9-9:6	B6-3:0	R10-9:6	B7-3:0	R11-9:6	
R8-5:0	G8-9:8	R9-5:0	G9-9:8	R10-5:0	G10-9:8	R11-5:0	G11-9:8	
G8-7:0		G9-7:0		G10-7:0		G11-7:0		
B8-9:2		B9-9:2		B10-9:2		B11-9:2		
B8-1:0	R12-9:4	B9-1:0	R13-9:4	B10-1:0	R14-9:4	B11-1:0	R15-9:4	
R12-3:0	G12-9:6	R13-3:0	G13-9:6	R14-3:0	G14-9:6	R15-3:0	G15-9:6	
G12-5:0	B12-9:8	G13-5:0	B13-9:8	G14-5:0	B14-9:8	G15-5:0	B15-9:8	
B12-7:0		B13-7:0		B14-7:0		B15-7:0		

R1360-9:2		R1361-9:2		R1362-9:2		R1363-9:2		
R1360-1:0	G1360-9:4	R1361-1:0	G1361-9:4	R1362-1:0	G1362-9:4	R1363-1:0	G1363-9:4	
G1360-3:0	B1360-9:6	G1361-3:0	B1361-9:6	G1362-3:0	B1362-9:6	G1363-3:0	B1363-9:6	
B1360-5:0	R1364-9:8	B1361-5:0	R1365-9:8	B1362-5:0		B1363-5:0		
R1364-7:0		R1365-7:0						
G1364-9:2		G1365-9:2						
G1364-1:0	B1364-9:4	G1365-1:0	B1365-9:4					
B1364-3:0		B1365-3:0						<-- End of Active Pixel
BS		BS		BS		BS		
VB-ID		VB-ID		VB-ID		VB-ID		
Mvid7:0		Mvid7:0		Mvid7:0		Mvid7:0		
Maud7:0		Maud7:0		Maud7:0		Maud7:0		

a. *R0-9:2 = red bits 9:2 of pixel, G = green, B = blue, BS = blanking start, BE = blanking end. VB-ID = video blanking ID. Mvid7:0, and Maud7:0 are portions of the time stamps for video and audio stream clocks.*
b. *Tan-shaded symbols and partial symbols indicate zero-padding.*

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The following sections describe how the data types listed below map into 4-, 2-, and 1-lane Main-Links:

- 8, 6, 10, 12, and 16bpc RGB pixels,
- 8, 10, 12, and 16bpc YCbCr4:4:4/4:2:2/4:2:0/Y-only, and
- 6, 7, 8, 10, 12, 14, and 16bpp RAW data

As can be seen in Table 2-8 through Table 2-34, when only one lane is enabled of either a 2- or 4-lane DP device, Lane 0 must be enabled. When only two lanes are enabled, Lanes 0 and 1 must be enabled.

2.2.1.3.1 8bpc RGB/YCbCr 4:4:4 (24 bits per pixel)

Table 2-8 through Table 2-10 show 8bpc RGB/YCbCr 4:4:4 stream mapping into a 4-, 2-, or 1-lane Main-Link, respectively. Bit 7 of each color is mapped to bit 7 of each lane, while bit 0 of each color is mapped to bit 0 of each lane. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-8: 8bpc RGB to a 4-Lane Main-Link Mapping

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

Table 2-9: 8bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-7:0	R1-7:0
G0-7:0	G1-7:0
B0-7:0	B1-7:0
R2-7:0	R3-7:0
G2-7:0	G3-7:0
B2-7:0	B3-7:0
R4-7:0	R5-7:0
G4-7:0	G5-7:0
B4-7:0	B5-7:0

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Table 2-10: 8bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-7:0
G0-7:0
B0-7:0
R1-7:0
G1-7:0
B1-7:0

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2.2.1.3.2 6bpc RGB (18 bits per pixel)

Table 2-11 through Table 2-13 show 6bpc RGB stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. Bit 5 of R0 is mapped to bit 7 of Lane 0 while bit 4 of G0 is mapped to bit 0 of Lane 0.

Table 2-11: 6bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-5:0 | G0-5:4	R1-5:0 | G1-5:4	R2-5:0 | G2-5:4	R3-5:0 | G3-5:4
G0-3:0 | B0-5:2	G1-3:0 | B1-5:2	G2-3:0 | B2-5:2	G3-3:0 | B3-5:2
B0-1:0 | R4-5:0	B1-1:0 | R5-5:0	B2-1:0 | R6-5:0	B3-1:0 | R7-5:0
G4-5:0 | B4-5:4	G5-5:0 | B5-5:4	G6-5:0 | B6-5:4	G7-5:0 | B7-5:4
B4-3:0 | R8-5:2	B5-3:0 | R9-5:2	B6-3:0 | R10-5:2	B7-3:0 | R11-5:2
R8-1:0 | G8-5:0	R9-1:0 | G9-5:0	R10-1:0 | G10-5:0	R11-1:0 | G11-5:0
B8-5:0 | R12-5:4	B9-5:0 | R13-5:4	B10-5:0 | R14-5:4	B11-5:0 | R15-5:4
R12-3:0 | G12-5:2	R13-3:0 | G13-5:2	R14-3:0 | G14-5:2	R15-3:0 | G15-5:2
G12-1:0 | B12-5:0	G13-1:0 | B13-5:0	G14-1:0 | B14-5:0	G15-1:0 | B15-5:0

Table 2-12: 6bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-5:0 | G0-5:4	R1-5:0 | G1-5:4
G0-3:0 | B0-5:2	G1-3:0 | B1-5:2
B0-1:0 | R2-5:0	B1-1:0 | R3-5:0
G2-5:0 | B2-5:4	G3-5:0 | B3-5:4
B2-3:0 | R4-5:2	B3-3:0 | R5-5:2
R4-1:0 | G4-5:0	R5-1:0 | G5-5:0
B4-5:0 | R6-5:4	B5-5:0 | R7-5:4
R6-3:0 | G6-5:2	R7-3:0 | G7-5:2
G6-1:0 | B6-5:0	G7-1:0 | B7-5:0

Table 2-13: 6bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-5:0 | G0-5:4
G0-3:0 | B0-5:2
B0-1:0 | R1-5:0
G1-5:0 | B1-5:4
B1-3:0 | R2-5:2

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2.2.1.3.3 10bpc RGB/YCbCr 4:4:4 (30 bits per pixel)

Table 2-14 through Table 2-16 show 10bpc RGB/YCbCr 4:4:4 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-14: 10bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0 | G0-9:4	R1-1:0 | G1-9:4	R2-1:0 | G2-9:4	R3-1:0 | G3-9:4
G0-3:0 | B0-9:6	G1-3:0 | B1-9:6	G2-3:0 | B2-9:6	G3-3:0 | B3-9:6
B0-5:0 | R4-9:8	B1-5:0 | R5-9:8	B2-5:0 | R6-9:8	B3-5:0 | R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0 | B4-9:4	G5-1:0 | B5-9:4	G6-1:0 | B6-9:4	G7-1:0 | B7-9:4
B4-3:0 | R8-9:6	B5-3:0 | R9-9:6	B6-3:0 | R10-9:6	B7-3:0 | R11-9:6
R8-5:0 | G8-9:8	R9-5:0 | G9-9:8	R10-5:0 | G10-9:8	R11-5:0 | G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0 | R12-9:4	B9-1:0 | R13-9:4	B10-1:0 | R14-9:4	B11-1:0 | R15-9:4
R12-3:0 | G12-9:6	R13-3:0 | G13-9:6	R14-3:0 | G14-9:6	R15-3:0 | G15-9:6
G12-5:0 | B12-9:8	G13-5:0 | B13-9:8	G14-5:0 | B14-9:8	G15-5:0 | B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0

Table 2-15: 10bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-9:2	R1-9:2
R0-1:0 | G0-9:4	R1-1:0 | G1-9:4
G0-3:0 | B0-9:6	G1-3:0 | B1-9:6
B0-5:0 | R2-9:8	B1-5:0 | R3-9:8
R2-7:0	R3-7:0
G2-9:2	G3-9:2
G2-1:0 | B2-9:4	G3-1:0 | B3-9:4
B2-3:0 | R4-9:6	B3-3:0 | R5-9:6
R4-5:0 | G4-9:8	R5-5:0 | G5-9:8
G4-7:0	G5-7:0
B4-9:2	B5-9:2
B4-1:0 | R6-9:4	B5-1:0 | R7-9:4
R6-3:0 | G6-9:6	R7-3:0 | G7-9:6
G6-5:0 | B6-9:8	G7-5:0 | B7-9:8
B6-7:0	B7-7:0

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Table 2-16: 10bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-9:2
R0-1:0 | G0-9:4
G0-3:0 | B0-9:6
B0-5:0 | R1-9:8
R1-7:0
G1-9:2
G1-1:0 | B1-9:4
B1-3:0 | R2-9:6

2.2.1.3.4 12bpc RGB/YCbCr 4:4:4 (36 bits per pixel)

Table 2-17 through Table 2-19 show 12bpc RGB/YCbCr 4:4:4 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-17: 12bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-11:4	R1-11:4	R2-11:4	R3-11:4
R0-3:0 | G0-11:8	R1-3:0 | G1-11:8	R2-3:0 | G2-11:8	R3-3:0 | G3-11:8
G0-7:0	G1-7:0	G2-7:0	G3-7:0 |
B0-11:4	B1-11:4	B2-11:4	B3-11:4
B0-3:0 | R4-11:8	B1-3:0 | R5-11:8	B2-3:0 | R6-11:8	B3-3:0 | R7-11:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-11:4	G5-11:4	G6-11:4	G7-11:4
G4-3:0 | B4-11:8	G5-3:0 | B5-11:8	G6-3:0 | B6-11:8	G7-3:0 | B7-11:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

Table 2-18: 12bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-11:4	R1-11:4
R0-3:0 | G0-11:8	R1-3:0 | G1-11:8
G0-7:0	G1-7:0
B0-11:4	B1-11:4
B0-3:0 | R2-11:8	B1-3:0 | R3-11:8
R2-7:0	R3-7:0
G2-11:4	G3-11:4
G2-3:0 | B2-11:8	G3-3:0 | B3-11:8
B2-7:0	B3-7:0

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Table 2-19: 12bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-11:4
R0-3:0 | G0-11:8
G0-7:0
B0-11:4
B0-3:0 | R1-11:8

2.2.1.3.5 16bpc RGB/YCbCr 4:4:4 (48 bits per pixel)

Table 2-20 through Table 2-22 show 16bpc RGB/YCbCr 4:4:4 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-20: 16bpc RGB Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-15:8	R1-15:8	R2-15:8	R3-15:8
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-15:8	G1-15:8	G2-15:8	G3-15:8
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-15:8	B1-15:8	B2-15:8	B3-15:8
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-15:8	R5-15:8	R6-15:8	R7-15:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-15:8	G5-15:8	G6-15:8	G7-15:8
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-15:8	B5-15:8	B6-15:8	B7-15:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

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Table 2-21: 16bpc RGB Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
R0-15:8	R1-15:8
R0-7:0	R1-7:0
G0-15:8	G1-15:8
G0-7:0	G1-7:0
B0-15:8	B1-15:8
B0-7:0	B1-7:0
R2-15:8	R3-15:8
R2-7:0	R3-7:0
G2-15:8	G3-15:8
G2-7:0	G3-7:0
B2-15:8	B3-15:8
B2-7:0	B3-7:0

Table 2-22: 16bpc RGB Mapping to a 1-Lane Main-Link

Lane 0
R0-15:8
R0-7:0
G0-15:8
G0-7:0
B0-15:8
B0-7:0

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2.2.1.3.6 8bpc YCbCr 4:2:2 (16 bits per pixel)

Table 2-23 through Table 2-25 show 8bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-23: 8bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr2-7:0
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0	Cb10-7:0	Cr10-7:0
Y8-7:0	Y9-7:0	Y10-7:0	Y11-7:0

Table 2-24: 8bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-7:0	Cr0-7:0
Y0-7:0	Y1-7:0
Cb2-7:0	Cr2-7:0
Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0
Y4-7:0	Y5-7:0
Cb6-7:0	Cr6-7:0
Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0
Y8-7:0	Y9-7:0
Cb10-7:0	Cr10-7:0
Y10-7:0	Y11-7:0

Table 2-25: 8bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-7:0
Y0-7:0
Cr0-7:0
Y1-7:0
Cb2-7:0
Y2-7:0

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2.2.1.3.7 10bpc YCbCr 4:2:2 (20 bits per pixel)

Table 2-26 through Table 2-28 show 10bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-26: 10bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-9:2	Cr0-9:2	Cb2-9:2	Cb2-9:2
Cb0-1:0 | Y0-9:4	Cr0-1:0 | Y1-9:4	Cb2-1:0 | Y2-9:4	Cb2-1:0 | Y3-9:4
Y0-3:0 | Cb4-9:6	Y1-3:0 | Cr4-9:6	Y2-3:0 | Cb6-9:6	Y3-3:0 | Cr6-9:6
Cb4-5:0 | Y4-9:8	Cr4-5:0 | Y5-9:8	Cb6-5:0 | Y6-9:8	Cr6-5:0 | Y7-9:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-9:2	Cr8-9:2	Cb10-9:2	Cr10-9:2
Cb8-1:0 | Y8-9:4	Cr8-1:0 | Y9-9:4	Cb10-1:0 | Y10-9:4	Cr10-1:0 | Y11-9:4
Y8-3:0 | Cb12-9:6	Y9-3:0 | Cr12-9:6	Y10-3:0 | Cb14-9:6	Y11-3:0 | Cr14-9:6
Cb12-5:0 | Y12-9:8	Cr12-5:0 | Y13-9:8	Cb14-5:0 | Y114-9:8	Cr14-5:0 | Y15-9:8
Y12-7:0	Y13-7:0	Y14-7:0	Y15-7:0

Table 2-27: 10bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-9:2	Cr0-9:2
Cb0-1:0 | Y0-9:4	Cr2-1:0 | Y1-9:4
Y0-3:0 | Cb2-9:6	Y1-3:0 | Cr2-9:6
Cb2-5:0 | Y2-9:8	Cr2-5:0 | Y3-9:8
Y2-7:0	Y3-7:0
Cb4-9:2	Cr4-9:2
Cb4-1:0 | Y4-9:4	Cr4-1:0 | Y5-9:4
Y4-3:0 | Cb6-9:6	Y5-3:0 | Cr6-9:6
Cb4-5:0 | Y6-9:8	Cr6-5:0 | Y7-9:8
Y6-7:0	Y7-7:0

Table 2-28: 10bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-9:2
Cb0-1:0 | Y0-9:4
Y0-3:0 | Cr0-9:6
Cr0-5:0 | Y1-9:8
Y1-7:0

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2.2.1.3.8 12bpc YCbCr 4:2:2 (24 bits per pixel)

Table 2-29 through Table 2-31 show 12bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-29: 12bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-11:4	Cr0-11:4	Cb2-11:4	Cr2-11:4
Cb0-3:0 | Y0-11:8	Cr0-3:0 | Y1-11:8	Cb2-3:0 | Y2-11:8	Cr2-3:0 | Y3-11:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-11:4	Cr4-11:4	Cb6-11:4	Cr6-11:4
Cb4-3:0 | Y4-11:8	Cr4-3:0 | Y5-11:8	Cb63:0 | Y6-11:8	Cr6-3:0 | Y7-11:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-30: 12bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-11:4	Cr0-11:4
Cb0-3:0 | Y0-11:8	Cr0-3:0 | Y1-11:8
Y0-7:0	Y1-7:0
Cb2-11:4	Cr2-11:4
Cb2-3:0 | Y2-11:8	Cr2-3:0 | Y3-11:8
Y2-7:0	Y3-7:0

Table 2-31: 12bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-11:4
Cb0-3:0 | Y0-11:8
Y0-7:0

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2.2.1.3.9 16bpc YCbCr 4:2:2 (32 bits per pixel)

Table 2-32 through Table 2-34 show 16bpc YCbCr 4:2:2 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-32: 16bpc YCbCr 4:2:2 Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-15:8	Cr0-15:8	Cb2-15:8	Cr2-15:8
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr2-7:0
Y0-15:8	Y1-15:8	Y2-15:8	Y3-15:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-15:8	Cr4-15:8	Cb6-15:8	Cr6-15:8
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-15:8	Y5-15:8	Y6-15:8	Y7-15:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-33: 16bpc YCbCr 4:2:2 Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Cb0-15:8	Cr0-15:8
Cb0-7:0	Cr0-7:0
Y0-15:8	Y1-15:8
Y0-7:0	Y1-7:0
Cb2-15:8	Cr2-15:8
Cb2-7:0	Cr2-7:0
Y2-15:8	Y3-15:8
Y2-7:0	Y3-7:0

Table 2-34: 16bpc YCbCr 4:2:2 Mapping to a 1-Lane Main-Link

Lane 0
Cb0-15:8
Cb0-7:0
Y0-15:8
Y0-7:0
Cr0-15:8
Cr0-7:0
Y1-15:8
Y1-7:0

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2.2.1.3.10 8bpc YCbCr 4:2:0 (12 bits per pixel)

Table 2-35 through Table 2-40 show 8bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-35: 8bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-7:0	Y0_3-7:0	Y0_5-7:0	Y0_7-7:0
Y0_0-7:0	Y0_2-7:0	Y0_4-7:0	Y0_6-7:0
Cb0_0-7:0	Cb0_2-7:0	Cb0_4-7:0	Cb0_6-7:0
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-7:0	Y0_10-7:0	Y0_12-7:0	Y0_14-7:0
Cb0_8-7:0	Cb0_10-7:0	Cb0_12-7:0	Cb0_14-7:0

Table 2-36: 8bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-7:0	Y1_3-7:0	Y1_5-7:0	Y1_7-7:0
Y1_0-7:0	Y1_2-7:0	Y1_4-7:0	Y1_6-7:0
Cr0_0-7:0	Cr0_2-7:0	Cr0_4-7:0	Cr0_6-7:0
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-7:0	Y1_10-7:0	Y1_12-7:0	Y1_14-7:0
Cr0_8-7:0	Cr0_10-7:0	Cr0_12-7:0	Cr0_14-7:0

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Table 2-37: 8bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-7:0	Y0_3-7:0
Y0_0-7:0	Y0_2-7:0
Cb0_0-7:0	Cb0_2-7:0
Y0_5-7:0	Y0_7-7:0
Y0_4-7:0	Y0_6-7:0
Cb0_4-7:0	Cb0_6-7:0

Table 2-38: 8bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-7:0	Y1_3-7:0
Y1_0-7:0	Y1_2-7:0
Cr0_0-7:0	Cr0_2-7:0
Y1_5-7:0	Y1_7-7:0
Y1_4-7:0	Y1_6-7:0
Cr0_4-7:0	Cr0_6-7:0

Table 2-39: 8bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-7:0
Y0_0-7:0
Cb0_0-7:0
Y0_3-7:0
Y0_2-7:0
Cb0_2-7:0

Table 2-40: 8bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-7:0
Y1_0-7:0
Cr0_0-7:0
Y1_3-7:0
Y1_2-7:0
Cr0_2-7:0

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2.2.1.3.11 10bpc YCbCr 4:2:0 (15 bits per pixel)

Table 2-41 through Table 2-46 show 10bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-41: 10bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-9:2	Y0_3-9:2	Y0_5-9:2	Y0_7-9:2
Y0_1-1:0 | Y0_0-9:4	Y0_3-1:0 | Y0_2-9:4	Y0_5-1:0 | Y0_4-9:4	Y0_7-1:0 | Y0_6-9:4
Y0_0-3:0 | Cb0_0-9:6	Y0_2-3:0 | Cb0_2-9:6	Y0_4-3:0 | Cb0_4-9:6	Y0_6-3:0 | Cb0_6-9:6
Cb0_0-5:0 | Y0_9-9:8	Cb0_2-5:0 | Y0_11-9:8	Cb0_4-5:0 | Y0_13-9:8	Cb0_6-5:0 | Y0_15-9:8
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-9:2	Y0_10-9:2	Y0_12-9:2	Y0_14-9:2
Y0_8-1:0 | Cb0_8-9:4	Y0_10-1:0 | Cb0_10-9:4	Y0_12-1:0 | Cb0_12-9:4	Y0_14-1:0 | Cb0_14-9:4
Cb0_8-3:0 | Y0_17-9:6	Cb0_10-3:0 | Y0_19-9:6	Cb0_12-3:0 | Y0_21-9:6	Cb0_14-3:0 | Y0_23-9:6
Y0_17-5:0 | Y0_16-9:8	Y0_19-5:0 | Y0_18-9:8	Y0_21-5:0 | Y0_20-9:8	Y0_23-5:0 | Y0_22-9:8
Y0_16-7:0	Y0_18-7:0	Y0_20-7:0	Y0_22-7:0

Table 2-42: 10bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-9:2	Y1_3-9:2	Y1_5-9:2	Y1_7-9:2
Y1_1-1:0 | Y1_0-9:4	Y1_3-1:0 | Y1_2-9:4	Y1_5-1:0 | Y1_4-9:4	Y1_7-1:0 | Y1_6-9:4
Y1_0-3:0 | Cr0_0-9:6	Y1_2-3:0 | Cr0_2-9:6	Y1_4-3:0 | Cr0_4-9:6	Y1_6-3:0 | Cr0_6-9:6
Cr0_0-5:0 | Y1_9-9:8	Cr0_2-5:0 | Y1_11-9:8	Cr0_4-5:0 | Y1_13-9:8	Cr0_6-5:0 | Y1_15-9:8
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-9:2	Y1_10-9:2	Y1_12-9:2	Y1_14-9:2
Y1_8-1:0 | Cr0_8-9:4	Y1_10-1:0 | Cr0_10-9:4	Y1_12-1:0 | Cr0_12-9:4	Y1_14-1:0 | Cr0_14-9:4
Cr0_8-3:0 | Y1_17-9:6	Cr0_10-3:0 | Y1_19-9:6	Cr0_12-3:0 | Y1_21-9:6	Cr0_14-3:0 | Y1_23-9:6
Y1_17-5:0 | Y1_16-9:8	Y1_19-5:0 | Y1_18-9:8	Y1_21-5:0 | Y1_20-9:8	Y1_23-5:0 | Y1_22-9:8
Y1_16-7:0	Y1_18-7:0	Y1_20-7:0	Y1_22-7:0

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Table 2-43: 10bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-9:2	Y0_3-9:2
Y0_1-1:0 | Y0_0-9:4	Y0_3-1:0 | Y0_2-9:4
Y0_0-3:0 | Cb0_0-9:6	Y0_2-3:0 | Cb0_2-9:6
Cb0_0-5:0 | Y0_5-9:8	Cb0_2-5:0 | Y0_7-9:8
Y0_5-7:0	Y0_7-7:0
Y0_4-9:2	Y0_6-9:2
Y0_4-1:0 | Cb0_4-9:4	Y0_6-1:0 | Cb0_6-9:4
Cb0_4-3:0 | Y0_9-9:6	Cb0_6-3:0 | Y0_11-9:6
Y0_9-5:0 | Y0_8-9:8	Y0_11-5:0 | Y0_10-9:8
Y0_8-7:0	Y0_10-7:0

Table 2-44: 10bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-9:2	Y1_3-9:2
Y1_1-1:0 | Y1_0-9:4	Y1_3-1:0 | Y1_2-9:4
Y1_0-3:0 | Cr0_0-9:6	Y1_2-3:0 | Cr0_2-9:6
Cr0_0-5:0 | Y1_5-9:8	Cr0_2-5:0 | Y1_7-9:8
Y1_5-7:0	Y1_7-7:0
Y1_4-9:2	Y1_6-9:2
Y1_4-1:0 | Cr0_4-9:4	Y1_6-1:0 | Cr0_6-9:4
Cr0_4-3:0 | Y1_9-9:6	Cr0_6-3:0 | Y1_11-9:6
Y1_9-5:0 | Y1_8-9:8	Y1_11-5:0 | Y1_10-9:8
Y1_8-7:0	Y1_10-7:0

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Table 2-45: 10bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-9:2
Y0_1-1:0 | Y0_0-9:4
Y0_0-3:0 | Cb0_0-9:6
Cb0_0-5:0 | Y0_3-9:8
Y0_3-7:0
Y0_2-9:2
Y0_2-1:0 | Cb0_2-9:4
Cb0_2-3:0 | Y0_5-9:6
Y0_5-5:0 | Y0_4-9:8
Y0_4-7:0

Table 2-46: 10bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-9:2
Y1_1-1:0 | Y1_0-9:4
Y1_0-3:0 | Cr0_0-9:6
Cr0_0-5:0 | Y1_3-9:8
Y1_3-7:0
Y1_2-9:2
Y1_2-1:0 | Cr0_2-9:4
Cr0_2-3:0 | Y1_5-9:6
Y1_5-5:0 | Y1_4-9:8
Y1_4-7:0

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2.2.1.3.12 12bpc YCbCr 4:2:0 (18 bits per pixel)

Table 2-47 through Table 2-52 show 12bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-47: 12bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-11:4	Y0_3-11:4	Y0_5-11:4	Y0_7-11:4
Y0_1-3:0 | Y0_0-11:8	Y0_3-3:0 | Y0_2-11:8	Y0_5-3:0 | Y0_4-11:8	Y0_7-3:0 | Y0_6-11:8
Y0_0-7:0	Y0_2-7:0	Y0_4-7:0	Y0_6-7:0
Cb0_0-11:4	Cb0_2-11:4	Cb0_4-11:4	Cb0_6-11:4
Cb0_0-3:0 | Y0_9-11:8	Cb0_2-3:0 | Y0_11-11:8	Cb0_4-3:0 | Y0_13-11:8	Cb0_6-3:0 | Y0_15-11:8
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-11:4	Y0_10-11:4	Y0_12-11:4	Y0_14-11:4
Y0_8-3:0 | Cb0_8-11:8	Y0_10-3:0 | Cb0_10-11:8	Y0_12-3:0 | Cb0_12-11:8	Y0_14-3:0 | Cb0_14-11:8
Cb0_8-7:0	Cb0_10-7:0	Cb0_12-7:0	Cb0_14-7:0

Table 2-48: 12bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-11:4	Y1_3-11:4	Y1_5-11:4	Y1_7-11:4
Y1_1-3:0 | Y1_0-11:8	Y1_3-3:0 | Y1_2-11:8	Y1_5-3:0 | Y1_4-11:8	Y1_7-3:0 | Y1_6-11:8
Y1_0-7:0	Y1_2-7:0	Y1_4-7:0	Y1_6-7:0
Cr0_0-11:4	Cr0_2-11:4	Cr0_4-11:4	Cr0_6-11:4
Cr0_0-3:0 | Y1_9-11:8	Cr0_2-3:0 | Y1_11-11:8	Cr0_4-3:0 | Y1_13-11:8	Cr0_6-3:0 | Y1_15-11:8
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-11:4	Y1_10-11:4	Y1_12-11:4	Y1_14-11:4
Y1_8-3:0 | Cr0_8-11:8	Y1_10-3:0 | Cr0_10-11:8	Y1_12-3:0 | Cr0_12-11:8	Y1_14-3:0 | Cr0_14-11:8
Cr0_8-7:0	Cr0_10-7:0	Cr0_12-7:0	Cr0_14-7:0

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Table 2-49: 12bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-11:4	Y0_3-11:4
Y0_1-3:0 | Y0_0-11:8	Y0_3-3:0 | Y0_2-11:8
Y0_0-7:0	Y0_2-7:0
Cb0_0-11:4	Cb0_2-11:4
Cb0_0-3:0 | Y0_5-11:8	Cb0_2-3:0 | Y0_7-11:8
Y0_5-7:0	Y0_7-7:0
Y0_4-11:4	Y0_6-11:4
Y0_4-3:0 | Cb0_4-11:8	Y0_6-3:0 | Cb0_6-11:8
Cb0_4-7:0	Cb0_6-7:0

Table 2-50: 12bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-11:4	Y1_3-11:4
Y1_1-3:0 | Y1_0-11:8	Y1_3-3:0 | Y1_2-11:8
Y1_0-7:0	Y1_2-7:0
Cr0_0-11:4	Cr0_2-11:4
Cr0_0-3:0 | Y1_5-11:8	Cr0_2-3:0 | Y1_7-11:8
Y1_5-7:0	Y1_7-7:0
Y1_4-11:4	Y1_6-11:4
Y1_4-3:0 | Cr0_4-11:8	Y1_6-3:0 | Cr0_6-11:8
Cr0_4-7:0	Cr0_6-7:0

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Table 2-51: 12bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-11:4
Y0_1-3:0 | Y0_0-11:8
Y0_0-7:0
Cb0_0-11:4
Cb0_0-3:0 | Y0_3-11:8
Y0_3-7:0
Y0_2-11:4
Y0_2-3:0 | Cb0_2-11:8
Cb0_2-7:0

Table 2-52: 12bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-11:4
Y1_1-3:0 | Y1_0-11:8
Y1_0-7:0
Cr0_0-11:4
Cr0_0-3:0 | Y1_3-11:8
Y1_3-7:0
Y1_2-11:4
Y1_2-3:0 | Cr0_2-11:8
Cr0_2-7:0

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2.2.1.3.13 16bpc YCbCr 4:2:0 (24 bits per pixel)

Table 2-53 through Table 2-58 show 16bpc YCbCr 4:2:0 stream mapping into 4-, 2-, and 1-lane Main-Links, respectively (two tables per each lane count, one for even lines, and one for odd lines). Y0_1 means Luminance (Y) of Pixel 1 of Line 0.

Table 2-53: 16bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y0_1-15:8	Y0_3-15:8	Y0_5-15:8	Y0_7-15:8
Y0_1-7:0	Y0_3-7:0	Y0_5-7:0	Y0_7-7:0
Y0_0-15:8	Y0_2-15:8	Y0_4-15:8	Y0_6-15:8
Y0_0-7:0	Y0_2-7:0	Y0_4-7:0	Y0_6-7:0
Cb0_0-15:8	Cb0_2-15:8	Cb0_4-15:8	Cb0_6-15:8
Cb0_0-7:0	Cb0_2-7:0	Cb0_4-7:0	Cb0_6-7:0
Y0_9-15:8	Y0_11-15:8	Y0_13-15:8	Y0_15-15:8
Y0_9-7:0	Y0_11-7:0	Y0_13-7:0	Y0_15-7:0
Y0_8-15:8	Y0_10-15:8	Y0_12-15:8	Y0_14-15:8
Y0_8-7:0	Y0_10-7:0	Y0_12-7:0	Y0_14-7:0
Cb0_8-15:8	Cb0_10-15:8	Cb0_12-15:8	Cb0_14-15:8
Cb0_8-7:0	Cb0_10-7:0	Cb0_12-7:0	Cb0_14-7:0

Table 2-54: 16bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Four Main-Link Lanes

Lane 0	Lane 1	Lane 2	Lane 3
Y1_1-15:8	Y1_3-15:8	Y1_5-15:8	Y1_7-15:8
Y1_1-7:0	Y1_3-7:0	Y1_5-7:0	Y1_7-7:0
Y1_0-15:8	Y1_2-15:8	Y1_4-15:8	Y1_6-15:8
Y1_0-7:0	Y1_2-7:0	Y1_4-7:0	Y1_6-7:0
Cr0_0-15:8	Cr0_2-15:8	Cr0_4-15:8	Cr0_6-15:8
Cr0_0-7:0	Cr0_2-7:0	Cr0_4-7:0	Cr0_6-7:0
Y1_9-15:8	Y1_11-15:8	Y1_13-15:8	Y1_15-15:8
Y1_9-7:0	Y1_11-7:0	Y1_13-7:0	Y1_15-7:0
Y1_8-15:8	Y1_10-15:8	Y1_12-15:8	Y1_14-15:8
Y1_8-7:0	Y1_10-7:0	Y1_12-7:0	Y1_14-7:0
Cr0_8-15:8	Cr0_10-15:8	Cr0_12-15:8	Cr0_14-15:8
Cr0_8-7:0	Cr0_10-7:0	Cr0_12-7:0	Cr0_14-7:0

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Table 2-55: 16bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y0_1-15:8	Y0_3-15:8
Y0_1-7:0	Y0_3-7:0
Y0_0-15:8	Y0_2-15:8
Y0_0-7:0	Y0_2-7:0
Cb0_0-15:8	Cb0_2-15:8
Cb0_0-7:0	Cb0_2-7:0
Y0_5-15:8	Y0_7-15:8
Y0_5-7:0	Y0_7-7:0
Y0_4-15:8	Y0_6-15:8
Y0_4-7:0	Y0_6-7:0
Cb0_4-15:8	Cb0_6-15:8
Cb0_4-7:0	Cb0_6-7:0

Table 2-56: 16bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over Two Main-Link Lanes

Lane 0	Lane 1
Y1_1-15:8	Y1_3-15:8
Y1_1-7:0	Y1_3-7:0
Y1_0-15:8	Y1_2-15:8
Y1_0-7:0	Y1_2-7:0
Cr0_0-15:8	Cr0_2-15:8
Cr0_0-7:0	Cr0_2-7:0
Y1_5-15:8	Y1_7-15:8
Y1_5-7:0	Y1_7-7:0
Y1_4-15:8	Y1_6-15:8
Y1_4-7:0	Y1_6-7:0
Cr0_4-15:8	Cr0_6-15:8
Cr0_4-7:0	Cr0_6-7:0

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Table 2-57: 16bpc YCbCr 4:2:0 Even Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y0_1-15:8
Y0_1-7:0
Y0_0-15:8
Y0_0-7:0
Cb0_0-15:8
Cb0_0-7:0
Y0_3-15:8
Y0_3-7:0
Y0_2-15:8
Y0_2-7:0
Cb0_2-15:8
Cb0_2-7:0

Table 2-58: 16bpc YCbCr 4:2:0 Odd Lines (Starting with Line 0) over One Main-Link Lane

Lane 0
Y1_1-15:8
Y1_1-7:0
Y1_0-15:8
Y1_0-7:0
Cr0_0-15:8
Cr0_0-7:0
Y1_3-15:8
Y1_3-7:0
Y1_2-15:8
Y1_2-7:0
Cr0_2-15:8
Cr0_2-7:0

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2.2.1.3.14 8bpp Y-only

Table 2-59 through Table 2-61 show 8bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively. Bit 7 of each color is mapped to bit 7 of each lane, while bit 0 of each color is mapped to bit 0 of each lane.

Table 2-59: 8bpp Y-only to a 4-Lane Main-Link Mapping

Lane 0	Lane 1	Lane 2	Lane 3
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-60: 8bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-7:0	Y1-7:0
Y2-7:0	Y3-7:0
Y4-7:0	Y5-7:0
Y6-7:0	Y7-7:0

Table 2-61: 8bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-7:0
Y1-7:0
Y2-7:0
Y3-7:0

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2.2.1.3.15 10bpp Y-only

Table 2-62 through Table 2-64 show 10bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-62: 10bpp Y-only Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Y0-9:2	Y1-9:2	Y2-9:2	Y3-9:2
Y0-1:0 | Y4-9:4	Y1-1:0 | Y5-9:4	Y2-1:0 | Y6-9:4	Y3-1:0 | Y7-9:4
Y4-3:0 | Y8-9:6	Y5-3:0 | Y9-9:6	Y6-3:0 | Y10-9:6	Y7-3:0 | Y11-9:6
Y8-5:0 | Y12-9:8	Y9-5:0 | Y13-9:8	Y10-5:0 | Y14-9:8	Y11-5:0 | Y15-9:8
Y12-7:0	Y13-7:0	Y14-7:0	Y15-7:0

Table 2-63: 10bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-9:2	Y1-9:2
Y0-1:0 | Y2-9:4	Y1-1:0 | Y3-9:4
Y2-3:0 | Y4-9:6	Y3-3:0 | Y5-9:6
Y4-5:0 | Y6-9:8	Y5-5:0 | Y7-9:8
Y6-7:0	Y7-7:0

Table 2-64: 10bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-9:2
Y0-1:0 | Y1-9:4
Y1-3:0 | Y2-9:6
Y2-5:0 | Y3-9:8
Y3-7:0

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2.2.1.3.16 12bpp Y-only

Table 2-65 through Table 2-67 show 12bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-65: 12bpp Y-only Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Y0-11:4	Y1-11:4	Y2-11:4	Y3-11:4
Y0-3:0 | Y4-11:8	Y1-3:0 | Y5-11:8	Y2-3:0 | Y6-11:8	Y3-3:0 | Y7-11:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0 |

Table 2-66: 12bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-11:4	Y1-11:4
Y0-3:0 | Y2-11:8	Y1-3:0 | Y3-11:8
Y2-7:0	Y3-7:0

Table 2-67: 12bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-11:4
Y0-3:0 | Y1-11:8
Y1-7:0

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2.2.1.3.17 16bpp Y-only

Table 2-68 through Table 2-70 show 16bpp Y-only stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-68: 16bpp Y-only Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
Y0-15:8	Y1-15:8	Y2-15:8	Y3-15:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Y4-15:8	Y5-15:8	Y6-15:8	Y7-15:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-69: 16bpp Y-only Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
Y0-15:8	Y1-15:8
Y0-7:0	Y1-7:0
Y2-15:8	Y3-15:8
Y2-7:0	Y3-7:0

Table 2-70: 16bpp Y-only Mapping to a 1-Lane Main-Link

Lane 0
Y0-15:8
Y0-7:0
Y1-15:8
Y1-7:0

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2.2.1.3.18 6bpp RAW

Table 2-71 through Table 2-73 show 6bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-71: 6bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-5:0 | RAW4-5:4	RAW1-5:0 | RAW5-5:4	RAW2-5:0 | RAW6-5:4	RAW3-5:0 | RAW7-5:4
RAW4-3:0 | RAW8-5:2	RAW5-3:0 | RAW9-5:2	RAW6-3:0 | RAW10-5:2	RAW7-3:0 | RAW11-5:2
RAW8-1:0 | RAW12-5:0	RAW9-1:0 | RAW13-5:0	RAW10-1:0 | RAW14-5:0	RAW11-1:0 | RAW15-5:0

Table 2-72: 6bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-5:0| RAW2-5:4	RAW1-5:0| RAW3-5:4
RAW2-3:0 | RAW4-5:2	RAW3-3:0 | RAW5-5:2
RAW4-1:0 | RAW6-5:0	RAW5-1:0 | RAW7-5:0

Table 2-73: 6bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-5:0 | RAW1-5:4
RAW1-3:0 | RAW2-5:2
RAW2-1:0 | RAW3-5:0

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2.2.1.3.19 7bpp RAW

Table 2-74 through Table 2-76 show 7bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-74: 7bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-6:0 | RAW4-6	RAW1-6:0 | RAW5-6	RAW2-6:0 | RAW6-6	RAW3-6:0 | RAW7-6
RAW4-5:0 | RAW8-6:5	RAW5-5:0 | RAW9-6:5	RAW6-5:0 | RAW10-6:5	RAW7-5:0 | RAW11-6:5
RAW8-4:0 | RAW12-6:4	RAW9-4:0 | RAW13-6:4	RAW10-4:0 | RAW14-6:4	RAW11-4:0 | RAW15-6:4
RAW12-3:0 | RAW16-6:3	RAW13-3:0 | RAW17-6:3	RAW14-3:0 | RAW18-6:3	RAW15-3:0 | RAW19-6:3
RAW16-2:0 | RAW20-6:2	RAW17-2:0 | RAW21-6:2	RAW18-2:0 | RAW22-6:2	RAW19-2:0 | RAW23-6:2
RAW20-1:0 | RAW24- 6:1	RAW21-1:0 | RAW25- 6:1	RAW22-1:0 | RAW26- 6:1	RAW23-1:0 | RAW27- 6:1
RAW24-0 | RAW28-6:0	RAW25-0 | RAW29-6:0	RAW26-0 | RAW30-6:0	RAW27-0 | RAW31-6:0

Table 2-75: 7bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-6:0 | RAW2-6	RAW1-6:0 | RAW3-6
RAW2-5:0| RAW4-6:5	RAW3-5:0| RAW5-6:5
RAW4-4:0 | RAW6-6:4	RAW5-4:0 | RAW7-6:4
RAW6-3:0 | RAW8-6:3	RAW7-3:0 | RAW9-6:3
RAW8-2:0 | RAW10-6:2	RAW9-2:0 | RAW11-6:2
RAW10-1:0 | RAW12-6:1	RAW11-1:0 | RAW13-6:1
RAW12-0 | RAW14-6:0	RAW13-0 | RAW15-6:0

Table 2-76: 7bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-6:0 | RAW1-6
RAW1-5:0 | RAW2-6:5
RAW2-4:0 | RAW3-6:4
RAW3-3:0 | RAW4-6:3
RAW4-2:0 | RAW5-6:2
RAW5-1:0 | RAW6-6:1
RAW6-0 | RAW7-6:0

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2.2.1.3.20 8bpp RAW

Table 2-77 through Table 2-79 show 8bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-77: 8bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-7:0	RAW1-7:0	RAW2-7:0	RAW3-7:0
RAW4-7:0	RAW5-7:0	RAW6-7:0	RAW7-7:0

Table 2-78: 8bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-7:0	RAW1-7:0
RAW2-7:0	RAW3-7:0
RAW4-7:0	RAW5-7:0
RAW6-7:0	RAW7-7:0

Table 2-79: 8bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-7:0
RAW1-7:0
RAW2-7:0
RAW3-7:0

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2.2.1.3.21 10bpp RAW

Table 2-80 through Table 2-82 show 10bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-80: 10bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-9:2	RAW1-9:2	RAW2-9:2	RAW3-9:2
RAW0-1:0 | RAW4-9:4	RAW1-1:0 | RAW5-9:4	RAW2-1:0 | RAW6-9:4	RAW3-1:0 | RAW7-9:4
RAW4-3:0 | RAW8-9:6	RAW5-3:0 | RAW9-9:6	RAW6-3:0 | RAW10-9:6	RAW7-3:0 | RAW11-9:6
RAW8-5:0 | RAW12-9:8	RAW9-5:0 | RAW13-9:8	RAW10-5:0 | RAW14-9:8	RAW11-5:0 | RAW15-9:8
RAW12-7:0	RAW13-7:0	RAW14-7:0	RAW15-7:0

Table 2-81: 10bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-9:2	RAW1-9:2
RAW0-1:0 | RAW2-9:4	RAW1-1:0 | RAW3-9:4
RAW2-3:0 | RAW4-9:6	RAW3-3:0 | RAW5-9:6
RAW4-5:0 | RAW6-9:8	RAW5-5:0 | RAW7-9:8
RAW6-7:0	RAW7-7:0

Table 2-82: 10bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-9:2
RAW0-1:0 | RAW1-9:4
RAW1-3:0 | RAW2-9:6
RAW2-5:0 | RAW3-9:8
RAW3-7:0

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2.2.1.3.22 12bpp RAW

Table 2-83 through Table 2-85 show 12bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-83: 12bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-11:4	RAW1-11:4	RAW2-11:4	RAW3-11:4
RAW0-3:0 | RAW4-11:8	RAW1-3:0 | RAW5-11:8	RAW2-3:0 | RAW6-11:8	RAW3-3:0 | RAW7-11:8
RAW4-7:0	RAW5-7:0	RAW6-7:0	RAW7-7:0 |

Table 2-84: 12bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-11:4	RAW1-11:4
RAW0-3:0 | RAW2-11:8	RAW1-3:0 | RAW3-11:8
RAW2-7:0	RAW3-7:0

Table 2-85: 12bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-11:4
RAW0-3:0 | RAW1-11:8
RAW1-7:0

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2.2.1.3.23 14bpp RAW

Table 2-86 through Table 2-88 show 14bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-86: 14bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-13:6	RAW1-13:6	RAW2-13:6	RAW3-13:6
RAW0-5:0 | RAW4-13:12	RAW1-5:0 | RAW5-13:12	RAW2-5:0 | RAW6-13:12	RAW3-5:0 | RAW7-13:12
RAW4-11:4	RAW5-11:4	RAW6-11:4	RAW7-11:4
RAW4-3:0 | RAW8-13:10	RAW5-3:0 | RAW9-13:10	RAW6-3:0 | RAW10-13:10	RAW7-3:0 | RAW11-13:10
RAW8-9:2	RAW9-9:2	RAW10-9:2	RAW11-9:2
RAW8-1:0 | RAW12-13:8	RAW9-1:0 | RAW13-13:8	RAW10-1:0 | RAW14-13:8	RAW11-1:0 | RAW15-13:8
RAW12-7:0	RAW13-7:0	RAW14-7:0	RAW15-7:0

Table 2-87: 14bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-13:6	RAW1-13:6
RAW0-5:0 | RAW2-13:12	RAW1-5:0 | RAW3-13:12
RAW2-11:4	RAW3-11:4
RAW2-3:0 | RAW4-13:10	RAW3-3:0 | RAW5-13:10
RAW4-9:2	RAW5-9:2
RAW4-1:0 | RAW6-13:8	RAW5-1:0 | RAW7-13:8
RAW6-7:0	RAW7-7:0

Table 2-88: 14bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-13:6
RAW0-5:0 | RAW1-13:12
RAW1-11:4
RAW1-3:0 | RAW2-13:10
RAW2-9:2
RAW2-1:0 | RAW3-13:8
RAW3-7:0

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2.2.1.3.24 16bpp RAW

Table 2-89 through Table 2-91 show 16bpp RAW stream mapping into 4-, 2-, and 1-lane Main-Links, respectively.

Table 2-89: 16bpp RAW Mapping to a 4-Lane Main-Link

Lane 0	Lane 1	Lane 2	Lane 3
RAW0-15:8	RAW1-15:8	RAW2-15:8	RAW3-15:8
RAW0-7:0	RAW1-7:0	RAW2-7:0	RAW3-7:0
RAW4-15:8	RAW5-15:8	RAW6-15:8	RAW7-15:8
RAW4-7:0	RAW5-7:0	RAW6-7:0	RAW7-7:0

Table 2-90: 16bpp RAW Mapping to a 2-Lane Main-Link

Lane 0	Lane 1
RAW0-15:8	RAW1-15:8
RAW0-7:0	RAW1-7:0
RAW2-15:8	RAW3-15:8
RAW2-7:0	RAW3-7:0

Table 2-91: 16bpp RAW Mapping to a 1-Lane Main-Link

Lane 0
RAW0-15:8
RAW0-7:0
RAW1-15:8
RAW1-7:0

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2.2.1.4 Symbol Stuffing and Transfer Unit

To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the Link Layer must perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) must be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing. The dummy data symbols must be all 00h before scrambling. The dummy data symbols are inserted both between FS and FE, and between BS and BE.

The way symbols are stuffed must be different between active video period and blanking period.

- During the active video period:
  - Stuffing symbols must be framed with control symbols FS and FE within Transfer Unit (TU) as shown in Figure 2-13. (TU is described with an example in Section 2.2.1.4.1.) All symbols between FS and FE must be stuffing dummy data symbols, while all the symbols in the TU before FS must be valid data symbols.
  - FS and FE must be inserted in all lanes in the same LS_Clk cycle.
  - When there is only one symbol to stuff, FE must be used and FS is omitted.
  - Transfer unit size must be 32 to 64 link symbols per lane, except for the last TU of the horizontal line which contains no stuffing symbols (FS/FE) and truncates with the last active pixel of the line.
  - The last TU of a horizontal video line must end with BS and must not end with an FS/FE insertion.
- During the blanking period:
  - All non-control symbols between the first BS of the blanking period and the first BE of the active video period are dummy stuffing data symbols (except for VB-ID, Mvid7:0, and Maud7:0). These dummy data symbols may be substituted with SDPs.

Note: *BS is inserted at the same symbol time during vertical blanking period as during the active video period, as stated in Section 2.2.1.2.*

  - During vertical blanking period, BS is transmitted on each lane followed by VB-ID, Mvid7:0, and Maud7:0. All the rest of the symbols between the BS at the beginning of vertical blanking interval and the BE at the end of the vertical blanking interval are dummy symbols that may be substituted with SDPs.

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Figure 2-13: Transfer Unit

The transfer unit (TU) size must be in the range of 32 to 64 link symbols per lane. The DP Source device must fix the TU size for a given video timing format.

The first pixel data of the horizontal active Display Line, immediately after BE, must be placed as the first valid data symbols of the first TU of a line. The partial pixel data of Pixel 0 must always be placed on Lane 0.

TU may end at a partial pixel boundary. For example, a part of the blue data of a pixel may be transported in one TU while the rest of the blue data for that pixel is transported in the next TU. The ratio of the valid symbol to stuffing symbol is determined by the ratio between the packed data stream rate and the link symbol rate. Depending on the packed stream rate relative to link symbol rate, a certain number of valid symbols will accumulate every "TU-size" link symbol clock cycles. The DPTX within the Source device will transmit those valid symbols over the Main-Link while the next accumulation starts. This process will repeat until the end of a video line is reached, which is marked by the insertion of BS symbol on all the lanes.

Using the above stuffing method, the number of valid data symbols per TU per lane (except for the last TU of a line which may be cut because of the end of active pixel) will be approximated with the following equation:

*# of valid data symbols per lane = packed data rate/link symbol rate * TU size*

The last TU at the end of the horizontal active display period may (or is likely to) have fewer valid data symbols than that obtained from the above equation. The DPRX must discard all the data symbols after BS (except for VB-ID, Mvid7:0, and Maud7:0) as well as those "zero-padded bits" at the end of the horizontal active display period.

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2.2.1.4.1 Transfer Unit Example (Informative)

Table 2-92 shows an example of transfer unit for a 1366x768, 30bpp RGB video stream (Strm_Clk = 80MHz) transported over a 4-lane Main-Link running at 2.7Gbps (or 270 Msymbols per second per lane). The TU size is fixed to 64 link symbols per lane in this example.

The number of valid symbols within the transfer unit is calculated as follows:

Stream: 30bpp, 80MHz → Packed data rate over 4 lanes = 75 Msymbols / second / lane

*Average valid symbols per TU = 75M / 270M * 64 = 17.8*

The number of valid data symbols per TU will naturally alternate, and over time, the average number will come to the appropriate non-integer value calculated from the above equation. As can be seen in Table 2-92, the valid data in a transfer unit may end at non-pixel boundary.

Table 2-92: Transfer Unit of 30bpp RGB Video over 2.7Gbps/Lane Main-Link[a]

Lane 0	Lane 1	Lane 2	Lane 3
BE	BE	BE	BE
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0 | G0-9:4	R1-1:0 | G1-9:4	R2-1:0 | G2-9:4	R3-1:0 | G3-9:4
G0-3:0 | B0-9:6	G1-3:0 | B1-9:6	G2-3:0 | B2-9:6	G3-3:0 | B3-9:6
B0-5:0 | R4-9:8	B1-5:0 | R5-9:8	B2-5:0 | R6-9:8	B3-5:0 | R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0 | B4-9:4	G5-1:0 | B5-9:4	G6-1:0 | B6-9:4	G7-1:0 | B7-9:4
B4-3:0 | R8-9:6	B5-3:0 | R9-9:6	B6-3:0 | R10-9:6	B7-3:0 | R11-9:6
R8-5:0 | G8-9:8	R9-5:0 | G9-9:8	R10-5:0 | G10-9:8	R11-5:0 | G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0 | R12-9:4	B9-1:0 | R13-9:4	B10-1:0 | R14-9:4	B11-1:0 | R15-9:4
R12-3:0 | G12-9:6	R13-3:0 | G13-9:6	R14-3:0 | G14-9:6	R15-3:0 | G15-9:6
G12-5:0 | B12-9:8	G13-5:0 | B13-9:8	G14-5:0 | B14-9:8	G15-5:0 | B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0
R16-9:2	R17-9:2	R18-9:2	R19-9:2
R16-1:0 | G16-9:4	R17-1:0 | G17-9:4	R18-1:0 | G18-9:4	R19-1:0 | G19-9:4
G16-3:0 | B16-9:6	G17-3:0 | B17-9:6	G18-3:0 | B18-9:6	G19-3:0 | B19-9:6
FS	FS	FS	FS
Dummy Data Symbols (44 x 4)			
FE	FE	FE	FE
B16-5:0 | R20-9:8	B17-5:0 | R21-9:8	B18-5:0 | R22-9:8	B19-5:0 | R23-9:8
R20-7:0	R21-7:0	R22-7:0	R23-7:0
----------			

a. The pixel rate in this example is 80Mpixels per sec. The Main-Link bit rate is 2.7Gbps/lane. The first TU of a line is marked by the blue arrow to the right of the table.

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2.2.1.4.2 Transfer Unit Generation with FEC Encoding/Decoding Enabled

New to *DP v1.4*.

When FEC encoding/decoding is enabled (see Section 3.5.1.5), a DPTX Link Layer shall insert FEC parity place holder and parity marker (FEC_PARITY_PH and FEC_PM, respectively) link symbols. The number of FEC_PARITY_PH and FEC_PM link symbols shall be as follows:

- **1-lane configuration**
  - 12 FEC_PARITY_PH link symbols inserted after 500 Link Layer link symbols
  - Every 128th set of 12 FEC_PARITY_PH link symbols followed by an FEC PM link symbol
- **2- and 4-lane configurations**
  - Six FEC_PARITY_PH link symbols inserted after 250 Link Layer link symbols
  - Every 256th set of six FEC_PARITY_PH link symbols followed by an FEC PM link symbol

The resulting FEC overhead is approximately 2.3%.

The transmission of the FEC parity symbols is strictly periodic and is agnostic to Link Layer link symbol transmission.

A DP Source device, when calculating the maximum pixel bandwidth that it can transmit over its DP link, shall take this 2.3% overhead into account.

A DP Source device in SST mode shall be able to evenly distribute the additional valid pixel data symbols across all the TUs for a fully subscribed link in which the peak pixel bandwidth calculated from the pixel rate and pixel bit depth with the 2.3% overhead is equal to the link bandwidth to account for time slots occupied for FEC parity symbol transmission.

In case the link bandwidth is not fully subscribed, a DP Source device in SST mode may have extra valid pixel data symbols that will have accumulated during the time slots of FEC Codes transmission.

A DP Source device in SST mode may not set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 when it is not enabling FEC encoding for the purpose of avoiding the 2.3% FEC overhead. When the DP Source device in SST mode makes that choice, it must set the FEC_READY bit and initiate Link Training before enabling FEC.

2.2.1.5 Main Stream Attribute Packet/SDP Insertion

The dummy stuffing data symbols during the video blanking periods (both vertical and horizontal) may be substituted either with main stream attribute (MSA) data or an SDP. Both must be framed with SS and SE control symbols as shown in Figure 2-14.

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Figure 2-14: Secondary-Data Insertion

SDPs are used, for example, for the following purposes:

- *CEA-861-F* INFOFRAME SDP
- Audio_Stream SDP
- Audio_TimeStamp SDP

Main stream attribute data must be protected via redundancy. The redundancy must be further enhanced via inter-lane skewing, as described in Section 2.2.1.6. SDPs must be protected by ECC (error correcting code) based on Reed Solomon code, as described in Section 2.2.6.

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2.2.1.6 Inter-lane Skewing

After inserting the Main-Link attributes data (and optionally, SDP), the DPTX must insert a skew of two LS_Clk cycles between adjacent lanes. Figure 2-15 shows how the symbols must be transported after this inter-lane skewing. All the symbols, both those transmitted during video display period and those transmitted during video blanking period, are skewed by two LS_Clk periods between adjacent lanes.

Figure 2-15: Inter-Lane Skewing

The purpose of the inter-lane skewing is to increase the immunity of the link against external noise. Without inter-lane skewing an external impulse may, for example, corrupt the Mvid7:0 symbols on all lanes. Inter-lane skewing reduces the possibility of such a corruption.

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2.2.2 Stream Reconstruction in the Sink Device

The stream reconstruction by the Link Layer in the DPRX must be a mirror image of what takes place within the DPTX. Table 2-93 lists the actions that must be taken by the DPRX.

Table 2-93: DPRX Stream Reconstruction Actions within the Sink Device

Action	Description
1 Inter-lane de-skewing	Must remove the two LS_Clk skewing among adjacent lanes inserted by the DPTX.
2 Error correction	All the values of DisplayPort main stream attributes except for time stamp value Mvid must stay constant. Therefore, the DPRX must filter out any intermittent data corruption by comparing with the previous values. As for the time stamp values Mvid/Maud and VB-ID, "majority voting" must be used to determine the value.
3 SDP de-multiplexing	Secondary data must be de-multiplexed using SS and SE as the separator. The DPRX must perform Reed-Solomon (15:13) (RS (15:13)) decoding upon extracting the SDP
4 Symbol un-stuffing	Remove stuffing symbols.
5 Data unpacking	Data unpacking must take place to reconstruct pixel data from data characters transported over the Main-Link. Unpacking is dependent on the pixel data color depth and format (as described in Section 2.2.1.3).
6 Stream clock regeneration	Stream clock regeneration is covered in Section 2.2.3.

2.2.3 Stream Clock Regeneration

This section describes the details of original stream clock regeneration from the stream transported over the Main-Link within the Sink device. The following equations conceptually explain how the stream clock (Strm_Clk) can be derived from the Main-Link Symbol clock (LS_Clk), using Time Stamps Mvid and Nvid:

$$f_Strm_Clk = Mvid / Nvid * f_LS_Clk$$

where:

- f_Strm_Clk = Stream clock frequency
- Mvid = Feedback pulse period / t_Strm_Clk
- Nvid = Reference pulse period / t_LS_Clk
- f_LS_Clk = Main-Link symbol clock frequency

The t_Strm_Clk and t_LS_Clk are the stream clock and the Main-Link Symbol clock periods, respectively. The reference pulse and feedback pulse are shown in Figure 2-16.

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Figure 2-16: Reference Pulse and Feedback Pulse of Stream Clock Regeneration Circuit

The above equation can also be expressed as:

$$Mvid / Nvid = f_Strm_Clk/f_LS_Clk$$

It must be noted that Mvid/Nvid is a ratio determined by the pixel rate (typically expressed in Mpixels/sec) and Main-Link Symbol Clock rate. Therefore, the Mvid and Nvid values are agnostic to either pixel encoding format or component bit depth.

The Mvid and Nvid time stamps must both be 24-bit values.

When the DPTX and stream source share the same reference clock, the Mvid and Nvid time stamp values remain constant. This way of generating Main-Link Symbol clock and stream clock is called Synchronous Clock mode. A DP Source device may select a stream clock frequency that allows for static and relatively small (e.g., 64 or less) Mvid and Nvid values. These choices are implementation-specific.

If the stream clock and Main-Link Symbol clock are asynchronous with each other, the value of Mvid changes over time. This way of generating Main-Link Symbol clock and stream clock is called Asynchronous Clock mode. The value Mvid is bound to change while the value Nvid remains constant. The value of Nvid in this Asynchronous Clock mode must be set to 2^{15} (= 32768) or higher. A value of power of 2 is recommended.

When in Asynchronous Clock mode, the DPTX must measure Mvid using a counter running at the LS_Clk frequency, as shown in Figure 2-17. The full counter value after every [Nvid x LS_Clk cycles] must be transported in the DP MSA packet. The least significant eight bits of Mvid (Mvid7:0) must be transported once per main video stream horizontal period, following BS symbol sequence and VB-ID.

When Mvid7:0 crosses the 8-bit boundary, the entire Mvid23:0 changes. For example, when Mvid23:0 is 000FFFh at one point in time for a given main video stream, the value may turn to 0010000h at another point. The Sink device is responsible for determining the entire Mvid23:0 value, based on the updated Mvid7:0.

In Asynchronous Clock mode, the Sink device must use the received Mvid and Nvid values as a hint for regenerating the pixel clock. The final stream clock regeneration must be realized so that the regenerated video active line and frame timings are in sync with BE framing control symbol reception.

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Figure 2-17: Mvid and Nvid Value Determination Example in Asynchronous Clock Mode in a Source Device

Note 1: *Use of an Nvid value of 32768 does not mandate that the reference pulse period be 32768 * t_LS_Clk, which is roughly 121us for Main-Link at HBR (2.7Gbps/lane). The value of Nvid (which is 32768 or 8000h) and Mvid (which is measured by the counter in the DPTX) may be divided by power of two (or right-shifted) to realize the reference pulse period suited for each implementation.*

The method for right-shifting Mvid depends on the required accuracy and jitter tolerance of each application. The simplest method of rounding up to the nearest integer value (thus, resulting in approximated stream clock regeneration) may be used for certain applications where the regenerated stream timing is gen-locked to the incoming data. Other applications may use a more-elaborate fractional Mvid PLL based approach for increasing the accuracy while maintaining the low jitter.

In some implementations, the value of Mvid may be accumulated multiple times to use even larger Mvid and Nvid values for stream clock regeneration.

How a Sink device uses (or even does not use) Mvid and Nvid values for stream clock regeneration is implementation-specific.

Note 2: *This section covers the stream clock regeneration in SST mode and does not apply to MST mode, unless an MST Source device is directly driving an MST Sink device over a single link, because the Mvid and Nvid generated by a Source device describes the ratio between the Strm_Clk and the LS_Clk of the link that the Source device is driving. In case there are multiple links (using MST Branch devices) between a Source and Sink device, the Sink device must ignore the Mvid and Nvid values. An MST Sink device must be able to regenerate a stream clock without depending on Mvid and Nvid values because the MST Sink device might be plugged into an MST Branch device, not an MST Source device.*

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2.2.3.1 De-spreading of the Regenerated Stream Clock

Support for down-spreading of the link frequency (with modulation frequencies of 30 to 33kHz) to minimize EMI is required for Sink and Branch devices compliant with the DisplayPort Standard. Support for down-spreading by DPTX is an implementation decision and is optional. Note that, to facilitate testing, the MAX_DOWNSPREAD bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 0) may be used by a reference Sink device during compliance testing of devices that have chosen to implement enablement of SSC based on that bit.

For a certain Sink device, such as an audio Sink device, the regenerated stream clock must not have down-spreading. Such Sink devices must perform de-spreading when regenerating the stream clock. The method of de-spreading is implementation-specific.

2.2.3.2 DPRX Stream Clock Regeneration with FEC Encoding/Decoding Enabled

New to *DP v1.4*.

The transmission of the FEC parity symbols is strictly periodic and is agnostic to Link Layer link symbol transmission. With the insertion of FEC_PARITY_PH and FEC_PM link symbols, transmission of a BE and BS symbol sequence relative to the main stream video display enable (DE) rising edge and falling edge can be skewed, as follows:

- **1-lane configuration** – Up to 12 link symbol clock cycles, time-to-time
- **2 and 4-lane configurations** – Up to seven link symbol clock cycles, time-to-time

A DPRX shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations.

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2.2.4 Main Stream Attribute Data Transport

This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as described in Table 2-94. Table 2-94 also lists the DPCD registers associated with these attributes.

Table 2-94: Main Stream Attribute Data Fields

Symbol	# of Bits	Bit #	Description
Mvid	24	23:0	**Mvid** Video time stamp value used by a DP Sink device as a hint for regenerating pixel clock. Used for main video stream clock regeneration. Comprised of three 8-bit bytes: • Mvid23:16 • Mvid15:8 • Mvid7:0
Nvid	24	23:0	**Nvid** Video time stamp value used by a DP Sink device as a hint for regenerating pixel clock. Used for main video stream clock regeneration. Comprised of three 8-bit bytes: • Nvid23:16 • Nvid15:8 • Nvid7:0
HTotal	16	15:0	**Horizontal Total** Horizontal total of transmitted main video stream, measured in pixel count.
VTotal	16	15:0	**Vertical Total** Vertical total of transmitted main video stream, measured in line count.
HStart	16	15:0	**Horizontal Active Start** Horizontal active start from leading edge of Hsync, measured in pixel count.
VStart	16	15:0	**Vertical Active Start** Vertical active start from leading edge of Vsync, measured in line count.
HSyncPolarity (HSP)	1	0	**Horizontal Sync Polarity** Hsync polarity, measured in pixel count. 0 = Active high pulse. Synchronization signal is high for the sync pulse width. 1 = Active low pulse. Synchronization signal is low for the sync pulse width.
HSyncWidth (HSW)	15	14:0	**Horizontal Sync Width** Hsync width, measured in pixel count.

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Table 2-94: Main Stream Attribute Data Fields (Continued)

Symbol	# of Bits	Bit #	Description
VSyncPolarity (VSP)	1	0	**Vertical Sync Polarity** Vsync polarity, measured in line count. 0 = Active high pulse. Synchronization signal is high for the sync pulse width. 1 = Active low pulse. Synchronization signal is low for the sync pulse width.
VSyncWidth (VSW)	15	14:0	**Vertical Sync Width** Vsync width, measured in line count.
HWidth	16	15:0	**Horizontal Active Video Width** Active video width, measured in pixel count.
VWidth	16	15:0	**Vertical Active Video Height** Active video height, measured in line count.
MISC0	8	7:0	**Miscellaneous0**
		0	**Synchronous Clock** Applies to the main video stream clock, and does not apply to the audio clock. (See Section 2.2.5.2.) Synchronousness/asynchronousness of the main video stream and that of the audio stream clock may be independently set. 0 = Link clock and main video stream clock are asynchronous. 1 = Link clock and main video stream clock are synchronous. The value Mvid must be constant, regardless of whether link clock down-spread is enabled.
		7:1	**Colorimetry Indicator Field, Bits 7:1.** Used with MISC1, bit 7:6, to comprise the Colorimetry Indicator field. (See Section 2.2.4.3.)

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Table 2-94: Main Stream Attribute Data Fields (Continued)

Symbol	# of Bits	Bit #	Description
MISC1	8	7:0	**Miscellaneous1**
		0	**Interlaced Vertical Total Even** 0 = Number of lines per interlaced frame (consisting of two fields) is an odd number. 1 = Number of lines per interlaced frame (consisting of two fields) is an even number.
		2:1	**Stereo Video Attribute** 00 = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done used an SDP called Video_Stream_Configuration (VSC) Packet. 01 = For progressive video, the next frame is RIGHT EYE. 10 = RESERVED. 11 = For progressive video, the next frame is LEFT EYE. ***Note:*** *Frame sequential stereoscopic 3D video transport in interlaced video timing format is not supported in this version of the Standard.*
		5:3	**RESERVED** Cleared to 0h.
		7:6	**Pixel Encoding/Colorimetry Format Indicator Field** Bit 6 is new to DP v1.3. Used with MISC0, bits 7:1, to comprise the Colorimetry Indicator field. (See Section 2.2.4.3.) When MISC1, bit 6, is Set to 1, a Source device uses a VSC SDP to indicate the Pixel Encoding/Colorimetry Format and that a Sink device must ignore MISC1, bit 7, and MISC0, bits 7:1 (MISC1, bit 7, and MISC0, bits 7:1, become “don’t care”).

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This MSA data must be transported as shown in Figure 2-18 (after 2-LS_Clk-cycle inter-lane skewing).

Lane 0	Lane 1	Lane 2	Lane 3
SS	SS	SS	SS
SS	SS	SS	SS
Mvid23:16	Mvid23:16	Mvid23:16	Mvid23:16
Mvid15:8	Mvid15:8	Mvid15:8	Mvid15:8
Mvid7:0	Mvid7:0	Mvid7:0	Mvid7:0
Htotal15:8	Hstart15:8	Hwidth15:8	Nvid23:16
Htotal7:0	Hstart7:0	Hwidth7:0	Nvid15:8
Vtotal15:8	Vstart15:8	Vheight15:8	Nvid7:0
Vtotal7:0	Vstart7:0	Vheight7:0	MISC0_7:0
HSP|HSW14:8	VSP|VSW14:8	All 0s	MISC1_7:0
HSW7:0	VSW7:0	All 0s	All 0s
SE	SE	SE	SE

4-lane Main-Link

HSW = Hsync Width
HSP = Hsync Polarity
VSW = Vsync Width
VSP = Vsync Polarity

Lane 0	Lane 1
SS	SS
SS	SS
Mvid23:16	Mvid23:16
Mvid15:8	Mvid15:8
Mvid7:0	Mvid7:0
Htotal15:8	Hstart15:8
Htotal7:0	Hstart7:0
Vtotal15:8	Vstart15:8
Vtotal7:0	Vstart7:0
HSP|HSW14:8	VSP|VSW14:8
HSW7:0	VSW7:0
Mvid23:16	Mvid23:16
Mvid15:8	Mvid15:8
Mvid7:0	Mvid7:0
Hwidth15:8	Nvid23:16
Hwidth7:0	Nvid15:8
Vheight15:8	Nvid7:0
Vheight7:0	MISC0_7:0
All 0s	MISC1_7:0
All 0s	All 0s
SE	SE

2-lane Main-Link

Lane 0
SS
SS
Mvid23:16
Mvid15:8
Mvid7:0
Htotal15:8
Htotal7:0
Vtotal15:8
Vtotal7:0
HSP|HSW14:8
HSW7:0
Mvid23:16
Mvid15:8
Mvid7:0
Hstart15:8
Hstart7:0
Vstart15:8
Vstart7:0
VSP|VSW14:8
VSW7:0
Mvid23:16
Mvid15:8
Mvid7:0
Hwidth15:8
Hwidth7:0
Vheight15:8
Vheight7:0
All 0s
All 0s
Mvid23:16
Mvid15:8
Mvid7:0
Nvid23:16
Nvid15:8
Nvid7:0
MISC0_7:0
MISC1_7:0
All 0s
SE

1-lane Main-Link

Figure 2-18: Transport of DisplayPort Main Stream Attribute

The Main Stream Attributes packet must be distinguished from an SDP by the fact that it starts with two consecutive “SS” symbols per lane.

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2.2.4.1 Main Stream Attribute Secondary-data Packet Generation Options

Entire section rewritten for *DP v1.4*.

2.2.4.1.1 Ignore MSA Video Timing Parameters (Ignore MSA) Option

MSA SDP video timing information is designed for video modes in which the parameters are static. For modes that dynamically change the video timing, the main stream attribute fields cannot be used. Also, in some systems, Hsync/Vsync may not be used.

Therefore, a Source device that supports a special mode of operation in which one or more MSA parameters are non-static or unused may transmit invalid values for those MSA parameters, as long as the Source device is able to discover that the Sink device supports that special mode of operation.

A Source device shall query a Sink device's ability to ignore MSA video timing parameters (Ignore MSA option) by reading the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) and its ability to support seamless video timing change over a range of timing exposed by EDID and DisplayID. The query must occur before enabling a dynamic video timing change of the incoming video stream without valid MSA video timing parameters for the fields listed in Table 2-95.

Table 2-95: MSA SDP Timing Parameters that Can Be Ignored

HTotal[15:0]	HStart[15:0]	HSyncPolarity[0] (HSP)	HSyncWidth[14:0] (HSW)
VTotal[15:0]	VStart[15:0]	VSyncPolarity[0] (VSP)	VSyncWidth[14:0] (VSW)

2.2.4.1.2 Video Horizontal Blanking Expansion Option

New to *DP v1.4*.

Video Horizontal Blanking Expansion is an operation in which a DPRX regenerates a pixel clock cycle ($t_{_Regen_PixClk}$) that is shorter than the pixel clock of the DP video stream from the DP Source device ($t_{_Src_PixClk}$), while regenerating the same video horizontal period (in time units) and the same horizontal active pixel count (Hwidth parameter in an MSA SDP):

- Video horizontal period, Hperiod = Htotal × $t_{_PixClk}$
- Alternately expressed, Htotal = Hperiod / $t_{_PixClk}$

For DP Source video and DPRX-regenerated video:

- Htotal_Src = Hperiod / $t_{_Src_PixClk}$
- Htotal_Regen = Hperiod / $t_{_Regen_PixClk}$

Because Hperiod is the same and $t_{_Regen_PixClk} < t_{_Src_PixClk}$:

- Htotal_Regen > $Htotal_{_Src}$

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Horizontal blank pixel cycle count, Hblank = Htotal - Hwidth.

Because Hwidth is the same between the DP Source video and DPRX-regenerated video while $Htotal_{_Src}$ is larger than $Htotal_{_Regen}$:

- $Hblank_{_Regen} > Hblank_{_Src}$

Thus, Video Horizontal Blanking Expansion operation results from the reduction of $t_{_Regen_PixClk}$ relative to $t_{_Src_PixClk}$ (which means, in terms of pixel clock frequency, $f_{_Regen_PixClk} > f_{_Src_PixClk}$. Figure 2-19 illustrates the Video Horizontal Blanking Expansion operation.

Figure 2-19: Video Horizontal Blanking Expansion Operation

2.2.4.1.2.1 Enabling Horizontal Blanking Expansion

When plugged to a DPRX capable of Horizontal Blanking Expansion operation, a DP Source device may prompt the DPRX to enable Horizontal Blanking Expansion operation by programming the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) prior to the video transmission that needs to be expanded.

2.2.4.1.2.2 DPRX Horizontal Blanking Expansion Capability Discovery

A DP Source device discovers whether a DPRX operating in SST mode supports DPRX Horizontal Blanking Expansion operation by reading the RECEIVE_PORT0_CAP_1 and RECEIVE_PORT0_CAP_0 registers (DPCD Addresses 00009h and 00008h, respectively).

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2.2.4.1.2.3 Horizontal Blanking Expansion Dependency on Buffer Size (Normative)

The maximum $Htotal_{_Regen}$, $Max_Htotal_{_Regen}$ for a given $Htotal_{_Src}$ is calculated as follows:

- $Max_Htotal_{_Regen} = Htotal_{_Src} \times Hwidth / (Hwidth – [Buffer\ Size\ in\ Pixel\ Count])$

The minimum $Htotal_{_Src}$, $Max_Htotal_{_Src}$ for a given $Htotal_{_Regen}$ is calculated as follows:

- $Min_Htotal_{_Src} = Htotal_{_Regen} \times (Hwidth – [Buffer\ Size\ in\ Pixel\ Count])/Hwidth$

For $Htotal_{_Regen}$ of 4400 pixel clock cycles and Hwidth of 4096 pixels (i.e., a 4Kp60Hz timing as per CEA861 Standard, with the pixel clock frequency of 594MHz), the buffer size of 200 pixels enables the $Min_Htotal_{_Src}$ of 4186 pixel clock cycles. The corresponding DP Source pixel clock frequency, $f_{_Src_PixClk}$, is calculated as follows:

- $f_{_Src_PixClk}$ = 4186 pixel clock cycles / 4400 pixel clock cycles × 594MHz = 566MHz

For pixel bit depth of 30 bpp, the resulting DP Source video pixel bandwidth is:

- Pixel bandwidth in MBps = 566MP/s × 30 bpp = 2122MBps

The above pixel bandwidth fits within the DP link bandwidth of 5.4Gbps/lane over 4 lanes which is 2160MBps (= 540MBps/lane × 4 lanes).

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2.2.4.2 Main Stream Attribute for Interlaced Video Stream

An interlaced video streams frame consists of two fields:

- Top field, which contains the first active line of a frame
- Bottom field, which contains the second active line of a frame

Figure 2-20 shows the video format of an interlaced video stream that has an odd number of lines per frame. Figure 2-21 shows the case with an even number of lines per frame.

Figure 2-20: Interlaced Video Format/Timing for Odd Number of Lines per Frame

Figure 2-21: Interlaced Video Format/Timing for Even Number of Lines per Frame

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When transporting an interlaced video stream, the timing parameters of the top field must always be conveyed in the MSA packet.

As defined in Table 2-6, the Interlace_Flag bit in the VB-ID (bit 2) must be set to 1 when an interlaced video stream is transported. The FieldID_Flag bit in the VB-ID (bit 1) is cleared to 0 right after the last active line of the top field and to 1 right after the last active line of the bottom field. For non-interlaced video, VB-ID bits 2:1 must remain 00.

In the example shown in Figure 2-20, the Vertical Active Start, Vertical Total, Vertical Sync Width, and Vertical Active Video Height of the MSA packet must be set to:

- Vertical Active Start = 2 (decimal)
- Vertical Total = 12 (decimal)
- Vertical Sync Width = 1 (decimal)
- Vertical Active Video Height = 9 (decimal)

In the example shown in Figure 2-21 the Vertical Active Start, Vertical Total, Vertical Sync Width, and Vertical Active Video Height of the MSA packet must be set to:

- Vertical Active Start = 2 (decimal)
- Vertical Total = 13 (decimal)
- Vertical Sync Width = 1 (decimal)
- Vertical Active Video Height = 9 (decimal)

In addition, MISC1, bit 0, must be set to 1 when the number of lines per frame of the interlaced video stream is an even number.

2.2.4.3 Main Stream Attribute Field for Indication of Color Encoding Format and Content Color Gamut

Table 2-96 shows how MSA MISC0 field, bits 7:1, and MISC1 field, bits 7:6, are used by a DP Source device to indicate the pixel encoding and colorimetry format of the transmitted video stream. A Source device can set the MISC1 field, bit 6, to instruct a Sink device to use a VSC (Video Stream Configuration) SDP, as described in Section 2.2.5.6 instead of the MISC1/MISC0 fields for pixel encoding/colorimetry format indication. For YCbCr420 and BT2020 Colorimetry Formats, VSC SDP must be used The Sink device declares that it can support VSC for colorimetry and pixel encoding formats in the Extended Receiver Capability field (DPCD Addresses 02200h through 022FFh; see Table 2-165).

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Table 2-96: MISC1 and MISC0 Fields for Pixel Encoding/Colorimetry Format Indication[a]

Colorimetry Format	MSA Bits					
	MISC1		MISC0			
	6	7:6	2:1	3	4	7:5[b]
RGB unspecified color space (Legacy RGB mode)	When MISC1, bit 6, is Set to 1, a Source device uses a VSC SDP to indicate the Pixel Encoding/Colorimetry Format and that a Sink device must ignore MISC1, bit 7, and MISC0, bits 7:1 (MISC1, bit 7, and MISC0, bits 7:1, become "don't care").	0	00	0	0	000, 001, 010, 011, 100 (6, 8, 10, 12, 16bpc, respectively)
CEA RGB (sRGB primaries)		0	00	1	0	
RGB wide gamut fixed point (XR8, XR10, XR12)		0	11	0	0	001, 010, 011 (8, 10, 12bpc, respectively)
RGB wide gamut floating point (scRGB)		0	11	0	1	100 (16bpc)
Y-only		1	00	0	0	001, 010, 011, 100 (8, 10, 12, 16 bits/luminance, respectively)
RAW		1	01	0	0	001, 010, 011, 100, 101, 110, 111 (6, 7, 8, 10, 12, 14, 16bpp, respectively) 000 = RESERVED
YCbCr (ITU601/ITU709)		0	01 = 4:2:2 10 = 4:4:4	1	0 = BT601 1 = BT709	001, 010, 011, 100 (8, 10, 12, 16bpc, respectively)
xvYCC (xvYCC601/xvYCC709)		0	01 = 4:2:2 10 = 4:4:4	0	0 = BT601 1 = BT709	
AdobeRGB		0	00	1	1	000, 001, 010, 011, 100 (6, 8, 10, 12, 16bpc RGB, respectively)
DCI-P3		0	11	1	0	011, 100 (12, 16bpc RGB, respectively)
Color Profile[c]		0	11	1	1	000, 001, 010, 011, 100 (8, 10, 12, 16bpc RGB, respectively)

a. All other values are RESERVED.
b. bpc = bits per component.
c. The "Color Profile" to be transported from a DP Source device to DP Sink device as "Simplified Color Profile" VCP code in MCCS Standard.

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2.2.5 SDP Formats

Table 2-97 shows how the SDP is constructed.

Table 2-97: SDP Header

Byte #	Content
HB0	**Secondary-Data Packet ID**
HB1	**Secondary-Data Packet type**
HB2	**Secondary-Data-packet-specific header, Byte 0**
HB3	**Secondary-Data-packet-specific header, Byte 1**

For DisplayPort, the following SDP types are defined as shown in Table 2-98.

Table 2-98: SDP Type

Packet Type Value	Packet Type	Transmission Timing
00h	DisplayPort RESERVED	
01h	Audio_TimeStamp	At least once per video frame
02h	Audio_Stream	During H / V blank period of Main Video stream
03h	DisplayPort RESERVED	
04h	Extension	During H / V blank period of Main Video stream
05h	Audio_CopyManagement	During H / V blank period of Main Video stream
06h	ISRC	During H / V blank period of Main Video stream
07h	Video Stream Configuration (VSC)	During H / V blank period of Main Video stream
08h through 0Fh	Camera Generic 0 through 7	During H / V blank period of Main Video stream
10h	Picture Parameter Set (PPS)	During H / V blank period of Main Video stream
11h through 1Fh	DisplayPort RESERVED	
20h	Video Stream Configuration Extension for VESA (VSC_EXT_VESA)	During H / V blank period of Main Video stream
21h	VSC_EXT_CEA for future CEA INFOFRAME with payload of more than 28 bytes	
22h through 7Fh	DisplayPort RESERVED	
80h + Audio INFOFRAME Type (04h)	*CEA-861-F* Audio INFOFRAME	As per *CEA-861-F* for Audio INFOFRAME
80h + Non-audio INFOFRAME Type	*CEA-861-F* Non-audio INFOFRAME	As per *CEA-861-F* for INFOFRAME, including *CEA-861.3* within which Dynamic Range and Mastering INFOFRAME are defined

If multiple audio streams are being transported simultaneously, the Secondary-Data Packet ID in HB0 must be used to associate the Audio_Stream SDP with its Audio_TimeStamp SDP and *CEA-861-F* Audio INFOFRAME SDP.

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2.2.5.1 INFOFRAME SDP

Figure 2-22 shows an INFOFRAME SDP over the Main-Link. Section 2.2.6 explains the construction of the parity bytes (PBs) that are shown in Figure 2-22. The INFOFRAME SDP shall be used to convey Audio INFOFRAME control information, as specified in *CEA-861-F*. Other INFOFRAME coding types, as specified in *CEA-861-F*, *Table 5*, shall use the VSC_EXT_VESA or VSC_EXT_CEA SDP, as appropriate.

Lane 0	Lane 1	Lane 2	Lane 3
SS	SS	SS	SS
HB0	HB1	HB2	HB3
PB0	PB1	PB2	PB3
DB0	DB4	DB8	DB12
DB1	DB5	DB9	DB13
DB2	DB6	DB10	DB14
DB3	DB7	DB11	DB15
PB4	PB5	PB6	PB7
DB16	DB20	DB24	DB28
DB17	DB21	DB25	DB29
DB18	DB22	DB26	All 0s
DB19	DB23	DB27	All 0s
PB8	PB9	PB10	PB11
SE	SE	SE	SE

4-lane Main-Link

Lane 0	Lane 1
SS	SS
HB0	HB1
PB0	PB1
HB2	HB3
PB2	PB3
DB0	DB4
DB1	DB5
DB2	DB6
DB3	DB7
PB4	PB5
DB8	DB12
DB9	DB13
DB10	DB14
DB11	DB15
PB6	PB7
DB16	DB20
DB17	DB21
DB18	DB22
DB19	DB23
PB8	PB9
DB24	DB28
DB25	DB29
DB26	All 0s
DB27	All 0s
PB10	PB11
SE	SE

2-lane Main-Link

Lane 0
SS
HB0
PB0
HB1
PB1
HB2
PB2
HB3
PB3
DB0
DB1
DB2
DB3
PB4
DB4
DB5
DB6
DB7
PB5
⋮
DB24
DB25
DB26
DB27
PB10
DB28
DB29
All 0s
All 0s
PB11
SE

1-lane Main-Link

SS = Secondary-data packet Start
SE = Secondary-data packet End
HB*xx* = Header Byte
PB*xx* = Parity Byte
DB*xx* = Data Byte

Figure 2-22: INFOFRAME SDP

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2.2.5.1.1 INFOFRAME SDP Header v1.2

A DP device shall comply with *CEA-861-F* when using the INFOFRAME SDP as an Audio INFOFRAME.

The DB1 ~ DB*N* (Data Byte 1 ~ Data Byte *N*), as specified in *CEA-861-F*, are mapped to SDP DB0 ~ DB [*N* -1]. The unused bytes must be zero-padded.

In use cases for coding types other than One Bit or DST audio, certain control information such as the audio stream's Sampling Frequency, Sample Bits, and Coding Type can be set through Audio INFOFRAME or Stream header bits. When the Stream header case is used, the Audio INFOFRAME shall be set to "Refer to Stream Header" so that the control information can be passed to the receiver through *IEC 60958* or *IEC 61937* Stream header bits. (See *IEC 60958-3* for stream header bit field programming requirements.)

In use cases for the One Bit audio coding type, Sampling Frequency, and in the case of 8-channel One Bit audio, Speaker Mapping, must be set through the Audio INFOFRAME (CA, DM_INH, LSV, and LFEPBL). The Audio INFOFRAME sample size is ***not*** valid for 2- or 8-channel One Bit audio. Channel Count and Coding Type must be set in the Audio_Stream SDP header, leaving the matching Audio INFOFRAME fields cleared to 0 to indicate "Refer to Stream header."

In use cases for the DST audio coding type, Sampling Frequency must be set through the Audio INFOFRAME. Coding Type must be set in the Audio_Stream SDP header. Setting Channel Count in the Audio_Stream SDP header is ***not*** applicable for DST audio because the number of DST Audio channels is carried within the audio payload stream itself. This leaves the matching Audio INFOFRAME CC and CT fields cleared to 0 to indicate "Refer to Stream Header." Audio INFOFRAME Sample Size and Channel Allocation are ***not*** valid for DST audio.

Although some parameters are available in both the Audio_Stream and Audio INFOFRAME SDPs, the values of those in the Audio_Stream SDP take precedence.

The supported Audio coding types shall be transmitted by the Source device only if the Sink device indicates support for receiving the named coding type. The Sink device will indicate the support by way of short audio descriptions. For additional information, see *CEA-861-F* and *CEA-861.2*.

Other audio packing formats may be added in a future revision of this Standard while maintaining the consistent secondary-data mapping specification described in this Standard.

INFOFRAME SDPs shall be sent once per frame during the vertical blanking period of the main video stream. For the transport of an Audio INFOFRAME SDP without a main video stream, see Section 2.2.5.3.6. For further details regarding audio transport over DisplayPort, see Appendix A.

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Table 2-99 summarizes the header bytes of an INFOFRAME SDP v1.2.

Table 2-99: INFOFRAME SDP v1.2 Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID** Audio INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP must have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	**80h + Audio INFOFRAME Type value**
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count - 1)** For INFOFRAME, the value must be 1Bh (i.e., Data Byte Count = 28 bytes). Unused bytes must be zero-padded.
HB3	1:0	**Most Significant Two Bits of (Data Byte Count - 1)**
	7:2	**INFOFRAME SDP Version Number** 12h (010010b).

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2.2.5.1.2 INFOFRAME SDP Header v1.3 and Payload

Table 2-100 describe how to populate INFOFRAME SDP Header v1.3. Table 2-101 describes payload byte mapping of a non-audio CEA INFOFRAME. v1.3 shall be used for non-audio CEA INFOFRAME encapsulation.

Table 2-100: INFOFRAME SDP v1.3 Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID** Shall be 00h for non-Audio INFOFRAME. For Audio INFOFRAME: • When only one audio stream per main video stream is being transmitted, the value shall be 00h • When multiple audio streams per main video stream are being transmitted, this SDP ID value is used to distinguish one audio stream from the others
HB1	7:0	**80h + Non-audio INFOFRAME Type value**
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count - 1)** For Non-audio INFOFRAME, the value must be 1Dh (i.e., Data Byte Count = 30 bytes). Unused bytes must be zero-padded.
HB3	1:0	**Most Significant Two Bits of (Data Byte Count - 1)** Clear to 00b.
	7:2	**INFOFRAME SDP Version Number** 13h (010011b).

Table 2-101: SDP Payload v1.3 Data Bytes for Non-audio CEA INFOFRAME Encapsulation – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**CEA Header Byte 2 (INFOFRAME Version Number)**
DB1	7:0	**CEA Header Byte 3 (Length of INFOFRAME)**
DB2	7:0	**CEA Payload Byte 1**
DB3	7:0	**CEA Payload Byte 2**
DB4	7:0	**CEA Payload Byte 3**
…	…	**…**
DB29	7:0	**CEA Payload Byte 28** ***Note:*** *For CEA Payload size < 28 bytes, non-existent payload bytes are zero-padded.*
DB30	7:0	**Zero Padding**
DB31	7:0	**Zero Padding**

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2.2.5.2 Audio_TimeStamp SDP

Figure 2-23 shows an Audio_TimeStamp SDP over the Main-Link.

For the transport of an Audio_TimeStamp SDP without the main video stream, see Section 2.2.5.3.6. For more information about audio transport over DP, see Appendix A.

Figure 2-23: Audio_TimeStamp SDP Mapping over Main-Link

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The Audio_TimeStamp SDP consists of Maud23:0 and Naud23:0. The relationship of Maud and Naud is expressed in the following equation:

$$Maud / Naud = 512 * fs / f_LS_Clk$$

where *fs* is the sampling frequency of the audio stream being transported. Naud value is set to 2^{15} (=32,768) when the audio clock is asynchronous to the LS_Clk.

In addition to the Audio_TimeStamp SDP, Maud7:0 are transported once per main video stream horizontal line period immediately following Mvid7:0.

It is the responsibility of a Sink device to avoid audio glitch as long as the accuracy of the Audio_TimeStamp SDP value is within ±0.5%.

Note: *In MST mode, the Sink device must ignore the Maud and Mvid values sent by an MST Source device unless the MST Sink device is directly connected to the MST Source device via a single link as the Source device generates those values based on the LS_Clk of the link it is driving. An MST Sink device must be able to regenerate a stream clock without depending on Mvid and Mvid time stamp values because the MST Sink device might be plugged into an MST Branch device, not an MST Source device.*

2.2.5.2.1 Audio_TimeStamp SDP Header

Table 2-102 describes the header bytes of an Audio_TimeStamp SDP.

Table 2-102: Header Bytes of Audio_TimeStamp SDP

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, and Audio_CopyManagement SDP, and ISRC SDP must have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	01h
HB2	7:0	**Least Significant Eight Bits of (Data Byte Count - 1)** For an Audio_TimeStamp SDP, the value must be 17h (i.e., Data Byte Count = 24 bytes). Unused bytes must be zero-padded.
HB3	1:0	**Most Significant 2 Bits of (Data Byte Count - 1)**
	7:2	**Audio_TimeStamp Version Number** 12h.

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2.2.5.2.2 Audio_TimeStamp SDP Values (Informative)

Table 2-103 shows some examples of the audio time stamp SDP values for various audio sampling frequencies when the audio clock and Main-Link Symbol clock are synchronous.

Table 2-103: Examples of Maud and Naud Values (Informative)[a]

Coding Type	Audio Sample Frequency (kHz)	LS_Clk Frequency							
		162 MHz		270 MHz		540 MHz		810 MHz	
		Maud	Naud	Maud	Naud	Maud	Naud	Maud	Naud
LPCM and Compressed Audio with Fs ≤ 6.144Mbps	32	1024	10125	1024	16875	1024	33750	1024	50625
	44.1	784	5625	784	9375	784	18750	784	28125
	48	512	3375	512	5625	512	11250	512	16875
	64	2048	10125	2048	16875	2048	33750	2048	50625
	88.2	1568	5625	1568	9375	1568	18750	1568	28125
	96	1024	3375	1024	5625	1024	11250	1024	16875
	128	4096	10125	4096	16875	4096	33750	4096	50625
	176.4	3136	5625	3136	9375	3136	18750	3136	28125
	192	2048	3375	2048	5625	2048	11250	2048	16875
HBR	256	8192	10125	8192	16875	8192	33750	8192	50625
	352.8	6272	5625	6272	9375	6272	18750	6272	28125
	384	4096	3375	4096	5625	4096	11250	4096	16875
	512	16384	10125	16384	16875	16384	33750	16384	50625
	705.6	12544	5625	12544	9375	12544	18750	12544	28125
	768	8192	3375	8192	5625	8192	11250	8192	16875
	1024	32768	10125	32768	16875	32768	33750	32768	50625
	1411.2	25088	5625	25088	9375	25088	18750	25088	28125
	1536	16384	3375	16384	5625	16384	11250	16384	16875

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Table 2-103: Examples of Maud and Naud Values (Informative)[a] (Continued)

Coding Type	Audio Sample Frequency (kHz)	LS_Clk Frequency							
		162 MHz		270 MHz		540 MHz		810 MHz	
		Maud	Naud	Maud	Naud	Maud	Naud	Maud	Naud
One Bit and DST audio at normal or double rate	2048 (64 x 32)	65536	10125	65536	16875	65536	33750	65536	50625
	2822.4 (64 x 44.1)	50176	5625	50176	9375	50176	18750	50176	28125
	3072 (64 x 48)	32768	3375	32768	5625	32768	11250	32768	16875
	4096 (128 x 32)	131072	10125	131072	16875	131072	33750	131072	50625
	5644.8 (128 x 44.1 and 64 x 88.2)	100352	5625	100352	9375	100352	18750	100352	28125
	6144 (128 x 48 and 64 x 96)	65536	3375	65536	5625	65536	11250	65536	16875
	11289.6 (128 x 88.2 and 64 x 176.4)	200704	5625	200704	9375	200704	18750	200704	28125
	12288 (128 x 96 and 64 x 192)	131072	3375	131072	5625	131072	11250	131072	16875
	22579.2 (128 x 176.4)	401408	5625	401408	9375	401408	18750	401408	28125
	24576 (128 x 192)	262144	3375	262144	5625	262144	11250	262144	16875

a. No down-spreading, with synchronous clock, assumed.

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2.2.5.3 Audio_Stream SDP

Transport of an audio stream is optional. When an audio stream is transported, the Audio INFOFRAME SDP describing the attribute of the audio stream and Audio_TimeStamp SDP must be also transported, each once per frame during the vertical blanking period of the main video stream.

Audio_Stream SDPs must be sent during both horizontal and vertical blanking periods of the main video stream. During the horizontal and vertical blanking periods, DP Source device must transmit an Audio_Stream SDP whenever it has sufficient data to form a packet and access to the Main-Link to transmit the packet(s). For more information about audio transport over DP, see Section 2.2.5.3 and Appendix A.

Audio_Stream SDPs with compressed audio that uses the *IEC 61937* Transport standard will set the HB3.Coding Type, as follows:

- 0000 = Encoded content ≤ 6.144Mbps is transmitted
- 0001 = Encoded content exceeding 6.144Mbps is transmitted over the link

IEC 61937-encoded bit rates that exceed 6.144Mbps will be known as Audio High Bit Rate. DP allows nine different types of high bit rate transports, as listed in Table 2-104. Dolby True-HD and DTS Master Audio formats require higher bit rates for transport. A DP Source device must use one of these nine high bit rates to transmit such encoded content.

HBR audio delivery shall use the 8-channel layout packet configuration. This results in four *IEC 60958* transport frames per layout packet. Audio_Stream SDP Header configuration should be as follows:

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- *HB2.3DChannelCount* = 0 through 31 (N/A)
- *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
- *HB3.ChannelCount* = 7 (8-channel mode)
- *HB3.CodingType* = 1h (*IEC 61937*-encoded audio High Bit Rate)

Table 2-104: Audio High Bit Rate Mode (Informative)

DP Packet Rate 8-channel Layout (kHz)	*IEC 61937* Payload Bit Rate 2 x 16 bits per Frame, 4 Frames per Layout (Mbps)	*IEC 60958* Transport Bit Rate 2 x 32 bits per Frame (Mbps)	*IEC 60958* Frame Rate (kHz)	Audio_TimeStamp fs Indication (kHz)
64	8.192	16.384	256[a]	256
88.2	11.2896	22.5792	352.8[a]	352.8
96	12.288	24.576	384[a]	384
128	16.384	32.768	512[a]	512
176.4	22.5792	45.1584	705.6[a]	705.6
192	24.576	49.152	768	768
256[b]	32.768	65.536	1024[a]	1024
352.8[b]	45.1584	90.3168	1411.2[a]	1411.2
384[b]	49.152	98.304	1536[a]	1536

a. Audio High Bit Rate is ***not*** *supported in DP v1.3 (and lower).*
b. DisplayPort 8-channel layout packet rate exceeds DP v1.3 (and lower) maximum 8-channel layout packet rate.

IEC 61937-encoded audio streams with bit rates less than or equal to 6.144Mbps will be known as "Non-HBR *IEC 61937*-encoded audio." Non-HBR *IEC 61937*-encoded audio shall use the 2-channel layout packet configuration. DisplayPort allows nine different Non-HBR *IEC 61937* transports that use the 2-channel layout packet configuration (see Table 2-105). This configuration uses one *IEC 60958* transport frame per layout packet. The Audio_Stream SDP header configuration for this method should be as follows:

- *HB2.3DChannelCount* = 0 through 31 (N/A)
- *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
- *HB3.ChannelCount* = 1 (2-channel mode)
- *HB3.CodingType* = 0h (Non-HBR *IEC 61937*-encoded audio)

While it is theoretically possible to use the 8-channel layout packet configuration to transport Non-HBR *IEC 61937*-encoded audio at 32, 44.1, and 48kHz sampling rates, the 8-channel layout shall not be used to convey Non-HBR *IEC 61937*-encoded audio.

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Table 2-105: Non-HBR-Encoded Audio 2-channel Layout (Informative)

DP Packet Rate 2-channel Layout (kHz)	*IEC 61937* Payload Bit Rate 2 x 16 bits per Frame, 1 Frame per Layout (Mbps)	*IEC 60958* Transport Bit Rate 2 x 32 bits per Frame (Mbps)	*IEC 60958* Frame Rate (kHz)	Audio_TimeStamp fs Indication (kHz)
32	1.024	2.048	32	32
44.1	1.4112	2.8224	44.1	44.1
48	1.536	3.072	48	48
64	2.048	4.096	64[a]	64
88.2	2.8224	5.6448	88.2	88.2
96	3.072	6.144	96	96
128	4.096	8.192	128[a]	128
176.4	5.6448	11.2896	176.4	176.4
192	6.144	12.288	192	192

a. Audio Bit Rate is ***not*** *supported in DP v1.3 (and lower).*

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Audio_Stream SDPs with no compression, LPCM audio can have four layouts, as listed in Table 2-106. The Audio_Stream SDP header configuration for LPCM and 3D LPCM audio is as follows:

- 2-channel LPCM
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 0 or 1 (2-channel mode)
  - *HB3.CodingType* = 0h (LPCM audio, coding type indicated in *IEC 60958* header)
- 8-channel LPCM
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 2 through 7 (8-channel mode)
  - *HB3.CodingType* = 0h (LPCM audio, coding type indicated in *IEC 60958* header)
- 16-channel 3D LPCM
  - *HB2.3DChannelCount* = 0 through 15 (16-channel mode)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 0 through 7 (N/A)
  - *HB3.CodingType* = 2h (3D LPCM audio)
- 32-channel 3D LPCM
  - *HB2.3DChannelCount* = 16 through 31 (32-channel mode)
  - *HB2.OneBit_DST_Double_Rate* = 0 through 1 (N/A)
  - *HB3.ChannelCount* = 0 through 7 (N/A)
  - *HB3.CodingType* = 2h (3D LPCM audio)

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Table 2-106: LPCM Audio Modes (Informative)

DP Packet Rate (kHz)	*IEC 60958* Data Transport Rate 2 x 32 bits per Frame				Audio_TimeStamp fs Indication (kHz)
	2-channel LPCM 1 Frame per Layout (Mbps)	8-channel LPCM 4 Frames per Layout (Mbps)	16-channel 3D LPCM 8 Frames per Layout (Mbps)	32-channel 3D LPCM 16 Frames per Layout (Mbps)	
32	2.048	8.192	16.384	32.768	32
44.1	2.8224	11.2896	22.5792	45.1584	44.1
48	3.072	12.288	24.576	49.152	48
64[a]	4.096	16.384	N/A	N/A	64
88.2	5.6448	22.5792	45.1584	90.3168	88.2
96	6.144	24.576	49.152	98.304	96
128[a]	8.192	32.768	N/A	N/A	128
176.4	11.2896	45.1584	90.3168	180.6336	176.4
192	12.288	49.152	98.304	196.608	192

a. Audio Packet Rate is ***not*** *supported in DP v1.3 (and lower).*

Audio_Stream SDPs with One Bit or DST audio can have three layouts, as listed in Table 2-107. The Audio_Stream SDP header configuration for One Bit and DST audio is as follows:

- 2-channel One Bit audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 or 1 (64x or 128x)
  - *HB3.ChannelCount* = 0 or 1 (2-channel mode)
  - *HB3.CodingType* = 3h (One Bit audio coding type)
- 8-channel One Bit audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 or 1 (64x or 128x)
  - *HB3.ChannelCount* = 2 through 7 (8-channel mode)
  - *HB3.CodingType* = 3h (One Bit audio coding type)
- DST audio
  - *HB2.3DChannelCount* = 0 through 31 (N/A)
  - *HB2.OneBit_DST_Double_Rate* = 0 or 1 (64x or 128x)
  - *HB3.ChannelCount* = 0 through 7 (N/A)
  - *HB3.CodingType* = 4h (DST audio coding type)

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Table 2-107: One Bit and DST Audio Modes (Informative)

Sample Frequency. as Indicated in Audio INFOFRAME (kHz)	HB2.OneBit_DST_Double_Rate	# of Bytes per Frame at 75 fps	One Bit Layouts per Frame at 75fps[a]	One Bit Layout Rate (kHz)	2-channel One Bit Transport Rate at 64 bits per Layout (Mbps)	8-channel One Bit Transport Rate at 256 bits per Layout (Mbps)	DST Layouts per Frame at 75fps[b]	DST Layout Rate (kHz)	DST Transport Rate at 256 bits per Layout (Mbps)	Audio_TimeStamp fs Indication (kHz)
32	0	3413.333	975.238	73.143	4.681	18.725	121.905	9.143	2.341	2048
	1	6826.667	1950.476	146.286	9.362	37.449	243.810	18.286	4.681	4096
44.1	0	4704	1344	100.8	6.451	25.805	168	12.6	3.226	2822.4
	1	9408	2688	201.6	12.902	51.610	336	25.2	6.451	5644.8
48	0	5120	1462.857	109.714	7.022	28.087	182.857	13.714	3.511	3072
	1	10240	2925.714	219.429	14.043	56.174	365.714	27.429	7.022	6144
88.2	0	9408	2688	201.6	12.902	51.610	336	25.2	6.451	5644.8
	1	18816	5376	403.2	25.805	103.219	672	50.4	12.902	11289.6
96	0	10240	2925.714	219.429	14.043	56.174	365.714	27.429	7.022	6144
	1	20480	5851.429	438.857	28.087	112.347	731.429	54.857	14.043	12288
176.4	0	18816	5376	403.2	25.805	103.219	672	50.4	12.902	11289.6
	1	37632	10752	806.4	51.610	206.438	1344	100.8	25.805	22579.2
192	0	20480	5851.429	438.857	28.087	112.347	731.429	54.857	14.043	12288
	1	40960	11702.857	877.714	56.174	224.695	1462.857	109.714	28.087	24576

a. *Indicates the number of One Bit audio layouts at which the Frame Start Flag should be asserted, rounded to the next integer number of layouts.*

b. *Indicates the number of DST audio layouts at which the Frame Start Flag should be asserted, rounded to the next integer number of layouts.*

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2.2.5.3.1 Audio Playback Latency Requirement

A DP Sink device audio recovery time from idle to playback (i.e., audio being presented to the end-user) must not exceed 50ms from the time the first Audio Sample, Audio INFOFRAME, or audio clock regeneration packet is received. The Sink device must mute playback during recovery of the local audio clock to avoid audible noise. A DP Source device may send Audio_TimeStamp and/or INFOFRAME SDPs prior to sending the Audio_Stream SDP to ensure that any recovery necessary at the DP Sink device has completed.

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2.2.5.3.2 Audio_Stream SDP Header

Table 2-108 describes the header bytes of an Audio_Stream SDP.

Table 2-108: Audio_Stream SDP Header Bytes

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP must have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	02h
HB2	4:0	**3DChannelCount** New to *DP v1.4*. Applicable only for 3D LPCM coding types. Indicates *Number of Channels - 1*. Available in 16- and 32-channel layouts: • 16-channel layout is identified exclusively using this field equal to or larger than 0, but less than 16. Includes the possibility of Mono or Stereo Audio carried in this 3D LPCM Coding Type layout. • 32-channel layout is identified exclusively using this field equal to or larger than 16, but less than 32 For all 3D-channel layouts, there is no requirement on a DP Source device to match this value to the actual channel count. A DP Sink device must use this field to determine whether the incoming Audio_Stream SDP has a 16- or 32-channel layout. Actual channel count and the channel-to-speaker mapping must be obtained from the Audio INFOFRAME SDP Channel Allocation field, as well as DB6 through DB9.
	5	**OneBit_DST_Double_Rate** New to *DP v1.4*. Applicable only for One Bit audio or DST audio coding types. 0 = One Bit audio or underlying uncompressed DST bit stream sample rate = 64x sample frequency, as indicated in DB2 of the Audio INFOFRAME SDP. 1 = One Bit audio or underlying uncompressed DST bit stream sample rate = 128x sample frequency, as indicated in DB2 of Audio INFOFRAME SDP.
	7:6	**RESERVED** Read all 0s.

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Table 2-108: Audio_Stream SDP Header Bytes (Continued)

Byte #	Bit #	Content
HB3	2:0	**ChannelCount** 2-channel layout and mono vs. stereo are identified exclusively using this field: 0 = Mono 1 = Stereo 8-channel layout is identified exclusively using this field equal to or larger than 2. For 8-channel layout, there is no requirement on a Source device to match this value to the actual channel count, and a Sink device must use this field to determine whether the incoming Audio_Stream SDP has an 8-channel layout. Actual channel count and the channel-to-speaker mapping must be obtained from the Audio INFOFRAME SDP Channel Allocation field.
	3	**RESERVED** Read 0.
	7:4	**Coding Type** Support for values 2h through 4h added in *DP v1.4*. 0h = 2- to 8-channel LPCM 192kHz content/*IEC 61937*-encoded content with bit rates less than or equal to 6.144Mbps (*IEC 60958*-like encoding). 1h = *IEC 61937*-encoded content for bit rates exceeding 6.144Mbps (*IEC 60958*-like encoding). 2h = 1- to 32-channel 3D LPCM audio, up to 192kHz content; used in conjunction with the HB2 3DChannelCount field (bits 4:0), which renders the ChannelCount field inapplicable. 3h = One Bit audio, up to 192kHz content; used in conjunction with the ChannelCount field, which renders the HB2 3DChannelCount field (bits 4:0) inapplicable. 4h = DST audio, up to 192kHz content; both ChannelCount and 3DChannelCount are not applicable. The number of DST Audio channels is carried in the audio payload stream itself. All other values are RESERVED for DisplayPort.

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2.2.5.3.3 Audio_Stream Data Mapping over the Main-Link

The HB3 ChannelCount field (bits 2:0) of an Audio_Stream SDP is the count of non-3D LPCM audio or One Bit audio channels transmitted through a DP Main-Link. The DPRX must use this 3-bit value to decide how to interpret the payload of an Audio_Stream SDP. One to eight channels are supported in non-3D LPCM, *IEC 61937*-encoded, or One Bit DisplayPort audio transport.

The HB2 3DChannelCount field (bits 4:0) of an Audio_Stream SDP is the count of 3D LPCM audio channels transmitted through a DP Main-Link. The DPRX must use this 5-bit value to determine how to interpret the Audio_Stream SDP payload. One to 32 channels are supported in 3D LPCM DP audio transport.

Figure 2-24 shows the Audio_Stream SDP mapping over the Main-Link for 1- to 2-channel LPCM audio, *IEC 61937*-encoded Non-HBR audio, or One Bit audio. Figure 2-25 shows the Audio_Stream SDP mapping over the Main-Link for 3- to 8-channel LPCM audio, *IEC 61937*-encoded HBR audio, or One Bit audio. Figure 2-33 shows the mapping within each 4-byte payload of the LPCM or *IEC 61937*-encoded Audio_Stream SDP. Figure 2-34 shows the mapping within each 4-byte payload of the One Bit Audio_Stream SDP.

Figure 2-26 shows the Audio_Stream SDP mapping over the Main-Link for 1- to 16-channel 3D LPCM audio. Figure 2-27 shows the mapping for 17- to 32-channel 3D LPCM audio. Figure 2-33 shows the mapping within each 4-byte payload of the 3D LPCM Audio_Stream SDP.

For 1- to 2-channel audio, two sets of 32-bit audio packet payload carry one audio sample.
For 3- to 8-channel audio, eight sets of 32-bit audio packet payload carry one audio sample.
For 1- to 16-channel audio, 16 sets of 32-bit audio packet payload carry one audio sample.
For 17- to 32-channel audio, 32 sets of 32-bit audio packet payload carry one audio sample.

Figure 2-28 shows the Audio_Stream SDP mapping over the Main-Link for DST audio. Figure 2-35 shows the mapping within each of the eight sub-layouts of the DST Audio_Stream SDP.

Those sets of 32-bit audio packet payloads that carry the same audio sample must have the same value in the SP (Sample Present) bit. If the sample is present, SP must be set to 1. If the sample is absent, SP must be cleared to 0.

An Audio_Stream SDP transfer must not stop in the middle of an audio sample, and must be zero-padded, if necessary, so that it meets the minimum required payload size of 16 bytes. For designs that support Split SDP transactions, an Audio_Stream SDP may be temporarily interrupted, if needed, at the end of an hblank period and resume at the start of the next Horizontal Blanking period (see Section 2.2.5.12 for details).

For example, when a 2-channel audio is transmitted over a 1-lane Main-Link, the packet may be ended after PB7 in Figure 2-24 because the transmission of Sample 0 is completed at that point. However, it must not end after PB6. Furthermore, it must not end after PB5 because it would not meet the minimum payload size of 16 bytes. If only S0 is available for transmission, 0s must be transmitted in the S1 location.

Audio high bit rate transmission shall always use the 8-channel layout to transmit the content. Pa/Pb sync words shall be located only on the Channel 1 and Channel 2 location in the 8-channel layout, this Pa/Pb sync word location restriction applies to only Dolby True-HD and DTS HD Master Audio transmission.

The mapping of audio data to channels depends on the audio-data-to-speaker mapping.

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S1_Ch1_B0	S1_Ch2_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S1_Ch1_B1	S1_Ch2_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S1_Ch1_B2	S1_Ch2_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S1_Ch1_B3	S1_Ch2_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S2_Ch1_B0	S2_Ch2_B0	S3_Ch1_B0	S3_Ch2_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S2_Ch1_B1	S2_Ch2_B1	S3_Ch1_B1	S3_Ch2_B1	PB4	PB5	S0_Ch1_B0
S2_Ch1_B2	S2_Ch2_B2	S3_Ch1_B2	S3_Ch2_B2	S1_Ch1_B0	S1_Ch2_B0	S0_Ch1_B1
S2_Ch1_B3	S2_Ch2_B3	S3_Ch1_B3	S3_Ch2_B3	S1_Ch1_B1	S1_Ch2_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S1_Ch1_B2	S1_Ch2_B2	S0_Ch1_B3
SE	SE	SE	SE	S1_Ch1_B3	S1_Ch2_B3	PB4
Note: *Explanation of combined "_"-related text:* • *S = Sample.* • *B = Byte.* • *Ch = Channel.* *For example, S0_Ch1_B0 means Byte 0 of Channel 1 of Sample 0.*				PB6	PB7	S0_Ch2_B0
				S2_Ch1_B0	S2_Ch2_B0	S0_Ch2_B1
				S2_Ch1_B1	S2_Ch2_B1	S0_Ch2_B2
				S2_Ch1_B2	S2_Ch2_B2	S0_Ch2_B3
				S2_Ch1_B3	S2_Ch2_B3	PB5
				PB8	PB9	S1_Ch1_B0
				S3_Ch1_B0	S3_Ch2_B0	S1_Ch1_B1
				S3_Ch1_B1	S3_Ch2_B1	S1_Ch1_B2
				S3_Ch1_B2	S3_Ch2_B2	S1_Ch1_B3
				S3_Ch1_B3	S3_Ch2_B3	PB6
				PB10	PB11	S1_Ch2_B0
				SE	SE	S1_Ch2_B1
						S1_Ch2_B2
						S1_Ch2_B3
						PB7

Figure 2-24: Audio_Stream SDP over Main-Link for 2-Channel Layout Audio

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
						S2_Ch1_B0
						S2_Ch1_B1
						S2_Ch1_B2
						S2_Ch1_B3
						PB8
						S2_Ch2_B0
						S2_Ch2_B1
						S2_Ch2_B2
						S2_Ch2_B3
						PB9
						S3_Ch1_B0
						S3_Ch1_B1
						S3_Ch1_B2
						S3_Ch1_B3
						PB10
						S3_Ch2_B0
						S3_Ch2_B1
						S3_Ch2_B2
						S3_Ch2_B3
						PB11
						SE

Figure 2-24: Audio_Stream SDP over Main-Link for 2-Channel Layout Audio (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	S0_Ch4_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	S0_Ch4_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch4_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch8_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	S0_Ch8_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch8_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
SE	SE	SE	SE	S0_Ch3_B3	S0_Ch4_B3	PB4
Note: *Explanation of combined "_"-related text:*				PB6	PB7	S0_Ch2_B0
• *S = Sample.*				S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
• *B = Byte.*				S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
• *Ch = Channel.*				S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
For example, S0_Ch1_B0 means Byte 0 of Channel 1 of Sample 0.				S0_Ch5_B3	S0_Ch6_B3	PB5
				PB8	PB9	S0_Ch3_B0
				S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
				S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
				S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
				S0_Ch7_B3	S0_Ch8_B3	PB6
				PB10	PB11	S0_Ch4_B0
				SE	SE	S0_Ch4_B1
						S0_Ch4_B2
						S0_Ch4_B3
						PB7
						S0_Ch5_B0
						S0_Ch5_B1
						S0_Ch5_B2
						S0_Ch5_B3
						PB8

Figure 2-25: Audio_Stream SDP over Main-Link for 8-Channel Layout Audio

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
						S0_Ch6_B0
						S0_Ch6_B1
						S0_Ch6_B2
						S0_Ch6_B3
						PB9
						S0_Ch7_B0
						S0_Ch7_B1
						S0_Ch7_B2
						S0_Ch7_B3
						PB10
						S0_Ch8_B0
						S0_Ch8_B1
						S0_Ch8_B2
						S0_Ch8_B3
						PB11
						SE

Figure 2-25: Audio_Stream SDP over Main-Link for 8-Channel Layout Audio (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	S0_Ch4_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	S0_Ch4_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch4_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch8_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	S0_Ch8_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch8_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
S0_Ch9_B0	S0_Ch10_B0	S0_Ch11_B0	S0_Ch12_B0	S0_Ch3_B3	S0_Ch4_B3	PB4
S0_Ch9_B1	S0_Ch10_B1	S0_Ch11_B1	S0_Ch12_B1	PB6	PB7	S0_Ch2_B0
S0_Ch9_B2	S0_Ch10_B2	S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
S0_Ch9_B3	S0_Ch10_B3	S0_Ch11_B3	S0_Ch12_B3	S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
PB12	PB13	PB14	PB15	S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
S0_Ch13_B0	S0_Ch14_B0	S0_Ch15_B0	S0_Ch16_B0	S0_Ch5_B3	S0_Ch6_B3	PB5
S0_Ch13_B1	S0_Ch14_B1	S0_Ch15_B1	S0_Ch16_B1	PB8	PB9	S0_Ch3_B0
S0_Ch13_B2	S0_Ch14_B2	S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
S0_Ch13_B3	S0_Ch14_B3	S0_Ch15_B3	S0_Ch16_B3	S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
PB16	PB17	PB18	PB19	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
SE	SE	SE	SE	S0_Ch7_B3	S0_Ch8_B3	PB6
Note: *Explanation of combined "_"-related text:*				PB10	PB11	S0_Ch4_B0
• *S = Sample.*				S0_Ch9_B0	S0_Ch10_B0	S0_Ch4_B1
• *B = Byte.*				S0_Ch9_B1	S0_Ch10_B1	S0_Ch4_B2
• *Ch = Channel.*				S0_Ch9_B2	S0_Ch10_B2	S0_Ch4_B3
For example, S0_Ch1_B0 means Byte 0 of Channel 1 of Sample 0.				S0_Ch9_B3	S0_Ch10_B3	PB7
				PB12	PB13	S0_Ch5_B0
				S0_Ch11_B0	S0_Ch12_B0	S0_Ch5_B1
				S0_Ch11_B1	S0_Ch12_B1	S0_Ch5_B2
				S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B3
				S0_Ch11_B3	S0_Ch12_B3	PB8

Figure 2-26: Audio_Stream SDP over Main-Link for 16-Channel Layout Audio (3D LPCM Audio Extension Type Code 13)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
				PB14	PB15	S0_Ch6_B0
				S0_Ch13_B0	S0_Ch14_B0	S0_Ch6_B1
				S0_Ch13_B1	S0_Ch14_B1	S0_Ch6_B2
				S0_Ch13_B2	S0_Ch14_B2	S0_Ch6_B3
				S0_Ch13_B3	S0_Ch14_B3	PB9
				PB16	PB17	S0_Ch7_B0
				S0_Ch15_B0	S0_Ch16_B0	S0_Ch7_B1
				S0_Ch15_B1	S0_Ch16_B1	S0_Ch7_B2
				S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B3
				S0_Ch15_B3	S0_Ch16_B3	PB10
				PB18	PB19	S0_Ch8_B0
				SE	SE	S0_Ch8_B1
						S0_Ch8_B2
						S0_Ch8_B3
						PB11
						S0_Ch9_B0
						S0_Ch9_B1
						S0_Ch9_B2
						S0_Ch9_B3
						PB12
						S0_Ch10_B0
						S0_Ch10_B1
						S0_Ch10_B2
						S0_Ch10_B3
						PB13
						S0_Ch11_B0
						S0_Ch11_B1
						S0_Ch11_B2
						S0_Ch11_B3
						PB14
						S0_Ch12_B0
						S0_Ch12_B1
						S0_Ch12_B2
						S0_Ch12_B3
						PB15

Figure 2-26: Audio_Stream SDP over Main-Link for 16-Channel Layout Audio (3D LPCM Audio Extension Type Code 13) (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
						S0_Ch13_B0
						S0_Ch13_B1
						S0_Ch13_B2
						S0_Ch13_B3
						PB16
						S0_Ch14_B0
						S0_Ch14_B1
						S0_Ch14_B2
						S0_Ch14_B3
						PB17
						S0_Ch15_B0
						S0_Ch15_B1
						S0_Ch15_B2
						S0_Ch15_B3
						PB18
						S0_Ch16_B0
						S0_Ch16_B1
						S0_Ch16_B2
						S0_Ch16_B3
						PB19
						SE

Figure 2-26: Audio_Stream SDP over Main-Link for 16-Channel Layout Audio (3D LPCM Audio Extension Type Code 13) (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	S0_Ch4_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	S0_Ch4_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch4_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch8_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	S0_Ch8_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch8_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
S0_Ch9_B0	S0_Ch10_B0	S0_Ch11_B0	S0_Ch12_B0	S0_Ch3_B3	S0_Ch4_B3	PB4
S0_Ch9_B1	S0_Ch10_B1	S0_Ch11_B1	S0_Ch12_B1	PB6	PB7	S0_Ch2_B0
S0_Ch9_B2	S0_Ch10_B2	S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
S0_Ch9_B3	S0_Ch10_B3	S0_Ch11_B3	S0_Ch12_B3	S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
PB12	PB13	PB14	PB15	S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
S0_Ch13_B0	S0_Ch14_B0	S0_Ch15_B0	S0_Ch16_B0	S0_Ch5_B3	S0_Ch6_B3	PB5
S0_Ch13_B1	S0_Ch14_B1	S0_Ch15_B1	S0_Ch16_B1	PB8	PB9	S0_Ch3_B0
S0_Ch13_B2	S0_Ch14_B2	S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
S0_Ch13_B3	S0_Ch14_B3	S0_Ch15_B3	S0_Ch16_B3	S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
PB16	PB17	PB18	PB19	S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
S0_Ch17_B0	S0_Ch18_B0	S0_Ch19_B0	S0_Ch20_B0	S0_Ch7_B3	S0_Ch8_B3	PB6
S0_Ch17_B1	S0_Ch18_B1	S0_Ch19_B1	S0_Ch20_B1	PB10	PB11	S0_Ch4_B0
S0_Ch17_B2	S0_Ch18_B2	S0_Ch19_B2	S0_Ch20_B2	S0_Ch9_B0	S0_Ch10_B0	S0_Ch4_B1
S0_Ch17_B3	S0_Ch18_B3	S0_Ch19_B3	S0_Ch20_B3	S0_Ch9_B1	S0_Ch10_B1	S0_Ch4_B2
PB20	PB21	PB22	PB23	S0_Ch9_B2	S0_Ch10_B2	S0_Ch4_B3
S0_Ch21_B0	S0_Ch22_B0	S0_Ch23_B0	S0_Ch24_B0	S0_Ch9_B3	S0_Ch10_B3	PB7
S0_Ch21_B1	S0_Ch22_B1	S0_Ch23_B1	S0_Ch24_B1	PB12	PB13	S0_Ch5_B0
S0_Ch21_B2	S0_Ch22_B2	S0_Ch23_B2	S0_Ch24_B2	S0_Ch11_B0	S0_Ch12_B0	S0_Ch5_B1
S0_Ch21_B3	S0_Ch22_B3	S0_Ch23_B3	S0_Ch24_B3	S0_Ch11_B1	S0_Ch12_B1	S0_Ch5_B2
PB24	PB25	PB26	PB27	S0_Ch11_B2	S0_Ch12_B2	S0_Ch5_B3
S0_Ch25_B0	S0_Ch26_B0	S0_Ch27_B0	S0_Ch28_B0	S0_Ch11_B3	S0_Ch12_B3	PB8

Figure 2-27: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (3D LPCM Audio Extension Type Code 13)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
S0_Ch25_B1	S0_Ch26_B1	S0_Ch27_B1	S0_Ch28_B1	PB14	PB15	S0_Ch6_B0
S0_Ch25_B2	S0_Ch26_B2	S0_Ch27_B2	S0_Ch28_B2	S0_Ch13_B0	S0_Ch14_B0	S0_Ch6_B1
S0_Ch25_B3	S0_Ch26_B3	S0_Ch27_B3	S0_Ch28_B3	S0_Ch13_B1	S0_Ch14_B1	S0_Ch6_B2
PB28	PB29	PB30	PB31	S0_Ch13_B2	S0_Ch14_B2	S0_Ch6_B3
S0_Ch29_B0	S0_Ch30_B0	S0_Ch31_B0	S0_Ch32_B0	S0_Ch13_B3	S0_Ch14_B3	PB9
S0_Ch29_B1	S0_Ch30_B1	S0_Ch31_B1	S0_Ch32_B1	PB16	PB17	S0_Ch7_B0
S0_Ch29_B2	S0_Ch30_B2	S0_Ch31_B2	S0_Ch32_B2	S0_Ch15_B0	S0_Ch16_B0	S0_Ch7_B1
S0_Ch29_B3	S0_Ch30_B3	S0_Ch31_B3	S0_Ch32_B3	S0_Ch15_B1	S0_Ch16_B1	S0_Ch7_B2
PB32	PB33	PB34	PB35	S0_Ch15_B2	S0_Ch16_B2	S0_Ch7_B3
SE	SE	SE	SE	S0_Ch15_B3	S0_Ch16_B3	PB10
Note: *Explanation of combined "_"-related text:* • *S = Sample.* • *B = Byte.* • *Ch = Channel.* *For example, S0_Ch1_B0 means Byte 0 of Channel 1 of Sample 0.*				PB18	PB19	S0_Ch8_B0
				S0_Ch17_B0	S0_Ch18_B0	S0_Ch8_B1
				S0_Ch17_B1	S0_Ch18_B1	S0_Ch8_B2
				S0_Ch17_B2	S0_Ch18_B2	S0_Ch8_B3
				S0_Ch17_B3	S0_Ch18_B3	PB11
				PB20	PB21	S0_Ch9_B0
				S0_Ch19_B0	S0_Ch20_B0	S0_Ch9_B1
				S0_Ch19_B1	S0_Ch20_B1	S0_Ch9_B2
				S0_Ch19_B2	S0_Ch20_B2	S0_Ch9_B3
				S0_Ch19_B3	S0_Ch20_B3	PB12
				PB22	PB23	S0_Ch10_B0
				S0_Ch21_B0	S0_Ch22_B0	S0_Ch10_B1
				S0_Ch21_B1	S0_Ch22_B1	S0_Ch10_B2
				S0_Ch21_B2	S0_Ch22_B2	S0_Ch10_B3
				S0_Ch21_B3	S0_Ch22_B3	PB13
				PB24	PB25	S0_Ch11_B0
				S0_Ch23_B0	S0_Ch24_B0	S0_Ch11_B1
				S0_Ch23_B1	S0_Ch24_B1	S0_Ch11_B2
				S0_Ch23_B2	S0_Ch24_B2	S0_Ch11_B3
				S0_Ch23_B3	S0_Ch24_B3	PB14
				PB26	PB27	S0_Ch12_B0
				S0_Ch25_B0	S0_Ch26_B0	S0_Ch12_B1
				S0_Ch25_B1	S0_Ch26_B1	S0_Ch12_B2
				S0_Ch25_B2	S0_Ch26_B2	S0_Ch12_B3
				S0_Ch25_B3	S0_Ch26_B3	PB15

Figure 2-27: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (3D LPCM Audio Extension Type Code 13) (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
				PB28	PB29	S0_Ch13_B0
				S0_Ch27_B0	S0_Ch28_B0	S0_Ch13_B1
				S0_Ch27_B1	S0_Ch28_B1	S0_Ch13_B2
				S0_Ch27_B2	S0_Ch28_B2	S0_Ch13_B3
				S0_Ch27_B3	S0_Ch28_B3	PB16
				PB30	PB31	S0_Ch14_B0
				S0_Ch29_B0	S0_Ch30_B0	S0_Ch14_B1
				S0_Ch29_B1	S0_Ch30_B1	S0_Ch14_B2
				S0_Ch29_B2	S0_Ch30_B2	S0_Ch14_B3
				S0_Ch29_B3	S0_Ch30_B3	PB17
				PB32	PB33	S0_Ch15_B0
				S0_Ch31_B0	S0_Ch32_B0	S0_Ch15_B1
				S0_Ch31_B1	S0_Ch32_B1	S0_Ch15_B2
				S0_Ch31_B2	S0_Ch32_B2	S0_Ch15_B3
				S0_Ch31_B3	S0_Ch32_B3	PB18
				PB34	PB35	S0_Ch16_B0
				SE	SE	S0_Ch16_B1
						S0_Ch16_B2
						S0_Ch16_B3
						PB19
						S0_Ch17_B0
						S0_Ch17_B1
						S0_Ch17_B2
						S0_Ch17_B3
						PB20
						S0_Ch18_B0
						S0_Ch18_B1
						S0_Ch18_B2
						S0_Ch18_B3
						PB21
						S0_Ch19_B0
						S0_Ch19_B1
						S0_Ch19_B2
						S0_Ch19_B3
						PB22

Figure 2-27: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (3D LPCM Audio Extension Type Code 13) (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
						S0_Ch20_B0
						S0_Ch20_B1
						S0_Ch20_B2
						S0_Ch20_B3
						PB23
						S0_Ch21_B0
						S0_Ch21_B1
						S0_Ch21_B2
						S0_Ch21_B3
						PB24
						S0_Ch22_B0
						S0_Ch22_B1
						S0_Ch22_B2
						S0_Ch22_B3
						PB25
						S0_Ch23_B0
						S0_Ch23_B1
						S0_Ch23_B2
						S0_Ch23_B3
						PB26
						S0_Ch24_B0
						S0_Ch24_B1
						S0_Ch24_B2
						S0_Ch24_B3
						PB27
						S0_Ch25_B0
						S0_Ch25_B1
						S0_Ch25_B2
						S0_Ch25_B3
						PB28
						S0_Ch26_B0
						S0_Ch26_B1
						S0_Ch26_B2
						S0_Ch26_B3
						PB29

Figure 2-27: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (3D LPCM Audio Extension Type Code 13) (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
						S0_Ch27_B0
						S0_Ch27_B1
						S0_Ch27_B2
						S0_Ch27_B3
						PB30
						S0_Ch28_B0
						S0_Ch28_B1
						S0_Ch28_B2
						S0_Ch28_B3
						PB31
						S0_Ch29_B0
						S0_Ch29_B1
						S0_Ch29_B2
						S0_Ch29_B3
						PB32
						S0_Ch30_B0
						S0_Ch30_B1
						S0_Ch30_B2
						S0_Ch30_B3
						PB33
						S0_Ch31_B0
						S0_Ch31_B1
						S0_Ch31_B2
						S0_Ch31_B3
						PB34
						S0_Ch32_B0
						S0_Ch32_B1
						S0_Ch32_B2
						S0_Ch32_B3
						PB35
						SE

Figure 2-27: Audio_Stream SDP over Main-Link for 32-Channel Layout Audio (3D LPCM Audio Extension Type Code 13) (Continued)

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_SL1_B0	S0_SL2_B0	S0_SL3_B0	S0_SL4_B0	HB2	HB3	HB1
S0_SL1_B1	S0_SL2_B1	S0_SL3_B1	S0_SL4_B1	PB2	PB3	PB1
S0_SL1_B2	S0_SL2_B2	S0_SL3_B2	S0_SL4_B2	S0_SL1_B0	S0_SL2_B0	HB2
S0_SL1_B3	S0_SL2_B3	S0_SL3_B3	S0_SL4_B3	S0_SL1_B1	S0_SL2_B1	PB2
PB4	PB5	PB6	PB7	S0_SL1_B2	S0_SL2_B2	HB3
S0_SL5_B0	S0_SL6_B0	S0_SL7_B0	S0_SL8_B0	S0_SL1_B3	S0_SL2_B3	PB3
S0_SL5_B1	S0_SL6_B1	S0_SL7_B1	S0_SL8_B1	PB4	PB5	S0_SL1_B0
S0_SL5_B2	S0_SL6_B2	S0_SL7_B2	S0_SL8_B2	S0_SL3_B0	S0_SL4_B0	S0_SL1_B1
S0_SL5_B3	S0_SL6_B3	S0_SL7_B3	S0_SL8_B3	S0_SL3_B1	S0_SL4_B1	S0_SL1_B2
PB8	PB9	PB10	PB11	S0_SL3_B2	S0_SL4_B2	S0_SL1_B3
SE	SE	SE	SE	S0_SL3_B3	S0_SL4_B3	PB4
Note: *Explanation of combined "_"-related text:* • *S = Sample.* • *B = Byte.* • *SL = Sub-layout.* *For example, S0_SL1_B0 means Byte 0 of Sub-layout 1 of Sample 0.*				PB6	PB7	S0_SL2_B0
				S0_SL5_B0	S0_SL6_B0	S0_SL2_B1
				S0_SL5_B1	S0_SL6_B1	S0_SL2_B2
				S0_SL5_B2	S0_SL6_B2	S0_SL2_B3
				S0_SL5_B3	S0_SL6_B3	PB5
				PB8	PB9	S0_SL3_B0
				S0_SL7_B0	S0_SL8_B0	S0_SL3_B1
				S0_SL7_B1	S0_SL8_B1	S0_SL3_B2
				S0_SL7_B2	S0_SL8_B2	S0_SL3_B3
				S0_SL7_B3	S0_SL8_B3	PB6
				PB10	PB11	S0_SL4_B0
				SE	SE	S0_SL4_B1
						S0_SL4_B2
						S0_SL4_B3
						PB7
						S0_SL5_B0
						S0_SL5_B1
						S0_SL5_B2
						S0_SL5_B3
						PB8

Figure 2-28: Audio_Stream SDP over Main-Link for DST Audio Layout

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
						S0_SL6_B0
						S0_SL6_B1
						S0_SL6_B2
						S0_SL6_B3
						PB9
						S0_SL7_B0
						S0_SL7_B1
						S0_SL7_B2
						S0_SL7_B3
						PB10
						S0_SL8_B0
						S0_SL8_B1
						S0_SL8_B2
						S0_SL8_B3
						PB11
						SE

Figure 2-28: Audio_Stream SDP over Main-Link for DST Audio Layout (Continued)

2.2.5.3.4 Audio_Stream SDP Splitting in SST Transport Format

New to *DP v1.4*.

The HB3 ChannelCount field (bits 2:0) of an Audio_Stream SDP is the count of non-3D LPCM audio or One Bit audio channels transmitted through a DP Main-Link. The DPRX must use this 3-bit value to decide how to interpret the payload of an Audio_Stream SDP. One to eight channels are supported in non-3D LPCM, *IEC 61937*-encoded, or One Bit DisplayPort audio transport.

2.2.5.3.5 Speaker Mapping

Entire section rewritten for *DP v1.4*.

Byte 3 of the Audio INFOFRAME, as defined in *CEA-861-F*, *Section 6.6.2*, contains information that describes the mapping of speaker locations into the audio transport channels. This 8-bit Channel Allocation field, CA 7:0, applies to 3- to 8-channel uncompressed audio. The speaker location mapping of the 3- to 8-channel LPCM audio or 3- to 8-channel One Bit audio data transported must match the 8-bit data (CA7:0) that is transported within the Audio INFOFRAME.

A Sink device can indicate the active speaker configuration through the use of the Speaker Allocation Data Block as described in *CEA-861-F*, *Section 7.5.3*. Sink devices that support 3- to 8-channel LPCM audio or 3- to 8-channel One Bit audio shall include this Data Block.

A Sink device that supports Object-Based Audio or High Channel-Count Audio shall use the Room Configuration Descriptor Data Block as described in *CEA-861.2*, *Table 3*, instead of the Speaker Allocation information. In addition, the Sink device may choose to provide additional information and include Speaker Location Descriptors, as described in *CEA-861.2*, *Table 4*.

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A Source device that needs to transport 3D LPCM audio shall use either the *Delivery According to the Speaker Mask* or *Delivery by Channel Index* method, as described in *CEA-861.2*, *Section 3.6* and *Section 3.7*, respectively. Similar to the 2- or 8-channel layout, all SP bits of the 16- or 32-channel 3D LPCM audio layout must carry the same value, all asserted if the sample is present, or all de-asserted if the sample is not present. The ordering of active LPCM channels within the 32-channel layout shall follow the rules as described in *CEA-861.2*, *Section 3.6*, when the Source device uses the *Delivery According to the Speaker Mask* method, –or– the rules as described in *CEA-861.2*, *Section 3.7*, when the Source device uses the *Delivery by Channel Index* method. When 16 or fewer active channels are required, the 16-channel layout can be used.

Figure 2-29 through Figure 2-32 describe the required channel ordering within the LPCM 16- or 32-channel layout for examples of fully or partially populated 3D LPCM audio systems.

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
–	–	–	–	–	–	FRC	FLC	–	BC	BR	BL	FC	LFE1	FR	FL

Figure 2-29: 3D LPCM Audio Data Allocation with Audio INFOFRAME Byte 4 = FEh, 8.1 SPM Asserted (Informative)

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
–	–	–	–	–	–	–	FRC	FLC	BC	BR	BL	FC	LFE1	FR	FL

Figure 2-30: 3D LPCM Audio Data Allocation with Audio INFOFRAME Byte 4 = FFh, 8.1 SPM Asserted RCD Order Used (Informative)

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Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
LFE2	TpFC	TpFR	TpFL	FRW	FLW	FRC	FLC	TpC	BC	BR	BL	FC	LFE1	FR	FL
Channel Number															
32	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**
–	–	TpRS	TpLS	BtFR	BtFL	TpBR	TpBL	TpSiR	TpSiL	SiR	SiL	BtFC	TpBC	RS	LS

Figure 2-31: 3D LPCM Audio Data Allocation with Audio INFOFRAME Byte 4 = FEh, All SPM Asserted (Informative)

Channel Number															
16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
LS	TpFC	TpC	TpFR	TpFL	FRW	FLW	FRC	FLC	BC	BR	BL	FC	LFE1	FR	FL
Channel Number															
32	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**
–	–	TpRS	TpLS	BtFR	BtFL	BtFC	TpBR	TpBL	TpSiR	TpSiL	SiR	SiL	TpBC	LFE2	RS

Figure 2-32: 3D LPCM Audio Data Allocation with Audio INFOFRAME Byte 4 = FFh, All SPM Asserted RCD Order Used (Informative)

2.2.5.3.6 Data Mapping within Audio_Stream SDP Payload

Entire section rewritten for *DP v1.4*.

An Audio_Stream SDP payload consists of four bytes of data per lane, each four bytes protected by a parity byte.

Figure 2-33 shows the data mapping within the 4-byte payload of an Audio_Stream SDPthat contains data with *IEC 60958*-encoding or *IEC 61937* transport. In these cases, the audio payload would use the 2- or 8-channel layout with LPCM audio or *IEC 61937*-compressed audio, as well as the 16- or 32-channel layout with 3D LPCM audio. In Figure 2-24 and Figure 2-25, these four bytes correspond to, for example, S0_Ch1_B0, S0_Ch1_B1, S0_Ch1_B2, and S0_Ch1_B3. (See Figure 2-24 through Figure 2-27 for the 4-byte payload mapping of the LPCM audio, *IEC 61937*-encoded audio, or 3D LPCM audio within the Audio_Stream SDP over the Main-Link.)

Figure 2-34 shows the data mapping within the 4-byte payload of a One Bit Audio_Stream SDP. This One Bit audio data follows the *IEC 14496-3*, *Subpart 10*, encoding standard. (See Figure 2-24 and Figure 2-25 for the mapping of the 4-byte One Bit audio payload within the Audio_Stream SDP over the Main-Link.)

Figure 2-35 shows the data mapping within each of the eight 4-byte sub-layout payloads of a DST Audio_Stream SDP. This DST audio data also follows the *IEC 14496-3*, *Subpart 10*, encoding standard. (See Figure 2-27 for the mapping of the eight sub-layout payloads of the DST audio within the Audio_Stream SDP over the Main-Link.)

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Figure 2-33: Data Mapping within the 4-Byte Payload of an Audio_Stream SDP with *IEC 60958*-like Coding

Figure 2-34: Data Mapping within the 4-Byte Payload of an Audio_Stream SDP with One Bit Audio Coding

Figure 2-35: Data Mapping within the 4-Byte Payload Sub-layout of a DST Audio_Stream SDP with DST Audio Coding

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Table 2-109 shows the bit definition of the 4-byte Audio_Stream SDP payload shown in Figure 2-33.

Table 2-109: Bit Definition of an Audio_Stream SDP Payload with *IEC 60958*-like Coding

Bit Name	Byte #	Bit #	Description
Audio sample word	0	7:0	**Audio Data** Content of this data depends on the audio coding type. In case of LPCM audio, the most significant bit of the audio is placed in Byte 2, bit 7. If the audio data size is less than 24 bits, unused least significant bits must be zero-padded.
	1	7:0	
	2	7:0	
V	3	0	**Validity Flag**
U		1	**User Bit**
C		2	**Channel Status**
P		3	**Parity Bit**
PR		5:4	**Preamble Code and its Correspondence with *IEC 60958* Preamble** 00 = Subframe 1 and start of the audio block (11101000 preamble). 01 = Subframe 1 (1110010 preamble). 10 = Subframe 2 (1110100 preamble). 11 = RESERVED
R		6	**RESERVED** Must be 0.
SP		7	**Sample Present Bit** 0 = Sample information is not present. 1 = Sample information is present and can be processed. All channels of one audio sample, whether used or unused, must have the same value for this flag. Useful when 2-channel audio is transported over a 4-lane Main-Link. In this operation, Main-Link Lanes 2 and 3 may or may not have the audio sample data. Indicates whether the audio sample is present.

Table 2-110: Bit Definition of an Audio_Stream SDP Payload with One Bit Audio Coding

Bit Name	Byte #	Bit #	Description
Audio sample bitstream	0	7:0	**Audio Data Stream** One Bit audio data consists of a single bit per sample. Each SDP payload layout consists of a 28-bit portion of a continuous stream of 1-bit consecutive samples belonging to the given audio channel. The first sampled bit of the 28-bit portion is placed in Byte 0, bit 0. The last sampled bit of the 28-bit portion is placed in Byte 3, bit 3.
	1	7:0	
	2	7:0	
	3	3:0	

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Table 2-110: Bit Definition of an Audio_Stream SDP Payload with One Bit Audio Coding (Continued)

Bit Name	Byte #	Bit #	Description
F	3	4	**Frame Start Flag** 0 = Setting for all but the first One Bit SDP payload layout in a series of layouts comprising the One Bit audio frame. 1 = Indicates the first One Bit SDP payload layout in a series of layouts comprising the One Bit audio frame. Valid only when the matching Sample Present Bit is set to 1. All channels layouts of the One Bit audio sample must have the same value for this flag.
C		5	**Channel Status** C(0:NLPF - 33) = 0 as RESERVED. C(NLPF-32:NLPF - 2) = GTC(31:1). C(NLPF - 1) = GTC Field Validity. If GTC Field Validity is 0, the Sink device should ignore the GTC. These bits carry channel status, assembled from One Bit Layout Sample 0 to One Bit Layout Sample NLPF, one bit per sample. One Bit Layout Sample 0 is marked with the Frame Start Flag bit set to 1. Valid only when the matching Sample Present Bit is set to 1. All channel layouts of the One Bit audio sample must have the same value for this flag. ***Note:*** • *NLPF = Number of One Bit audio layouts per frame* • *GTC = Global Time Code presentation time*
V		6	**Valid Flag** 0 = Sample information is not valid. 1 = Sample information is valid and can be processed. Valid only when the matching Sample Present Bit is set to 1.
SP		7	**Sample Present Bit** 0 = Sample information is not present. 1 = Sample information is present and can be processed. All channels of one audio sample, whether used or unused, must have the same value for this flag. Useful when 2-channel audio is transported over a 4-lane Main-Link. In this operation, Main-Link Lanes 2 and 3 may or may not have the audio sample data. Indicates whether the audio sample is present.

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Table 2-111: Bit Definition of an Audio_Stream SDP Payload with DST Audio Coding

Bit Name	Byte #	Bit #	Description
Audio sample bitstream	0	7:0	**Audio Data Stream** DST audio data consists of a stream of compressed One Bit audio data. Each of the eight 4-byte sub-layouts of the DST SDP payload layout consists of a 28-bit portion of a continuous stream of the compressed audio data. The first sampled bit of the 28-bit portion is placed in Byte 0, bit 0. The last sampled bit of the 28-bit portion is placed in Byte 3, bit 3. The DST data bitstream is loaded into the eight payload sub-layouts in ascending payload layout order, Sub-layouts 1 to 8.
	1	7:0	
	2	7:0	
	3	3:0	
F	3	4	**Frame Start Flag** 0 = Setting for all but the first DST SDP payload layout in a series of layouts comprising the DST audio frame. 1 = Indicates the first DST SDP payload layout in a series of layouts comprising the DST audio frame. Valid only when the matching Sample Present Bit is set to 1. All eight 4-byte sub-layouts of the DST audio layout must have the same value for this flag.
C		5	**Channel Status** C(0:NLPF-33) = 0 as RESERVED. C(NLPF-32:NLPF-2) = GTC(31:1). C(NLPF-1) = GTC Field Validity. If GTC Field Validity is 0, the Sink device should ignore the GTC. These bits carry channel status, assembled from DST Sub-layout Sample 0 to DST Sub-layout Sample NLPF, one bit per DST sub-layout sample. DST Sub-layout Sample 0 is marked with the Frame Start Flag bit set to 1. Valid only when the matching Sample Present Bit is set to 1. All eight sub-layouts of the DST audio layout must have the same value for this flag. ***Note:*** • *NLPF = Number of DST audio sub-layouts per frame* • *GTC = Global Time Code presentation time*
V		6	**Valid Flag** 0 = Sample information is not valid. 1 = Sample information is valid and can be processed. Valid only when the matching Sample Present Bit is set to 1. All eight sub-layouts of the DST layout must have the same value for this flag.
SP		7	**Sample Present Bit** 0 = Sample information is not present. 1 = Sample information is present and can be processed. All eight sub-layouts of the DST layout must have the same value for this flag. Can be used to mark non-active DST layouts in long packet sequences.

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2.2.5.3.7 Audio_Stream SDP Transport Capacity and Video Dependency (Informative)

New to *DP v1.4*.

DP v1.4 supports the transport of an audio stream while a video stream is being transported over the link.

Audio_Stream SDPs are sent during the horizontal and vertical blanking periods of the main video stream. The audio bandwidth requirement can be expressed in terms of the required audio sample rate and the main video line rate, as follows:

AudioSamplesReqPerLine = AudioFs / VideoHFreq

where:

- *AudioFs* is the desired audio sample frequency as listed in Table 2-100
- VideoHFreq is the horizontal line frequency of the main video stream

During the vertical blanking period, Audio_Stream SDPs can appear at any time during the entire line period. The bandwidth consumed by the other SDPs that could occupy the vertical blanking period does not practically constrain the audio samples per line requirement within that period.

However, the horizontal blanking period's available capacity will determine whether the audio bandwidth requirement can be met. Because no other SDP is required to occupy the horizontal blanking region, only the required Audio_Stream SDP size needs to be compared against the available Hblank symbol capacity to determine whether a particular audio mode can be supported.

The number of symbols available for the Audio_Stream SDP during the Hblank period depends on the main video stream timing and Main-Link configuration, specifically the Link Symbol Clock Frequency and Lane Count. The number of Audio_Stream SDP symbols required per line and per Hblank is determined by the Audio Coding Type and related layouts per sample and symbols per layout. Concatenating the audio layouts within a single SDP will increase efficiency by reducing the overhead for SDP header and SE footer symbols. Splitting the SDP across more than one line and Hblank will increase efficiency by avoiding the requirement of rounding up to the next integer number of layouts per line. However, even with these efficiency measures, there may be some main video stream mode and audio mode combinations that will have a restricted maximum audio sample rate. This maximum audio sample rate could be determined by comparing the available horizontal blanking period symbol capacity against the required audio SDP symbol count for each sample frequency. Video modes that reduce link rates that use options such as reduced blanking timing and/or the MSA Video Horizontal Blanking Expansion option should be analyzed for any audio mode restrictions.

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The number of symbols available for an Audio_Stream SDP during the horizontal blanking period is as follows:

*StrmSymbolCntAvailPerHblank = FLOOR(t_HBlank * LSClkFreq * LaneCnt - MainLinkOverhead)*

where:

- *t_HBlank* is the main video stream horizontal blanking period
- *LSClkFreq* is the Link Symbol Clock frequency
- *LaneCnt* is the Main-Link's lane count
- *MainLinkOverhead* is the symbol count required on the Main-Link at the beginning and end of the horizontal blanking period, and is defined as follows:

  MainLinkOverhead = BSSymbolCnt + VBIDSymbolCnt + MvidSymbolCnt + MaudSymbolCnt + BESymbolCnt

  where:

  - *BSSymbolCnt* is equal to *LaneCnt* * 4, the number of Blanking Start symbols; Enhanced Framing mode provides the worst case number
  - *VBIDSymbolCnt* is equal to 4, the number of VB-ID symbols
  - *MvidSymbolCnt* is equal to 4, the number of Mvid symbols
  - *MaudSymbolCnt* is equal to 4, the number of Maud symbols
  - *BESymbolCnt = LaneCnt*, the number of Blanking End symbols

  Using the above definitions, the Main-Link overhead can be simplified as follows:

  *MainLinkOverhead = LaneCnt * 5 + 12*

The number of symbols required for an Audio_Stream SDP during the horizontal blanking period is as follows:

AudioSymbolCntReqPerHblank = `ceil((AudioSamplesReqPerLine * AudioLayoutsPerSample * AudioSymbolsPerLayout + ceil(AudioSamplesReqPerLine * AudioLayoutsPerSample / MaxLayoutsPerAudioSDP) * AudioSDPOverhead) * AudioSDPMargin)`

where:

- *AudioSamplesReqPerLine* is the number of audio samples that must be transported on each main video line to meet the audio sample rate requirements
- *AudioLayoutsPerSample* is the number of audio layouts required per audio sample for the given audio mode (see Table 2-112)
- *AudioSymbolsPerLayout* is the number of symbols required per audio layout for the given audio mode (see Table 2-112)
- *MaxLayoutsPerAudioSDP* is the maximum number of audio layouts that can be assembled into a single Audio_Stream SDP (see Table 2-112)

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- *AudioSDPMargin* is an implementation-specific safety margin that is used to prevent possible audio sample underrun; recommended values of 1.05 to 1.1 can be used
- *AudioSDPOverhead* is the symbol count required at the beginning and end of the Audio_Stream SDP, and is defined as follows:

  AudioSDPOverhead = SSSymbolCnt + HeaderSymbolCnt + HeaderParitySymbolCnt + SESymbolCnt

where:

- *SSSymbolCnt = LaneCnt*, the number of Audio_Stream SDP Start symbols
- *HeaderSymbolCnt* is equal to 4, the number of Audio_Stream SDP Header symbols
- *HeaderParitySymbolCnt* is equal to 4, the number of Audio_Stream SDP Header Parity symbols
- *SESymbolCnt = LaneCnt*, the number of Audio_Stream SDP End symbols

Using the above definitions, the Audio_Stream SDP overhead can be simplified as follows:

*AudioSDPOverhead = LaneCnt * 2 + 8*

Table 2-112 summarizes the supported audio mode conversion details:

- Samples to layouts
- Layouts to symbols
- Maximum layouts allowed within a single Audio_Stream SDP

Table 2-112: Summary of Audio_Stream SDP Coding Type Payload Capacity (Informative)

Audio Coding Type	AudioLayoutsPerSample	AudioSymbolsPerLayout	MaxLayoutsPerAudioSDP
2-channel LPCM	1/2	20	16
8-channel LPCM	1	40	32
16-channel 3D LPCM	1	80	32
32-channel 3D LPCM	1	160	32
2-channel One Bit	1/56	20.2	16
8-channel One Bit	1/28	40	32
DST	1/224	40	32
HBR	1/4.2	40	32

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Main video mode and audio combinations that meet the following requirements can be supported as follows:

AudioSymbolCntReqPerHblank < *StrmSymbolCntAvailPerHblank*

Consider the limitations of 32-channel 3D LPCM audio support on the 4096x2160p60 video mode with Reduced Blanking v2 timing, DMT ID = 57h. The relevant details of this video mode with two Main-Link configurations are as follows:

- Horizontal Line Frequency = *VideoHFreq* = 133.32kHz
- Horizontal Blanking Period = *t_HBlank* = 0.1436925us
- Details for 4-Lane at 540MHz Link Symbol Clock Frequency, 24bpp RGB:

  StrmSymbolCntAvailPerHblank = `floor(t_HBlank * LSClkFreq * LaneCnt - MainLinkOverhead)` = `floor(0.1436925us * 540MHz * 4 - (4 * 5 + 12))` = *278 symbols*

- Details for 4-Lane at 270MHz Link Symbol Clock Frequency, 12bpp 4:2:0 YCbCr:

  StrmSymbolCntAvailPerHblank = `floor(t_HBlank * LSClkFreq * LaneCnt - MainLinkOverhead)` = `floor(0.1436925us * 270MHz * 4 - (4 * 5 + 12))` = *123 symbols*

Table 2-113 lists relevant details for 32-channel 3D LPCM required audio support for the seven available sample frequencies. A 110% margin was used for *AudioSDPMargin*.

Table 2-113: 32-channel 3D LPCM Audio Requirements on DMT = 57h Mode (Informative)

AudioFs	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
AudioSamplesReqPerLine	0.24	0.33	0.36	0.66	0.72	1.32	1.44
AudioSymbolCntReqPerHblank	60	76	81	135	145	251	272

Considering that 278 symbols should be available during the horizontal blanking period that uses the 4-Lane 540MHz configuration, all Audio sample frequencies up to 192kHz should be supported. However, with only 123 symbols available in the 4-Lane 270MHz configuration, only 32, 44.1, and 48kHz 32-channel audio sample rates can be supported. There is insufficient Hblank capacity to support 88.2, 96, 176.4, and 192kHz audio sample frequencies in this configuration.

2.2.5.3.8 Transport of Audio Packets without Main Video Stream

The DisplayPort Standard supports the transport of audio stream while no video stream is being transported over the link.

When the link is active without a main video stream, a Source device must insert a BS symbol followed by VB-ID, Mvid7:0, and Maud7:0, referred to as "BS symbol set," every 2^{13}, or 8192 link symbols.

Both the NoVideoStream_Flag and VerticalBlanking_Flag bits in the VB-ID (bits 3 and 0, respectively) must be set to 1 in this condition and Mvid7:0 is cleared to 00h.

A Source device must transmit an Audio_Stream SDP after each BS symbol set. In addition, a Source device must insert an Audio INFOFRAME SDP and Audio_TimeStamp SDP once after every 512th BS symbol set.

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2.2.5.4 Audio_CopyManagement SDP

Transport of an Audio_CopyManagement SDP is an application-specific option. When an audio stream is transported and it has a specific copy management requirement from the higher level application, the Audio_CopyManagement SDP describing the copy management attribute of the audio stream must also be transported. For general audio stream that has no copy management requirement, transmission of the Audio_CopyManagement SDP is optional (with HB3 Copy Management Type field (bits 7:2) cleared to 00h if sent).

A DP Sink device may indicate it does not support ACM or ISRC by clearing the ACM_ISRC_sup bit in its capability declaration. In this case, the DP Source device must not send any Audio_CopyManagement SDP to the Sink device (on top of not sending any audio stream with copy management requirement to the Sink device). If the DP Sink device supports Audio_CopyManagement, and does not see the Audio_CopyManagement SDP within two video frames after audio stream is transported, it must treat the audio stream transported has no copy management requirement.

A DP Source device must support Audio_CopyManagement SDP transmission if enabled by higher-level application (unless the Sink device does not support ACM/ISRC).

When a new audio stream with copy management requirement is transported, or if there is any change in the audio stream copy management requirements, an Audio_CopyManagement SDP with up-to-date information must be transmitted within one frame of the start of transmission of the affected audio stream. The packet must continue to be sent once per frame, for as long as the copy management requirement persists.

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2.2.5.4.1 Audio_CopyManagement SDP Header

Table 2-114 describes the header bytes of an Audio_CopyManagement SDP.

Table 2-114: Header Bytes of Audio_CopyManagement SDP

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP must have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	05h
HB2	7:0	**Least Significant Eight bits of (Data Byte Count - 1)** For an Audio_CopyManagement SDP, the value must be 0Fh (i.e., Data Byte Count = 16 bytes). Unused bytes must be zero-padded.
HB3	1:0	**Most Significant 2 Bits of (Data Byte Count - 1)**
	7:2	**Copy Management Type** Indicates the type of copy management associated with the audio stream. 000000 = No Copy Management requirement is indicated by the higher-level application, Equivalent to no transmission of the Audio_CopyManagement SDP. 000001 = *IEC 60958* Audio. Copy management is required through *IEC 60958* Serial Copy Management System (SCMS) control bits, which are embedded in the audio stream channel status. 000010 = DVD Audio. DVD audio copy management is required. See DVD Specifications for Read-Only Disc, Part 4: Audio Specification, Version 1.2, for details regarding the copy control attributes in the data payload. All other values are RESERVED.

2.2.5.4.2 Audio_CopyManagement SDP Data

The data payload of the Audio_CopyManagement SDP depends on the HB3 Copy Management Type field (bits 7:2) value:

- Copy Management Type = No Copy Management – No valid data. All 16 bytes are 0s.
- Copy Management Type = *IEC 60958* Audio – No valid data. All 16 bytes are 0s.
- Copy Management Type = DVD Audio – 1 byte of data content exists, with the remaining 15 bytes padded with 0s. See DVD Specifications for Read-Only Disc, Part 4: Audio Specification, Version 1.2, for details of the copy control attributes in the data content.
    - Bit 1:0 – Audio quality
    - Bit 3:2 – Audio copy permission
    - Bit 6:4 – Audio copy number
    - Bit 7 – Audio transaction

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Figure 2-36 shows the payload size equal to 16 bytes. It is allowed to have the payload size equal to 32 bytes, with unused bytes zero-padded.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB8
						SE

Figure 2-36: Audio_CopyManagement SDP over the Main-Link

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2.2.5.5 International Standard Recording Code SDP

Transport of an International Standard Recording Code (ISRC) SDP is an application-specific option. When an audio stream is transported and it has specific ISRC and/or UPC/EAN requirement from the higher level application, the ISRC SDP describing the UPC_EAN_ISRC information of the audio stream must also be transported. For general audio stream that has no ISRC or UPC/EAN requirement, no ISRC SDP will be sent.

A DP Sink device may indicate it does not support ACM or ISRC by clearing the ACM_ISRC_sup bit in its capability declaration. In this case, the DP Source device must not send any ISRC SDP to the Sink device (on top of not sending any audio stream with ISRC requirement to the Sink device). If the DP Sink device supports ISRC, and does not see the ISRC SDP within two frames after audio stream is transported, it shall treat the audio stream transported has no ISRC requirement.

A DP Source device must support ISRC SDP transmission if enabled by higher-level application (unless the Sink device does not support ACM/ISRC). When an audio track with ISRC information is transported, the ISRC SDP must be transmitted multiple times (see the ISRC status description for further details) following the transmission of the affected audio track. If transported, ISRC SDPs must be sent during both horizontal and vertical blanking periods of the main video stream.

See DVD Specifications for Read-Only Disc, Part 4: Audio Specification, Version 1.2, for details of the UPC_EAN_ISRC fields.

2.2.5.5.1 ISRC SDP Header

Table 2-115 describes the header bytes of an ISRC SDP.

Table 2-115: Header Bytes of ISRC SDP

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID** INFOFRAME SDP, Audio_TimeStamp SDP, Audio_Stream SDP, Audio_CopyManagement SDP, and ISRC SDP must have the same Packet ID when they are associated with the same audio stream.
HB1	7:0	06h
HB2	7:0	**Least Significant Eight bits of (Data Byte Count - 1)** For an ISRC SDP, the value must be 0Fh (i.e., Data Byte Count = 16 bytes).

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Table 2-115: Header Bytes of ISRC SDP (Continued)

Byte #	Bit #	Content
HB3	1:0	**Most Significant 2 Bits of (Data Byte Count - 1)**
	2	**ISRC Type** Indicates whether the ISRC information is delivered in a single ISRC SDP or two ISRC SDPs. A complete set of UPC_EAN_ISRC information can be sent in one or two ISRC SDPs. 0 = UPC_EAN_ISRC information has only 16 bytes; therefore, only a single SDP is sent. 1 = UPC_EAN_ISRC information has the full 32 bytes; therefore, two ISRC SDPs are required to be sent. ***Note:*** *SDP size limitation was kept mainly to ease DP-to-HDMI transport protocol converter device implementation.*
	3	**ISRC SDP #** Indicates the packet number if the ISRC information is to be sent in two ISRC SDPs (i.e., ISRC Type bit is set to 1). Always cleared to 0 if the ISRC Type bit is cleared to 0. 0 = ISRC SDP contains the first 16 bytes (15:0) of the UPC_EAN_ISRC information. 1 = ISRC SDP contains the second 16 bytes (31:16) of the UPC_EAN_ISRC information.
	4	**ISRC Valid** Indicates the UPC_EAN_ISRC information contained within the ISRC SDP is valid. 0 = Source device cannot obtain the complete UPC_EAN_ISRC information. 1 = ISRC information is complete and valid.
	7:5	**ISRC Status** Indicates status of the ISRC information in reference to an audio track position. Each track of audio may have the specific ISRC and/or UPC/EAN information. Per DVD Audio specification, if UPC_EAN_ISRC information exists, the DP Source device must send the set of ISRC SDPs multiple times per audio track: • At least two complete sets of ISRC SDPs with the ISRC Status of 000 at the beginning of the audio track. • Multiple complete set of ISRC SDPs with the ISRC Status of 010 in the middle of the audio track. • At least two complete sets of ISRC SDPs with the ISRC Status of 100 before the end of the audio track.

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2.2.5.5.2 ISRC SDP Data

The ISRC SDP data payload depends on the HB3 ISRC Type bit (bit 2):

- If the HB3 ISRC SDP # bit (bit 3) of an ISRC SDP is cleared to 0, the data payload contains bytes 15:0 of the UPC_EAN_ISRC information.
- If the HB3 ISRC SDP # bit (bit 3) of an ISRC SDP is set to 1, the data payload contains bytes 31:0 of the UPC_EAN_ISRC information.

Figure 2-37 shows the payload size equal to 16 bytes. It is allowed to have the payload size equal to 32 bytes, with unused bytes zero-padded.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB8
						SE

Figure 2-37: ISRC SDP over the Main-Link

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2.2.5.6 Video_Stream_Configuration SDP

When a DP Sink device has a DPCD r1.2 or higher and stereoscopic 3D rendering capability (as expressed in EDID), a DP Source device may send 3D Stereo in-band signaling using a VSC SDP by clearing the MSA packet MISC1 field, bits 2:1, to 00. When a DP Sink device has its VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 3) set to 1, a DP Source device may send Pixel Encoding/Colorimetry Format indication using a VSC by setting MISC1 field, bit 6, to 1. Besides checking the VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED bit, the DP Source device must also read the DP Sink device's supported pixel encoding and colorimetry formats by reading EDID, and must select the format supported by the DP Sink device.

For an eDP interface, a VSC SDP may also be used to communicate Panel Self Refresh (PSR) control. Both a VSC rev 1 SDP and a VSC rev 2 SDP, as identified by HB2 in Table 2-116, carry the 3D Stereo in-band signaling within Byte 0 (DB0) of the SDP payload. A VSC rev 2 SDP has seven additional payload bytes to carry the PSR control information. Details of these additional VSC rev 2 SDPs are described in *eDP v1.4b*. When non-stereo video is being sent by the Source device, this can be indicated by setting DB0 to 0h. (See Table 2-117.)

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2.2.5.6.1 VSC SDP Header

Table 2-116 describes the header bytes of the VSC SDP.

Table 2-116: Header Bytes of VSC SDP

Byte #	Bit #	Content
HB0	7:0	**Secondary-Data Packet ID = 0**
HB1	7:0	07h
HB2	4:0	**Revision Number** 01h = VSC SDP supporting 3D stereo only. 02h = VSC SDP supporting 3D stereo and PSR (applies to eDP v1.3 and higher). 03h = VSC SDP supporting 3D stereo and PSR2 (applies to eDP v1.4 and higher). 04h = RESERVED for PSR2 use extension (applies to eDP v1.4 and higher). 05h = VSC SDP supporting 3D stereo, PSR2, and Pixel Encoding/ Colorimetry Format indication. A DP Source device is allowed to indicate the pixel encoding/colorimetry format to the DP Sink device with VSC SDP only when the DP Sink device supports it (i.e., VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 3) is set to 1). All other values are RESERVED.
	7:5	**RESERVED** Read all 0s.
HB3	4:0	**Number of Valid Data Bytes** 01h = VSC SDP supporting 3D stereo only (HB2 = 01h). 08h = VSC packet supporting 3D stereo + PSR (HB2 = 02h). 0Ch = VSC SDP supporting 3D stereo + PSR2 (HB2 = 03h). 13h = VSC SDP supporting 3D stereo, + PSR2, + Pixel Encoding/ Colorimetry Format indication (HB2 = 05h).
	7:5	**RESERVED** Read all 0s.

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2.2.5.6.2 VSC SDP Payload for 3D Stereo

Table 2-117 shows the bit definitions of Byte 0 (DB0) for a VSC SDP payload. The bit definitions for Data Byte 0 (DB0) are the same for VSC rev 1 (HB2 = 01h) through Rev 5 (HB2 = 05h) SDP.

Table 2-117: VSC SDP Payload DB0

DB0, bits 3:0 = Stereo Interface Method Code	DB0, bits 7:4 = Stereo Interface Method-Specific Parameter
0 = Non Stereo Video	Must be cleared to 0x0.
1 = Frame/Field Sequential	**Frame/Field Sequential Type** **Value 0x0:** Left and Right view indication based on the MISC1 field, bits 2:1. **Value 0x1:** Right when Stereo Signal = 1 **Value 0x2:** Left when Stereo Signal = 1 All other values for this field (0x3-0xF) are RESERVED for future use. ***Note:*** *Stereo Signal refers to an out-of-band signaling, indicating the left and right frame and can be conveyed using VESA stereo connector or some other equivalent means.*
2 = Stacked Frame	**Stacked Frame Type** **Value 0x0:** Left view is on top and right view on bottom. All other values for this field (0x1-0xF) are RESERVED for future use.

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Table 2-117: VSC SDP Payload DB0 (Continued)

DB0, bits 3:0 = Stereo Interface Method Code	DB0, bits 7:4 = Stereo Interface Method-Specific Parameter
3 = Pixel Interleaved	**Interleave Pattern Type** For interleave pattern types 1 through 4, a 2x2 pattern grid (as shown in **Figure 2**) is used to illustrate the interleaving pattern of the composited stereo frame. **Value 0x0:** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below. **Value 0x1:** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below. **Value 0x2:** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below.

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Table 2-117: VSC SDP Payload DB0 (Continued)

DB0, bits 3:0 = Stereo Interface Method Code	DB0, bits 7:4 = Stereo Interface Method-Specific Parameter
3 = Pixel Interleaved (continued)	**Value 0x3:** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below. **Value 0x4:** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below. All other values for this field (0x5-0xF) are RESERVED for future use.
4 = Side-by-side	**Value 0x0:** A value of 0x0 indicate left half of the image represents left EYE view and right half represents right EYE view **Value 0x1:** A value of 0x1 indicate left half of the image represents right EYE view and right half represents left EYE view All other values for this field (0x2-0xF) are RESERVED for future use.
Values 0x5-0xF	RESERVED

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Figure 2-38 shows the pixel pattern representation for Pixel Interleaved method.

Figure 2-38: Pixel Pattern Representation for Pixel Interleaved Method

Figure 2-39 shows the interleave pattern corresponding to 2-way interleaved stereo where right image pixels are on even lines.

Figure 2-39: Interleave Pattern Corresponding to 2-way Interleaved Stereo where Right Image Pixels are on Even Lines

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Figure 2-40 shows the interleave pattern corresponding to a checkerboard pattern with alternating left and right image pixels.

Figure 2-40: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels

Figure 2-41 shows side-by-side stereo format with left view followed by right view.

Figure 2-41: Side-by-Side Stereo Format with Left View followed by Right View

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Figure 2-42 shows field sequential stereo format with left view and right view indicated, via the MISC1 field, bits 2:1, of the MSA packet.

Figure 2-42: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 Field, bits 2:1, of the MSA

Figure 2-43 shows stacked top, bottom stereo format with left view on top and right view on bottom.

Figure 2-43: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom

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Figure 2-44 shows the VSC SDP mapping over Main-Link with the payload size equal to 16 bytes. It is allowed to have the payload size equal to 32 bytes, with unused bytes zero-padded.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB8
						SE

Figure 2-44: VSC SDP over the Main-Link

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2.2.5.6.3 VSC SDP Payload for PSR2

See *eDP v1.4b*.

2.2.5.6.4 VSC SDP Payload for Pixel Encoding/Colorimetry Format

Table 2-118 shows the bit definitions of DB16 through DB18 of the VSC SDP for Pixel Encoding and Colorimetry Format indication.

Table 2-118: VSC SDP Payload for DB16 through DB18

VSC Byte Offset	Value								Description/Format
	7	6	5	4	3	2	1	0	
10h = DB16	**Pixel Encoding and Colorimetry Formats**								
	RGB = 0h				RGB				
					0h				sRGB
					1h				RGB wide gamut fixed point
					2h				RGB wide gamut floating point (scRGB)
					3h				AdobeRGB
					4h				DCI-P3
					5h				Custom Color Profile
					6h				ITU-R BT.2020 R'G'B'
					7h – Fh				RESERVED
	YCbCr 444 = 1h				YCbCr 444				
					0h				ITU-R BT.601
					1h				ITU-R BT.709
					2h				$xvYCC_{601}$
					3h				$xvYCC_{709}$
					4h				$sYCC_{601}$
					5h				$Adobe_{YCC601}$
					6h				ITU-R BT.2020 $Y'_C C'_{BC} C'_{RC}$
					7h				ITU-R BT.2020 $Y'C'_B C'_R$
					8h – Fh				RESERVED

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Table 2-118: VSC SDP Payload for DB16 through DB18 (Continued)

VSC Byte Offset	Value								Description/Format
	7	6	5	4	3	2	1	0	
10h = DB16	**Pixel Encoding and Colorimetry Formats (Continued)**								
	YCbCr 422 = 2h				YCbCr 422				
					0h				ITU-R BT.601
					1h				ITU-R BT.709
					2h				$xvYCC_{601}$
					3h				$xvYCC_{709}$
					4h				$sYCC_{601}$
					5h				$Adobe_{YCC601}$
					6h				ITU-R BT.2020 $Y'_CC'_{BC}C'_{RC}$
					7h				ITU-R BT.2020 $Y'C'_BC'_R$
					8h – Fh				RESERVED
	YCbCr 420 = 3h				YCbCr 420				
					0h				ITU-R BT.601
					1h				ITU-R BT.709
					2h				$xvYCC_{601}$
					3h				$xvYCC_{709}$
					4h				$sYCC_{601}$
					5h				$Adobe_{YCC601}$
					6h				ITU-R BT.2020 $Y'_CC'_{BC}C'_{RC}$
					7h				ITU-R BT.2020 $Y'C'_BC'_R$
					8h – Fh				RESERVED
	Y Only = 4h				Y Only				
					0h				DICOM Part 14 Grayscale Display Function
					1h – Fh				RESERVED
	RAW = 5h				RAW				
					0h				Custom Color Profile
					1h – Fh				RESERVED
	RESERVED = 6h – Fh				–				RESERVED

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Table 2-118: VSC SDP Payload for DB16 through DB18 (Continued)

VSC Byte Offset	Value								Description/Format
	7	6	5	4	3	2	1	0	
11h = DB17	**Dynamic Range and Component Bit Depth**								
	0, 1	–							**Dynamic Range** (Bit 7) 0 = VESA range 1 = CEA range
	–	0h				–			**RESERVED** (Bit 6:3)
	–					0h – 7h			**Component Bit Depth Type** (Bits 2:0) Possible Component Bit Depth values are dependent on the encoding format and colorimetry.
	–					0h – 4h			For pixel encoding format RGB, the following Component Bit Depth values are defined: 0 = 6bpc 1 = 8bpc 2 = 10bpc 3 = 12bpc 4 = 16bpc All other values are RESERVED.
	–					1h – 4h			For pixel encoding formats YCbCr444, YCbCr422, YCbCr420, and Y Only, the following Component Bit Depth values are defined: 1 = 8bpc 2 = 10bpc 3 = 12bpc 4 = 16bpc All other values are RESERVED.
	–					0h – 4h			For pixel encoding format RAW, the following Component Bit Depth values are defined: 0 = RESERVED 1 = 6bpc 2 = 7bpc 3 = 8bpc 4 = 10bpc 5 = 12bpc 6 = 14bpc 7 = 16bpc

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Table 2-118: VSC SDP Payload for DB16 through DB18 (Continued)

VSC Byte Offset	Value								Description/Format
	7	6	5	4	3	2	1	0	
12h = DB18	**Content Type**								
	0h				0	–			**RESERVED** (Bit 7:3)
	–					0h – 7h			**Content Type** (Bits 2:0) 0 = Not defined. 1 = Graphics. 2 = Photo. 3 = Video. 4 = Game. All other values are RESERVED. ***Note:*** *See CEA-861-F for the definition and expected processing by a stream sink for the above content types.*

2.2.5.7 Extension SDP

The transport of an Extension SDP is an application- or vendor-specific option. A DP Source device must write its 24-bit IEEE_OUI (Organizational Unique ID) registers (DPCD Addresses 00300h through 00302h) (and additional data, as needed), via the AUX transactions. Then, it must read the 24-bit IEEE_OUI registers (DPCD Addresses 00400h through 00402h) (and additional data, as needed) of the Sink device, via the AUX CH. Support of the 24-bit ID is mandatory. If the downstream device is a Branch device, the IEEE OUI registers are located at DPCD Addresses 00500h through 00502h.

Extension SDP must be used only after a DP Source and Sink device have both confirmed that they support the vendor-specific Extension SDP usage.

A Branch device must forward the AUX CH write or read request transactions for the 24-bit IEEE OUI to its downstream device.

Figure 2-45 shows the minimum size of an Extension SDP mapped onto Main-Link. The DP Source device must generate parity bytes for both the header and data. Use of parity for error checking and correction by the DP Sink device is an implementation-specific option.

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4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
SE	SE	SE	SE	DB3	DB7	PB3
				PB4	PB5	DB0
				DB8	DB12	DB1
				DB9	DB13	DB2
				DB10	DB14	DB3
				DB11	DB15	PB4
				PB6	PB7	DB4
				SE	SE	DB5
						DB6
						DB7
						PB5
						…
						DB12
						DB13
						DB14
						DB15
						PB8
						SE

Figure 2-45: Extension SDP Mapping over the Main-Link

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2.2.5.7.1 Extension SDP Header

Table 2-119 summarizes the header bytes of an Extension SDP.

Table 2-119: Header Bytes of an Extension SDP

Byte#	Content
HB0	Usage of this byte is vendor-specific
HB1	04h
HB2	Usage of this byte is vendor-specific
HB3	Usage of this byte is vendor-specific

2.2.5.8 Camera SDP

The SDP type values of 08h through 0Fh must be reserved for vendor-specific camera application use.

2.2.5.8.1 Camera SDP Header

The SDP header for camera applications shall be defined as listed in Table 2-120.

Table 2-120: Header Bytes of a Camera SDP

Byte	Content
HB0	**Secondary-Data Packet ID**
HB1	**SDP Type** Valid values are 08h through 0Fh, which must be reserved for vendor-specific camera application use
HB2	Usage of this byte is vendor-specific
HB3	Usage of this byte is vendor-specific

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The Camera SDP payload contains the vendor-specific auxiliary data of the frame's main video stream. Figure 2-46 lists the Main-Link mappings of the header and data payloads.

4-Lane Main-Link				2-Lane Main-Link		1-Lane Main-Link
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 0**	**Lane 1**	**Lane 0**
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
DB0	DB4	DB8	DB12	HB2	HB3	HB1
DB1	DB5	DB9	DB13	PB2	PB3	PB1
DB2	DB6	DB10	DB14	DB0	DB4	HB2
DB3	DB7	DB11	DB15	DB1	DB5	PB2
PB4	PB5	PB6	PB7	DB2	DB6	HB3
…	…	…	…	DB3	DB7	PB3
DBN-16	DBN-12	DBN-8	DBN-4	PB4	PB5	DB0
DBN-15	DBN-11	DBN-7	DBN-3	…	…	DB1
DBN-14	DBN-10	DBN-6	DBN-2	DBN-8	DBN-4	DB2
DBN-13	DBN-9	DBN-5	DBN-1	DBN-7	DBN-3	DB3
PBN/4	PBN/4+1	PBN/4+2	PBN/4+3	DBN-6	DBN-2	PB4
SE	SE	SE	SE	DBN-5	DBN-1	…
				PBN/4+2	PBN/4+3	DBN-4
				SE	SE	DBN-3
						DBN-2
						DBN-1
						PBN/4-3
						SE

Figure 2-46: Camera SDP Mapping over the Main-Link

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2.2.5.8.2 Camera SDP Transport (Informative)

A video stream comprising RAW data is framed identically to any other rasterized video, using vertical blanking periods, horizontal blanking periods and active video periods, and transported using Single-stream Transport (SST) format, –or– as a stream within Multi-stream Transport (MST) format. MSA and related SDPs (if needed) shall be transported during the blanking period(s).

Camera SDPs can be transmitted with or without the presence of a main video stream. Figure 2-47 illustrates the transport timing of Camera RAW active pixels (main video stream) and Camera SDPs.

Figure 2-47: Camera RAW Active Pixels (Main Video Stream) and Camera SDP Transport

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2.2.5.9 Picture Parameter Set SDP

Support for the Picture Parameter Set Secondary-data Packet (PPS SDP) is new to *DP v1.4*.

The PPS is defined within the PPS syntax definition in *DSC v1.2*, *Annex E*. The PPS is sent using the SDP format over the Main-Link during the vertical blanking interval. The Sink device uses the last PPS transmitted before the BS symbol sequence of the scan line prior to where the active region starts, as illustrated in Figure 2-48. The compression parameters may be changed in between compressed frames by transmitting a new PPS. The PPS applies to all subsequent pictures until another PPS is sent. The Sink device will retain the most-recent PPS until the Decompression Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) is cleared to 0.

It is recommended that the encoder and decoder use the PPS values specified in *DSC v1.2*, *Table E-2*.

Figure 2-48: PPS Timing

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2.2.5.9.1 PPS SDP Header and Payload Bytes

Table 2-121 defines the PPS SDP header bytes. Figure 2-49 illustrates the PPS SDP over the Main-Link in 4-, 2-, and 1-lane configuration payload bytes.

Table 2-121: PPS SDP Header Bytes – HB0 through HB3

Byte #	Bit #	Content
HB0	7:0	Secondary Data Packet ID = 0.
HB1	7:0	Secondary Data Packet Type = 10h.
HB2	7:0	Number of Payload Data Bytes - 1 = 7Fh.
HB3	7:0	**RESERVED** Read all 0s.

Figure 2-49: PPS SDP Payload Layout

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2.2.5.10 Video Stream Configuration Extension VESA SDP

Support for Video Stream Configuration Extension VESA (VSC_EXT_VESA) is new to *DP v1.4*.

The VSC_EXT_VESA SDP allows a DP Source device to send video stream-related metadata aligned with the stream. The VSC_EXT_VESA SDP chaining framework enables a flexible metadata transportation framework that can handle transport of a few bytes of payload, using a single VSC_EXT_VESA SDP to up 2KB (and beyond), by chaining multiple VSC_EXT_VESA SDPs per video frame.

A single VSC_EXT_VESA SDP is composed of four header bytes and 32 payload bytes. *DP v1.4* (and higher) defines the header bytes and the associated fields; the payload may be defined within *DP v1.4* (and higher) or by other standards organizations for specific feature support.

The VSC_EXT_VESA SDP is mainly intended for carrying non-CEA-defined header-related metadata that describes the header stream content attributes; however, the same framework can be used for other purposes when large payload data must be transported.

Figure 2-50 describes the VSC_EXT_VESA SDP chaining and metadata transport framework. The framework is composed of a flag that indicates whether any additional VSC_EXT_VESA SDPs are to follow as part of the SDP header bytes. The VSC_EXT_VESA SDP header bytes also include a flag indicating whether the header's Packet Sequence field is being sequentially incremented, starting from 0, as part of the VSC_EXT_VESA SDP chaining framework. The metadata transport framework also allows the DP Sink device to expose supported payload types and associated setup time requirements, explicitly or implicitly, in EDID/DisplayID and it is required that the DP Source device shall transmit all VSC_EXT_VESA SDPs, thereby ensuring that the DP Sink device setup time requirement is met.

As shown in Figure 2-50, within a single DP frame, the VSC_EXT_VESA SDP framework allows Frame *N*'s metadata to be transported before the setup time and Frame *N*+1's metadata to be transported as early as the first horizontal blank after BE.

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x = VESA or CEA (i.e., VSC_EXT_*x* is VSC_EXT_VESA or VSC_EXT_CEA, depending on the SDP type)

Figure 2-50: VSC_EXT_VESA SDP Framework

When a DP Sink device has a DPCD r1.4 (or higher) and its VSC_EXT_VESA_SDP_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 4) set to 1, a DP Source device may send stream metadata using a single VSC_EXT_VESA SDP framework for the supported payload type exposed in EDID and/or DisplayID by the DP Sink device.

If a DP Sink device, in addition to setting the VSC_EXT_VESA_SDP_SUPPORTED bit, also sets the VSC_EXT_VESA_SDP_CHAINING_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 5) to 1, a DP Source device may send stream metadata using multiple VSC_EXT_VESA SDPs that chain framework for the supported payload type exposed in EDID and/or DisplayID by the DP Sink device.

A DP Sink device that supports VSC_EXT_VESA SDP chaining shall support chaining of up to 64 SDPs equal to 2KB in size. A DP Sink device that supports the chaining of VSC_EXT_VESA SDPs beyond 64 shall indicate the number (count) that exceeds 64 in the VSC_EXT_VESA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_VESA_SDP_MAX_CHAINING register (DPCD Address 02212h, bits 7:0). If a DP Sink device supports the chaining of the maximum of 96 SDPs, the device shall program the VSC_EXT_VESA_SDP_MAX_CHAINING register to the value of 32 decimal (20h).

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2.2.5.10.1 VSC_EXT_VESA and VSC_EXT_CEA SDP Header and Payload Bytes

Table 2-122 describes the VSC_EXT_VESA and VSC_EXT_CEA SDP header bytes.
Table 2-123 describes the VSC_EXT_VESA and VSC_EXT_CEA SDP payload bytes (actual payload is dependent on the payload type).

Table 2-122: VSC_EXT_VESA and VSC_EXT_CEA SDP Header Bytes – HB0 through HB3

Byte #	Bit #	Content
HB0	7:0	**Secondary Data Packet ID** Specific to stream (usually 00h).
HB1	7:0	**Secondary Data Packet Type** 20h = VESA. 21h = CEA.
HB2	1:0	**VSC_EXT_VESA SDP Framework Version.** Cleared to 0s.
	5:2	**RESERVED** Read all 0s.
	6	0 = Packet Sequence field is fixed. 1 = Packet Sequence field is incremented with chained packets.
	7	0 = No chained packets to follow. 1 = Chained packet(s) to follow.
HB3	4:0	**Packet Sequence** Range is from 0 to 31. Shall be cleared to 0 if one SDP can pack payload data; to be wrapped around for chaining of more than 32 VSC_EXT_VESA SDPs.
	7:5	**RESERVED** Read all 0s.

Table 2-123: VSC_EXT_VESA and VSC_EXT_CEA SDP Payload Bytes – DB0 through DB31

Byte #	Bit #	Content
DB0	7:0	**Payload Byte 1**
DB1	7:0	**Payload Byte 2**
DB2	7:0	**Payload Byte 3**
…	…	**…**
DB30	7:0	**Payload Byte 31**
DB31	7:0	**Payload Byte 32**

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2.2.5.11 Video Stream Configuration Extension CEA SDP

Support for Video Stream Configuration Extension CEA (VSC_EXT_CEA) is new to *DP v1.4*.

VSC_EXT_CEA SDP shall be used for future CEA INFOFRAMEs that have more than 28 bytes of payload. A CEA INFOFRAME whose payload size is 28 or fewer bytes shall be encapsulated in the INFOFRAME SDP described in Section 2.2.5.1.

The SDP Type value for a VSC_EXT_CEA_SDP is 21h (see Table 2-122). The VSC_EXT_CEA SDP's specification is identical to that of a VSC_EXT_VESA SDP (see Section 2.2.5.10).

When a DP Sink device has a DPCD r1.4 (or higher) and its VSC_EXT_CEA_SDP_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 6) set to 1, a DP Source device may send stream metadata using a single VSC_EXT_CEA SDP framework for the supported payload type exposed in EDID and/or DisplayID by the DP Sink device.

If a DP Sink device, in addition to setting the VSC_EXT_CEA_SDP_SUPPORTED bit, also sets the VSC_EXT_CEA_SDP_CHAINING_SUPPORTED bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 7) to 1, a DP Source device may send stream metadata using multiple VSC_EXT_CEA SDPs that chain framework for the supported payload type exposed in EDID and/or DisplayID by the DP Sink device.

A DP Sink device that supports VSC_EXT_CEA SDP chaining shall support the chaining of up to 64 SDPs equal to 2KB in size. A DP Sink device that supports the chaining of VSC_EXT_CEA SDPs beyond 64 shall indicate the number (count) that exceeds 64 in the VSC_EXT_CEA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_CEA_SDP_MAX_CHAINING register (DPCD Address 02213h, bits 7:0). If a DP Sink device supports the chaining of the maximum of 96 SDPs, the device shall program the VSC_EXT_CEA_SDP_MAX_CHAINING register to the value of 32 decimal (20h).

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2.2.5.12 SDP Splitting in SST Mode

Support for SDP splitting in SST mode is new to *DP v1.4*.

A DP Source device shall support SDP splitting in SST and MST formats. The DP Source device has an option of when it will use the SDP splitting capability. In SST mode, the capability for a DP Sink device to reconstruct a split SDP is indicated by setting the SST_SPLIT_SDP_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 1).

Note: *In MST mode, the capability for a DP Sink device to reconstruct a split SDP is normative (see Section 2.6.3.3.2 for details).*

SDP splitting is the process of splitting SDPs with a main stream including BE/BS symbol sequence, associated data (VB-ID/Mvid7:0 /Maud7:0), and MSA packet, as shown in Figure 2-51.

Only one level of splitting is allowed. SDP splitting by another SDP is prohibited. The SDP stream may be interrupted at any time, and may additionally be interrupted more than once (e.g., such as when the horizontal blank is short and the secondary packet length is long). In SST implementations, interruption and resumption of the SDP can occur at any on any individual symbol boundary.

Note: *In MST implementations, interruption and resumption of the SDP shall occur at the 4-symbol sequence boundary (see Section 2.6.3.3.2 for details).*

SDP splitting can occur during HBlank and VBlank periods. SDP splitting can also occur while IDLE_PATTERN is being transmitted (no main video stream pixel data is transmitted).

Figure 2-51: SDP Splitting in SST Mode Examples

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2.2.6 ECC for SDP

All SDPs must be protected via ECC. (DP Main-Link Attributes data is protected via redundancy.)

The SDP must consist of a 4-byte header protected by four bytes of parity, followed by a payload consisting of a multiple of 8 bytes of data protected by the same multiple of 2 bytes of parity (i.e., 8 packet body bytes have 2 bytes of parity, 16 packet body bytes have 4 bytes of parity, etc.). The SDP must end with a parity byte. SDPs constructed with fewer than 8 bytes of data must use zero padding to fill the remaining data positions.

2.2.6.1 ECC Based on RS (15, 13)

DisplayPort uses Reed-Solomon code, RS (15, 13), with a symbol size of one nibble (four bits) in the ECC block.

The basic principle of error correcting encoding is to find the remainder of the message divided by a generator polynomial G(*x*).

The encoder works by simulating a Linear Feedback Shift Register with degree equal to G(x), and feedback taps with the coefficients of the generating polynomial of the code. In general the generator polynomial G(x) for any number of parity, configurable as the NPAR is as follows:

$$G(x) = (x - \alpha^0)\,(x - \alpha^1)\,(x - \alpha^2)\,(x - \alpha^3)\,(x - \alpha^4)\,\ldots\,(x - \alpha^{NPAR-1})$$

Because RS (15, 13) with a symbol size of one nibble is chosen, the second degree generator polynomial is used as follows:

$$G(x) = (x - \alpha^0)\,(x - \alpha^1) = x^2 - g_1 * x + g_0$$

Note: *Subtraction is equivalent to addition in binary fields.*

Therefore:

$$G(x) = x^2 + g_1 * x + g_0$$

where:

- $g_1 = \alpha^4$ and $g_0 = \alpha$

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With encoding of the base field GF (2^4), "α" is equal to (0, 0, 1, 0), which gives α^4 = (0, 0, 1, 1).

The logic equations for implementing g1 and g0 multiplications are listed below (where c[3:0] is a 4-bit nibble being multiplied by g1 or g0):

$$g_1 * c[3:0] = \{c[3]\hat{}[2], c[2]\hat{}[1], c[3]\hat{}[1]\hat{}[0], c[3]\hat{}[0]$$

$$g_0 * c[3:0] = \{c[2], c[1], c[3]\hat{}[0], c[3]\}$$

The following three messages show the outputs of ECC for input data with parity nibbles shown in ***underlined, bold, italic-font*** numbers:

- Transmitted Message:
  f, e, d, c, b, a, 9, 8, ***2, 2***
- Transmitted Message:
  9, 8, 3, 2, 1, 7, 5, 4, ***8, f,***
- Transmitted Message:
  7, 6, 5, 9, 8, 1, 3, 2, ***7, 2,***

2.2.6.2 ECC g_1 and g_0 C-code (Informative)

Figure 2-52 shows the block diagram of an RS (15:13) encoder with a symbol size of nibble.

Figure 2-52: Block Diagram of an RS (15:13) Encoder

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The following code shows ECC g_1 and g_0 in C-code.

```
//-----------------------------------------------------
//c * a^1
//-----------------------------------------------------
unsigned char gfmul_1( unsigned char ) ;
unsigned char gfmul_1( a )
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;
 for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply
*/
 c[i] = a & 0x01 ;
 a = a >> 1 ;
}

gf_mul[0] = c[3] ;
gf_mul[1] = c[0] ^ c[3] ;
gf_mul[2] = c[1] ;
gf_mul[3] = c[2] ;
r = 0 ;
for ( i=0; i<4; i++) {
 r = ((gf_mul[i] & 0x01) << i) | r ;
}
return (r) ;
}
//-------------------------------------------------------
// c * a^4
//-------------------------------------------------------
unsigned char gfmul_4( unsigned char ) ;
unsigned char gfmul_4( a )
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;
 for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply
*/
 c[i] = a & 0x01 ;
 a = a >> 1 ;
}
gf_mul[0] = c[0] ^ c[3] ;
gf_mul[1] = c[0] ^ c[1]^ c[3] ;
gf_mul[2] = c[1] ^ c[2] ;
gf_mul[3] = c[2] ^ c[3] ;
r = 0 ;
for ( i=0; i<4; i++) {
 r = ((gf_mul[i] & 0x01) << i) | r ;
}
return (r) ;
}
//-------------------------------------------------------------
```


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2.2.6.3 Nibble Interleaving

To further enhance the error correcting capability, ECC block of DisplayPort incorporates nibble interleaving after the incoming data packet is error correcting encoded. Combining RS (15:13) with the nibble interleaving, the ECC block is capable of correcting up to 2-byte error in a 16-byte data block.

As shown in Figure 2-53 (for Payload) and Figure 2-55 (for Header), Lane 0 is interleaved with Lane 1, while Lane 2 is interleaved with Lane 3 for 2- and 4-lane Main-Link configurations. Interleaving for a 1-lane Main-Link is shown in Figure 2-54 (for Payload) and Figure 2-56 (for Header).

Figure 2-53: ECC Block Nibble-Interleaving for 2- and 4-Lane Main-Links

Figure 2-54: ECC Block Nibble-Interleaving for a 1-Lane Main-Link

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Figure 2-55: ECC Block Nibble-Interleaving for 2- and 4-Lane Main-Links (Header)

Figure 2-56: ECC Block Nibble-Interleaving for a 1-Lane Main-Link (Header)

Note: *nb00 is the lowest nibble of HB0, nb01 is the highest nibble of HB0, nb08 is the lowest nibble of HB1, and nb09 is the highest nibble of HB1.*

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Because the symbol size is a nibble (4 bits wide), the length of the code-word is 15 nibbles (= 2^4 - 1) within the ECC block.

For packet payloads, two parity nibbles (or one byte) must be generated for eight data nibbles (or four bytes) for the packet payload per lane as shown in Figure 2-57. Only 10 nibbles consisting of eight data nibbles and two parity nibbles shall be used. The remaining most significant five nibbles must be zero-padded, and must not be transmitted over a DP link.

As for the packet header, four nibbles of the 15 nibbles must be used as shown in Figure 2-58. Those four nibbles consist of two data (i.e., packet header) nibbles and two parity nibbles. The remaining most significant 11 nibbles must be zero-padded, and must not be transmitted. With this protection, the ECC block is capable of correcting a 2-byte error in a 4-byte packet header.

Figure 2-57: Makeup of 15 Nibble Code-Word for Packet Payload

Figure 2-58: Makeup of 15 Nibble Code-Word for Packet Header

2.2.6.4 Corrective Action in the Event of Three Symbol Errors (Informative)

The ECC method described above cannot correct the errors when there are three or more symbol errors. Corrective action by a Sink device in case such an error condition is encountered is an implementation-specific choice and beyond the scope of this standard.

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2.3 AUX CH States and Arbitration

2.3.1 AUX CH STATES Overview

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction.

Upon detecting the DPRX through the Hot Plug Detect mechanism as described in Section 3.1.3.2 must put its AUX CH to AUX IDLE State, S2 (Figure 2-59). The DPRX must also be in AUX IDLE State, D1 (Figure 2-60) when it asserts the HPD signal.

Optionally, the Sink device may monitor the presence of the DPTX. If the Sink device is monitoring the presence of a DPTX, the Sink device may enter the AUX IDLE state only when the DPTX is detected.

In state S2, the DPTX must be in “Talk Mode” and must issue a Request command as needed. The DPRX, in state D1, must be in “Listen Mode” and must be waiting for a Request command.

Upon issuing a Request transaction, the DPTX must transition to state S3, the AUX Request CMD Pending State. In S3 state, the DPTX must be in “Listen Mode” waiting for the DPRX to reply. Upon receipt of a Request transaction, the DPRX must go to state D2, the AUX Reply CMD Pending state. Once in D2 state, the DPRX must be in “Talk Mode,” ready to send a reply over the AUX CH.

Upon the reception of a Request transaction, the DPRX must reply within a maximum of 300us (Response Timer timeout period). If, for some reason, the DPRX is unable to send the reply within the Response Timer timeout period, the DPRX must go back to D1 without reply. The DPTX must wait for up to 400us (Reply Timer timeout period) upon entering S3. When no reply is received in Reply Timer timeout period, the DPTX must go back to S2 and must be allowed to initiate a Request transaction as needed.

Transitions from D0 to D1 through the D0' state may be used by DPRXs that implement optional DPTX detect functionality. In the D0' state, Reset is de-asserted from the DPRX; however, the DPTX is not detected.

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Note: DPTX may be disabled by Policy Maker.
Upon being enabled, DPTX enters S0 state.

Figure 2-59: AUX CH DPTX State Diagram

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Note: If HPD is de-asserted, D0 will always be the next state.

Figure 2-60: AUX CH DPRX State Diagram

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2.3.1.1 Rules of DP_PWR State for a Source Device

For cases where the DP_PWR pin is enabled to supply power, Table 2-124 lists the rules of the DP_PWR state in conjunction with the AUX CH DPTX state shown in Figure 2-59 for a Source device.

Table 2-124: Rules of DP_PWR State for a Source Device

DP_PWR State	Rules
S0	Source device may disable DP_PWR • Source device is either OFF (or reset) or not monitoring HPD • Source device may go to S1 state any time
S1	Source device must enable DP_PWR: • Source device is monitoring HPD signal status • Source device goes to S2 state when HPD signal is present • Source device may go to S0 state any time
S2 and S3	Source device must enable DP_PWR: • Source device is either transmitting or ready to transmit (after Link Training) bits over Main-Link • Source device goes to S1 state when HPD signal is absent • Source device may go to S0 state any time

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2.3.1.2 Rules of DP_PWR State for a Sink Device

Table 2-125 lists the rules for the DP_PWR state in conjunction with the AUX CH DPRX state shown in Figure 2-60 for a Sink device.

Table 2-125: Rules of DP_PWR State for a Sink Device

DP_PWR State	Rules
D0	Sink device may disable DP_PWR: • Sink device is OFF (or reset) or not monitoring Source Detection signal • Sink device de-asserts HPD signal • Sink device may go to D1 state any time • Sink device may go to D0' state if it supports Source Detect feature and Source device is not detected
D0'	Sink device must enable DP_PWR (For a tethered Sink device, upon detecting DP_PWR Consumer): • Sink device de-asserts HPD signal, but monitors Source Detect status • Sink device goes to D1 when Source detected • Sink device may go to D0 state any time
D1 and D2	Sink device must enable DP_PWR (For a tethered Sink device, upon detecting DP_PWR Consumer): • Sink device asserts HPD signal • Sink device is either receiving or ready to receive bits over Main-Link • Sink device goes to D0' state when Source is absent • Sink device remains in D1 even when Source writes 010 to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h,bits 2:0) • Sink device may go to D0 state any time

A Sink device may be in “Power-Save” mode even in the D1 state when it is not receiving bits over the Main-Link. In the power-save mode, the Sink device may put itself in the following condition:

- **Main-Link Receiver is disabled** – Different signals parked at Vbias_RX
- **AUX CH Receiver is monitoring differential signals** – It must be ready to reply upon differential signal detection within 1ms

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2.3.2 Link Layer Arbitration Control

As described above, the Source and Sink devices must not be in Talk mode or Listen mode at the same time. Furthermore, the Response Timer timeout period of the Sink device must be shorter than that of Reply Timer of the Source device. In the case of a timeout, both the Source and Sink devices must return to the AUX IDLE state, which is Talk mode for the Source device and Listen mode for the Sink device. Therefore, contention and live lock will be avoided.

2.3.3 Policy Maker AUX Services

There are multiple applications and services that initiate AUX transactions. Some examples are:

- AUX Link Services
  - Receiver capability read
  - Link configuration (training)
  - Link status read
- AUX Device Services
  - EDID read
  - MCCS (Monitor Command and Control Set) control

The DP AUX CH must not support nested transactions. In other words, one transaction must be ended before another transaction can be initiated. The Policy Maker must be responsible for determining the order in which the multiple AUX Request transactions get executed per their priorities. The Link Layer shall merely initiate AUX transaction as it receives the request from the Policy Maker.

A request transaction may not end in full-completion. The Sink device may reply with NACK or DEFER when not ready for full-completion. The Policy Maker must decide on the follow-up action if the Request transaction is replied with NACK or DEFER.

The amount of data transported over the AUX CH per transaction must be limited to 16 bytes or fewer (i.e., the burst size must be 16 data bytes maximum). This limitation is set to prevent a single transaction from monopolizing the bus for an extended period of time. No transaction must occupy the AUX CH more than 500us. If a given transaction requires more than 16 bytes of data to be transported, the Policy Maker must divide it into multiple transactions with no transaction larger than 16 bytes.

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2.3.4 Detailed DPTX AUX CH State and Event Description

Table 2-126: DPTX AUX CH State and Event Descriptions

State/Event	Description
S0: Reset	State S0 must be entered from any state when RESET is asserted.
S1: AUX CH Unplugged	The HPD signal is un-asserted (low state). Upon entry, the level of the HPD signal must be passed up to the Link Policy Maker. The DPRX is either not connected or has not asserted the HPD signal. The AUX CH is unavailable. Therefore, AUX CH services such as DPCD, EDID, etc., are not available.
S2: AUX CH IDLE	The HPD signal is asserted (high). The DPRX is connected to either its main power supply or "trickle" power, though the state of the DPRX's power switch (if any) is not specified. A message indicating AUX CH available must be passed up to the Policy Maker. In this state, no AUX Command is pending and the AUX CH is available for the Policy Maker to initiate request transactions. The source must stay in Talk Mode until a request transaction has been completed according to the AUX CH syntax as it is specified in this section. Upon sending STOP, the last part of a request transaction, the DPTX must transition to State S3 provided HPD is still asserted.
S3: AUX Request CMD PENDING	Upon completion of an AUX request transaction, the DPTX AUX CH must enter State S3. In this state, the DPTX is waiting to receive a Reply message from the DPRX. The DPTX must not issue commands in this state. The DPTX AUX CH must stay in Listen mode. Upon entry to this state, the Reply-Wait Timer (400us) must reset and start counting. The DPTX AUX CH must exit from this state and enter State S2, AUX IDLE state, when it receives the Reply Command from the DPRX, or when its Reply Command Timer times out. In case of a Reply Timer timeout, the DPTX device must retry at least three times, because no reply may be due to the DPRX device "waking" from a power-saving state, which may take up to 1ms.
Transition from any State to S0	Occurs when RESET is asserted.
Transition S0:S1	Occurs when RESET is de-asserted.
Transition S1:S2	Occurs upon Hot Plug Detection.
Transition S2:S1 or S3:S1	Occurs upon Hot Plug Detection.
Transition S2:S3	Occurs upon the completion of DPTX AUX Request Transaction.
Transition S3:S2	Must take place either when the DPTX AUX CH receives a Reply Command from the Sink device, or when the Reply Command Timer (400us) times out.

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2.3.5 Detailed DPRX AUX CH State and Event Description

Table 2-127: DPRX AUX CH State and Event Description

State/Event	Description
D0: DPRX Not Ready	The DPRX must transition to this state from any other state when RESET is asserted. In this state, the HPD signal is de-asserted. The DPRX AUX CH may be disabled. Upon RESET de-assertion, the DPRX must transition to the D1 state, unless DPTX device detection is implemented, in which case the DPRX must transition to the D0' state.
D0': DPTX Not Detected	This state is optional and may be used by DPRXs that monitor the presence of the DPTX. When RESET is de-asserted and HPD signal is asserted and the DPTX is not detected, this optional state may be entered. Upon detection of the DPTX, the DPTX must transition to D1.
D1: AUX CH Idle	In this state the DPRX AUX CH must stay in "Listen mode," waiting for the DPTX to send an AUX Request Command over the AUX CH. The DPRX AUX CH must also stay in this state after an invalid signal (e.g., invalid SYNC, STOP or channel code) is received. Upon receiving an AUX request transaction command from the DPTX, the DPRX AUX CH must transition to the D2 state and its response timer (300us) resets and begins counting. In Listen mode, a DPRX must either receive and decode the request transaction or detect the presence of a differential signal input, even if it is in a power-saving state. If the DPRX is in a power-saving mode and cannot reply within the Response Timeout period of 300us, it must exit the power-saving mode within 1ms of detecting the presence of a differential signal input so that it can provide an AUX reply within three AUX transaction retries by the DPTX. A DPRX must make its best effort to avoid issuing no reply except when "waking" from a power-saving mode.
D2: AUX Reply CMD Pending	In this state the DPRX must be in "Talk mode," getting ready to reply to the DPTX. Upon completion of the reply transaction, the DPRX must transition to the D1 state. A timeout condition of the response timer must cause the DPRX to transition to the D1 state without initiating a reply transaction.
Transition of D0: D0' (Optional transition)	Occurs when RESET is de-asserted and HPD signal is asserted.
Transition of D0':D1 (Optional transition)	Occurs upon DPTX detect, after the optional D0' state is entered.
Transition of D0:D1	Occurs when RESET is de-asserted and when the DPRX has asserted the HPD signal and is ready to serve for services over AUX CH.
Transition of D1:D2	Occurs upon receiving an AUX Request transaction from the DPTX.
Transition of D2:D1	Occurs when the Sink device completes its reply to the DPTX, or the DPRX fails to reply before the response timer (300us) times out.

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2.4 Overview of DP MST Isochronous Transport Service

DP Isochronous Transport Service, based on micro-packet architecture, transports the audio and video streams from a Stream Source to a Stream Sink via DP link(s), as shown in Figure 2-61.

Figure 2-61: DisplayPort Data Transport Channels

This section describes the overview of the Multi-Stream Transport (MST) Isochronous Transport Service extension. The MST extension enables the transport of multiple streams from multiple stream Sources in one or more DP Source devices to multiple Stream Sinks in one or more DP Sink devices connected via DP Branch devices as shown in Figure 2-62. This is in contrast with Single-stream Transport (SST) mode which is limited to a transport of single main stream and optional SDP stream as described in Section 2.2.

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Figure 2-62: DP Multi-Stream Transport

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2.4.1 Connection-oriented Transport

The DP Isochronous Transport Service is a connection-oriented transport providing for management of stream transfer from a Stream Source device to a Stream Sink device, independent of the actual underlying stream transport mechanisms.

Virtual Channel is an end-to-end, direct virtual connection between a Stream Source device and a Stream Sink device. On the underlying DP Layers level, multiple links (called "path") may need to be traversed to realize the Virtual Channel connection, as shown in Figure 2-63. Over each link, the Virtual Channel is mapped to a payload called "VC Payload" of the micro-packet.

Figure 2-63: Illustration of Virtual Channel, Link, and Path

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The end-to-end, direct-connection nature of Virtual Channel becomes more apparent when there are multiple Stream Sinks and multiple Stream Sources, as shown in Figure 2-64 and Figure 2-65. In the Dual Display Clone example illustrated in Figure 2-64, Link1 between the DP Source Device and DP Branch Device1 carries a single payload for the single Stream Source device. In the Extended Desktop example illustrated in Figure 2-65, Link1 between the DP Source Device with two Stream Sources and the DP Branch Device1 carries two payloads – one for Stream Source1 and the other for Stream Source2.

Figure 2-64: Single-Stream Source Device to Dual-Stream Sink Devices (Dual-Display Clone)

Figure 2-65: Dual-Stream Source Devices to Dual-Stream Sink Devices (Extended Desktop)

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2.4.2 Layers of DP Isochronous Transport Service

The Isochronous Transport Service uses the sideband communications over sideband channel (AUX CH and HPD) for the management of topology/virtual channel connection/Main-Link and performs Main-Link symbol mapping. The particular services provided in each layer differ between SST-only and MST-capable devices, with MST-capable devices generally providing a superset of functionality.

The layers of SST-only Isochronous Transport Services and MST Isochronous Transport Service are shown in Figure 2-66 and Figure 2-67, respectively, and briefly described in the remainder of this section.

Figure 2-66: SST-only Isochronous Transport Service Layers

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Figure 2-67: MST Isochronous Transport Service Layers

Layers above DP Isochronous Transport Service Layers (i.e., Virtual Channel Management Layer and Application Layer) are application-/implementation-specific, and, therefore, beyond the scope of this Standard. The DisplayPort Standard refers to the implementation guidelines of the Stream/ Link Policy Maker.

2.4.2.1 Topology Management Layer

- Present in every MST DP device (i.e., a device that has a DPTX and/or DPRX, also referred to as a DP node).
- Added for MST Isochronous Transport Service; not present in SST-mode. An MST-capable device transmitting in SST transport format still provides for this function.
  - Topology Manager in a DP Source device discovers and maintains the topology via sideband communication.
  - Topology Assistant in a DP Branch device provides topology information to Topology Manager via sideband communication.

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2.4.2.2 Payload Bandwidth Management Layer

- Present in every MST DP device with DPTX, namely, a DP Source device and DP Branch device.
- Added for MST Isochronous Transport Service; not present in SST-mode. An MST-capable device transmitting in SST transport format still provides this function.
- Avoids the overflow of the buffer in the path from the stream source in a DP Source device to the Stream Sink in a DP Sink device.
  - Source Payload Bandwidth Manager in a DP Source device receives the stream bandwidth, calculates Payload Bandwidth Number (PBN) corresponding to the stream bandwidth, forwards the PBN value via sideband communication, and sets the VC Payload Bandwidth of its own downstream link by allocating sufficient time slots to the VC Payload.
  - Branch Payload Bandwidth Manager in a DP Branch device receives and forwards the PBN via sideband communication, and sets the VC Payload Bandwidth of its own downstream link by allocating sufficient time slots to the VC Payload.
  - Instructs the Main-Link Symbol Mapping Layer how many time slots to allocate to a VC Payload Allocation and when to enable/disable insertion of Stream Symbols from VC Payload Mapping Layer into a VC Payload.

2.4.2.3 Link Management Layer

- Present in every MST DPTX and DPRX.
- Present in both MST and SST modes (referred to as Link Policy Maker in SST-only devices).
- Establishes and maintains Main-Link through Link Training and Link Maintenance.
  - Link Management Layer of DPTX instructs Main-Link Symbol Mapping Layer to transmit Link Training Pattern Sequences and, once Link Training is successful, to transmit micro-packets (called Multi-stream Transport Packet, or MTP) to keep the link enabled; also monitors the status of the DPRX it is driving.
  - Link Management Layer of DPRX provides for ADJUST_REQUEST for DPTX drive setting optimization during Link Training, and keeps the link status information up to date, generating IRQ_HPD pulse when it requires the attention of Link Management Layer of the DPTX.

2.4.2.4 Main-Link Symbol Mapping Layer

- Present in every DPTX and DPRX.
- Enhanced for MST Isochronous Transport Service.
  - Main-Link Symbol Mapping Layer of DPTX transmits Link Training Pattern Sequences and MTP Symbols as instructed by the Link Management Layer; also allocates time slots to a VC Payload and controls the insertion of Stream Symbols coming from the VC Payload Mapping Layer as instructed by the Payload Bandwidth Management Layer.
  - Main-Link Symbol Mapping Layer of DPRX receives Main-Link Symbols and informs its Link Management Layer of the link quality; also keeps VC Payload allocation synchronized with that of DPTX of the immediate upstream DP device and extracts Stream Symbols from incoming MTP Symbols.

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2.4.2.5 VC Payload Mapping Layer

- Present per stream.
- Present both in MST mode and SST mode (Stream-to-TU Payload Mapping Layer)
  - VC Payload Mapping Layer in a DP Source device receives stream (both data and control) from a stream source and converts it to Stream Symbols inserted into VC Payload.
  - VC Payload Mapping Layer in a DP Sink device regenerates the stream from incoming Stream Symbols.
  - VC Payload Mapping Layer in a DP Branch device passes through incoming Stream Symbols from its upstream DPRX to its downstream DPTX in a manner that is agnostic to stream data format/symbol type/lane count (i.e., no symbol parsing needed).
    - If the first (or most upstream) DP Branch device is receiving Main-Link Symbols from a DP Source device in SST Mode, the VC Payload Mapping Layer of that DP Branch device must perform more than Stream Symbol pass-through. How to perform the conversion from SST Stream Symbols to MST Stream Symbols is an implementation-specific choice.
    - If the last (or most downstream) DP Branch device is driving a DP Sink device in SST mode, the VC Payload Mapping Layer of that DP Branch device must perform more than Stream Symbol pass-through. How to perform the conversion from MST Stream Symbols to SST Stream Symbols is an implementation-specific choice.

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2.4.3 Sideband CH Communications

As noted above, the Topology Management Layer, Payload Bandwidth Management Layer, and Link Management Layer use Sideband CH communications for management. Sideband CH Communications take place over AUX CH and HPD signal line.

In addition to AUX Transaction between DP device pair across a single link, Message Transaction across any DP device pair over one or more links in the topology is available. Unlike AUX Transaction which is always initiated by an upstream DP device, Message Transaction is full-duplex bidirectional, and can be initiated either by an upstream or downstream DP device.

The Topology Management Layer and Payload Mapping Layer work across the topology, and therefore use Message Transactions for management as well as DPCD access via Native AUX Transactions. Link Management is across a single link between DPTX and DP Sink, and uses DPCD access only.

Figure 2-68: Sideband CH Communication Layers

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2.5 Topology Management Layer

The Topology Management Layer using Messaging AUX Client, covered in Section 2.11, helps the Topology Manager in a DP Source device (optional in DP Sink device) determine what devices are in the topology.

This section consists of the following sub-sections:

- Section 2.5.1 – Primitives of MST DP Devices and Device Types

  Primitives of the MST DP devices are DPTX, DPRX, branching unit, stream source, and stream sink. MST DP Branch, Source, Sink, and Composite devices are comprised of various combinations of these primitives.

- Section 2.5.2 – MST Topologies

  DP Branch devices of MST topology need to be MST devices supporting Topology Management while the "end" device (DP Source, DP Sink, and Converter device) may be either MST or SST device.

- Section 2.5.3 – MST Device Identification

  MST device with a branching unit is identified with Globally Unique Identifier (GUID) and Relative Address (RAD). The end device that has no branching unit is identified as a "peer device" connected to one of the ports of the MST device with a branching unit. A DP device with DPRX with DPCD Revision number 1.2 or higher must have the GUID register (DPCD Addresses 00030h through 0003Fh).

- Section 2.5.4 – Topology Manager and Topology Assistant

  Topology Management is conducted through the collaboration between Topology Manager in MST DP Source device (optionally in MST DP Sink device) and Topology Assistant in MST device with a branching unit.

- Section 2.5.5 – Topology Discovery

  Topology Manager obtains information about the topology by using Native AUX transactions and Messaging AUX Client, namely, LINK_ADDRESS Message Transaction. (Messaging AUX Client is covered in Section 2.11.) The amount of information obtained about the topology and the use of the information is Topology Manager implementation-specific.

- Section 2.5.6 – Topology Maintenance

  Topology Manager receives notifications when DP devices and legacy devices are connected and disconnected from the topology. These notifications are provided by Topology Assistants via Messaging AUX Client, namely, CONNECTION_STATUS_NOTIFY Message Transaction.

- Section 2.5.7 – Topologies with SST-only Source devices

  Topology option with SST Source Device is restricted.

- Section 2.5.8 – Loop Handling

  MST Topology Management feature provides for sufficient information for Topology Manager to properly handle a topology with a loop and/or a parallel path.

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2.5.1 Primitives of MST DP Devices and Device Types

Primitives of DP devices are a DPTX, DPRX, branching unit, stream source, and stream sink.

The branching unit must meet the following requirements:

- Have both input and output ports and be capable of VC Payload routing from the input ports to the output ports.
- Have at least one input port and one output port.
- Have no more than eight physical ports each of which is connected either to DPTX (output port) or DPRX (input port). The physical port numbers of a branching unit are from Port 0h up to Port 7h. The physical input ports, if present, are assigned smaller port numbers than physical output ports.
- Have no more than eight logical ports that are internally connected (and therefore, not connected to DPTX/DPRX). Logical port numbers of a branching unit are from Port 8h up to Port Fh. The logical input ports, if present, are assigned smaller port numbers than the logical output ports.

Figure 2-69: Branching Unit

Note: *A PHY Repeater device having PHY Layer circuits of DPTX and DPRX only (namely, DPTX_PHY and DPRX_PHY, respectively) is transparent in DP topology.*

2.5.1.1 Connection between Primitives: Physical Link and Logical Link

The connection between a DPTX and DPRX is called a "physical link," while the connection between a branching unit and a stream source/stream sink/another branching unit is called a "logical link."

2.5.1.2 DP Branch Device

A DP device that has a branching unit, at least one DPTX, and at least one DPRX, but has no stream source/sink is called a DP Branch device.

A DP Branch device that supports MST mode is called an "MST DP Branch device." An MST DP Branch device must support Topology Management as Topology Assistant.

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2.5.1.3 DP Source Device

A DP device that has one or multiple stream sources, has one or multiple DPTXs, but has no DPRX, is called a "DP Source device."

A DP Source device that supports MST mode is called an "MST DP Source device." A MST DP Source device must support Topology Management to play the role of Topology Manager.

2.5.1.4 DP Sink Device

A DP device that has one or multiple stream sinks, has one or multiple DPRXs, but has no DPTX is called a DP Sink device. As for the presence/absence of a branching unit within a DP Sink device, the following rules apply:

- DP Sink device either with single main stream sinks or with a single main stream sink and a single SDP stream has no branching unit inside.
- DP Sink device that has multiple main stream sinks has a branching unit inside, whether each main stream sink has SDP stream sinks or not. The output port number of the branching unit is assigned to Main/SDP Stream Router of each main stream sink, as shown in Figure 2-70.
- DP Sink device that has a single stream sink and multiple SDP stream sinks has a branching unit with one input port and one output port, as shown in Figure 2-71.
- DP Sink device that has no main stream sink, but has multiple SDP stream sinks has a branching unit with one input port and one output port, as shown in Figure 2-72.
- DP Sink device with a branching unit must support Topology Management as the Topology Assistant. A DP Sink device can choose to play the role of the Topology Manager.

Figure 2-70: MST Multi-Sink Device with Multiple Main Stream Sinks and SDP Sinks

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Figure 2-71: MST Sink Device with Single Main Stream Sink and Multiple SDP Sinks

Figure 2-72: MST Audio-only Sink Device with SDP Sinks

2.5.1.5 DP Composite Device

A DP Branch device with either stream source(s) or stream sink(s) is called a "DP Composite device." The DP Composite device must support Topology Management as the Topology Assistant.

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2.5.2 MST Topologies

This Standard supports interconnections of MST and SST DP devices into topologies. The Branch devices of the MST topology must be MST Branch devices. SST devices are allowed in the topology only as the end devices such as SST DP Source devices and SST DP Sink devices.

Topology Management is an MST feature; therefore, Topology Management is not supported by SST devices. An SST device is identified by the MST Topology Management layer as a peer device connected to an MST Branch device.

The maximum number of links between a stream source to a stream sink must be 15 or fewer. Of these, the maximum number of physical links is limited to seven. Figure 2-73 shows an example MST topology where all DP Source and Branch devices are MST devices supporting Topology Management and all DP Sink devices are those that have no branching unit.

Figure 2-73: Example MST Topology

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2.5.3 MST Device Identification

The Topology Management layer uniquely identifies each MST DP device with a branching unit within the topology. GUID and RAD are used for the identification. Those devices that do not support Topology Management, namely MST DP devices that have no branching unit and SST devices, are identified as peer devices connected to the ports of the MST devices with a branching unit.

2.5.3.1 Global Unique Identifier

MST DP devices may perform more than one function. For example, an MST DP Sink device may contain an USB hub. In such cases, the system needs to know that both functions are within the same physical unit.

Depending on the topology, it is possible for a single physical device to be accessed through multiple paths. In such situations, the Topology Manager must be able to infer that the physical device is the same, thereby reducing end user confusion in user interface. The 16-byte GUID, accessible through DPCD access, is used for these identification purposes.

All the devices with DPRX with DPCD Revision number 1.2 or higher must have the GUID register (DPCD Addresses 00030h through 0003Fh). For those devices with their own unique GUID, this GUID register is Read Only. For those devices with DPCD Revision number 1.2 or higher, but the GUID register is all 0s as power-on reset value, the GUID register is both writable and readable.

In case there is an integrated USB or USB hub device, the GUID must match the GUID in the Container Descriptor of the integrated USB device or hub. All functions within the physical MST DP device must report the same GUID.

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2.5.3.2 Relative Address

Each MST DP device port is addressable using a relative address. The RAD is relative to the MST DP device. Each RAD is a sequence of port numbers. For visual purposes, each port number is separated by a decimal, ".". In the example topology in Figure 2-74, Sink 1's RAD relative to Source 2 is 0.2.2.1. A message from Source 1 must be sent out Port 0 of Source 1, Port 2 of Branch 2, and out Port 1 of Branch 3 to reach Sink 1. The RAD of Source 1 relative to Sink 1 is 0.0.0. A message from Sink 1 must be sent out Port 0 of Sink 1, Port 0 of Branch 3, and Port 0 of Branch 2 to reach Source 1. The RAD for all the Sink devices relative to the Source devices in Figure 2-74 is given in its table.

Relative Address of Devices Accessible from Source Device 1

Device	Relative Address
Branch Device 2	0
Branch Device 3	0.2
Sink Device 1	0.2.1
Sink Device 2	0.2.2

Relative Address of Devices Accessible from Source Device 2

Device	Relative Address
Branch Device 1	0
Branch Device 2	0.2
Branch Device 3	0.2.2
Sink Device 1	0.2.2.1
Sink Device 2	0.2.2.2
Branch Device 4	0.1
Sink Device 3	0.1.1
Branch Device 5	0.1.2
Sink Device 4	0.1.2.1
Sink Device 5	0.1.2.2

Figure 2-74: Example Topology with RAD of Devices Relative to Source Devices

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2.5.4 Topology Manager and Topology Assistant

The Topology Management Layer in a MST Source device (or optionally in an MST Sink device) is called the "Topology Manager," while the Topology Management Layer in an MST device with a branching unit is called the "Topology Assistant."

2.5.4.1 Topology Manager

The Topology Manager is responsible for generating and maintaining the "DP device to RAD" table. The Topology Manager uses local Native AUX transactions and Message Transactions to build and maintain the table. How the Topology Manager builds and maintains the table is described in the subsequent sections.

2.5.4.2 Topology Assistant

Topology Assistant is the name of the Topology Management Layer in an MST device with a branching unit. The Topology Assistant uses local Native AUX transactions to gather information regarding peer devices connected to it and provides for the information as requested by the Topology Manager. The information provided by Topology Assistants is described later in this section.

2.5.5 Topology Discovery

The goal of Topology Discovery is Stream Policy Maker implementation-specific. The goal may be to find the closest DP Sink device, build a DP Sink device to RAD table, or graphically display the topology showing each device and its associated interconnections.

2.5.5.1 Topology Manager

The Topology Manager uses Native AUX transactions and Message Transactions to implement its Topology Discovery algorithm. Upon power up, the Topology Manager monitors the connection status of its local DFPs via the HPD signal of each port. When a device is connected to one of its DP ports, the Topology Manager reads the capabilities of the immediate downstream DP device using Native AUX transactions. The device capabilities include the device type and whether Messaging is supported. If the connected device (i.e., the peer device) is an MST device with a branching unit, the Topology Manager can instruct the Messaging AUX Client to send a LINK_ADDRESS message transaction request to the device to determine the device GUID, the number of input and output ports and the type and capabilities of devices connected to the device's input and output ports (called "Peer_Device Types"). The Topology Manager, using the information obtained from the LINK_ADDRESS message transaction response, can further send LINK_ADDRESS messages to other MST DP devices containing branching units until the goal of its Topology Discovery is met.

2.5.5.2 Topology Assistant

The responsibility of the Topology Assistant in an MST device with a branching unit during the Topology Discovery procedure is to reply to the LINK_ADDRESS Request Message Transaction with its capabilities and the Peer Device Type of each DP device connected to its DPTX and DPRX ports (either physical or logical). The Topology Manager gathers the information of the peer devices using Native AUX transactions.

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2.5.6 Topology Maintenance

Topology Maintenance is the continual monitoring for DP device connection or removal from the topology. The Topology Assistant within each MST DP Branch/Composite device is responsible for detecting and notifying the Topology Managers when devices are connected or removed. What the Topology Manager does with this notification is implementation-specific.

2.5.6.1 Topology Manager

During Topology Maintenance, the Topology Manager may receive CONNECTION_STATUS_NOTIFY Broadcast Request Message transactions when MST DP Branch devices are connected to or disconnected from the topology. The following information is provided with the CONNECTION_STATUS_NOTIFY Broadcast Request Message transaction:

- GUID of the MST device where the connection change was detected
- Port number on the device and whether the port is an input or output where the connection change was detected
- New connection status for the port where the connection change was detected
- Peer device type if a new DP device was connected
- Whether the newly connected DP device supports Messaging

How the Topology Manager uses this information is implementation-specific. The notification may be ignored if not required.

2.5.6.2 Topology Assistant

Once an MST DP device with a branching unit powers on, it continually monitors the connection status of each of its input and output ports using the connection mechanism associated with the corresponding port type, HPD for DPTX ports and cable termination for DPRX ports. All internal DP Sinks of a logical branch device are connected by default. When the connection status of any DP port changes, the new status is broadcast out to all connected DPTX and DPRX ports using the CONNECTION_STATUS_NOTIFY Broadcast Request Message transaction. The Topology Assistant continues monitoring its DPTX and DPRX ports for connection changes. The Topology Assistant may receive one or more LINK_ADDRESS Message Transaction requests. Each LINK_ADDRESS request will be handled the same as during the Topology Discovery procedure.

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2.5.7 Topologies with SST-only Source devices

When a topology contains one or more SST-only DP Source devices, the MST DP Branch device connected to the SST-only DP Source devices must perform the SST-only Topology Management function. The MST DP Branch device recognizes the upstream device as the SST-only device when the upstream device keeps the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) cleared to 0. An MST upstream device may act and be treated as an SST-only device by not setting the UP_REQ_EN bit to 1.

The SST-only Topology Management function is a basic input to output port selection. The MST DP Branch device connected to an SST-only Source device acts as an SST-only Branch device as described in Section 5.3. An MST Branch device acting as an SST-only Branch device must not perform SST input-to-MST output conversion.

A DPTX of an MST DP Source device may choose to transmit in SST transport format (i.e., keeps the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) of the downstream device cleared to 0) while setting the UP_REQ_EN bit to 1, as long as it performs the role of Topology Manager and Source Payload Bandwidth Manager and originates Message Transactions for virtual channel management prior to SST stream transmission. After the MST DP Source device establishes the virtual channel, using Message Transactions, and transmits in SST transport format, the MST DP Branch device must convert the SST input into MST output.

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2.5.8 Loop Handling

While DP MST topologies should be constructed without loops or parallel paths, the Topology Manager must be able to handle the case where loops or parallel paths exist.

The GUID obtained from the LINK_ADDRESS Message Transaction request and the RAD of the DP device queried provide for sufficient information to determine whether a loop or parallel path in the topology exists. The path chosen to access a DP device accessible through multiple paths is Topology Manager implementation-specific, including the handling of a topology that has a loop and/or a parallel path. An example topology with a loop and a parallel path is shown in Figure 2-75 along with the GUID and RAD for the loop and parallel path.

Figure 2-75: MST Topology with a Loop and a Parallel Path

The procedure the Messaging AUX client uses for handling Broadcast Message Transaction when loops are present is defined in Section 2.11.

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2.6 MST Operation

The Multi-Stream Transport (MST) Extension Specification described in this section achieves the following features:

- Transport of multiple streams that are asynchronous with one another and de-coupled from the link timing, with the packetizing overhead as small as 1.6%
- Addition or deletion of a stream without affecting the other streams being transported
- Symbol Stream Sequence pass-through operation of DP Branch devices in the path (except those performing the conversion between MST and SST symbol mapping) is agnostic to symbol types, data types/format, and Main-Link lane count
- Robust link; predictable link timing and redundancy in VC Payload symbol transmission (regardless of the lane count)

DP devices that support MST mode must support SST mode as well.

Stream Policy Maker is the entity that decides the audio and/or video streams to be transported. Stream Policy Maker makes use of the Payload Bandwidth Manager and the Topology Manager to achieve this task. To decide on the specific stream to use, Stream Policy Maker optionally determines the various audio and/or video modes that could be set at that moment based on various constraints and capabilities along the path.

This section focuses on the enumeration of path constraints within the Stream Policy Maker, the Main-Link Symbol Management Layer, Payload Bandwidth Management Layer and VC Payload Mapping Layer (Figure 2-76) and consists of the sub-sections summarized below.

Figure 2-76: Layers Covered in this Section

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- Section 2.6.1 – Enumeration of Path Constraints
  - Stream Policy Maker optionally determines the various audio and/or video modes that could be set at the moment based on various constraints and capabilities along the path.
- Section 2.6.2 – Link Timing Generation Based on Multi-Stream Transport Packet
  - The timing is self-generated by Main-Link Symbol Manager, rather than dictated by the timing of the stream being transported.
- Section 2.6.3 – Symbol Sequence Mapping into VC Payload
  - Symbol Sequence mapped into VC Payload consists of 4-symbol sequence units regardless of the Main-Link lane count.
  - Only a DP Source device generates Stream Symbol Sequence, while a DP Branch device forwards the Stream Symbol Sequence.
  - VC Payload Fill (VCPF) Symbol Sequence is inserted by Main-Link Symbol Manager in the absence of Stream Symbols. Stream Symbol Sequence mapped by VC Payload Mapper replaces VCPF Symbol Sequence when streams are transported.
  - VC Payload Symbol Generation method in MST mode enables pass-through of Stream Symbols by the intermediate DP Branch devices.
- Section 2.6.4 – Time Slot Count Allocation to VC Payload
  - Source Payload Bandwidth Manager and Branch Payload Bandwidth Managers collaborate to ensure that a stream be transported in the VC Payloads established for the stream over the path without causing overflow. Source Payload Bandwidth Manager calculates Payload Bandwidth Number (PBN) for a stream and passes the PBN value to the downstream Branch devices to let the Branch Payload Bandwidth Managers determine the VC Payload size in time slot count per MTP.
  - Source and Branch Payload Bandwidth Managers make sure that the VC Payloads are set to the smallest possible size so that the maximum number of streams may be transported simultaneously. A Source device performs the rate governing and evenly distributes the number of Stream Symbols over multiple MTPs by throttling the Stream Symbol Sequence insertion rate.
- Section 2.6.5 – VC Payload Allocation Synchronization Management
  - VC Payload is managed by synchronizing the VC Payload ID Tables between the DPTX and DPRX and also by synchronizing the VC Payload allocation over the Main-Link to the table.
- Section 2.6.6 – ALLOCATE_PAYLOAD Timing Sequence
  - ALLOCATE_PAYLOAD Message Transaction keeps the VC Payloads over multiple links between a stream source and a stream sink synchronized.
- Section 2.6.7 – Impacts of Various Events on VC Payload ID Table
  - Some events such as unplug event and loss of link affect the VC Payload ID Tables.
- Section 2.6.8 – Robustness Requirement
  - Certain actions are required for a DPRX to make the link as robust as possible by taking advantage of the self-generated Link timing and VC Payload Symbol generating methods of the MST DPTX.

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- Section 2.6.9 – Control Functions, Control Symbols, and K-Code Assignment
  - Control Symbols are mapped to ANSI 8b/10b K-codes. Most of the Control Symbols as well as all the Data Symbols are scrambled.
- Section 2.6.10 – Conversion between MST and SST Symbol Mapping
  - Simple pass-through operation does not apply to those DP Branch Devices converting from MST-mapped symbols to SST-mapped symbols (or vice versa).
  - Switching between MST mode and SST mode results in the interruption to the transport of streams.

Figure 2-77, Figure 2-78, and Figure 2-79 show the logical block diagrams of an MST DP Source device, DP Sink device, and DP Branch device, respectively. These diagrams are zoomed in and described in Section 2.6.2 and Section 2.6.3.

Figure 2-77: Logical Block Diagram of MST DP Source Device

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Figure 2-78: Logical Block Diagram of MST DP Sink Device

Figure 2-79: Logical Block Diagram of MST DP Branch Device

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Figure 2-80 and Figure 2-81 show the logic block diagrams of SST DP Source and Sink devices, respectively, for reference purposes. These diagrams, when compared to Figure 2-77 and Figure 2-78, illustrate the similarity of VC Payload Mapping Layer blocks between SST in 4-lane configuration and MST.

Figure 2-80: Logical Block Diagram of SST DP Source Device

Figure 2-81: Logical Block Diagram of SST DP Sink Device

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2.6.1 Enumeration of Path Constraints

An MST Source device uses a combination of LINK ADDRESS and ENUM PATH RESOURCES Message Transactions to determine resource constraints on a given path. LINK ADDRESS returns a Current Capabilities Structure (CCS), as defined in Table 2-128 and Table 2-129, indicating static device capabilities. ENUM PATH RESOURCES returns dynamic path resources (currently only the available link bandwidth) on a path through the Available PBN parameter.

Table 2-128: Current Capabilities Structure Syntax

Syntax	# of Bits
`Current_Capabilities_Structure`	
`Max Frame Height`	16
`Max Frame Width`	16
`Max Frame Size`	24
`Max Frame Rate`	10
`RESERVED`	6
`Color Depth Supported RGB`	8
`Color Depth Supported YCbCr`	16
`Max Pixel Clock`	16
`S3D Formats Supported`	16
`Max Streams Supported`	7
`Other Unspecified Capability Exists`	1

Table 2-129: Current Capabilities Structure Field Definitions

Field	Description
Max Frame Height	Maximum Active Height of the video frame that the device supports.
Max Frame Width	Maximum Active Width of the video frame that the device supports.
Max Frame Size	Maximum Active Frame Size of the video frame that the device supports. Specified in number of MacroBlocks (16 pixels by 16 pixels). This field can further refine the Max Frame Height and Max Frame Width constraints.
Max Frame Rate	Maximum rate at which the device can consume frames. Specified in terms of number of frames per second.
Color Depth Supported RGB	Indicates the color depth value that the device supports for RGB, Luma, and Chroma, The bit field values are defined in Table 2-130. Color Depth Supported RGB uses one instance of Table 2-130,
Color Depth Supported YCbCr	Indicates the color depth value that the device supports for RGB, Luma, and Chroma, The bit field values are defined in Table 2-130. Color Depth Supported YCbCr uses two instances of Table 2-130, with the table for Luma preceding the table for Chroma.
Max Pixel Clock	Maximum pixel clock that the device supports on the DFP used by the input path under characterization. Value is conveyed in units of MHz.
S3D Formats Supported	Indicates support for various S3D formats, as defined in Table 2-131.
Max Streams Supported	Maximum number of streams that the device supports.
Other Unspecified Capability Exists	Indicates presence of a vendor-specific constraint. The Source device discovers this constraint in a vendor-specific manner.

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Table 2-130: Bit Field Definition for Color Depth Indication for RGB, Luma, and Chroma

Bitfield	Meaning
1h	6bpc
2h	8bpc
4h	10bpc
8h	12bpc
10h	16bpc
All other values	RESERVED

Table 2-131: Bit Field Definition for S3D Capabilities

Bitfield	Meaning
0h	No S3D support
1h	Frame/Field Sequential, Value 0x0
2h	Frame/Field Sequential, Value 0x1
4h	Frame/Field Sequential, Value 0x2
8h	RESERVED
10h	Stacked Frame: Left view on top, right on bottom
20h	RESERVED
40h	Pixel Interleaved, Value 0x0
80h	Pixel Interleaved, Value 0x1
100h	Pixel Interleaved, Value 0x2
200h	Pixel Interleaved, Value 0x3
400h	Pixel Interleaved, Value 0x4
800h	RESERVED
1000h	Side by Side, Value 0x0
2000h	Side by Side, Value 0x1
4000h	RESERVED
8000h	RESERVED

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2.6.1.1 Multi-function DP MST Branch Device Enumeration

New to *DP v1.4*.

A basic MST Branch device contains an MST Branching Unit (BU) capable of the following operations:

- DP MST-in, DP MST-out VC Payload routing as an intermediate MST Branch device
- DP MST-to-DP SST conversion as the last MST Branch device

A multi-function MST Branch device, as the last MST Branch device, is capable of performing one or more of the following operations in addition to the basic MST Branch device capabilities listed above:

- Transport protocol conversion
- Video horizontal blanking expansion
- Ignore-MSA handling for adaptive sync support
- Pixel encoding format conversion (e.g., YCbCr4:4:4-to-YCbCr4:2:0)
- Display Stream Compression (DSC) decompression

Multi-function MST Branch may contain local stream sinks to constitute a multi-function MST Branch-Sink device

2.6.1.1.1 Virtual DP Peer Device with DPCD Registers

A multi-function MST Branch or Branch-Sink device shall enumerate those multi-function downstream-facing ports (DFPs) connected to SST devices, both DP and non-DP transport DFPs, and local stream sinks with virtual DP peer devices equipped with DPCD registers. (See Section 2.6.1.1.2 for details regarding Virtual DP Peer Device DPCD registers.)

Figure 2-82 illustrates an example of a multi-function MST Branch-Sink device with one MST-capable DPTX port, two MST-capable DP++ TX ports, one HDMI TX port, and one local stream sink. DP++ TX Port 1 has neither a downstream device nor level-shifting dongle connected in this example.

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Figure 2-82: Multi-function Branch-Sink Device Example

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Figure 2-83 shows how this multi-function MST Branch-Sink device enumerates the following topology to the DP MST Source device:

- DP++ TX Port 2 with a DP SST monitor connection enumerated as a virtual DP-to-DP peer device with Virtual DPCD register set
- HDMI TX Port enumerated as Virtual DP-to-HDMI Protocol Converter peer device with Virtual DPCD register set
- The local stream sink enumerated as Virtual DP Sink peer device with Virtual DPCD register set

Figure 2-83: Example Multi-function MST Branch-Sink Device Enumeration

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Figure 2-84 shows the enumeration after DP SST Monitor 1 is plugged to DP++ TX Port 1. After the plugging of a DP SST device, the multi-function MST Branch-Sink device changes DP++ TX Port 1 to a Virtual DP-to-DP peer device with a Physical DPTX Port that has a DP SST peer device, and then issues a Connection Status Notify (CSN) message transaction to the DP MST Source device.

If a level-shifting dongle been plugged to the DP++ TX Port 1, the multi-function MST Branch-Sink device would have changed DP++ TX Port 1 to a Virtual DP-to-HDMI peer device.

Figure 2-84: Enumeration after DP SST Monitor 1 Plugged

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The DP MST Source addresses each of the virtual peer devices and connected downstream DP devices (which are physical DP peer devices) using RAD, as defined in Section 2.5.3.

For example, a DP MST Source device may simultaneously do the following:

- Enable DSC Decompression capability of Virtual DP-to-DP Peer Device 1 (because the DP SST device connected to it is not DSC Decompression-capable),
- Disable DSC Decompression capability of Virtual DP-to-DP Peer Device 2, and
- Enable DSC Decompression capability of its downstream DP SST device

Such control granularity by the DP MST Source device is possible by setting both the virtual and physical DPCD register bits by way of REMOTE_DPCD_RD and REMOTE_DPCD_WR message transactions, as illustrated in Figure 2-85.

Figure 2-85: DSC Decompression Operation Control by way of Virtual/Physical DPCD Register Setting

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2.6.1.1.2 DPCD Registers Relevant to Virtual DP Peer Devices

Table 2-132 lists the DPCD registers pertinent for use with virtual DP peer devices. As for the remaining DPCD registers, a multi-function MST Branch device shall replay with the DPCD register values of the DPRX of its MST BU.

Table 2-132: DPCD Registers Relevant to Virtual DP Peer Devices

DPCD Address	Bit #	Definition	AUX CH Read/Write from DPTX
00005h	**DOWN_STREAM_PORT_PRESENT**		Read Only
	0	**DFP_PRESENT** 0 = Device is a virtual DP Sink peer device and has DFP(s). 1 = Device is another type of virtual DP peer device and has DFP(s).	
00007h	**DOWN_STREAM_PORT_COUNT**		Read Only
	3:0	**DFP_COUNT** 0h for a virtual DP Sink peer device. 1h for other virtual DP peer devices.	
	6	**MSA_TIMING_PAR_IGNORED** Virtual DP peer devices that support the Ignore MSA option shall set this bit as described in Section 2.2.4.1.1.	
00008h	**RECEIVE_PORT0_CAP_0** Virtual DP peer devices that support the MSA Horizontal Blanking Expansion option shall program this register as described in Section 2.2.4.1.2.		Read Only
00009h	**RECEIVE_PORT0_CAP_1** Virtual DP peer devices that support the MSA Horizontal Blanking Expansion option shall program this register as described in Section 2.2.4.1.2.		Read Only
00060h through 0006Ch	**DSC Capabilities**		Read Only
00080h through 00083h	**Detailed Capabilities Info** Detailed capabilities information for the DFP(s) of the virtual DP peer device.		Read Only
00107h	**DOWNSPREAD_CTRL**		Read/Write
	7	**MSA_TIMING_PAR_IGNORE_EN** This bit can be set to 1 only if the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) is set to 1.	
00160h	**DSC ENABLE**		Read/Write
00200h	**SINK_COUNT** Used by virtual DP-to-non-DP peer device to indicate connection of the non-DP downstream device.		Read Only

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Table 2-132: DPCD Registers Relevant to Virtual DP Peer Devices (Continued)

DPCD Address	Bit #	Definition	AUX CH Read/Write from DPTX
0020Fh and 02011h	**DSC STATUS**		Clearable Read Only
00240h through 00245h	**TEST_CRC-related registers**		Read Only
03030h through 03034h	**Downstream HDMI Link Status Reporting-related registers**		Read Only
03050h through 03053h	**DVI/HDMI Mode Configuration and Pixel Processing Configuration-related registers**		Read/Write
03054h through 03059h	**OUTPUT_HTOTAL/_HSTART/_HSP_HSW** For Horizontal Blanking Expansion operation as described in Section 2.2.4.1.2.		Read/Write

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2.6.1.1.3 DSC Resource Management of DSC-capable Multi-function DP MST Branch Device

A multi-function DP MST Branch device may have multiple virtual DP peer devices with DSC decompression capability. This section describes the policy of DSC resource management among multiple virtual DP peer devices with DSC decompression capability.

The capability of DSC engine (consisting of one or more DSC decoder units) is exposed in the following registers (see Section 2.7 for details):

- Peak DSC throughput at DPCD Address 0006Bh
- DSC slice capabilities at DPCD Addresses 00064h and and 0006Dh
- DSC maximum slice width at DPCD Address 0006Dh

A multi-function DP MST Branch device with multiple virtual DP peer devices with DSC capability shall expose fixed DSC capability upon connection of a Sink device and persists for the duration of the connection. The multi-function DP MST Branch device shall manage the DSC unit resource and assign DSC units to a DSC engine when a port is connected based on its own policy.

An upstream DP MST DSC Source device shall rely on the DSC capability exposed by the multi-function DP MST Branch device in the DSC capability DPCD registers listed above.

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2.6.2 Link Timing Generation Based on Multi-Stream Transport Packet

The DPTX enables an MST mode by setting the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) to 1 via Native AUX write after having verified that its downstream DPRX has the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) set to 1.

In SST mode, Main-Link timing is governed by the timing of the main stream the link it is transporting in that the BS/SR symbol insertion interval is dictated by the horizontal period of the main video stream. The TU (transfer unit), the vessel of micro-packets in SST mode, is transported only during main video stream active period. In MST mode, Main-Link timing is self-generated and is not governed by the timing of the transported streams. The vessel of micro-packets is called MTP (Multi-Stream Transport Packet). The MTP is 64 link-symbol cycles (i.e., 64 time slots) long, starting with MTP Header in the first time slot (or Time Slot 0), and is constantly transported, regardless of the presence/absence of streams.

Main-Link Symbol Manager of DPTX inserts SR Control Symbol to MTP Header time slot every 1024th MTP as a Link Frame boundary marker, resulting in SR insertion interval of 2^{16} time slots, as shown in Figure 2-86.

Figure 2-86: Link Timing Generation in MST Mode

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2.6.2.1 MST Link Timing Generation with FEC Encoding/Decoding Enabled

New to *DP v1.4*.

When FEC encoding/decoding is enabled (see Section 3.5.1.5), a DPTX Link Layer shall insert FEC parity place holder and parity marker (FEC_PARITY_PH and FEC_PM, respectively) link symbols. The number of FEC_PARITY_PH and FEC_PM link symbols shall be as follows:

- **1-lane configuration**
  - 12 FEC_PARITY_PH link symbols inserted after 500 Link Layer link symbols
  - Every 128th set of 12 FEC_PARITY_PH link symbols followed by an FEC PM link symbol
- **2- and 4-lane configurations**
  - Six FEC_PARITY_PH link symbols inserted after 250 Link Layer link symbols
  - Every 256th set of six FEC_PARITY_PH link symbols followed by an FEC PM link symbol

The transmission of the FEC parity symbols is strictly periodic and is agnostic to Link Layer link symbol transmission being interrupted by the inserted FEC parity symbols.

The Link Layer link symbol transmission timing, including SR Symbol transmission timing, is skewed due to FEC_PARITY_PH and FEC_PM link symbol insertion.

2.6.3 Symbol Sequence Mapping into VC Payload

The Payload Bandwidth Manager of each DPTX in the path from a DP Source to a target Sink device allocates time slots within the MTP to a VC Payload to establish the virtual channel for transporting a stream.

When no time slot is allocated for any VC Payload, all 63 non-MTPH time slots are filled with data 0x00 (before data scrambling), as shown in Figure 2-87.

Figure 2-87: Time Slot Allocation to VC Payload

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Two types of Symbol Sequences are mapped to the VC Payload time slots:

- Stream Symbol Sequence generated by VC Payload Mapper of a DP Source device
- VC Payload Fill (VCPF) Symbol Sequence generated by Main-Link Symbol Manager of a DP Source device and DP Branch devices

A Stream Symbol Sequence generator is present only in a DP Source device. A DP Branch device generates VCPF Symbol Sequence, but no a Stream Symbol Sequence. Rather, the DP Branch device forwards the Stream Symbol Sequence received from the upstream DP device. When there is no Stream Symbol Sequence to forward, the Branch device transmits the VCPF Symbol Sequence it generates.

Both Symbol Sequences consist of a unit of four symbols, regardless of lane count, as shown in Figure 2-88.

Upon the establishing a new VC Payload, a DPTX sends VCPF Symbol Sequence as the default symbol sequence for at least 16 MTPs before starting the transmission of Stream Symbol Sequences. When there is no Stream Symbol Sequence to insert, the DPTX continues transmitting VCPF Symbol Sequence.

Figure 2-88: VC Payload Symbol Generator of a DP Source Device

When a DPTX is driving four lanes, the 4-symbol sequence unit – Sym_x, Sym_y, Sym_z, and Sym_aa (Sym = C for Control Symbol, and D for Data Symbol) – is mapped into the single time slot in the VC Payload time slots. For 1- and 2-lane configurations, the 4-symbol sequence unit is sequentially mapped, as shown Figure 2-89.

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Figure 2-89: 4-Symbol Sequence Unit Mapping to Main-Link Lanes

The 4-symbol sequence unit pattern repeats itself when the VC Payload for a given stream is concatenated, as shown in Figure 2-90. As can be seen in the diagram, the 4-symbol sequence unit may straddle the VC Payload boundary of a given stream in an MTP.

Figure 2-90: Repetition of 4-Symbol Sequence Unit Example for 1-Lane Main-Link

Table 2-133 summarizes the VC Payload Control Symbol Sequences.

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Table 2-133: Summary of VC Payload Control Symbol Sequence

VC Payload Control Symbol Sequence[a]	Symbol Name	Control Code Sequence
VC Payload Fill Control	VCPF	C0-C1-C2-C3[b]
Stream Control		
Stream Framing Control	BS	C0-C0-C0-C0
	BE	C1-C1-C1-C1
	SS	C3-C3-C3-C3
	SE	C6-C6-C6-C6
Stream Fill Control	SF	C4-C4-C4-C4

a. VCPF symbols are generated either by a DP Source device for rate governing, or a DP Branch device when there is no stream symbol from the upstream device to forward to the downstream link. Stream symbols are generated by a DP Source device, not a DP Branch device.

b. C0, C1, C2, and C3 correspond to Sym_x, Sym_y, Sym_z, and Sym_aa, respectively, in Figure 2-89.

The subject of Control Code to ANSI 8b/10b K code mapping is described in Section 2.6.9.

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2.6.3.1 VC Payload Fill Symbol Sequence

The VC Payload Fill (VCPF) Symbol Sequence inserted by Main-Link Symbol Manager consists of four Control Symbols, as shown in Table 2-133.

When no Stream Symbols to transmit while the link is enabled, the DPTX repeats sending VCPF Symbol Sequence.

The VCPF Symbol Sequence is the only control sequence designed to allow for robust detection of the correct phase in the presence of bit errors. A single, isolated bit error cannot convert a non-VCPF Symbol Sequence into a false VCPF Symbol Sequence. With all other control sequences, a single bit error could cause a phase detection error. DPRX devices must use only the VCPF Symbol Sequence to detect the phase of the 4-symbol sequence unit mapping to Main-Link lanes in the 1- and 2-lane cases. DPRX devices must continuously implement phase error correction to ensure recovery from any loss of 4-symbol sequence phase lock.

2.6.3.2 Stream Symbol Sequence

Stream Symbols consist of Data Symbols and Control Symbols.

2.6.3.2.1 Control Symbols

- Stream Framing Control Symbols (namely BS, BE, SS, and SE)
- Stream Fill Control Symbols
  - SF symbols are inserted when Rate Governor in a DP Source device selects Stream Symbol Sequence Generator side of Payload multiplexer (see Figure 2-88), but VC Payload Mapper has no meaningful Stream Symbol Sequence to insert.
  - During the blanking period of the main video stream, SF symbols are inserted by a DP Source device by default as there are no meaningful Stream Symbol Sequences to insert. Those SF symbols during the blanking period are replaced with Stream Framing Control Symbols, VB-ID packet (namely VB-ID, Mvid7:0, and Maud7:0, immediately following the BS Control Symbol Sequence), MSA SDP, and SDPs.
  - VB-ID, MSA SDPs, and SDPs must not contain SF codes – i.e., after the start of these packet types, no SF codes must be inserted until the complete packet has been transmitted; the only exception is for SF within an active video line during nested SDP packet transmission, because SDP transmission does not resume until after BS/VB-ID transmission.

Control Code Sequence of the Stream Control Symbols is listed in Table 2-133.

In SST mode, every 512th BS is replaced with SR for scrambler reset. In other words, BS is used not only as Stream Framing Control Symbol (blanking start, corresponding to Display Enable falling edge of the main video stream), but also as Link Timing Control Symbol (i.e., SR as the Link Frame boundary and BS as the Link Line boundary). To enhance BS and SR Control Symbol error immunity, Enhanced Framing Symbol Sequence must be used for BS and SR with SST transport format, as described in Section 2.2.1.2.

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In MST mode, the Link Frame boundary (SR, inserted once in 2^{16} time slots) is completely de-coupled from the timing of the stream the link is transporting. The BS symbol sequence is used only as a Stream Framing Control Symbol and is never replaced with SR. The BS symbol sequence consists of four symbols, regardless of the lane count.

Note: *There is no Control Symbol marking the Link Line boundary in the MST mode. It should be noted, however, that a notion of a Link Line may be established for any upper layer protocol that requires Link Line boundary by setting the Link Line boundaries relative to the Link Frame boundary, which is fixed to 2^{16} time slots. For example, there are 32 Link Lines per Link Frame if the Link Line interval is set to 32 MTPs.*

2.6.3.2.2 Data Symbols

- Main Stream Data Symbols
- VB-ID packet (VB-ID/Mvid7:0/Maud7:0)
- MSA SDP Data Symbols
- SDP Data Symbols including Parity Byte Symbols

Stream Data Symbol mapping of MST mode is identical to that of SST mode in 4-lane Main-Link configuration.

The AV stream is mapped into VC Payload time slots of the stream as shown in Figure 2-91 in MST mode, regardless of the Main-Link lane count that the DPTX is driving. In case the lane count is one or two lanes, the Lane Count Adjust block (Figure 2-88) sequentially maps to the lane count, as shown in Figure 2-89.

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Figure 2-91: AV Stream Mapping in MST Mode After VC Payloads for a Given Main Video Stream are Concatenated and VC Payload Fill Symbol Sequences Removed

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2.6.3.3 SDP Transport in MST Mode

Figure 2-92, Figure 2-93, and Figure 2-94 show the logical block diagrams of Stream-to-VC Payload Mapping Layer of DP Source, Sink, and Branch devices, respectively.

Figure 2-92: DP Source Device VC Payload Mapping Logical Block Diagram

Figure 2-93: DP Sink Device VC Payload Mapping Logical Block Diagram

Figure 2-94: Pass-through DP Branch Device VC Payload Mapping Logical Block Diagram

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From a stream interface standpoint, the VC Payload Mapping Layer is analogous to the Stream-to-Link Symbol Mapping Layer of SST mode. MST mode extension de-couples the transport from the stream generation, but re-uses the part of the structure of the Stream-to-Link Symbol Mapping Layer in SST mode to allow for commonality in implementation of the MST and SST systems. As is the case with Stream-to-Link Symbol Mapping Layer in SST mode, VC Payload Mapping Layer can receive a main stream and one or more SDP streams.

There are three notable differences between MST and SST modes concerning SDP transport:

- Number of time slots available for SDP transport
- Support for SDP splitting – normative feature for MST-capable DP Branch/Sink devices
- Transport of SDP-only without a main stream

2.6.3.3.1 Number of Data Symbols Available for SDP Transport (Informative)

In MST mode, the Main-Link Symbol Mapper of the DPTX reads symbols from VC Payload Mapper in a DP Source device on every link symbol clock edge when the Rate Governor selects the Stream Symbol Sequence Generator side of Payload multiplexer during the VC Payload time slots for the stream. When there is no main stream data and VB-ID packet/MSA packet to transmit, SDP may be transported.

This sub-section is informative as the number of SDP payloads to be transported is dependent on how the Source device packs the SDP. In this section, the example is shown where the SDP payload size is fixed to 32 bytes. Concatenating the payloads within a single SDP reduces the time slot usage overhead for SDP header and SE symbol insertion, and thus increases the data symbols available for SDP payload transport.

The number of MTPs per main video stream horizontal blanking period (MtpCntPerHBlank) is:

$$MtpCntPerHBlank = \frac{t_HBlank}{64 * t_TimeSlot}$$

where:

- t_HBlank is the main video stream horizontal blanking period
- t_TimeSlot is the link time slot period (i.e., the Link Symbol Clock period)

The number of Stream Symbols per t_HBlank (StrmSymblCntPerHBlank) is:

$$StrmSymblCntPerHBlank = MtpCntPerBlank * Throttled_VCP_Size * LaneCnt$$

where:

- LaneCnt is the lane count of the Main-Link

During t_HBlank, BS, VB-ID packet, and BE symbol sequence must be sent, resulting in 20 of StrmSymblCntPerHBlank used for these symbols. Therefore, the number of Stream Symbols available for SDP is as follows:

$$StrmSymblCntForSdpPerHBlank = StrmSymblCntPerHBlank - 20$$

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SDP data has an overhead of SS, SE, Header, and Parity. SdpDataEfficiency is:

$$SdpDataEfficiency = \frac{SdpDataSize}{SdpDataSize + SdpOverhead}$$

When the SDP data size is 32 bytes, for example, the total overhead is 24 bytes. Therefore, SdpDataEfficiency becomes:

$$SdpDataEfficiency = \frac{32}{32 + 24} = \frac{4}{7}$$

The number of symbols available for SDP Data per t_HBlank (SdpDataSmbCnt) is:

$$SdpDataSmbCnt = StrmSymblCntForSdpPerHBlank * SdpDataEfficiency$$

The resulting SdpDataRate is:

$$SdpDataRate = SdpDataSmbCnt / t_HPeriod$$

The SdpDataRate must be equal to or larger than the peak data rate of the stream packed into the SDPs.

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2.6.3.3.2 SDP Splitting in MST Mode

Note: *Support for SDP splitting in SST mode is discussed in Section 2.2.5.12.*

In MST mode, a DP Source device has an option of SDP splitting. SDP splitting is the process of splitting SDPs with a main stream including BE/BS symbol sequence, associated data (VB-ID/ Mvid7:0 /Maud7:0), and MSA packet, as shown in Figure 2-95.

Only one level of splitting is allowed in MST mode. SDP splitting by another SDP is prohibited. The SDP stream may be interrupted at any time, and may additionally be interrupted more than once (e.g., in the case where the horizontal blank is short and secondary packet length is long). Interruption and resumption of the SDP must take place at the 4-symbol sequence boundary.

A DP Sink device in MST mode must be capable of reassembling the nested SDP.

Figure 2-95: SDP Splitting in MST Mode

2.6.3.3.3 SDP-only Transport without Main Stream

MST mode, as is the case with SST mode, supports the transport of SDP-only stream without a main stream, such as an audio-only stream without a main video stream. In this condition, BS Control Symbol Sequence followed by VB-ID packet is inserted every 1024th time slot of the VC Payload where the SDP is transported.

2.6.3.3.4 No SDP/Main Stream

Even if neither a SDP stream nor main stream is being sent, the BS Control Symbol Sequence followed by VB-ID packet is inserted every 1024th time slot of the VC Payload replacing SF Symbol Sequences as long as the DP Source device sets the Rate Governing block to select the Stream Symbol Generator side of VC Payload Multiplexer. The DP Source device may stop the insertion of Stream Symbols by always selecting the VCPF Symbol Sequence (which is by setting the TARGET_Average_StreamSymbolTimeSlotsPerMTP to 0.0, as described in the next section).

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2.6.4 Time Slot Count Allocation to VC Payload

Aside from the MTP Header time slot, the remaining 63 time slots of the MTP are available for allocation to one or multiple VC Payloads. The layer that manages the allocation of the time slots to VC Payloads is the Payload Bandwidth Manager.

There are two types of Payload Bandwidth Managers:

- One in an MST DP Source device, called “Source Payload Bandwidth Manager”
- One in MST DP Branch devices, called “Branch Payload Bandwidth Manager”

Working together, Source and Branch Payload Bandwidth Managers make sure of the following:

- Allocate sufficient bandwidth to the VC Payloads constituting the virtual channel from the Source device to the target Sink device for transporting a stream without causing overflow of buffers in the path
- Minimize the VC Payload bandwidth allocation overhead so that the number of streams transported over the DP links can be maximized

Source Payload Bandwidth Manager has the following responsibilities:

- Determine the peak bandwidth of a stream it needs to transport
- From the peak stream bandwidth, calculates the Payload Bandwidth Number (or PBN) value for the stream to be transported and passes the PBN value to the downstream Branch devices via ALLOCATE_PAYLOAD message transaction
- Calculate the VC Payload size in time slot count of the link it is driving and throttles the Stream Symbol Sequence insertion rate so that transmission of the Stream Symbol Sequence is evenly distributed over multiple MTPs

Branch Payload Bandwidth Manager has the following responsibility:

- Upon receiving the PBN value, calculates the smallest possible VC Payload size in time slot count of the link it is driving that provides for sufficient bandwidth for the PBN value

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The interaction between Source Payload Bandwidth Manager and Branch Payload Bandwidth Manager is shown in Figure 2-96.

Figure 2-96: Bandwidth Management by Payload Bandwidth Manager

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2.6.4.1 PBN Value Calculation by a Source Device Payload Bandwidth Manager

The PBN is an integer number calculated by Source device Payload Bandwidth Manager representing a peak bandwidth of a stream to be transported in a VC Payload. The PBN value has the unit of 54/64MBps.

Note: *The unit of 54/64MBps is an arbitrary unit chosen based on common multiplier to render an integer PBN for all link rate/lane counts combinations*

The Source Payload Bandwidth Manager calculates a PBN value using a peak stream bandwidth value. The calculated value is likely to have a fraction. The Source Payload Bandwidth manager adds 0.6% margin to the calculated fractional PBN value and rounds it up to the nearest integer. This integer PBN value is the one the Source Payload Bandwidth Manager passes to downstream Branch devices.

The 0.6% margin accounts both for the deviation of the link rate driven by a downstream DP Branch device (as small as nominal link rate minus 5300ppm, or 0.53%, including link rate down-spreading) and of the link rate driven by the DP Source device itself (as large as nominal link rate plus 300ppm, or 0.03%).

The following example show how the PBN value is determined for a pixel stream with the pixel rate of 154MP/s (i.e., WUXGA, 1920x1200 at 60Hz of vertical frame rate with reduced horizontal blanking) and the pixel data size of 30 bits per pixel (or 3.75 bytes per pixel).

$$
\begin{aligned}
&PeakPixelBandwidth \\
&= 154MHz * 30BitsPerPixel / 8BitsPerByte \\
&= 577.5MBps \\
&= 577.5MBps * \frac{1}{54/64MBps / PBN} \\
&= 684.444PBN \\
&ADDITION_OF_0.6\%_MARGIN \\
&CEIL\ (684.444 * 1.006) = 689PBN
\end{aligned}
$$

2.6.4.1.1 PBN Value Calculation with FEC Encoding/Decoding Enabled

New to *DP v1.4*.

FEC overhead of 2.3%, downspreading overhead of 0.5%, and MST Branch device link reference clock difference of up to 0.06% (= 600ppm) add up to approximately 3% total overhead.

A DP Source device in MST mode shall use the following equation to calculate the effective PBN value to be communicated to the downstream devices by way of ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD message transactions from the native PBN value derived from the pixel rate and pixel bit depth.

$$PBN_EFFECITVE = PBN_NATIVE * 100/(100 - 3)$$

A DP Source device in MST mode shall evenly distribute the additional valid pixel data symbols across its VC Payload time slots, per MTP, to account for the time slots occupied by FEC parity symbol transmission.

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A DP Source device in MST mode may not set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 when it is not enabling FEC encoding for the purpose of avoiding the 2.3% FEC overhead. When the DP Source device in MST mode makes that choice, it has to set the FEC_READY bit and initiate Link Training before enabling FEC.

2.6.4.2 VC Payload Size Determination by Branch Payload Bandwidth Manager

The unit of the PBN value simplifies the task of determining the VC Payload size in time slot count for the Branch Payload Bandwidth Manager. The Branch Payload Bandwidth Manager determines the VC Payload size in time slot count per MTP as follows:

$$VCPayload_Size_Branch = CEIL\ (PBN_Value\ /\ VCPayload_Bandwidth_for_OneTimeSlotPer_MTP_Allocation)$$

For example, a 4-lane Main-Link at RBR (1.62Gbps) has a link bandwidth of 648MBps. When the Branch Payload Bandwidth Manager allocates one time slot per MTP to a VC Payload, the resulting VC Payload Bandwidth is 648MBps * 1 time slot/64 time slots, which is equal to 12 * 54 / 64MBps or 12 PBN.

For the above pixel stream with the PBN value of 689, the Branch Payload Bandwidth Manager driving its downstream Main-Link at RBR over 4 lanes sets the VC Payload size in time slot count per MTP, as follows:

$$VCPayload_Size_Branch = CEIL\ (689PBN\ /\ 12PBN\ /\ TimeSlotPerMTP) = 58TimeSlots/MTP$$

The DPTX of a Branch device may be driving the link at a rate lower than the nominal link rate due to down-spread (0.5% maximum from the nominal) and the reference clock variation (±300ppm or ±0.03% from the nominal). As noted earlier, the Source device Payload Bandwidth Manager adds 0.6% margin when it calculates to account for those deviations.

The VC Payload bandwidths in PBN value when one time slot is allocated per every MTP for various link configurations are shown in Table 2-134.

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Table 2-134: VC Payload Bandwidth for One Time Slot per MTP Allocation for Various Link Configurations

Link Type	# of Lanes	Nominal Link Bandwidth (excluding ANSI 8b/10b channel coding overhead) (MBps)	VC Payload Bandwidth when one time slot per every MTP is allocated (PBN)
HBR3	1	810	15
	2	1620	30
	4	3240	60
HBR2	1	540	10
	2	1080	20
	4	2160	40
HBR	1	270	5
	2	540	10
	4	1080	20
RBR	1	162	3
	2	324	6
	4	648	12

2.6.4.3 VC Payload Size Determination by a Source Payload Bandwidth Manager

As noted earlier, it is only a DP Source device that generates Stream Symbol Sequences. The Source Payload Bandwidth Manager calculates the average Stream Symbol time slots per MTP over the link it is driving (i.e., between the Source device and the first device with a Branching Unit) as follows:

$$Average_StreamSymbolTimeSlotsPerMTP = PeakStreamBandwidth / LinkBandwidth * 64$$

The Source Payload Bandwidth Manager rounds up the Average_StreamSymbolTimeSlotsPerMTP to set the VCPayload_Size_Source, as follows:

$$VCPayload_Size_Source = CEIL\ (Average_StreamSymbolTimeSlotsPerMTP = PeakStreamBandwidth / LinkBandwidth * 64)$$

The Source Payload Bandwidth Manager throttles Stream Symbol insertion rate so that the average of Stream Symbol time slots per MTP is evenly distributed to TARGET_Average_StreamSymbolTimeSlotsPerMTP:

$$TARGET_Average_StreamSymbolTimeSlotsPerMTP = TS_INT + TS_FRAC_enum / TS_FRAC_denom$$

where TS_INT is an integer, and TS_FRAC_enum / TS_FRAC_denom is a simplified fraction.

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The TARGET_Average_StreamSymbolTimeSlotsPerMTP value must not be smaller than the Average_StreamSymbolTimeSlotsPerMTP. The TARGET_Average_StreamSymbolTimeSlotsPerMTP may be higher than the Average_StreamSymbolTimeSlotsPerMTP, as long as the following condition is met:

$$Maximum_TARGET_Average_StreamSymbolTimeSlotsPerMTP \leq PBN_Value_to_DownstreamBranchDevices \,/\, (LinkBandwidth_Source * 54)$$

where LinkBandwidth_Source is the bandwidth of the link Source device is driving.

For 4-lane Main-Link, the number of Stream Symbol time slots per MTP fluctuates between TS_INT and [TS_INT + 1] over the TS_FRAC_denom MTPs. TS_FRAC_enum MTPs have [TS_IN + 1] Stream Symbol time slots and [TS_FRAC_denom - TS_FRAC_enum] MTPs have TS_INT Stream Symbol time slots. Those TS_FRAC_enum MTPs with [TS_INT + 1] Stream Symbol time slots must be evenly distributed over TS_FRAC_denom MTPs.

For 1- and 2-lane Main-Link configurations, the fact that Symbol Sequences are 4-symbol multiples affects how the Stream Symbols insertion rate get throttled. Over the [TS_FRAC_denom * 4 / LaneCount] MTPs the Stream Symbols per MTP must be evenly distributed to TARGET_Average_StreamSymbolTimeSlotsPerMTP value.

When the PeakStreamBandwidth is 577.5MBps and when the bandwidth of the link Source device is driving is 1080MBps (i.e., 4-lane HBR):

$$Average_StreamSymbolTimeSlotsPerMTP = 577.5MBps \,/\, 1080MBps * 64 = 34.222$$

Therefore, the Source Payload Bandwidth Manager sets the VCPayload_Size_Source to 35 time slots. The maximum allowed TARGET_Average_StreamSymbolTimeSlotsPerMTP is:

$$Maximum_TARGET_Average_StreamSymbolTimeSlotsPerMTP = 689 * 64 * (54/64) / 1080 = 34.45$$

So, the Source Payload Bandwidth Manager may set the TARGET_Average_StreamSymbolTimeSlotsPerMTP to 34.25, that is, TS_INT = 34, TS_FRAC_enum = 1, TS_FRAC_denom = 4.

One out of four MTPs has 35 Stream Symbol time slots with 0 VCPF Symbol time slots within the VC Payload. Three out of four MTPs have 34 Stream Symbol time slots with 1 VCPF Symbol time slot.

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2.6.4.3.1 Maximum Allowed Rate Governing Deviation from Target Average for a Source Device

A DP Source device must throttle the Stream Symbol insertion rate so that the accumulation of transmitted stream symbol count is in the following range at the beginning of any MTP:

$$ACTUAL_AccumulatedSymbolCount > TARGET_AccumulatedSymbolCount - 8$$
$$ACTUAL_AccumulatedSymbolCount \leq TARGET_AccumulatedSymbolCount$$

The remainder of this sub-section describes the rationale behind the maximum allowed rate governing deviation above and should be regarded as informative.

For each MTP, the target number of transmitted Stream Symbols for a given VC Payload is *M*:

$$M = LaneCount * (TS_INT + TS_FRAC_ENUM / TS_FRAC_DENOM)$$

For each MTP, the actual number of transmitted Stream Symbols is *N*:

$$N = \sum_{\substack{TimeSlots \\ inVCPayload}} (LaneCount - RG)$$

where RG = 4 if the time slot is occupied by the first VCPF code (VCPF0, or C0), and RG = 0 otherwise. Note that VCPF Symbols occupy 4/LaneCount time slots so the fact that *N* temporarily decreases for LANE_COUNT smaller than 4-inches represents the fact that a decision to introduce VCPF0 on a given time slot will cause subsequent time slot(s) to be occupied by the remaining VCPF codes (C1, C2, and C3). (Note that an insertion of VCPF Symbol in a VC Payload in one MTP may span to the VC Payload of the next MTP in case of 1- and 2-lane Main-Link.)

Compute the accumulation of delta D between target and actual numbers of transmitted symbols:

$$D = \sum_{MTPs} (N - M)$$

The *D* value is per MTP, not per time slot in a given MTP.

Insert VCPF0 (the first code of VCPF Symbol Sequence) if and only if D will otherwise exceed zero.

Summarizing:

$$D = \left(\sum_{MTPs} \left(\sum_{\substack{TimeSlots \\ inVCPayload}} (LaneCount - RG) - LaneCount * (TS_INT + TS_FRAC_ENUM / TS_FRAC_DENOM) \right) \right)$$

where RG = 0 or 4.

The limit on the variability of D is determined by the following factors:

- Because symbols are inserted in sets of four and the constraint $D \leq 0$ must be met, the VCPF insertion algorithm must insert VCPF symbol if and only if the D value on the current time slot would be less than four with a VCPF symbol inserted. The resulting variability is $-4 < Delta1 \leq 0$.

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- Because VCPF symbols are inserted in sets of four, in the 1-lane case a decision to insert VCPF0 will result in VCPF1 through VCPF3 in the next three allocated time slots. The resulting variability is $-3 \leq Delta2 \leq 0$. In the 2-lane case, only the next allocated time slot after the start of VCPF Symbol Sequence will contain VCPF symbol, and in the 4-lane case, each VCPF Symbol Sequence is transmitted completely within the single time slot.

Adding up Delta1 and Delta2, $-7 < Delta1 + Delta2 \leq 0$, determines the minimum possible variability range for D. For simplicity (because all symbols are managed in sets of four at the Stream to VC Payload Mapping Layer), the range of D (when measured at the start of an MTP) is constrained to:

$$-8 < D \leq 0$$

Thus, the contribution to the rate variability observed at the DPRX due to rate governing in the Source device is eight symbols.

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2.6.4.3.2 Rate Governing Sample Pseudo-Code (Informative)

The following pseudo-code is provided to show how rate governing could be implemented with a simple state machine.

Note: *This example implementation is for reference purposes only.*

RG Parameters:

```
   D // range of D is -256 to 0 so 8 integer (no sign) bits are
required; number of fractional bits is equal to number of bits
of Y value
   X.Y // X.Y calculated by multiplying
TARGET_Average_StreamSymbolTimeSlotsPerMTP by Lane Count. X is an
8-bit value in the range 0 to 252, Y is implementation-dependent
but should be at least 2 bits and ideally more
```

Other Parameters (not specifically for rate governing but referenced below):

```
  PHASE // 2-bit value to represent the four phases in the single-lane
case, or two phases in two-lane case
  LANE_COUNT // 2-bit value; 1 = 1-lane, 2 = 2-lane, 0 = 4-lane
```

Initial condition and no time slot allocated to a VC Payload:

```
  Set D = 0
  Set X.Y = 0
  Set PHASE=0
```


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At least sixteen symbols after ACT for new VC Payload time slot allocation, and any time for existing or reallocated VC Payload:

```
  Update X.Y to nonzero value (new X.Y automatically takes effect on
next MTPH)
If MTPH Time Slot
{
  D = D - X.Y
}
else if VC Time Slot
{
  if PHASE = 0  // Only decide whether to start RG or VC data on phase
zero since both are transmitted in sets of four
  {
    if D <= -4  // Ensures that four Stream Symbols cannot cause D > 0
    {
     Read (from VC Payload Mapper) and start transmitting set of four
Stream Symbols
     D <= D + 4  // Decrement D by amount of data that will be
transmitted (some may be in subsequent time slots)
    }
    else
    {
      start Rate Governing  // Don't update D since no data was sent
    }
  else
  {
     continue previously started 4-symbol sequence (VCPF Symbols or
Stream Symbols)  // Don't update D since the change in D (if any) in
the PHASE=0 case was already accounted for
  }
  PHASE = PHASE + LANE_COUNT
}
```


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2.6.5 VC Payload Allocation Synchronization Management

Prior to starting a stream transfer from a stream Source to a stream Sink, a Stream Policy Maker, based on the topology map information provided by the Topology Manager, establishes the virtual channel connection between the stream Source and Sink with the help of Payload Bandwidth Managers in the DP Source and Branch devices in the path. The Payload Bandwidth Manager maps the virtual channel to a VC Payload on a DP link.

The Payload Bandwidth Manager establishes and maintains VC Payloads it is receiving and transmitting/forwarding by managing the VC Payload ID Table. The Payload Bandwidth Manager:

- Keeps its VC Payload ID Table synchronized with that of the DPRX of the downstream device it is driving through Native AUX transactions
- Keeps the VC Payload time slot allocation over the Main-Link synchronized with the VC Payload ID Table through an ACT Trigger control sequence inserted into MTP Header time slots

Each DPTX and DPRX of an MST-capable device has a VC Payload ID Table. The table within the DPRX is mapped to the DPCD Address space as shown in Table 2-135. It should be noted that reading of the DPRX's VC Payload ID Table by the immediate upstream DPTX's Payload Bandwidth Manager is not required for normal operation. When to read this table (e.g., for debugging purposes) is an implementation-specific choice for developers of DP Source and Branch devices.

Though it is possible for an upstream device to update the VC Payload ID Table of a remote downstream device via REMOTE_DPCD message transaction, the remote update of a VC Payload ID Table is prohibited. Only the immediate upstream device is allowed to update the VC Payload ID Table of the downstream device because only the immediate upstream device is capable of initiating the ACT Trigger control sequence over the Main-Link.

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Table 2-135: VC Payload ID Table of DPRX Mapped to DPCD Address Space

DPCD Address	Time Slot	VC Payload ID (7-bit value RO)[a]
2C1h	1	1
2C2h	2	1
2C3h	3	1
2C4h	4	1
2C5h	5	1
2C6h	6	3
2C7h	7	3
2C8h	8	3
2C9h	9	3
2CAh	10	3
2CBh	11	3
2CCh	12	3
2CDh	13	3
2CEh	14	4
2CFh	15	4
2D0h	16	4
2D1h	17	4
2D2h	18	4
2D3h	19	4
2D4h	20	4
2D5h	21	4
2D6h	22	5
2D7h	23	5
2D8h	24	5
2D9h	25	5
2DAh	26	5
2DBh	27	0
2DCh	28	0
2DDh	29	0
2DEh	30	0
…	…	…
2FFh	63	0

a. *This table shows an example in which VC Payload ID #2 has been deleted. Time slots with VC Payload ID value 0 are not allocated.*

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The VC Payload ID assignment is uniquely managed by each Payload Bandwidth Manager of a DP device with a DPTX. The Payload Bandwidth Manager of a DP Branch device must maintain the mapping of the VC Payload Mapping Tables of its DPRXs to those of its DPTXs.

The VC Payload ID Table of a DPRX is updated by the Payload Bandwidth Manager of the immediate upstream device, via Native AUX transactions to DPCD Addresses shown in Table 2-136.

Table 2-136: DPCD Address Map for VC Payload Table Update and ACT Status Verification[a]

DPCD Address	Bit #	Definition	Read/Write over AUX CH
001C0h	**PAYLOAD_ALLOCATE_SET** Writing 00h, 00h, and 3Fh to DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively, clears the entire VC Payload ID table. The DPRX, upon this, immediately ignores the incoming VC Payloads (if any) without waiting or ACT on the Main-Link.		Write/Read
	6:0	**VC Payload ID to Be Allocated** ID of 0 indicates that the time slots are unallocated.	
	7	**RESERVED**	Read 0
001C1h	**PAYLOAD_ALLOCATE_START_TIME_SLOT**		Write/Read
	5:0	**Starting Time Slot of VC Payload ID in DPCD Address 002C0h**	
	7:6	**RESERVED**	Read all 0s
001C2h	**PAYLOAD_ALLOCATE_TIME_SLOT_COUNT**		Write/Read
	5:0	**Time Slot Count of VC Payload ID in DPCD Address 002C0h**	
	7:6	**RESERVED**	Read all 0s
002C0h	**PAYLOAD_TABLE_UPDATE_STATUS**		Clearable Read Only
	0	**VC Payload ID Table Updated** 0 = Not updated since the last time that this bit was cleared. 1 = Updated, cleared to 0 when the DP Source device writes 1.	
	1	**ACT Handled** 0 = ACT is not handled since the last time that this bit was read. 1 = ACT is handled, cleared to 0 when the VC Payload ID Table Updated bit (bit 0) is set to 1.	
	7:2	**RESERVED**	Read all 0s

a. *This table duplicates DPCD Address in formation for the registers described here, from Table 2-156 (DPCD Addresses 001C0h through 001C2h) and Table 2-157 (DPCD Address 002C0h).*

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The Payload Bandwidth Manager writes the VC Payload ID, its start location and size in time slot count, via Native AUX write transaction to DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively.

To delete a VC Payload, the Payload Bandwidth Manager writes the VC Payload ID to be deleted to DPCD Addresses 001C0h, its start location before deletion to DPCD Addresses 001C1h, and a value of 00h to DPCD Addresses 001C2h. Clearing the ID to 00h, the start location to 00h, and the size to 3Fh clears the DPRX's entire VC Payload ID Table.

After it has verified that the VC Payload ID Table is updated (VC Payload ID Table Updated bit in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bit 0) is set to 1), the Payload Bandwidth Manager is to trigger the VC Payload allocation over the Main-Link, by inserting an ACT Trigger sequence into four consecutive MCT Header time slots, as shown in Figure 2-97. The ACT sequence is always preceded by the 32 MTPH time slot Encryption Control Field (ECF), as described in Section 2.6.11. The ACT sequence must not be inserted in the following MTPH time slots:

- 36 to 5 MTPH time slots prior to Link Frame boundary SR
- Time slot for SR
- 1 to 34 MTPH time slots following SR

Furthermore, the ACT sequence must not straddle the above keep-out MTPH time slots.

Figure 2-97: ACT Allocation Change Trigger Sequence

The Payload Bandwidth Manager then confirms the successful handling of ACT Trigger Control Sequence by the downstream DPRX by reading the ACT Handled bit in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bit 1, is set to 1).

Using the Native AUX transactions and ACT Trigger Control sequence described above, Payload Bandwidth Manager may add a new VC Payload (new allocation), change a VC Payload size (decrease/increase), or delete a VC Payload (de-allocation). In any event, a Branch device's Payload Bandwidth Manager must eliminate any unallocated time slots in between VC Payloads, as shown in Figure 2-98.

When a DPRX receives an ACT Trigger Control sequence without any change to values at DPCD Addresses 001C0h through 001C2h, the DPRX must not make any changes to the VC Payload allocation.

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Figure 2-98: VC Payload Allocation Change

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2.6.6 ALLOCATE_PAYLOAD Timing Sequence

To synchronize the VC Payload time slot allocation change across the multiple links of the path, Payload Bandwidth Manager issues an ALLOCATE_PAYLOAD Message Transaction. This section describes the timing sequence of interactions among the Payload Bandwidth Manager, Main-Link Symbol Manager, and VC Payload Mapper surrounding an ALLOCATE_PAYLOAD Message Transaction.

An ALLOCATE_PAYLOAD Message Transaction uses the VC Payload ID and PBN values as the variables of this transaction. Optionally, the MST DP Source Device may execute an ENUM_PATH_RESOURCES Message Transaction to check the available PBN value of the path before executing an ALLOCATE_PAYLOAD Message Transaction.

An MST Source device targets both ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD at the last MST device with a branching unit driving a stream sink. In other words, the Payload Bandwidth Manager of a DP Source device sets the Relative Address (RAD) field of the header of the Message Transaction to point to the last MST device with a branching unit. The port number (either physical or logical) of the branching unit to which the Sink device is plugged to is included in the body of the Message Transaction.

When transporting an SDP stream (e.g., an audio stream), the Payload Bandwidth Manager of a DP Source device specifies the SDP stream sink number in the body of the ALLOCATE_PAYLOAD Message Transaction.

A timing sequence for adding a new payload is shown in Figure 2-99. The Payload Bandwidth Manager of each DPTX in the path, upon receiving ALLOCATE_PAYLOAD message transaction, updates the VC Payload ID Table and VC Payload time slot allocation, using the procedures described in Section 2.6.5. Once successful, it forwards the message transaction to its downstream DP device in the path.

When the Payload Bandwidth Manager of a DP Source device verifies that the ACT Trigger Control sequence has been successfully handled by the DPRX of the downstream device, it may set the Throttled_VCP_Size (i.e., X.Y) value to the non-zero value to start the Stream Symbol Sequence insertion at least 16 MTPs after the new VC Payload is established.

The Payload Bandwidth manager of a DP Branch device, upon verifying the successful handling of the ACT Trigger, waits for 16 MTPs after the new VC Payload is established and starts forwarding Stream Symbol Sequence from the upstream DP device.

Figure 2-100 shows a timing sequence for adding a new payload that results in error. Upon receiving NAK Reply Message to ALLOCATE_PAYLOAD message transaction it has initiated, the Payload Bandwidth Manager of the DP Source device issues another ALLOCATE_PAYLOAD with PBN value cleared to 0 to delete the VC Payloads from the links on which the VC Payload allocations have been just completed.

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Figure 2-99: Example Time Sequence for Adding a New Payload

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Figure 2-100: Timing Sequence for Adding a New Payload with Error

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A timing sequence for successfully deleting a payload is shown in Figure 2-101.

Figure 2-101: Timing Sequence for Deleting a Payload

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A timing sequence for deleting a Payload with an error is shown in Figure 2-102. The DP Branch device that has experienced error in allocation change on the link it is driving must first retry to resolve the error condition.

Figure 2-102: Timing Sequence for Deleting a Payload with an Error

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A timing sequence for deleting a Payload with an error that is not locally recoverable by the DP Branch device is shown in Figure 2-103. The DP Branch device must clear the entire VC Payload ID Table and reply with NAK to the DP Source device.

Figure 2-103: Timing Sequence for Deleting a Payload with Locally Unrecoverable Error

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A timing sequence for reducing the VC Payload time slot allocation is shown in Figure 2-104. The DP Source device must reduce the Throttled_VCP_Size value prior to this operation to avoid the overflow in the path. As a result of the Throttled_VCP_Size reduction, the VC Payload ends up transmitting more VCPF Symbol Sequences until the VC Payload Size is reduced following ACT Trigger Control sequence.

Figure 2-104: Timing Sequence for Reducing the VC Payload Allocation

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A timing sequence for increasing the VC Payload time slot allocation is shown in Figure 2-105. The DP Source device must wait, receiving the ACK Reply Message, before increasing the Throttled_VCP_Size value to avoid the overflow in the path.

Figure 2-105: Timing Sequence for Increasing the VC Payload Allocation

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2.6.7 Impacts of Various Events on VC Payload ID Table

The various events and their impacts on the VC Payload ID Table are described in Table 2-137.

Table 2-137: Various Events and Impacts on VC Payload ID Table

Events	Results
ALLOCATE_PAYLOAD, with a new VC Payload ID	Time slots allocated at the end of VC Payload ID Table to support the requested PBN.
ALLOCATE_PAYLOAD, with an existing VC payload ID and with the same PBN value	No change in Payload Allocation table.
ALLOCATE_PAYLOAD, with an existing VC Payload ID, but with a new, non-zero PBN value	The number of time slots allocated to VC Payload ID is adjusted to support the new PBN value. Higher numbered time slots are moved up to make room if new PBN is larger than original PBN. Higher numbered time slots are moved down to remove the gap of unused time slots after the number of time slots was reduced due to new PBN value.
ALLOCATE_PAYLOAD, with an existing VC Payload ID, but with PBN value cleared to 0	Time slots numbered higher than the last time slot used by the VC Payload ID are moved down to the first time slot used by the VC Payload ID, essentially removing the VC Payload ID from the table.
Loss of Stream within a DP Source device	No change in VC Payload ID table. When the rate governing value X.Y is non-zero, the Main-Link Symbol Mapper sends Stream Fill symbols when the Stream Symbols are selected by VC Payload multiplexer. When Payload Bandwidth Manager sets X.Y to 0.0, sends Rate Governing symbols only.
Loss of incoming Stream Symbols or loss of VC Payload symbol sequence phase lock for a DP Branch device	No change in VC Payload ID table. The DP Branch device sends Rate Governing symbols in these conditions.

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Table 2-137: Various Events and Impacts on VC Payload ID Table (Continued)

Events	Results
Loss of link followed by link training	The DP device whose DPRX has detected the link loss (Device D) generates IRQ_HPD to notify the upstream DPTX of "link-lost" status and clears the ACT Handled bit in the PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h, bit 1) while keeping the VC Payload ID table intact on the DFP's DPTX and UFP's DPRX. On its DFP's DPTX, Device D fills the VC Payloads that have been affected by the loss of link with Rate Governing symbol sequence. If there is no subsequent link training to recover the link by the upstream DPTX for extended period (e.g., for a few seconds), the DP device: • Clears the VC Payload ID table of the DPRX port, and • Initiates ALLOCATE_PAYLOAD with PBN value cleared to 0, to delete those VC Payloads that were coming from the port. The DP device whose DPTX has conducted the link training for link maintenance (Device U) first reads the registers at DPCD Addresses 002C0h through 002FFh of the downstream device (Device D). If the registers at DPCD Addresses 002C0h through 002CFh are all cleared to 00h, that is an indication that Device D has cleared the VC Payload ID table. Device U notifies its upstream devices of this event by way of a RESOURCE_STATUS_NOTIFY message transaction. ***Note:*** *Device U does not need to read all the registers at DPCD Addresses 002C0h through 002FFh; reading of DPCD Addresses 002C0h through 002CFh is sufficient.* If the registers at DPCD Addresses 002C0h through 002CFh retain the values previously set by Device U, that is an indication that Device D has retained the VC Payload ID table and Device U attempts for a local recovery. For the local recovery, Device U performs Native AUX write transactions to the PAYLOAD_ALLOCATE_SET, PAYLOAD_ALLOCATE_START_TIME_SLOT, and PAYLOAD_ALLOCATE_TIME_SLOT_COUNT registers (DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively), followed by ACT on Main-Link and Native AUX read transaction for ACT status flag verification to restore time slot allocations to VC Payloads in the same order they existed before link training was required. The time slot allocation stops when there is an insufficient number of time slots remaining for any subsequent VC Payloads. Device U initiates ALLOCATE_PAYLOAD with PBN value cleared to 0 to delete those VC Payloads that have lost the time slots as the result of the link training. In case the link cannot be re-established, it deletes all the VC Payloads. After the local recovery, Device U issues RESOURCE_STATUS_NOTIFY message transaction, in case the link bandwidth has changed as the result of the link training.

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Table 2-137: Various Events and Impacts on VC Payload ID Table (Continued)

Events	Results
Unplug event or receipt of CONNECTION_STATUS_NOTIFY	The DP device whose DPRX has detected the disconnect event (Device D) clears the following registers: • MSTM_CTRL (DPCD Address 00111h) • PAYLOAD_ALLOCATE_SET (DPCD Address 001C0h) • PAYLOAD_ALLOCATE_START_TIME_SLOT (DPCD Address 001C1h) • PAYLOAD_ALLOCATE_TIME_SLOT_COUNT (DPCD Address 001C2h) • PAYLOAD_TABLE_UPDATE_STATUS (DPCD Address 002C0h) The DP device also clears the VC Payload ID table of the disconnected DPRX, then initiates ALLOCATE_PAYLOAD with the PBN value cleared to 0 to delete those VC Payloads that were coming from the disconnected port. The DP device whose DFP's DPTX detected the unplug event (Device U) then deletes the VC Payloads that were being transmitted from the unplugged port. Device U deletes those VC Payloads from the VC Payload ID table of the unplugged DPTX port, then, issues CONNECT_STATUS_NOTIFY message transaction to its upstream devices. DP Source devices, upon receiving CONNECT_STATUS_NOTIFY, delete all the VC Payloads transmitted through Device U with ALLOCATE PAYLOAD with PBN = 0. (CLEAR_VC_PAYLOAD_ID_TABLE may be used in case all the VC Payloads are to be deleted.)
POWER_UP_PHY and POWER_DOWN_PHY	VC Payload ID tables are preserved. Loss of link, when it is preceded by POWER_DOWN_PHY does not result in clearing of VC Payload ID tables.

Notes: *A DP Branch device receiving a POWER_DOWN_PHY executes on it (i.e., write 0x02 to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h)) of the downstream DPRX) only when either none of the VC Payloads on its downstream link is carrying Stream Symbols or there is no VC Payloads. Upon receiving ALLOCATE_PAYLOAD for VC Payload allocation through the link on which POWER_DOWN_PHY has been executed, the DP Branch device must execute POWER_UP_PHY (i.e., write 0x01 to the SET_POWER & SET_DP_PWR_VOLTAGE register).*

Power cycling of the DPTX of an upstream DP device is detected by the DPRX of the downstream DP device as a loss of link without preceding POWER_DOWN_PHY and is handled as such.

Power cycling of the DPRX of a downstream DP device is detected by the DPTX of the upstream DP device as an unplug event and is handled as such.

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2.6.8 Robustness Requirement

There are four aspects to the robustness of the MST mode:

- Link timing robustness through predictable, self-generated link timing
- Trigger Control Sequence robustness in MTP Header time slots
- VC Payload 4-symbol sequence phase locking
- VC Payload symbol robustness through redundancy in symbol transmission, regardless of the lane count

This section describes the DPRX implementation requirements for utilizing the above aspects for improved robustness of the link.

2.6.8.1 Link Timing Robustness

The DPTX must maintain the 2^{16} symbol interval of SR in MST mode following the establishment of Main-Link via Link Training.

The DPRX must make sure the consistency of SR interval before using the SR symbol as the link timing reference point. Besides, the DPRX must disregard the appearance of SR symbol at an unexpected time slot which may result from an intermittent symbol error over Main-Link. The DPRX must wait for four consecutive SRs with 2^{16} time-slot intervals before switching to an SR location different from the original location.

2.6.8.2 Trigger Control Sequence Robustness in MTP Header Time Slot

Because the location of Trigger Control Sequence such as ACT Trigger Sequence is unpredictable, other than it is inserted in MTP Header time slots, the DPTX sends 4-symbol sequence per lane on four consecutive MTP Header time slots.

The DPRX must use this 4-symbol sequence redundancy to properly detect the Trigger Control Sequence even when two out of the four Control Symbols have errors.

2.6.8.3 VC Payload 4-Symbol Sequence Boundary Establishment

The DPRX must establish the 4-symbol sequence boundary and must correct symbols that do not match the Stream Control Symbol Sequence/Rate Governing Symbol Sequence rule.

2.6.8.4 Stream Framing Symbol Sequence Robustness

Stream Framing Symbol Sequence (namely, each of BS, BE, SS, and SE) consists of four consecutive, identical Control Codes. Majority voting after ANSI 8b/10b decoding must be used for robustness. The DPRX must pick the Control Code that appears in two or more symbols in the 4-symbol sequence.

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2.6.9 Control Functions, Control Symbols, and K-Code Assignment

Control Functions consist of sets of defined control symbols or sequences, and are used in both the Main-Link Symbol Management and VC Payload Mapping Layers. To improve link integrity, MST uses 4-symbol sequences to identify all the Data Symbols and those Control Symbols that appear in VC Payload time slots. To minimize emission effects of these 4-symbol codes, the underlying K-codes used are selected using a scrambled index scheme. To maximize error robustness, the remaining Control Functions inserted to MTP Header Time slot are directly mapped to 1-symbol K-codes.

2.6.9.1 Control Functions

Table 2-138 defines control function codes used in the MTP Header time slots. Table 2-139 defines control function codes that may appear within the MTP data payload time slots.

Table 2-138: MTP Header Control Functions

Control Function	Control Symbol	Code/Control Symbol Sequence[a]	Comment
Scrambler Reset	SR	K28.5	Comma character; Link Frame Indicator.
RESERVED	–	K28.1	Not used.
RESERVED	–	K28.7	Not used to avoid coding complication.
RESERVED	–	K28.4	Not used for EMI reduction purpose.
Allocation Change Trigger	ACT	C0-C1-C1-C0	Trigger to downstream device indicating change in allocation on local link. ACT Control Function sequence is unique from others; its 4-code control symbol sequence spans four consecutive MTP Header time slots).

a. Cx indicates an indexed control symbol, as defined in Section 2.6.9.2.

Table 2-139: MTP Payload Control Functions

Control Function	Control Symbol	Control Symbol Sequence (C_*x*, C_*y*, C_*z*, C_*aa*)
Rate Governing	RG	C0-C1-C2-C3
Blank Start	BS	C0-C0-C0-C0
Blank End	BE	C1-C1-C1-C1
End of Chunk	EOC	C2-C2-C2-C2
Secondary Start	SS	C3-C3-C3-C3
Stream Fill	SF	C4-C4-C4-C4
RESERVED	–	C5-C5-C5-C5
Secondary End	SE	C6-C6-C6-C6
RESERVED	–	C7-C7-C7-C7

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2.6.9.2 Control Symbol Index Scrambling

In control symbol index scrambling, for each control symbol Cx, "x" defines a (pre-scrambled) index integer value between 0 and 7. A scrambled index is then calculated using the current contents of the Main-Link data scrambling LFSR as follows:

$$Scrambled\ Index = Index^{\{LFSR[13],LFSR[14],\ LFSR[15]\}}$$

Finally, this scrambled index determines the actual K-code selected, using the mapping provided in Table 2-140.

Table 2-140: Scrambled Index to K-Code Map

Scrambled Index	K-Code
0	K23.7
1	K27.7
2	K28.0
3	K28.2
4	K28.3
5	K28.6
6	K29.7
7	K30.7

2.6.9.3 Data Symbol Scrambling

The data symbol scrambling is identical between MST mode and SST mode. All data symbols are scrambled.

2.6.10 Conversion between MST and SST Symbol Mapping

All DP devices that support MST mode must also support SST mode. This requirement ensures interoperation between an MST device and SST device.

The DPRX capable of supporting MST mode sets the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0). The MST-capable DPTX must first verify whether the downstream DPRX has the MST_CAP bit set, via Native AUX read. If the bit is set and if the DPTX chooses to enable MST mode, then it sets the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0), via Native AUX write of the downstream DPRX set.

For a DP Source device and a DP Sink device, whether to enable MST mode is a policy-making choice. A DP Branch device must always set the MST_CAP bit to 1 on its DPRX, and set the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) of the DPRX of the downstream DP device to 1, as long as the downstream device has the MST_CAP bit set to 1.

For those DP Branch devices converting SST Symbol Mapping to MST Symbol Mapping or MST Symbol Mapping to SST Symbol Mapping, the simple pass-through operation described in Section 2.6.3.3 does not apply.

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2.6.10.1 Last Branch Device

The last Branch device receiving MST-mapped symbols and driving an SST-only mode DPRX should first regenerate the receiving stream, and then map the regenerated stream into SST-mapped symbols including Mvid/Nvid, Maud/Naud, and ECC parity generation. Because the reference clock of the last Branch device and that of the DP Source device sourcing streams are asynchronous with each other, Asynchronous Clocking mode must be used for Mvid/Nvid and Maud/Naud. That is, the Nvid and Naud values must be set to 8000h. The last Branch device is required to generate Mvid and Maud with ±0.1% accuracy.

DP Sink device receiving streams from the last Branch device must use Mvid and Maud as hints for stream clock regeneration, as is the case with stream clock regeneration with link rate down-spreading enabled in SST mode.

Note: *Intermediate DP Branch devices pass through the Stream Symbols Sequence without parsing the contents. Therefore, those intermediate DP Branch devices pass through Mvid/Nvid, Maud/Naud, and SDP ECC parity as is.*

There may be ways to simplify the conversion from MST symbol mapping to SST symbol mapping, but it is an implementation-specific choice and is beyond the scope of this Standard.

2.6.10.1.1 Enablement of Enhanced Framing Symbol Sequence by the Last Branch Device

The last Branch device driving the downstream device in SST mode must enable the Enhanced Framing Symbol Sequence as long as the downstream device supports the sequence.

2.6.10.2 First Branch Device

The first Branch device receiving SST-mapped symbols from an SST-only mode Source device must forward the stream to the downstream link in SST transport format with the same link configuration as the upstream link.

When an upstream Source device is MST-capable, but chooses to transmit in SST format, the MST Source device must initiate ALLOCATE_PAYLOAD message transaction to establish the virtual channel to the target Sink device. In this case, the first Branch device converts incoming SST-mapped symbols into MST-mapped symbols including Mvid/Nvid, Maud/Naud, and ECC parity generation. Since the reference clock of the last Branch device and that of the DP Source device sourcing streams are asynchronous with each other, Asynchronous Clocking Mode must be used for Mvid/Nvid and Maud/Naud.

There may be ways to simplify this conversion, but it is an implementation-specific choice and beyond the scope of this Standard.

2.6.10.2.1 Enhanced Framing Symbol Sequence support by the First Branch Device

The first Branch device must support the Enhanced Framing Symbol Sequence in SST mode.

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2.6.10.3 Mode Switching between MST Mode and SST Mode

The DPTX and DPRX capable of MST mode must support SST mode to interoperate with SST-only mode DP devices.

Switching between MST mode and SST mode results in interruption of the transport of stream(s), because the DPTX must stop the stream transport prior to this mode switch. There are two options:

- The DPTX re-initiates Link Training, and come out of the Link Training with Idle Pattern in SST mode or no-VC Payload (i.e., empty MTP) pattern in MST mode.
- The DPTX stops the transport of streams (resulting in IDLE PATTERN in SST mode, or no VC Payload (empty MTP) pattern in MST mode), sets/clears the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) using a Native AUX write, depending on the direction of the mode switch, and switches the Main-Link pattern at BS (for SST-to-MST mode switch) or at SR (for MST-to-SST mode switch). Starting of a stream transport or a VC Payload allocation must wait at least four BS intervals (after switching to SST mode) or four SR intervals (after switching to MST mode).

2.6.11 MTPH Usages for CP Extension in MST Mode

Two additional usages of MTPH time slots are defined for the CP Extension in MST mode – Encryption Control Field and Link Verification Pattern (LVP).

2.6.11.1 Encryption Control Field

The Encryption Control Field (ECF) consists of an 8-data symbol sequence spanning eight consecutive MTPHs. The data symbol sequence is identical per-lane, regardless of lane count. The ECF is repeated four consecutive times, resulting in a total sequence length of 32 MTPs. The DPRX is required to apply majority voting on the repeated ECFs for error correction.

How the ECF is used is specific to Content Protection system ported onto MST DP link and is therefore beyond the scope of this Standard.

The DPTX must transmit four consecutive ECFs at least once per Link Frame, starting exactly 36 MTPHs prior to the Link Frame boundary SR signal. The ECF may be transmitted by DPTX anywhere outside the keep-out area. When it is sent outside the fixed location starting from the 36 MTPH time slots prior to SR, the ECF must be immediately followed by an ACT sequence.

Besides this fixed location, the DPTX may send four consecutive ECFs anywhere immediately prior to the ACT sequence that spans four consecutive MTPH time slots.

Neither the four consecutive ECFs nor the ACT sequence must straddle the SR and Link Verification Pattern (described in Section 2.6.11.2).

The DPRX must monitor both the fixed four consecutive ECFs' location and 32 MTPH time slots prior to ACT sequence and take proper encryption action.

The timing relationships of these fields for the link frame boundary case are shown in Figure 2-106.

The timing relationship of four consecutive ECFs and ACT sequence is shown in Figure 2-107. Note that the MTP $N + 4$ in Figure 2-107 may optionally occur at MTP#0 (the link frame boundary), in which case MTPH $N + 5$ and MTPH $N + 6$ will contain the LVP, as shown in Figure 2-106. Also, the MTP $N - 32$ may optionally occur at MTP #3 after the link frame boundary, in which case MTPH N containing the first ACT sequence starts on MTP #36 immediately after the reserved time slots shown in Figure 2-106.

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Figure 2-106: MSTM ECF and LVP Signaling at Link Frame Boundary

Figure 2-107: ECF Immediately Prior to ACT Sequence

2.6.11.2 Link Verification Pattern

The two consecutive MTPH time slots immediately following the Link Frame boundary SR signal are used for transporting the 16-bit Link Verification Pattern (LVP), the least significant byte (bits 7:0) transmitted first and the most significant byte (bits 15:8) last.

In SST mode, the HDCP SYNC DETECT bit in the VB-ID (bit 5) is used to sequentially transport the 16-bit Link Verification Pattern. In MST mode, bit 5 becomes "don't care."

2.6.11.3 Encryption of MTPH Time Slots

The data symbols transported in those MTPH time slots for ECFs must not be encrypted. LVP must be encrypted. Whether to encrypt other MTPH time slots is up to the policy of the content protection system running over MST DP link.

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2.7 Compressed Display Stream Transport Services

DisplayPort may transport a bitstream as per *DSC v1.2*. Support for DSC is optional for DP Source, Branch, and Sink devices. When DSC is enabled, FEC shall be enabled.

DP Display Stream Compression (DSC) maps to a new Stream Compression Layer, logically located below the Stream Layer and above the Transport Layer in the DP Layer Architecture Model, as illustrated in Figure 2-108. The DSC algorithm, described in *DSC v1.2*, is logically separate from the transport services. Note that this logical separation is neither intended to imply nor restrict an implementation.

Figure 2-108: DisplayPort Layer Architecture Model with Compression

2.7.1 Transport Buffer Model

Figure 2-109 illustrates an architectural view of the compression elements and transport buffers. A downstream frame buffer may optionally be included with the compressed data before the Decompressor, or with the reconstructed data after the Decompressor. System designers should refer to *DSC v1.2* for rate buffer size requirements for any combination of pixel stream and the bitstream rate.

Figure 2-109: High-Level Compression Architectural Elements

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2.7.2 Configuration – Discovery, Enabling, and Disabling

A DP device capable of DSC decompression is referred to as a "DP DSC Sink device." A DP DSC Sink device may be either a DP Sink device or a DP Branch device with DSC decompression capability. The device shall declare its decompression capability in the DSC Capability DPCD registers at DPCD Addresses 00060h through 0006Ch. A DSC-capable DP Source device is referred to as a "DP DSC Source device." A DP DSC Source device shall read the DSC Capability DPCD registers at DPCD Addresses 00060h through 0006Ch to confirm whether the Sink device is capable of supporting decompression.

The DSC data structures of a DP DSC Sink device are held in the DSC DPCD register locations from DPCD Addresses 00060h through 0006Ch accessed through native AUX transactions. For MST devices, the DSC data structures are accessed through REMOTE_DPCD_RD message transactions to the virtual DP peer device (see Section 2.6.1.1).

Figure 2-110 illustrates the initial discovery, setup, and enabling of DSC.

A DSC-capable device with a higher *DSC v1.sub-version number* (e.g., version 1.2) shall be able to operate with any other DSC-capable device of the same or lower *DSC v1.sub-version number* (e.g., version 1.2). See the appropriate *DSC v1.x* for more information on interoperability between sub-versions.

Figure 2-110: Initial Discovery, Setup and Enable of DSC Compression

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2.7.2.1 DP DSC Source Device

If a DP DSC Sink device is discovered downstream, a DP DSC Source device may enable compression by setting the Decompression Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) to 1. After the bit is set, the DP DSC Source device shall not clear Decompression Enable bit to 0 while the CompressedStream_Flag bit in the VB-ID (bit 6) is set to 1.

After the DP DSC Source device receives an ACK from its setting of the Decompression Enable bit, the DP DSC Source device shall send the Picture Parameter Set (PPS), as detailed in Section 2.2.5.9. Only after the PPS is sent shall the Source device set the CompressedStream_Flag bit in the VB-ID (bit 6) to indicate whether compression is enabled (flag state of 1) or disabled (flag state of 0), over each individual video frame following the VB-ID. The PPS value shall persist across the CompressedStream_Flag transitions. The PPS is required to be sent, as follows:

- After the Decompression Enable bit is set, and
- If a PPS parameter changes

See *DSC v1.2* for further details.

If compression on a frame is enabled, the DP DSC Source device shall set the CompressedStream_Flag to 1 no later than one scan line prior to where the active region starts. If compression on a frame is disabled, the DP DSC Source device shall clear the CompressedStream_Flag to 0 no later than one scan line prior to where the active region starts. These timing requirements are illustrated in Figure 2-111, which defines these timings relative to events visible to a DPRX.

2.7.2.2 DP DSC Sink Device

After sending an ACK response to the AUX write transaction (DP SST DSC Sink device) or REMOTE_DPCD_WR message transaction (DP MST DSC Sink device) to set the Decompression Enable bit in the DSC ENABLE register (DPCD Address 00160h, bit 0) to 1, the DP DSC Sink device shall be ready to receive and process the PPS followed by the compressed stream, until the Decompression Enable bit is cleared to 0 by the DP DSC Source device.

The DP DSC Sink device shall use any PPS sent from the DP DSC Source device only while the Decompression Enable bit is set. The device shall ignore any PPS received when the Decompression Enable bit is not set.

The DP DSC Sink device shall monitor the CompressedStream_Flag bit in the VB-ID (bit 6), which indicates whether compression is enabled (flag state of 1) or disabled (flag state of 0), over each individual video frame.

The DP DSC Sink device shall ignore this flag state during the active region. These timing requirements are illustrated in Figure 2-111, which defines these timings relative to events visible on the DP link.

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Figure 2-111: Compressed/Uncompressed Stream Indication in VB-ID

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2.7.3 Minimum Slices Per Line Requirement

A DP DSC Sink device shall support, at a minimum, a specific number of slices per Display Line for each of the display's supported display modes defined as a combination of resolution and refresh rate. Table 2-141 lists the required slices per Display Line for a given display mode's pixel throughput rate. If a display is driven by more than one MST stream, the pixel throughput rate is the cumulative pixel throughput rate of all the MST streams used for the display.

Table 2-141: Required Slice Count per Display Line[a]

Display Peak Pixel Rate (ppr) (MP/s)	Slice per Display Line Requirement[b]	Alternative Slice per Display Line Requirement[c]
ppr ≤ 340	1	1
340 < ppr ≤ 680	2	1
680 < ppr ≤ 1360	4	2
1360 < ppr ≤ 3200[d]	8[d]	4
3200 < ppr ≤ 4800	12	8
4800 < ppr ≤ 6400	16	8
6400 < ppr ≤ 8000	20	12
8000 < ppr ≤ 9600	24	12

a. *Table values are subject to different restrictions and/or limits. See the text within this section for rules specific to handling maximum slice width.*
b. *This column has requirements based on a DP DSC Source device at 1 pixel per clock (DP DSC Sink device at 3 pixels per clock) throughput rate. The third ("Alternative") column addresses a DP DSC Source device at 2 pixels per clock (DP DSC Sink device at 6 pixels per clock) only throughput rate modes. See the text within this section for further details.*
c. ***DSC v1.2 (or higher) native 4:2:0 mode only** – This column applies to a display mode that is available only as a 4:2:0 sub-sampled pixel stream when DSC v1.2 (or higher) native 4:2:0 mode is used.*
d. *The ppr values in MP/s units that are greater than 2720 assume a DSC throughput capability of 400MP/s. The ppr values in MP/s units that are less than or equal to 2720 assume a DSC throughput capability of 340MP/s.*

If a display has a display mode (resolution and refresh rate) that meets the requirements listed below, it may support the Alternative Slices/Display Line column of Table 2-141 for that mode for *DSC v1.2* (or higher):

- Display mode is available only with a 4:2:0 sub-sampled pixel stream
- DSC encoder and decoder processes use DSC native 4:2:0 mode coding

If the slice size from the table requires a size greater than MaxSliceWidth (number of pixels per Chunk, as specificed by the DSC Max Slice Width field in the DSC Maximum Slice Width register (DPCD Address 0006Ch, bits 7:0)), the next higher allowed slice count value shall be used in place of the table-supplied value. This adjustment repeats until the slice width is less than or equal to MaxSliceWidth.

For further details and usage examples, see Appendix L.

A DP DSC Source device shall be able to support all slice per line combinations listed in Table 2-141, up to the highest display mode that the Source device supports.

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A DP DSC Source device may set any slice per line count that the DP DSC Sink device supports, as long as the slice width is less than or equal to MaxSliceWidth.

2.7.3.1 Additional Slice per Display Line Options

A DP DSC Sink device may support additional slice per Display Line configurations. All supported slice per Display Line configurations shall be declared in the DSC SLICE CAPABILITIES 1 and Peak DSC Throughput (DSC Sink) registers (DPCD Addresses 00064h and 0006Bh, respectively).

The DP link may carry multiple independent bitstreams. The DSC SLICE CAPABILITIES 1 register set includes a declaration of the number of bitstreams that a DP DSC Sink device can support. System designers should refer to *DSC v1.2* for guidance to ensure that the bitstream is correctly coded or decoded based on the number of slices per Display Line and the number of DSC bitstreams that carry the display data. (See Appendix L for details.)

2.7.3.2 Additional DP DSC Sink DSC Capabilities

If a DP DSC Sink device can support throughputs greater than the default values (340 and 400MP/s in the 3 pixels per clock mode; see Section 2.7.3) or slice widths greater than the default width of 2560 pixels, the device may declare its greater capabilities in the Peak DSC Throughput (DSC Sink) and DSC Maximum Slice Width registers (DPCD Addresses 0006Bh and 0006Ch, respectively). The DP DSC Source device may use this information to identify possible additional supported configurations.

For example, a 4K (3840-pixel-wide) display that uses *CVT v1.2* timings with reduced Blanking 1 mode at a 90Hz refresh rate requires a maximum Peak rate of 811.44MP/s. As per Table 2-141, that requires four slices per Display Line. If the DP DSC Sink device advertises a higher throughput capability of 600MHz in Throughput Mode 0 (Throughput Mode 0 field (bits 3:0) in the Peak DSC Throughput (DSC Sink) register is programmed to 6), the DP DSC Source device has the option of using only two slices per Display Line ((811.44MP/s / 600MP/s) = 1.35; rounded up = 2), assuming it can also support that throughput rate. The DP DSC Source device will also need to check that the slice width of 1920 pixels (3840 pixels / 2 slices) is not overly large. In this case, every device shall be able to support slices of at least 2560 pixels; thus, two slices would be a valid configuration. If the slice width was larger than the 2560 default, the DP DSC Source device could check the DSC Maximum Slice Width register to see whether the DP DSC Sink device's MaxSliceWidth is larger than the default 2560. If that value is larger than the calculated pixel width, the calculated slice width could be used.

2.7.3.3 Framing and Compressed Stream Mapping

This section describes the rules for transporting a compressed stream over the DP Main-Link.

When a Source device enables DSC, the DP DSC Source device shall send a DSC-encoded bitstream, instead of uncompressed raw pixel data, over the link during the active video period. The Source device shall maintain the video frame format. The definition of MSA remains unchanged. Link Bandwidth management is carried out as specified in Section 2.2.1.4.

For Link Bandwidth purposes, the number of bits allocated for each slice is calculated as `ceil(`***bits_per_pixel*** × ***slice_width*** `/ 8)` × ***slice_height***, and the size of each chunk is calculated as `ceil(`***bits_per_pixel*** × ***slice_width*** `/ 8)`.

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The slice height shall be restricted such that the active video height is an integer multiple of this value. Compressed Display Stream data is transported in units of chunks. The Source device shall insert an End of Chunk (EOC) after the transmission of each chunk. EOC shall be inserted in all lanes in the same LS_Clk (DP Main-Link Symbol Clock) cycle. Figure 2-112 illustrates EOC placement.

Figure 2-112: Example of Packing DSC Data Bytes within a Video Frame

The bytes of the DSC bitstream are spread across the enabled lanes, starting with Byte 0 on Lane 0. If the bytes within a chunk are not a multiple of the number of lanes, dummy data is inserted as padding to make it a multiple of the number of lanes. The contents of the dummy data used for padding is TX-implementation specific. Note that normal data, not special k-codes, shall be chosen. The chunk and any required padding is then followed by an EOC. EOC Control Link Symbol to 8b/10b special characters mapping is defined in Table 3-7 (SST format) and Table 2-139 (MST format).

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In both SST and MST formats, the Source device shall send the BS symbol sequence after it has transmitted the last chunk of the scan line and EOC, as required and described in Section 2.2.1.2. Compressed data transmission shall resume immediately after the next BE symbol. In MST format, EOC Control link symbols are inserted four times, regardless of the lane count (i.e., four consecutive time slots in 1-lane configuration, two consecutive time slots across two lanes in 2-lane configuration, and one time slot across four lanes in the 4-lane configuration), as is the uncompressed video stream transport in MST format described in Section 2.6.3.

The DP DSC Sink device shall report an error if the number of bytes received for a chunk does not match the chunk size specified in the PPS by setting the Chunk Length Error bit in the DSC STATUS register (DPCD Address 0020Fh and 02011h, bit 2), and then generating an IRQ_HPD. The Sink device shall then report RC buffer underrun and overflow error(s) by setting the RC Buffer Overflow and RC Buffer Under-run bit in the DSC STATUS register (DPCD Address 0020Fh and 02011h, bits 1:0, respectively), and then generating an IRQ_HPD on the RC buffer underrun or overflow error(s). The Source device handles the error(s) in an implementation-specific manner.

The DSC algorithm restricts artifacts that result from errors in the received bitstream to the slice in which the errors occurred. Standard DP compressed stream transport services do ***not*** provide additional error resiliency features beyond the required FEC to mitigate the potential impact of bit-error-induced artifacts. Care should be taken during DP system design to account for this.

2.8 AUX Transaction Syntax in Manchester Transaction Format

The syntaxes used for various AUX transactions in Manchester transaction format are described in this section. As described in Section 3.4, the Manchester transaction format uses Manchester-II coding at the nominal bit rate of 1Mbps.

The following two categories are explained:

- Native AUX transaction syntax
- Syntax for mapping of an I^2C transaction onto AUX transaction called I^2C-over-AUX transaction

This section describes the DP AUX transaction syntax suitable for a half-duplex, bidirectional AUX CH PHY Layer. The number of bus turnarounds is reduced to minimize the half-duplex overhead.

The AUX CH PHY Layer consists of a single differential pair carrying self-clocking data. All transactions must start with a preamble "SYNC" for synchronizing the Requester (DPTX) and the Replier (DPRX), and must end with a "STOP" condition.

A 4-bit command, COMM3:0, must be transmitted after the preamble, followed by a 20-bit address, ADDR19:0. The DisplayPort capability, status and control functions are directly mapped to the 20-bit address space. In addition, DisplayPort uses these 20 bits to access I^2C devices.

After the transmission of command and address, the data bytes must be transmitted except for Address-only transaction for I^2C-over-AUX transaction. Burst data transfer is supported. The burst data size must be limited to a maximum of 16 bytes.

Bit 3 (msb) of the request command field indicates whether the transaction is a Native AUX transaction or an I^2C-over-AUX transaction.

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Table 2-142: Bit/Byte Size of Various Data Types of AUX Transaction Syntax

Data Type	Bit Width
Command	4 bits
Address	Request transaction – 20 bits.
	Reply transaction – None (0000b must be padded to Command, to form a byte).

Data	Request transaction:
	• For read – 1 byte (Length byte)
	• For write – 1 byte (Length byte) + *N* Data bytes
	  • Length byte ("LEN") defines the number of bytes to be written to or to be read from the AUX Replier (DPRX) by the AUX Requester (DPTX)
	  • *N* = Integer value from 1 to 16 (i.e., a DPTX is required to limit the burst data size to 16 or fewer bytes)

	Reply transaction:
	• For read = *N* Data bytes
	  • *N* = Integer value from 1 to 16, the number of bytes ready to be sent
	• For write = 0 or 1 Data byte
	  • When AUX Replier NACKs the write request transaction, it must indicate how many bytes have been written
	  • For an I^2C write over the AUX CH, the AUX Replier, following the ACK, must indicate how many bytes have been written to the I^2C slave

Note: *In this Standard, "►" is attached to a signal name that is driven by the Requester, while "◄" is attached to a signal driven by the Replier.*

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2.8.1 Command Definition

Request and reply command definitions of AUX transactions are described in this section.

2.8.1.1 Request Command Definition

Table 2-143: Request Command Definition, Bit 3

Bit #	Value	Description

3	0	**I^2C-over-AUX Transaction**
		Functions as an I^2C-over-AUX transaction, and:
		• Bit 2 = MOT (Middle-of-Transaction) bit
		• Bits 1:0 = I2C Command
		  • 00 = Write
		  • 01 = Read
		  • 10 = Write_Status_Update_Request
		  • 11 = RESERVED
		Note: *For further details regarding the MOT bit and I^2C Write Status Request, see Section 2.8.5, and Section 2.8.7. See also see Table 2-145, which provides further detail regarding bits 2:0 when bit 3 is cleared to 0.*

	1	**DisplayPort Transaction**
		Functions as a Native AUX transaction, and:
		• Bits 2:0 = Request type
		  • 000 = Write
		  • 001 = Read

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2.8.1.2 Reply Command Definition

The 4-bit Reply Command field is divided into the Native AUX Reply field (bits 1:0) and I2C-over-AUX Reply field (bits 3:2). The I2C-over-AUX Reply field is valid only when Native AUX Reply field is AUX_ACK (cleared to 00). When the Native AUX Reply field is not 00, then the I2C-over-AUX Reply field must be 00 and ignored.

Table 2-144: Reply Command Definition, Bits 3:0

Bit #	Value	Description
1:0		**Native AUX Reply field**
	00	**AUX_ACK** For write transactions: • All the data bytes have been written. For read transactions: • Ready to reply to Read request with data following. • A DPRX (Replier) may assert a STOP condition before transmitting the total number of requested data bytes when not all the bytes are available.
	01	**AUX NACK** For write transactions: • AUX NACK must be followed by a data byte “M”, where “M” indicates the number of data bytes successfully written. • When a DPTX is writing a DPCD address not supported by the DPRX, the DPRX shall reply with AUX NACK and “M” equal to zero. For read transactions: • A DPRX receiving a Native AUX read request for an unsupported DPCD address must reply with an AUX ACK and read data set equal to zero instead of replying with AUX NACK.
	10	**AUX DEFER** For write and read transactions: • Not ready for the write/read request. A DPTX may retry later.
	11	**RESERVED**

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Table 2-144: Reply Command Definition, Bits 3:0 (Continued)

Bit #	Value	Description
3:2		**I^2C-over-AUX Reply field** A DPRX must not forward an I^2C transaction to an I^2C slave unless the AUX CH has received all the data bytes. When the DPTX fails to receive all the data bytes it either AUX NACKs (with "M" set equal to the number of received data bytes) or AUX DEFERs (not ready to receive the request transaction). The DPTX may either abort the I^2C-over-AUX transaction or retry at a later time. I^2C-over-AUX Reply field is only valid when paired with AUX ACK.
	00	**I2C ACK** For I^2C write transactions: • I2C ACK must be followed by the data byte "M", where "M" is the number of bytes the DPRX has written to its I^2C slave without NACK. The data byte "M" must be omitted when all the data bytes have been written. See Section 2.8.5.2 for examples. For I^2C read transactions: • The I^2C slave has ACKed the I^2C address and the DPRX is ready to reply with data following. • The DPRX may assert a STOP condition before transmitting the total number of requested data bytes when not all the bytes are available.
	01	**I2C NACK** For I^2C write transactions: • I2C NACK must be followed by a data byte "M", except when the I^2C slave has NACKed the I^2C address, in which case the reply transaction shall end with I2C NACK without the data byte "M". Data byte "M" indicates the number of bytes the DPRX has successfully written to its I^2C slave before receiving the NACK. The byte on which the NACK occurred is excluded from the number. For I^2C read transactions: • The I^2C slave has NACKed the I^2C address.
	10	**I2C DEFER** For I^2C write and read transactions: • The I^2C slave has yet to ACK or NACK the I^2C transaction.
	11	**RESERVED**

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2.8.2 AUX Transaction Response/Reply Timeouts

AUX Replier (the DPRX) must start sending the reply back to the AUX requester (the DPTX) within the 300us response period. The Response Timeout timer starts ticking after the DPRX has finished receiving the AUX STOP condition which ends the AUX Request transaction.

The timer is reset either when the Response Timeout period has elapsed or the DPRX has started to send the AUX Sync pattern (which follows 10 to 16 active pre-charge pulses) for the Reply transaction.

If the DPTX does not receive a reply from the DPRX it must wait for a 400us Reply Timeout period before initiating the next AUX Request transaction. The Reply Timeout timer starts ticking after the DPTX finishes sending the AUX STOP condition.

The timer is reset either when the Reply Timeout period elapses or DPTX detects the first 0 in Manchester-II code, which is in active pre-charge pulses and AUX Sync pattern of the Reply transaction.

2.8.3 Native AUX Request Transaction Syntax

SYNC► COMM3:0|ADDR19:16► ADDR15:8► ADDR7:0► LEN7:0► (DATA0_7:0► …) STOP

2.8.3.1 Write Request Transactions

For write transactions (COMM3:0 = 1000), the Request transaction must stop when the number of bytes (1 to 16 = LEN7:0 value + 1, all other values are invalid) has been transmitted from the Requester to the Replier.

2.8.3.2 Read Request Transactions

For read transactions (COMM3:0 = 1001), the Request transaction must stop after LEN7:0 (i.e., no data must be transmitted). The Requester expects the Replier to reply with [LEN7:0 value + 1] bytes (= 1 to 16 bytes) of data.

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2.8.4 Native AUX Reply Transaction Syntax

SYNC◄ COMM3:0|0000◄ (DATA0_7:0◄ …) STOP

2.8.4.1 Reply Transaction to Write Request

A reply transaction to a write request must end in one of the following three conditions:

- The Replier has received a write request, and has completed the write. The Replier must reply to the transaction by sending an AUX ACK.
  - SYNC◄ 00|AUX ACK|0000◄ STOP◄
- The Replier has received a write request, but has not completed the write. The Replier must end the transaction by sending AUX NACK as the first COMM3:0, and then, the number of written bytes M as DATA0_7:0.
  - SYNC◄ 00| NACK|0000◄ DATA0_7:0◄ STOP◄

  Where DATA0_7:0 shows the number of written bytes, M.
- Replier has received a write request, but is not ready to accept the write request. Replier must reply with AUX_DEFER.
  - SYNC◄ 00|AUX_DEFER|0000◄ STOP◄

2.8.4.2 Reply Transaction to a Read Request

A reply transaction to a Read request must end in one of the following four conditions:

- Replier has received a read request, but is not ready to reply with the read data. Must end the transaction by sending AUX DEFER as the first COMM3:0.
  - SYNC◄ 00|AUX DEFER|0000◄ STOP◄
- Replier has received a read request and is ready. Must reply by sending AUX ACK as the first command, transmit back the number of requested bytes, assert the STOP condition, and release the AUX CH.
  - SYNC◄ 00|AUX ACK|0000◄ STOP◄
- Replier has received a read request and is ready with some (M + 1 bytes) but not all, of requested data bytes. Must reply by sending AUX ACK as the first command**,** transmit back the number of bytes that can be replied**,** assert the STOP condition, and release the AUX CH.
  - SYNC◄ 00|AUX ACK|0000◄ DATA0_7:0◄ …DATAM_7:0◄ STOP◄
- Replier has received a read request for *N* bytes and is ready. Must reply with AUX ACK as the first command, transmit back the number of requested bytes, assert STOP condition, and then release the AUX CH.
  - SYNC◄ 00|AUX ACK|0000◄ DATA0_7:0◄ …DATAN-1_7:0◄ STOP◄

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2.8.5 I^2C Bus Transaction Mapping onto AUX Syntax

The mapping of an I^2C transaction onto the I^2C-over-AUX transactions as defined in this Standard is agnostic to the application-specific usage of the I^2C data bytes. Neither the DPTX nor DPRX must be aware of how each of the data bytes in the I^2C transaction is used for a specific I^2C application.

A single I^2C transaction may be mapped onto one or multiple I^2C-over-AUX transactions to accommodate the bit-rate difference between I^2C and AUX CH. How (or whether) to divide an I^2C transaction into multiple I^2C-over-AUX transactions is DPTX-implementation-specific. For an I^2C-over-AUX transaction, a DPTX may initiate an "Address-only" request transaction in which the DPTX STOPs the AUX transaction after sending the Request command field and 20-bit Address without sending LENGTH byte/data bytes.

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2.8.5.1 I²C-over-AUX Request Transaction Command

When bit 3 (msb) of the Request command is cleared to 0 (see Table 2-143), the requested transaction must be an I2C-over-AUX Transaction. A single I²C transaction may be divided into multiple I²C-over-AUX transactions, each with bit 3 of the Request command set to 0.

In an I²C bus transaction, the remaining three bits, 2:0, of the Request command are defined as listed in Table 2-145.

Table 2-145: Request Command Definition, Bits 2:0, When Bit 3=0

Bit #	Value	Description
1:0		**I²C Command**
	00	**Write**
	01	**Read**
	10	**Write_Status_Update_Request** When the last I²C write transaction resulted in a reply of either I2C_DEFER or ACK followed by a data byte "M", where "M" is the number of bytes written to the I²C slave, AUX Requester (DPTX) may issue the following special request to inquire the status of the last I²C write: SYNC► COM3:0 (= 0110)|0000► 0000|0000► 0|7-bit I²C address (the same as the last)► 0000|0000 (Length byte)► STOP► To this request, AUX Replier (DPRX) must reply with the latest status.
	11	**RESERVED**
2	1	**MOT (Middle-of-Transaction) bit** This bit must be set when the I²C transaction does not end (or STOP) with the current AUX transaction. The I²C master in the DPRX must send the 7-bit I²C address and read or write command only when: • This bit is set to 1 for the first time (i.e., in the first AUX transaction for the START of an I²C transaction), –or– • RepeatedStart is issued, which results in either a new I²C address or the same I²C address but with the read/write command opposite of the previous command.

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2.8.5.2 I²C Write Transaction

In this section, mapping of an I²C Write transaction onto the AUX transaction(s) is described using an example in which three data bytes are written. An I²C master in the Source device will initiate an I²C Write transaction to an I²C slave in a Sink device via the AUX CH between DPTX in the Source device and DPRX in the Sink device as shown in Figure 2-113. Three variants of the operation are shown, demonstrating a variety of ways to accomplish the goal of performing an I²C Write transaction.

In the following descriptions, the I²C slave in the Sink device acknowledges the I²C Write. When the I²C slave non-acknowledges the I²C write (either I²C address is not supported or the write data byte is not accepted), what corrective action to take is up to the I²C master in the Source device and beyond the scope of this Standard.

Figure 2-113: Examples of AUX CH Bridging Two I²C Buses

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I^{2}C Write Example 1:

START► 1001000|0► ACK◄ Data0► ACK◄ Data1► ACK◄ Data2► ACK◄ STOP►

- I^{2}C Write Mapping Method 1

  The I^{2}C address byte transfer and each data byte write are mapped into separate AUX transactions. In the example shown in Table 2-146, the bit rate of the I^{2}C bus in the Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I^{2}C slave in the Sink device can acknowledge each byte within the 300us of the Response Timeout period.

Table 2-146: I^{2}C Write Transaction Example 1

#	I^{2}C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^{2}C Transaction in the Sink Device
1	START► 1001000|0► (I^{2}C Write with I^{2}C address = 1001000; I^{2}C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I^{2}C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
5	ACK◄ Data0► (I^{2}C clock stretched by DPTX before ACK to Data0)			
6		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data0► STOP► (MOT = 1, the same I^{2}C address, Length = 1 byte)		
7			Wait up to 300us	Data0► ACK◄
8			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	

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Table 2-146: I²C Write Transaction Example 1 (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
9	ACK◄ Data1► (I²C clock stretched by DPTX before ACK to Data1)			
10		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data1► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
11			Wait up to 300us	Data1► ACK◄
12			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
13	ACK◄ Data2► (I²C clock stretched by DPTX before ACK to Data2)			
14		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data2► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
15			Wait up to 300us	Data2► ACK◄
16			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
17	ACK◄ STOP►			
18		SYNC► 0000|0000► 00000000► 0|1001000► STOP► (Address-only transaction with MOT = 0 and the same I²C address, indicating I²C STOP to DPRX)		
19			Wait up to 300us	STOP►
20			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	

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- I^2C Write mapping Method 1 with a slower I^2C bus in the Sink device:

  In the version shown in Table 2-147, the bit rate of the I^2C bus in the Sink device is set to 25kHz (=40us per bit). At this bit rate, the I^2C slave in the Sink device cannot acknowledge even a single byte within the 300us of the Response Timeout period. The DP TX must issue an I^2C Status Update Request to work with such a slow I^2C bus in the Sink device.

Table 2-147: I^2C Write Transaction Method 1 with a Slow I^2C Bus in the Sink Device

#	I^2C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in the Sink Device
1	START► 1001000|0► (I^2C Write with I^2C address = 1001000; I^2C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I^2C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► (DPRX does not get ACK to I^2C address before Reply Timeout expires)
4			SYNC◄ 1000|0000◄ STOP◄ (I2C DEFER/AUX ACK)	
5		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I^2C address)		
6			Wait up to 300us	ACK◄ (DPRX gets ACK to I^2C address)
7			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
8	ACK◄ Data0► (I^2C clock stretched by DPTX before ACK to Data0)			

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Table 2-147: I²C Write Transaction Method 1 with a Slow I²C Bus in the Sink Device (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
9		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
10			Wait up to 300us	Data0► (DPRX does not get ACK for Data 0 write before Reply Timeout expires)
11			SYNC◄ 1000|0000◄ STOP◄ (I2C DEFER/AUX ACK)	
12		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I²C address)		
13			Wait up to 300us	ACK◄ (DPRX gets ACK to Data0 write)
14			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
15	ACK◄ Data1► (I²C clock stretched by DPTX before ACK to Data1)			
16		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data1► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
17			Wait up to 300us	Data1► (DPRX does not get ACK for Data1 write before Reply Timeout expires)
18			SYNC◄ 1000|0000◄ STOP◄ (I2C DEFER/AUX ACK)	

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Table 2-147: I²C Write Transaction Method 1 with a Slow I²C Bus in the Sink Device (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
19		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I²C address)		
20			Wait up to 300us	ACK◄ (DPRX gets ACK to Data1 write)
21			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
22	ACK◄ Data2► (I²C clock stretched by DPTX before ACK to Data2)			
23		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data2► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
24			Wait up to 300us	Data2► (DPRX does not get ACK for Data2 write before Reply Timeout expires)
25			SYNC◄ 1000|0000◄ STOP◄ (I2C DEFER/AUX ACK)	
26		SYNC► 0110|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 1 and the same I²C address)		
27			Wait up to 300us	ACK◄ (DPRX gets ACK to Data2 write)
28			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
29	ACK◄ STOP►			

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Table 2-147: I²C Write Transaction Method 1 with a Slow I²C Bus in the Sink Device (Continued)

#	I²C Transaction in the Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in the Sink Device
30		SYNC► 0000|0000► 00000000► 0|1001000► STOP► (Address-only transaction with MOT = 0 and the same I²C address, indicating I²C STOP to DPRX)		
31			Wait up to 300us	STOP►
32			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	

- I²C Write Mapping Method 2:

  I²C address byte transfer is mapped into address-only AUX transaction, while the write of multiple data bytes is mapped into a single AUX transaction (as long as the number of bytes is equal to or fewer than 16 bytes, which is the maximum burst data byte size of AUX transaction).

  As a variation of Method 2, DP TX may combine the entire transaction (I²C address transfer and data bytes write) into a single AUX transaction.

  Method 2 is faster than Method 1. However, if the I²C slave in the Sink non-acknowledges the Write Data Byte, the I²C Master in the Source will not know which byte was non-acknowledged.

  In the example shown in Table 2-148, four bytes of data (Data0 to Data 3) are written. The bit rate of the I²C bus in a Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I²C slave in the Sink device can acknowledge up to three bytes within the 300us of Response Timeout period.

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Table 2-148: I²C Write Transaction Method 2

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
1	START► 1001000|0► (I²C Write with I²C address = 1001000; I²C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I²C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
5	ACK◄ Data0► ACK◄ Data1► ACK◄ Data2► ACK◄ Data3► ACK◄ STOP►			
6		SYNC► 0000|0000► 00000000► 0|1001000► 0000|0011► Data0► Data1► Data2► Data3► STOP► (MOT = 0, the same I²C address, Length = 4 bytes, indicating I2C STOP to DPRX after 4 bytes of Write)		
7			Wait up to 300us	Data0► ACK◄ Data1► ACK◄ Data2► ACK◄

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Table 2-148: I²C Write Transaction Method 2 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
8			SYNC◄ 0000|0000◄ 0000|0011◄ STOP◄ (I2C ACK/AUX ACK, three bytes written to I²C slave)	Data3► ACK◄ STOP► (DPRX gets ACK to Data3 write while sending AUX Reply to DPTX)
9		SYNC► 0010|0000► 00000000► 0|1001000► STOP► (Write_Status_Update_Request with MOT = 0 and the same I²C address)		
10			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK, indicating the Requester (DPTX) of the completion of the 4-byte Write to I²C Slave in the Sink device)	

2.8.5.3 I²C Read Transaction

In this section, the mapping of an I²C read transaction onto AUX transaction(s) is described using two examples in which first example 2 bytes and in the second example 10 bytes are read. An I²C master in the Source device will initiate an I²C read transaction to an I²C slave in the Sink device via the AUX CH between DPTX (in the Source device) and DPRX (in the Sink device).

In the examples shown in this section the I²C Slave in the Sink device acknowledges the I²C Read. When the I²C slave non-acknowledges the I²C Read (I²C address not supported), what corrective action to take is up to the I²C Master in the Source device and beyond the scope of this Standard.

Example 1: I²C Read of Two Data Bytes

START► 1001000|1► ACK◄ Data0◄ ACK► Data1◄ NACK► STOP►

- I²C Read Mapping Method 1

  In Method 1, the I²C address byte transfer, and each data byte read are mapped into separate AUX transactions. In the example shown in Table 2-149, the bit rate of the I²C bus in the Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I²C slave in the Sink device can send each byte within the 300us of Response Timeout period.

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Table 2-149: I²C Read Transaction Method 1

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
1	START► 1001000|1► (I²C read with I²C address = 1001000; I²C Clock stretched by DPTX before ACK)			
2		SYNC► 0101|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 1 and I²C address = 100100)		
3			Wait up to 300us	START► 1001000|1► ACK◄
4			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK, I²C address is acknowledged)	
5	ACK◄ (I²C clock stretched by DPTX after ACK)			
6		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
7			Wait up to 300us	Data0◄
8			SYNC◄ 0000|0000◄ Data0◄ STOP◄ (I2C ACK/AUX ACK, sends Data0)	
9	Data0◄ ACK► (I²C clock stretched by DPTX after ACK)			

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Table 2-149: I²C Read Transaction Method 1 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
10		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
11				ACK► Data1◄
12			SYNC◄ 0000|0000◄ Data1◄ STOP◄ (I2C ACK/AUX ACK, sends Data1)	
13	Data1◄ NACK► STOP►			
14		SYNC► 0001|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I2C STOP to DPRX)		
15			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	NACK► STOP►

I²C Read Example 2

START► 1001000|1► ACK◄ Data0◄ ACK► Data1◄ ACK► Data2◄ ACK► Data3◄ ACK► Data4◄ ACK► Data5◄ ACK► Data6◄ ACK► Data7◄ ACK► Data8◄ ACK► Data9◄ NACK► STOP►

- I²C Read Mapping Method 2

  In Method 2, DPTX pre-fetches read data from the I²C slave in the Sink device via the DPRX to speed up the read operation. As is the previous example, the bit rate of the I²C bus in the Sink device is set to 100kHz (= 10us per bit). At this bit rate, the I²C slave in the Sink device can send back up to 3 bytes within the 300us of Response Timeout period.

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Table 2-150: I²C Read Transaction Example 2

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
1	START► 1001000|1► (I²C read with I²C address = 1001000; I²C clock stretched by DPTX before ACK)			
2		SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C read with MOT = 1, I²C address = 100100, and Length = 16 bytes)		
3			Wait up to 300us	START► 1001000|1► ACK◄ (DPRX gets ACK to I²C address and Data0)
4			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK, I²C address is acknowledged, but no data available yet)	
5	ACK◄ (I²C clock stretched by DPTX after ACK)	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data0◄ ACK►
6			Wait up to 300us	Data1◄ ACK► Data2◄ ACK► Data3◄ ACK►
7			SYNC◄ 0000|0000◄ Data0◄ Data1◄ Data2◄ Data3◄ STOP◄ (I2C ACK/AUX ACK, sends Data0 to Data3)	
8	Data0◄ ACK►	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data4◄ ACK►

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Table 2-150: I²C Read Transaction Example 2 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
9	Data1◄ ACK► Data2◄ ACK►		Wait up to 300us	Data5◄ ACK► Data6◄ ACK► Data7◄ ACK►
10	Data3◄ ACK► (I²C clock stretched by DPTX after the last ACK, as needed)		SYNC◄ 0000|0000◄ Data4◄ Data5◄ Data6◄ Data7◄ STOP◄ (I2C ACK/AUX ACK, sends Data4 to Data7)	
11	Data4◄ ACK►	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data8◄ ACK►
12	Data5◄ ACK► Data6◄ ACK►		Wait up to 300us	Data9◄ ACK► Data10◄ ACK► Data11◄ ACK►
13	Data7◄ ACK► (I²C clock stretched by DPTX after the last ACK, as needed)		SYNC◄ 0000|0000◄ Data8◄ Data9◄ Data10◄ Data11◄ STOP◄ (I2C ACK/AUX ACK, sends Data8 to Data11)	
14	Data8◄ ACK►	SYNC► 0101|0000► 00000000► 0|1001000► 0000|1111► STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data12◄ ACK►
15	Data9◄ NACK► STOP►		Wait up to 300us	Data13◄ ACK► Data14◄ ACK► Data15◄ ACK►

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Table 2-150: I²C Read Transaction Example 2 (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
16			SYNC◄ 0000|0000◄ Data12◄ Data13◄ Data14◄ Data15◄ STOP◄ (I2C ACK/AUX ACK, sends Data12 to Data15)	
17		SYNC► 0001|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I2C STOP to DPRX)		Data16◄ ACK►
18			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	Data17◄ NACK► STOP►

It should be noted that the I²C slave does not have a prior knowledge of how many bytes its I²C master wants to read. The I²C slave keeps sending out read data bytes until its master issues an I²C NACK. I²C-over-AUX syntax supports this paradigm. A DPTX which may be an I²C slave to its master (e.g., GPU software driver) will issue I²C-over-AUX read request transaction with LEN cleared to 0 (i.e., requesting one byte) and MOT bit set to 1. When its master NACKs, a DPTX will send address-only read I²C-over-AUX read request with MOT bit cleared to 0.

In some implementations, however, a DPTX may have prior knowledge of exactly how many bytes it wants to read via I²C-over-AUX read transaction(s). This may be the case when a GPU with an integrated DPTX is sending MCCS commands via DDC/CI transport mechanism; the GPU software driver, in this scenario, may *synthesize* I²C-over-AUX transaction, instead of a DPTX *translating* I²C into I²C-over-AUX transaction.

If the number of bytes to be read is known and is equal to or fewer than 16, a DPTX may initiate an I²C-over-AUX read request transaction with LEN set to the number of bytes minus 1 and MOT bit cleared to 0. A DPRX will issue I²C stop condition to its I²C slave after it has read number of bytes equal to LEN + 1. When the DPRX can read only a number of bytes that is fewer than [LEN +1], the DPTX may repeat the same request transaction. Even in this condition, the DPRX will issue I²C stop condition to its I²C slave after it has read the number of bytes equal to LEN + 1.

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If the number of bytes to be read is greater than 16, a DPTX may initiate an I^2C-over-AUX read request transaction with LEN set to 15 (= 16 bytes) and MOT bit set to 1. From the next transaction on, the DPTX will reduce LEN value to the number of read data bytes a DPRX can send out in a single I^2C-over-AUX read reply transaction so that the number of bytes a DPRX reads from its I^2C slave matches that a DPTX receives from a DPRX. When the remaining number of bytes becomes equal to or fewer than 16 bytes, a DPTX may request the exact number of remaining bytes with MOT bit cleared to 0.

2.8.5.4 I^2C Write followed by I^2C Read

When the I^2C write is followed by an I^2C Read via Repeated Start condition as defined in the I^2C Specification, the MOT bit of the Request Command field must stay = 1 while the transaction switches from I^2C write to I^2C read. Upon detecting this condition, the DPRX must generate an I^2C Repeated Start condition and switch from I^2C write to I^2C read.

In this section, the mapping of an I^2C write transaction followed by an I^2C Read transaction onto AUX transactions is described using an example in which one data byte is written to set an address offset within a 256-byte I^2C data block and two data bytes are read.

The I^2C Write Mapping Method 1 and the I^2C Read Mapping Method 1 are used in this example. The DP TX may use other methods as described in the previous sections.

In the following description, the I^2C slave in the Sink device acknowledges the I^2C transaction. When the I^2C slave non-acknowledges it, what corrective action to take is up to the I^2C master in the Source device and beyond the scope of this Standard.

Example of I^2C write followed by I^2C read:

START► 1001000|0► ACK◄ Data0► ACK◄ REPEATED_START►
1001000|1► ACK◄ Data0'◄ ACK► Data1'◄ NACK► STOP►

Table 2-151: I^2C Write followed by an I^2C Read

#	I^2C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I^2C Transaction in Sink Device
1	START► 1001000|0► (I^2C write with I^2C address = 1001000; I^2C clock stretched by DPTX before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I^2C address = 1001000)		
3			Wait up to 300us	START► 1001000|0► ACK◄

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Table 2-151: I²C Write followed by an I²C Read (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
4			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
5	ACK◄ Data0► (I²C clock stretched by DPTX before ACK to Data0)			
6		SYNC► 0100|0000► 00000000► 0|1001000► 0000|0000► Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
7			Wait up to 300us	Data0► ACK◄
8			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	
9	ACK◄ REPEATED_START► 1001000|1► (Switches to I²C read after issuing REPEATED_START condition with the same I²C address. I²C clock stretched by DPTX before ACK to I²C read address)			
10		SYNC► 0101|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 1 and the same I²C address, indicated I²C REPEATED_START condition to DPRX)		
11			Wait up to 300us	REPEATED_START► 1001000|1► ACK◄

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Table 2-151: I²C Write followed by an I²C Read (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
12			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK, I²C address is acknowledged)	
13	ACK◄ (I²C clock stretched by DPTX after ACK)			
14		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
15			Wait up to 300us	Data0'◄
16			SYNC◄ 0000|0000◄ Data0'◄ STOP◄ (I2C ACK/AUX ACK, sends Data0')	
17	Data0'◄ ACK► (I²C clock stretched by DPTX after ACK)			
18		SYNC► 0101|0000► 00000000► 0|1001000► 0000|0000► STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
19				ACK► Data1'◄
20			SYNC◄ 0000|0000◄ Data1'◄ STOP◄ (I2C ACK/AUX ACK, sends Data1')	

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Table 2-151: I²C Write followed by an I²C Read (Continued)

#	I²C Transaction in Source Device	AUX Request Transaction by DPTX	AUX Reply Transaction by DPRX	I²C Transaction in Sink Device
21	Data1'◄ NACK► STOP►			
22		SYNC► 0001|0000► 00000000► 0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DPRX)		
23			SYNC◄ 0000|0000◄ STOP◄ (I2C ACK/AUX ACK)	NACK► STOP►

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2.8.6 Conversion of I^2C Transaction to Native AUX Transaction (Informative)

Conversion of an I^2C transaction into a Native AUX transaction by the DPTX is implementation-specific and beyond the scope of this Standard.

When the mapping of I^2C transaction over the AUX CH, the translation of I^2C to AUX transaction by the DPTX and that of the AUX to the I^2C by the DPRX must agree with each other. Therefore, the translation mechanism is defined in this Standard.

The conversion of an I^2C transaction to a Native AUX transaction by the DPTX is transparent to the DPRX. Whether it is converted from an I^2C transaction or not, the DPRX will receive the same Native AUX transaction. It is for this reason that the conversion of an I^2C transaction into a Native AUX transaction by the DPTX is beyond the scope of this Standard.

It should be noted that a Sink device is to reply to an I^2C-over-AUX request transaction with AUX DEFER when it is not ready to receive an AUX transaction (as is the case with a Native request transaction). When a Source device receives an AUX DEFER reply, it must repeat the same request transaction if it wants to retry it.

2.8.7 I^2C-over-AUX Transaction Clarifications and Implementation Rules

This section provides clarifications to I^2C-over-AUX implementations. The objective is to eliminate interoperability issues that may be caused by varying interpretations of the specification.

A single I^2C transaction may be (or is likely to be) divided into multiple I^2C-over-AUX transactions. This is because the maximum number of data bytes per I^2C-over-AUX transaction is limited to 16 bytes while I^2C specification does not prohibit even the infinite number of burst write/read operations.

A Source device may initiate Native AUX transactions in between I^2C-over-AUX transactions for a given I^2C transaction. However, a Source device must not interleave I^2C-over-AUX transactions for multiple I^2C transactions: It must complete or terminate one I^2C transaction before starting I^2C-over-AUX transactions for another I^2C transaction. It should be noted that each AUX transaction, whether it is a Native transaction or an I^2C-over-AUX transaction, consists of a request transaction initiated by a Source device and a reply transaction by a Sink device. Until it has received a reply transaction for the current request transaction, the Source device must not initiate another request transaction.

The syntax of the I^2C transactions is very much implementation-dependent. The syntax specification does not assume any fixed I^2C transaction syntax in an attempt to make it applicable to any I^2C implementation. The I^2C master of a DPRX in a Sink device will "imitate" the I2C_SCL/I2C_SDA waveforms of those received by the I^2C slave of a DPTX in a Source device (with the exception of the timing of I^2C clock stretching as described in Section 2.8.7.1.6.8 and Section 2.8.7.2.6).

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A DPTX in a Source device acting as an I^2C slave and AUX Requester may not know how many data bytes its I^2C master is intending to write or read in an I^2C transaction. Unless it knows the number of data bytes at the beginning of an I^2C transaction, the DPTX is recommended to generate I^2C-over-AUX transactions with LEN value equal to 0 corresponding to one data byte. This way, the DPTX will not write or read more bytes than intended by its I^2C master.

As far as the bit rate is concerned, the I^2C specification lists certain bit rates (100k-/400k-/3.4M-bits/sec or bps) and the VESA E-DDC Standard (based on I^2C as the PHY Layer) notes the bit rate of 100kbps. In reality, however, the I^2C bit rate is very dependent on implementations and "channel" qualities. Over a long-reach VGA cable, for example, it is common for a DDC master to have to reduce the bit rate down to 1k ~ 10kbps. The AUX CH bit rate, in comparison, is strictly required to be in the range of 1Mbps ±20% per Manchester format AUX transaction specification. The I^2C-over-AUX specification comprehends this inherent difference (and the variation of the difference) of the bit rates between I^2C and AUX CH. The extension of DPCD field for Sink device to declare its I^2C bit rate capability and for Source device to set the I^2C bit rate among those rates supported by the Sink device further adds to the robustness of the I^2C-over-AUX specification for bridging the bit rate gap.

2.8.7.1 Clarifications for a Source Device

This section describes the clarifications for a Source device.

2.8.7.1.1 Downstream I^2C Bit Rate Detection/Configuration

The extension to the DPCD field for a DPRX to declare its I^2C bit rate capability and for a DPTX to set the I^2C bit rate among those rates supported by the DPRX should be referenced. Alternatively, a DPTX and DPRX may set the I^2C bit rate in a vendor-specific manner.

At a low bit rate, the I^2C slave interfacing with the I^2C master within the DPRX takes a long time to accept/send bytes. At 1kbps, for example, the transport of 1 byte including ACK/NACK takes about 10ms. Therefore, the DPTX must extend the interval of successive I^2C-over-AUX transactions in case the downstream I^2C bit rate is low.

When an MST Source device is accessing the I^2C slave of a DP device connected to via multiple MST Branch devices, the MST Source device must get the I^2C bit rate of the DP device with the I^2C slave and set the desired bit rate by originating REMOTE_I2C_READ and REMOTE_I2C_WRITE message transactions to the last MST Branch device driving the DP device. After setting the I^2C bit rate, the MST Source device originates a REMOTE_I2C message transaction to the last MST Branch device that generates the corresponding I^2C-over-AUX transactions.

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2.8.7.1.2 Prompting the Termination of I^2C Transaction

An address-only I^2C-over-AUX (either write or read) with MOT bit cleared to 0 prompts the Sink device to issue I2C STOP condition to its I^2C slave any time, even before the current I^2C transaction is completed.

An address-only I^2C-over-AUX with MOT bit cleared to 0 must not be issued when there is no ongoing I^2C-over-AUX transaction. If a Source device wants to initiate an I^2C transaction to a certain I^2C Device Address and then terminate it, the following I^2C-over-AUX transactions must be used:

- Address-only transaction with MOT set to 1
- Address-only transaction with MOT cleared to 0

2.8.7.1.3 MOT Bit

The MOT bit cleared to 0 prompts the Sink device to issue I2C STOP condition to its I^2C slave after completing the current I^2C-over-AUX transaction. As noted above, a Source device may issue an address-only I^2C-over-AUX (either write or read) with MOT bit cleared to 0 any time to terminate the current I^2C transaction even before its completion.

2.8.7.1.4 Prompting Repeated I^2C Start Condition

A Source device may issue I^2C-over-AUX with MOT set to 1, then issue another I^2C-over-AUX to the same I^2C Device Address, but a different command (i.e., write followed by read or read followed by write). This action by the Source device prompts the Sink device to initiate the second I^2C transaction following Repeated I^2C Start, instead of I2C STOP.

A Source device may also issue I^2C-over-AUX with MOT set to 1, then issue another I^2C-over-AUX to a different I^2C Device Address either with the same command or a different command. This action also prompts the Sink device to initiate the second I^2C transaction following Repeated Start condition, instead of I2C STOP condition.

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2.8.7.1.5 I^{2}C-write-over-AUX

A Source device may start I^{2}C-write-over-AUX request transaction either with:

- An address-only I^{2}C-write-over-AUX with MOT bit set to 1, or
- Address + LEN + Data bytes I^{2}C-write-over-AUX with MOT bit cleared to 0 or set to 1

The remainder of this section describes the permissible I^{2}C-over-AUX transactions following various replies from the Sink device. The Source device may issue a Native AUX transaction in between I^{2}C-over-AUX transactions even before a given I^{2}C transaction is completed/terminated.

2.8.7.1.5.1 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by no "M" Value to a Request Transaction with MOT Bit Cleared to 0

The I^{2}C transaction is completed. The Source device may initiate another AUX transaction, whether it is Native AUX transaction or I^{2}C-over-AUX transaction to either the same or different I^{2}C Device Address.

2.8.7.1.5.2 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by No "M" Value to a Request Transaction with MOT Bit Set to 1

The Source device must issue one of the following two I^{2}C-over-AUX transactions:

- Proceed with the next I^{2}C-over-AUX transaction either with the same or different I^{2}C Device Address. The transaction may be either an I^{2}C-write-over-AUX or I^{2}C-read-over-AUX.
  - If the ensuing I^{2}C-over-AUX request transaction is either read or to a different I^{2}C Device Address, the I^{2}C master within the DPRX must issue a REPEATED START condition to its I^{2}C Device Address.
- Issue an address-only I^{2}C-over-AUX with MOT bit cleared to 0 to prompt I2C STOP to terminate the current I^{2}C-write-over-AUX transaction.

2.8.7.1.5.3 Upon I2C_DEFER|AUX_ACK Reply, with MOT Bit in Request Transaction Cleared to 0 or Set to 1

The Source device must either:

- Issue an I2C_WRITE_STATUS_UPDATE command, or
- Issue an address-only I^{2}C-over-AUX with MOT bit cleared to 0 to prompt I2C STOP to terminate the current I^{2}C-write-over-AUX transaction. See Section 2.8.7.1.5.6 for an example of how to abort an I^{2}C-over-AUX transfer given repeated AUX_DEFERs. This is similar to receiving an unexpectedly high number of repeated I2C_DEFER responses.

2.8.7.1.5.4 Upon the Reply of I2C_ACK|AUX_ACK followed by "M" Value to the I^{2}C-write-over-AUX, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device must either:

- Issue I2C_WRITE_STATUS_UPDATE command, or
- Issue an address-only I^{2}C-over-AUX with MOT bit cleared to 0 to prompt I2C STOP to terminate the current I^{2}C-write-over-AUX transaction.

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2.8.7.1.5.5 Upon Receiving I2C_NACK|AUX_ACK Reply followed by Either "M" Value or no "M" Value, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

After stopping the current I^2C transaction by issuing Address-only I^2C-over-AUX transaction with MOT cleared to 0, the Source device may start another AUX transaction. As one of the possible transactions, it may attempt the I^2C-write-over-AUX transaction to the same I^2C Device Address to make sure that the Sink device consistently I2C_NACKs.

2.8.7.1.5.6 Upon Receiving AUX_DEFER Reply to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device must either:

- Repeat the identical I^2C-write-over-AUX transaction keeping the same LEN value and Data bytes, or
- Issue an address-only I^2C-over-AUX with MOT bit equal to 0 to prompt I2C STOP to terminate the current I^2C-write-over-AUX transaction. See Section 2.8.7.1.5.6.1 for more information. Prior to aborting the transfer the Source must retry the transaction several times before assuming an error condition is present which justifies the abort.

2.8.7.1.5.6.1 Source Retry Attempts following AUX_DEFER Response prior to Aborting Transfer

A DP Source device is required to retry at least seven times upon receiving AUX_DEFER before giving up the AUX transaction.

If the DP Source device has a way of knowing the I^2C bit rate capability options of the downstream device and of setting the rate, either through vendor-specific method or through the I2C Speed Control Capabilities Bit Map and I2C Speed Control/Status Bit Map registers (DPCD Addresses 0000Ch and 00109h) for those downstream devices with DPCD Rev. 1.2 or higher, it is recommended to adjust the retry interval and/or number of request data bytes based on the I^2C bit rate.

It is also recommended that a Source take into account the various possible implementations from Sink devices of the I^2C-over-AUX burst write transaction. For example, a Sink device may issue AUX_DEFERs until all data in a write burst has been written to the I^2C Slave. Then it may respond with a single I^2C ACK. At various I^2C Bus Speeds and burst sizes, this results in a wide array of retry limits. For example, Table 2-152 lists various I^2C bus speeds and various burst sizes. Assuming Sink implementation which issues AUX_DEFERs until all data is written, we come up with a worst case retry limit. **This example is for reference purposes only**; it does not take into account many factors that affect overall response time. It does not take into account I^2C Slave clock stretching, DP Source retry interval (assumes Source repeats request immediately following DP Sink AUX DEFER response), or varying DP Sink response times (assumes 300us AUX Response timeout immediately followed by Sink device's AUX Defer response).

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The calculations are based on the following assumptions:

- AUX request cycle consists of an I^2C-over-AUX Request + 300us AUX Response Timeout + AUX Response. The AUX Request is 66 AUX Channel Bit times (precharge + Sync + Stop + CMD + Add + LEN) + 8 * BurstSize AUX Channel Bit times.
- An example timeline for the transfers is as follows:

```
--------I2C Cycle -----------------------
AUX    Resp      AUX     AUX   Resp       AUX   AUX   Resp       AUX
Req    TimeOut   Resp      Req   TimeOut  Resp    Req   TimeOut   Resp
     |--------------| |--------------|
          K              K
```

- # of retries * K + 300us = I^2C Cycle length,
  where K = Response Timeout + AUX Response + AUX Request
- # of retries = (I^2C Cycle length - 300us) / (Request Timeout + AUX Response + AUX Request)

Table 2-152: Burst Write Sizes/Bus Speed

I^2C Bus Speed (kbps)	Burst Write Sizes						
	1	**2**	**4**	**6**	**8**	**12**	**16**
1	43	63	102	138	171	232	285
5	8	13	20	27	34	46	57
10	4	6	10	14	17	23	28
100	0	0	1	1	2	2	3
400	0	0	0	0	0	0	1
1000	0	0	0	0	0	0	0

If the Source device has no way of knowing the downstream I^2C bit rate, the Source device may either retry for the period specified for the worst-case bit rate (in the order of 1kbps) or request just 1 byte to "gauge" the effective downstream I^2C bit rate. Such precaution is especially recommended when the downstream device is a DP-to-Legacy converter Branch device, where a long "legacy" cable may force a very low I^2C bit rate.

The Source device must properly terminate the pending I^2C-over-AUX transaction before starting I^2C-over-AUX for another I^2C transaction. The recommended way to abort the transfer (after the recommended number of retries has been attempted) is to first issue an address-only I^2C-over-AUX with MOT bit equal to 0 to prompt I^2C STOP to terminate the current transaction. If the response to this is an AUX_DEFER, then the source may abort the transaction.

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2.8.7.1.5.7 Upon Receiving AUX_NACK Reply followed by Either "M" Value or no "M" Value

The Source device may initiate another AUX transaction. (A Sink device must not reply with AUX_NACK to I^2C-write-over-AUX transaction unless there is a mismatch between the LEN + 1 value and the number of received data bytes.)

2.8.7.1.5.8 No Reply

The Source device may initiate another AUX transaction. (A Sink device must reply unless it either has detected an illegal command or is in a power-save mode due to the write of 02h value to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, via a Native AUX transaction.)

2.8.7.1.6 I^2C-read-over-AUX

A Source device may start I^2C-read-over-AUX request transaction either with:

- An address-only I^2C-read-over-AUX with MOT set to 1, or
- An "Address + LEN" I^2C-read-over-AUX with MOT set to either 0 or 1

The remainder of this section describes the permissible I^2C-over-AUX transactions following various replies from the Sink device. The Source device may issue a Native AUX transaction in between I^2C-over-AUX transactions even before a given I^2C transaction is completed/terminated.

2.8.7.1.6.1 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by the "Total" Number of Data Bytes Equal to LEN + 1, to a Request Transaction with MOT Bit Cleared to 0

The I^2C transaction is completed. The Source device may initiate another AUX transaction, whether it is a Native AUX transaction, I^2C-over-AUX transaction to either the same or different I^2C Device Address.

2.8.7.1.6.2 Upon Receiving the Reply of I2C_ACK|AUX_ACK followed by the "Total" Number of Data Bytes Equal to LEN + 1 to a Request Transaction with MOT Bit Set to 1

The Source device must issue one of the following two I^2C-over-AUX transactions:

- Proceed with the next I^2C-over-AUX transaction either with the same or different I^2C Device Address. The transaction may be either I^2C-write-over-AUX or I^2C-read-over-AUX.
  - If the ensuing I^2C-over-AUX request transaction is either a write to any address or a read to a different I^2C Device Address, the I^2C master within the DPRX must issue a REPEATED START condition to its I^2C Device Address.
- Issue an address-only I^2C-over-AUX with MOT bit cleared to 0 to prompt I2C STOP to terminate the current I^2C-read-over-AUX transaction.

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2.8.7.1.6.3 Upon I2C_DEFER|AUX_ACK Reply, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device must either:

- Repeat the identical I^2C-read-over-AUX transaction keeping the same LEN value, or
- Issue an address-only I^2C-over-AUX with MOT bit cleared to 0 to prompt I2C STOP to terminate the current I^2C-read-over-AUX transaction. See Section 2.8.7.1.6.6 for an example of how to abort an I^2C-over-AUX transfer given repeated AUX_DEFERs. This is similar to receiving an unexpectedly high number of repeated I2C_DEFER responses.

2.8.7.1.6.4 Upon the Reply of I2C_ACK|AUX_ACK followed by the Total Number of Data Bytes Fewer than LEN + 1, to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device must:

- Repeat the identical I^2C-read-over-AUX transaction with the updated LEN value equal to the original LEN value minus the total number of data bytes received so far,
- Repeat the identical I^2C-read-over-AUX transaction with the same LEN value as the original value, or,
- Issue an address-only I^2C-over-AUX with MOT bit cleared to 0 to prompt I2C STOP to terminate the current I^2C-read-over-AUX transaction.

It should be noted that when the Source device repeats the same I^2C-read-over-AUX transaction with the same LEN value as the original value, the Sink device is likely to read more data bytes than the Source device needs.

2.8.7.1.6.5 Upon Receiving I2C_NACK|AUX_ACK Reply to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

For I^2C read operation, I^2C slave only asserts either ACK or NACK to the Device Address. For read data byte transfer from the slave to the master, it is the I^2C master that asserts either ACK or NACK. Because of this fact, I2C_NACK|AUX_ACK reply to the I^2C-read-over-AUX request transaction means that the I^2C slave in the Sink device has asserted NACK to the specified I^2C Device Address.

The Source device has the following options:

- Attempt an I^2C-write-over-AUX to the same I^2C Device Address to check whether the Sink device consistently I2C_NACKs to that I^2C Device Address
- Address-only I^2C-over-AUX with MOT = 0, to prompt the Sink device to terminate the current I^2C transaction
- Initiates an I^2C-over-AUX to a different I^2C Device Address, prompting the Sink device to issue a Repeated I^2C Start

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2.8.7.1.6.6 Upon Receiving AUX_DEFER Reply to a Request Transaction with MOT Bit Cleared to 0 or Set to 1

The Source device must either:

- Repeat the identical I^2C-read-over-AUX transaction keeping the same LEN value, or,
- Issue Address-only I^2C-over-AUX with MOT bit cleared to 0 to prompt I^2C STOP to terminate the current I^2C-read-over-AUX transaction. See Section 2.8.7.1.6.6.1 for more information. Prior to aborting the transfer, the Source must retry the transaction several times before assuming an error condition is present which justifies the abort.

2.8.7.1.6.6.1 Source Retry Attempts following AUX_DEFER Response prior to Aborting Transfer

A DP Source device is required to retry at least seven times upon receiving AUX_DEFER before giving up the AUX transaction.

If the DP Source device has a way of knowing the I^2C bit rate capability options of the downstream device and of setting the rate, either through vendor-specific method or through the I2C Speed Control Capabilities Bit Map and I2C Speed Control/Status Bit Map registers (DPCD Addresses 0000Ch and 00109h) for those downstream devices with DPCD Rev. 1.2 or higher, it is recommended to adjust the retry interval and/or number of request data bytes based on the I^2C bit rate.

It is also recommended that a Source take into account the various possible implementations from Sink devices of the I^2C-over-AUX burst read transaction. For example, a Sink device may issue AUX_DEFERs until all data in a read burst is ready. Then it may respond with all data words. At various I^2C Bus Speeds and burst sizes, this results in a wide array of retry limits. For example, Table 2-153 lists various I^2C bus speeds and various burst read sizes. Assuming a Sink device implementation which issues AUX_DEFERs until all read data is available, we come up with a worst case retry limit. **This example is for reference purposes only**; it does not take into account many factors which affect overall response time. It does not take into account I^2C Slave clock stretching, DP Source retry interval (it assumes Source repeats request immediately following DP Sink AUX_DEFER response), or varying DP Sink response times (it assumes 300us AUX Response timeout immediately followed by Sink's AUX_DEFER response).

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The calculations are based on the following assumptions:

- AUX request cycle consists of an I^2C-over-AUX Request (66 AUX Channel Bit times = precharge + Sync + Stop + CMD + Add + LEN) + 300us AUX Response timeout + AUX Response
- An example timeline for the transfers is as follows:

```
--------I2C Cycle -----------------------
AUX    Resp     AUX   AUX   Resp      AUX   AUX  Resp      AUX
Req    TimeOut Resp   Req    TimeOut Resp    Req   TimeOut Resp
     |--------------| |--------------|
          K              K
```

- # of retries * K + 300us = I^2C Cycle length,
  where K = Response Timeout + AUX Response + AUX Request
- # of retries = (I^2C Cycle length - 300us) / (Request Timeout + AUX Response + AUX Request)

Table 2-153: Burst Read Sizes/Bus Speed

I^2C Bus Speed (kbps)	Burst Read Sizes						
	1	**2**	**4**	**6**	**8**	**12**	**16**
1	44	66	110	154	198	287	375
5	9	13	22	31	39	57	75
10	4	6	11	15	20	28	37
100	0	0	1	1	2	3	4
400	0	0	0	0	0	0	1
1000	0	0	0	0	0	0	0

If the Source device has no way of knowing the downstream I^2C bit rate, Source device may either retry for the period specified for the worst-case bit rate (in the order of 1kbps) or request just 1 byte to "gauge" the effective downstream I^2C bit rate. Such precaution is especially recommended when the downstream device is a DP-to-Legacy converter Branch device, where a long "legacy" cable may force a very low I^2C bit rate.

The Source device must properly terminate the pending I^2C-over-AUX transaction before starting I^2C-over-AUX for another I^2C transaction. The recommended way to abort the transfer (after the recommended number of retries has been attempted) is to first issue an address-only I^2C-over-AUX with MOT bit equal to 0 to prompt I^2C STOP to terminate the current transaction. If the response to this is an AUX_DEFER, then the source may abort the transaction.

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2.8.7.1.6.7 No Reply

The Source device may initiate another AUX transaction. (A Sink device must reply unless it either has detected an illegal command or is in a power-save mode due to the write of 02h value to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, via a Native AUX transaction.)

2.8.7.1.6.8 Clock Stretching

For an address-only I^2C-over-AUX with MOT bit set to 1 and data byte transfer portion of I^2C-write-over-AUX transaction, the I^2C slave within a DPTX does not know in advance whether the DPRX will reply with I2C_ACK or I2C_NACK. Therefore, it must stretch the I^2C clock after the eighth pulse (i.e., the last data bit), instead of after the ninth pulse (i.e., I^2C ACK/NACK).

For data byte transfer portion of an I^2C-read-over-AUX transaction, the I^2C slave within a DPTX must stretch the I^2C clock after the ninth pulse (i.e., I^2C ACK/NACK) to monitor whether its I^2C master will assert I^2C ACK or NACK to the data byte.

2.8.7.2 Clarifications for a Sink Device

This section describes the clarifications for a Sink device.

2.8.7.2.1 I^2C Bit Rate Capability Declaration and Setting

A device with DPRX such as a Sink device declares its I^2C it rate capability at the I2C Speed Control Capabilities Bit Map register (DPCD Address 0000Ch). A device with a DPTX such as a Source device sets the I^2C bit rate by writing to the I2C Speed Control/Status Bit Map register (DPCD Address 00109h). Alternatively, DPTX and DPRX may set the I^2C bit rate in a vendor-specific manner.

2.8.7.2.2 Termination/Completion of I^2C Transaction

Upon receiving an address-only I^2C-over-AUX request transaction with MOT bit cleared to 0 from a Source device, the Sink device must issue I2C STOP condition to its I^2C slave promptly, even before the current I^2C transaction is completed.

Upon receiving an address + LEN + Data bytes (for write, no Data bytes for read) I^2C-over-AUX request transaction with MOT cleared to 0 from a Source device, the Sink device must issue I2C STOP condition upon completion of the current I^2C-over-AUX transaction (i.e., when all the address and/or data bytes have been ACKed by its I^2C slave).

When a Source device initiates a new I^2C transaction without properly completing/terminating the current I^2C transaction (which a Source device must **not** do), a Sink device is recommended to reply with an I2C_NACK|AUX_ACK and issue I2C STOP condition to its I^2C slave.

When a Source device neither completes/terminates nor initiates a new I^2C transaction, a Sink device must timeout after a certain period (e.g., 1s) and issue I2C STOP condition to its I^2C slave to avoid locking up the I^2C bus within a Sink device indefinitely. This scenario is possible when a Source device is powered down, disconnected, or somehow locked up in the middle of an I^2C transaction.

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A Sink device supporting detection of Source and/or Powered-Source is recommended to issue I2C STOP condition to its I^2C slave when a disconnect event is detected in the middle of an I^2C transaction.

2.8.7.2.3 REPEATED I2C START Condition

A Source device may issue I^2C-over-AUX with MOT set to 1, then issue another I^2C-over-AUX to the same I^2C Device Address, but a different command (i.e., write followed by read or read followed by write).

A Source device may also issue I^2C-over-AUX with MOT set to 1, then issue another I^2C-over-AUX to a different I^2C Device Address with the same command (i.e., write followed by write or read followed by read).

The Sink device must initiate the second I^2C transaction following Repeated I^2C Start, instead of I2C STOP.

2.8.7.2.4 I^2C-write-over-AUX

This section describes the permissible replies by a Sink device after receiving an I^2C-write-over-AUX request transaction from a Source device. A Sink device must reply with one of the ways as described in this section.

2.8.7.2.4.1 I2C_ACK|AUX_ACK followed by No “M” Value

All the data bytes have been written to and ACKed by the I^2C slave.

- When the MOT bit was 0, the I^2C transaction is complete. The Sink device must issue I2C STOP condition to its I^2C slave.
- When the MOT bit was 1, the I^2C transaction is still ongoing. The Sink device must not issue I^2C STOP condition.
  - If the ensuing I^2C-over-AUX transaction is either I^2C-read-over-AUX or to a different I^2C Device Address, the Sink device must issue I2C REPEATED START condition to its I^2C slave.

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2.8.7.2.4.2 I2C_ACK|AUX_ACK followed by "M" Value

Of the data bytes sent by the Source device, the number of bytes equal to "M" (that is smaller than LEN + 1 value) have been written to and ACKed by the I^2C slave.

The Sink device must continue writing to its I^2C slave until the number of bytes equal to LEN + 1 has been ACKed by the slave.

- Upon receiving ensuing I2C_WRITE_STATUS_UPDATE request transaction, the Sink device must reply with I2C_ACK|AUX_ACK with the updated "M" value.
- Upon receiving ensuing address-only I^2C-over-AUX with MOT bit cleared to 0 transaction, the Sink device must issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.
- Upon receiving ensuing I^2C-over-AUX transaction that is neither I2C_WRITE_STATUS_UPDATE nor an address-only I^2C-over-AUX with MOT bit cleared to 0, the Sink device is recommended to reply with I2C_NACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction. (A Source device must issue either I2C_WRITE_STATUS_UPDATE or an address-only I^2C-over-AUX with MOT bit cleared to 0.)

2.8.7.2.4.3 I2C_DEFER|AUX_ACK

None of the data bytes has been ACKed/NACKed by the I^2C slave.

- A Sink device must continue writing to its I^2C slave until the number of bytes equal to LEN+1 has been ACKed by the slave.
  - Upon receiving ensuing I2C_WRITE_STATUS_UPDATE request transaction, the Sink device must reply with I2C_ACK|AUX_ACK with the updated "M" value. If the Sink device has yet to receive ACK from the I^2C slave, however, it is to issue I2C_DEFER|AUX_ACK again.
  - Upon receiving ensuing address-only I^2C-over-AUX with MOT bit cleared to 0 transaction, the Sink device must reply with I2C_ACK|AUX_ACK to Source device and issue I^2C STOP condition to its slave promptly even before completion of the current I^2C transaction.
  - Upon receiving ensuing I^2C-over-AUX transaction that is neither I2C_WRITE_STATUS_UPDATE nor an address-only I^2C-over-AUX with MOT bit cleared to 0, the Sink device is recommended to reply with I2C_NACK|AUX_ACK to Source device and issue I^2C STOP condition to its slave promptly even before completion of the current I^2C transaction. (A Source device must issue either I2C_WRITE_STATUS_UPDATE or an address-only I^2C-over-AUX with MOT bit cleared to 0.)

2.8.7.2.4.4 I2C_NACK|AUX_ACK followed by Either "M" Value or No "M" Value

Either I^2C Device Address or Data byte are NACKed by the I^2C slave.

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2.8.7.2.4.5 AUX_DEFER

A Sink device is handling the request, but is not ready to reply with either I2C_ACK or I2C_NACK. Until NACKed by the I^2C slave, the Sink device must continue handling the request.

- Upon receiving ensuing I^2C-write-over-AUX transaction identical to the previous one (the same I^2C Device Address, LEN value, and Data bytes), the Sink device will reply to the Source device as described in this section while continuing handling the request.
- Upon receiving ensuing address-only I^2C-write-AUX with MOT bit cleared to 0 transaction, the Sink device must reply with I2C_ACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.
- Upon receiving ensuing I^2C-over-AUX transaction that is neither identical to the previous one nor an address-only I^2C-write-over-AUX transaction, the Sink device is recommended to reply with I2C_NACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction. (A Source device must issue either an I^2C-write-over-AUX transaction identical to the previous one or an address-only- I^2C-over-AUX with MOT bit cleared to 0.)

2.8.7.2.4.6 AUX_NACK followed by Either “M” Value or No “M” Value

A Sink device must not reply with AUX_NACK to I^2C-write-over-AUX transaction, unless there is a mismatch between the LEN + 1 value and the number of received data bytes.

2.8.7.2.4.7 No Reply

A Sink device must reply unless it either has detected an illegal command or is in a power-save mode due to the write of 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, via a Native AUX transaction.

2.8.7.2.5 I^2C-read-over-AUX

This section describes the permissible replies by a Sink device after receiving an I^2C-read-over-AUX request transaction from a Source device. A Sink device must reply with one of the ways as shown in this section.

2.8.7.2.5.1 I2C_ACK|AUX_ACK followed by the Total Number of Data Bytes Equal to LEN + 1

All the data bytes have been read from the I^2C slave.

- When the MOT bit was 0, the I^2C transaction is complete. The Sink device must issue NACK to the final Data byte and issue I2C STOP condition to its I^2C slave.
- When the MOT bit was 1, the I^2C transaction is still on-going. The Sink device must not issue I2C STOP condition.
  - If the ensuing I^2C-over-AUX transaction is I^2C-write-over-AUX or I^2C-read-over-AUX to a different I^2C Device Address, the Sink device must issue REPEATED I2C START condition to its I^2C slave.

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2.8.7.2.5.2 I2C_ACK|AUX_ACK followed by the Total Number of Bytes Fewer than LEN + 1

The Sink device must continue reading from its I^2C slave until the number of bytes equal to LEN + 1 has been read.

- Upon receiving ensuing I^2C-read-over-AUX transaction to the same I^2C Device with the LEN value updated to equal to the original value minus the total number of bytes replied by the Sink device so far, the Sink device must reply with I2C_ACK|AUX_ACK with the Data bytes that have been read from the Slave but were not replied back to the Source device in the previous reply transaction(s).
- Upon receiving ensuing I^2C-read-over-AUX transaction to the same I^2C Device with the same LEN value as the original value, the Sink device must reply with number of Data bytes equal to LEN value + 1 (or fewer if it cannot) irrespective of how many bytes it had already replied.
- Upon receiving ensuing Address-only I^2C-over-AUX transaction with MOT = 0, the Sink device must terminate the I^2C transaction by issuing I2C STOP.
- Upon receiving ensuing I^2C-over-AUX transaction that is none of the above, the Sink device is recommended to reply with I2C_NACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.

2.8.7.2.5.3 I2C_DEFER|AUX_ACK

A Sink device must continue reading from its I^2C slave until the number of bytes equal to LEN + 1 has been read.

- Upon receiving ensuing I^2C-read-over-AUX transaction identical to the previous one (the same I^2C Device Address and LEN value), the Sink device must reply with I2C_ACK|AUX_ACK with the Data bytes that have been read from the Slave but were not replied back to the Source device in the previous reply transaction.
- Upon receiving ensuing address-only I^2C-over-AUX with MOT bit cleared to 0 transaction, the Sink device must reply with I2C_ACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.
- Upon receiving ensuing I^2C-over-AUX transaction that is neither identical to the previous one nor an address-only I^2C-over-AUX with MOT bit cleared to 0, the Sink device is recommended to reply with I2C_NACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.

2.8.7.2.5.4 I2C_NACK|AUX_ACK

I^2C Device Address is NACKed by the I^2C slave.

It should be noted that the Sink device is not to terminate the I^2C transaction following I2C_NACK to the I^2C Device Address. Therefore, the Source device must prompt the termination, by issuing an address-only I^2C-over-AUX transaction with MOT bit cleared to 0.

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2.8.7.2.5.5 AUX_DEFER

The Sink device is handling the request, but is not ready to reply with either I2C_ACK or I2C_NACK. Until NACKed by the I^2C slave (to the I^2C Device Address). The Sink device must continue handling the request.

- Upon receiving ensuing I^2C-read-over-AUX transaction identical to the previous one (the same I^2C Device Address and LEN value), the Sink device will reply to the Source device as described in this section while continuing handling the request.
- Upon receiving ensuing address-only I^2C-over-AUX transaction with MOT bit cleared to 0, the Sink device must reply with I2C_ACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.
- Upon receiving ensuing I^2C-over-AUX transaction that is neither identical to the previous one nor an address-only I^2C-read-over-AUX transaction, the Sink device is recommended to reply with I2C_NACK|AUX_ACK to the Source device and issue I2C STOP condition to its slave promptly even before the completion of the current I^2C transaction.

2.8.7.2.5.6 AUX_NACK

A Sink device must not reply with AUX_NACK to I^2C-read-over-AUX transaction.

2.8.7.2.5.7 No Reply

A Sink device must reply unless it either has detected an illegal command or is in a power-save mode due to the write of 02h value to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) by the Source device, via a Native AUX transaction.

2.8.7.2.6 Clock Stretching

When reading the last Data byte of an I^2C-read-over-AUX with MOT bit set to 1, the I^2C master within a DPRX must stretch the I^2C clock after the eighth pulse (i.e., the last data bit), instead of after the ninth pulse (I^2C ACK/NACK). When the ensuing I^2C-over-AUX transaction is the address-only with MOT bit cleared to 0, the I^2C master within the DPRX must assert I2C NACK to its I^2C slave. Otherwise, it must assert I2C ACK.

For I^2C Device Address and Data write, I^2C master within a DPRX must stretch the I^2C clock after the ninth pulse (i.e., ACK/NACK bit).

2.8.7.3 Accessing EDID of More Than Two Blocks

An EDID of more than two blocks may be used by a DP Sink device for stream sink capability exposure. A DP Source device and DP Sink device must use E-DDC segment protocol to retrieve extra blocks. The DP Sink device must automatically reset the segment offset to 0 whenever a DP Source device sends and I^2C-over-AUX transaction with MOT=0 (indicating an I^2C STOP condition).

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2.9 AUX Services

This section describes two types of AUX services – AUX Link Services and AUX Device Services. These are the Link Layer services used by “Policy Makers” for link and device management in the Source and Sink devices.

Whenever the Hot Plug Detect signal is active (connectors are plugged in and the Sink device has at least a “trickle” AC power), AUX services must be available.

There are two Policy Makers:

- Stream Policy Maker
  - Manages stream
    - Stream transport initialization, and maintenance (more on this subject is covered in the following sections)
    - Uses AUX Device Services
    - Gets link information from Link Policy Maker
- Link Policy Maker
  - Manages link
    - Link discovery, initialization, and maintenance
    - Uses AUX Link Services

Both Source and Sink devices must have these two policy makers. Policy Makers may be implemented as operating system, software driver, firmware, or hardware state machine. The choice is implementation-specific.

In this Standard, only the semantics of the interface between the Link Layer and Stream Policy Makers is defined. Syntax (i.e., API) is implementation-specific, and not covered in this Standard.

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2.9.1 Stream Transport Initiation Sequence

The Stream Source Policy Maker, before transport initiation, must take the following actions:

- Read EDID from the Sink device
- Set stream attributes for Main Stream attribute data and *CEA-861-F* INFOFRAME generation
- Optionally (recommended), get the following information from the Link Policy Maker
  - Link Configuration field (DPCD Addresses 00100h through 001FFh; see Table 2-156) – Total link bandwidth
    - To avoid oversubscription of the link bandwidth
  - Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155) – Number and types of ports available in RX
    - To determine the number and types of streams that may be transported
  - Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157) – Synchronized? Excessive error symbols?
    - To make sure that the link is ready for transport

When a stream is ready for transport, the Stream Source Policy Maker must start the transport of isochronous stream along with stream attributes data.

The Stream sink, upon receiving a stable stream, must decode the stream attributes data and start reconstructing the incoming isochronous stream.

The Stream Source Policy Maker may incorporate the receiver capability information for the stream source management: A DP-aware Stream Source Policy Maker, for example, may try to limit the stream bandwidth to prevent link bandwidth oversubscription. If a stream is going to oversubscribe the link bandwidth, the Stream Source Policy Maker may inform the stream source. The stream source, upon receiving this notice, may take a corrective action, such as the reduction of image resolution and/or color depth (in bits per pixel).

Though it is desirable, such an interaction between two policy makers is optional. In other words, DisplayPort Link must be implemented to function with a legacy Source Policy Maker that is unaware of DisplayPort.

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Diagrams of a typical action flow of the Source and Sink devices upon a Hot Plug Detect event are shown in Figure 2-114.

Notes: *The diagrams are examples only. It is not required, for instance, that an EDID read precede a DPCD read.*

Figure 2-114 shows a typical action flow for a consumer detachable, box-to-box DP connection. When DisplayPort is used for an embedded connection, such as from a GPU to a notebook panel TCON within a notebook PC, a DPCD read may not be needed. In this embedded configuration, the Source device (GPU) may, instead, use the DPRX's pre-set receiver capability information.

Figure 2-114: Action Flow Sequences of the Source upon HPD Event (Informative)

2.9.2 Stream Transport Termination Sequence

Examples of events causing stream termination are:

- Link error event notice by a Link Policy Maker
- Stream timing change
- Stream format change, unstable stream timing, or loss of stream

The stream source must terminate the transport of the Main Stream and Secondary-data. It may re-initiate the transport following the initiation sequence after the link is re-established. The recommended corrective action for the stream sink is to either display a blank screen, possibly with an alert message, or to turn off the display until stable stream reception is resumed.

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2.9.3 DPCD Field Address Mapping

Table 2-154 lists the DisplayPort address mapping and the tables in which they are listed (Table 2-155 through Table 2-170) for the byte-addressed DPCD.

Table 2-154: DPCD Field Address Mapping

DPCD Address	DPCD Field	See
00000h through 000FFh	Receiver Capability	Table 2-155
00100h through 001FFh	Link Configuration	Table 2-156
00200h through 002FFh	Link/Sink Device Status	Table 2-157
00300h through 003FFh	Source Device-specific	Table 2-158
00400h through 004FFh	Sink Device-specific	Table 2-159
00500h through 005FFh	Branch Device-specific	Table 2-160
00600h through 006FFh	Link/Sink Device Power Control	Table 2-161
00700h through 007FFh	eDP-specific	Table 2-162
00800h through 00FFFh	RESERVED (usage to be defined)	–
01000h through 017FFh	Sideband MSG Buffers	Table 2-163
01800h through 01FFFh	RESERVED (usage to be defined)	–
02000h through 021FFh	DPRX Event Status Indicator	Table 2-164
02200h through 022FFh	Extended Receiver Capability	Table 2-165
02300h through 02FFFh	RESERVED (usage to be defined)	–
03000h through 030FFh	Protocol Converter Extension	Table 2-166
03100h through 5FFFFh	RESERVED (usage to be defined)	–
60000h through 61CFFh	Multi-touch (for eDP)	Table 2-167
61D00h through 67FFFh	RESERVED (usage to be defined)	–
68000h through 69FFFh	HDCP 1.3 and HDCP2.2	Table 2-168
6A000h through EFFFFh	RESERVED (usage to be defined)	–
F0000h through F02FFh	LT-tunable PHY Repeater	Table 2-169
F0300h through FFEFFh	RESERVED (usage to be defined)	–
FFF00h through FFFFFh	MyDP-specific	Table 2-170

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2.9.3.1 DPCD Data Structure Revision Declaration

In this Standard, the Extended Receiver Capability field is added. The Extended Receiver Capability field at DPCD Addresses 02200h through 022FFh is valid with DPCD Rev. 1.4 (and higher). DPCD Addresses 02200h through 0220Fh (Extended Base Receiver Capability registers) match DPCD Addresses 00000h through 0000Fh (original Base Receiver Capability registers) except for the following three registers (the values might differ):

- DPCD_REV register (DPCD Address 00000h)
- MAX_LINK_RATE register (DPCD Address 00001h)
- DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h)

The Extended Receiver Capability registers at DPCD Addresses 02200h through 0220Fh must contain the DPRX's true capability, while the original Base Receiver Capability registers at DPCD Addresses 00000h through 0000Fh might indicate DPCD r1.1, a MAX_LINK_RATE of 2.7Gbps/lane, and no DFP to avoid interoperability issues with some of the existing DP Source devices that malfunction when they discover the higher capabilities within those three registers. A DPRX that supports the Extended Receiver Capability field must set the EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT bit in the TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bit 7) to 1. The Extended Receiver Capability field has a data structure that helps a device that has a DPTX better comprehend the receiver's capability (e.g., the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h)). The DPCD Revision number at DPCD Address 00000h must not be higher than that at DPCD Address 02200h.

A downstream device must reset all DPCD Control and Configuration registers that are to be set by an upstream device, under the following conditions:

- Upon power-on reset, before asserting the HPD signal
- Upon detecting the disconnect of the upstream device

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2.9.3.2 DPCD Field Address Mapping Tables

Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
Note: *This table includes a* ***Byte #*** *column, for those registers that include multiple bytes within the Receiver Capability field. For those that do not include multiple bytes, the column is left blank.*				
00000h	**DPCD_REV** DPCD data structure revision number.			Read Only
		3:0	**Minor Revision Number**	
		7:4	**Major Revision Number** 10h = DPCD r1.0. 11h = DPCD r1.1. 12h = DPCD r1.2. 13h = DPCD r1.3 (for *eDP v1.4* DPRX only). 14h = DPCD r1.4. All other values are RESERVED. A DP device with a DPRX with DPCD r1.2 (or higher) must support the GUID register (DPCD Addresses 00030h through 0003Fh). Furthermore, a DP Sink device with DPCD r1.2 (or higher) with stereo display capability support (as declared in EDID and DisplayID) must support the handling of 3D Stereo in-band signaling using Video_Stream_Configuration (VSC) SDP. ***Note:*** *The DPCD revision number does not necessarily match the DisplayPort version number.*	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00001h	**MAX_LINK_RATE** Maximum link rate of Main-Link lanes = Value x 0.27Gbps per lane.			Read Only
		7:0	**MAX_LINK_RATE** Only four values are supported. All other values are RESERVED except for *eDP v1.4* (DPCD r1.3 or lower) and MyDP DPRX. 06h = 1.62Gbps/lane. 0Ah = 2.7Gbps/lane. 14h = 5.4Gbps/lane. 1Eh = 8.1Gbps/lane. *eDP v1.4* DPRX (DPCD r1.3 or lower) can program the MAX_LINK_RATE register value to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. See *eDP v1.4b*. A MyDP DPRX of an active MyDP converter (either MyDP-to-legacy converter or MyDP-to-DP lane-count converter) can support a value of 19h (6.75Gbps/lane). As for the MAX_LINK_RATE value requirement of an SST-only Branch device in the presence of a downstream device, see Section 2.1.4.1.	
00002h	**MAX_LANE_COUNT** Maximum number of lanes = Value.			Read Only
		4:0	**MAX_LANE_COUNT** Only three values are supported. All other values are RESERVED. 1h = One lane (Lane 0 only). 2h = Two lanes (Lanes 0 and 1 only). 4h = Four lanes (Lanes 0, 1, 2, and 3). As for the MAX_LANE_COUNT value requirement of an SST-only Branch device in the presence of a downstream device, see Section 2.1.4.1.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00002h		5	**POST_LT_ADJ_REQ_SUPPORTED** 0 = Post-Link Training Adjust Request is not supported. 1 = Post-Link Training Adjust Request is supported (see Section 3.5.1.2.4). POST_LT_ADJ_REQ is the third phase of Link Training. This procedure is used only if TPS4 cannot be used in the second (i.e., EQ) phase of Link Training. (TPS4 can be used only if the DPTX and DPRX both support TPS4.) An upstream device with a DPTX (Source or Branch device) aware of the procedure indicates granting of the procedure by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5). The downstream device indicates that the procedure is in progress by setting the POST_LT_ADJ_REQ_IN_PROGRESS bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 1, respectively). This is done at the end of the second phase of Link Training when the downstream device sets Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157) register bits to indicate LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE completion.	Read Only
		6	**TPS3_SUPPORTED** Indicates Link Training Pattern Sequence 3 (TPS3) support. 0 = TPS3 is not supported. 1 = TPS3is supported (mandatory for Downstream devices that support HBR2, optional for others).	
		7	**ENHANCED_FRAME_CAP** Applies only to Single Stream Transport Format. 0 = Enhanced Framing symbol sequence for BS and SR is not supported. 1 = Enhanced Framing symbol sequence for BS and SR is supported as described in Section 2.2.1.2. A DPRX with DPCD Data Structure r1.1 and higher (as expressed in the DPCD_REV register (DPCD Address 00000h)) must set this bit to 1. ***Note:*** *Non-Enhanced Framing (referred to as Default Framing) was deprecated in DPCD r1.4.*	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00003h	**MAX_DOWNSPREAD**			Read Only
		0	**MAX_DOWNSPREAD** 0 = No down spread. 1 = Up to 0.5% down-spread. Support of up to 0.5% down-spread is required for DPCD r1.1 (and higher) Sink and Branch devices. Therefore, this bit must be set to 1.	
		5:1	**RESERVED**	Read all 0s
		6	**NO_AUX_TRANSACTION_LINK_TRAINING** 0 = Requires AUX transactions to synchronize to a DPTX. 1 = Does not require AUX transactions when the link configuration is already known. A DPTX, when it activates its Main-Link, can transmit TPS1 and TPS2 (or TPS3 or TPS4) for the minimum of 500us each. The known-good drive current and pre-emphasis level (or those used in the last "full" Link Training with AUX transactions) must be used when Link Training is performed without AUX transactions. Regardless of this bit's value, a DP Sink device must send an IRQ_HPD pulse when it cannot synchronize to the incoming stream. For embedded implementations in which there is no HPD line, either the proper operation should be guaranteed by design or the Source device can periodically poll the link status.	Read Only
		7	**TPS4_SUPPORTED** Indicates Link Training Pattern Sequence 4 (TPS4) support. 0 = TPS4 is not supported. 1 = TPS4 is supported (mandatory for Downstream devices with DPCD r1.4, except for eDP DPRXs).	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00004h	**NORP & DP_PWR_VOLTAGE_CAP** ***Note:*** *When bits 7:5 of this register are cleared to 000, the downstream device is capable of producing the default 3.3V DP_PWR setting DP_PWR only.* *A downstream DP device capable of generating DP_PWR voltage higher than the default 3.3V DP_PWR setting must complete the voltage level transition within 1ms. During the transition, the DP device must not generate a voltage exceeding the voltage range of the higher of the two voltage levels between which the switching is taking place.*			Read Only
		0	**NORP** Number of Receiver Ports = Value + 1. 0 = One receiver port. 1 = Two or more receiver ports (see Note below). For SST transport format, the maximum number is two (for which this bit is set to 1), one for an uncompressed video stream and the other for its associated audio stream. The receiver can simultaneously receive up to "NORP" isochronous streams. The smallest available Receiver Port number is assigned. For example, when there is only one receiver port, the receiver port is assigned to Receiver Port 0. Receiver Port 1 shall be assigned only after Receiver Port 0 has already been assigned. ***Note:*** *An MST Sink device might have more than two receiver ports because it can have three or more stream sinks. However, an MST Sink device must program this bit according to the number of receiver ports when it is operating in SST mode. The MST Sink device is required to operate in SST mode to interoperate with an SST upstream device.* *A Topology Manager in an MST Source device must use the LINK_ADDRESS and REMOTE_DPCD message transactions to discover the number of receiver ports, rather than relying on this bit.*	
		4:1	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00004h		5	**5V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +4.9 to +5.5V on the DP_PWR pin of its DP connector. 1 = Downstream device is capable of producing +4.9 to +5.5V on the DP_PWR pin of its DP connector.	Read Only
		6	**12V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +12V ±10%. 1 = Downstream device is capable of producing +12V ±10% on the DP_PWR pin of its DP connector.	
		7	**18V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +18V ±10%. 1 = Downstream device is capable of producing +18V ±10% on the DP_PWR pin of its DP connector.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00005h	**DOWN_STREAM_PORT_PRESENT**			Read Only
		0	**DFP_PRESENT** 1 = Device is a Branch device and has downstream-facing port(s) (DFP(s)).	
		2:1	**DFP_TYPE** Indicates the DFP type of DFP 0. 00 = DisplayPort. 01 = Analog VGA or analog video over DVI-I. 10 = DVI, HDMI, or DP++. 11 = Others (this DFP type might not have an EDID in the Sink device; for example, Sink devices on composite video and Svideo ports do not have an EDID, but Sink devices on a wireless or USB interface might). A Branch device must provide more-detailed Downstream enumeration data on all of its DFPs, including DFP 0 at DPCD Address 00080h and above. ***Note:*** *Further requirements for Branch devices are provided in Section 5.3.3. Requirements for Source devices when transmitting through a Branch device are provided in Section 5.1.6.*	
		3	**FORMAT_CONVERSION** 0 = This Branch device does not have a format conversion block. 1 = This DFP has a format conversion block. ***Notes:*** *1 Applicable only to a Branch device.* *2 Topology Manager in an MST Source device must use the LINK_ADDRESS message transaction to discover the DFP capability, rather than relying on this bit.*	
		4	**DETAILED_CAP_INFO_AVAILABLE** 0 = DFP capability field is 1 byte per port, starting from DPCD Address 00080h. 1 = DFP capability field is 4 bytes per port for detailed capability description starting from DPCD Address 00080h. For DPRX and DPCD r1.4, detailed capability information support is mandatory.	
		7:5	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00006h	**MAIN_LINK_CHANNEL_CODING**			Read Only
		0	**ANSI 8b/10b** 1 = DisplayPort receiver supports the Main-Link channel coding specification, as specified in ANSI X3.230-1994, Clause 11.	
		7:1	**RESERVED**	Read all 0s
00007h		**DOWN_STREAM_PORT_COUNT**		Read Only
		3:0	**DFP_COUNT** Indicates the number of DFPs. 0h = No DFPs. Type and capability of the DFP are enumerated at DPCD Addresses 00080h through 0008Fh.	
		5:4	**RESERVED**	Read all 0s
		6	**MSA_TIMING_PAR_IGNORED** Applies to eDP and box-to-box DP. 0 = Sink device requires the MSA timing parameters HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW) to be sent by the Source device for rendering the incoming video stream. 1 = Sink device is capable of rendering the incoming video stream without the above-mentioned MSA timing parameters.	Read Only
		7	**OUI Support** 0 = OUI is not supported. 1 = OUI is supported (OUI and Device Identification mandatory for DPCD r1.2 and DPCD r1.4; for DPCD r1.3 (which is for *eDP v1.4* DPRX), support for OUI is an implementation option). IEEE_OUI registers (DPCD Addresses 00400h through 00402h) for a Sink device, plus DPCD Addresses 00403h through 0040Bh for Device Identification. IEEE_OUI registers (DPCD Addresses 00500h through 00502h) for a Branch device, plus DPCD Addresses 00503h through 0050Bh for Device Identification.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00008h	**RECEIVE_PORT0_CAP_0** Note updated in *DP v1.4*. Support for bits 5:3 added in *DP v1.4*. Receiver Port 0 Capability 0. ***Note:*** *A Source device operating in MST mode does not use this MST Sink/Branch device register.*			Read Only
		0	**RESERVED**	Read all 0s
		1	**LOCAL_EDID_PRESENT** 0 = This receiver port does not have a local EDID. 1 = This receiver port has a local EDID. A local EDID is mandatory for Sink devices and Format Converters.	Read Only
		2	**ASSOCIATED_TO_PRECEDING_PORT** 0 = This port is used for the main isochronous stream. This bit must always be cleared to 0 for Receiver Port 0. 1 = This port is used for the secondary isochronous stream of the main stream received in the preceding port.	
		3	**HBLANK_EXPANSION_CAPABLE** 0 = DPRX is not capable of Horizontal Blanking Expansion operation. 1 = DPRX is capable of Horizontal Blanking Expansion operation.	
		4	**BUFFER_SIZE_UNIT** Defines the units to be used for defining the buffer size declared in the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h). 0 = Units are in pixel counts. 1 = Units are in byte counts. The DPRX shall ensure that the byte count unit is converted to the pixel count unit, as follows: Buffer_Size_in_Pixels = Buffer_Size_in_Bytes/Pixel_Depth_in_Bytes	
		5	**BUFFER_SIZE_PER_PORT** Defines units used for defining the buffer size declared in the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h). 0 = Buffer size is per-lane. 1 = Buffer size is per-port and independent of the lane count.	
		7:6	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00009h	**RECEIVE_PORT0_CAP_1** Updated in *DP v1.4*. Receiver Port 0 Capability 1. ***Note:*** *A Source device operating in MST mode does not use this MST Sink/Branch device register.*			Read Only
		7:0	**BUFFER_SIZE** Buffer size = (Value + 1) × 32. The unit is defined by the following RECEIVE_PORT0_CAP_0 register (DPCD Address 00008h) bits: • BUFFER_SIZE_UNIT bit (bit 4) value, and • BUFFER_SIZE_PER_PORT bit (bit 5) value, per-lane or per-port	
0000Ah	**RECEIVE_PORT1_CAP_0** Receiver Port 1 Capability 0. Bit definition is identical to that of the RECEIVE_PORT0_CAP_0 register (DPCD Address 00008h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 is not present, this register is read all 0s.* *2 A Source device operating in MST mode does not use this register.*			Read Only

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0000Bh	**RECEIVE_PORT1_CAP_1** Receiver Port 1 Capability 1. Bit definition is identical to that of the RECEIVE_PORT0_CAP_1 register (DPCD Address 00009h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 not present, this register is read all 0s.* *2 A Source device operating in MST mode does not use this field.*			Read Only
0000Ch	**I^2C Speed Control Capabilities Bit Map** Bit or bits set to indicate I^2C speed control capabilities. Support for source control of the I^2C speed is optional but recommended when the DPRX implements a physical I^2C bus. If the DPRX does not implement a physical I^2C bus, this register is cleared to 00h. Otherwise, if the DPRX does not provide source control of the I^2C speed, this register is also cleared to 00h. In this case the DPRX, upon receiving an I^2C-over-AUX transaction, generates an I^2C transaction at the I^2C bit rate of its choice. Otherwise, bit values in this register are assigned to I^2C speeds. 00000001b = 1Kbps. 00000010b = 5Kbps. 00000100b = 10Kbps. 00001000b = 100Kbps. 00010000b = 400Kbps. 00100000b = 1Mbps. 01000000b = RESERVED. 10000000b = RESERVED.			Read Only
0000Dh	**eDP_CONFIGURATION_CAP** RESERVED for eDP. Always reads 00h for external receivers.			Read Only

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0000Eh	**TRAINING_AUX_RD_INTERVAL**			Read Only
		6:0	**TRAINING_AUX_RD_INTERVAL** Link Status/Adjust Request read interval during Main-Link Training. 00h = 100us for the Main-Link Clock Recovery phase and 400us for the Main-Link Channel Equalization phase. 01h = 100us for the Main-Link Clock Recovery phase; 4ms for the Main-Link Channel Equalization phase. 02h = 100us for the Main-Link Clock Recovery phase; 8ms for the Main-Link Channel Equalization phase. 03h = 100us for the Main-Link Clock Recovery phase; 12ms for the Main-Link Channel Equalization phase. 04h = 100us for the Main-Link Clock Recovery phase; 16ms for the Main-Link Channel Equalization phase. All other values are RESERVED.	
		7	**EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT** 0 = Not present. 1 = Present at DPCD Addresses 02200h through 022FFh. A DPRX with DPCD r1.4 (or higher) must have an Extended Receiver Capability field.	
0000Fh	**ADAPTOR_CAP** Capabilities of Branch devices that adapt to legacy video transports.			Read Only
		0	**FORCE_LOAD_SENSE_CAP** 0 = Does not support VGA force load adaptor sense mechanism. 1 = Supports VGA force load adaptor sense mechanism.	
		1	**ALTERNATE_I2C_PATTERN_CAP** 0 = Does not support alternate I^2C patterns. 1 = Supports alternate I^2C patterns.	
		7:2	**RESERVED**	Read all 0s
00010h through 0001Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only.** **For other DPCD Revisions up to DPCD r1.4, RESERVED.**			
	SUPPORTED_LINK_RATES See *eDP v1.4*.			
00020h	**RESERVED** (Deprecated FAUX-related register.)			Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00021h	**MSTM_CAP**			Read Only
		0	**MST_CAP** 0 = Does not support MST format and has no Branching Unit, and therefore does not support Sideband MSG handling. 1 = Supports MST format and has a Branching Unit, and therefore supports Sideband MSG handling.	
		7:1	**RESERVED**	Read all 0s
00022h	**NUMBER_OF_AUDIO_ENDPOINTS** Number of audio endpoints available at this port. Applies to both audio devices (i.e., devices with no video endpoints) and devices with video endpoints that have audio endpoints associated with them. This value must be 0 for Branch devices. ***Notes:*** *Audio endpoints are always associated with video endpoints in devices with video endpoints.* *A DP Sink device declares its audio stream sinking capability by setting the NORP bit in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bit 0) to 1 and by placing the audio capability descriptor in the CEA Extension Block of EDID. When these fields indicate the presence of an audio stream sinking capability and the NUMBER_OF_AUDIO_ENDPOINTS register is cleared to 0, a DP Source device must assume that the number of audio endpoints for this DP device is equal to 1.* *A DP Sink device that has more than one audio endpoint must set this register equal to the number of endpoints.*			Read Only

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00023h	**AV_SYNC_DATA_BLOCK AV_GRANULARITY** ***Note:*** *DPRX's AV_SYNC capability discovery – Not all DPRXs with DPCD r1.2 or higher support the AV_SYNC feature. Devices with a DPTX that want to use this register value are recommended to verify that the AV_SYNC_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 2) is set to 1.*			Read Only
		3:0	**AG_FACTOR** Audio Granularity factor values used for the AUD_DEC_LAT[7:0], AUD_DEC_LAT[15:8], AUD_PP_LAT[7:0], and AUD_PP_LAT[15:8] fields in the AV_SYNC_DATA_BLOCK registers (DPCD Addresses 00024h through 00027h, respectively). 0000 = 3ms 0001 = 2ms (default) 0010 = 1ms 0011 = 500us 0100 = 200us 0101 = 100us 0110 = 10us 0111 = 1us All other values are RESERVED.	
		7:4	**VG_FACTOR** Video Granularity factor values used for the VID_INTER_LAT[7:0] and VID_PROG_LAT[7:0] fields in the AV_SYNC_DATA_BLOCK registers (DPCD Addresses 00028h and 00029h, respectively). 0000 = 3ms 0001 = 2ms (default) 0010 = 1ms 0011 = 500us 0100 = 200us 0101 = 100us All other values are RESERVED.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00024h	**AV_SYNC_DATA_BLOCK**			Read Only
	0	7:0	**AUD_DEC_LAT[7:0]** AUD_DEC_LAT is the worst-case Audio decode post processing latency reported in the AUD_PP_LAT[7:0], and AUD_PP_LAT[15:8] fields in the AV_SYNC_DATA_BLOCK registers (DPCD Addresses 00026h through 00027h, respectively). (Reported in terms of AG factor.)	
00025h	**AV_SYNC_DATA_BLOCK**			Read Only
	1	7:0	**AUD_DEC_LAT[15:8]**	
00026h	**AV_SYNC_DATA_BLOCK**			Read Only
	2	7:0	**AUD_PP_LAT[7:0]** AUD_PP_LAT is the worst case Audio post processing latency. (Reported in terms of AG factor.)	
00027h	**AV_SYNC_DATA_BLOCK**			Read Only
	3	7:0	**AUD_PP_LAT[15:8]**	
00028h	**AV_SYNC_DATA_BLOCK**			Read Only
	4	7:0	**VID_INTER_LAT[7:0]** Worst-case Video interlaced latency for Video/Film mode. (Reported in terms of VG factor.)	
00029h	**AV_SYNC_DATA_BLOCK**			Read Only
	5	7:0	**VID_PROG_LAT[7:0]** Worst-case Video progressive latency for Video/Film mode. (Reported in terms of VG factor.)	
0002Ah	**AV_SYNC_DATA_BLOCK**			Read Only
	6	7:0	**REP_LAT[7:0]** Delay incurred in the repeater/Branch device while receiving and forwarding DP streams to the downstream device, in 10us granularity.	
0002Bh	**AV_SYNC_DATA_BLOCK**			Read Only
	7	7:0	**AUD_DEL_INS[7:0]** AUD_DEL_INS is the maximum additional delay that the Sink device is capable of inserting in addition to the inherent delays reported by the Sink device (AUD_DEC_LAT[7:0], AUD_DEC_LAT[15:8], AUD_PP_LAT[7:0], and AUD_PP_LAT[15:8] fields in the AV_SYNC_DATA_BLOCK registers (DPCD Addresses 00024h through 00027h, respectively)), in 1us granularity. Sink devices are required to support a minimum of 5ms of delay insertion in the Audio path.	
0002Ch	**AV_SYNC_DATA_BLOCK**			Read Only
	8	7:0	**AUD_DEL_INS[15:8]**	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0002Dh	**AV_SYNC_DATA_BLOCK**			Read Only
	9	7:0	**AUD_DEL_INS[23:16]**	
0002Eh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**			
	RECEIVER_ADVANCED_LINK_POWER_MANAGEMENT_CAPABILITES See *eDP v1.4*.			
0002Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**			
	AUX FRAME SYNC See *eDP v1.4*.			
00030h through 0003Fh	**GUID** Must be supported in all DPRX with DPCD revision number 1.2 or higher. Must be generated according to IETF RFC 4122 and stored in Network Byte Order, i.e.: • DPCD Address 00030h contains the first octet (time_low, MSB) • DPCD Address 0003Fh contains the last octet (node(5)) When a Sink device has an integrated USB or hub device, the Container ID of the Sink device must match the GUID in the Container Descriptor of that USB device or hub. All functions that are not removable from (i.e., are integrated into) the one physical device must advertise the same Container ID GUID, regardless of the interface (DP or non-DP) through which it is reported. In a Sink device that has multiple audio and video endpoints, all the endpoints must return the same GUID.			Read Only (Write/Read Only if DPCD r1.2 or higher, but 00030h through 0003Fh are all 0s as power-on reset values)
00040h	**For DockPort-capable DPRX (DPCD r1.2 or DPCD r1.4).**			
	DOCKPORT_CAP See *DockPort v1.0a*.			
00041h	**For DockPort-capable DPRX (DPCD r1.2 or DPCD r1.4).**			
	DisplayPort SpecVerMaj See *DockPort v1.0a*.			
00042h	**For DockPort-capable DPRX (DPCD r1.2 or DPCD r1.4).**			
	DisplayPort SpecVerMin See *DockPort v1.0a*.			
00043h through 00053h	**RESERVED**			Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00054h	**RX_GTC_VALUE_0** ***Note:*** *DPRX's GTC capability discovery – Not all DPRXs with DPCD r1.2 or higher support the GTC. Devices with a DPTX that want to use this register value are recommended to verify one of the following:* • *GTC_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 0) is set to 1* • *Downstream DPRX supports PSR2, which is defined in eDP v1.4* *When a device with a DPTX attempts GTC lock acquisition with a DPRX that does not support GTC, the lock acquisition fails with the DPRX not updating the RX_GTC_VALUE_x register.*			Read Only
	0	7:0	**RX_GTC_VALUE7:0**	
00055h	**RX_GTC_VALUE_1** See note for RX_GTC_VALUE_0 register.			Read Only
	1	7:0	**RX_GTC_VALUE15:8**	
00056h	**RX_GTC_VALUE_2** See note for RX_GTC_VALUE_0 register.			Read Only
	2	7:0	**RX_GTC_VALUE23:16**	
00057h	**RX_GTC_VALUE_3** See note for RX_GTC_VALUE_0 register.			Read Only
	3	7:0	**RX_GTC_VALUE31:24**	
00058h	**RX_GTC_MSTR_REQ**			Read Only
		0	**RX_GTC_MSTR_REQ** 0 = RX does not request to be a GTC Master. 1 = RX requests to be a GTC Master.	
		1	**TX_GTC_VALUE_PHASE_SKEW_EN** 0 = DPTX resets its GTC value to the received RX_GTC_VALUE (RX_GTC_VALUE_0, RX_GTC_VALUE_1, RX_GTC_VALUE_2, and RX_GTC_VALUE_3 registers (DPCD Addresses 00054h through 00057h, respectively)) and uses the delta between its GTC value and the received RX_GTC_VALUE to frequency adjust its GTC value. 1 = DPTX resets its GTC value to the received RX_GTC_VALUE, but does NOT use the delta between its GTC value and the received RX_GTC VALUE to frequency adjust its GTC value; in other words, the RX_GTC_VALUE is used for phase adjust only. Used only when the DPRX is the GTC Master.	
		7:2	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00059h	**RX_GTC_FREQ_LOCK_DONE**			Read Only
		0	**RX_GTC_FREQ_LOCK_DONE** 0 = DPRX has not realized the GTC_FREQ_LOCK_DONE 1 = DPRX has realized the GTC_FREQ_LOCK_DONE Used only when the DPTX is the GTC Master.	
		7:1	**RESERVED**	Read all 0s
0005Ah	**RX_GTC_PHASE_SKEW_OFFSET_0**			Read Only
	0	7:0	**RX_GTC_PHASE_SKEW_OFFSET7:0**	
0005Bh	**RX_GTC_PHASE_SKEW_OFFSET_1**			Read Only
	1	7:0	**RX_GTC_PHASE_SKEW_OFFSET15:8**	
0005Ch through 0005Fh	**RESERVED**			Read all 0s
00060h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00060h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC SUPPORT			
		0	**DSC Support** 0 = Decompression using DSC is not supported. 1 = Decompression using DSC is supported.	
		7:1	**RESERVED**	Read all 0s
00061h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00061h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC ALGORITHM REVISION			
		3:0	**DSC Version Major** Indicates the major version of DSC.	
		7:4	**DSC Version Minor** Indicates the minor version of DSC.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00062h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00062h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC RC BUFFER BLOCK SIZE			
		1:0	**RC Buffer Block Size** Rate control buffer block size. 00 = 1KB. 01 = 4KB. 10 = 16KB. 11 = 64KB.	
		7:2	**RESERVED**	Read all 0s
00063h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00063h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC RC BUFFER SIZE			
		7:0	**Each Rate Buffer Size, in Units of Blocks** Buffer size (in blocks) = value + 1. Actual buffer size is calculated by multiplying the RC buffer size (in blocks) and the block size indicated by the RC Buffer Block Size field in the DSC RC BUFFER BLOCK SIZE register (DPCD Address 00062h, bits 1:0). **Example** – If the RC Buffer Block Size is programmed to 11 (64KB) and the rate buffer size (in blocks) is 0111 1111 (128), each rate buffer size = 64KB × 128 = 8MB. ***Note:*** *This value is as specified in DSC v1.2, Table E-1. It is the maximum algorithmic rate buffer size (minRateBufferSize) that the Sink device may support and is used by the Source device to ensure that the hrdDelay requirement is met.*	
00064h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00064h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC SLICE CAPABILITIES 1 Used in combination with the DSC SLICE CAPABILITIES 2 register (DPCD Address 0006Dh) to indicate the number of slices per Display Line supported, per display. Each slice per Display Line must be supported in all resolutions that a DP DSC Sink device supports, as long as the slice width and decoder throughput requirements are not exceeded. 0 = Number of Slices per Display Line is not supported. 1 = Number of Slices per Display Line is supported.			
		0	**1 Slice per Display Line**	
		1	**2 Slices per Display Line**	
		2	**RESERVED**	Read 0
		3	**4 Slices per Display Line**	Read Only
		4	**6 Slices per Display Line** ***Note:*** *This value is not included as part of the standard slice value number set. A display may declare support of this number of slices per Display Line as an available configuration, in addition to the normative slice per Display Line value, as provided in Table 2-141.*	
		5	**8 Slices per Display Line**	
		6	**10 Slices per Display Line** ***Note:*** *This value is not included as part of the standard slice value number set. A display may declare support of this number of slices per Display Line as an available configuration, in addition to the normative slice per Display Line value, as provided in Table 2-141.*	
		7	**12 Slices per Display Line**	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00065h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00065h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC LINE BUFFER BIT DEPTH			
		3:0	**Line Buffer Bit Depth** Contains the bit depth used by the Sink device to store the reconstructed pixels within the line buffer. 0000 = 9 bits. 0001 = 10 bits. 0010 = 11 bits. 0011 = 12 bits. 0100 = 13 bits. 0101 = 14 bits. 0110 = 15 bits. 0111 = 16 bits. 1000 = 8 bits. All other values are RESERVED.	
		7:4	**RESERVED**	Read all 0s
00066h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00066h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC BLOCK PREDICTION SUPPORT			
		0	**Block Prediction Support** 0 = Block prediction is not supported. 1 = Block prediction is supported.	
		7:1	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00067h and 00068h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00067h and 00068h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	MAXIMUM *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR Indicates the maximum ***bits_per_pixel*** that the DP DSC Sink device may support. The format is U6.4 (unsigned, four fractional bits). ***Note:*** *Minimum **bits_per_pixel**, as well as the increment of **bits_per_pixel**, are indicated by the MINIMUM bits_per_pixel SUPPORTED BY THE DECOMPRESSOR register (DPCD Addresses 0006Eh and 0006Fh).*			
	0	7:0	***bits_per_pixel*7:0** Contains the least significant eight bits of the maximum ***bits_per_pixel*** that the DP DSC Sink device may support.	
	1	1:0	***bits_per_pixel*9:8** Contains the most significant two bits of the maximum ***bits_per_pixel*** that the DP DSC Sink device may support.	
	1	7:2	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00069h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
00069h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC COLOR FORMAT CAPABILITIES			
		0	**RGB Support** A DP DSC Sink device shall support RGB color format. 0 = RGB is not supported. 1 = RGB is supported.	
		1	**YCbCr 4:4:4 Support** 0 = YCbCr 4:4:4 is not supported. 1 = YCbCr 4:4:4 is supported.	
		3:2	**YCbCr 4:2:2 Support** 00 = YCbCr 4:2:2 is not supported. 01 = YCbCr 4:2:2 is supported (*DSC v1.1* or lower). 10 = YCbCr 4:2:2 is supported (native 4:2:2 mode (*DSC v1.2* or higher)). 11 = RESERVED.	
		4	**YCbCr 4:2:0 Support** 0 = YCbCr 4:2:0 is not supported. 1 = YCbCr 4:2:0 is supported (native 4:2:0 mode (*DSC v1.2* or higher)).	
		7:5	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Ah	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
0006Ah	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC COLOR DEPTH CAPABILITIES			
		0	**RESERVED**	Read 0
		1	**8 Bits per Color Support** A DP DSC Sink device must support 8bpc. 0 = 8bpc is not supported. 1 = 8bpc is supported.	Read Only
		2	**10 Bits per Color Support** 0 = 10bpc is not supported. 1 = 10bpc is supported.	
		3	**12 Bits per Color Support** 0 = 12bpc is not supported. 1 = 12bpc is supported.	
		4	**RESERVED**	Read 0
		5	**16 Bits per Color Support** 0 = 16bpc is not supported. 1 = 16bpc is supported.	Read Only
		7:6	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Bh	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
0006Bh	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	Peak DSC Throughput (DSC Sink)			
		3:0	**Throughput Mode 0** Decoding of three pixels per clock in units of megapixels per second. 0 = Not supported. 1 = 340MP/s. 2 = 400MP/s. 3 = 450MP/s. 4 = 500MP/s. 5 = 550MP/s. 6 = 600MP/s. 7 = 650MP/s. 8 = 700MP/s. 9 = 750MP/s. 10 = 800MP/s. 11 = 850MP/s. 12 = 900MP/s. 13 = 950MP/s. 14 = 1000MP/s. 15 = RESERVED.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Bh		7:4	**Throughput Mode 1** Decoding of six pixels per clock in units of megapixels per second (used in native 4:2:0 mode (*DSC v1.2* or higher)). 0 = Not supported. 1 = 340MP/s. 2 = 400MP/s. 3 = 450MP/s. 4 = 500MP/s. 5 = 550MP/s. 6 = 600MP/s. 7 = 650MP/s. 8 = 700MP/s. 9 = 750MP/s. 10 = 800MP/s. 11 = 850MP/s. 12 = 900MP/s. 13 = 950MP/s. 14 = 1000MP/s. 15 = RESERVED.	Read Only
0006Ch	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			
0006Ch	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC Maximum Slice Width			
		7:0	**DSC Max Slice Width** MaxSliceWidth = Number of pixels × 320. The minimum number allowed is 8 (2560 pixels). 8h = 2560 pixels	
0006Dh through 0006Fh	**For DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***			
	eDP Compression-related Functions See *eDP v1.4*.			

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
0006Dh	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	DSC SLICE CAPABILITIES 2 Used in combination with the DSC SLICE CAPABILITIES 1 register (DPCD Address 00064h) to indicate the number of slices per Display Line supported, per display. Each slice per Display Line must be supported in all resolutions that a DP DSC Sink device supports, as long as the slice width and decoder throughput requirements are not exceeded. 0 = Number of Slices per Display Line is not supported. 1 = Number of Slices per Display Line is supported.			
		0	**16 Slices per Display Line**	
		1	**20 Slices per Display Line**	
		2	**24 Slices per Display Line**	
		7:3	**RESERVED**	Read all 0s
0006Eh and 0006Fh	**For DPCD r1.4 when used with *DP v1.4* (and higher)**			Read Only
	MINIMUM *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR Indicates the minimum ***bits_per_pixel*** that the DP DSC Sink device may support. The format is U6.4 (unsigned, four fractional bits). ***Note:*** *Maximum **bits_per_pixel** is indicated by the MINIMUM bits_per_pixel SUPPORTED BY THE DECOMPRESSOR register (DPCD Addresses 00067h and 00068h).*			
	0	7:0	***bits_per_pixel*7:0** Contains the least significant eight bits of the minimum ***bits_per_pixel*** that the DP DSC Sink device may support.	
	1	1:0	***bits_per_pixel*9:8** Contains the most significant two bits of the minimum ***bits_per_pixel*** that the DP DSC Sink device may support.	
	1	3:2	**RESERVED**	Read all 0s
	1	6:4	**INCREMENT OF *bits_per_pixel* SUPPORTED BY THE DECOMPRESSOR** Incremental values between the MINIMUM and MAXIMUM ***bits_per_pixel*** that the DP DSC Sink device may support. 000 = 1/16bpp. 001 = 1/8bpp. 010 = 1/4bpp. 011 = 1/2bpp. 100 = Integer values only for bits per pixel. All other values are RESERVED.	Read Only
	1	7	**RESERVED**	Read 0

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00070h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**			
	PANEL SELF REFRESH CAPABILITY SUPPORTED AND VERSION See *eDP v1.4*.			
00071h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**			
	PANEL SELF REFRESH CAPABILITIES See *eDP v1.4*.			
00072h through 0007Fh	**RESERVED**			Read all 0s
00080h through 0008Fh	**Detailed Capabilities Info** 4-byte field, 1 byte per port type. DETAILED_CAP_INFO_AVAILABLE **bit in the** DOWN_STREAM_PORT_PRESENT **register (DPCD Address 00005h, bit 4) = 0**			Read Only
	0	**DFPX_CAP** 1 byte per DFP. x = DFP number. The Port_x capability is stored at address of the DFP number plus 80h.		
		2:0	**DFPX_TYPE** 000 = DisplayPort. 001 = Analog VGA. 010 = DVI. 011 = HDMI. 100 = Others without EDID support. 110 = Wireless. 111 = RESERVED.	
		3	**DFPX_HPD** 0 = DFP is not HPD-aware. 1 = DFP is HPD-aware.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	0	7:4	**NON_EDID_DFPX_ATTRIBUTE** **(Bits 2:0 = 100 above)** 0001 = 720x480 interlaced, 60Hz. 0010 = 720x480 interlaced, 50Hz. 0011 = 1920x1080 interlaced, 60Hz. 0100 = 1920x1080 interlaced, 50Hz. 0101 = 1280x720 progressive, 60Hz. 0111 = 1280x720 progressive, 50Hz. All other values are RESERVED. ***Notes:*** *1 A Source device may detect the interface type of the Sink device by reading the Video Input Definition byte of EDID.* *2 Some interfaces may not have a built-in HPD support, but a Branch device may have its own HPD method. In that case, Bit 3 must be set to 1. For example, A Branch device with analog VGA DFP may periodically read EDID for the purpose of detecting an analog VGA Sink. HPD support on the DFPs is recommended. For example, Windows Logo Program Device Requirements Version 3.01 requires HPD support on all digital display interfaces and strongly recommends it even for analog display interfaces.*	Read Only

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) = 1** DPCD Address 00080h (Byte 0) through 00083h (Byte 3) for DFP0 DPCD Address 00084h (Byte 0) through 00087h (Byte 3) for DFP1 DPCD Address 00088h (Byte 0) through 0008Bh (Byte 3) for DFP2 DPCD Address 0008Ch (Byte 0) through 0008Fh (Byte 3) for DFP3 ***Note:*** *A DP upstream device must read the capability from DPCD Addresses 00080h through 00083h. A DP Branch device with multiple DFPs must report the detailed capability information of the lowest DFP number to which a downstream device is connected, consistent with the EDID access routing policy of an SST-only DP Branch device as described in Section 2.1.4.1.*			Read Only
	0	**DFPX_CAP** (x = DFP number. The Port_x capability is stored at address of the DFP number plus 80h.)		
		2:0	**DFP*X*_TYPE** 000 = DisplayPort. 001 = Analog VGA. 010 = DVI. 011 = HDMI. 100 = Others without EDID support. 101 = DP++. 110 = Wireless. 111 = RESERVED.	
		3	**DFPX_HPD** 0 = DFP is not HPD-aware. 1 = DFP is HPD-aware.	
		7:4	**NON_EDID_DFPX_ATTR** **(Bits 2:0 = 100 above)** 0001 = 720x480 interlaced, 60Hz. 0010 = 720x480 interlaced, 50Hz. 0011 = 1920x1080 interlaced, 60Hz. 0100 = 1920x1080 interlaced, 50Hz. 0101 = 1280x720 progressive, 60Hz. 0111 = 1280x720 progressive, 50Hz. All other values are RESERVED.	

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For DP DFP**			Read all 0s
	3:1	**RESERVED**		
	For Analog VGA DFP			Read Only
	1	7:0	**Maximum Pixel Rate** Maximum pixel rate in MP/s, divided by 8.	
	2	1:0	**Maximum Bits per Component** 00 = 8bpc supported 01 = 10bpc supported 10 = 12bpc supported 11 = 16bpc supported ***Note:*** *The DisplayPort input bits per component equal to or smaller than the maximum bits per component must be supported by the Analog VGA DAC.*	Read Only
		7:2	**RESERVED**	Read all 0s
	3	7:0	**RESERVED**	Read all 0s
	For DVI DFP			Read Only
	1	7:0	**Maximum TMDS Character Clock Rate** Maximum TMDS character clock rate supported in Mbps divided by 2.5 (e.g., 66 (0x42) for 165MHz, 90 (0x5a) for 225MHz). ***Note:*** *A TMDS clock rate in excess of 165MHz on a DVI link is only supported for a Dual-Link DVI port.*	
	2	1:0	**Maximum Bits per Component** 00 = 8bpc supported. 01 = 10bpc supported. 10 = 12bpc supported. 11 = 16bpc supported.	
		7:2	**RESERVED**	Read all 0s
	3	0	**RESERVED**	Read all 0s
		1	**DUAL_LINK** 0 = Single Link DVI output. 1 = Dual Link DVI output high pixel clock (assumed transition point of 165MHz).	Read Only
		2	**HIGH_COLOR_DEPTH** 0 = DVI High Color Depth not supported. 1 = DVI High Color Depth supported (only meaningful when Byte 2 is non-zero).	
		7:3	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For HDMI DFP**			Read Only
	1	7:0	**Maximum TMDS Character Clock Rate** Maximum TMDS character clock rate supported in Mbps divided by 2.5. For example, a value of F0h (= 240 decimal) is placed in this register for a TMDS character clock rate of 600MHz.	
	2	1:0	**Maximum Bits per Component** 00 = 8bpc is supported. 01 = 10bpc is supported. 10 = 12bpc is supported. 11 = 16bpc is supported.	
		7:2	**RESERVED**	Read all 0s
	3	0	**FRAME_SEQ_TO_FRAME_PACK** 0 = Conversion from 3D Frame Sequential to Frame Pack is not supported. 1 = Conversion from 3D Frame Sequential to Frame Pack is supported.	Read Only
		1	**YCBCR422_PASS_THROUGH_SUPPORT** 0 = Not supported 1 = Supported	
		2	**YCBCR420_PASS_THROUGH_SUPPORT** 0 = Not supported 1 = Supported	
		3	**CONVERSION_FROM_YCBCR444_TO_YCBCR422_SUPPORT** 0 = Not supported 1 = Supported	
		4	**CONVERSION_FROM_YCBCR444_TO_YCBCR420_SUPPORT** 0 = Not supported 1 = Supported	
		7:5	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For DP++ DFP**			Read Only
	1	7:0	**Maximum TMDS Character Clock Rate** Maximum TMDS character clock rate supported in Mbps divided by 2.5	
	2	1:0	**Maximum Bits per Component** 00 = 8bpc supported. 01 = 10bpc supported. 10 = 12bpc supported. 11 = 16bpc supported.	
		7:2	**RESERVED**	Read all 0s
	3	0	**FRAME_SEQ_TO_FRAME_PACK** 0 = Conversion from 3D Frame Sequential to Frame Pack is not supported. 1 = Conversion from 3D Frame Sequential to Frame Pack is supported.	Read Only
		7:2	**RESERVED**	Read all 0s

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Table 2-155: Address Mapping within DPCD Receiver Capability Field (DPCD Addresses 00000h through 000FFh) (Continued)

DPCD Address	Register			Read/Write over AUX CH
	Byte #	Bit #	Definition within Receiver Capability Field	
00080h through 0008Fh	**For Wireless DFP**			Read Only
	1	**WIRELESS_CAP_BYTE**		
		3:0	**WIRELESS_TECHNOLOGY** 0000 = WiGig Display Extension All other values are RESERVED.	
		7:4	**RESERVED**	Read all 0s
	2	**WDE_TOPOLOGY** Only if WiGig Display Extension; otherwise, RESERVED.		Read Only
		1:0	**NUMBER_OF_WDE_TX_ON_DEVICE**	
		3:2	**WDE_TX_CONCURRENCY_CAP** Programmed to the number of WDE TXs that can be concurrently active.	
		7:4	**RESERVED**	Read all 0s
	3	**RESERVED**		Read all 0s
00090h	**FEC_CAPABILITY** New to *DP v1.4*.			Read Only
		0	**FEC_CAPABLE** 0 = Not capable. 1 = Capable.	
		1	**UNCORRECTED_BLOCK_ERROR_COUNT_CAPABLE** Support required for an FEC-capable DPRX. 0 = Not capable. 1 = Capable.	
		2	**CORRECTED_BLOCK_ERROR_COUNT_CAPABLE** 0 = Not capable. 1 = Capable.	
		3	**BIT_ERROR_COUNT_CAPABLE** 0 = Not capable. 1 = Capable.	
		7:4	**RESERVED**	Read all 0s
00091h through 000FFh	**RESERVED**			Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00100h		**LINK_BW_SET** Main-Link Bandwidth Setting = Value x 0.27Gbps/lane. ***Note:*** *Because the upstream device is required to set this value within the MAX_LINK_RATE register (DPCD Address 00001h), there is no power-on reset default value for this register. It is suggested to program this register to 01h because a certain PC graphics controller under basic software control (e.g., VBIOS) may choose to output 640x480 at 60Hz RGB video over a 1-lane Main-Link at RBR (1.62Gbps/lane) without setting this register and the LANE_COUNT_SET register (DPCD Address 00101h) in the event that the HPD input is not asserted at the time the basic software is loaded.* Four values are supported. All other values are RESERVED with the exception of *eDP v1.4* DPTX and MyDP DPTX. 06h = 1.62Gbps/lane 0Ah = 2.7Gbps/lane 14h = 5.4Gbps/lane 1Eh = 8.1Gbps/lane An *eDP v1.4* DPTX, upon reading DPCD r1.3 (which is applicable only for *eDP v1.4* DPRX) and a MAX_LINK_RATE register value of 00h uses the LINK_RATE_SET field in the LINK_RATE_SET and TX_GTC_CAPABILITY register (DPCD Address 00115h, bits 2:0) instead of writing to this register. (See *eDP v1.4b*.) A MyDP Source device, upon reading the MAX_LINK_RATE register of the downstream DPRX programmed to 19h (which can be the case only for a MyDP-to-Legacy or MyDP-to-DP lane count converter) can program the LINK_BW_SET register (DPCD Address 00100h) to 19h to enable 6.75Gbps/lane.	Write/Read

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00101h	**LANE_COUNT_SET** Main-Link Lane Count = Value.		Write/Read
	4:0	**LANE_COUNT_SET** Three values are supported. All other values are RESERVED. ***Note:*** *Because the upstream device is required to set this value within the MAX_LINK_RATE register (DPCD Address 00001h), there is no power-on reset default value for this field. It is suggested to program this field to 1h. (See the Note within the description for the LINK_BW_SET register (DPCD Address 00100h.)* 1h = 1 lane (Lane 0 only) 2h = 2 lanes (Lanes 0 and 1 only) 4h = 4 lanes A Source device may choose any lane count as long as it does not exceed the capability of the DPRX.	
	5	**POST_LT_ADJ_REQ_GRANTED** Must be cleared to 0 upon power-on reset or an upstream device disconnect. An upstream device with a DPTX sets this bit to 1 to grant the POST_LT_ADJ_REQ procedure by the downstream DPRX if the downstream DPRX supports POST_LT_ADJ_REQ, but does not support TPS4. If the upstream DPTX and downstream DPRX both support TPS4, TPS4 must be used instead of POST_LT_ADJ_REQ. See Section 3.5.1.2.4 for details regarding POST_LT_ADJ_REQ.	Write/Read
	6	**RESERVED**	Read 0
	7	**ENHANCED_FRAME_EN** Must be cleared to 0 upon power-on reset or an upstream device disconnect. 0 = Enhanced Framing symbol sequence is not enabled. 1 = Enhanced Framing symbol sequence for BS and SR is enabled. Applicable to SST-only mode. A DPTX must set this bit to 1 when the DPRX has the ENHANCED_FRAME_CAP bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 7) set to 1.	Write/Read

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00102h	**TRAINING_PATTERN_SET** Effect of the Bits 3:0 value is DPCD revision-dependent. Must be cleared to 00h upon power-on reset or an upstream device disconnect.		
	For DPCD r1.1 (Bits 3:0)		Write/Read
	1:0	**TRAINING_PATTERN_SELECT** Link Training Pattern Sequence selection. 00 = Training not in progress (or disabled). 01 = Link Training Pattern Sequence 1. 10 = Link Training Pattern Sequence 2. 11 = RESERVED.	
	3:2	**LINK_QUAL_PATTERN_SET** 00 = Link quality test pattern not transmitted 01 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1) 10 = Symbol Error Rate measurement pattern transmitted 11 = PRBS7 transmitted The PRBS7 bit sequence must be as follows: ----- direction ---→ 0010000011000010100 0111100100010110011101010 01 1111010000111000100100110 11 0101101111011000110100101 11 0111001100101010111111100 00 ***Note:*** *Upper left is transmitted first and lower right is transmitted last.*	
	For DPCD r1.2 and DPCD r1.3 (Bits 3:0)		Write/Read
	1:0	**TRAINING_PATTERN_SELECT** Link Training Pattern Sequence selection. 00 = Training not in progress (or disabled). 01 = Link Training Pattern Sequence 1. 10 = Link Training Pattern Sequence 2. 11 = Link Training Pattern Sequence 3.	
	3:2	**RESERVED** Replaced with per-lane control in each Lane's LINK_QUAL_PATTERN_SET fields in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 2:0).	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00102h	**For DPCD r1.4 (Bits 3:0)**		Write/Read
	3:0	**TRAINING_PATTERN_SELECT** Link Training Pattern Selection. 0000 = Training not in progress (or disabled). 0001 = Link Training Pattern Sequence 1. 0010 = Link Training Pattern Sequence 2. 0011 = Link Training Pattern Sequence 3. 0111 = Link Training Pattern Sequence 4. All other values are RESERVED.	
	4	**RECOVERED_CLOCK_OUT_EN** 0 = Recovered clock output from a test pad of DPRX is not enabled. 1 = Recovered clock output from a test pad of DPRX enabled.	
	5	**SCRAMBLING_DISABLE** 0 = DPTX scrambles data symbols before transmission. 1 = DPTX disables scrambler and transmits all symbols without scrambling.	
	7:6	**SYMBOL_ERROR_COUNT_SEL** 00 = Count Disparity and Illegal Symbol errors 01 = Count Disparity errors only 10 = Count Illegal Symbol errors only 11 = RESERVED	

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00103h	**TRAINING_LANE0_SET** Link Training Control_Lane0. Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	1:0	**VOLTAGE SWING SET** 00 = Voltage swing level 0. 01 = Voltage swing level 1. 10 = Voltage swing level 2. 11 = Voltage swing level 3.	
	2	**MAX_SWING_REACHED** The transmitter must support at least three levels of voltage swing (levels 0, 1 and 2). If only three levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 10 (level 2)), then this bit must be set to 1, and cleared in all other cases. If all four levels of voltage swing are supported (VOLTAGE SWING SET field (bits 1:0) are programmed to 11 (level 3)), then this bit must be set to 1,and cleared in all other cases.	
	4:3	**PRE-EMPHASIS_SET** 00 = Pre-emphasis level 0. 01 = Pre-emphasis level 1. 10 = Pre-emphasis level 2. 11 = Pre-emphasis level 3.	
	5	**MAX_PRE-EMPHASIS_REACHED** The transmitter must support at least three levels of pre-emphasis (levels 0, 1 and 2). Support of additional pre-emphasis level is optional. If only three levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 10 (level 2)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. If all four levels of pre-emphasis are supported (transmitter programmed PRE-EMPHASIS_SET field (bits 4:3) to 11 (level 3)), then the transmitter must set this bit to indicate to the receiver that the maximum pre-emphasis level has been reached, and clear this bit in all other cases. Support of independent pre-emphasis level control for each lane is also optional.	
	7:6	**RESERVED**	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00104h	**TRAINING_LANE1_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE0_SET register (DPCD Address 00103h), but for Lane 1.		Write/Read
00105h	**TRAINING_LANE2_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE0_SET register (DPCD Address 00103h), but for Lane 2.		Write/Read
00106h	**TRAINING_LANE3_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE0_SET register (DPCD Address 00103h), but for Lane 3.		Write/Read
00107h	**DOWNSPREAD_CTRL** Down-spreading control. Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	3:0	**RESERVED**	Read all 0s
	4	**SPREAD_AMP** Spreading amplitude. 0 = Main-Link signal is not down-spread. 1 = Main-Link signal is down-spread by equal to or less than 0.5% with a modulation frequency in the range of 30 to 33kHz.	Write/Read
	6:5	**RESERVED**	Read all 0s
	7	**MSA_TIMING_PAR_IGNORE_EN** 0 = Source device sends valid data for MSA timing parameters HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW) 1 = Source device may send invalid data for the above-mentioned MSA timing parameters. The Sink device must ignore these parameters and regenerate the incoming video stream without depending on these parameters. (This bit can be set to 1 only if the MSA_TIMING_PAR_IGNORED bit in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bit 6) is set to 1.)	Write/Read
00108h	**MAIN_LINK_CHANNEL_CODING_SET** Must be programmed to 01h upon power-on reset or an upstream device disconnect.		Write/Read
	0	**SET_ANSI 8b/10b** Selects the Main-Link channel coding specification, as specified in ANSI X3.230-1994, Clause 11.	
	7:1	**RESERVED**	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00109h	**I^2C Speed Control/Status Bit Map** Must be programmed to the default I^2C bit rate of the downstream device which is an implementation-specific choice.		Write/Read
	7:0	If the I2C Speed Control Capabilities Bit Map register (DPCD Address 0000Ch) is 00h (indicating that the DPRX does not implement a physical I^2C bus or does not support I^2C speed control), then a write to this register is ignored and a read returns 00h. Otherwise, bit values in this register are assigned to I^2C speeds. 00000001b = 1Kbps. 00000010b = 5Kbps. 00000100b = 10Kbps. 00001000b = 100Kbps. 00010000b = 400Kbps. 00100000b = 1Mbps. 01000000b = RESERVED. 10000000b = RESERVED. On read, the DPRX returns a value with exactly one bit set to indicate the speed currently in use. On write, software provides a mask to limit the speeds to be enabled. The DPRX must use the slowest enabled speed. ***Note:*** *Software can select slowest capable speed by writing 11111111b.* If the result of the mask with the speed capabilities is 00000000b, then the DPRX selects the speed to be used according to an implementation-dependent algorithm.	

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
0010Ah	**eDP_CONFIGURATION_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Read all 0s
	For non-eDP Sinks		
	7:0	**RESERVED**	
	For eDP Sinks		Write/Read
	0	**ALTERNATE_SCRAMBLER_RESET_ENABLE** See eDP v1.4.	
	1	**RESERVED** The FRAMING_CHANGE option for eDP has been deprecated.	Read all 0s
	6:2	**RESERVED**	
	7	**PANEL_SELF_TEST_ENABLE** Source sets to 1 to enable optional LCD Panel Self Test, as specified in eDP v1.4. Power-on default value = 0. Intended for use as a test mode only. Changing the value of this bit while the link is active may produce unpredictable results.	Write/Read
0010Bh	**LINK_QUAL_LANE0_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. The controls in this register supersede the controls in the TRAINING_PATTERN_SET register (DPCD Address 00102h).		Write/Read
	2:0	**LINK_QUAL_PATTERN_SET** 000 = Link quality test pattern not transmitted. 001 = D10.2 test pattern (unscrambled) transmitted (same as Link Training Pattern Sequence 1). 010 = Symbol Error Rate Measurement Pattern transmitted. 011 = PRBS7 transmitted. 100 = 80-bit custom pattern transmitted. 101 = CP2520 (HBR2 Compliance EYE pattern) transmitted. 110, 111 = RESERVED.	
	7:3	**RESERVED**	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
0010Ch		**LINK_QUAL_LANE1_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh), but for Lane 1.	Write/Read
0010Dh		**LINK_QUAL_LANE2_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh), but for Lane 2.	Write/Read
0010Eh		**LINK_QUAL_LANE3_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh), but for Lane 3.	Write/Read
0010Fh and 00110h		**RESERVED** (Deprecated Post Cursor2-related registers.)	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00111h	**MSTM_CTRL** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Takes effect only when the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1.		Write/Read
	0	**MST_EN** 0 = UFP will transmit audio/visual data in Single Stream Format. 1 = UFP will transmit audio/visual data in Multi-Stream Format. The upstream device must not change the value of this bit while transmitting Audio/Video data and the behavior of the receiving port in these circumstances is implementation-dependent. A Multi-Stream-capable Sink, when rendering a single stream, may be configured into either Single Stream transport mode or Multi-Stream transport mode. The decision of which mode to use is up to the Source Policy Maker or upstream Branch device. MST format is forwarded by the Branching Unit of a downstream device to further downstream only if the DPTX sets the UP_REQ_EN bit (bit 1) to 1 to enable Message Transactions. It is because the MST transmission must always be preceded by Message Transactions for Topology Management and Virtual Channel establishment.	
	1	**UP_REQ_EN** 0 = Prohibits the Downstream DPRX from originating/forwarding an UP_REQ message transaction. 1 = Allows the Downstream DPRX to originating/forwarding an UP_REQ message transaction. The DPTX may set this bit to 1 without setting the MST_EN bit (bit 0), to transmit in SST transport format while playing the role of Topology Manager and Source Payload Bandwidth Manager. The DPTX may set this bit only when the Downstream DPRX has its MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) set to 1. Setting this bit has no effect when the MST_CAP bit is cleared to 0. The DPTX must set this bit to 1 before initiating a down request message.	
	2	**UPSTREAM_IS_SRC** 0 = Upstream device is either a Source device predating DP Standard Ver.1.2 or a Branch device. 1 = Set to 1 by a DP Source device to indicate to the downstream device the presence of a Source device, not a Branch device.	
	7:3	**RESERVED**	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00112h	7:0	**AUDIO_DELAY[7:0]** Must be cleared to 00h upon power-on reset or an upstream device disconnect. AUDIO_DELAY is the additional delay in 1us granularity to be inserted by a Sink device. The Source must not program values that exceed the Sink device delay insertion capability reported in the AUD_DEL_INS[7:0], AUD_DEL_INS[15:8], and AUD_DEL_INS[23:16] fields in the AV_SYNC_DATA_BLOCK registers (DPCD Addresses 0002Bh through 0002Dh, respectively). Power reset default 0. Writing the audio delay value to the AUDIO_DELAY[7:0], AUDIO_DELAY[15:8], and AUDIO_DELAY[23:16] registers (DPCD Addresses 00112h through 00114h, respectively) may not have an effect when the Sink device's AV_SYNC_CAP bit in the DPRX_FEATURE_ENUMERATION_LIST register (DPCD Address 02210h, bit 2) is cleared to 0.	Write/Read
00113h	7:0	**AUDIO_DELAY[15:8]** Must be cleared to 00h upon power-on reset or an upstream device disconnect.	Write/Read
00114h	7:0	**AUDIO_DELAY[23:16]** Must be cleared to 00h upon power-on reset or an upstream device disconnect.	Write/Read
00115h	**LINK_RATE_SET and TX_GTC_CAPABILITY** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	2:0	**LINK_RATE_SET** See eDP v1.4.	
	3	**TX_GTC_CAP** 0 = DPTX does not have the GTC capability. 1 = DPTX has the GTC capability.	Write/Read
	4	**TX_GTC_SLAVE_CAP** 0 = DPTX cannot operate as a GTC Slave. 1 = DPTX can operate as a GTC Slave.	
	7:5	**RESERVED**	Read all 0s
00116h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**		
	RECEIVER ADVANCED LINK POWER MANAGEMENT CONFIGURATION See *eDP v1.4*.		
00117h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**		
	SINK DEVICE AUX_FRAME_SYNC CONFIGURATION See *eDP v1.4*.		

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00118h	**UPSTREAM_DEVICE_DP_PWR_NEED** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	0	**DP_PWR_NOT_NEEDED_BY_UPSTREAM_DEVICE** 0 = The upstream device needs DP_PWR provided by DPRX device through DP_PWR connector pin for operation. 1 = The upstream device does not need DP_PWR provided by DPRX device through DP_PWR connector pin for operation. The DPRX device with Source Detect capability may disable DP_PWR. The DPRX device must re-enable DP_PWR upon Source Detect event.	
	7:1	**RESERVED**	Read all 0s
00119h	**EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	0	**DPRX_SLEEP_WAKE_TIMEOUT_PERIOD_GRANTED** 0 = An upstream DP device has not granted the extended wake timeout period 1 = An upstream DP device has granted the wake timeout period requested by a downstream DP device at the EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST register (DPCD Address 02211h).	
	7:1	**RESERVED**	Read all 0s
0011Ah through 0011Fh	**RESERVED**		Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00120h	**FEC_CONFIGURATION** New to *DP v1.4*.		RD/WR (Cleared to 00h at power-on reset and upstream device disconnect)
	0	**FEC_READY** 0 = Not ready. A DP Source device shall set this bit to 1 and initiate Link training before start FEC encoding. 1 = Ready. A DP Source may start FEC encoding without having to reinitiate Link Training.	
	3:1	**FEC_ERROR_COUNT_SEL** 000 = FEC_ERROR_COUNT_DIS. 001 = UNCORRECTED_BLOCK_ERROR_COUNT. 010 = CORRECTED_BLOCK_ERROR_COUNT. 011 = BIT_ERROR_COUNT. All other values are RESERVED.	
	5:4	**LANE_SELECT** 00 = Lane 0. 01 = Lane 1. 10 = Lane 2. 11 = Lane 3.	
	7:6	**RESERVED**	Read all 0s
00121h through 00125h	**RESERVED** (FAUX-related registers were deprecated.)		Read all 0s
00126h through 00153h	**RESERVED**		Read all 0s
00154h	**TX_GTC_VALUE7:0** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
00155h	**TX_GTC_VALUE15:8** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
00156h	**TX_GTC_VALUE23:16** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
00157h	**TX_GTC_VALUE31:24** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00158h	**RX_GTC_VALUE_PHASE_SKEW_EN** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	0	**RX_GTC_VALUE_PHASE_SKEW_EN** 0 = DPRX resets its GTC value to the received TX_GTC_VALUE (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 registers (DPCD Addresses 00154h through 00157h, respectively)) and uses the delta between its GTC value and the received TX_GTC_VALUE to frequency adjust its GTC value. 1 = DPRX resets its GTC value to the received TX_GTC_VALUE, but does NOT use the delta between its GTC value and the received TX_GTC_VALUE to frequency adjust its GTC value; in other words, the TX_GTC_VALUE is used only for GTC value phase adjust only. Used only when the **DPTX** is the GTC Master.	
	7:1	**RESERVED**	Read all 0s
00159h	**TX_GTC_FREQ_LOCK_DONE** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	0	**TX_GTC_FREQ_LOCK_DONE** 0 = **DPTX** has not realized the GTC_FREQ_LOCK_DONE. 1 = **DPTX** has realized the GTC_FREQ_LOCK_DONE. Used only when the DPRX is the GTC Master.	
	7:1	**RESERVED**	Read all 0s
0015Ah	**TX_GTC_PHASE_SKEW_OFFSET7:0** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
0015Bh	**TX_GTC_PHASE_SKEW_OFFSET15:8** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
0015Ch through 0015Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others.**		
	AUX_FRAME_SYNC VALUE See *eDP v1.4*.		

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
00160h	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***		
	eDP Compression-related Functions See *eDP v1.4*.		
00160h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**		Read/Write
	DSC ENABLE New to *DP v1.4*.		
	0	**Decompression Enable** 0 = Decompression is not enabled. 1 = Decompression is enabled.	
	7:1	**RESERVED**	Read all 0s
00161h through 0016Fh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**		
	eDP Compression-related Functions See *eDP v1.4*.		
00170h	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**		
	PANEL SELF REFRESH ENABLE AND CONFIGURATION See *eDP v1.4*		
00171h through 0019Fh	**RESERVED**		Read all 0s
001A0h	**ADAPTOR_CTRL** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Control of Branch devices that adapt to legacy video transports. Takes effect only when the ADAPTOR_CAP register (DPCD Address 0000Fh) is programmed to 3h.		Write/Read
	0	**FORCE_LOAD_SENSE** Prompts the DP-to-Legacy Converter device to sense the presence of a legacy Sink device.	
	7:1	**RESERVED**	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
001A1h	**BRANCH_DEVICE_CTRL** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read
	0	**Hot Plug/Hot Unplug Event Notification Type** 0 = HPD Long Pulse used for upstream notification (default). 1 = IRQ_HPD used for upstream notification. The Source device must set this bit to 1 to enable the Branch device to use IRQ_HPD for upstream notification of a downstream plug/unplug event, if the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is cleared to 0. If the Branch device's UP_REQ_EN bit is set to 1, then the Plug/ Unplug Event Notification Type control bit is "don't care" (CONNECTION_STATUS_NOTIFY messages are used). HDCP-enabled devices, see HDCP Specification for additional information related to plug/unplug event handling.	
	7:1	**RESERVED**	Read all 0s
001A2h through 001BFh	**RESERVED**		Read all 0s
001C0h	**PAYLOAD_ALLOCATE_SET** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Writing 00h, 00h, and 3Fh to DPCD Addresses 001C0h, 001C1h, and 001C2h, respectively, clears the entire VC Payload ID table. The DPRX, upon this, immediately ignores the incoming VC Payloads (if any) without waiting or ACT on the Main-Link. Takes effect only when the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1.		Write/Read
	6:0	**VC Payload ID to Be Allocated** ID of 0 indicates that the time slots are unallocated.	
	7	**RESERVED**	Read 0
001C1h	**PAYLOAD_ALLOCATE_START_TIME_SLOT** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Takes effect only when the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1.		Write/Read
	5:0	**Starting Time Slot of VC Payload ID in DPCD Address 002C0h**	
	7:6	**RESERVED**	Read all 0s

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Table 2-156: Address Mapping within DPCD Link Configuration Field (DPCD Addresses 00100h through 001FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link Configuration Field	
001C2h	**PAYLOAD_ALLOCATE_TIME_SLOT_COUNT** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Takes effect only when the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1.		Write/Read
	5:0	**Time Slot Count of VC Payload ID in DPCD Address 002C0h**	
	7:6	**RESERVED**	Read all 0s
001C3h through 001FFh	**RESERVED**		Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
Note: *DPRX with DPCD Rev. 1.2 or higher must have the same Link/Sink Device Status field registers at DPCD Addresses 00200h through 00205h to the corresponding DPRX Event Status Indicator registers at DPCD Addresses 02002h through 0200Fh. Clearable/Read Only (CRO) bit is cleared in both address ranges when an upstream device clears the bit in one of the ranges.*			
00200h (and 02002h)	**SINK_COUNT** Sink device count.		Read Only
	7, 5:0	**SINK_COUNT** Total number of the Sink devices within this device and those connected to the DFPs of this device. ***Note:*** *A Branch device must add up the Rendering Function counts read from all of its DFPs. It must add one more if it has a local Rendering Function.*	
	6	**CP_READY** Set to 1 when all of the Sink devices (local Sink device and those connected to its DFPs) are CP-capable. This bit is set at the conclusion of Content Protection Authentication as, and if, required by the appropriate Content Protection specification. ***Notes:*** *The Source device transmits content that requires content protection only when all the Branch and Sink devices in the link are CP-ready except for Repeater devices. (A Repeater device is not required to perform a decryption/encryption operation, and therefore is not required to be CP-ready.)* *HDCP Version 1.3 Amendment for DisplayPort does not use this bit.*	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00201h (and 02003h)	**DEVICE_SERVICE_IRQ_VECTOR**		Write 1 to Clear/Read The Sink clears each bit when the Source writes 1 to the specific bit position via an AUX CH write transaction. The Source may write 1 in multiple bit positions in a single transaction.
	0	**RESERVED (FOR FUTURE)** **REMOTE_CONTROL_COMMAND_PENDING** For DP devices that support Sideband MSG handling (MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1), a Sink Event (e.g., a remote control command pending) must be handled as a message transaction.	
	Bit 1 definition is DPCD revision-dependent. **For DPCD r1.0 through DPCD r1.2 and DPCD r1.4 (Bit 1)**		
	1	**AUTOMATED_TEST_REQUEST** 1 = Source device must read DPCD Addresses 00218h through 002BFh for the requested link test.	
	For DPCD r1.3 (Bit 1, applicable to *eDP v1.4* DPRX only)		
	1	**TOUCH_INTERRUPT** See *eDP v1.4*.	
	Definitions of Bits 7:2 are not DPCD revision-dependent		Write 1 to Clear/Read The Sink clears each bit when the Source writes 1 to the specific bit position via an AUX CH write transaction. The Source may write 1 in multiple bit positions in a single transaction.
	2	**CP_IRQ** This bit is used by an optional content protection system.	
	3	**MCCS_IRQ** This bit is used by an optional MCCS system in the Sink device.	
	4	**DOWN_REP_MSG_RDY** 1 = Source device must read the DOWN_REP_MSG from the DOWN_REP_MSG DPCD locations and process the Sideband MSG.	
	5	**UP_REQ_MSG_RDY** 1 = Source device must read the UP_REQ_MSG from the UP_REQ_MSG DPCD locations and process the Sideband MSG.	
	6	**SINK_SPECIFIC_IRQ** Usage is vendor-specific.	
	7	**RESERVED**	Read 0

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00202h (and 0200Ch)	**LANE0_1_STATUS** Lane 0 and Lane 1 Status.		Read Only
	0	**LANE0_CR_DONE**	
	1	**LANE0_CHANNEL_EQ_DONE**	
	2	**LANE0_SYMBOL_LOCKED**	
	3	**RESERVED**	Read 0
	4	**LANE1_CR_DONE**	Read Only
	5	**LANE1_CHANNEL_EQ_DONE**	
	6	**LANE1_SYMBOL_LOCKED**	
	7	**RESERVED**	Read 0
00203h (and 0200Dh)	**LANE2_3_STATUS** Bit definition is identical to that of the LANE0_1_STATUS register (DPCD Address 00202h), but for Lanes 2 and 3.		Read Only
00204h (and 0200Eh)	**LANE_ALIGN__STATUS_UPDATED**		Read Only
	0	**INTERLANE_ALIGN_DONE**	
	1	**POST_LT_ADJ_REQ_IN_PROGRESS** 1 = DPRX is conducting POST_LT_ADJ_REQ. Valid only for a DPRX that sets the POST_LT_ADJ_REQ_SUPPORTED bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 5) is set and after a DPTX grants the procedure by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5).	
	5:2	**RESERVED**	Read all 0s
	6	**DOWNSTREAM_PORT_STATUS_CHANGED** Set in a Branch device when it detects a change in the connection status of any of its DFPs.	Read Only
	7	**LINK_STATUS_UPDATED** Link Status and Adjust Request updated since the last read. Set when updated and cleared after read.	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00205h (and 0200Fh)	**SINK_STATUS** The Sink device must set bits 1:0 as soon as it determines that the corresponding received stream is properly re-generated and within the supported stream format range. The Sink device must clear bits 1:0 as soon as it determines that the corresponding received stream is no longer being properly re-generated or within the supported stream format range.		Read Only
	0	**RECEIVE_PORT_0_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
	1	**RECEIVE_PORT_1_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
	7:2	**RESERVED**	Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00206h	**ADJUST_REQUEST_LANE0_1** Voltage Swing and Equalization Setting Adjust Request for Lanes 0 and 1. When this register is read and found to have changed from a previous read, both during Link Training (including the POST_LT_ADJ_REQ phase) and automated PHY Layer testing, the DPTX shall write the voltage swing and pre-emphasis level requested by this register to the TRAINING_LANE*x*_SET register(s) (DPCD Address(es) 00103h through 00106h).		Read Only
	1:0	**VOLTAGE_SWING_LANE0** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3	
	3:2	**PRE-EMPHASIS_LANE0** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3	
	5:4	**VOLTAGE_SWING_LANE1** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3	
	7:6	**PRE-EMPHASIS_LANE1** 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3	
00207h	**ADJUST_REQUEST_LANE2_3** Bit definition is identical to that of the ADJUST_REQUEST_LANE0_1 register (DPCD Address 00206h), but for Lanes 2 and 3.		Read Only
00208h	**TRAINING_SCORE_LANE0** Usage is Sink device implementation-specific.		Read Only
00209h	**TRAINING_SCORE_LANE1** Usage is Sink device implementation-specific.		Read Only
0020Ah	**TRAINING_SCORE_LANE2** Usage is Sink device implementation-specific.		Read Only

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
0020Bh	**TRAINING_SCORE_LANE3** Usage is Sink device implementation-specific.		Read Only
0020Ch	**RESERVED** (Deprecated Post Cursor2-related register.)		Read all 0s
0020Dh and 0020Eh	**RESERVED** (Deprecated FAUX-related register.)		Read all 0s
0020Fh and 0200Dh	**For eDP Compression-related Function for DPCD r1.3 (*eDP v1.4* DPRX); RESERVED for DPCD r1.2 (and lower); RESERVED for DPCD r1.4 when used with *DP v1.3***		
	DSC STATUS See *eDP v1.4*.		
0020Fh and 02011h	**For DPCD r1.4 when used with *DP v1.4* (and higher)**		Read/Write
	DSC STATUS New to *DP v1.4*.		
	0	**RC Buffer Under-run** 0 = No error. 1 = Buffer under-run. Sticky until cleared by a write of 1.	
	1	**RC Buffer Overflow** 0 = No error. 1 = Buffer overflow. Sticky until cleared by a write of 1.	
	2	**Chunk Length Error** 0 = No error. 1 = Chunk Length error. Sticky until cleared by a write of 1.	
	7:3	**RESERVED**	Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00210h and 00211h		**SYMBOL_ERROR_COUNT_LANE0** 15-bit value storing the symbol error count of Lane 0: • DPCD Address 00210h, bits 7:0 = Error Count Bits 7:0 • DPCD Address 00211h, bits 6:0 = Error Count Bits 14:8 DPCD Address 00211h, bit 7 = Error count valid. • Set to 1 when the error count value is valid For Symbol Error Rate Measurement (repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols For PRBS7 pattern: • Measures the number of mismatched bits For CP2520 (HBR2 Compliance EYE pattern; repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols When no test pattern is being transmitted (normal operation): • Measures the number of illegal symbols or disparity errors as controlled by the SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) The 15-bit value is cleared upon an AUX CH read by the transmitter. When the symbol error count exceeds 2^{15} - 1(= 32,767), the value must be kept at 2^{15} - 1, instead of wrapping around.	Read Only

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00212h and 00213h		**SYMBOL_ERROR_COUNT_LANE1** 15-bit value storing the symbol error count of Lane 1: • DPCD Address 00212h, bits 7:0 = Error Count Bits 7:0 • DPCD Address 00213h, bits 6:0 = Error Count Bits 14:8 DPCD Address 00213h, bit 7 = Error count valid. • Set to 1 when the error count value is valid For Symbol Error Rate Measurement (repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols For PRBS7 pattern: • Measures the number of mismatched bits For CP2520 (HBR2 Compliance EYE pattern; repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols When no test pattern is being transmitted (normal operation): • Measures the number of illegal symbols or disparity errors as controlled by the SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) The 15-bit value is cleared upon an AUX CH read by a transmitter When the symbol error count exceeds 2^{15} - 1 (= 32,767), the value must be kept at 2^{15} - 1, instead of wrapping around.	Read Only

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00214h and 00215h		**SYMBOL_ERROR_COUNT_LANE2** 15-bit value storing the symbol error count of Lane 2: • DPCD Address 00214h, bits 7:0 = Error Count Bits 7:0 • DPCD Address 00215h, bits 6:0 = Error Count Bits 14:8 DPCD Address 00215h, bit 7 = Error count valid. • Set to 1 when the error count value is valid. For Symbol Error Rate Measurement (repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols For PRBS7 pattern: • Measures the number of mismatched bits For CP2520 (HBR2 Compliance EYE pattern; repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols When no test pattern is being transmitted (normal operation): • Measures the number of illegal symbols or disparity errors as controlled by the SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) The 15-bit value is cleared upon an AUX CH read by a transmitter. When the symbol error count exceeds 2^{15} - 1 (= 32,767), the value must be kept at 2^{15} - 1, instead of wrapping around.	Read Only

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00216h and 00217h		**SYMBOL_ERROR_COUNT_LANE3** 15-bit value storing the symbol error count of Lane 3: • DPCD Address 00216h, bits 7:0= Error Count Bits 7:0 • DPCD Address 00217h, bits 6:0 = Error Count Bits 14:8 DPCD Address 00217h = Error count valid. • Set to 1 when the error count value is valid For Symbol Error Rate Measurement (repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols For PRBS7 pattern: • Measures the number of mismatched bits For CP2520 (HBR2 Compliance EYE pattern; repetition of scrambled 00h before ANSI 8b/10b encoding): • Measures the number of mismatched symbols When no test pattern is being transmitted (normal operation): • Measures the number of illegal symbols or disparity errors as controlled by the SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) The 15-bit value is cleared upon an AUX CH read by a transmitter. When the symbol error count exceeds 2^{15} - 1 (= 32,767), the value must be kept at 2^{15} - 1, instead of wrapping around.	Read Only

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
Note: *DPCD Addresses 00218h through 002BFh comprise the Automated Testing sub-field. Use of this sub-field is optional; however, support is recommended, because the automation facilitates a test process.*			
00218h	**TEST_REQUEST** Test requested by the Sink device. All other values are RESERVED.		Read Only
	0	**TEST_LINK_TRAINING** 0 = No link training test is requested. 1 = Link training test is requested. See the TEST_LINK_RATE register (DPCD Address 00219h) and the TEST_LANE_COUNT field in the TEST_LANE_COUNT register (DPCD Address 00220h, bits 4:0) for link rate and link width requested, respectively.	
	1	**TEST_PATTERN** 0 = No test pattern is requested. 1 = Test pattern is requested.	
	2	**TEST_EDID_READ** 0 = No EDID read test is requested. 1 = EDID read test is requested. Checksum of the last EDID block read is written to the TEST_EDID_CHECKSUM register (DPCD Address 00249h). The source will also send a color square test pattern.	
	3	**PHY_TEST_PATTERN** 1 = Requests the PHY test pattern as specified in the PHY_TEST_PATTERN register (DPCD Address 00248h).	
	7:4	**RESERVED** (Bit 4 is a deprecated FAUX-related bit.)	Read all 0s
00219h	**TEST_LINK_RATE**		Read Only
	7:0	**TEST_LINK_RATE** 06h = 1.62Gbps/lane 0Ah = 2.7Gbps/lane 14h = 5.4Gbps/lane 1Eh = 8.1Gbps/lane Use of other link rate values for testing are implementation-specific.	
0021Ah through 0021Fh	**RESERVED**		Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00220h	**TEST_LANE_COUNT**		Read Only
	4:0	**TEST_LANE_COUNT** 01h = One lane 02h = Two lanes 04h = Four lanes All other values are RESERVED.	
	7:5	**RESERVED**	Read all 0s
00221h	**TEST_PATTERN** Test pattern requested by the Sink device. 00h = No test pattern transmitted 01h = Color ramps 02h = Black and white vertical lines 03h = Color square All other values are RESERVED.		Read Only
00222h and 00223h	**TEST_H_TOTAL** Horizontal total of transmitted video stream, in pixel count.		Read Only
	00222h 7:0	**TEST_H_TOTAL Bits 15:8**	
	00223h 7:0	**TEST_H_TOTAL Bits 7:0**	
00224h and 00225h	**TEST_V_TOTAL** Vertical total of transmitted video stream, in line count.		Read Only
	00224h 7:0	**TEST_V_TOTAL Bits 15:8**	
	00225h 7:0	**TEST_V_TOTAL Bits 7:0**	
00226h and 00227h	**TEST_H_START** Horizontal active start from Hsync start, in pixel count.		Read Only
	00226h 7:0	**TEST_H_START Bits 15:8**	
	00227h 7:0	**TEST_H_START Bits 7:0**	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00228h and 00229h	**TEST_V_START** Vertical active start from Vsync start, in line count.		Read Only
	00228h 7:0	**TEST_V_START Bits 15:8**	
	00229h 7:0	**TEST_V_START Bits 7:0**	
0022Ah and 0022Bh	**TEST_HSYNC** Hsync polarity and width, in pixel count.		Read Only
	0022Ah 7	**TEST_HSYNC_POLARITY**	
	0022Ah 6:0	**TEST_HSYNC_WIDTH Bits 14:8**	
	0022Bh 7:0	**TEST_HSYNC_WIDTH Bits 7:0**	
0022Ch and 0022Dh	**TEST_VSYNC** Vsync polarity and width, in line count.		Read Only
	0022Ch 7	**TEST_VSYNC_POLARITY**	
	0022Ch 6:0	**TEST_VSYNC_WIDTH Bits 14:8**	
	0022Dh 7:0	**TEST_VSYNC_WIDTH Bits 7:0**	
0022Eh and 0022Fh	**TEST_H_WIDTH** Horizontal active video width, in pixel count (e.g., 400h = 1024 active).		Read Only
	0022Eh 7:0	**TEST_H_WIDTH Bits 15:8**	
	0022Fh 7:0	**TEST_H_WIDTH Bits 7:0**	
00230h and 00231h	**TEST_V_HEIGHT** Vertical active video height, in line count (e.g., 300h = 768 active).		Read Only
	00230h 7:0	**TEST_V_HEIGHT Bits 15:8**	
	00231h 7:0	**TEST_V_HEIGHT Bits 7:0**	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00232h and 00233h	**TEST_MISC** ***Note:*** *DPCD Address 00232h, bits 7:0, are the same definition as the MISC0 field in the Main Stream Attribute data. (See Table 2-94.)*		Read Only
	00232h 0	**TEST_SYNCHRONOUS_CLOCK** 0 = Link clock and stream clock are asynchronous. 1 = Link clock and stream clock are synchronous.	
	00232h 2:1	**TEST_COLOR_FORMAT** 00 = RGB. 01 = YCbCr 4:2:2. 10 = YCbCr 4:4:4. 11 = RESERVED.	
	00232h 3	**TEST_DYNAMIC_RANGE** 0 = VESA range (from 0 to the maximum). 1 = CEA range (as defined in *CEA-861-F*, *Section 5*).	
	00232h 4	**TEST_YCBCR_COEFFICIENTS** 0 = ITU601. 1 = ITU709.	
	00232h 7:5	**TEST_BIT_DEPTH** Bits per component. 000 = 6 bits. 001 = 8 bits. 010 = 10 bits. 011 = 12 bits. 100 = 16 bits. All other values are RESERVED.	
	00233h 0	**TEST_REFRESH_DENOMINATOR** 0 = 1 1 = 1.001	
	00233h 1	**TEST_INTERLACED** 0 = Non-interlaced 1 = Interlaced	
	00233h 7:2	**RESERVED**	Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00234h	**TEST_REFRESH_RATE_NUMERATOR** Indicates the refresh rate requested by the Sink device (e.g. 60 = 60Hz numerator). Refresh rate = TEST_REFRESH_RATE_NUMERATOR / TEST_REFRESH_DENOMINATOR. (See TEST_REFRESH_DENOMINATOR bit in the TEST_MISC register (DPCD Address 00233h, bit 0).)		Read Only
00235h through 0023Fh	**RESERVED** For test automation extensions.		Read all 0s
00240h and 00241h	**TEST_CRC_R_Cr** Stores the 16-bit CRC value of the R or Cr component. ***Note:*** *This field is also used for CRC reporting as part of the Panel Self Refresh (PSR) specification defined in eDP Standard (version 1.3 and above).*		Read Only
	00240h 7:0	**CRC Value Bits 7:0**	
	00241h 7:0	**CRC Value Bits 15:8**	
00242h and 00243h	**TEST_CRC_G_Y** Stores the 16-bit CRC value of the G or Y component. ***Note:*** *This field is also used for CRC reporting as part of the PSR specification defined in eDP Standard (version 1.3 and above).*		Read Only
	00242h 7:0	**CRC Value Bits 7:0**	
	00243h 7:0	**CRC Value Bits 15:8**	
00244h and 00245h	**TEST_CRC_B_Cb** Stores the 16-bit CRC value of the B or Cb component. ***Note:*** *This field is also used for CRC reporting as part of the PSR specification defined in eDP Standard (version 1.3 and above).*		Read Only
	00244h 7:0	**CRC Value Bits 7:0**	
	00245h 7:0	**CRC Value Bits 15:8**	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00246h	**TEST_SINK_MISC**		Read Only
	3:0	**TEST_CRC_COUNT** 4-bit wrap counter that increments each time the TEST_CRC*x_x* registers are updated. Reset to 0 when the TEST_SINK_START bit in the TEST_SINK register (DPCD Address 00270h, bit 0) is 0.	
	4	**RESERVED**	Read 0
	5	**TEST_CRC_SUPPORTED** 0 = Sink device does not support CRC. 1 = Sink device supports CRC.	Read Only
	7:6	**RESERVED**	Read all 0s
00247h	**RESERVED** For test automation extensions.		Read all 0s
00248h	**PHY_TEST_PATTERN**		Read Only
	2:0	**PHY_TEST_PATTERN_SEL** 000 = No test pattern selected 001 = D10.2 without scrambling 010 = Symbol_Error_Measurement_Count 011 = PRBS7 100 = 80-bit custom pattern transmitted 101 = CP2520 (HBR2 Compliance EYE pattern) 110, 111 = RESERVED	
	7:3	**RESERVED** ***Note:*** *Values in the ADJUST_REQUEST_LANEx_y register(s) (DPCD Address(es) 00206h and 00207h) specify the requested voltage swing and pre-emphasis level.*	Read all 0s
00249h	**For DPCD r1.0 and r1.1**		Read all 0s
	RESERVED		
	For DPCD r1.2 (and higher)		
	RESERVED (FAUX-related register deprecated.)		

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
0024Ah and 0024Bh	**For DPCD r1.0 and r1.1**		Read all 0s
	RESERVED		
	For DPCD r1.2 (and higher)		Read Only
	HBR2_COMPLIANCE_SCRAMBLER_RESET Count of number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence (SR BF BF SR). Count includes the reset sequence. Value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence.		
	0024Ah 7:0	**HBR2_COMPLIANCE_SCRAMBLER_RESET Value Bits 7:0**	
	0024Bh 7:0	**HBR2_COMPLIANCE_SCRAMBLER_RESET Value Bits 15:8**	
0024Ch through 0024Fh	**RESERVED** For test automation extensions.		Read all 0s
00250h through 00259h	**TEST_80BIT_CUSTOM_PATTERN** Stores the 80-bit custom pattern for Source device compliance measurements (LSB sent first).		Read Only
	00250h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 7:0**	
	00251h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 15:8**	
	00252h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 23:16**	
	00253h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 31;24**	
	00254h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 39:32**	
	00255h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 47:40**	
	00256h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 55:48**	
	00257h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 63:56**	
	00258h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 71:64**	
	00259h 7:0	**TEST_80BIT_CUSTOM_PATTERN Value Bits 79:72**	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
0025Ah	**CONTINUOUS_80BIT_PATTERN_FROM DPRX_AUX_CH_CAPABILITY**		Read Only
	0	**CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_CAP** 0 = Not supported 1= Supported	
	7:1	**RESERVED**	Read all 0s
0025Bh	**CONTINUOUS_80BIT_PATTERN_FROM DPRX_AUX_CH_CTRL**		Read/Write
	0	**CONTINUOUS_80BIT_PATTERN_FROM_DPRX_AUX_CH_EN** The DPRX must clear this bit when either of the following occurs: • Duration expiration –or– • Detection of an upstream DP device disconnect 0 = Disable the continuous transmission of the 80-bit pattern programmed at the TEST_80BIT_CUSTOM_PATTERN register (DPCD Addresses 00250h and 00259h) 1 = Enable the continuous transmission of the 80-bit pattern programmed at the TEST_80BIT_CUSTOM_PATTERN register While the transmission is enabled, AUX transactions over AUX CH are unavailable.	
	2:1	**DURATION_CTRL** 00 = 15 seconds 01 = 30 seconds 10 = 60 seconds 11 = 120 seconds	
	7:3	**RESERVED**	Read all 0s
0025Ch through 0025Fh	**RESERVED** For test automation extensions.		Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00260h	**TEST_RESPONSE**		Write/Read
	0	**TEST_ACK** 0 = Writing 0 has no effect on the TEST_REQ state. 1 = Positive acknowledgement of the TEST_REQ. Clears the TEST_REQ interrupt flag and indicates to the Sink device that the Source device has started the requested test mode.	
	1	**TEST_NAK** 0 = Writing 0 has no effect on the TEST_REQ state. 1 = Negative acknowledgement of the TEST_REQ. Clears the TEST_REQ interrupt flag and indicates to the Sink device that the Source device will not start the requested test mode.	
	2	**TEST_EDID_CHECKSUM_WRITE** 0 = No EDID checksum write to the TEST_EDID_CHECKSUM register (DPCD Address 00261h). 1 = EDID checksum has been written to the TEST_EDID_CHECKSUM register.	
	7:3	**RESERVED**	Read all 0s
00261h	**TEST_EDID_CHECKSUM** In TEST_EDID mode, the checksum of the last EDID block that was read is written here.		Write/Read
00262h	**RESERVED** (FAUX-related register deprecated.)		Read all 0s
00263h through 0026Fh	**RESERVED** For test automation extensions.		Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00270h	**TEST_SINK**		Write/Read
	0	**TEST_SINK_START** 0 = Stop calculating CRC on the next frame 1 = Start calculating CRC on the next frame ***Note:*** *The CRC calculation is performed on the entire frame. A 16-bit CRC is generated per component, based on the following polynomial:* $f(x) = x^{16} + x^{15} + x^2 + 1$ *The CRC calculation is only performed on active pixels. The msb is shifted in first. For any color format that is less than 16 bits per component, the lsb is zero-padded. Appendix J contains an example implementation.*	
	3:1	**RESERVED**	Read all 0s
	5:4	**PHY_SINK_TEST_LANE_SEL** When the PHY_SINK_TEST_LANE_EN bit (bit 7) is set to 1 (i.e., only one lane is enabled for jitter tolerance tests), this field indicates which lane is enabled. 00 = Lane 0 01 = Lane 1 10 = Lane 2 11 = Lane 3	Write/Read
	6	**RESERVED**	Read 0
	7	**PHY_SINK_TEST_LANE_EN** 1 = A specific lane on the Sink device is tested for crosstalk, with other lanes receiving a "clock" pattern at approximately half the bit rate. In this mode, the receiver accumulates error counts for the enabled lane in: • SYMBOL_ERROR_COUNT_LANE0 register (DPCD Addresses 00210h and 00211h) for Lane 0 • SYMBOL_ERROR_COUNT_LANE1 register (DPCD Addresses 00212h and 00213h) for Lane 1 • SYMBOL_ERROR_COUNT_LANE2 register (DPCD Addresses 00214h and 00215h) for Lane 2 • SYMBOL_ERROR_COUNT_LANE3 register (DPCD Addresses 00216h and 00217h) for Lane 3 Sink device treatment of the other lanes is implementation-dependent.	Write/Read

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00271h	**TEST_AUDIO_MODE**		Read Only
	3:0	**TEST_AUDIO_SAMPLING_RATE** 0000 = 32kHz. 0001 = 44.1kHz. 0010 = 48kHz. 0011 = 88.2kHz. 0100 = 96kHz. 0101 = 176.4kHz. 0110 = 192kHz. All other values are RESERVED.	
	7:4	**TEST_AUDIO_CHANNEL_COUNT** 0000 = 1 Channel. 0001 = 2 Channels. 0010 = 3 Channels. 0011 = 4 Channels. 0100 = 5 Channels. 0101 = 6 Channels. 0110 = 7 Channels. 0111 = 8 Channels. All other values are RESERVED.	
00272h	**TEST_AUDIO_PATTERN_TYPE** Audio test pattern requested by the reference Sink device.		Read Only
	7:0	**TEST_AUDIO_PATTERN** 00h = Operator-defined. 01h = Sawtooth Pattern. All other values are RESERVED.	

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00273h	**TEST_AUDIO_PERIOD_CH_1** Indicates period of test pattern for Channel 1 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH1** 0000 = Unused. 0001 = 3 Samples. 0010 = 6 Samples. 0011 = 12 Samples. 0100 = 24 Samples. 0101 = 48 Samples. 0110 = 96 Samples. 0111 = 192 Samples. 1000 = 384 Samples. 1001 = 768 Samples. 1010 = 1536 Samples. All other values are RESERVED.	
	7:4	**RESERVED**	Read all 0s
00274h	**TEST_AUDIO_PERIOD_CH_2** Indicates period of test pattern for Channel 2 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH2** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 2.	
	7:4	**RESERVED**	Read all 0s
00275h	**TEST_AUDIO_PERIOD_CH_3** Indicates period of test pattern for Channel 3 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH3** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 3.	
	7:4	**RESERVED**	Read all 0s
00276h	**TEST_AUDIO_PERIOD_CH_4** Indicates period of test pattern for Channel 4 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH4** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 4.	
	7:4	**RESERVED**	Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00277h	**TEST_AUDIO_PERIOD_CH_5** Indicates period of test pattern for Channel 5 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH5** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 5.	
	7:4	**RESERVED**	Read all 0s
00278h	**TEST_AUDIO_PERIOD_CH_6** Indicates period of test pattern for Channel 6 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH6** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 6.	
	7:4	**RESERVED**	Read all 0s
00279h	**TEST_AUDIO_PERIOD_CH_7** Indicates period of test pattern for Channel 7 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH7** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 7.	
	7:4	**RESERVED**	Read all 0s
0027Ah	**TEST_AUDIO_PERIOD_CH_8** Indicates period of test pattern for Channel 8 in audio samples.		Read Only
	3:0	**TEST_AUDIO_PERIOD_CH8** Bit definition is identical to that of the TEST_AUDIO_PERIOD_CH1 field in the TEST_AUDIO_PERIOD_CH_1 register (DPCD Address 00273h, bits 3:0), but for Channel 8.	
	7:4	**RESERVED**	Read all 0s
0027Bh through 0027Fh	**RESERVED**		Read all 0s

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Table 2-157: Address Mapping within DPCD Link/Sink Device Status Field (DPCD Addresses 00200h through 002FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Status Field	
00280h	**FEC_STATUS** New to *DP v1.4*.		Clearable Read Only (Write 1 to clear the set bit)
	0	**FEC_DECODE_EN_DETECTED** 0 = Not detected. 1 = Detected.	
	1	**FEC_DECODE_DIS_DETECTED** 0 = Not detected. 1 = Detected.	
	7:2	**RESERVED**	Read all 0s
00281h	**FEC_ERROR_COUNT0** New to *DP v1.4*.		Read Only
	7:0	**FEC_ERROR_COUNT7:0** Least significant eight bits of the 15-bit error count.	
00282h	**FEC_ERROR_COUNT1** New to *DP v1.4*.		Read Only
	6:0	**FEC_ERROR_COUNT14:8** Most significant seven bits of the 15-bit error count.	
	7	**FEC_ERROR_COUNT_VALID** 0 = Not valid. 1 = Valid.	
00283h through 002BFh	**RESERVED**		Read all 0s
002C0h	**PAYLOAD_TABLE_UPDATE_STATUS**		Clearable Read Only
	0	**VC Payload ID Table Updated** 0 = Not updated since the last time that this bit was cleared. 1 = Updated, cleared to 0 when the DP Source device writes 1.	
	1	**ACT Handled** 0 = ACT is not handled since the last time that this bit was read. 1 = ACT is handled, cleared to 0 when the VC Payload ID Table Updated bit (bit 0) is set to 1.	
	7:2	**RESERVED**	Read all 0s
002C1h	**VC_PAYLOAD_ID_SLOT_1**		Read Only
002C2h	**VC_PAYLOAD_ID_SLOT_2**		Read Only
…	…		Read Only
002FFh	**VC_PAYLOAD_ID_SLOT_63**		Read Only

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Table 2-158: Address Mapping within DPCD Source Device-specific Field (DPCD Addresses 00300h through 003FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Source Device-specific Field	
00300h	**IEEE_OUI** Must be cleared to 00h upon power-on reset or an upstream device disconnect. First two hex digits. Example: For IEEE OUI 00-1B-C5, this field is cleared to 00h. Defaults to 00h before being written to by the Source device.		Write/Read (Burst write for 00300h through 0030Bh)
00301h	**IEEE_OUI** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Second two hex digits. Example: For IEEE OUI 00-1B-C5, this field is set to 1Bh. Defaults to 00h before being written to by the Source device.		Write/Read (Burst write for 00300h through 0030Bh)
00302h	**IEEE_OUI** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Third two hex digits. Example: For IEEE OUI 00-1B-C5, this field is set to C5h. Defaults to 00h before being written to by the Source device.		Write/Read (Burst write for 00300h through 0030Bh)
00303h through 00308h	**Device Identification String** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Identifies the Source device. Up to six ASCII characters, starting at DPCD Address 00303h. Remaining bytes are 00h if fewer than six characters. A Source device shall always update all six bytes (including any zero bytes) with a burst write. All bytes default to 00h before being written to by the Source device.		Write/Read (Burst write for 00300h through 0030Bh)
00309h	**Hardware Revision** Must be cleared to 00h upon power-on reset or an upstream device disconnect.		Write/Read (Burst write for 00300h through 0030Bh)
	3:0	**Hardware Minor Revision** Integer, reset to 0 when the major revision increments. Typically incremented on a minor silicon (e.g., metal mask change) or board revision. Defaults to 00h before being written to by the Source device.	
	7:4	**Hardware Major Revision** Integer, typically incremented on a major silicon or board revision.	

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Table 2-158: Address Mapping within DPCD Source Device-specific Field (DPCD Addresses 00300h through 003FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Source Device-specific Field	
0030Ah	**Firmware/Software Major Revision** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Integer, typically incremented on new functionality. Defaults to 00h before being written to by the Source device.		Write/Read (Burst write for 00300h through 0030Bh)
0030Bh	**Firmware/Software Minor Revision** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Integer, reset to 0 when the firmware/software major revision increments. Typically incremented on bug fixes. Defaults to 00h before being written to by the Source device.		Write/Read (Burst write for 00300h through 0030Bh)
0030Ch through 003FFh	**RESERVED** For Source device-specific usage, specified by the owner of the IEEE OUI written to in IEEE_OUI registers (DPCD Addresses 00300h through 00302h), and identified by the Source Identification registers (DPCD Addresses 00300h through 0030Bh). A Sink device that does not support the Source-device specified behavior specified by the owner of the IEEE OUI written to in DPCD Addresses 00300h through 00302h as being associated with the Source Identification must AUX_ACK all writes, but take no other action, and must respond to reads with an AUX_ACK and the value 00h.		Vendor-specific

Table 2-159: Address Mapping within DPCD Sink Device-specific Field (DPCD Addresses 00400h through 004FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Sink Device-specific Field	
00400h	**IEEE_OUI** First two hex digits. Example: for IEEE OUI 00-1B-C5, this field is cleared to 00h. Mandatory for Sink devices, 00h for Branch devices.		Read Only
00401h	**IEEE_OUI** Second two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to 1Bh. Mandatory for Sink devices, 00h for Branch devices.		Read Only
00402h	**IEEE_OUI** Third two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to C5h. Mandatory for Sink devices, 00h for Branch devices.		Read Only

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Table 2-159: Address Mapping within DPCD Sink Device-specific Field (DPCD Addresses 00400h through 004FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Sink Device-specific Field	
00403h through 00408h	**Device Identification String** Identifies the Sink Device. Up to six ASCII characters, starting at DPCD Address 00403h. Remaining bytes are 00h if fewer than six characters. Mandatory for Sink devices, 00h for Branch devices.		Read Only
00409h	**Hardware Revision**		Read Only
	3:0	**Hardware Minor Revision** Integer, reset to 0 when major revision increments. Typically incremented on a minor silicon (e.g., metal mask change) or board revision. Mandatory for Sink devices, 00h for Branch devices.	
	7:4	**Hardware Major Revision** Integer, typically incremented on a major silicon or board revision.	
0040Ah	**Firmware/Software Major Revision** Integer, typically incremented on new functionality. Mandatory for Sink devices, 00h for Branch devices.		Read Only
0040Bh	**Firmware/Software Minor Revision** Integer, reset to 0 when the firmware/software major revision increments. Typically incremented on bug fixes. Mandatory for Sink devices, 00h for Branch devices.		Read Only
0040Ch through 004FFh	**RESERVED** For Sink device-specific usage, specified by the owner of the IEEE OUI provided in the IEEE_OUI registers (DPCD Addresses 00400h through 00402h). Branch devices shall AUX_ACK all writes, but take no other action and shall respond to reads with an AUX_ACK and the value 00h.		Vendor-specific

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Table 2-160: Address Mapping within DPCD Branch Device-specific Field (DPCD Addresses 00500h through 005FFh)

DisplayPort Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Branch Device-specific Field	
00500h	**IEEE_OUI** First two hex digits. Example: for IEEE OUI 00-1B-C5, this field is cleared to 00h. Mandatory for Branch devices, 00h for Sink devices.		Read Only
00501h	**IEEE_OUI** Second two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to 1Bh. Mandatory for Branch devices, 00h for Sink devices.		Read Only
00502h	**IEEE_OUI** Third two hex digits. Example: for IEEE OUI 00-1B-C5, this field is set to C5h. Mandatory for Branch devices, 00h for Sink devices.		Read Only
00503h through 00508h	**Device Identification String** Identifies the Branch device. Up to six ASCII characters, starting at DPCD Address 00503h. Remaining bytes are 00h if fewer than six characters. Mandatory for Branch devices, 00h for Sink devices.		Read Only
00509h	**Hardware Revision**		Read Only
	3:0	**Hardware Minor Revision** Integer, reset to 0 when major revision increments. Typically incremented on a minor silicon (e.g., metal mask change) or board revision. Mandatory for Branch devices, 00h for Sink devices.	
	7:4	**Hardware Major Revision** Integer, typically incremented on a major silicon or board revision.	
0050Ah	**Firmware/Software Major Revision** Integer, typically incremented on new functionality. Mandatory for Branch devices, 00h for Sink devices.		Read Only
0050Bh	**Firmware/Software Minor Revision** Integer, reset to 0 when the firmware/software major revision increments. Typically incremented on bug fixes. Mandatory for Branch devices, 00h for Sink devices.		Read Only
0050Ch through 005FFh	**RESERVED** For Branch device-specific usage, specified by the owner of the IEEE OUI written to in the IEEE_OUI registers (DPCD Addresses 00500h through 00502h). Sink devices shall AUX_ACK all writes, but take no other action, and shall respond to reads with an AUX_ACK and the value 00h.		Vendor-specific

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Table 2-161: Address Mapping within DPCD Link/Sink Device Power Control Field (DPCD Addresses 00600h through 006FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Power Control Field	
00600h	**SET_POWER & SET_DP_PWR_VOLTAGE** ***Notes:*** *1 When bits 7:5 are cleared to 000 (binary), the downstream device keeps the DP_PWR voltage to the default 3.3V DP_PWR setting. Only one bit may be set at a time. Setting a bit takes effect only if the downstream device is capable of generating the requested DP_PWR supply voltage as indicated in the xV_DP_PWR_CAP bits in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bits 7:5). A downstream DP device capable of generating DP_PWR voltage higher than the default 3.3V DP_PWR setting must complete the voltage level transition within 1ms. During the transition, the DP device must not generate a voltage exceeding the voltage range of the higher of the two voltage levels between which the switching is taking place.* *2 An SST-in, SST-out Branch device must forward this value to its downstream devices.* *When set to D3 state, a Sink device may put its AUX CH circuit in a "power-saving" state. In this mode, the AUX CH circuit may only detect the presence of a differential signal input without replying to an AUX CH request transaction. Upon detecting the presence of a differential signal input, the Sink device must exit the "power-saving" state within 1ms.*		Write/Read
	2:0	**SET_POWER_STATE** Must be programmed to 001 (binary) upon power-on reset or an upstream device disconnect. 001 = Set local Sink device and all downstream Sink devices to D0 (normal operation mode). 010 = Set local Sink device and all downstream Sink devices to D3 (power-down mode). 101 = Set Main-Link for local Sink device and all downstream Sink devices to D3 (power-down mode), keep AUX block fully powered, ready to reply within a Response Timeout period of 300us. All other values are RESERVED.	
	4:3	**RESERVED**	Read all 0s

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Table 2-161: Address Mapping within DPCD Link/Sink Device Power Control Field (DPCD Addresses 00600h through 006FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Link/Sink Device Power Control Field	
00600h	5	**SET_DN_DEVICE_DP_PWR_5V** Must be cleared to 0 upon power-on reset or an upstream device disconnect. 1 = DP_PWR pin of the DP connector of the downstream device to 5V.	Write/Read
	6	**SET_DN_DEVICE_DP_PWR_12V** Must be cleared to 0 upon power-on reset or an upstream device disconnect. 1 = DP_PWR pin of the DP connector of the downstream device to 12V.	
	7	**SET_DN_DEVICE_DP_PWR_18V** Must be cleared to 0 upon power-on reset or an upstream device disconnect. 1 = DP_PWR pin of the DP connector of the downstream device to 18V.	
00601h through 006FFh	**RESERVED for DPRX and Sink Devices Power Control**		Read all 0s

Table 2-162: Address Mapping within DPCD eDP-specific Field (DPCD Addresses 00700h through 007FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within eDP-specific Field	
00700h through 007FFh	**RESERVED for eDP** See *eDP v1.4b*.		

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Table 2-163: Address Mapping within DPCD Sideband MSG Buffers Field (DPCD Addresses 01000h through 017FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Sideband MSG Buffers Field	
01000h through 011FFh	**DOWN_REQ** ***Note:*** *An MST-capable upstream device must treat these registers as write-only because some MST-capable downstream devices may reply with all 00hs when read.*		Write/Read
01200h through 013FFh	**UP_REP** ***Note:*** *An MST-capable upstream device must treat these registers as write-only because some MST-capable downstream devices may reply with all 00hs when read.*		Write/Read
01400h through 015FFh	**DOWN_REP**		Read Only
01600h through 017FFh	**UP_REQ**		Read Only

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Table 2-164: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within DPRX Event Status Indicator Field	
Note: *This field must be supported for a DP device with a DPRX that is DPCD r1.2 or higher. An MST upstream device must use this field instead of the Link/Sink Device Status field registers, starting from DPCD Address 00200h.*			
02000h through 02001h	**RESERVED**		Read all 0s
02002h	**SINK_COUNT_ESI** Sink device count; same status available in the SINK_COUNT register (DPCD Address 00200h).		Read Only
	7, 5:0	**SINK_COUNT** Total number of the Sink devices within this device and those connected to the DFPs of this device. ***Note:*** *A Branch device must add up the Rendering Function counts read from all its DFPs. It must add one more if it has a local Rendering Function.*	
	6	**CP_READY** Set to 1 when all of the Sink devices (local Sink and those connected to its DFPs) are CP-capable. This bit is set at the conclusion of Content Protection Authentication as and if required by the appropriate Content Protection specification. ***Note:*** *The Source device transmits content that requires content protection only when all Branch and Sink devices within the link are CP-ready except for Repeater devices. (A Repeater device is not required to perform decryption/encryption operations, and therefore is not required to be CP-ready.)*	

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Table 2-164: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02003h	**DEVICE_SERVICE_IRQ_VECTOR_ESI0** Same flags available in the DEVICE_SERVICE_IRQ_VECTOR register (DPCD Address 00201h).		Clearable Read Only (Bit is cleared when 1 is written via an AUX CH write transaction)
	0	**RESERVED (for FUTURE)** **REMOTE_CONTROL_COMMAND_PENDING** For DP devices that support Sideband MSG handling (MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is set to 1), a Sink Event (e.g., a remote control command pending) must be handled as a message transaction.	
	Bit 1 definition is DPCD revision-dependent. **For DPCD r1.0 through DPCD r1.2 and DPCD r1.4 (Bit 1)**		
	1	**AUTOMATED_TEST_REQUEST** 1 = Source device must read DPCD Addresses 00218h through 002BFh for the requested link test.	
	For DPCD r1.3 (Bit 1, applicable to *eDP v1.4* DPRX only)		
	1	**TOUCH_INTERRUPT** See *eDP v1.4*.	
	Definitions of Bits 7:2 are not DPCD revision-dependent		Clearable Read Only (Bit is cleared when 1 is written via an AUX CH write transaction)
	2	**CP_IRQ** This bit is used by an optional content protection system.	
	3	**MCCS_IRQ** This bit is used by an optional MCCS system within the Sink device.	
	4	**DOWN_REP_MSG_RDY** 1 = Source device must read the DOWN_REP_MSG from the DOWN_REP_MSG DPCD locations and process the Sideband MSG.	
	5	**UP_REQ_MSG_RDY** 1 = Source device must read the UP_REQ_MSG from the UP_REQ_MSG DPCD locations and process the Sideband MSG.	
	6	**SINK_SPECIFIC_IRQ** Usage is vendor-specific.	
	7	**RESERVED**	Read 0

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Table 2-164: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02004h	**DEVICE_SERVICE_IRQ_VECTOR_ESI1**		Clearable Read Only (Bit is cleared when 1 is written via an AUX write transaction)
	0	**RX_GTC_MSTR_REQ_STATUS_CHANGE** The status of RX_GTC_MSTR_REQ has changed (readable in the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0)).	
	1	**LOCK_ACQUISITION_REQUEST** 0 = DPRX is not requesting a **DPTX** to initiate lock acquisition. 1 = DPRX is requesting a **DPTX** to initiate lock acquisition.	
	2	**CEC_IRQ** 1 = CEC-Tunneling-over-AUX status changed	
	7:3	**RESERVED**	Read all 0s
02005h	**LINK_SERVICE_IRQ_VECTOR_ESI0**		Clearable Read Only (Bit is cleared when 1 is written via an AUX CH write transaction)
	0	**RX_CAP_CHANGED** 1 = Upstream device must read the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155).	
	1	**LINK_STATUS_CHANGED** 1 = Upstream device must read the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157).	
	2	**STREAM_STATUS_CHANGED** 1 = Upstream Source device must re-check the Stream Status with the QUERY_STREAM_ENCRYPTION_STATUS message. Query Stream Encryption Message is discussed in Appendix H.	
	3	**HDMI_LINK_STATUS_CHANGED** 1 = Upstream DP device must read the downstream HDMI link status registers of the DP-to-HDMI protocol converter. Downstream HDMI link quality is reported at the DOWNSTREAM_HDMI_ERROR_STATUS_CH*x* registers (DPCD Addresses 03031h through 03033h).	
	4	**CONNECTED_OFF_ENTRY_REQUESTED** 1 = A downstream DP device sets this bit to 1 and generates an IRQ_HPD pulse to request entry to the CONNECTED_OFF power state. The downstream DP device may enter the CONNECTED_OFF power state only after this bit is cleared by the upstream device writing 1 to this bit. If the upstream device does not clear this bit within 1s after IRQ_HPD generation, the downstream device that requested entry into the CONNECTED_OFF power state must clear this bit, enter the OFF power state, and then de-assert HPD output.	
	7:5	**RESERVED**	Read all 0s

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Table 2-164: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within DPRX Event Status Indicator Field	
02006h through 0200Ah	**RESERVED for eDP** Optional eDP PSR-related status registers. See *eDP v1.3* (or higher) for register definitions.		Read all 0s
0200Bh	**For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others**		
	eDP Advanced Link Power Management (ALPM)-related Functions See *eDP v1.4*.		
0200Ch	**For DPCD r1.0 through DPCD r1.2 and DPCD r1.4 (Bit 1)**		Read Only
	LANE0_1_STATUS_ESI Same status available in the LANE0_1_STATUS register (DPCD Address 00202h).		
	0	**LANE0_CR_DONE**	
	1	**LANE0_CHANNEL_EQ_DONE**	
	2	**LANE0_SYMBOL_LOCKED**	
	3	**RESERVED**	Read 0
	4	**LANE1_CR_DONE**	Read Only
	5	**LANE1_CHANNEL_EQ_DONE**	
	6	**LANE1_SYMBOL_LOCKED**	
	7	**RESERVED**	Read 0
	For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others		
	SINK DEVICE AUX_FRAME_SYNC STATUS See *eDP v1.4*.		
0200Dh	**For DPCD r1.0 through DPCD r1.2 and DPCD r1.4 (Bit 1)**		Read Only
	LANE2_3_STATUS_ESI Same status available in the LANE2_3_STATUS register (DPCD Address 00203h). Bit definition is identical to that of the LANE0_1_STATUS_ESI register, but for Lanes 2 and 3.		
	For DPCD r1.3 (*eDP v1.4* DPRX) only; RESERVED for others		
	DSC STATUS See *eDP v1.4*.		

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Table 2-164: Address Mapping within DPCD DPRX Event Status Indicator Field (DPCD Addresses 02000h through 021FFh) (Continued)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within DPRX Event Status Indicator Field	
0200Eh	**LANE_ALIGN__STATUS_UPDATED_ESI** Same status available in the LANE_ALIGN__STATUS_UPDATED register (DPCD Address 00204h).		Read Only
	0	**INTERLANE_ALIGN_DONE**	
	1	**POST_LT_ADJ_REQ_IN_PROGRESS** 1 = DPRX is conducting POST_LT_ADJ_REQ. Valid only for a DPRX that sets the POST_LT_ADJ_REQ_SUPPORTED bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 5) is set and after a DPTX grants the procedure by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5).	
	5:2	**RESERVED**	Read all 0s
	6	**DOWNSTREAM_PORT_STATUS_CHANGED** Set in a Branch device when it detects a change in the connection status of any of its DFPs.	Read Only
	7	**LINK_STATUS_UPDATED** Link Status and Adjust Request updated since the last read. Set when updated and cleared after read.	
0200Fh	**SINK_STATUS_ESI** Same status available in the SINK_STATUS register (DPCD Address 00205h). The Sink device must set bits 1:0 as soon as it determines that the corresponding received stream is properly re-generated and within the supported stream format range. The Sink device must clear bits 1:0 as soon as it determines that the corresponding received stream is no longer being properly re-generated or within the supported stream format range.		Read Only
	0	**RECEIVE_PORT_0_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
	1	**RECEIVE_PORT_1_STATUS** 0 = Sink device is out of synchronization. 1 = Sink device is in synchronization.	
	7:2	**RESERVED**	Read all 0s
02010h through 02012h	**RESERVED for eDP.**		
02013h through 021FFh	**RESERVED**		Read all 0s

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02200h	**DP1.3_DPCD_REV** DPCD data structure revision number.		Read Only
	3:0	**Minor Revision Number**	
	7:4	**Major Revision Number** 14h = DPCD r1.4. All other values are RESERVED; however, the DPTX must ensure proper operation when it sees a DPCD revision value higher than DPCD r1.4. ***Note:*** *The DPCD revision number does not necessarily match the DisplayPort version number.*	
02201h	**MAX_LINK_RATE** Maximum link rate of Main-Link lanes = Value x 0.27Gbps per lane.		Read Only
	7:0	**MAX_LINK_RATE** Only four values are supported. All other values are RESERVED except for *eDP v1.4* (DPCD r1.3 or lower) and MyDP DPRX. 06h = 1.62Gbps/lane. 0Ah = 2.7Gbps/lane. 14h = 5.4Gbps/lane. 1Eh = 8.1Gbps/lane. *eDP v1.4* DPRX (DPCD r1.3 or lower) can program the MAX_LINK_RATE register value to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. See *eDP v1.4*. A MyDP DPRX of an active MyDP converter (either MyDP-to-legacy converter or MyDP-to-DP lane-count converter) can support a value of 19h (6.75Gbps/lane). As for the MAX_LINK_RATE value requirement of an SST-only Branch device in the presence of a downstream device, see Section 2.1.4.1.	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02202h	**MAX_LANE_COUNT** Maximum number of lanes = Value.		Read Only
	4:0	**MAX_LANE_COUNT** Only three values are supported. All other values are RESERVED. 1h = One lane (Lane 0 only). 2h = Two lanes (Lanes 0 and 1 only). 4h = Four lanes (Lanes 0, 1, 2, and 3). As for the MAX_LANE_COUNT value requirement of an SST-only Branch device in the presence of a downstream device, see Section 2.1.4.1.	
	5	**POST_LT_ADJ_REQ_SUPPORTED** 0 = Post-Link Training Adjust Request is not supported. 1 = Post-Link Training Adjust Request is supported (see Section 3.5.1.2.4). POST_LT_ADJ_REQ is the third phase of Link Training. This procedure is used only if TPS4 cannot be used in the second (i.e., EQ) phase of Link Training. (TPS4 can be used only if the DPTX and DPRX both support TPS4.) An upstream device with a DPTX (Source or Branch device) aware of the procedure indicates granting of the procedure by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5). The downstream device indicates that the procedure is in-progress by setting the POST_LT_ADJ_REQ_IN_PROGRESS bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 1, respectively). This is done at the end of the second phase of Link Training when the downstream device sets Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157) register bits to indicate LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE completion.	
	6	**TPS3_SUPPORTED** Indicates Link Training Pattern Sequence 3 (TPS3) support. 0 = TPS3 is not supported. 1 = TPS3 is supported (mandatory for Downstream devices that support HBR2, optional for others).	
	7	**ENHANCED_FRAME_CAP** Applies only to Single Stream Transport Format. 0 = Enhanced Framing symbol sequence for BS and SR is not supported. 1 = Enhanced Framing symbol sequence for BS and SR is supported as described in Section 2.2.1.2. Must be set to 1.	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02203h	**MAX_DOWNSPREAD**		Read Only
	0	**MAX_DOWNSPREAD** 0 = No down spread. 1 = Up to 0.5% down-spread.	
	5:1	**RESERVED**	Read all 0s
	6	**NO_AUX_TRANSACTION_LINK_TRAINING** 0 = Requires AUX transactions to synchronize to a DPTX. 1 = Does not require AUX transactions when the link configuration is already known. A DPTX, when it activates its Main-Link, can transmit TPS1 and TPS2 (or TPS3 or TPS4) for the minimum of 500us each. The known-good drive current and pre-emphasis level (or those used in the last "full" Link Training with AUX transactions) must be used when Link Training is performed without AUX transactions. Regardless of this bit's value, a DP Sink device must send an IRQ_HPD pulse when it cannot synchronize to the incoming stream. For embedded implementations in which there is no HPD line, either the proper operation should be guaranteed by design or the Source device can periodically poll the link status.	Read Only
	7	**TPS4_SUPPORTED** Indicates Link Training Pattern Sequence 4 (TPS4) support. 0 = TPS4 is not supported. 1 = TPS4 is supported (mandatory for Downstream devices with DPCD r1.4).	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02204h	**NORP & DP_PWR_VOLTAGE_CAP** ***Note:*** *When bits 7:5 are cleared to 000 (binary), the downstream device is capable of producing the default 3.3V DP_PWR setting DP_PWR only. A downstream DP device capable of generating DP_PWR voltage higher than the default 3.3V DP_PWR setting must complete the voltage level transition within 1ms. During the transition, the DP device must not generate a voltage exceeding the voltage range of the higher of the two voltage levels between which the switching is taking place.*		Read Only
	0	**NORP: Number of Receiver Ports = Value + 1** 0 = One receiver port. 1 = Two or more receiver ports (see Note below). For SST transport format, the maximum number is two (for which this bit is set to 1), one for an uncompressed video stream and the other for its associated audio stream. The receiver can simultaneously receive up to "NORP" isochronous streams. The smallest available Receiver Port number is assigned. For example, when there is only one receiver port, the receiver port is assigned to Receiver Port 0. Receiver Port 1 shall be assigned only after Receiver Port 0 has already been assigned. ***Note:*** *An MST Sink device might have more than two receiver ports because it can have three or more stream sinks. However, an MST Sink device must program this bit according to the number of receiver ports when it is operating in SST mode. The MST Sink device is required to operate in SST mode to interoperate with an SST upstream device.* *A Topology Manager in an MST Source device must use the LINK_ADDRESS and REMOTE_DPCD message transactions to discover the number of receiver ports, rather than relying on this bit.*	
	4:1	**RESERVED**	Read all 0s
	5	**5V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +4.9 to +5.5V on the DP_PWR pin of its DP connector. 1 = Downstream device is capable of producing +4.9 to +5.5V on the DP_PWR pin of its DP connector.	Read Only
	6	**12V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +12V ±10%. 1 = Downstream device is capable of producing +12V ±10% on the DP_PWR pin of its DP connector.	
	7	**18V_DP_PWR_CAP** 0 = Downstream device is not capable of producing +18V ±10%. 1 = Downstream device is capable of producing +18V ±10% on the DP_PWR pin of its DP connector.	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02205h	**DOWN_STREAM_PORT_PRESENT**		Read Only
	0	**DFP_PRESENT** 1 = Device is a Branch device and has downstream-facing port(s) (DFP(s)).	
	2:1	**DFP_TYPE** Indicates the DFP type of DFP 0. 00 = DisplayPort. 01 = Analog VGA or analog video over DVI-I. 10 = DVI, HDMI, or DP++. 11 = Others (this DFP type might not have an EDID in the Sink device (e.g., Sink devices on composite video and Svideo ports do not have an EDID, but Sink devices on a wireless or USB interface might)). A Branch device must provide more-detailed Downstream enumeration data on all of its DFPs, including DFP 0 at DPCD Addresses 00080h through 0008Fh. ***Note:*** *Further requirements for Branch devices are provided in Section 5.3.3. Requirements for Source devices when transmitting through a Branch device are provided in Section 5.1.6.*	
	3	**FORMAT_CONVERSION** 0 = This Branch device does not have a format conversion block. 1 = This DFP has a format conversion block. ***Notes:*** *1 Applicable only to a Branch device.* *2 Topology Manager in an MST Source device must use the LINK_ADDRESS message transaction to discover the DFP capability, rather than relying on this bit.*	
	4	**DETAILED_CAP_INFO_AVAILABLE** 0 = DFP capability field is 1 byte per port, starting from DPCD Address 00080h. 1 = DFP capability field is 4 bytes per port for detailed capability description starting from DPCD Address 00080h. Detailed capability information support is mandatory.	
	7:5	**RESERVED**	Read all 0s

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02206h	**MAIN_LINK_CHANNEL_CODING**		Read Only
	0	**ANSI 8b/10b** 1 = DisplayPort receiver supports the Main-Link channel coding specification, as specified in ANSI X3.230-1994, Clause 11.	
	7:1	**RESERVED**	Read all 0s
02207h	**DOWN_STREAM_PORT_COUNT**		Read Only
	3:0	**DFP_COUNT** Value = Number of DFPs. 0h = No DFPs. Type and capability of the DFP are enumerated at DPCD Addresses 00080h through 0008Fh.	
	5:4	**RESERVED**	Read all 0s
	6	**MSA_TIMING_PAR_IGNORED** Applies to eDP and box-to-box DP. 0 = Sink device requires the MSA timing parameters HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), HSyncWidth[14:0] (HSW), VTotal[15:0], VStart[15:0], VSyncPolarity[0] (VSP), and VSyncWidth[14:0] (VSW) to be sent by the Source device for rendering the incoming video stream. 1 = Sink device is capable of rendering the incoming video stream without the above-mentioned MSA timing parameters.	Read Only
	7	**OUI Support** 0 = OUI is not supported. 1 = OUI is supported (for DPCD r1.2 and DPCD r1.4, OUI and Device Identification support is mandatory; for DPCD r1.3 (which is for *eDP v1.4* DPRX), support for OUI is an implementation-specific option). IEEE_OUI registers (DPCD Addresses 00400h through 00402h) for a Sink device, plus DPCD Addresses 00403h through 0040Bh for Device Identification. IEEE_OUI registers (DPCD Addresses 00500h through 00502h) for a Branch device, plus DPCD Addresses 00503h through 0050Bh for Device Identification.	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02208h	**RECEIVE_PORT0_CAP_0** Receiver Port 0 Capability 0. ***Note:*** *A Source device operating in MST mode does not use this register.*		Read Only
	0	**RESERVED**	Read all 0s
	1	**LOCAL_EDID_PRESENT** 0 = This receiver port does not have a local EDID. 1 = This receiver port has a local EDID. A local EDID is mandatory for Sink devices and Format Converters.	Read Only
	2	**ASSOCIATED_TO_PRECEDING_PORT** 0 = This port is used for the main isochronous stream. This bit must always be cleared to 0 for Receiver Port 0. 1 = This port is used for the secondary isochronous stream of the main stream received in the preceding port.	
	7:3	**RESERVED**	Read all 0s
02209h	**RECEIVE_PORT0_CAP_1** Receiver Port 0 Capability 1. ***Note:*** *A Source device operating in MST mode does not use this register.*		Read Only
	7:0	**BUFFER_SIZE** Buffer size = (Value + 1) * 32 bytes per lane. The maximum is 8KB per lane.	
0220Ah	**RECEIVE_PORT1_CAP_0** Receiver Port 1 Capability 0. Bit definition is identical to that of the RECEIVE_PORT0_CAP_0 register (DPCD Address 02208h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 is not present, this register is read all 0s.* *2 A Source device operating in MST mode does not use this register.*		Read Only

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
0220Bh	**RECEIVE_PORT1_CAP_1** Receiver Port 1 Capability 1. Bit definition is identical to that of the RECEIVE_PORT0_CAP_1 register (DPCD Address 02209h), but for Port 1. ***Notes:*** *1 When Receiver Port 1 not present, this register is read all 0s.* *2 A Source device operating in MST mode does not use this field.*		Read Only
0220Ch	**I^2C Speed Control Capabilities Bit Map** Bit or bits set to indicate I^2C speed control capabilities. Support for source control of the I^2C speed is optional but recommended when the DPRX implements a physical I^2C bus. If the DPRX does not implement a physical I^2C bus, this register is cleared to 00h. Otherwise, if the DPRX does not provide source control of the I^2C speed, this register is also cleared to 00h. In this case the DPRX, upon receiving an I^2C-over-AUX transaction, generates an I^2C transaction at the I^2C bit rate of its choice. Otherwise, bit values in this register are assigned to I^2C speeds. 00000001b = 1Kbps. 00000010b = 5Kbps. 00000100b = 10Kbps. 00001000b = 100Kbps. 00010000b = 400Kbps. 00100000b = 1Mbps. 01000000b = RESERVED. 10000000b = RESERVED.		Read Only

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
0220Dh	**eDP_CONFIGURATION_CAP** Always reads 00h for external receivers. Read Only for eDP RXs.		Read Only
	0	**ALTERNATE_SCRAMBLER_RESET_CAPABLE** 1 = Indicates that this is an eDP device that can use the eDP alternate scrambler reset value of FFFEh.	
	1	**RESERVED** (The FRAMING_CHANGE option for eDP has been deprecated.)	Read all 0s
	7:2	**RESERVED** for eDP.	
0220Eh	**TRAINING_AUX_RD_INTERVAL**		Read Only
	6:0	**TRAINING_AUX_RD_INTERVAL** Link Status/Adjust Request read interval during Main-Link Training. 00h = 100us for the Main-Link Clock Recovery phase and 400us for the Main-Link Channel Equalization phase. 01h = 100us for the Main-Link Clock Recovery phase; 4ms for the Main-Link Channel Equalization phase. 02h = 100us for the Main-Link Clock Recovery phase; 8ms for the Main-Link Channel Equalization phase. 03h = 100us for the Main-Link Clock Recovery phase; 12ms for the Main-Link Channel Equalization phase. 04h = 100us for the Main-Link Clock Recovery phase; 16ms for the Main-Link Channel Equalization phase. All other values are RESERVED.	
	7	**EXTENDED_RECEIVER_CAPABILITY_FIELD_PRESENT** 0 = Not present. 1 = Present at DPCD Addresses 02200h through 022FFh. A DPRX with DPCD r1.4 (or higher) must have an Extended Receiver Capability field.	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
0220Fh	**ADAPTOR_CAP** Capabilities of Branch devices that adapt to legacy video transports.		Read Only
	0	**FORCE_LOAD_SENSE_CAP** 0 = Does not support VGA force load adaptor sense mechanism. 1 = Supports VGA force load adaptor sense mechanism.	
	1	**ALTERNATE_I2C_PATTERN_CAP** 0 = Does not support alternate I^2C patterns. 1 = Supports alternate I^2C patterns.	
	7:2	**RESERVED**	Read all 0s

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02210h	**DPRX_FEATURE_ENUMERATION_LIST** Support for bits 7:4 and 1 added in *DP v1.4*.		Read Only
	0	**GTC_CAP** A DPRX indicates support for the GTC feature by setting this bit. The GTC feature is defined in Section 2.13. 0 = Not supported. 1 = Supported.	
	1	**SST_SPLIT_SDP_CAP** A DPRX indicates support for SDP splitting in SST mode by setting this bit. The SST mode SDP Splitting feature is defined in Section 2.2.5.12. 0 = Not supported. 1 = Supported.	
	2	**AV_SYNC_CAP** A DP device indicates support of the AV Sync capability through audio delay insertion by setting this bit. The AV Sync feature is defined in Section 2.12. 0 = Not supported. 1 = Supported.	
	3	**VSC_SDP_EXTENSION_FOR_COLORIMETRY_SUPPORTED** A DP Source device, upon detecting this bit being set to 1 by a DP Sink device, can set the MISC1 field, bit 6, of an MSA Packet to 1 to indicate that pixel encoding format and colorimetry format are indicated in the VSC SDP. 0 = Not supported. 1 = Supported.	
	4	**VSC_EXT_VESA_SDP_SUPPORTED** 0 = Not supported. 1 = Supported.	
	5	**VSC_EXT_VESA_SDP_CHAINING_SUPPORTED** Support of up to 64 VSC_EXT_VESA SDP chaining is required for DP Sink devices that support chaining. DP Sink devices that support more than 64 SDPs of chaining indicate the maximum chaining count beyond 64 in the VSC_EXT_VESA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_VESA_SDP_MAX_CHAINING register (DPCD Address 02212h, bits 7:0). 0 = Not supported. 1 = Supported.	

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Table 2-165: Address Mapping within DPCD Extended Receiver Capability Field (DPCD Addresses 02200h through 022FFh) (Continued)

DPCD Address	Register		Read/Write over AUX CH
	Bit #	Definition within Extended Receiver Capability Field	
02210h	6	**VSC_EXT_CEA_SDP_SUPPORTED** 0 = Not supported. 1 = Supported.	Read Only
	7	**VSC_EXT_CEA_SDP_CHAINING_SUPPORTED** 0 = Not supported. 1 = Supported. Support of up to 64 VSC_EXT_CEA SDP chaining is required for DP Sink devices that support chaining. DP Sink devices that support more than 64 SDPs of chaining indicate the maximum chaining count beyond 64 in the VSC_EXT_CEA_SDP_MAX_CHAINING_COUNT field in the VSC_EXT_CEA_SDP_MAX_CHAINING register (DPCD Address 02213h, bits 7:0).	
02211h	**EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST**		Read Only
	7:0	**DPRX_SLEEP_WAKE_TIMEOUT_PERIOD** 00h = 1ms. 01h = 20ms. 02h = 40ms. 03h = 60ms. 04h = 80ms. 05h = 100ms. All other values are RESERVED. A downstream DP device (including a DP Sink device) must request the minimum timeout duration that it is capable of supporting.	
02212h	**VSC_EXT_VESA_SDP_MAX_CHAINING** New to *DP v1.4*.		Read Only
	7:0	**VSC_EXT_VESA_SDP_MAX_CHAINING_COUNT** DP Sink device supports the maximum number of SDP chaining equal to 64 plus the value in this register.	
02213h	**VSC_EXT_CEA_SDP_MAX_CHAINING** New to *DP v1.4*.		Read Only
	7:0	**VSC_EXT_CEA_SDP_MAX_CHAINING_COUNT** DP Sink device supports the maximum number of SDP chaining equal to 64 plus the value in this register.	
02214h through 022FFh	**RESERVED for Extended Receiver Capability**		Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
The Protocol Converter Extension field, containing CEC-tunneling registers, is valid only with DPCD r1.4 (or higher).				
03000h	**CEC_TUNNELING_CAPABILITY** Consumer Electronics Channel (CEC)-Tunneling-over-AUX capability.			Read Only
		0	**CEC_TUNNELING_CAPABLE** Set to 1 by a DP-to-HDMI protocol converter capable of CEC-Tunneling-over-AUX to indicate the capability to the DP Source device. A DP-to-HDMI converter with DPCD r1.4 (or higher) must set this bit to 1. Support of CEC-Tunneling-over-AUX by a DP-to-HDMI converter paired with a DP Source device to constitute an HDMI Source device is an implementation-specific choice.	
		1	**CEC_SNOOPING_CAPABLE** Set to 1 by a DP-to-HDMI protocol converter capable of passively snooping CEC messages to indicate the capability to the DP Source device.	
		2	**CEC_MULTIPLE_LA_CAPABLE** Set to 1 by a DP-to-HDMI protocol converter capable of acting as a Follower for multiple CEC Logical Addresses to indicate the capability to the DP Source device.	
		7:3	**RESERVED**	Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03001h	**CEC_TUNNELING_CONTROL**			Read/Write
		0	**CEC_TUNNELING_ENABLE** Prompts a DP-to-HDMI protocol converter to enable CEC message reception from, and transmission to, the CEC bus. The DP-to-HDMI protocol converter does not receive CEC messages unless this bit is set to 1. The DP-to-HDMI protocol converter does ***not*** acknowledge CEC messages unless this bit is set to 1 and at least one bit is set in the CEC_LOGICAL_ADDRESS_MASK register (DPCD Addresses 0300Eh and 0300Fh). When this bit is set to 1, temporary storage for received CEC messages is reset/cleared to 0 in the CEC_RX_MESSAGE_BUFFER register (DPCD Addresses 03010h through 0301Fh). Setting this bit to 1 shall bring the CEC-Tunneling-over-AUX function of the DP-to-HDMI protocol converter to a defined initial state. The DP-to-HDMI protocol converter, upon power-on reset and an upstream DP device disconnect/connect, must clear this bit to 0. When the upstream DP device clears this bit, the DP-to-HDMI protocol converter must flush the buffer and clear the status indication flags.	
		1	**CEC_SNOOPING_ENABLE** Prompts a DP-to-HDMI protocol converter to enable passive CEC message reception from the CEC bus when bit 0 (CEC_TUNNELING_ENABLE is set to 1. Writes are ignored when CEC_SNOOPING_ENABLE is cleared to 0. 0 = Receive all directly addressed CEC messages selected by the CEC_LOGICAL_ADDRESS_MASK register (DPCD Addresses 0300Eh and 0300Fh), and all CEC Broadcast messages. 1 = Receive all CEC messages, regardless of the Destination logical address. A DP-to-HDMI protocol converter, upon power-on reset or an upstream DP device disconnect/connect, must clear this bit to 0. When the upstream DP device clears this bit, the DP-to-HDMI protocol converter must flush the buffer and clear the status indication flags. Regardless of the state of this bit, a DP-to-HDMI protocol converter shall only act as a Follower for CEC frames according to the CEC_LOGICAL_ADDRESS_MASK register. This means that the converter shall not acknowledge or report CEC Line errors for CEC frames in which the bit corresponding to the Destination address is not set in the CEC_LOGICAL_ADDRESS_MASK register.	
		7:2	**RESERVED**	Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03002h	**CEC_RX_MESSAGE_INFO** A DP-to-HDMI protocol converter, upon 1) power-on reset, 2) an upstream DP device disconnect/connect, or 3) CEC_TUNNELING_ENABLE cleared to 0, must clear this register to 00h.			Read Only
		3:0	**CEC_RX_MESSAGE_LEN** Length of the CEC frame received from the CEC bus by a DP-to-HDMI protocol converter and placed into the CEC_RX_MESSAGE_BUFFER. The DP-to-HDMI protocol converter determines this by detecting the START bit and then waiting for the end-of-message (EOM) bit or the first not acknowledged block. The actual length (in number of blocks/bytes) is equal to CEC_RX_MESSAGE_LEN value + 1.	
		4	**CEC_RX_MESSAGE_HPD_STATE** Set to 1 by a DP-to-HDMI protocol converter if the Logical HPD was asserted at the start of this message. (See Table 5-8 for the definition of Logical HPD.)	
		5	**CEC_RX_MESSAGE_HPD_LOST** Set to 1 by a DP-to-HDMI protocol converter if the Logical HPD was de-asserted since the start of the previous message, since power-on reset, or an upstream device disconnect/connect. (See Table 5-8 for the definition of Logical HPD.)	
		6	**CEC_RX_MESSAGE_ACKED** Set to 1 by a DP-to-HDMI protocol converter if the received CEC frame was acknowledged. For broadcast messages this is 1 if no device negatively acknowledged any block in the frame. For a directly addressed message this is 1 if the follower acknowledged all blocks in the frame.	
		7	**CEC_RX_MESSAGE_ENDED** Set to 1 by a DP-to-HDMI protocol converter if the last block in the received CEC frame was the final block in the CEC message.	

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03003h	**CEC_TX_MESSAGE_INFO** DP-to-HDMI protocol converter, upon 1) power-on reset, 2) an upstream DP device disconnect/connect, or 3) CEC_TUNNELING_ENABLE cleared to 0, must set this register to 00h.			Read/Write
		3:0	**CEC_TX_MESSAGE_LEN** Length of the CEC message to be transmitted by a DP-to-HDMI protocol converter on the CEC bus. Actual number of bytes is equal to CEC_TX_MESSAGE_LEN value + 1.	
		6:4	**CEC_TX_RETRY_COUNT** Number of CEC frame re-transmissions that a DP-to-HDMI protocol converter shall attempt if a directly-addressed message is not acknowledged, a broadcast message is negatively acknowledged, or a CEC Line Error is detected. Valid values are 0 through 5. All other values are RESERVED.	
		7	**CEC_TX_MESSAGE_SEND / CEC_TX MESSAGE_BUFFER_UNAVAILABLE** Set to 1 by a DP Source device after it has written a complete CEC message to the CEC TX_MESSAGE_BUFFER, to prompt a DP-to-HDMI protocol converter to transmit the message on the CEC bus after first ensuring that the bus has been inactive for the appropriate *signal free time*, as required by CEC Specification. A DP-to-HDMI protocol converter shall clear this bit to zero after it has transmitted the CEC message on the CEC bus. The DP Source must not write a new CEC TX message into the CEC_TX_MESSAGE_BUFFER until this bit is cleared to 0 by the DP-to-HDMI protocol converter.	

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03004h	**CEC_TUNNELING_IRQ_FLAGS** A DP-to-HDMI protocol converter shall assert an IRQ_HPD pulse with the CEC_IRQ bit set whenever it sets a bit in this field to 1. The DP Source device must write a 1 to a bit to acknowledge the interrupt and clear the bit. DP-to-HDMI protocol converter, upon 1) power-on reset, 2) an upstream DP device disconnect/connect, or 3) CEC_TUNNELING_ENABLE cleared to 0, must set this register to 00h.			Write 1 to Clear/Read
		0	**CEC_RX_MESSAGE_INFO_VALID** Set to 1 by a DP-to-HDMI protocol converter after it has written a received CEC message into the CEC_RX_MESSAGE_BUFFER (mapped to DPCD addresses) and updated CEC_RX_MESSAGE_INFO. The DP Source device must read the CEC message from the CEC_RX_MESSAGE_BUFFER before clearing this bit. The reason is as follows: A DP-to-HDMI converter is required to move the next CEC RX message. If the CEC RX message is present and if this bit is cleared, from its temporary buffer to CEC_RX_MESSAGE_BUFFER, do the following: 1 Set this bit. 2 Set the CEC_IRQ bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 2). 3 Generate an IRQ_HPD, regardless of whether the DP Source device has read the previously placed CEC RX message, If the DP Source device clears this bit before reading the CEC RX message in the CEC_RX_MESSAGE_BUFFER, the message may be overwritten with the next message.	
		1	**CEC_RX_MESSAGE_OVERFLOW** Set to 1 by a DP-to-HDMI protocol converter when a CEC frame is received and there is no temporary storage available to hold the message data (see CEC_RX_MESSAGE_BUFFER). The protocol converter must not receive additional CEC messages (i.e., as a Follower it must negatively acknowledge a CEC frame on the CEC bus and drop a frame while snooping) until the CEC_RX_MESSAGE_OVERFLOW bit is cleared by the DP Source device.	
		3:2	**RESERVED**	Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03004h		4	**CEC_TX_MESSAGE_SENT** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was successfully transmitted within the permitted number of retries.	Write 1 to Clear/Read
		5	**CEC_TX_LINE_ERROR** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was not successfully transmitted after the specified number of retries, due to detection of a CEC Line Error on any block in the CEC frame during the last transmission attempt.	
		6	**CEC_TX_ADDRESS_NACK_ERROR** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was not successfully transmitted after the specified number of retries, due to a negative acknowledge of the Header Block of the CEC frame during the last transmission attempt.	
		7	**CEC_TX_DATA_NACK_ERROR** Set to 1 by a DP-to-HDMI protocol converter when the CEC message in the CEC_TX_MESSAGE_BUFFER was not successfully transmitted after the specified number of retries, due to a negative acknowledge of a Data Block in the CEC frame during the last transmission attempt.	
03005h through 0300Dh	**RESERVED for Protocol Converter Extension**			Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
0300Eh and 0300Fh	**CEC_LOGICAL_ADDRESS_MASK** DP-to-HDMI protocol converter, upon 1) power-on reset, 2) an upstream DP device disconnect/connect, or 3) CEC_TUNNELING_ENABLE cleared to 0, must set these 16 bits to 8000h (to enable as a follower for a Broadcast message).			Read/Write
		14:0	**CEC_LOGICAL_ADDRESS_MASK** This field defines the set of logical addresses for which a DP-to-HDMI protocol converter shall act as a Follower, and controls message delivery for *directly addressed* messages when snooping is disabled. Broadcast messages are always delivered. A DP-to-HDMI protocol converter shall act as a Follower for a CEC message **if and only if** the CEC_LOGICAL_ADDRESS_MASK contains the Destination address of the CEC message; this includes: • Acknowledging a directly-addressed message, • Negatively acknowledging a broadcast message, • Reporting a detected CEC Line Error. Bit 0 = Logical Address 0 Bit 1 = Logical Address 1 Bit 2 = Logical Address 2 Bit 3 = Logical Address 3 Bit 4 = Logical Address 4 Bit 5 = Logical Address 5 Bit 6 = Logical Address 6 Bit 7 = Logical Address 7 Bit 8 = Logical Address 8 Bit 9 = Logical Address 9 Bit 10 = Logical Address 10 Bit 11 = Logical Address 11 Bit 12 = Logical Address 12 Bit 13 = Logical Address 13 Bit 14 = Logical Address 14 0 = Do not act as a Follower for this address. Do not deliver messages with this Destination address to the CEC_RX_MESSAGE_BUFFER unless CEC_SNOOPING_ENABLE=1. 1 = Act as a Follower for this address. Deliver messages with this Destination address to the CEC_RX_MESSAGE_BUFFER even if CEC_SNOOPING_ENABLE=0. When CEC_MULTIPLE_LA_CAPABLE=1, a DP-to-HDMI protocol converter shall accept any 16-bit value in this field.	

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
0300Eh and 0300Fh		15	**CEC_LOGICAL_ADDRESS_MASK** Logical Address 15 0 = Do not act as a Follower for Broadcast messages, and do not report CEC Line Errors detected while receiving the Header Block of a CEC frame. 1 = Act as a Follower for Broadcast messages, and report CEC Line Errors detected while receiving the Header Block of a CEC frame. When CEC_MULTIPLE_LA_CAPABLE=0, a DP-to-HDMI protocol converter shall reply with AUX_NACK if the DP Source device attempts to write a value where more than one of bits 14:0 is set to 1. It shall also reply with AUX_NACK if bit 15 is cleared to 0 (the converter always acts as a Follower for broadcast messages in this case).	Read/Write
03010h through 0301Fh	**CEC_RX_MESSAGE_BUFFER** 16-byte buffer filled by a DP-to-HDMI protocol converter when a CEC message is received and this buffer is available (either no previous message or the previous message has been read by an upstream DP device). The first byte of the buffer (= DPCD 03010h) always contains the first byte of the received CEC message. A DP-to-HDMI protocol converter shall discard messages terminated due to CEC Line Errors. When a DP-to-HDMI protocol converter receives bytes of one or more additional CEC messages while the CEC_RX_MESSAGE_INFO_VALID bit remains set to 1, it shall store those bytes into a temporary storage not mapped to DPCD addresses. The temporary storage should be large enough to hold two seconds of CEC traffic and shall at least hold one second of CEC traffic.			Read/Write
03020h through 0302Fh	**CEC_TX_MESSAGE_BUFFER** 16-byte buffer filled by a DP Source device with a CEC message to be transmitted to the CEC bus by a DP-to-HDMI protocol converter. The first byte of the buffer (= DPCD 03020h) always contains the first byte of the CEC message, which determines the Initiator and Destination address. ***Note:*** *The Initiator logical address used for message transmission shall be determined solely by the first four bits of the first byte of this buffer.*			Read/Write
03030h	**DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED**			Read Only
		0	**DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED** 0 = Not supported 1 = Supported	
		7:1	**RESERVED**	Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03031h	**DOWNSTREAM_HDMI_ERROR_STATUS_CH0** ***Note:*** *Status is asynchronously updated on a 100ms cycle and cleared upon a read by an upstream DP device.*			Read Only
		0	1 = More than three errors since the last read.	
		1	1 = More than 10 errors since the last read.	
		2	1 = More than 100 errors since the last read.	
		7:3	**RESERVED**	Read all 0s
03032h	**DOWNSTREAM_HDMI_ERROR_STATUS_CH1** ***Note:*** *Status is asynchronously updated on a 100ms cycle and cleared upon a read by an upstream DP device.*			Read Only
		0	1 = More than three errors since the last read.	
		1	1 = More than 10 errors since the last read.	
		2	1 = More than 100 errors since the last read.	
		7:3	**RESERVED**	Read all 0s
03033h	**DOWNSTREAM_HDMI_ERROR_STATUS_CH2** ***Note:*** *Status is asynchronously updated on a 100ms cycle and cleared upon a read by an upstream DP device.*			Read Only
		0	1 = More than three errors since the last read.	
		1	1 = More than 10 errors since the last read.	
		2	1 = More than 100 errors since the last read.	
		7:3	**RESERVED**	Read all 0s
03034h	**HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT** ***Note:*** *This register is valid only after an EDID read. Consequently, the Source device is unable to rely on this register until after it has completed a full EDID read of all blocks in the EDID.*			Read Only
		0	**10bpc_Supported** 0 = 10bpc is not supported. 1 = 10bpc is supported.	
		1	**12bpc_Supported** 0 = 12bpc is not supported. 1 = 12bpc is supported.	
		2	**16bpc_Supported** 0 = 16bpc is not supported. 1 = 16bpc is supported.	
		7:3	**RESERVED**	Read all 0s
03035h through 0304Fh	**RESERVED for Protocol Converter Extension**			Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03050h	**PROTOCOL_CONVERTER_CONTROL_0** Register name changed and bit 0 description expanded in *DP v1.4*.			Read/Write
		0	**HDMI_DVI_OUTPUT_CONFIG** Valid only when the DFPX_TYPE is set to HDMI, in which case this bit defaults to 1. Otherwise, this bit defaults to 0. The Source device shall clear this bit to 0 if DFPX_TYPE is set to HDMI but the Source device determines (through EDID processing) that the connected display is DVI. 0 = DVI. Protocol Converter shall not transmit HDMI INFOFRAMES and shall not use video guard bands. Protocol Converter may also suppress audio, although the Source device is not expected to transmit audio as a result of EDID processing. 1 = HDMI. Protocol Converter shall transmit HDMI INFOFRAMES, use video guard bands, and pass-through audio.	
		7:1	**RESERVED**	Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03051h	**PROTOCOL_CONVERTER_CONTROL_1** Register name changed and support for bits 3:1 added in *DP v1.4*.			Read/Write
		0	**CONVERSION_TO_YCBCR420_ENABLE** Must be cleared to 0 upon power-on reset or an upstream device disconnect. 0 = Disable. 1 = Enable.	
		1	**HDMI_EDID_PROCESSING_DISABLE** May be set by the Source device before it reads the Sink device's EDID to disable autonomous EDID processing by the Protocol Converter when the Protocol Converter snoops the EDID reads. ***Note:*** *The Protocol Converter may read and process the EDID before setting SINK_COUNT to 1, but this behavior is not preferred.* 0 = HDMI autonomous EDID processing enabled (default). 1 = HDMI autonomous EDID processing disabled. Protocol Converter shall ensure that the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h) always reads as 00h, and that scrambling is not be autonomously enabled for TMDS Character Rates is less than 340 Mcsc.	
		2	**HDMI_AUTONOMOUS_SCRAMBLING_DISABLE** 0 = HDMI autonomous scrambling is enabled (default). 1 = HDMI autonomous scrambling disabled. Scrambling of HDMI output is controlled by bit 3 (HDMI_FORCE_SCRAMBLING).	
		3	**HDMI_FORCE_SCRAMBLING** No effect unless bit 2 (HDMI_AUTONOMOUS_SCRAMBLING_DISABLE) is set to 1. 0 = HDMI scrambling is disabled (default). 1 = HDMI scrambling is enabled.	
		7:4	**RESERVED**	Read all 0s
03052h	~~**CONVERSION_FROM_YCBCR444_TO_YCBCR422_ENABLE**~~ **PROTOCOL_CONVERTER_CONTROL_2** Register name changed in *DP v1.4*.			Read/Write
		0	**CONVERSION_TO_YCBCR422_ENABLE** Must be cleared to 0 upon power-on reset or an upstream device disconnect. 0 = Disable. 1 = Enable.	
		7:1	**RESERVED**	Read all 0s

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Table 2-166: Address Mapping within DPCD Protocol Converter Extension Field (DPCD Addresses 03000h through 030FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within Protocol Converter Extension Field	
03053h	**RESERVED for Protocol Converter Extension**			Read all 0s
03054h and 03055h	**OUTPUT_HTOTAL** New to *DP v1.4*. Used for Horizontal Blanking Expansion. A DP Source device shall program these registers prior to transmitting the video stream to be expanded by a DPRX. 0000h = Default			Read/Write
	0	7:0	**OUTPUT_HTOTAL7:0** Least significant eight bits of the 16-bit OUTPUT_HTOTAL.	
	1	7:0	**OUTPUT_HTOTAL15:8** Most significant eight bits of the 16-bit OUTPUT_HTOTAL.	
03056h and 03057h	**OUTPUT_HSTART** New to *DP v1.4*. Used for Horizontal Blanking Expansion. A DP Source device shall program these registers prior to transmitting the video stream to be expanded by a DPRX. 0000h = Default			Read/Write
	0	7:0	**OUTPUT_HSTART7:0** Least significant eight bits of the 16-bit OUTPUT_HSTART.	
	1	7:0	**OUTPUT_HSTART15:8** Most significant eight bits of the 16-bit OUTPUT_HSTART.	
03058h and 03059h	**OUTPUT_HSP_HSW** New to *DP v1.4*. Used for Horizontal Blanking Expansion. A DP Source device shall program these registers prior to transmitting the video stream to be expanded by a DPRX. 0000h = Default			Read/Write
	0	7:0	**OUTPUT_HSP_HSW7:0** Least significant eight bits of the 15-bit OUTPUT_HSP_HSW.	
	1	6:0	**OUTPUT_HSP_HSW14:8** Most significant seven bits of the 15-bit OUTPUT_HSP_HSW.	
	1	7	**OUTPUT_HSP** 0 = Positive pulse (default.) 1 = Negative pulse.	
0305Ah through 030FFh	**RESERVED for Protocol Converter Extension**			Read all 0s

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Table 2-167: Address Mapping within DPCD Multi-touch (for eDP) Field (DPCD Addresses 60000h through 61CFFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within Multi-touch (for eDP) Field	
The Multi-touch field is valid only with DPCD r1.3 (applicable to the *eDP v1.4* DPRX).			
60000h through 61CFFh	**RESERVED for Multi-touch (for *eDP v1.4* or higher)**		

Table 2-168: Address Mapping within DPCD HDCP 1.3 and HDCP2.2 Field (DPCD Addresses 68000h through 69FFFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within HDCP 1.3 and HDCP2.2 Field	
68000h through 68FFFh	**RESERVED for HDCP1.3** See HDCP v1.3.		
69000h through 69FFFh	**RESERVED for HDCP2.2** See HDCP v2.2.		

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
The LT-tunable PHY Repeater field is valid only with DPCD r1.4. LT-tunable PHY Repeater-related registers located at DPCD Addresses F0000h through F02FFh are valid only when the DPCD revision is DPCD r1.4 or higher. ***Note:*** *DPCD Addresses F0010h through F005Fh comprise the PHY_Repeater1 Configuration and Status field.*				
F0000h	**LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV** LT-tunable PHY Repeater must return the lowest common denominator of its own value and the downstream PHY Repeater link value only when the response received on a DFP is non-zero. If response received on a DFP is 0, the value of this field is returned.			Read Only
		3:0	**Minor Revision Number** 4h for this Standard.	
		7:4	**Major Revision Number** 1h for this Standard.	
F0001h	**MAX_LINK_RATE_PHY_REPEATER** Maximum link rate of Main-Link lanes = Value x 0.27Gbps.			Read Only
		7:0	**MAX_LINK_RATE** Only four values are supported. All other values are RESERVED except for *eDP v1.4* (DPCD r1.3 or lower) and MyDP DPRX. 06h = 1.62Gbps/lane. 0Ah = 2.7Gbps/lane. 14h = 5.4Gbps/lane. 1Eh = 8.1Gbps/lane. *eDP v1.4* DPRX (DPCD r1.3 or lower) can program the MAX_LINK_RATE register value to 00h to indicate that the DPRX supports the Main-Link rates by way of the Link Rate Table method. See *eDP v1.4*. A MyDP DPRX of an active MyDP converter (either MyDP-to-legacy converter or MyDP-to-DP lane-count converter) can support a value of 19h (6.75Gbps per lane).	

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F0002h	**PHY_REPEATER_CNT** Indicates the number of PHY Repeaters that are present. Up to eight are available.			Read Only
		7:0	PHY_REPEATER_CNT 80h = 1 PHY Repeater are present. 40h = 2 PHY Repeaters are present. 20h = 3 PHY Repeaters are present. … 01h = 8 PHY Repeaters are present. This field shall default to 80h when the data response received on a DFP is 0. For the case in which a non-zero value is received on a DFP, the value of this field is data received on the DFP divided by 2. This field is also used by the LT-tunable PHY Repeater to determine which PHY_REPEATER[8:1] CONFIGURATION AND STATUS register(s) to use during Link Training.	
F0003h	**PHY_REPEATER_MODE** Must be programmed to 55h upon power-on reset or an upstream device disconnect. Indicates the mode in which LT-tunable PHY Repeater is operating.			Write/Read
		7:0	**PHY_REPEATER_MODE** The LT-tunable PHY Repeater must return the lowest common denominator of its own value and the downstream PHY_REPEATER_MODE value only when the response received on a DFP is 55h or AAh. If the response received on a DFP is a value other than 55h or AAh, the value of this field is returned. The DPTX can use this field to control the PHY_REPEATER_MODE of all PHY Repeaters between the DPTX and DPRX. For example, a write request of AAh causes all PHY Repeaters to operate in Non-transparent mode. 55h = Transparent mode (default). AAh = Non-transparent mode.	

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F0004h	**Repeater_FEC_CAPABILITY** New to *DP v1.4*.			Read Only
		0	**FEC_CAPABLE** 0 = Not capable. 1 = Capable.	
		1	**UNCORRECTED_BLOCK_ERROR_COUNT_CAPABLE** 0 = Not capable. 1 = Capable.	
		2	**CORRECTED_BLOCK_ERROR_COUNT_CAPABLE** 0 = Not capable. 1 = Capable.	
		3	**BIT_ERROR_COUNT_CAPABLE** 0 = Not capable. 1 = Capable.	
		7:4	**RESERVED**	Read all 0s
F0005h through F000Fh	**RESERVED for LT-tunable PHY Repeater**			Read all 0s
F0010h	**TRAINING_PATTERN_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_PATTERN_SET register (DPCD Address 00102h). This field is mirrored in all PHY Repeaters. The remaining PHY Repeaters between DPTX and DPRX must snoop writes to this field.			Write/Read
F0011h	**TRAINING_LANE0_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE0_SET register (DPCD Address 00103h). The LT-tunable PHY Repeater upstream of PHY_Repeater1 must snoop writes to this field and update its output levels (Swing and Pre-emphasis) based on the value written to this field.			Write/Read
F0012h	**TRAINING_LANE1_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE1_SET register (DPCD Address 00104h). The LT-tunable PHY Repeater upstream of PHY_Repeater1 must snoop writes to this field and update its output levels (Swing and Pre-emphasis) based on the value written to this field.			Write/Read

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F0013h	**TRAINING_LANE2_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE2_SET register (DPCD Address 00105h). The LT-tunable PHY Repeater upstream of PHY_Repeater1 must snoop writes to this field and update its output levels (Swing and Pre-emphasis) based on the value written to this field.			Write/Read
F0014h	**TRAINING_LANE3_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the TRAINING_LANE3_SET register (DPCD Address 00106h). The LT-tunable PHY Repeater upstream of PHY_Repeater1 must snoop writes to this field and update its output levels (Swing and Pre-emphasis) based on the value written to this field.			Write/Read
F0015h	**LINK_QUAL_LANE0_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE0_SET register (DPCD Address 0010Bh).			Write/Read
F0016h	**LINK_QUAL_LANE1_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE1_SET register (DPCD Address 0010Ch).			Write/Read
F0017h	**LINK_QUAL_LANE2_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE2_SET register (DPCD Address 0010Dh).			Write/Read
F0018h	**LINK_QUAL_LANE3_SET_PHY_REPEATER1** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definition is identical to that of the LINK_QUAL_LANE3_SET register (DPCD Address 0010Eh).			Write/Read
F0019h through F002Fh	**RESERVED for LT-tunable PHY Repeater**			Read Only
F0030h	**LANE0_1_STATUS_PHY_REPEATER1** Bit definition is identical to that of the LANE0_1_STATUS register (DPCD Address 00202h).			Read Only
F0031h	**LANE2_3_STATUS_PHY_REPEATER1** Bit definition is identical to that of the LANE2_3_STATUS register (DPCD Address 00203h).			Read Only

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F0032h	**LANE_ALIGN_STATUS_UPDATED_PHY_REPEATER1** Bit definition is identical to that of the LANE_ALIGN__STATUS_UPDATED register (DPCD Address 00204h).			Read Only
F0033h	**ADJUST_REQUEST_LANE0_1_PHY_REPEATER1** Bit definition is identical to that of the ADJUST_REQUEST_LANE0_1 register (DPCD Address 00206h).			Read Only
F0034h	**ADJUST_REQUEST_LANE2_3_PHY_REPEATER1** Bit definition is identical to that of the ADJUST_REQUEST_LANE2_3 register (DPCD Address 00207h).			Read Only
F0035h and F0036h	**SYMBOL_ERROR_COUNT_LANE0_PHY_REPEATER1** Bit definition is identical to that of the SYMBOL_ERROR_COUNT_LANE0 register (DPCD Address 00210h and 00211h).			Read Only
F0037h and F0038h	**SYMBOL_ERROR_COUNT_LANE1_PHY_REPEATER1** Bit definition is identical to that of the SYMBOL_ERROR_COUNT_LANE1 register (DPCD Address 00212h and 00213h).			Read Only
F0039h and F003Ah	**SYMBOL_ERROR_COUNT_LANE2_PHY_REPEATER1** Bit definition is identical to that of the SYMBOL_ERROR_COUNT_LANE2 register (DPCD Address 00214h and 00215h).			Read Only
F003Bh and F003Ch	**SYMBOL_ERROR_COUNT_LANE3_PHY_REPEATER1** Bit definition is identical to that of the SYMBOL_ERROR_COUNT_LANE3 register (DPCD Address 00216h and 00217h).			Read Only
F003Dh	**IEEE_OUI** First two hex digits.			Read Only
F003Eh	**IEEE_OUI** Second two hex digits.			Read Only
F003Fh	**IEEE_OUI** Third two hex digits.			Read Only
F0040h through F0045h	**LT-tunable PHY Repeater Device Identification String** Identifies an LT-tunable PHY Repeater device. Up to six ASCII characters, starting at *XXX*h. Remaining bytes are 00h if fewer than six characters.			Read Only
F0046h	**Hardware Revision**			Read Only
F0047h	**Firmware/Software Major Revision**			Read Only
F0048h	**Firmware/Software Minor Revision**			Read Only
F0049h through F005Fh	**Vendor-Specific Space for PHY_Repeater1**			Vendor-Specific

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F0060h through F00AFh	**PHY_REPEATER2 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater2.			Write/Read and Read Only
F00B0h through F00FFh	**PHY_REPEATER3 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater3.			Write/Read and Read Only
F0100h through F014Fh	**PHY_REPEATER4 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater4.			Write/Read and Read Only
F0150h through F019Fh	**PHY_REPEATER5 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater5.			Write/Read and Read Only
F01A0h through F01EFh	**PHY_REPEATER6 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater6.			Write/Read and Read Only
F01F0h through F023Fh	**PHY_REPEATER7 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater7.			Write/Read and Read Only
F0240h through F028Fh	**PHY_REPEATER8 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0010h through F005Fh), but for PHY Repeater8.			Write/Read and Read Only
F0290h	**FEC_STATUS_PHY_REPEATER1**			Write/Read and Read Only
		0	**FEC_DECODE_EN_DETECTED** 0 = Not detected. 1 = Detected.	
		1	**FEC_DECODE_DIS_DETECTED** 0 = Not detected. 1 = Detected.	
		7:2	**RESERVED**	Read all 0s

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F0291h and F0292h	**FEC_ERROR_COUNT_PHY_REPEATER1** New to *DP v1.4*.			Write/Read and Read Only
	0	7:0	**FEC_ERROR_COUNT_PHY_REPEATER1_7:0** Least significant eight bits of the 15-bit error count.	
	1	6:0	**FEC_ERROR_COUNT_PHY_REPEATER1_14:8** Most significant seven bits of the 15-bit error count.	
	1	7	**FEC_ERROR_COUNT_VALID** 0 = Not valid. 1 = Valid.	
F0293h through F0297h	**RESERVED for LT-tunable PHY Repeater**			Read all 0s
F0298h and F029Fh	**FEC_PHY_REPEATER2 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater2.			Write/Read and Read Only
F02A0h and F02A7h	**FEC_PHY_REPEATER3 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater3.			Write/Read and Read Only
F02A8h and F02AFh	**FEC_PHY_REPEATER4 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater4.			Write/Read and Read Only
F02B0h and F02B7h	**FEC_PHY_REPEATER5 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater5.			Write/Read and Read Only
F02B8h and F02BFh	**FEC_PHY_REPEATER6 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater6.			Write/Read and Read Only
F02C0h and F02C7h	**FEC_PHY_REPEATER7 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater7.			Write/Read and Read Only

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Table 2-169: Address Mapping within DPCD LT-tunable PHY Repeater Field (DPCD Addresses F0000h through F02FFh) (Continued)

DPCD Address	Register			Read/ Write over AUX CH
	Byte #	Bit #	Definition within LT-tunable PHY Repeater Field	
F02C8h and F02CFh	**FEC_PHY_REPEATER8 CONFIGURATION AND STATUS FIELD** Must be cleared to 00h upon power-on reset or an upstream device disconnect. Bit definitions are identical to that of the PHY_Repeater1 Configuration and Status field (DPCD Addresses F0290h through F0292h), but for FEC_PHY Repeater8.			Write/Read and Read Only
F02D0h through F02FFh	**RESERVED for LT-tunable PHY Repeater**			Read all 0s

Table 2-170: Address Mapping within DPCD MyDP-specific Field (DPCD Addresses FFF00h through FFFFFh)

DPCD Address	Register		Read/ Write over AUX CH
	Bit #	Definition within MyDP-specific Field	
FFF00h	**RESERVED for MyDP-specific**		
FFF01h	**MyDP_POWR_CAP** See MyDP v1.0 and SCR.		
FFF02h through FFFFFh	**RESERVED for MyDP-specific**		

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2.9.4 AUX Link Services

To transport an isochronous data stream from the Source device to the Sink device, Link Policy Maker must first establish the Main-Link. The Main-Link must be established in the following sequence of steps.

Note: *All the commands are memory-mapped, whether setting or getting link parameters.*

Step_1:

Unless it has pre-set knowledge, the Source must initiate Link Discovery, by reading the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155) and Extended Receiver Capability field (DPCD Addresses 02200h through 022FFh; see Table 2-165) through the AUX CH. The Receiver Capability and Extended Receiver Capability fields must describe the Sink device DPRX's Main-Link receiver capability, such as the maximum bit rate and maximum number of lanes. Details on reading the DPCD are explained later in this section.

Step_2:

Based on the DPCD information, the Source must start the Link Initialization process. The following sequences must take place during Link Initialization:

1 The Link Policy Maker in the Source device must start Link Training. This function call notifies the Sink device of the ensuing transport of the training pattern through the Main-Link PHY Layer, with link configuration and training attributes defined in this function.

2 The Link Policy Maker of the Source device must check the training status and report of final results to the Stream Policy Maker.

If the Link Policy Maker detects a failed Link Training attempt, it must take corrective action. Possible correction actions are:

- Reduction of the bit rate if the link was in the high bit rate mode
- Termination of Link Initialization

This loop of setting the Main-Link configuration and forwarding training pattern, while checking the status must end with the final result of either pass or fail. "Pass" means that the bit lock and symbol lock have been achieved on each of the configured lanes, and all the lanes are symbol locked with proper inter-lane alignment (with skew of two LS_Clk period between adjacent lanes). Otherwise, it is "fail."

After the Main-Link is established, the Link Policy Maker of the Source device must check the link status whenever it detects the HPD (Hot Plug Detect) signal toggle after the rising edge of HPD. The Source device must ignore low or high pulse period of less than 0.25ms. In other words, the Source device must not check the link status until at least 0.25ms after the rising edge.

The Sink device must clear the HPD signal to a low level for 0.5 to 1ms before setting it high again whenever there is a status change either in the link or in the device. This will notify the Source device of the status change.

The Source device must check the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157) through an AUX read transaction to identify the cause within 100ms of the rising edge of the HPD. Upon identifying the cause, the Link Policy Maker must take corrective action.

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If the HPD is the result of a new device being connected, either directly to the Source device (signaled by a long HPD), or downstream of a Branch device (indicated by incrementing the value of the DFP_COUNT field in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bits 3:0) and signaled by an IRQ_HPD pulse), the Source device must read the new EDID that has been made available to it to ensure that content being transmitted over the link is able to be properly received and rendered.

Note: ***(Informative)*** *In case the HPD signal toggling (or bouncing) is the result of the Hot Unplug followed by Hot Plug of a cable-connector assembly, then the HPD signal is likely to remain unstable during the de-bouncing period, which is in the order of tens of milliseconds. The Source device may either check stability of the HPD signal before initiating an AUX read transaction or immediately initiate the AUX read transaction after each HPD rising edge.*

2.9.4.1 IEEE OUI and Device Identification

Device designs with different DP PHY Layer and/or Link Layer implementations must be distinguished by unique combinations of IEEE OUI, Device Identification String, Hardware Version and firmware/software version (collectively called the Source Device Identification, Sink Device Identification, or Branch Device Identification, as appropriate). The specific values for the offsets 00*n*03h through 00*n*0Bh are determined by the owner of the OUI specified in 00*n*00h through 00*n*02h (for $n = 3$ for Source devices, $n = 4$ for Sink devices, $n = 5$ for Branch devices). The Source device must use a burst write when updating the Source Device Identification.

This Standard does not preclude the Source device from dynamically updating the Source Device Identification. For example, if the Source device supports multiple independent Source device-specific behaviors, and needs to dynamically switch between them, then the Source device must use distinct Source Identifications for these. A Sink device must maintain the current values of the Source device-specific registers and associated states for the functions associated with each Source Identification that it supports, preserving these when the Source device switches away from the corresponding Source Device Identification and reinstating them when Source device switches back to the corresponding Source Device Identification.

2.9.4.2 DPCD in Multi-Link Topology with SST-only Mode Source Device

A DisplayPort topology has multiple links when one or more Sink devices connect to a Source device by way of Branch device(s). A Branch device forwarding SST transport format from an input port to an output port, acting as an SST-mode Repeater device, must comprehend the DPCD(s) of its downstream links as described in Section 2.1.4.1. An SST-only mode upstream DP device must check only the DPCD of its immediate downstream device regardless of the link topology.

2.9.4.2.1 Receiver Capability of Downstream Legacy Link

Generally speaking, a legacy link does not have a Receiver Capability field equivalent to that defined for DPCD.

Capabilities vary. Some legacy links can support both audio and video, while others are limited to video only. Supported pixel data rate and color format are also dependent on the type of legacy link and its implementation.

A DP Source device, when connected to a legacy Sink device via a DisplayPort-to-Legacy converter, must determine the stream format based on the Sink device capability expressed in the EDID of the legacy Sink device and whether the cable adaptor is an HDMI cable adaptor.

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2.9.4.3 Link Initialization through Link Training

DisplayPort link initialization (before transporting a stream) must be performed unless the Source Main-Link transmitter and the Sink Main-Link receiver are already in synchronization as indicated in the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157). During link initialization, AUX transactions must be used to train the link with a desired set of link configuration parameters. For a detailed description of the Link Training sequence, see Section 3.5.1.2.

An exception for Link Training requirement exists for embedded DisplayPort connections. When DP Source device reads 1 in the NO_AUX_TRANSACTION_LINK_TRAINING bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 6) of DP Sink device, it may transmit TPS1 (which is a repetition of D10.2 symbols without scrambling) and TPS2, TPS3, or TPS4, depending on the common capability of the DPTX and DPRX before switching to normal operation without AUX transactions (i.e., no AUX transactions are used to initiate training, during training or on completion of successful training).

There is another exception for a box-to-box connection. When DP Source device is resuming the transmission (e.g., after waking from sleep), the Source device may skip the AUX transactions for the link training if the following conditions are met:

- The Source device has determined that the HPD signal has remained asserted continuously (apart from IRQ_HPD notifications) since the link was last in full operation.
- The Source device has read 1 in NO_AUX_TRANSACTION_LINK_TRAINING bit after the initial Sink device detection.

If the conditions listed above are met, and if the Source device determines that bandwidth to be used is the same as that used when the link was last in full operation, the Source device may transmit Link Training Pattern Sequences 1 and 2 (500us minimum for each) using the last known good voltage swing and pre-emphasis settings before switching to the normal operation without AUX transactions. Whether the full Link Training is skipped or not, the DP Sink device must send an IRQ_HPD pulse over the HPD signal line when it fails to synchronize to the incoming Main-Link stream.

After Link Training is successfully completed (which means that the DPRX is synchronized to incoming Main-Link data) and before transport of a main video stream starts, the Source Main-Link transmitter must be sending the “idle pattern” consisting of BS symbol sequence BS+BF+BF+BS followed by the NoVideoStream_Flag bit in the VB-ID (bit 3) set to 1 inserted every 2^{13} (or 8192) link symbols. Every 512th occurrence of the BS symbol sequence set must be replaced by the scrambler reset symbol sequence SR+BF+BF+SR.

The Source device must start sending the idle pattern after it has cleared the Training_Pattern byte in the DPCD. The Sink device should be ready to receive the “idle pattern” as soon as it updates the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157), to indicate the successful completion of Link Training to the Source device.

Link training may result in the available bandwidth being lower than that originally attempted (e.g., an attempt to train at HBR fails, and training falls back to RBR). The Source device must not attempt to transmit an AV stream that requires a bandwidth higher than that actually in use.

A link may be re-trained for some reason. A Source must be tolerant to the available bandwidth resulting from re-training being lower than the bandwidth resulting from prior training, and this may in turn require a video mode set change.

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For a closed embedded connection, the DPTX and DPRX may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, the DPTX may start a normal operation following transmission of the Clock Recovery Pattern with pre-calibrated drive current and pre-emphasis level.

When switching to an MST format following the link training, the DPTX of an upstream device must set the MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) prior to starting Link Training. The upstream device is required to send a minimum of four MST Link Frames (four SR cycles) of empty MTPs prior to the startup of a stream.

2.9.4.4 Link Maintenance

The downstream device with a DPRX must maintain the Link Status flags in the following registers during normal operation:

- LANE*x*_*y*_STATUS register(s) and LANE*x*_*y*_STATUS_ESI registers (DPCD Address(es) 00202h and 00203h, and 0200Ch and 0200Dh, respectively)
- LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively)

Upon loss of synchronization with the Source for any reason other than after receiving a request to program the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) to 10b, or to request re-training the link for any reason, the Sink must clear the INTERLANE_ALIGN_DONE bit in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers and generate a distinct IRQ_HPD (i.e., distinct from an IRQ_HPD generated for any other reason). The Link Policy Maker of the Source device must check the link status whenever it detects the IRQ_HPD signal toggle within 100ms of the rising edge of the HPD for possible Main-Link synchronization loss. This check is performed by reading the Link Status field, located at DPCD Addresses 00200h through 00205h.

Note: *The format change in the transported stream does not necessarily result in a Link Status change, as long as the link remains stable. For example, some Source devices may choose to continue transmitting stuffing symbols when the stream has stopped. In this case, the Main-Link remains synchronized.*

2.9.4.5 Link Quality Test Support

DisplayPort supports a test procedure for measuring the link quality. The following features are supported:

- Transmission of a Nyquist pattern (repetition of D10.2 symbols without scrambling)
- Symbol Error measurement pattern
- PRBS7 bit pattern
- Custom 80-bit repeating pattern
- CP2520 (HBR2 Compliance EYE pattern)

The DP Source device may support the selecting of a test pattern independently for each of the lanes on the Main-Link.

Table 2-171 summarizes which patterns for Link Training and Link Quality Measurement are scrambled.

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Table 2-171: ANSI 8b/10b Encoding and Scrambling Rules for Link Management

Pattern Type	ANSI 8b/10b Encoded?	Scrambled?
Link Training Pattern Sequence 1	Yes	No
Link Training Pattern Sequence 2	Yes	No
Link Training Pattern Sequence 3	Yes	No
Link Training Pattern Sequence 4	Yes	Yes
D10.2 Test Pattern (Same as Link Training Pattern Sequence 1)	Yes	No
Symbol Error Rate Measurement Pattern	Yes	Yes
PRBS7	No	No
Custom 80-bit pattern	No	No
CP2520 Patterns 1/2/3	Yes	Yes

When transmitting a pattern that is not scrambled, the Source must set the SCRAMBLING_DISABLE bit in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bit 5). Sink devices must not rely on this bit being set.

2.9.4.5.1 Transmission of Nyquist Pattern

This pattern consists of repetition of D10.2 symbols (without scrambling), identical to Link Training Pattern Sequence 1 for Bit-lock. This pattern results in the Main-Link toggling at its highest frequency (e.g., 1.35GHz when the link bit rate is 2.7Gbps). System integrators may use this pattern to measure, for example, the jitter performance of the transmitted signals.

The DP Source device signals the transmission of this pattern by writing 001 to the Lane's LINK_QUAL_PATTERN_SET fields in the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh, bits 2:0).

Upon being notified of the transmission of this pattern, the DP Sink device must blank its screen while keeping the DPRX running.

2.9.4.5.2 Symbol Error Rate Measurement Pattern

This pattern consists of repetition of data 00h (prior to ANSI 8b/10b encoding) that is scrambled by a transmitter. (See Appendix E for details regarding the scrambling polynomial.) The DP Source device must periodically (every 2^{13} or 8192 symbols) transmit a Single Stream Transport BS symbol sequence. The PHY Layer must replace every 512th BS symbol sequence with an SR symbol sequence to reset the scrambler.

VB-ID/Mvid/Maud values, as well as the other data symbols, must be cleared to 00h while the Symbol Error Rate Measurement Pattern is being transmitted.

Upon being notified of the transmission of this pattern, the DP Sink device must start increasing the SYMBOL_ERROR_COUNT_LANE*x* register's (DPCD Addresses 00210h through 00217h; each register is comprised of two bytes, within which the error count is stored in the 15 least significant bits) value each time it has unscrambled data value other than 00h.

The DP Source device must read the SYMBOL_ERROR_COUNT_LANE*x* values some time later. Using the read values and elapsed time, it must calculate the approximate symbol error rate.

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Transmitting $1E^{+9}$ link symbols takes roughly 10s. Therefore, the transmitter is recommended to wait for 10 to 100s before reading the Symbol Error count from a receiver.

Symbol error rate is calculated as follows:

- At 8.1Gbps/lane:

  Symbol Error Rate in units of 10^{-9}
  *= Error_Count / (0.81 * Measurement Period in seconds)*

- At 5.4Gbps/lane:

  Symbol Error Rate in units of 10^{-9}
  *= Error_Count / (0.54 * Measurement Period in seconds)*

- At 2.7Gbps/lane:

  Symbol Error Rate in units of 10^{9}
  *= Error_Count / (0.27 * Measurement Period in seconds)*

- At 1.62Gbps/lane:

  Symbol Error Rate in units of 10^{-9}
  *= Error_Count / (0.162 * Measurement Period in seconds)*

2.9.4.5.3 PRBS and Bit Pattern

See the TRAINING_PATTERN_SET register (DPCD Address 00102h) for a detailed description of the PRBS7 bit pattern.

2.9.4.5.4 80-Bit Custom Pattern

An upstream DP device that supports HBR2 must be capable of sending out an 80-bit repeating pattern. An upstream DP device that does not support HBR2 may be capable of sending out an 80-bit repeating pattern. The custom pattern is not scrambled or encoded with ANSI 8b/10b. The custom pattern allows for more flexibility during Physical Compliance testing of upstream devices only (does not apply to downstream devices).

2.9.4.5.5 CP2520 (HBR2 Compliance EYE Pattern)

An upstream DP device that is capable of supporting HBR2 must be capable of sending the repetition of scrambled data 00h with ANSI 8b/10b encoding. (See Appendix E for details regarding the scrambling polynomial.) This capability is optional for upstream devices that do not support HBR2. The upstream device must output an Enhanced Framing Scrambler Reset sequence (SR BF BF SR) for every HBR2_COMPLIANCE_SCRAMBLER_RESET register (DPCD Addresses 0024Ah and 0024Bh) symbols transmitter (the count to include the four symbols comprising the scrambler reset sequence). If HBR2_COMPLIANCE_SCRAMBLER_RESET is fewer than 4, a scrambler reset sequence is not transmitted.

An HBR2-capable downstream DP device must be capable of receiving the CP2520 (HBR2 Compliance EYE pattern) from test equipment. During compliance testing, the downstream device scrambler will be reset by an SR symbol after Link Training completes. The HBR2 downstream DP device must start increasing the SYMBOL_ERROR_COUNT_LANE*x* register's (DPCD Addresses 00210h through 00217h; each register is comprised of two bytes, within which the error count is stored in the 15 least significant bits) value each time it has an unscrambled data value other than 00h.

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2.9.5 AUX Device Services

AUX Device Services are used for the purpose of communication between the graphic host (a DP Source device) and display device (a DP Sink device). The following are examples of display device services that are supported by using AUX transactions:

- EDID Support
- MCCS Support
- Sink Event Notification

EDID and MCCS over DDC/CI are supported by mapping I^2C transactions onto DisplayPort to maintain maximum software transparency.

In addition, the AUX transactions are expected to be used for an optional content protection feature.

2.9.5.1 E-DDC Support through I^2C Mapping

E-DDC allows the display to inform the host about its identity and capability using an I^2C bus. E-DDC enables the communication channel to address a larger set of data than the 128 bytes of the base EDID block. E-DDC allows access of up to 32KB of data based on a segment pointer which allows access to multiple blocks of 256 bytes.

Using the I^2C bus transaction mapping described in Section 2.8.5, E-DDC transactions may be supported with AUX transactions over the AUX CH.

2.9.5.2 MCCS over DDC/CI Support through I^2C-over-AUX Transactions

MCCS provides a set of commands that may be used to control the functions and features of the display.

By using the I^2C-over-AUX transactions described in Section 2.8.5, MCCS transactions over DDC/CI may be supported over the AUX CH.

This Standard does not define a minimum required set of MCCS commands. However, it should be noted that some specifications, including the MCCS standard and operating system logo programs, do define minimum sets to be supported.

2.9.5.3 Sink Event Notification

The DisplayPort Standard supports a mechanism through which a Sink device can notify the Source device of a Sink event.

An example of how the sink event notification may be supported is described in Appendix B.

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2.10 Alternate Scrambler Reset for eDP

2.10.1 Protocol Differentiation Method

An alternate scrambler reset method is defined to ensure non-interoperability between compliant eDP Sources and non-eDP Sinks where such non-interoperability is defined as the inability to reliably convey audio or video data from Source to Sink.

Implementation of this method is optional. Consistent with other eDP practices, the system integrator is ultimately responsible for ensuring interoperability between the eDP Source and Sink chosen for a particular application. Determination by a given device (Source, Sink, or Branch) used in an embedded system is an implementation matter beyond the scope of this Standard.

With the alternate scrambler reset method, the SR symbol resets the LFSRs in the Source and Sink devices to FFFEh, rather than (the non-eDP connection) value FFFFh. This method shall be implemented only in devices that provide eDP connections over embedded (non-user-accessible) interconnects. Tamper-resistant methods[a] should be used in devices that allow operation in either eDP or box-to-box DisplayPort applications to be determined at manufacturing/assembly time by the system integrator:

2.10.2 Symbol Error Rate Measurement Pattern Output (Informative)

Table 2-172 contains the first 50 symbols of the Symbol Error Rate Measurement Pattern following a Scrambler Reset. These are 8-bit values after scrambling and before ANSI 8b/10b encoding.

a. For example: package bond options, fuses, or external strapping options, buried vias/trace connections.

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Table 2-172: Symbol Error Rate Measurement Pattern following Scrambler Reset

Symbol #	Normal Scrambling (hex)	Alternate Scrambling (hex)	Symbol #	Normal Scrambling (hex)	Alternate Scrambling (hex)
1	FF	FF	26	02	CF
2	17	97	27	77	F1
3	C0	C0	28	2A	64
4	14	88	29	CD	07
5	B2	12	30	34	C5
6	E7	65	31	BE	DF
7	02	C9	32	E0	3F
8	82	94	33	A7	27
9	72	BA	34	5D	92
10	6E	BB	35	24	D0
11	28	AB	36	B1	0D
12	A6	2A	37	9B	D9
13	BE	01	38	A1	74
14	6D	14	39	BD	A9
15	BF	61	40	22	86
16	8D	2F	41	D4	23
17	BE	00	42	45	D2
18	40	29	43	1D	D4
19	A7	F8	44	D3	A3
20	E6	6F	45	D7	8D
21	2C	87	46	EA	A0
22	D3	CF	47	76	90
23	E2	F3	48	EE	3B
24	B2	14	49	2C	87
25	07	85	50	DA	96

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2.11 Messaging AUX Client

The Messaging AUX client described in this section achieves the following features:

- A mechanism for sending requests and receiving replies from remote DP nodes using Native AUX transactions to maintain a DP topology map, to add, update, and delete Virtual Channels, to read or write remote devices DPCD locations, and to send I^2C transactions to I^2C devices connected to remote DP nodes (e.g., EDID read).
- A mechanism for reporting status changes to clients of the Messaging AUX client
- A mechanism for reporting errors in delivery of requests to the request originator.

The Messaging AUX client is a client of the AUX transaction arbitor. The Messaging AUX client provides the means of communication between any two DP nodes of a topology. Figure 2-115 shows the position of the Messaging AUX client in DP nodes.

Figure 2-115: Messaging AUX Client in DP Nodes

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Clients of the Messaging AUX Client are the Topology Management, Payload Bandwidth Management, and Device-/Vendor-Specific Services for Stream/Link Policy Maker.

This section consists of the following sub-sections:

- Section 2.11.1 – Messaging AUX Client Layers

  Brief overview of the two functional layers constituting the Messaging AUX Client Layer; Message Transaction Layer on top of Sideband MSG Layer.

- Section 2.11.2 – Message Transaction Layer

  A Request and Reply Message Transaction pair constitutes a Message Transaction sequence. Request Message Transactions may be originated either by a DPTX of an upstream DP node (DOWN_REQ_MSG) or DPRX of a downstream DP node (UP_REQ_MSG). Syntax of Request and Reply Message Transactions and handling of multiple Message Transactions are covered in this sub-section.

- Section 2.11.3 – Sideband MSG Layer

  The Sideband MSG consists of Sideband MSG Header and Body. The Sideband MSG Header describes the target DP Node address (called Relative Address, or RAD) and which nodes along the message path are to receive the message. The Sideband MSG Body carries the Body of the Message Transaction. If the Message Transaction Body does not fit in a single Sideband MSG Body, it is divided into multiple Sideband MSG Bodies. Each Sideband MSG Header for a given Message Transaction has the same Sideband MSG Header except a bit indicating End Of Transaction (EMT) or Start of Transaction (SMT).

- Section 2.11.4 – AUX Support for Messaging AUX Client

  Sideband MSG uses Native AUX write/read transactions to certain DPCD address range to move Sideband MSG Header and Body between adjacent DP nodes. The intermediate DP nodes update Relative Address and forward the Sideband MSG to the target DP node.

- Section 2.11.5 – RAD Updated by MST Devices in the Path

  The RAD is an array of nibbles of size Link_Count_Total - 1 contained in Sideband MSG Header.

- Section 2.11.6 – Broadcast Message Transactions

  Messaging AUX Client provides for Broadcast messages as well as targeted messages. Broadcast Message Transactions are identified with a unique Relative Address with which the recipients of the Broadcast Message can reply with ACK/NACK Reply Message.

- Section 2.11.7 – Message Delivery

  Procedures and requirements are defined for delivering Sideband MSGs between DP devices using Native AUX requests.

- Section 2.11.8 – Error Handling

  Errors are handled at the Message Transaction Layer. The Sideband MSG will be dropped when an error is detected at the Sideband MSG Layer, thus causing a Message Transaction timeout error.

- Section 2.11.9 – Descriptions of Available Message Transaction Requests

  This sub-section describes the 14 available Request Message Transactions.

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The message syntax used within this section assumes the following:

- First byte defined is sent first.
- All fields are defined from most-significant bit and most significant byte first.
- The byte-aligned () function returns true when the next input bit is the first bit of a new byte (the next bit is on a new byte boundary).

2.11.1 Messaging AUX Client Layers

The Messaging AUX Client consists of two functional layers, Message Transaction Layer and Sideband MSG Layer, as shown in Figure 2-116.

Figure 2-116: Messaging AUX Client Layers

The Message Transaction Layer implements the Message Transaction protocol built on top of Sideband MSG protocol. The Message Transaction protocol is a request-reply protocol supporting the topology discovery and maintenance, establishment or removal of VC Payloads and transfer of data between DP nodes for Device-or Vendor-Specific Services.

Message Transaction protocol has a version number associated with it, as defined in Table 2-173. A Source device obtains this version number on a path by transmitting the GET_MESSAGE_TRANSACTION_VERSION Message Transaction to the last MST device with a branching unit driving a stream sink. This last MST device responds with the Message Transaction protocol version number that it implements, or replies with a NAK if that device does not support the GET_MESSAGE_TRANSACTION_VERSION Message Transaction. Upstream devices treat a NAK as indicating a Protocol Version Number of 1.

It is mandatory for all MST-capable Branch and Sink devices compliant to DP v1.3 and higher to support GET_MESSAGE_TRANSACTION_VERSION. Such devices must minimally return a value corresponding to Version and Revision number for the DisplayPort Standard as indicated in Table 2-173. In particular, DP v1.3-compliant devices must not return a Protocol Version Number of 01h because GET_MESSAGE_TRANSACTION_VERSION is now supported.

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Table 2-173: Message Transaction Protocol Version Numbers

DisplayPort Standard	Protocol Version Number
Version 1 Revision 2a	01h
Version 1 Revision 3	02h

Only MST DP devices which implement the Topology Maintenance function as a Topology Manager can originate request Message Transactions with a target DP device address. Any MST DP device can originate Broadcast Message Transactions as Broadcast Message Transactions do not contain a target DP device.

A Message Transaction request originated by a DPTX is referred to as a down (i.e., downward direction) request message, DOWN_REQ_MSG, and the associated reply is referred to as a down reply message, DOWN_REP_MSG (Figure 2-117). Message Transaction requests originating from a DPRX are referred to as an up (i.e., upward-direction) request message, UP_REQ_MSG and the associated reply is referred to as an up reply message, UP_REP_MSG (Figure 2-118).

Figure 2-117: Down Request Message and Down Reply Message

Figure 2-118: Up Request Message and Up Reply Message

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The Sideband MSG Layer implements the Sideband MSG protocol using Native AUX transactions as the underlying layer. The Sideband MSG protocol consists of data packets sent between two DP nodes. A Sideband MSG data packet consists of a Sideband MSG header containing the DP node address (Relative Address, or RAD) followed by the Sideband packet body containing the Sideband MSG client data and Sideband MSG body CRC.

Native AUX transactions are used to transfer the data from a DP node to its immediate downstream or upstream DP node.

2.11.2 Message Transaction Layer

The Message Transaction Layer implements the Message Transaction protocol. The Message Transaction protocol is used by one DP node to obtain or update information in another DP node.

2.11.2.1 Message Transaction Protocol

The Message Transaction protocol is comprised of Message Transaction sequences. There are two types of message transactions – Request and Reply Message transactions. A Request-and-Reply Message Transaction pair defines a Message Transaction sequence.

Table 2-174: Message Transaction Sequence Syntax

Syntax	# of Bits

`Message_Transaction_Sequence()`
`{`
`  Message_Transaction_Request()`
`  Message_Transaction_Reply()`
`}`	

2.11.2.2 Message_Transaction_Request ()

Table 2-175: Message Transaction Request Syntax

Syntax	# of Bits
`Message_Transaction_Request()` `{`	
`  zero`	1
`  Request_Identifier`	7
`  Request_Data()` `}`	

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2.11.2.2.1 Request_Identifier

The Request_Identifier field specifies the information to be obtained or updated. Table 2-176 is a list of valid Request_Identifiers.

Table 2-176: Request Names and Identifiers

Request Name	Request_Identifier
GET_MESSAGE_TRANSACTION_VERSION	00h
LINK_ADDRESS	01h
CONNECTION_STATUS_NOTIFY	02h
ENUM_PATH_RESOURCES	10h
ALLOCATE_PAYLOAD	11h
QUERY_PAYLOAD	12h
RESOURCE_STATUS_NOTIFY	13h
CLEAR_PAYLOAD_ID_TABLE	14h
REMOTE_DPCD_READ	20h
REMOTE_DPCD_WRITE	21h
REMOTE_I2C_READ	22h
REMOTE_I2C_WRITE	23h
POWER_UP_PHY	24h
POWER_DOWN_PHY	25h
SINK_EVENT_NOTIFY	30h
QUERY_STREAM_ENCRYPTION_STATUS	38h

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2.11.2.2.2 Request_Data ()

Request_Data is dependent upon the Request_Identifier of the request message transaction. Table 2-177 specifies the Request_Data for requests that have request data fields. The fields in Table 2-177 are defined in Section 2.11.9. Requests that are not listed in Table 2-177 do not have request data.

Table 2-177: Request Data

Syntax	# of Bits
`Request_Data()`	
`{`	
`if (Request Identifier == 00h) GET_MESSAGE_TRANSACTION_VERSION`	
`{`	
`Port_Number`	4
`Zeros`	4
`}`	
`else (Request_Identifier == 02h` **`CONNECTION_STATUS_NOTIFY`**	
`{`	
`Port_Number`	4
`zeros`	4
`Global_Unique_Identifier`	128
`zero`	1
`Legacy_Device_Plug_Status`	1
`DisplayPort_Device_Plug_Status`	1
`Messaging_Capability_Status`	1
`Input_Port`	1
`Peer_Device_Type`	3
`}`	
`else if (Request_Identifier == 10h)` **`ENUM_PATH_RESOURCES`**	
`{`	
`Port_Number`	4
`zeros`	4
`}`	
`else if (Request_Identifier == 11h` **`ALLOCATE_PAYLOAD`**	
`{`	
`Port_Number`	4
`Number_SDP_Streams`	4
`zero`	1
`Virtual_Channel_Payload_Identifier`	7
`Payload_Bandwidth_Number`	16
`for (i = 0; i < Number_SDP_Streams; i++)`	
`{`	
`SDP_Stream_Sink[i]`	4
`}`	
`while (!bytealigned())`	
`{`	
`zeros`	1
`}`	
`}`	
`else if (Request_Identifier == 12h)` **`QUERY_PAYLOAD`**	
`{`	

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Table 2-177: Request Data (Continued)

Syntax	# of Bits
Port_Number	4
zeros	4
zero	1
Virtual_Channel_Payload_Identifier	7
}	
else if (Request_Identifier == 13h) **RESOURCE_STATUS_NOTIFY**	
{	
Port_Number	4
zeros	4
Global_Unique_Identifier	128
Available_PBN	16
}	
else if (Request_Identifier == 20h) **REMOTE_DPCD_READ**	
{	
Port_Number	4
DPCD_Address	20
Number_Of_Bytes_To_Read	8
}	
else if (Request_Identifier == 21h) **REMOTE_DPCD_WRITE**	
{	
Port_Number	4
DPCD_Address	20
Number_Of_Bytes_To_Write	8
for (i = 0; i < Number_Of_Bytes_To_Write; i++)	
Write_Data[i]	8
}	
else if (Request_Identifier == 22h) **REMOTE_I2C_READ**	
{	
Port_Number	4
zeros	2
Number_Of_I2C_Transactions	2
for (i = 0; i < Number_Of_I2C_Transactions - 1; i++)	
{	
zero	1
Write_I2C_Device_Identifier[i]	7
Number_Of_Bytes_To_Write[i]	8
for (j = 0; j < Number_Of_Bytes_To_Write; j++)	
{	
I2C_Data_To_Write[i][j]	8
}	
zeros	3
No_Stop_Bit[i]	1
I2C_Transaction_Delay[i]	4
}	
zero	1
Read_I2C_Device_Identifier[i + 1]	7
Number_Of_Bytes_To_Read	8
}	

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Table 2-177: Request Data (Continued)

Syntax	# of Bits
else if (Request_Identifier == 23h) **REMOTE_I2C_WRITE**	
{	
Port_Number	4
zeros	5
Write_I2C_Device_Identifier	7
Number_Of_Bytes_To_Write	8
for (i = 0; i < Number_Of_Bytes_To_Write; i++)	8
I2C_Data_To_Write[i]	
}	
else if (Request_Identifier == 24h) **POWER_UP_PHY**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 25h) **POWER_DOWN_PHY**	
{	
Port_Number	4
zeros	4
}	
else if (Request_Identifier == 30h) **SINK_EVENT_NOTIFY**	
{	
TBD in future version of this standard	
}	
else if (Request_Identifier == 38h) **QUERY_STREAM_ENCRYPTION_STATUS**	
{	
Stream_ID	8
Client_ID	56
Stream_Event	2
Stream_Event_Mask	1
Stream_Behavior	2
Stream_Behavior_Mask	1
zeros	2
}	
}	

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2.11.2.3 Message_Transaction_Reply ()

Each Message Transaction request must have a corresponding Message Transaction reply. The Message Transaction Reply syntax is shown in Table 2-178.

Table 2-178: Message Transaction Reply Syntax

Syntax	# of Bits
`Message_Transaction_Reply ()`	
`{`	
`  Reply_Type`	1
`  Request_Identifier`	7
`  Reply_Data()`	
`}`	

2.11.2.3.1 Reply_Type

The Reply_Type field identifies whether the Message Transaction reply is an acknowledge (ACK), or negative acknowledge (NAK), message. Reply_Type set to 1 indicates the Message Transaction is a NAK, and Reply_Type set to a 0 indicates an ACK Message Transaction.

2.11.2.3.2 Request_Identifier

The Request_Identifier field is a copy of the Request Message Transaction field of the same name. This associates the reply with the corresponding request.

2.11.2.3.3 Reply_Data ()

The contents of the Message Transaction Reply Data field depend upon the Reply_Type field and the value of the Request_Identifier field, as shown in Table 2-179.

Table 2-179: Reply Data

Syntax	# of Bits
`Reply_Data()`	
`{`	
`  if (Reply_Type == '1')`	
`  {`	
`  Global_Unique_Identifier`	128
`  Reason_For_NAK`	8
`  NAK_Data`	8
`  }`	
`  else`	
`  ACK_Data()`	
`}`	

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2.11.2.3.3.1 Global_Unique_Identifier

The global unique identifier of the DP device originating the NAK reply message transaction.

2.11.2.3.3.2 Reason_For_NAK

Reason the NAK reply is generated. Table 2-180 gives the defined NAK reasons.

Table 2-180: Reasons for NAK

Reason_For_NAK	Short Name	Description
01h	WRITE_FAILURE	Insufficient buffer space to store message transaction
02h	INVALID_RAD	Invalid address including link count, sending a Sideband MSG to a logical port
03h	CRC_FAILURE	Message Transaction CRC error
04h	BAD_PARAM	Invalid request parameter
05h	DEFER	Unable to process message within timeout period **(defer)**
06h	LINK_FAILURE	Link failure
07h	NO_RESOURCES	Insufficient resources
08h	DPCD_FAIL	DPCD access failure
09h	I2C_NAK	I^2C NAK received
0Ah	ALLOCATE_FAIL	ALLOCATE_PAYLOAD request failure (not due to lack of resources)

2.11.2.3.3.3 WRITE_FAILURE

This reply is sent when a MST DP device is unable to send the Sideband MSG to the adjacent MST DP device as specified in Section 2.11.7.

2.11.2.3.3.4 INVALID_RAD

This reply is sent when the request message is received by an end device with the LCR not equal to zero.

2.11.2.3.3.5 CRC_FAILURE

This reply is sent when a MST DP device detects an invalid Sideband MSG Header CRC value or when the targeted device detects an invalid Sideband MSG Body CRC value.

2.11.2.3.3.6 BAD_PARAM

This reply is sent when a Message Transaction parameter is in error; for example, the next port number is invalid or no device is connected to the port associated with the port number.

2.11.2.3.3.7 DEFER

This reply is sent when a MST DP device cannot execute the message transaction within the time allocated as specified in Section 2.11.7. For example, this reply will be sent when an ALLOCATE_PAYLOAD message transaction is received while another ALLOCATE_PAYLOAD message transaction is being executed. When this condition occurs, the MST DP device receiving the second ALLOCATE_PAYLOAD will send a NAK reply with DEFER as the Reason_For_NAK to the second ALLOCATE_PAYLOAD message transaction.

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2.11.2.3.3.8 LINK_FAILURE

This reply is sent by in response to the Message Transaction requests requiring an active Main-Link. These requests are ENUM_PATH_RESOURCES and ALLOCATE_PAYLOAD. This reply is sent when the link cannot be established with the downstream DPRX.

2.11.2.3.3.9 NO_RESOURCES

This reply is sent in response to an ALLOCATE_PAYLOAD Message Transaction when the requested PBN bandwidth is unavailable. The reply is sent by the MST DP device which detects the lack of bandwidth. This reply is not sent when the ALLOCATE_PAYLOAD Message Transaction failed because the resource is in use by another source or a new stream cannot be allocated because the stream count limit has been reached. The stream count limit is an implementation decision and may be less than 63.

2.11.2.3.3.10 DPCD_FAIL

This reply is associated with the REMOTE_DPCD requests. The reply is sent when an AUX NACK or DEFER is received to any Native AUX transaction resulting from the execution of the REMOTE_DPCD request. The DPCD_FAIL response is sent after all AUX retries.

2.11.2.3.3.11 I2C_NAK

This reply is associated with the REMOTE_I2C requests. The reply is sent when an AUX NACK or DEFER is received to any I^2C-over-AUX transaction resulting from the execution of the REMOTE_DPCD request. The I2C_NAK response is sent after all AUX retries.

2.11.2.3.3.12 ALLOCATE_FAIL

This reply is sent in response to an ALLOCATE_PAYLOAD Message Transaction when the ALLOCATE_PAYLOAD Message Transaction fails for any reason other than the available PBN for the link is less than the PBN requested.

2.11.2.3.3.13 NAK_Data

Any other information needed for the NAK reply. For example, the DPCD write failure Reason_For_NAK reply uses the NAK_Data field to indicate the number of bytes written before the failure occurred.

2.11.2.3.3.14 ACK_Data ()

Table 2-181 defines the data supplied with the ACK reply for those requests which reply with data. The data fields listed in the table are defined in Section 2.11.9 that describes each request.

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2.11.2.4 Handling of Multiple Message Transaction Requests

Table 2-181: ACK_DATA

Syntax	# of Bits
ACK_Data()	
{	
if (Request Identifier == 00h) GET_MESSAGE_TRANSACTION_VERSION	
{	
Message_Transaction_Version_Number	8
}	
else (Request_Identifier == 01h) **LINK_ADDRESS**	
{	
Global_Unique_Identifier	128
zeros	4
Number_Of_Ports	4
for (i = 0; i < Number_Of_Ports; i++)	
{	
Input_Port[i]	1
Peer_Device_Type[i]	3
Port_Number[i]	4
Messaging_Capability_Status[i]	1
DisplayPort_Device_Plug_Status[i]	1
if (Peer_Device_Type[i] == 101b)	
{	
Current_Capabilities_Structure	128
}	
if (Input_Port[i] == 0)	
{	
Legacy_Device_Plug_Status[i]	1
zeros	5
DPCD_Revision	8
Peer_Global_Unique_Identifier	128
Number_SDP_Streams[i]	4
Number_SDP_Stream_Sinks[i]	4
}	
else	
{	
zeros	6
}	
}	
}	
else if (Request_Identifier == 10h) **ENUM_PATH_RESOURCES**	
{	
Port_Number	4
zeros	4
Full_Payload_Bandwidth_Number_Available	16
Payload_Bandwidth_Number	16
}	
else if (Request_Identifier == 11h) **ALLOCATE_PAYLOAD**	
{	
Port_Number	4
zeros	5
Virtual_Channel_Payload_Identifier	7
Allocated_Payload_Bandwidth_Number	16
}	

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Table 2-181: ACK_DATA (Continued)

Syntax	# of Bits
`else if (Request_Identifier == 12h)` **QUERY_PAYLOAD**	
`{`	
`Port_Number`	4
`zeros`	4
`Allocated_PBN`	16
`}`	
`else if (Request_Identifier == 20h)` **REMOTE_DPCD_READ**	4
`{`	4
`zeros`	8
`Port_Number`	
`Number_Of_Bytes_Read`	8
`for (i = 0; i < Number_Of_Bytes_To_Read; i++)`	
`Data_Read[i]`	
`}`	
`else if (Request_Identifier == 21h)` **REMOTE_DPCD_WRITE**	4
`{`	4
`zeros`	
`Port_Number`	
`else if (Request_Identifier == 22h)` **REMOTE_I2C_READ**	4
`{`	4
`zeros`	8
`Port_Number`	
`Number_Of_Bytes_Read`	8
`for (i = 0; i < Number_Of_Bytes_To_Read; i++)`	
`Data_Read[i]`	
`}`	
`else if (Request_Identifier == 24h)` **POWER_UP_PHY**	4
`{`	4
`Port_Number`	
`zeros`	
`}`	
`else if (Request_Identifier == 25h)` **POWER_DOWN_PHY**	4
`{`	4
`Port_Number`	
`zeros`	
`}`	
`else if (Request_Identifier == 38h)` **QUERY_STREAM_ENCRYPTION_STATUS**	2
`{`	1
`Stream_State`	1
`Stream_Repeater_Function`	1
`Stream_Encryption`	3
`Stream_Authentication`	3
`Zeros`	2
`Stream_output_sink_type`	2
`Stream_Output_CP_Type`	1
`Zeros`	8
`Signed`	
`Stream_ID`	
`if (Signed == 1)`	160
`{`	
`L'`	
`}`	
`}`	
`}`	

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A Message Transaction originator can issue up to two requests to a given Target MST DP node without waiting for a reply. The Target MST DP node may execute requests simultaneously. Message Transaction execution shall not inhibit forwarding node type Sideband MSGs to other MST DP nodes. Path messages are not forwarded until the MST DP node has performed the action required of the message. If there is a requirement for one message to complete before another message is to be executed, it is the message originator's responsibility to wait for the first message to be complete, by receiving an ACK, before issuing the second message.

2.11.3 Sideband MSG Layer

The Sideband MSG provides the mechanism for transferring data between MST DP nodes. The Sideband MSG protocol is used to transfer Message Transaction requests and replies between MST DP nodes. If the Message Transaction length is greater than what will fit into a Sideband MSG body, the Message Transaction is split across multiple Sideband MSGs. Figure 2-119 shows how a Message Transaction is split across multiple Sideband MSGs. In the example the Sideband MSG header size is assumed to be five bytes in length. The first byte of a Sideband MSG is written to the beginning of the appropriate DPCD Sideband MSG buffer.

Figure 2-119: Mapping Message Transaction to Multiple Sideband MSGs (SB MSG CRC Is the Sideband_MSG_Data_CRC Field)

A Sideband MSG packet consists of a Sideband_MSG_Header and Sideband_MSG_Body. The Sideband MSG packet must be less than or equal to 48 bytes. The Sideband_MSG_Header contains addressing information while the Sideband_MSG_Body contains the data to be transferred. The Sideband MSG packet is defined in Table 2-182.

Table 2-182: Sideband MSG Syntax

Syntax	# of Bits

`Sideband_MSG`
`{`
`  Sideband_MSG_Header()`
`  Sideband_MSG_Body()`
`}`	

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2.11.3.1 Sideband MSG Header ()

The Sideband MSG header specifies which DP nodes are to process or receive data of the Sideband MSG. The Sideband MSG header syntax is given in Table 2-183.

Table 2-183: Sideband MSG Header Syntax

Syntax	# of Bits
`Sideband_MSG_Header()`	
`{`	
`  Link_Count_Total`	4
`  Link_Count_Remaining`	4
`  for (i = 0; i < Link_Count_Total - 1; i++)`	
`  {`	
`  Relative_Address[i]`	4
`  }`	
`  while (!bytealigned())`	
`  {`	
`  zero_bit`	1
`  }`	
`  Broadcast_Message`	1
`  Path_Message`	1
`  Sideband_MSG_Body_Length`	6
`  Start_Of_Message_Transaction`	1
`  End_Of_Message_Transaction`	1
`  zero`	1
`  Message_Sequence_No`	1
`  Sideband_MSG_Header_CRC`	4
`}`	

2.11.3.1.1 Link_Count_Total

Link_Count_Total (LCT) is the total number of DP links a Sideband MSG traverses from message originator to message target. The maximum value for Link_Count_Total is 15. Therefore, the total number of physical DP links is 15.

2.11.3.1.2 Link_Count_Remaining

Link_Count_Remaining (LCR) is the remaining number of DP links a Sideband MSG must traverse to reach the message target. The Link_Count_Remaining value is initialized to the Link_Count_Total value by the originator Sideband MSG Layer. Along the message path, the DPTX device while forwarding the Sideband MSG decrements the Link_Count_Remaining value by one. The Link_Count_Remaining value is equal to Link_Count_Total - 1 when the message arrives at the first DP node from the message originator.

2.11.3.1.3 Relative_Address

The Relative_Address (RAD) is the address of a DP node relative to the originator of the Sideband MSG. How the RAD is updated by intermediate MST devices along the path of the Message Transaction to a target device is described in Section 2.11.5.

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2.11.3.1.4 Sideband_MSG_Body_Length

The Sideband_MSG_Body_Length gives the number of bytes contained in the Sideband MSG body. The number of data bytes transferred in the Sideband MSG body is the value of the Sideband_MSG_Body_Length field - 1. The Sideband_MSG_Body_Length field value includes the Sideband_MSG_Data_CRC. The size of a Message Transaction can be calculated by adding all the Sideband_MSG_Body_Length field values needed to transfer the Message Transaction and then subtracting the count of Sideband MSGs needed to transfer the Message Transaction.

2.11.3.1.5 Start_Of_Message_Transaction

When set to 1, Start_Of_Message_Transaction (SMT) bit indicates that the Sideband MSG body contains the start of a new Message Transaction.

2.11.3.1.6 End_Of_Message_Transaction

When set to 1, End_Of_Message_Transaction (EMT) bit indicates the current Sideband MSG is the last Sideband MSG for the current message transaction. This bit will be set to 1 even if the current message transaction requires only one Sideband MSG.

2.11.3.1.7 Path_Message

When set to 1, the Path_Message bit indicates all MST DP nodes between the originator and the target are required to read and react to the data in the Sideband MSG data area. When cleared to 0, intermediate DP nodes along the message transaction path may still need to modify the data within the Sideband MSG data area, but the data is only targeted for the target MST DP node. All MST DP nodes along the Sideband MSG path must modify the relative address and Link Count Remaining fields (LCR) as stated in Section 2.11.3.1.3 and Section 2.11.3.1.2, respectively, regardless of the state of the Path_Message bit. A DP device can only execute one path message at a time regardless of the source of the message.

2.11.3.1.8 Message_Sequence_No

The Message_Sequence_No (MSN), bit identifies individual Message Transactions to a given DP device. A DP Message Transaction originator cannot send two Message Transactions with the same MSN to the same DP device without a reply to the first Message Transaction being received first.

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2.11.3.1.9 Sideband_MSG_Header_CRC

The result of a CRC-4 calculation over the Sideband_MSG_Header starts with the Link_Count_Total and ends with the Message_Sequence_No field. The polynomial for the CRC-4 is $x^4 + x + 1$. The CRC-4 calculation is defined below.

```
uint8_t crc4(const uint8_t * data, size_t NumberOfNibbles)
{
      uint8_t    BitMask          = 0x80;
      uint8_t    BitShift         = 7;
      uint8_t    ArrayIndex       = 0;
      int        NumberOfBits     = NumberOfNibbles * 4;
      uint8_t    Remainder        = 0;

      while (NumberOfBits != 0)
      {
            NumberOfBits--;

            Remainder <<= 1;
            Remainder |= (data[ArrayIndex] & BitMask) >> BitShift;

            BitMask >>= 1;
            BitShift--;

            if (BitMask == 0)
            {
                  BitMask = 0x80;
                  BitShift = 7;
                  ArrayIndex++;
            }

            if ((Remainder & 0x10) == 0x10)
            {
               Remainder ^= 0x13;
            }
      }

      NumberOfBits = 4;
      while (NumberOfBits != 0)
      {
            NumberOfBits--;

            Remainder <<= 1;

            if ((Remainder & 0x10) != 0)
            {
               Remainder ^= 0x13;
            }
      }

      return Remainder;
}
```


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2.11.3.2 Sideband_MSG_Body()

The Sideband MSG body contains the data to be transferred between MST DP nodes. The Sideband MSG protocol does not examine the contents of the Sideband MSG body. The Sideband MSG body syntax is shown in Table 2-184.

Table 2-184: Sideband MSG Body Syntax

Syntax	# of Bits
`Sideband_MSG_Body()`	
`{`	
`  for (i = 0; i < Sideband_MSG_Body_Length - 1; i++)`	
`  {`	
`  Sideband_MSG_Data`	8
`  }`	
`  Sideband_MSG_Data_CRC`	8
`}`	

2.11.3.2.1 Sideband_MSG_Data

The Sideband MSG data contains the information to be transferred from one DP node to another. The Sideband_MSG_Body_Length field specifies the number of data bytes in the Sideband MSG body. The number of data bytes is the value of the Sideband_MSG_Body_Length field minus one.

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2.11.3.2.2 Sideband_MSG_Data_CRC

The result of a CRC-8 calculation over the Sideband_MSG_Data field of the Sideband_MSG_Body. The polynomial for the CRC-8 is $x^8 + x^7 + x^6 + x^4 + x^2 + 1$. The CRC-8 calculation is defined below.

```
uint8_t crc4(const uint8_t * data, uint8_t NumberOfBytes)
{
      uint8_t    BitMask          = 0x80;
      uint8_t    BitShift         = 7;
      uint8_t    ArrayIndex       = 0;
      uint16_t   NumberOfBits     = NumberOfBytes * 8;
      uint16_t   Remainder        = 0;

      while (NumberOfBits != 0)
      {
            NumberOfBits--;

            Remainder <<= 1;
            Remainder |= (data[ArrayIndex] & BitMask) >> BitShift;

            BitMask >>= 1;
            BitShift--;

            if (BitMask == 0)
            {
                  BitMask = 0x80;
                  BitShift = 7;
                  ArrayIndex++;
            }

            if ((Remainder & 0x100) == 0x100)
            {
                  Remainder ^= 0xD5;
            }
      }

      NumberOfBits = 8;
      while (NumberOfBits != 0)
      {
            NumberOfBits--;

            Remainder <<= 1;

            if ((Remainder & 0x100) != 0)
            {
                  Remainder ^= 0xD5;
            }
      }

      return Remainder & 0xFF;
}
```


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2.11.4 AUX Support for Messaging AUX Client

Sideband MSG packets move from MST DP node to node, using Native AUX read and write transactions. In the following sub-sections, AUX is used to indicate AUX transactions.

2.11.4.1 Messaging AUX Client DPCD Locations

See Section 2.9 for the following DPCD locations associated with the Messaging AUX client.

2.11.4.1.1 MST_CAP Bit of the MSTM_CAP DPCD Location

The MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) specifies whether the MST DPRX device supports the Messaging framework. If the DPRX indicates it supports the Messaging framework, it must be ready to accept Message Transactions from an MST DPTX.

2.11.4.1.2 UP_REQ_EN Bit of the MSTM_CTRL DPCD Location

The UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) specifies whether the MST DPTX device accepts and responds to UP Sideband MSGs. Once the MST DPTX sets the UP_REQ_EN bit to 1, it must be ready to accept and reply to Message Transactions from an MST DPRX.

2.11.4.1.3 DOWN_REP_MSG_RDY Bit of the DEVICE_SERVICE_IRQ_VECTOR DPCD Location

The MST DPRX device sets the DOWN_REP_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 4) to 1 after a valid Sideband DOWN_REP_MSG is written to the DOWN_REP DPCD locations. Once the DOWN_REP_MSG_RDY bit is set, the MST DPRX issues an IRQ_HPD to the connected MST DPTX.

When the MST DPTX device detects the IRQ_HPD, the MST DPTX reads the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers checking whether the DOWN_REP_MSG_RDY bit is set to 1. If the DOWN_REP_MSG_RDY bit is set to 1, the Sideband DOWN_REP_MSG is read from the MST DPRX DOWN_REP DPCD locations. The DPTX device must clear the DOWN_REP_MSG_RDY bit to 0 when reading of the message is complete.

The MST DPTX device is not required to wait for the IRQ_HPD signal. The MST DPTX device can poll the appropriate MST DPRX device DPCD locations to determine if any action is required. The MST DPRX is required to generate the IRQ_HPD signal regardless of whether the MST DPTX device supports detecting the IRQ_HPD signal.

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2.11.4.1.4 UP_REQ_MSG_RDY bit of the DEVICE_SERVICE_IRQ_VECTOR DPCD Location

The MST DPRX device sets the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) to 1 after a valid Sideband UP_REQ_MSG is written to the MST UP_REQ DPCD locations. Once the UP_REQ_MSG_RDY bit is set, the MST DPRX issues an IRQ_HPD to the connected MST DPTX.

When the MST DPTX device detects the IRQ_HPD, the MST DPTX reads the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers checking whether the UP_REQ_MSG_RDY bit is set to 1. If the UP_REQ_MSG_RDY bit is set to 1, the Sideband UP_REQ_MSG is read from the MST DPRX UP_REQ DPCD locations. The MST DPTX device must clear the UP_REQ_MSG_RDY bit to 0 when reading of the message is complete.

The MST DPTX device is not required to support detecting of the IRQ_HPD signal. The MST DPTX device can poll the appropriate MST DPRX device DPCD locations to determine if any action is required. The MST DPRX is required to generate the IRQ_HPD signal regardless of whether the MST DPTX device supports detecting the IRQ_HPD signal.

2.11.4.1.5 DOWN_REQ Sideband MSG Buffer

The Sideband DOWN_REQ Sideband MSG buffer holds the request Sideband MSG written by a MST DPTX device to be processed by the MST DPRX device. The first byte of every DOWN_REQ Sideband MSG is written to the start address of the DOWN_REQ Sideband MSG buffer. An MST DP Sink device is required to support the DOWN_REQ and DOWN_REP Sideband MSG buffers (DOWN_REQ and DOWN_REP registers (DPCD Addresses 01000h through 011FFh and 01400h through 015FFh, respectively)) if it expects to receive data on the Main-Link using MST packets. All MST DP Branch devices must support the DOWN_REQ Sideband MSG buffer for each MST DPRX.

2.11.4.1.6 UP_REP Sideband MSG Buffer

The UP_REP Sideband MSG buffer holds the reply Sideband MSG written by a MST DPTX device to be processed by the MST DPRX device. The first byte of every UP_REP Sideband MSG is written to the start address of the UP_REP Sideband MSG buffer. An MST DP Sink device is not required to support the UP_REQ and UP_REP Sideband MSG buffers (UP_REQ and UP_REP registers (DPCD Addresses 01600h through 017FFh and 01200h through 013FFh, respectively) if it does not originate Sideband MSG transactions. All MST DP Branch devices must support the UP_REP Sideband MSG buffer for each MST DPRX.

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2.11.4.1.7 DOWN_REP Sideband MSG Buffer

The Sideband DOWN_REP Sideband MSG buffer holds the reply Sideband MSG written by a MST DPRX device to be processed by the MST DPTX device. The first byte of the Sideband MSG containing the beginning of the Message Transaction is written to the start address of the DOWN_REP Sideband MSG DPCD. An MST DP Sink device is required to support the DOWN_REP Sideband MSG buffer (DOWN_REP registers (DPCD Addresses 01400h through 015FFh) if it expects to receive data on the Main-Link using MST packets. All MST DP Branch devices must support the DOWN_REP Sideband MSG buffer for each MST DPRX.

2.11.4.1.8 UP_REQ Sideband MSG Buffer

The Sideband UP_REQ Sideband MSG buffer holds the request Sideband MSG written by a MST DPRX device to be processed by the MST DPTX device. The first byte of the Sideband MSG containing the beginning of the Message Transaction is always written to the start address of the UP_REQ Sideband MSG DPCD. An MST DP Sink device is required to support the UP_REQ Sideband MSG buffer and corresponding UP_REP Sideband MSG buffer (UP_REQ and UP_REP registers (DPCD Addresses 01600h through 017FFh and 01200h through 013FFh, respectively) if the DP Sink device supports UP_REQ Sideband MSG transactions. All MST DP Branch devices must support the UP_REQ Sideband MSG buffer for each MST DPRX.

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2.11.5 RAD Updated by MST Devices in the Path

The RAD is an array of nibbles of size Link_Count_Total - 1 contained in Sideband MSG Header as described in Section 2.11.3.1. Each nibble of the Relative_Address field specifies the port number of each DPTX or DPRX node to which the message is being sent. When the message arrives at a DP node, Relative_Address[0] is the port number of the DPTX or DPRX within the node to send the message. Relative_Address[0] is the first port number sent as part of the RAD. Each node modifies the Relative_Address array as described with the following code sample:

```
for (i = 0; i < Link_Count_Remaining - 1; i++)
{
        Relative_Address[i] = Relative_Address[i + 1];
}
Relative_Address[i] = Input_Port_Number;
```

When the Sideband MSG arrives at the target DP node, the Relative_Address array contains the relative address of the Sideband MSG originator. Figure 2-120 shows an example of how the RAD is modified as a message traverses the path from originator to target.

Message from Source Device 2 to Branch Device 3 (LCT = 3)

Message arriving at	Relative Address	Link Count Remaining
Branch Device 1	2.2	2
Branch Device 2	2.0	1
Branch Device 3	1.0	0

Figure 2-120: RAD Update Along the Path Using Example Topology

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2.11.6 Broadcast Message Transactions

The Sideband MSG protocol supports the transmission of Broadcast Message Transactions.

2.11.6.1 Broadcast Message Syntax

A Sideband MSG with a Broadcast_Message Sideband MSG Header bit set is defined to be a "broadcast message." Broadcast messages are delivered one link at a time until the message reaches an end MST DP device. A Broadcast Sideband MSG does not have a RAD; the LCT equals 1 and the LCR equals 6. As the broadcast message is transmitted from one MST DP device to another, the LCR value is decremented by one. A broadcast message with an LCR of zero is removed, not transmitted to adjacent DP device. This mechanism removes broadcast messages when the topology contains loops.

Broadcast message may be either downward going (originated by an upstream MST DP device) or upward going (originated by a downstream MST DP device). When the broadcast message is received from an upstream-facing port (UFP), it is to be sent out all DFPs. Conversely, if the broadcast message is received from a DFP, the message is sent out all UFPs.

A broadcast message can be a path or node request depending upon the value of the Path_Message bit of the Sideband MSG header. If the broadcast message is a node request, only the end devices, MST DP Source or Sink devices process the request (or MST DP Branch devices if Source/Sink devices are not plugged). If the broadcast message is a path request, all MST DP devices which receive the broadcast message must process the request.

2.11.6.2 Broadcast Message Reply

Broadcast Message Transactions (consisting of one or multiple broadcast messages) must be replied to by the adjacent MST DP device receiving the message. The validity of the Sideband MSG header is verified along with the validity of the Sideband MSG body CRC. If an error is found, a NAK message is sent to the transmitter of the message indicating the error found. The adjacent MST DP device must retry forwarding broadcast message five times before replying with NAK. The transmitter resolves the error and sends the message again. If no error is found, an ACK reply is sent to the transmitter and no further action is required by the transmitter.

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2.11.7 Message Delivery

The procedures and requirements for delivering Sideband MSGs from one DP device to another are described in the following sections. The procedures and requirements are given based upon whether the DP device is the message originating device, message target device, or message forwarding device.

2.11.7.1 Message Originating Device

2.11.7.1.1 Down Request Message

The originator first ensures it has not sent a Message Transaction to the same DP device with the next Message Sequence Number (MSN). If a reply has not been received from the two previous Message Transaction requests, wait for a reply or timeout from one of the two outstanding requests. Use the freed MSN for the Message Transaction to be sent. If there is a requirement that Message Transactions are executed in a defined order, it is the responsibility of the originator to ensure the Message Transaction execution by waiting for a reply before sending subsequent messages.

The Message Transaction request is split into the required number of Sideband MSGs. The SMT bit is set in the Sideband MSG header of the first Sideband MSG of the Message Transaction request, and the EMT bit is set in the Sideband MSG header of the last Sideband MSG. If the Message Transaction request can be delivered with one Sideband MSG, the SMT and EMT bits are set in the Sideband MSG header.

The originating device will attempt to write the first Sideband MSG into the DPCD DOWN_REQ Sideband MSG buffer using Native AUX requests. If the receiving device replies with an AUX_DEFER, retry sending the Sideband MSG an implementation-specific number of times. If the receiving device replies with an AUX_ACK, continue writing the remaining Message Transaction Sideband MSGs. Wait four seconds for a reply from the target after successfully writing the last Message Transaction Sideband MSG.

2.11.7.1.2 Up Request Message

If a reply has not been received from the two previous Message Transaction requests, wait for a reply or timeout from one of the two outstanding requests. Use the freed MSN for the Message Transaction to be sent. The originator is responsible for ensuring that messages are executed in a given order by waiting for a reply before sending subsequent messages.

The Message Transaction request is split into the required number of Sideband MSGs. The SMT bit is set in the Sideband MSG header of the first Sideband MSG of the Message Transaction request, and the EMT bit is set in the Sideband MSG header of the last Sideband MSG. If the Message Transaction request can be delivered with one Sideband MSG, the SMT and EMT bits are set in the Sideband MSG header.

The originating device will write the first Sideband MSG into the DPCD UP_REQ Sideband MSG buffer, write 1 to the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) and then generate an IRQ_HPD to the upstream DP device. After 110ms, or after the upstream DP device writes 0 to the UP_REQ_MSG_RDY bit, ensure that the UP_REQ_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD UP_REQ Sideband MSG buffer. The originating DP device waits 4s for a reply after the upstream DP device reads the last Message Transaction Sideband MSG.

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2.11.7.2 Message Forwarding Device (Forward and Execute if Path Message)

2.11.7.2.1 Down Request Message Transaction

If there are at least 48 bytes available for reception of a Sideband MSG, reply with an AUX_ACK to the Native AUX request to write a Sideband MSG into the DPCD DOWN_REQ Sideband MSG buffer. If there is not 48 bytes free when the first Sideband MSG Native AUX write request is performed, reply with an AUX_DEFER until 48 bytes are available.

After the last Sideband MSG Native AUX write, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, attempt to write the Sideband MSG to the DPCD DOWN_REQ Sideband MSG buffer of the downstream DP device using Native AUX requests. After attempting to forward for 20ms, reply to the Message Transaction originator with a Message Transaction NAK reply.

If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After executing the Message Transaction, attempt to write the Sideband MSG to the DPCD DOWN_REQ Sideband MSG buffer of the downstream DP device using Native AUX requests. After attempting to forward for 20ms, reply to the Message Transaction originator with a Message Transaction NAK reply.

See Section 2.11.7.3.1 for handling of Node Message Transactions targeted for this DP device.

2.11.7.2.2 Down Reply Message Transaction

Upon detecting an IRQ_HPD, send Native AUX requests to read the DOWN_REP_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 4) to determine if a Down Reply Message Transaction must be read. If a down reply is available, read the reply from the DPCD DOWN_REP Sideband MSG buffer, then clear the DOWN_REP_MSG_RDY bit within 100ms of receiving the IRQ_HPD. The downstream DP device will clear the DOWN_REP_MSG_RDY bit and Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer after 110ms from the end of the IRQ_HPD pulse.

After the last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, write the Sideband MSG to the DPCD DOWN_REP Sideband MSG buffer, write 1 to the DOWN_REP_MSG_RDY bit, then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the DOWN_REP_MSG_RDY bit, ensure that the DOWN_REP_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer.

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If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. Once execution is complete, write the Message Transaction Sideband MSG to the DOWN_REP Sideband MSG buffer, write 1 to the DOWN_REP_MSG_RDY bit and then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the DOWN_REP_MSG_RDY bit, ensure that the DOWN_REP_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer.

2.11.7.2.3 Up Request Message Transaction

Upon detecting an IRQ_HPD, send Native AUX requests to read the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) to determine if an Up Request Message Transaction must be read. If an up request is available, read the request Sideband MSG from the DPCD UP_REQ Sideband MSG buffer and clear the UP_REQ_MSG_RDY bit within 100ms of receiving the IRQ_HPD. The downstream DP device will clear the UP_REQ_MSG_RDY bit and Sideband MSG from the DPCD UP_REQ Sideband MSG buffer after 110ms from the end of the IRQ_HPD pulse.

After last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, write the Sideband MSG to the DPCD UP_REQ Sideband MSG buffer, write 1 to the UP_REQ_MSG_RDY bit, then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the UP_REQ_MSG_RDY bit, ensure that the UP_REQ_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD UP_REQ Sideband MSG buffer.

If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. Once execution is complete, write the Message Transaction Sideband MSG to the UP_REQ Sideband MSG buffer, write 1 to the UP_REQ_MSG_RDY bit, then generate an IRQ_HPD within 5ms of last Sideband MSG Native AUX read request. After 110ms or after the upstream DP device writes 0 to the UP_REQ_MSG_RDY bit, ensure that the UP_REQ_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD UP_REQ Sideband MSG buffer. If the Up Request Message Transaction Sideband MSG was not read within 110ms by the upstream DP device, send a Message Transaction NAK to the originating device.

See Section 2.11.7.3.2 for handling of Up Node Message Transactions targeted for this DP device.

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2.11.7.2.4 Up Reply Message Transaction

If there are at least 48 bytes available for reception of a Sideband MSG, reply with an AUX_ACK to the Native AUX request to write a Sideband MSG into the DPCD UP_REP Sideband MSG buffer. If there are not 48 bytes free when the first Sideband MSG Native AUX write request is performed, reply with an AUX_DEFER until 48 bytes are available.

After the last Sideband MSG Native AUX write, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is to be forwarded, attempt to write the Sideband MSG to the DPCD UP_REP Sideband MSG buffer of the downstream DP device using Native AUX requests. Timeout after attempting to forward for 20ms and discard the Sideband MSG.

If the Sideband MSG is part of a Path Message Transaction, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After executing the Message Transaction, attempt to write the Sideband MSG reply to the DPCD UP_REP Sideband MSG buffer of the downstream DP device using Native AUX requests. Timeout after attempting to write the Message Transaction Sideband MSG reply for 20ms and discard the Message Transaction Sideband MSGs.

2.11.7.3 Message Targeted Device

2.11.7.3.1 Down Request Message

If there are at least 48 bytes available for reception of a Sideband MSG, reply with an AUX_ACK to the Native AUX request to write a Sideband MSG into the DPCD DOWN_REQ Sideband MSG buffer. If there are not 48 bytes free when the first Sideband MSG Native AUX write request is performed, reply with an AUX_DEFER until 48 bytes are available.

After last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is part of a Node Message Transaction to be executed locally, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. Once execution is complete, write the Message Transaction reply Sideband MSG to the DOWN_REP Sideband MSG buffer, write 1 to the DOWN_REP_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 4) and generate an IRQ_HPD within 5ms of the last Sideband MSG Native AUX read request. After 110ms, or after the upstream DP device writes 0 to the DOWN_REP_MSG_RDY bit, ensure that the DOWN_REP_MSG_RDY bit is cleared before removing the Sideband MSG from the DPCD DOWN_REP Sideband MSG buffer. If the Down Reply Message Transaction Sideband MSG is not read within 110ms by the upstream DP device, send a Message Transaction NAK to the originating device.

If the Message Transaction reply has to be sent using multiple Sideband MSGs, send the Sideband MSGs as soon as there is sufficient data to fill each Sideband MSG. Especially in the case of an I^2C read, send the Sideband MSGs as soon as there is sufficient data to fill a Sideband MSG without waiting for the entire I2C data to be read.

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2.11.7.3.2 Up Request Message

Upon detecting an IRQ_HPD, send Native AUX requests to read the UP_REQ_MSG_RDY bit in the DEVICE_SERVICE_IRQ_VECTOR and DEVICE_SERVICE_IRQ_VECTOR_ESI0 registers (DPCD Addresses 00201h and 02003h, respectively, bit 5) to determine if an Up Request Message Transaction must be read. If an up request is available, read the request Sideband MSG from the DPCD UP_REQ Sideband MSG buffer and then clear the UP_REQ_MSG_RDY bit within 100ms of receiving the IRQ_HPD. The downstream DP device will clear the UP_REQ_MSG_RDY bit and Sideband MSG from the DPCD UP_REQ Sideband MSG buffer after 110ms from the end of the IRQ_HPD pulse.

After last Sideband MSG Native AUX read, check the validity of the Sideband MSG header by validating the Sideband MSG Header CRC. Check the LCR and Path bit to determine whether the Sideband MSG is to be forwarded or is part of a Message Transaction request to be executed locally. If the Sideband MSG is part of a Node Message Transaction request to be executed locally, combine this Sideband MSG with any other Sideband MSGs for the same Message Transaction until the EMT Sideband MSG Header bit is set. After receiving the last Message Transaction Sideband MSG, execute the Message Transaction within 50ms. After executing the Message Transaction, attempt to write the Sideband MSG reply to the DPCD UP_REP Sideband MSG buffer of the downstream DP device using Native AUX requests. Timeout after attempting to write the Message Transaction Sideband MSG reply for 20ms and discard the Message Transaction Sideband MSGs.

If the Message Transaction reply has to be sent using multiple Sideband MSGs, send the Sideband MSGs as soon as there is sufficient data to fill each Sideband MSG. Especially in the case of an I^2C read, send the Sideband MSGs as soon as there is sufficient data to fill a Sideband MSG without waiting for the entire I^2C data to be read.

2.11.8 Error Handling

This section describes the error handling of Messaging AUX Client layers.

2.11.8.1 Message Transaction Layer Error Handling

Other than errors in the Sideband MSG header, errors must be detected and handled at the Message Transaction Layer. These errors include invalid request syntax, unable to respond to request within required timeout period, and request execution errors. The DP node detecting one or more of the above errors will reply to the originator with a NAK reply. The NAK reply will indicate the type of error detected. The Message Transaction originator must perform the reply timeout check. If an error to a request causes the system to be in an invalid state (e.g., all nodes failed to delete a virtual channel, it is the responsibility of the Message Transaction originator to return the system to a valid state). The Message Transaction originator is responsible for any retries.

2.11.8.2 Sideband MSG Layer Error Handling

Sideband MSG Layer must validate the CRC of the Sideband MSG header. If an error is detected in the Sideband MSG header, all Sideband MSG transactions up to, but not including, a Sideband MSG with the Start_Of_Message_Transaction bit of the Sideband MSG Header set to 1. This action causes the Sideband MSG originator to timeout. Upon timeout, the originator Sideband MSG Layer must inform the Message Transaction Layer of the timeout event. No retries are performed at the Sideband MSG Layer.

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2.11.8.3 AUX Layer Error Handling for Sideband MSG

No changes are made to the AUX transactions to support Sideband Messaging.

2.11.8.3.1 AUX Error Handling for Down Message Transactions

The AUX Layer of the DPTX uses Native AUX write transactions to write the Sideband MSG into the appropriate DPRX Down Sideband MSG buffer.

When the Native AUX write is unsuccessful within the number of retries allowed, the Sideband MSG Layer must notify the Message Transaction Layer of the failure. This would be the case when the message buffer is full. The Message Transaction Layer, in turn, should send a Message Transaction NAK to the message originator (e.g., Stream Policy Maker) indicating a Write_Failure occurred.

Figure 2-121: AUX Error While Delivering a Down Req Message

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2.11.8.3.2 AUX Error Handling for Up Message Transactions

The AUX layer of the DPRX generates an IRQ_HPD to prompt its immediate upstream DP node to initiate Native AUX read transactions and instruct the DPTX to read the Sideband MSG from the appropriate DPRX Up Sideband MSG buffer.

When the DPTX does not have sufficient room in its internal buffers to read the Sideband MSG, the DPTX must inform its Message Transaction Layer of the failure. The Message Transaction Layer, then, must send a Message Transaction NAK Reply to the message originator indicating a Write_Failure occurred.

Figure 2-122: AUX Error While Delivering an Up Req Message

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2.11.9 Descriptions of Available Message Transaction Requests

This section describes the available Message Transactions Requests.

2.11.9.1 ALLOCATE_PAYLOAD

The ALLOCATE_PAYLOAD is a path or node request Message Transaction allowing the change of payload allocation for a virtual channel between a DP Source and Sink device. The ALLOCATE_PAYLOAD request is used to allocate a payload for a new virtual channel, change the payload allocation of an existing virtual channel or the deletion the payload allocation of an existing virtual channel.

Table 2-185: ALLOCATE_PAYLOAD Message Syntax

Syntax	# of Bits	Format
ALLOCATE_PAYLOAD_Request()		
{		'0'
zero	1	'001 0001'
Request_Identifier	7	
Port_Number	4	
Number_SDP_Streams	4	
zero	1	'0'
Virtual_Channel_Payload_Identifier	7	
Payload_Bandwidth_Number	16	
for (i = 0; i < Number_SDP_Streams; i++)		
{		
SDP_Stream_Sink[i]	4	
}		
while (!bytealigned())		
{		
zero	1	'0'
}		
}		
ALLOCATE_PAYLOAD_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'001 0001'
Port_Number	4	
zeros	5	'0000'
Virtual_Channel_Payload_Identifier	7	
Allocated_Payload_Bandwidth_Number	16	
}		

Link training will be performed on each DP node from the source to the immediate upstream node from the sink if the link needs to be established. After the DP node determines the downstream link can support the requested PBN, Native AUX transactions are used to establish the downstream virtual channel. Each DP node forwards the ALLOCATE_PAYLOAD message to the next downstream device along the path specified by the RAD after the local virtual channel set-up is complete. If the DP node changes the virtual channel payload identifier within the DP device, the new virtual channel payload identifier replaces the virtual channel payload identifier in the received ALLOCATE_PAYLOAD request. See Section 2.6.6 for usage of the ALLOCATE_PAYLOAD Message Transaction.

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The path de-allocate payload reply version of the ALLOCATE_PAYLOAD Message Transaction is converted to a node Sideband MSG when the message is received by a MST DP Branch device with the VC Payload allocated to two or more DPTX ports. When the de-allocate payload reply is a node reply, MST DP devices receiving the reply will convert the VC Payload ID in the message and pass it on to the upstream MST DP device without de-allocating the VC Payload.

2.11.9.1.1 Port_Number

The target end port number of the DP device to be the endpoint of the virtual channel. This field has the same value in reply as in the request.

2.11.9.1.2 Virtual_Channel_Payload_Identifier

The virtual channel payload identifier of the virtual channel to be added, updated, or deleted. This field has the same value in reply as in the request.

2.11.9.1.3 Payload_Bandwidth_Number

The Payload Bandwidth Number required for the virtual channel assigned the above virtual channel identifier.

2.11.9.1.4 Allocated_Payload_Bandwidth_Number

The Payload Bandwidth Number (PBN) of the time slots actually allocated to the stream. The allocated PBN is the maximum allocated by any DP MST Branching unit. As the ALLOCATE_PAYLOAD Message Transaction reply is forwarded upstream, each DP MST branching unit replaces the Allocated_Payload_Bandwidth_Number with its allocated PBN if its allocated PBN is greater than the PBN in the reply.

2.11.9.1.5 Number_SDP_Streams

The Number_SDP_Streams field indicates the number of SDP streams which need to be routed to SDP stream sinks (the size of the SDP stream sink table which follows).

2.11.9.1.6 SDP_Stream_Sink

The SDP Stream Sink table contains the mapping of the SDP stream to the available SDP stream sinks. The first field of the table is associated with the first SDP stream, the second field the second SDP stream and so forth. The value of each field in the table is the SDP stream sink identifier to which the associated SDP stream is being sent. When the SDP_Stream_Sink value is cleared to 0, the destination SDP Sink device the SDP stream is sent is implementation-specific. It is the decision of the DP Sink device implementer as to how to handle two SDP streams assigned to the same SDP stream sink.

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2.11.9.2 CLEAR_PAYLOAD_ID_TABLE

The CLEAR_PAYLOAD_ID_TABLE path broadcast request message transaction is sent by a MST DP device to de-allocate all VC Payload Id. tables allocated to the port the message is received from. This broadcast message is not sent to all DFPs. The broadcast message is sent to those DPTX ports with VC Payloads allocated from the DPRX port being cleared. When the CLEAR_PAYLOAD_ID_TABLE request is received by a concentrator device, the MST DP Concentrator Branch device sends a NAK reply with the reason set to defer.

The MST DP Concentrator Branch device, ACKs CLEAR_PAYLOAD_ID_TABLE broadcast request message transactions, and converts the CLEAR_PAYLOAD_ID_TABLE request into a series of ALLOCATE_PAYLOAD requests for the VC Payload ID allocated to the DPRX port with the new PBN value cleared to 0 (de-allocate payload) to its downstream DPTX ports.

Table 2-186: CLEAR_PAYLOAD_ID_TABLE Message Syntax

Syntax	# of Bits	Format
CLEAR_PAYLOAD_ID_TABLE_Request()		
{		
zero	1	'0'
Request_Identifier	7	'001 0100'
}		
CLEAR_PAYLOAD_ID_TABLE_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'001 0100'
}		

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2.11.9.3 CONNECTION_STATUS_NOTIFY

The CONNECTION_STATUS_NOTIFY node broadcast request message transaction is sent by a DP branch device when it detects a DP or legacy device plug or unplug event. The MST device whose DPTX detected the connection status change will broadcast the message upstream, while the MST device whose DPRX detected the connection status change will broadcast the message downstream. All payloads allocated to the disconnected DP ports will be de-allocated as the broadcast message traverses both upstream and downstream.

The MST device with a branching unit whose DPRX detects the disconnect event must clear the VC Payload ID table of the disconnected DPRX port while maintaining VC Payload ID tables of other DPRX/DPTX ports and initiate ALLOCATE_PAYLOAD procedure to its downstream DP nodes to delete the VC Payloads allocated on the disconnected port, see Section 2.6.

The MST device with a branching unit whose DPTX detects the disconnect must clear the VC Payload ID table of the DPTX while maintaining those of the other DPTX/DPRX ports.

Table 2-187: CONNECTION_STATUS_NOTIFY Message Syntax

Syntax	# of Bits	Format
CONNECTION_STATUS_NOTIFY_Request()		
{		
zero	1	'0'
Request_Identifier	7	'000 0010'
Port_Number	4	
zeros	4	'0000'
Global_Unique_Identifier	128	
zero	1	'0'
Legacy_Device_Plug_Status	1	
DisplayPort_Device_Plug_Status	1	
Messaging_Capability_Status	1	
Input_Port	1	
Peer_Device_Type	3	
}		
CONNECTION_STATUS_NOTIFY_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'000 0010'
}		

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2.11.9.3.1 Global_Unique_Identifier

The Global Unique Identifier (GUID), of DP device sending the CONNECTION_STATUS_NOTIFY Message Transaction.

2.11.9.3.2 Port_Number

The port number on which the connection event was detected.

2.11.9.3.3 Legacy_Device_Plug_Status

This bit is valid if the Peer_Device_Type is set to SST-to-Legacy converter and the DisplayPort_Device_Plug_Status bit is set to 1. This bit indicates the connection status of the legacy device (VGA, DVI, or HDMI device). When the Legacy_Device_Plug_Status bit is set to 1, the legacy device is connected. The Legacy_Device_Plug_Status bit is cleared to 0 when the legacy device is disconnected. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.11.9.3.4 DisplayPort_Device_Plug_Status

When set to 1, the DPTX or DPRX is connected to an appropriate micro-packet device and the DPTX or DPRX is initialized.

2.11.9.3.5 Messaging_Capability_Status

When set to 1, the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is enabled for the DPRX unit and the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is enabled by a DPTX unit. The bit is cleared to 0 if the DPCD MST_CAP or UP_REQ_EN bit is disabled. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.11.9.3.6 Input_Port

When set to a one, the port information is for a DPRX; otherwise, the port information is for a DPTX.

2.11.9.3.7 Peer_Device_Type

Peer_Device_Type gives the DP device type connected to the indicated port. Table 2-188 defines the available device types. The Peer_Device_Type number of 010 will be returned for an SST Branch device connected to a DFP and for a DP device with MST Branching unit whether the Branching unit is a part of an MST Branch device, MST Composite Sink device, or MST Sink device.

Table 2-188: Peer Device Type

Peer_Device_Type	DP Peer Device Description
000	No device connected
001	Source device or SST Branch device connected to a UFP
010	Device with MST Branching Unit or SST Branch device connected to a DFP
011	SST Sink device or Stream Sink in an MST Sink/Composite device
100	DP-to-Legacy converter (DP to VGA, DVI, or HDMI)
101	DP-to-Wireless converter (DP to WDE or other wireless interfaces)
110	Wireless-to-DP converter (WDE or other wireless interface to DP)
111	RESERVED

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Table 2-189 provides information on how to determine the Peer_Device_Type and Messaging_Capability_Status fields from the cable plug status and DPCD status.

Table 2-189: Peer_Device_Type Determination[a]

Peer Device Connected to	Peer Device Description	Message Capability/Type		Signal Used for Presence Detection	DPCD Bits Used for Peer_Device_Type Determination			
		Message_Capability_Status	Peer_Device_Type		DFP_PRESENT[b]	DFP_TYPE[c]	MST_CAP/UP_REQ_EN[d]	UPSTREAM_IS_SRC[e]
N/A	None	0	000	No	X	X	X	X
UFP	MST Source Device	1	001	Powered Source Detect	0	X	UP_REQ_EN=1	1
UFP	SST-only Source Branch Device	0	001	Powered Source Detect	0	X	UP_REQ_EN=0	0
	MST Branch Device	1	010	Powered Source Detect	0	X	UP_REQ_EN=1	0
DFP	SST-only Branch Device (DP out)	0	010	HPD	1	00	MST_CAP=0	X
	Device with MST Branching Unit	1	010	HPD	1	00	MST_CAP=1	X
	DP-to-Legacy Converter	0	100	HPD	1	01=VGA 10=DVI/HDMI	0	X
	Stream Sink (without Branching Unit)	0	011	HPD	0	X	0	X
	DP-to-Wireless Converter	1	101	HPD	1	110	1	X
	Wireless-to-DP Converter	1	110	Completion of wireless pairing (beyond the scope of this Standard)	1	110	1	X

a. "X" indicates "don't care."
b. DFP_PRESENT bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 0).
c. DFP_TYPE field in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bits 2:1).

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d. *MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) and UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1).*
e. *UPSTREAM_IS_SRC bit in the MSTM_CTRL register (DPCD Address 00111h, bit 2).*

2.11.9.4 ENUM_PATH_RESOURCES

ENUM_PATH_RESOURCES is a path request message transaction used to determine the minimum available PBN of a path from the DP Source to Sink device.

Table 2-190: ENUM_PATH_RESOURCES Message Syntax

Syntax	# of Bits	Format
ENUM_PATH_RESOURCES_Request()		
{		
zero	1	'0'
Request_Identifier	7	'001 0000'
Port_Number	4	
zeros	4	'0000'
}		
ENUM_PATH_RESOURCES_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'001 0000'
Port_Number	4	
zeros	3	'000'
FEC_Capability	1	
Full_Payload_Bandwidth_Number	16	
Available_Payload_Bandwidth_Number	16	
}		

This message is targeted at the downstream DP Branch device of the path to be enumerated. The targeted DP device responds with its downstream available PBN. Each DP node along the path of the reply message replaces the available PBN in the reply message with its available downstream PBN if its available downstream PBN is less than that in the reply message.

2.11.9.4.1 FEC_Capability

New to *DP v1.4*.

Set to 1 if the path from the MST BU that is generating the reply message to the downstream end of the path to be enumerated supports Forward Error Correction (FEC) capability.

2.11.9.4.2 Full_Payload_Bandwidth_Number

The bandwidth of the link at the trained link rate and lane count between the DP Source device and the DP Sink device with no time slots allocated to VC Payloads, represented as a Payload Bandwidth Number. As with the Available_Payload_Bandwidth_Number, this number is determined by the link with the lowest lane count and link rate.

2.11.9.4.3 Available_Payload_Bandwidth_Number

The minimum payload bandwidth number supported by the path. Each node updates this number with its available payload bandwidth number if its payload bandwidth number is less than that in the Message Transaction reply.

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2.11.9.4.4 Port_Number

The target port number of the MST DP device to be enumerated.

2.11.9.5 LINK_ADDRESS

The LINK_ADDRESS node message transaction is targeted at MST devices with a branching unit. This transaction is used to determine the resources available of a particular MST device with a branching unit, and the type of devices connected to the branching unit (Peer_Device_Type). The resources reported by an MST device with a branching unit are the number of input and output ports (both physical and logical), whether a peer device is connected to the input or output port and whether the peer device is a Branch/Sink/Source (Peer_Device_Type) device, and if the device is a Sink device, how many SDP stream sinks are available, and whether the peer device supports topology enhancement.

As for the Current Capabilities Definition, see Table 2-129. The Current Capabilities Definition field is available only if the sideband message version number is 02h or larger.

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Table 2-191: LINK_ADDRESS Message Syntax

Syntax	# of Bits	Format
LINK_ADDRESS_Request()		
{		
zero	1	'0'
Request_Identifier	7	'000 0001'
}		
LINK_ADDRESS_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'000 0001'
Global_Unique_Identifier	128	
zeros	4	'0000'
Number_Of_Ports	4	
for (i = 0; i < Number_Of_Ports; i++)		
{		
Input_Port[i]	1	
Peer_Device_Type[i]	3	
Port_Number[i]	4	
Messaging_Capability_Status[i]	1	
DisplayPort_Device_Plug_Status[i]	1	
if (Peer_Device_Type[i] == 101b)		
{		
Current_Capabilities_Structure	128	
}		
if (Input_Port[i] == 0)		
{		
Legacy_Device_Plug_Status[i]	1	
zeros	5	'0 0000'
DPCD_Revision	8	
Peer_Global_Unique_Identifier	128	
Number_SDP_Streams[i]	4	
Number_SDP_Stream_Sinks[i]	4	
}		
else		
{		
zeros	6	'00 0000'
}		
}		
}		

2.11.9.5.1 Global_Unique_Identifier

The GUID of the targeted DP device.

2.11.9.5.2 Number_Of_Ports

The number of DPTX/DPRX units the DP node contains.

2.11.9.5.3 Current_Capabilities_Structure

The CCS of the targeted DP device.

2.11.9.5.4 Input_Port

When set to 1, the port information is for a DPRX. Otherwise, the port information is for a DPTX.

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2.11.9.5.5 Peer_Device_Type

Peer_Device_Type gives the DP device type connected to the indicated port. Table 2-188 gives the defined peer device types. The DP Peer Branch device type will be returned for all branch types, physical, logical, or combined. This field is valid if the DisplayPort_Device_Plug_Status is set to 1.

2.11.9.5.6 Port_Number

The port number of the port being reported. Physical port numbers will be from 0 to 7 while logical port numbers will be from 8 to 15 (0x0F).

2.11.9.5.7 Messaging_Capability_Status

When set to 1, the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) is enabled by a DPRX unit or the UP_REQ_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 1) is enabled by a DPTX unit. The bit is cleared to 0 if the MST_CAP or UP_REQ_EN bit is disabled. This field is valid if the DisplayPort_Device_Plug_Status is set to 1.

2.11.9.5.8 DisplayPort_Device_Plug_Status

When set to 1, the DPTX or DPRX is connected appropriately and the DPTX or DPRX is initialized.

2.11.9.5.9 Legacy_Device_Plug_Status

This bit is valid if the Peer_Device_Type is set to SST-to-Legacy converter. This bit indicates the connection status of the legacy device (VGA, DVI, or HDMI device). When the Legacy_Device_Plug_Status bit is set to 1, the legacy device is connected. The Legacy_Device_Plug_Status bit is cleared to 0 when the legacy device is disconnected. This field is valid if the DisplayPort_Device_Plug_Status is set to 1.

2.11.9.5.10 DPCD_Revision

The DPCD revision number of the DPRX of a DP device. Will be cleared to 0 if a DPRX is not connected to the port.

2.11.9.5.11 Peer_Global_Unique_Identifier

This field is valid if the DPCD revision number of the DPRX of a DP device is DPCD r1.2 (or higher). This field will contain the GUID of the DPRX device (GUID register (DPCD Addresses 00030h through 0003Fh)). This field will be cleared to 0 if the DP device's revision is less than DPCD r1.2 or a DPRX is not connected to the port.

2.11.9.5.12 Number_SDP_Streams

The Number_SDP_Streams field reports the number of SDP streams the DP port can simultaneously handle. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

2.11.9.5.13 Number_SDP_Stream_Sinks

The Number_SDP_Stream_Sinks field reports the number of SDP stream sinks associated with the DP port. This field is valid if the DisplayPort_Device_Plug_Status bit is set to 1.

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2.11.9.6 POWER_DOWN_PHY

POWER_DOWN_PHY request is a path or node request message transaction.

Table 2-192: POWER_DOWN_PHY Message Syntax

Syntax	# of Bits	Format
POWER_DOWN_PHY_Request()		
{		
zero	1	'0'
Request_Identifier	7	'010 0101'
Port_Number	4	
zeros	4	'0000'
}		
POWER_DOWN_PHY_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'010 0101'
Port_Number	4	
zeros	4	'0000'
}		

If the message is sent as a path request, all DP nodes from the DP device adjacent to the originator and the targeted DP node will be placed in the D3 power state if none of the payloads allocated to the DPTX contain stream symbol sequences. Each node's immediate upstream device will use Native AUX writes to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) to set the power state of the downstream node. The downstream node is set to the D3 state as the reply message transaction propagates upstream. When a DP device receives the acknowledge message from the downstream device, it uses Native AUX transactions to set the downstream DP device into the D3 power state before sending the ACK reply to the upstream DP device specified by the RAD. If setting the downstream to the D3 power state failed, a NAK reply is sent to the upstream DP device. The power state does not change if a NAK reply is received.

If the message is a node request, the DP node identified by the RAD will place the DP device connected to the port specified by the Port_Number parameter in the D3 power state if none of the payloads allocated to the DPTX contain active data, using a Native AUX WR to the SET_POWER & SET_DP_PWR_VOLTAGE register.

For both path and node requests, POWER_DOWN_PHY does NOT affect VC Payload ID table.

2.11.9.6.1 Port_Number

The target DFP number of the DP device to be powered down.

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2.11.9.7 POWER_UP_PHY

POWER_UP_PHY request is a path or node request message transaction.

Table 2-193: POWER_UP_PHY Message Syntax

Syntax	# of Bits	Format
POWER_UP_PHY_Request()		
{		
zero	1	'0'
Request_Identifier	7	'010 0100'
Port_Number	4	
zeros	4	'0000'
}		
POWER_UP_PHY_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'010 0100'
Port_Number	4	
zeros	4	'0000'
}		

If the message is sent as a path request, all DP nodes from the source immediate downstream device and the targeted DP node will be placed in the D0 power state. Each nodes immediate upstream device will use Native AUX writes to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) to set the power state of the downstream node.

If the message is a node request, the DP node identified by the RAD will place the DP device connected to the port specified by the Port_Number parameter in the D0 power state, using a Native AUX write to the SET_POWER & SET_DP_PWR_VOLTAGE register.

For both path and node requests, the POWER_UP_PHY does NOT affect VC Payload ID table.

2.11.9.7.1 Port_Number

The target port number of the DP device to be powered up.

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2.11.9.8 QUERY_PAYLOAD

The QUERY_PAYLOAD request determines the available payload bandwidth number for the virtual channel specified by the Virtual_Channel_Payload_Identifier parameter.

Table 2-194: QUERY_PAYLOAD Message Syntax

Syntax	# of Bits	Format
QUERY_PAYLOAD_Request()		
{		
zero	1	'0'
Request_Identifier	7	'001 0010'
Port_Number	4	
zeros	5	'0 0000'
Virtual_Channel_Payload_Identifier	7	
}		
QUERY_PAYLOAD_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'001 0010'
Port_Number	4	
zeros	4	'0000'
Allocated_PBN	16	
}		

2.11.9.8.1 Port_Number

The target port number of the DP device to be queried.

2.11.9.8.2 Virtual_Channel_Payload_Identifier

The virtual channel payload identifier of the virtual channel being queried. Each DP node updates Virtual_Channel_Payload_Identifier parameter as the request traverses.

2.11.9.8.3 Allocated_PBN

The allocated downstream payload bandwidth number for the virtual channel on the DFP specified by the QUERY_PAYLOAD request message transaction parameters.

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2.11.9.9 REMOTE_DPCD_READ

The REMOTE_DPCD_READ request reads DPCD location in the targeted DP node. Instead of directly reading DPCD of a remote DPRX, the REMOTE_DPCD_READ request is targeted to the DPTX immediately upstream to the DPRX causing the DPTX to initiate DPCD read accesses, via Native AUX transactions.

Table 2-195: REMOTE_DPCD_READ Message Syntax

Syntax	# of Bits	Format
REMOTE_DPCD_READ_Request()		
{		
zero	1	'0'
Request_Identifier	7	'010 0000'
Port_Number	4	
DPCD_Address	20	
Number_Of_Bytes_To_Read	8	
}		
REMOTE_DPCD_READ_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'010 0000'
zeros	4	'0000'
Port_Number	4	
Number_Of_Bytes_Read	8	
for (i = 0; i < Number_Of_Bytes_Read; i++)		
DPCD_Byte_Read[i]	8	
}		

2.11.9.9.1 Port_Number

The target port number of the DP device for the Native AUX transactions.

2.11.9.9.2 DPCD_Address

The 20-bit DPCD address to read or write data.

2.11.9.9.3 Number_Of_Bytes_To_Read

Number of DPCD data bytes to read starting from the DPCD address provided, incrementing the address for each byte read.

2.11.9.9.4 Number_Of_Bytes_Read

The actual number of DPCD data bytes read starting from the DPCD address given.

2.11.9.9.5 DPCD_Byte_Read

The DPCD data byte read.

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2.11.9.10 REMOTE_DPCD_WRITE

The REMOTE_DPCD_WRITE request writes data into DPCD locations in the targeted DP node. Instead of directly writing DPCD of a remote DPRX, the REMOTE_DPCD_WRITE request is targeted to the DPTX immediately upstream to the DPRX causing the DPTX to initiate DPCD write accesses, via Native AUX transactions.

Table 2-196: REMOTE_DPCD_WRITE Message Syntax

Syntax	# of Bits	Format
REMOTE_DPCD_WRITE_Request()		
{		
zero	1	'0'
Request_Identifier	7	'010 0001'
Port_Number	4	
DPCD_Address	20	
Number_Of_Bytes_To_Write	8	
for (i = 0; i < Number_Of_Bytes_Write; i++)		
DPCD_Byte_To_Write[i]	8	
}		
REMOTE_DPCD_WRITE_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'010 0001'
zeros	4	'0000'
Port_Number	4	
}		
REMOTE_DPCD_WRITE_Nak_Reply()		
{		
Reply_Type	1	'1'
Request_Identifier	7	'010 0001'
Global_Unique_Identifier	128	
Reason_For_Nak	8	
Number_Of_Bytes_Written_Before_Failure	8	
}		

2.11.9.10.1 Port_Number

The target port number of the DP device for Native AUX transactions.

2.11.9.10.2 DPCD_Address

The 20-bit DPCD address to read or write data.

2.11.9.10.3 Number_Of_Bytes_To_Read

Number of DPCD data bytes to read starting from the DPCD address provided, incrementing the address for each byte read.

2.11.9.10.4 Number_Of_Bytes_To_Write

Number of DPCD data bytes to write starting from the DPCD address given.

2.11.9.10.5 DPCD_Byte_To_Write

The DPCD data byte to write.

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2.11.9.10.6 Number_Of_Bytes_Written_Before_Failure

If the Reason_For_Nak is DPCD_Write_Failure, the Number_Of_Bytes_Written_Before_Failure field contains the number of DPCD bytes written before the failure occurred.

2.11.9.10.7 Global_Unique_Identifier

The GUID of the targeted DP device.

2.11.9.11 REMOTE_I2C_READ

The REMOTE_I2C_READ requests the I^2C location attached to a remote DP node. The REMOTE_I2C_READ request is targeted to the DPTX immediately upstream to the DPRX of a DP node to which its I^2C location is attached and causes the DPTX to initiate an I^2C-over-AUX transaction. REMOTE_I2C_READ Message Transaction is capable of transporting multiple I^2C transactions such as an I^2C write followed by an I^2C read with a repeated start.

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Table 2-197: REMOTE_I^{2}C_READ Message Syntax

Syntax	# of Bits	Format
REMOTE_I2C_READ_Request()		
{		
zero	1	'0'
Request_Identifier	7	'010 0010'
Port_Number	4	
zeros	2	'00'
Number_Of_I2C_Write_Transactions	2	
for (i = 0; i < Number_Of_I2C_Transactions; i++)		
{		
zero	1	'0'
Write_I2C_Device_Identifier[i]	7	
Number_Of_Bytes_To_Write[i]	8	
for (j = 0; j < Number_Of_Bytes_To_Write; j++)		
{		
I2C_Data_To_Write[i][j]	8	
}		
zeros	3	'000'
No_Stop_Bit[i]	1	
I2C_Transaction_Delay[i]	4	
}		
zero	1	'0'
Read_I2C_Device_Identifier	7	
Number_Of_Bytes_To_Read	8	
}		
REMOTE_I2C_READ_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'010 0010'
zeros	4	'0000'
Port_Number	4	
Number_Of_Bytes_Read	8	
for (i = 0; i < Number_Of_Bytes_Read; i++)		
I2C_Device_Byte_Read	8	
}		
REMOTE_I2C_READ_Nak_Reply()		
{		
Reply_Type	1	'1'
Request_Identifier	7	'010 0010'
Global_Unique_Identifier	128	
Port_Number	4	
zeros	4	'0000'
Reason_For_Nak	8	
zeros	6	'00 0000'
I2C_NAK_Transaction	2	
}		

See Section 2.8 for how to send I^{2}C transactions over the AUX CH.

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2.11.9.11.1 Number_Of_I2C_Write_Transactions

The total number of I^2C write transactions to be sent with this Message Transaction.

2.11.9.11.2 Port_Number

The target port number of the DP device to receive the I^2C transactions.

2.11.9.11.3 Write_I2C_Device_Identifier

The I^2C device identifier to receive the write request.

2.11.9.11.4 Number_Of_Bytes_To_Write

The number of data bytes to write to the I^2C device.

2.11.9.11.5 I2C_Data_To_Write

The I^2C write data for the write request.

2.11.9.11.6 No_Stop_Bit

When set to 1, a stop bit is not sent at the end of the I^2C transaction; otherwise, when cleared to 0, a stop will be generated at the end of the I^2C transaction.

2.11.9.11.7 I2C_Transaction_Delay

The amount of delay to insert between this and the next I^2C transaction. The delay unit is 10ms. The delay range is 0 to 150ms.

2.11.9.11.8 Read_I2C_Device_Identifier

The I^2C device identifier to receive the read request.

2.11.9.11.9 Number_Of_Bytes_To_Read

The number of data bytes requested to be read from the I^2C device.

2.11.9.11.10 Number_Of_Bytes_Read

The number of data bytes read from the I^2C device.

2.11.9.11.11 I2C_Device_Byte_Read

A data byte read from the I^2C device.

2.11.9.11.12 Global_Unique_Identifer

The GUID of the targeted DP device.

2.11.9.11.13 Reason_For_NAK

See Section 2.11.2.3.3.

2.11.9.11.14 I2C_NAK_Transaction

The I^2C transaction number in which the NAK was received. The I^2C transaction number is from 1 to 3.

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2.11.9.12 REMOTE_I2C_WRITE

The REMOTE_I2C_WRITE request writes data to the I^2C locations attached to a remote DP node. The REMOTE_I2C_WRITE request is targeted to the DPTX immediately upstream to the DPRX of a DP node to which its I^2C location is attached and causes the DPTX to initiate I^2C-over-AUX write transactions.

Table 2-198: REMOTE_I^2C_WRITE Message Syntax

Syntax	# of Bits	Format
`REMOTE_I2C_WRITE_Request()`		
`{`		
`zero`	1	'0'
`Request_Identifier`	7	'010 0011'
`Port_Number`	4	
`zeros`	5	'0 0000'
`Write_I2C_Device_Identifier`	7	
`Number_Of_Bytes_To_Write`	8	
`for (i = 0; i < Number_Of_Bytes_Write; i++)`		
`I2C_Data_To_Write`	8	
`}`		
`REMOTE_I2C_WRITE_Ack_Reply()`		
`{`		
`Reply_Type`	1	'0'
`Request_Identifier`	7	'010 0011'
`zeros`	4	'0000'
`Port_Number`	4	
`}`		

See Section 2.8 for how to send I^2C transactions over the AUX CH.

2.11.9.12.1 Port_Number

The target port number of the DP device to receive the I^2C transactions.

2.11.9.12.2 Write_I2C_Device_Identifier

The I^2C device identifier to receive the write request.

2.11.9.12.3 Number_Of_Bytes_To_Write

The number of data bytes to write to the I^2C device.

2.11.9.13 RESOURCE_STATUS_NOTIFY

The RESOURCE_STATUS_NOTIFY node broadcast request message transaction is sent when either of two events occur. One event is when the total available PBN of a link does not support the total required PBN of all allocated payloads. This condition can occur when link training occurs after payloads have been allocated and the new total available PBN value does not support the payloads allocated. After receiving this broadcast message, a DP Source can use the QUERY_PAYLOAD request to determine which streams are still allocated and which were de-allocated. If after link training, the link trains to a new total available PBN, but available PBN still supports all allocated payloads, this broadcast message is not sent as described in Section 2.6.

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The second event is when the available PBN through a MST DP Concentrator Branch device changes. For example, when the available PBN through a MST DP Concentrator Branch device changes due to the ALLOCATE_PAYLOAD request, the RESOURCE_STATUS_NOTIFY node broadcast request is sent out all DPRX ports. The RESOURCE_STATUS_NOTIFY node broadcast request message is sent in response to any request which causes a concentrator payload allocation change.

Table 2-199: RESOURCE_STATUS_NOTIFY Message Syntax

Syntax	# of Bits	Format
RESOURCE_STATUS_NOTIFY_Request()		
{		
zero	1	'0'
Request_Identifier	7	'001 0011'
Port_Number	4	
zeros	4	'0000'
Global_Unique_Identifier	128	
Available_PBN	16	
}		
RESOURCE_STATUS_NOTIFY_Ack_Reply()		
{		
Reply_Type	1	'0'
Request_Identifier	7	'001 0011'
}		

2.11.9.13.1 Global_Unique_Identifier

The GUID of DP device reporting resource change.

2.11.9.13.2 Port_Number

DPTX port number of resource change.

2.11.9.13.3 Avaliable_PBN

The newly available PBN for the port where resource allocation changed.

2.11.9.13.4 SINK_EVENT_NOTIFY

SINK_EVENT_NOTIFY is an upward-going Broadcast Message Transaction. For example, a change to a Sink device (e.g., a display) induced by an end user action, via OSD button and menu is to be communicated to a Source device (e.g., PC graphics) via SINK_EVENT_NOTIFY Broadcast Message Transaction. The syntax is to be defined in the future revision of this standard.

2.11.9.13.5 QUERY_STREAM_ENCRYPTION_STATUS

For the definition of QUERY_STREAM_ENCRYPTION_STATUS, see Appendix I.

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2.12 Audio-to-Video and Audio-to-Audio Synchronization

2.12.1 Overview

Audio-to-Video synchronization is a mechanism which synchronizes the audio stream with the video stream on a single monitor or multi-monitor/daisy chain configuration. In a multi-monitor configuration if the same audio stream is sent to multiple monitors, audio-to-audio synchronization needs to be controlled to provide a good end-user experience. This section describes a mechanism enabling both AV (audio-to-video) Sync and AA (audio-to-audio) Sync between DP Source and Sink devices. This section is applicable to Source and Sink devices which provide audio capability and all DP Branch devices.

ATSC guidelines[a] are that "The sound program should never lead the video program by more than 15ms, and should never lag the video program by more than 45ms." This tolerance level ensures good user experience while listening to media content.

DisplayPort requires that a Sink device performs the audio-to-video delay compensation internally if there is a mismatch between audio-to-video processing delays from the point at which the audio-to-video streams arrive at DP input connector. A Sink device must adhere to the guidelines specified in the ATSC specification. The audio-to-video synchronization features provided by this Standard allows synchronization of audio-to-video paths when these streams are sent to multiple devices in either a daisy-chain topology or when branch devices exist in the topology.

Sink devices must report the processing delay of audio and video through audio-video Sync Data Block (AVSDB). See Section 2.12.2 for the AVSDB specification. The Source device must read the audio and video delay data and calculate the delay compensation that is necessary to synchronize audio with video. See Section 2.12.3.2 for details on AV sync delay compensation.

Audio-to-audio delay compensation is performed when same audio stream is sent to multiple Sink devices. The Source must perform coarse delay compensation and Sink device must perform fine delay compensation. The Source must determine the coarse and fine delay values after enumerating processing/decode delay values from the various connected Sink devices. See Section 2.12.3.3 for details on audio-to-audio delay compensation.

Figure 2-123 shows an example with a Source device connected to three monitors via different ports which output audio and video through those ports. The Source device reads the processing latency of audio and video through AUX channel from the DPCD registers and sends the delay values to the higher-level application where the audio-video latency is compensated. The Source may generate audio delay values and write them to the independent display devices so that the audio delay compensation can be performed in those device endpoints.

Note: *Dependencies on the application itself exist to provide a system level solution beyond the scope of this standard, and as such all Source requirements described within this section are optional.*

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a. *www.atsc.org/standards/is_191.pdf, "ATSC Implementation Subcommittee Finding: Relative Timing of Sound and Vision for Broadcast Operations."*

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Figure 2-123: Source Device Delay Aggregation and Introduction of Delay Stamps

2.12.2 DisplayPort AV Sync Data Block

The AV Sync Data Block (AVSDB) is a set of DPCD registers which describe the Sink's audio-to-video decode and post processing delays, and additional delay insertion capability. The values reported by the Sink device must be static. The Sink device is responsible for meeting the static delay values reported and internally compensating for any variation between different modes of operation. The AVSDB is allocated to DPCD Addresses 00023h through 0002Dh.

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2.12.3 Delay Compensation

2.12.3.1 Audio Delay DPCD Register

The AUDIO_DELAY[7:0], AUDIO_DELAY[15:8], and AUDIO_DELAY[23:16] registers (DPCD Addresses 00112h through 00114h, respectively) are required in Sink devices to allow Source device-based fine-grain control of the audio path delay. The Source device will compute the additional audio delay that needs to be introduced in the Sink device and write this value to the AUDIO_DELAY-related registers. Sink devices must be responsible to add the specified additional delay on the audio path based on the delay stamp values. See Section 2.12.3.2 and Section 2.12.3.3 on how the delay stamp values are calculated.

2.12.3.2 AV Sync Delay Compensation

The Sink device must report the audio and video latency in the AVSDB if the Sink device is capable of rendering audio streams. The Source device must read the delay values and compute the necessary delay compensation. It is expected that the Sink device internally will perform the AV compensation to ensure that the audio-to-video latencies are consistent. In a configuration where the stream is connected to multiple DP Sink devices (e.g., through a repeater or an intermediate branch device) the Source must perform the delay compensation to ensure AV sync. The Source must also perform the delay compensation when the same Source device is connected (through multiple output ports of the Source device) to multiple DisplayPort devices rendering audio-to-video streams containing the same data audio-to-video data.

An example of a DisplayPort monitor connected through repeater device is presented in Figure 2-124. In this example, a repeater device is connected to the Source device and receives an audio-to-video stream through DP cable. The repeater device forwards the video stream to a DP monitor which supports only video, while the audio output is driven directly by repeater device that also includes an audio rendering capability. The monitor and repeater device may have different video and audio processing delays. The Source device will enumerate each of these delays and determine the Point of Sync (PoS) which is point in time to which audio and video streams will be rendered for play back. To meet PoS, the Source device must add a delay to video stream. The Source device must compute delay stamp value for audio and write the delay stamp value on the Sink device.

Audio delay stamp value
= PoS – (Sink device or Repeater inherent audio delay +
delay added to audio in Source device)

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Figure 2-124: DisplayPort Monitor Connected through a Repeater Device

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Sink devices must provide a minimum of 5ms buffering built-in for fine-grained delay compensation. If the calculated audio delay does not exceed the Sink device's capability, the Source device programs the AUDIO_DELAY-related registers with the required delay. If the calculated audio delay exceeds the Sink device's capability, the Source device must introduce a coarse-grain delay on the audio path and recalculate the fine-grained delay required of the Sink device. The resulting fine-grained delay is then programmed into the AUDIO_DELAY-related registers. An example of this delay compensation timing is depicted in Figure 2-125.

Figure 2-125: Delay Compensation for Audio-to-Video Synchronization

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In Figure 2-126, the DP Source is streaming the same audio-to-video stream to multiple DP monitors, each of which may have different audio-to-video decode/post processing latencies. The Source device enumerates the delays between each of these monitors. It also enumerates the audio buffering delay that it is capable of inserting. The Source will identify the PoS to which all the audio-to-video stream of different monitors will be rendered at a point in time. The PoS must be equal to or greater than the maximum audio or video delays introduced by the Sink devices in configuration. The Source must compensate for any additional delay required on the video path on the Source device to meet PoS.

Each Sink device is expected to have a minimum of 5ms audio insertion delay on its path. The Region Of Overlap (ROO) is defined as a region in which the total audio delay (monitor inherent post processing or decode audio delay + Sink buffer delay) on the audio path between different monitors overlap. If the Source cannot identify ROO, it can add coarse delay on audio path to have a ROO. The fine-grain audio delay adjustments are controlled by writing delay stamp values. The Source can pick any point in time within the ROO and identify that as the PoS. The total delay on both audio and video should be equal to PoS after compensation.

Figure 2-126: DisplayPort Source Streaming Audio-to-Video Streams to Multiple Monitors

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Figure 2-127 illustrates audio and video delays incurred in two different Sink devices. The Source enumerates various delays incurred in audio and video path of the Sink devices. The Source will compensate for the video delay to meet PoS. Audio delay stamps are calculated to meet the PoS, PoS minus Sink inherent Processing or decode delay gives "Audio delay stamp value." If this exceeds Sink insertion delay (of 5ms or more), then the Source device will have to insert coarse delay on the audio path and the fine delay will be regulated through audio delay stamps.
Final audio delay stamps are written by the Source device, via the AUDIO_DELAY[7:0], AUDIO_DELAY[15:8], and AUDIO_DELAY[23:16] registers (DPCD Addresses 00112h through 00114h, respectively).

Figure 2-127: Delay Compensation for Audio-to-Video Sync in a Multi-Monitor Configuration

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2.12.3.3 Audio-to-Audio Sync Delay Compensation

In the configuration shown in Figure 2-128 a single audio stream is sent to multiple DisplayPort devices which are capable of playing an audio stream on built-in monitor speakers. These Sink devices can be configured to play audio only, i.e. without video streams being sent to Sink device. The Sink devices must report the audio post processing or decode latency on the AV Sync data block. The Source reads these values to calculate how to compensate for the latencies to achieve audio-to-audio synchronization between these devices.

Sink devices are required to support minimum of 5ms plus the jitter (variance in audio decode or post processing latency in any given mode) incurred on the audio path. Since the Sink devices are expected to report worst case audio delay, the jitter buffer can be used to compensate for jitter incurred in the Sink device.

In the example in Figure 2-128, Monitors 1 and 2 incur different delays on audio path. They also support audio buffering for optional audio-to-audio delay compensation. Source device enumerates the audio latency and additional buffering support in these monitors and then computes ROO. If ROO exists, then it determines the PoS for delay compensation. If ROO does not exist, then coarse delay is inserted to have ROO. The Source will compute delay stamp value and write it on Sink AVSDB registers.

Audio delay stamp value = PoS - (Sink inherent delay + any delay added in Source)

When each of the monitors introduce additional delay as per each delay stamp, the total delay incurred in its Audio path meets PoS and Audio-to-Audio synchronization requirements are satisfied.

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Figure 2-128: Delay Compensation for Audio-to-Audio Sync

2.13 Global Time Code and Audio Inter-channel Sync

This section describes the following two subjects:

- Introduction of the Global Time Code (GTC) of the DisplayPort Standard. The GTC is synchronized between DP devices across a DP link to a 100ns precision. This synchronization is repeated across the entire topology. One end of a link operates as a GTC Master and the other end as a GTC Slave. A GTC Slave synchronizes its GTC value to that of a GTC Master. Each GTC-capable Branch and Sink device must be able to operate as either a GTC Master or GTC Slave. For a GTC-capable Source device, the ability to operate as a GTC Slave is an optional feature.
- Application of GTC for realizing an audio inter-channel synchronization with a 100ns precision when audio channels are rendered on multiple audio stream sinks connected via DP links.

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2.13.1 Global Time Code

The GTC is a 32-bit value, in units of 1ns (the lsb corresponds to 1ns). The GTC value of FFFFFFFFh corresponds to just less than 4.3s. A protocol is defined using Native AUX transaction for DP devices across a DP link to align GTCs to a 100ns precision.

GTC support is required for DP Sink devices with DPCD r1.2 or higher supporting audio and all DP Branch devices with DPCD r1.2 or higher, and is recommended for DP Source devices supporting audio.

Source devices communicate to their downstream devices whether it supports GTC capable and whether it is capable of operating as GTC Slave by setting the TX_GTC_SLAVE_CAP and TX_GTC_CAP bits in the LINK_RATE_SET and TX_GTC_CAPABILITY register (DPCD Address 00115h, bits 4:3, respectively).

2.13.1.1 GTC Accumulator Requirement

The GTC generator will typically be implemented as an accumulator driven by a GTC reference clock. How many counts the GTC value gets increased for each GTC reference clock depends on the GTC reference clock frequency and the precision of the accumulator. For example, if the GTC accumulator is 32 bits with the lsb corresponding to 1ns and if the GTC reference clock is 100MHz (i.e., 10ns per clock cycle), the value is increased by 10 decimal counts per clock cycle.

GTC synchronization between a GTC Master and a GTC Slave consists of two phases; initial frequency adjust phase (lock acquisition phase) and the ensuing periodic frequency adjust phase (lock maintenance phase). During the lock acquisition phase (at the end of which the propagation delay over the DP link is adjusted), the GTC value is transferred from a GTC Master to a GTC Slave every 1ms, while the GTC value transfer takes place every 10ms during the lock maintenance phase.

The GTC reference clock on both ends must be 96MHz or higher during the initial frequency adjust phase, and 24MHz or higher during the periodic frequency adjust phase. When the reference clock is switched, care must be taken to ensure that the switching event does not impact GTC tracking and lock timing requirements. The reference clock must have a long-term accuracy of ±100ppm from its nominal frequency. No spread-spectrum clocking is allowed for the GTC reference clock.

As long as a GTC Master's GTC value has no error more than 12 counts during the lock acquisition phase and no error more than 50 counts during the lock maintenance phase (both coming from GTC accumulator latching edge uncertainty), a GTC Slave must be able to settle to the following:

- During the lock acquisition phase, should be within ±12 counts of a GTC Master's GTC value on the average (the averaging method described toward the end of the Lock Acquisition Phase description part, right before the Phase Skew Offset part of Section 2.13.1.3.1 and Section 2.13.1.3.2), and must be no worse than ±25 counts at any time.
- During the lock maintenance phase, should be within ±50 counts of a GTC Master's GTC value on the average, and must be no worse than ±100 counts at any time.

A GTC Slave must be able to adjust the rate at which it increases the GTC value by adjusting the reference clock value, the increment value, or both the reference clock frequency and the increment value.

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How to adjust the GTC accumulator increment rate (i.e., a damping factor) during the lock maintenance phase is left to the GTC Slave implementer's choice in this revision of the GTC specification. As a general guideline, a GTC Slave should keep its GTC increment adjustment per 10ms interval to the following range:

(Next GTC value - Current GTC value) - (Current GTC value - Previous GTC value) | ≤ 100

Note: *The fact that a GTC Slave increment adjustment guideline is defined per 10ms interval does not imply that the lock maintenance period must be exactly 10ms. Though the lock maintenance interval is 10ms typical, it is bound to vary time to time. A GTC Slave compares its own delta (i.e., Current GTC value - Previous GTC value) to that the delta of a GTC Master's. This way, a GTC Slave is tolerant to the lock maintenance interval variation.*

Though the GTC is a 32-bit value with the lsb representing 1ns, the GTC accumulator in a GTC Slave must be able to increment the GTC accumulator value in precision of well below 1ns in average over lock acquisition/maintenance intervals. For a lock maintenance interval of 10ms and GTC reference clock frequency of 24MHz, there are 240000 GTC accumulation cycles. For example, to adjust the GTC value increment by 25ns per 10ms period, the average increment rate per GTC accumulation cycle must be increased by 0.000104 counts (= 25ns / 240000 cycles).

2.13.1.2 DPCD Fields for GTC

GTC synchronization involves the register bits listed in Table 2-200 in the DPCD field.

Table 2-200: DPCD Fields for GTC Operation

DPCD Address	Definition	Write/Read Over AUX CH
00054h	**RX_GTC_VALUE_0**	Read Only
00055h	**RX_GTC_VALUE_1**	Read Only
00056h	**RX_GTC_VALUE_2**	Read Only
00057h	**RX_GTC_VALUE_3**	Read Only
00058h	**RX_GTC_MSTR_REQ** The TX_GTC_VALUE_PHASE_SKEW_EN and RX_GTC_MSTR_REQ bits (bits 1:0, respectively) are used. Bits 7:2 are RESERVED (Read all 0s). See the RX_GTC_MSTR_REQ register's description in Table 2-155 for further details.	Read Only
00059h	**RX_GTC_FREQ_LOCK_DONE** The RX_GTC_FREQ_LOCK_DONE bit (bit 0) is used. Bits 7:1 are RESERVED (Read all 0s). See the RX_GTC_FREQ_LOCK_DONE register's description in Table 2-155 for further details.	Read Only
0005Ah	**RX_GTC_PHASE_SKEW_OFFSET_0**	Read Only
0005Bh	**RX_GTC_PHASE_SKEW_OFFSET_1**	Read Only
00115h	**LINK_RATE_SET and TX_GTC_CAPABILITY** The TX_GTC_SLAVE_CAP and TX_GTC_CAP bits (bits 4:3, respectively) are used. Bits 7:5 are RESERVED (Read all 0s). See the LINK_RATE_SET and TX_GTC_CAPABILITY register's description in Table 2-156 for further details.	Write/Read
00154h	**TX_GTC_VALUE7:0**	Write/Read

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Table 2-200: DPCD Fields for GTC Operation (Continued)

DPCD Address	Definition	Write/Read Over AUX CH
00155h	**TX_GTC_VALUE15:8**	Write/Read
00156h	**TX_GTC_VALUE23:16**	Write/Read
00157h	**TX_GTC_VALUE31:24**	Write/Read
00158h	**RX_GTC_VALUE_PHASE_SKEW_EN** The RX_GTC_VALUE_PHASE_SKEW_EN bit (bit 0) is used. Bits 7:1 are RESERVED (Read all 0s). See the RX_GTC_VALUE_PHASE_SKEW_EN register's description in Table 2-156 for further details.	Write/Read
00159h	**TX_GTC_FREQ_LOCK_DONE** The TX_GTC_FREQ_LOCK_DONE bit (bit 0) is used. Bits 7:1 are RESERVED (Read all 0s). See the TX_GTC_FREQ_LOCK_DONE register's description in Table 2-156 for further details.	Write/Read
0015Ah	**TX_GTC_PHASE_SKEW_OFFSET7:0**	Write/Read
0015Bh	**TX_GTC_PHASE_SKEW_OFFSET15:8**	Write/Read
02004h	**DEVICE_SERVICE_IRQ_VECTOR_ESI1** The LOCK_ACQUISITION_REQUEST and RX_GTC_MSTR_REQ_STATUS_CHANGE bits (bits 1:0, respectively) are used. Bits 7:3 are RESERVED (Read all 0s). See the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register's description in Table 2-164 for further details.	Clearable Read Only (Bit is cleared when 1 is written via an AUX write transaction)

2.13.1.3 GTC Lock Acquisition and Maintenance between Adjacent DP Devices with Manchester Transaction Format

A GTC Master sends its GTC value at the time of the first differential signal edge in the command field (FIRST_COMMAND_EDGE) of a normal Native AUX transaction syntax.

For a Native AUX request transaction, the FIRST_COMMAND_EDGE is the differential signal edge ending the AUX_SYNC pattern, as shown in Figure 2-129 (as the msb in the command field is 1).

For a reply transaction, the FIRST_COMMAND_EDGE is later than the SYNC End (as the msb of the reply command to NATIVE AUX transaction is always 0).

The GTC value sampling point applies regardless whether a DPTX or DPRX is the GTC Master.

A GTC Master must sample the GTC value at the time FIRST_COMMAND_EDGE leaves its package pins. Both a GTC Master and GTC Slave must measure the FIRST_COMMAND_EDGE position with the accuracy of 10.25ns or better during lock acquisition, and 41ns or better during lock maintenance.

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Figure 2-129: GTC Value Measurement Point by GTC Master

The DPTX must give the GTC-related Native AUX transactions higher priorities than other AUX transaction so that a GTC slave can receive the GTC values at expected intervals. As soon as the other AUX transaction is complete (i.e., AUX_ACK, AUX_DEFER, AUX_NACK, or reply timeout), the DPTX must initiate GTC-related Native AUX transaction once lock acquisition interval (1 to 1.5ms, with 1ms typical) has elapsed during lock acquisition and lock maintenance interval (10 to 13ms, with 10ms typical) during lock maintenance.

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The lock acquisition and maintenance intervals are defined as the time from the start of one transaction to the start of the next transaction.

Figure 2-130: Lock Acquisition and Maintenance Intervals

The DPRX must not reply with AUX_DEFER. The DPRX must not reply with AUX_NACK except for the following two conditions:

- **Unless the request transaction is corrupted** – The DPRX may return no reply in case the request transaction is corrupted.
- **The DPRX must be a GTC Master** – The DPRX requests to be a GTC Master by setting the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0) and RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0) to 1, and then issuing an IRQ_HPD.

Upon AUX_NACK or retry, the DPTX must retry up to three times with the GTC value of the FIRST_COMMAND_EDGE position of the retry request transaction, unless it has received IRQ_HPD with the above bits set.

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2.13.1.3.1 GTC Lock Acquisition/Maintenance Procedure When DPTX Is GTC Master

2.13.1.3.1.1 Lock Acquisition Phase

During the lock acquisition phase, the DPTX sends the GTC value at the time of FIRST_COMMAND_EDGE to a DPRX by writing the value to the TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 registers (DPCD Addresses 00154h through 00157h)), via a single Native AUX burst write request transaction every lock acquisition interval. A DPTX must issue the burst write transaction as soon as 1ms has elapsed from the last write and other pending AUX reply transaction is received (or timed out). In the event it cannot initiate the Native AUX transaction to the TX_GTC_VALUE-related registers within 1.5ms after the previous one, the DPTX may either initiate the transaction after the next interval, which is 2ms from the previous transaction or restart the interval.

The DPRX records its own GTC value at the following two time spots:

- At the arrival of FIRST_COMMAND_EDGE for every AUX request transaction ("FIRST_COMMAND_EDGE" time value)
- At the time it has finished receiving the 32-bit TX GTC value ("GTC_Reception" time value), if it is a single Native AUX burst write transaction to the TX_GTC_VALUE-related registers.

During the lock acquisition phase, a DPRX resets its own GTC accumulator to:

GTC_Reset value
= TX GTC value + (GTC_Reception value - FIRST_COMMAND_EDGE value)

The delta between GTC_Reception value and FIRST_COMMAND_EDGE value is roughly 64us, as there are 64 AUX bit periods between the FIRST_COMMAND_EDGE to the reception of the 32-bit data (namely, 4-bit command, 20-bit address, 8-bit LEN, and 32-bit data).

Starting from the subsequent single Native AUX burst write transaction to the TX_GTC_VALUE-related registers, a DPRX adjusts the GTC accumulator increment rate based on the delta between the GTC_Reset and GTC_Reception values. If the GTC_Reset value is larger, it increases the increment rate. If smaller, it reduces the rate. How much to frequency adjust depends on the absolute amount of delta. A DPRX increases its internal "Lock_Count" value by 1 if the delta is within ±12.5ns. If within ±25ns, but larger than ±12.5ns, it keeps the same Lock_Count. If larger than ±25ns, it clears the Lock_Count to 0. When the Lock_Count is equal to or higher than 5, a DPRX must set RX_GTC_FREQ_LOCK_DONE bit. It must not set the bit to 1 before that.

2.13.1.3.1.2 Phase Skew Offset at the End of Lock Acquisition Phase

After 10 Native AUX write transactions to the TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 registers (DPCD Addresses 00154h through 00157h)) in lock acquisition interval (for each of which it receives AUX_ACK reply), a DPTX reads from the RX_GTC_VALUE-related registers (RX_GTC_VALUE_0, RX_GTC_VALUE_1, RX_GTC_VALUE_2, and RX_GTC_VALUE_3 registers (DPCD Addresses 00054h through 00057h)) and the RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0), by issuing a single Native AUX read burst request transaction to DPCD Addresses 00054h through 00059h.

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If the RX_GTC_FREQ_LOCK_DONE bit is set, the DPTX repeats a Native AUX burst write transaction to the TX_GTC_VALUE-related registers, followed by a Native AUX burst read transaction from the RX_GTC_VALUE-related registers and RX_GTC_FREQ_LOCK_DONE bit multiple times at each 1ms lock acquisition interval.

If it reads the RX_GTC_FREQ_LOCK_DONE bit cleared to 0, a DPTX has a choice of either re-initiating the lock acquisition phase or giving up the lock acquisition.

Note that a DPRX must not be designed to depend on the GTC burst read following the GTC burst write, and must accommodate unrelated AUX transactions in between.

For each of the above Native AUX read reply transactions with the RX_GTC_FREQ_LOCK_DONE bit set to 1, the DPTX records the delta between its own GTC accumulator value at FIRST_COMMAND_EDGE.

Over multiple consecutive read reply transactions for which the RX_GTC_FREQ_LOCK_DONE bit remains set, the DPTX calculates the average of the signed delta value. The phase offset is half of the average of the delta. How many times to read the RX_GTC_VALUE-related registers before calculating the average is left to DPTX implementation choice. A minimum of four reads is recommended.

The DPTX then writes the calculated phase offset value to the TX_GTC_PHASE_SKEW_OFFSET7:0 and TX_GTC_PHASE_SKEW_OFFSET15:8 registers (DPCD Addresses 0015Ah and 0015Bh, respectively) with the RX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_VALUE_PHASE_SKEW_EN register (DPCD Address 00158h, bit 0) set to 1, via a single Native AUX burst write request transaction to DPCD Addresses 00158h through 0015Bh. Upon this Native AUX write transaction, the DPRX increases its GTC accumulator count by TX_GTC_PHASE_SKEW_OFFSET value without adjusting the increment rate. After receiving AUX_ACK to the Native AUX write transaction to DPCD Addresses 00158h through 0015Bh, the DPTX clears the RX_GTC_VALUE_PHASE_SKEW_EN bit with the Native AUX write transaction to DPCD Address 00158h.

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2.13.1.3.1.3 Lock Maintenance Phase

The lock maintenance phase is entered once a DPTX clears the RX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_VALUE_PHASE_SKEW_EN register (DPCD Address 00158h, bit 0).

During the lock maintenance phase, a DPTX writes the TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 registers (DPCD Addresses 00154h through 00157h)) every lock maintenance interval. A DPTX must issue the AUX write transaction as soon as 10ms has elapsed from the last write to the TX_GTC_VALUE-related registers and other pending AUX reply transaction is received (or timed out). A DPRX adjusts the GTC accumulator increment rate to maintain the following condition:

Current GTC value - Previous GTC value
= Current TX_GTC_VALUE - Previous TX_GTC_VALUE ±50ns

When the DPRX judges that it is not possible to consistently stay within the above range despite the best effort, the DPRX clears the RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0), sets the LOCK_ACQUISITION_REQUEST bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 1), and generates IRQ_HPD. In this revision of the GTC specification, when to make the judgment is left to each DPRX implementer.

2.13.1.3.2 GTC Lock Acquisition/Maintenance Procedure When DPRX Is GTC Master

For a DPRX interfacing with a DPTX capable of GTC-Slave operation (as indicated by a DPTX's setting the TX_GTC_CAP bit in the LINK_RATE_SET and TX_GTC_CAPABILITY register (DPCD Address 00115h, bit 3) to 1) to request to be a GTC Master, it sets the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0) and RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0), and issues IRQ_HPD.

A DPRX acting as a GTC Master sets the LOCK_ACQUISITION_REQUEST bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 1) and generates IRQ_HPD to request for the start of lock acquisition.

2.13.1.3.2.1 Lock Acquisition Phase

During the lock acquisition phase, a DPTX reads the GTC value of the DPRX by reading the RX_GTC_VALUE-related registers (RX_GTC_VALUE_0, RX_GTC_VALUE_1, RX_GTC_VALUE_2, and RX_GTC_VALUE_3 registers (DPCD Addresses 00054h through 00057h)) and RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0), via a single Native AUX burst read request transaction to DPCD Addresses 00054h through 00059h every lock acquisition interval 1ms. Upon the Native AUX read reply transaction, the DPRX stores its GTC value at the FIRST_COMMAND_EDGE differential edge ending the AUX SYNC pattern to the RX_GTC_VALUE-related registers.

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A DPTX records its own GTC value at the following two time spots:

- At the arrival of FIRST_COMMAND_EDGE for the reply transaction ("FIRST_COMMAND_EDGE" time value).
- At the time it has finished receiving the 32-bit RX GTC value ("GTC_Reception" time value).

During the lock acquisition phase, a DPTX resets its own GTC accumulator to:

GTC_Reset value
= RX GTC value + (GTC_Reception value - FIRST_COMMAND_EDGE value)

The delta between the GTC_Reception and FIRST_COMMAND_EDGE values is roughly 40us, as there are 40 AUX bit periods between the FIRST_COMMAND_EDGE to the reception of the 32-bit data (namely, 8-bit reply command and 32-bit data).

Starting from the subsequent Native AUX burst read from DPCD Addresses 00054h through 00059h every lock acquisition interval, a DPTX adjusts the GTC accumulator increment rate based on the delta between the GTC_Reset and GTC_Reception values. If the GTC_Reset value is larger, the DPTX increases the increment rate. If the GTC_Reset value is smaller, the DPTX reduces the rate.

How much to adjust depends on the absolute amount of delta. A DPTX increases its internal "Lock_Count" value by 1 if the delta is within ±12.5ns. If the delta is within ±25ns, but larger than ±12.5ns, the DPTX keeps the same Lock_Count. If the delta is larger than ±25ns, the DPTX clears the Lock_Count to 0. When the Lock_Count is equal to or higher than 5, the DPTX must write its GTC value to the TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 (DPCD Addresses 00154h through 00157h)) and sets the TX_GTC_FREQ_LOCK_DONE bit in the TX_GTC_FREQ_LOCK_DONE register (DPCD Address 00159h, bit 0) to 1, using a single AUX write burst transaction to DPCD Addresses 00154h through 00159h. It must not set the bit before that.

2.13.1.3.2.2 Phase Skew Offset at the End of Lock Acquisition Phase

After setting the TX_GTC_FREQ_LOCK_DONE bit in the TX_GTC_FREQ_LOCK_DONE register (DPCD Address 00159h, bit 0) to 1, a DPTX repeats writing to the following registers:

- TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 (DPCD Addresses 00154h through 00157h)
- RX_GTC_VALUE_PHASE_SKEW_EN register (DPCD Address 00158h)
- TX_GTC_FREQ_LOCK_DONE register (DPCD Address 00159h)

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The DPTX the repeats reading of the registers listed below, using a single AUX burst read transaction to DPCD Addresses 00054h through 0005Bh, until it reads that the RX_GTC_FREQ_LOCK_DONE bit is set to 1 every lock acquisition interval:

- RX_GTC_VALUE-related registers (RX_GTC_VALUE_0, RX_GTC_VALUE_1, RX_GTC_VALUE_2, and RX_GTC_VALUE_3 (DPCD Addresses 00054h through 00057h))
- RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0)
- RX_GTC_PHASE_SKEW_OFFSET_0 and RX_GTC_PHASE_SKEW_OFFSET_1 registers (DPCD Addresses 0005Ah and 0005Bh, respectively)

The DPRX records the value written to the TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 (DPCD Addresses 00154h through 00157h)), as long as the TX_GTC_FREQ_LOCK_DONE bit remains set.

For each of the above Native AUX write transactions with the TX_GTC_FREQ_LOCK_DONE set to 1, a DPRX records the delta between its own GTC accumulator value at FIRST_COMMAND_EDGE and the received TX_GTC_VALUE-related register values. Over multiple consecutive read reply transactions for which the TX_GTC_FREQ_LOCK_DONE bit remains set, the DPRX calculates the average of the signed delta value. The phase offset is half of the average of the delta. How many times to record the TX GTC value before calculating the average is left to DPRX-implementation choice. The minimum of four is recommended.

The DPRX then sets the RX_GTC_PHASE_SKEW_OFFSET_0 and RX_GTC_PHASE_SKEW_OFFSET_1 registers to the calculated phase offset value and sets the TX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 1) to 1. Upon the subsequent Native AUX read transaction from DPCD Addresses 00054h through 00059h, the DPTX increases its GTC accumulator count by the RX_GTC_PHASE_SKEW_OFFSET_0 and RX_GTC_PHASE_SKEW_OFFSET_1 register values without adjusting the increment rate. After replying with AUX_ACK to this write transaction, the DPRX clears the TX_GTC_VALUE_PHASE_SKEW_EN bit.

It should be noted that an AUX burst transaction by a DPTX is part of the read/write pair during the phase offset calculation procedure described above, as shown in Figure 2-131.

If a DPTX does not set the TX_GTC_FREQ_LOCK_DONE bit to 1 after 10 reads from DPCD Addresses 00054h through 00059h, a DPRX may prompt the DPTX to stop the lock acquisition by doing the following:

1. Clearing the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0).
2. Clearing the RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0).
3. Issuing an IRQ_HPD.

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Figure 2-131: AUX Transactions for GTC Synchronization (Informative)

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2.13.1.3.2.3 Lock Maintenance Phase

The lock maintenance phase is entered once a DPTX reads the TX_GTC_VALUE_PHASE_SKEW_EN bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 1) cleared.

During the lock maintenance phase, a DPTX reads the RX_GTC_VALUE-related registers (RX_GTC_VALUE_0, RX_GTC_VALUE_1, RX_GTC_VALUE_2, and RX_GTC_VALUE_3 registers (DPCD Addresses 00054h through 00057h)) every lock maintenance interval. A DPTX must issue the AUX read transaction as soon as 10ms has elapsed from the last write to the TX_GTC_VALUE-related registers (TX_GTC_VALUE7:0, TX_GTC_VALUE15:8, TX_GTC_VALUE23:16, and TX_GTC_VALUE31:24 registers (DPCD Addresses 00154h through 00157h)) and other pending AUX reply transaction is received (or timed out). A DPRX adjusts the GTC accumulator increment rate to maintain the following condition:

Current GTC value - Previous GTC value
= Current RX_GTC_VALUE - Previous RX_GTC_VALUE ±50ns

When a DPRX judges that it is not possible to consistently stay within the above range despite the best effort, the DPRX doing the following:

- Clears the RX_GTC_FREQ_LOCK_DONE bit in the RX_GTC_FREQ_LOCK_DONE register (DPCD Address 00059h, bit 0),
- Sets the LOCK_ACQUISITION_REQUEST bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 1), and
- Generates an IRQ_HPD

In this revision of the GTC specification, when to make the judgment is left to each DPRX implementer.

2.13.1.4 Selection of GTC Grand Master

When multiple GTC-capable DP devices are connected via multiple DP links in a given topology, one device must be selected as a GTC Grand Master. A device connected to the GTC Grand Master becomes a GTC Slave. This GTC Slave device when it conducts the GTC synchronization with another device becomes a GTC Master. As a result of the series of GTC synchronizations, all DP devices in the topology become synchronized to the GTC Grand Master.

By default, an upstream device is a GTC Master of any DP link. When there is only one DP Source device in a topology, therefore, that one DP Source device becomes the GTC Grand Master.

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2.13.1.4.1 Selection of GTC Grand Master When Multiple Source Devices Present

When there are multiple Source devices in a topology that has one or multiple Concentrator Branch devices, only one device is chosen as a GTC Grand Master.

When one of the UFPs of a Concentrator (UFP1) has either achieved the GTC Lock or started the GTC lock acquisition with its upstream device (Upstream Device1), and when another upstream device (Upstream Device2) connected to the other UFP (UFP2) starts GTC lock acquisition, the Concentrator port takes the following actions:

1. Sets the RX_GTC_MSTR_REQ bit in the RX_GTC_MSTR_REQ register (DPCD Address 00058h, bit 0) to 1.
2. Sets the RX_GTC_MSTR_REQ_STATUS_CHANGE bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 0) to 1 and generates an IRQ_HPD.
3. Upon IRQ_HPD handling by Upstream Device2, initiates GTC lock acquisition as GTC Master.
4. Subsequently, maintains GTC Lock as a GTC Master.

If Upstream Device2 is another Branch device, that Branch device is to re-initiate GTC lock acquisition as a GTC Master to other downstream and upstream links if those links have already either started or achieved GTC lock acquisition.

If a Concentrator receives Native AUX transactions for GTC lock acquisition from multiple upstream devices simultaneously, the Concentrator accepts one of the upstream devices as a GTC Master. To the upstream device that was not selected, the Concentrator replies with AUX_NACK, and initiate GTC lock acquisition as a GTC Master as described above. If there are multiple Source devices that support a GTC Master mode of operation only, then only one of them can make use of GTC.

How a Concentrator selects one upstream device it accepts as a GTC Grand Master is an implementation-specific decision and is beyond the scope of this Standard.

2.13.1.4.1.1 Disabling GTC Synchronization

The Grand Master status is relinquished when an AUX transaction for Lock Acquisition or Maintenance is skipped for five consecutive intervals.

2.13.1.4.1.2 Branch Device GTC Handling Requirements

All the MST-capable DPTX and DPRX ports of a Branch device must be able to handle GTC both in Master mode and Slave mode. Only one of the DPTX/DPRX ports of a Branch device acts as GTC Slave while other ports act as GTC Master to the adjacent devices.

A Branch device must have only one GTC value to be used for all the ports.

2.13.1.4.1.3 Power Management while GTC Is in Use

It should be noted that AUX should remain powered while GTC is in use. Otherwise, GTC operation will not work.

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2.13.2 Application of GTC for Audio Inter-channel Synchronization

Having established a common global time reference across all nodes, the DP audio stream source must determine the GTC presentation time for each audio frame.

An *IEC 60958* audio frame consists of 192 audio samples. A One Bit audio or DST audio frame consists of the number of samples that occur within 1/75th of a second. The DP audio stream Source must insert the desired GTC presentation time for the audio frame into the "Channel" field ("C" in Figure 2-33 through Figure 2-35) in a bit serial manner in the last 32 samples of an audio frame (Number of Samples per Frame - 32 to Number of Samples per Frame - 1), starting with the msb of the GTC in the first audio sample of the series.

Of the 32-bit field, the most significant 31 bits of the GTC value (bits 31:1) occupy the most significant 31 bits of the field. The lsb is used to indicate the validity of the field. If the lsb is 0, the field is to be ignored by a stream sink.

The 31-bit GTC value represents the starting time of the presentation of immediately upcoming audio frame.

The DP Source device must choose GTC presentation values as follows, based on the audio delay capabilities discovered through the mechanism described in Section 2.12:

- Calculate the propagation delay to each of the audio stream sinks in the topology
- Calculate the GTC presentation value that all audio stream sinks can realize within their audio delay capabilities
- Increase the GTC presentation value each frame by the GTC delta between two audio frames

Note: *The audio sample rate is* ***not*** *synchronized to the GTC rate. The GTC should be used as a "ruler." An audio stream sink device should render the audio within ±500ns of the specified GTC value.*

2.13.2.1 Presentation Time

The presentation time is defined at the points in systems as defined below:

- **Systems with speakers** – At analog speaker terminals
- **Systems with analog audio outputs** – At the analog audio-out jack
- **Systems with digital outputs** – At the digital output jack at the signal edge in that particular digital protocol defining the sample rendering instant.

With the presentation time plane defined as above, one may use an audio test signal that has a well-defined edge (e.g., a sawtooth wave) at a known time to verify that the audio is being rendered at the proper time.

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2.13.2.1.1 Dynamic Adjustment of Presentation Time

If an audio stream already has embedded GTC values for a presentation time, but there is a need to adjust the playback offset, an audio source device should set the AudioMute_Flag bit in the VB-ID (bit 4) on the link, adjust the presentation time, and then clear the AudioMute_Flag bit.

In case an audio sink device encounters abrupt change in the presentation time received from an audio source device relative to its presentation time based on its current audio sampling rate without preceding the AudioMute_Flag bit, the Sink device should make sure that the change is persistent by checking the presentation time for a few extra times, and, if persistent, should make the presentation time change in a matter that results in minimum audio glitch.

2.13.2.1.2 Presentation Time Insertion for Multi-Channel Audio

When rendering multi-channel audio on multiple physical audio rendering devices, a source device, as a rule, is required to insert the same presentation time in all audio channels. In case a rendering skew is needed among multiple physical audio rendering devices, it is the responsibility of the source device to insert the skew among multiple audio channels before audio stream transmission.

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3 PHY Layer

3.1 Introduction

The DisplayPort PHY Layer specified the physical properties of a direct connection between a port on an upstream device (i.e., an AV output port on a DP Source or Branch device) and a port on a downstream device (i.e., an AV input port on a DP Sink or Branch device). It de-couples the data transmission electrical specifications from the DisplayPort Link Layer, thereby allowing modularity for future Link Layer specific design enhancements and also future changes to the transport media type, such as the use of Hybrid devices. The PHY Layer is further sub-divided into logical and electrical functional sub-blocks, as shown in Figure 3-1.

Figure 3-1: DP PHY Layer

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3.1.1 PHY Layer Functions

This section summarizes the functionalities of the DisplayPort PHY Layer.

3.1.1.1 Hot Plug/Unplug Detection Circuitry

The PHY Layer is responsible for both the detection of Hot Plug/Unplug and notification of the Link Layer:

- **Logical Sub-block** – Notifies Hot Plug/Unplug events to the upper layer
- **Electrical Sub-block** – Detects a Hot Plug/Unplug event

3.1.1.2 AUX Channel Circuitry

The PHY Layer provides for the half-duplex bidirectional AUX channel for services such as Link Configuration or Maintenance and EDID access, using 1Mbps Manchester-II coding.

- Logical Sub-block
  - Supports Manchester-II coding
  - Generates and detects Start/Stop condition, and locks to the synchronization pattern for the appropriate encoding
  - Encoding and decoding of data for the appropriate encoding
- Electrical Sub-block
  - Consists of a single differential pair, both ends of the link equipped with driver and receiver for half-duplex bidirectional operation
    - Driving end
      - Drives a doubly terminated, AC-coupled differential pair in a manner compliant with the AUX channel electrical specification for encoding
    - Receiving end
      - Receives the incoming differential signal and extracts the data

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3.1.1.3 Main-Link Circuitry

The PHY Layer provides the unidirectional Main-Link for the transport of isochronous streams and secondary-data packets.

- Logical Sub-block
  - Scrambling and de-scrambling
  - ANSI 8b/10b encoding/decoding
  - Serialization and de-serialization
  - Link Training and Link Status Monitor
  - Adjusts link rate, spreading, drive current level, and pre-emphasis level, as needed
    - Link Quality Measurement for testability
- Electrical Sub-block
  - Consists of up to four differential pairs
  - Transmitter
    - Drives doubly terminated, AC-coupled differential pairs in a manner compliant with the Main-Link Transmitter electrical specification
  - Receiver
    - Receives the incoming differential signals and extract the data with its link CDR (clock and data recovery) circuits

3.1.2 Link-PHY Layer Interface Signals

This section summarizes the interface signals between the Link and PHY Layers.

3.1.2.1 Hot Plug/Unplug Detection

Hot Plug/Unplug Detection circuitry provides for the Hot Plug/Unplug Status signal to Link Layer.

The de-bouncing timer must belong to Link Layer and not to the PHY Layer.

3.1.2.2 AUX Channel

The interface signal for the AUX channel between the Link and PHY Layers must consist of an 8-bit data signal plus 1-bit control signal. The control signal is used to indicate Start or Stop of the AUX CH transaction. Use of the 1-bit control signal to indicate Start/Stop conditions is implementation-specific and is not covered in this Standard.

3.1.2.3 Main-Link

The interface signal for the Main-Link between the Link and PHY Layers consists of an 8-bit data signal per Main-Link lane plus a 1-bit control signal. The control signal is used for special symbols such as BS (Blank Start) and BE (Blank End) for framing an isochronous data stream. Use of the 1-bit control signal is implementation-specific and is not covered in this Standard.

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3.1.3 PHY Layer and Link Media Interface Signals

This section summarizes the interface signals between the PHY Layer and Link Media consisting of PCB, connector, and cable. (Connector and cable may be absent for certain link configurations, such as a chip-to-chip connection.)

3.1.3.1 DP_PWR / DP_PWR_RETURN

A DP Source, Sink or locally self-powered Branch device must provide power on the DP_PWR pin of the box-to-box DP connector. Branch devices that are not self-powered[a] need not supply DP_PWR. Power provided at DP_PWR is intended to power consumer devices connected directly to the power provider's connector.

3.1.3.2 Hot Plug/Unplug Detection

One signal, Hot Plug Detect (HPD), is used by a device (an upstream device) to detect that a downstream-facing port (DFP) on the device has been connected to another device (the downstream device). Implementation of HPD is optional for an embedded link configuration. At least a "trickle power" must be present both in the upstream and downstream devices for a Hot Plug event to be detected.

Downstream devices must be ready for an AUX CH transaction whenever they assert (drive high) the HPD signal. Even in power-saving mode(s) (see Section 5.2.5), a downstream device that keeps its HPD signal asserted must be able to detect the presence of an AUX CH differential signal input. The downstream device must exit the power-saving mode within 1ms of the differential signal being detected.

3.1.3.3 AUX Channel

The AUX Channel consists of one differential pair (AUX-CH+ and AUX-CH-).

At least "trickle power" must be present both in upstream device and downstream device for the AUX Channel to be functional.

A downstream device that supports upstream device detection, an optional feature, must monitor the DC voltage of the AUX CH lines between the AC coupling capacitors and its upstream connector.

3.1.3.4 Main-Link

The Main-Link consists of up to four differential pairs (Main-Link Lane 0+, Main-Link 0-, Main-Link Lane 1+, Main-Link Lane 1- …).

Both the upstream and downstream device must be fully powered for the Main-Link to be functional.

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a. *Self-powered capable Branch devices that are physically disconnected from their independent power source are effectively "not self-powered," and need not supply DP_PWR.*

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3.1.4 Compliance Measurement Points

The compliance measurement points are shown in Figure 3-2. Normative specifications are provided for measurements taken at the connectors (Compliance Measurement Points TP2, TP3 and TP3_EQ). Informative specifications applying to silicon devices are provided in Appendix D for TP1 and TP4.

A compliance test load that consists of a pair of 50Ω resistive loads as shown in Figure 3-3 is used during the electrical measurements for transmitter testing at the appropriate compliance point. A tester providing an equivalent load and with built-in equalization or software equivalent is used to qualify appropriate stressed test signals used during the measurement of receive jitter at TP3 and TP3_EQ for the Main-Link and the AUX Forward Channel, and at TP2 for the AUX Back Channel.

Figure 3-2: Compliance Measurement Points of the Channel

Figure 3-3: Compliance Test Load

TP3_EQ is introduced for HBR and HBR2 because the losses in the channel interconnect may result in an attenuated or closed EYE at TP3. Measurements made at TP3 are passed through the Reference Receiver Equalizer to generate TP3_EQ (see Section 3.5.2.10).

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3.1.4.1 Compliance Cable Models

Compliance cable models are physical and/or mathematical models used in compliance testing when the impact of cable assemblies must be represented to complete the compliance test. To ensure interoperability, compliance cable models are intended to represent realistic worst-case cable assemblies for insertion loss, return loss, impedance profile, Far End Noise (FEN), Near End Noise (NEN), and skew (intra-pair and inter-pair), but must not exceed any electrical performance limits defined in Section 4. A realistic worst-case cable assembly may not match the max electrical performance limits exactly for any or all parameters since the limits are intended to cover a wide range of cable assembly construction and not all max electrical performance limits are expected to occur simultaneously in a single cable. For this reason, where compliance testing is performed using physical cables, it may be appropriate to use two or more physical reference cables, not just a single physical reference cable.

As an example, the compliance configurations for HBR2 are shown using both a physical cable model and a mathematical cable model. In all other cases, a physical cable model is shown, but an equivalent configuration using a mathematical cable model is equally acceptable.

For device transmitter compliance testing, intra-pair skew in compliance cable model is intended to be 0ps.

See the latest DisplayPort PHY Compliance Test Specification for complete compliance cable model information.

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3.1.4.2 Main-Link Compliance Configurations

This section illustrates the test configurations for testing the compliance of upstream and downstream devices.

Note: *The illustrations do not include the aggressor connections that must be present for cross-talk related tests.*

3.1.4.2.1 HBR2 Compliance Configuration

For testing compliance of an HBR2 upstream device, a compliance cable model is used to measure the EYE at TP3_EQ. The model may be implemented either as a physical reference cable or as a mathematical model incorporated into the analyzer. Figure 3-4 illustrates both options.

Figure 3-4: HBR2 Upstream Device Compliance Test Configuration

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For testing compliance of an HBR2 downstream device, a stressed signal generator is calibrated by measuring the EYE at TP3_EQ using a compliance cable model. The model may be implemented either as a physical reference cable or as a mathematical model incorporated into the generator. The analyzer is then removed from the configuration and the stressed signal generator, including the compliance cable model, is applied to the downstream device. If the mathematical model is incorporated into the generator, then the appropriate model must be selected depending on whether the downstream device is a device with a DP receptacle, a tethered device with a Mini DP connector, or a tethered device with a full-size DP connector. Alternate methods for calibrating the output of the stressed signal generator to generate the appropriately stressed signal at TP3 may be used.

Figure 3-5: HBR2 Downstream Device Compliance Test Configuration

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3.1.4.2.2 HBR Compliance Configuration

An analyzer is connected directly to the device for testing the compliance of an HBR upstream device. This is illustrated in Figure 3-6.

Figure 3-6: HBR Upstream Device Compliance Test Configuration

For testing compliance of an HBR downstream device with a DP receptacle connector, a stressed signal generator is calibrated by measuring the EYE at TP3_EQ. The analyzer is then removed from the configuration and the stressed signal generator is applied to the downstream device. This is illustrated in Figure 3-7.

Figure 3-7: HBR Downstream Device Compliance Test Configuration

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For testing compliance of an HBR downstream device with a tethered cable, a stressed signal generator is calibrated by measuring the EYE at TP2. The analyzer is then removed from the configuration and the stressed signal generator, including a compliance cable model, is applied to the downstream device. The model may be implemented either as a physical reference cable or as a mathematical model incorporated into the generator. If the mathematical model is incorporated into the generator, then the appropriate model must be selected depending on whether the downstream device is a tethered device with a mini DP connector, or a tethered device with a full-size DP connector. This is illustrated in Figure 3-8.

Figure 3-8: HBR Tethered Downstream Device Compliance Test Configuration

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3.1.4.2.3 RBR Compliance Configuration

An analyzer is connected directly to the device for testing the compliance of an RBR Upstream device. This is illustrated in Figure 3-9.

Figure 3-9: RBR Upstream Device Compliance Test Configuration

For testing compliance of an RBR downstream device with a DP receptacle connector, a stressed signal generator is calibrated by measuring the EYE at TP3. The analyzer is then removed from the configuration and the stressed signal generator is applied to the downstream device. This is illustrated in Figure 3-10.

Figure 3-10: RBR Downstream Device Compliance Test Configuration

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For testing compliance of an RBR downstream device with a tethered cable, a stressed signal generator is calibrated by measuring the EYE at TP2. The analyzer is then removed from the configuration and the stressed signal generator, including a compliance cable model, is applied to the downstream device. The model may be implemented either as a physical reference cable or as a mathematical model incorporated into the generator. If the mathematical model is incorporated into the generator, then the appropriate model must be selected depending on whether the downstream device is a tethered device with a mini DP connector, or a tethered device with a full-size DP connector. This is illustrated in Figure 3-11.

Figure 3-11: RBR Tethered Downstream Device Compliance Test Configuration

3.1.4.3 AUX Channel Compliance Configurations

The AUX channel is a half-duplex channel, thus both the upstream-facing port (UFP) and DFP have both transmitter and receiver functions. The direction of transmission from the UFP to the DFP is referred to as the AUX Forward Channel, and the direction of transmission from the DFP to the UFP is referred to as the AUX Back Channel. Individual AUX transactions are Manchester transactions.

The Manchester Forward Channel transmitter compliance test point is TP2, and the Manchester Forward Channel receiver compliance test point is TP3. The Manchester Back Channel transmitter compliance test point is TP3 and the Manchester Back Channel receiver compliance test point is TP2. The compliance specifications for the Forward Channel and the Back Channel are identical. No cable models are used for Manchester transmitter or receiver compliance testing.

For Manchester transmitter compliance testing, an analyzer is connected directly to the transmitter compliance test point. For Manchester receiver compliance testing, a stressed signal generator is calibrated using an analyzer, and then the analyzer is disconnected and the stressed signal generator is connected to the receiver.

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3.1.5 Electrical Signal Definitions

The following definitions apply to both Main-Link and AUX CH signaling.

3.1.5.1 Definition of Differential Voltage

A differential signal is defined by taking the voltage difference between two conductors. In this Standard, a differential signal or differential pair is comprised of a voltage on a positive conductor, V_{D+}, and a negative conductor, V_{D-}. The differential voltage (V_{DIFF}) is defined as the difference of the positive and the negative conductor voltages ($V_{DIFF} = V_{D+} - V_{D-}$), as shown in Figure 3-12.

The Common Mode Voltage (V_{CM}) is defined as the average or mean voltage present on the same differential pair ($V_{CM} = [V_{D+} + V_{D-}] / 2$).

Figure 3-12: Definition of Differential Voltage and Differential Voltage Peak-to-Peak

This Standard's electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following equations:

- Symmetrical Differential Swing

  $$V_{DIFFp\text{-}p} = (2 * max\,|V_{D+} - V_{D-}|)$$

- Asymmetrical Differential Swing

  $$V_{DIFFp\text{-}p} = (max\,|V_{D+} - V_{D-}|\ \{V_{D+} > V_{D-}\} + max\,|V_{D+} - V_{D-}|\ \{V_{D+} < V_{D-}\})$$

- Common-Mode Voltage

  $$V_{CMp} = (max\,|V_{D+} + V_{D-}| / 2)$$

The definition equations only produce a single number (the number in the specification tables) and are not suitable for plotting a waveform.

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3.1.5.2 Voltage Swing and Pre-emphasis

The DPTX specification for the Main-Link allows four differential peak-peak voltage swing levels, and four pre-emphasis (Post Cursor1) levels.

Certain combinations of voltage swing levels and pre-emphasis levels result in differential peak-to-peak voltages which are outside the allowable range, and thus are not allowed. Table 3-1 lists the allowable combinations of voltage swing and pre-emphasis levels.

Table 3-1: Allowed Vdiff_pp and Pre-emphasis Combinations

Voltage Swing Level	Pre-emphasis Level			
	Level 0	Level 1	Level 2	Level 3
	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp
0	Required	Required	Required	Optional
1	Required	Required	Required	Not allowed
2	Required	Required	Not allowed	Not allowed
3	Optional	Not allowed	Not allowed	Not allowed

Note: *Pre-emphasis, as used in this standard, is defined as 20 multiplied by $\log_{10}$ of the ratio of the peak-to-peak amplitude for the first T_{BIT} immediately following a transition divided by the peak-to-peak amplitude for the subsequent bits until the next transition ($20 \cdot \log(V_{DIFF\text{-}PRE} / V_{DIFF})$).*

An example of pre-emphasis is shown in Figure 3-13. When there are consecutive single bits of opposite values being transmitted, all the consecutive bit transitions must be pre-emphasized to the voltage swing of V_{DIFF_PRE}.

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Figure 3-13: Example of Pre-emphasis

The notation $V_{DIFF\text{-}PRE_v_p}$ is used to denote the $V_{DIFF\text{-}PRE}$ measured at voltage level v and pre-emphasis level p (i.e., the voltage measured on a transition bit). The notation $V_{DIFF_v_p}$ is used to denote the V_{DIFF} measured at voltage level v and pre-emphasis level p (i.e. the voltage measured on the non-transition bits). The notation T_{BIT} denotes the time taken to transmit a single bit.

The values of $V_{DIFF\text{-}PRE_2_0}$ and $V_{DIFF_2_0}$ are measured and used as a baseline for the requirements for all other values of $V_{DIFF\text{-}PRE_v_p}$ and $V_{DIFF_v_p}$.

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3.1.6 Scrambling

Scrambling of the Main-Link data is performed for EMI reduction prior to ANSI 8b/10b encoding on the transmitter. De-scrambling of the data symbols is performed following ANSI 8b/10b decoding at the receiver. Use of scrambling should result in approximately 7dB reduction in peak spectrum.

Each of the Main-Link lanes is scrambled and de-scrambled independently, each with a 16-bit internal LFSR, as follows:

$$G(X) = X^{16} + X^{5} + X^{4} + X^{3} + 1$$

Each byte of data is scrambled/de-scrambled with the most significant 8 bits of the LFSR in reverse bit order:

{D'[7], D'[6], D'[5], D'[4], D'[3], D'[2], D'[1], D'[0]}
= {D[7], D[6], D[5], D[4], D[3], D[2], D[1], D[0]} ^ {LFSR[8]. LFSR[9], LFSR[10], LFSR[11], LFSR[12], LFSR[13], LFSR[14, LFSR[15]}

In Single-stream Transport (SST) mode, the UFP must replace every 512th BS BF BF BS or BS CP CP BS symbol sequence with an SR BF BF SR or SR CP CP SR symbol sequence. In Multi-stream Transport (MST) mode, the UFP must transmit an SR symbol as the MTPH every 1024 Multi-stream packets (thus, an SR symbol is transmitted every 65,536 symbols). The SR symbol or SR BF BF SR or SR CP CP SR symbol sequence is used to reset the LFSR to FFFFh (or FFFEh for eDP Alternate Scrambler Seed), so that the first byte of data following the scrambler reset is scrambled/de-scrambled with FFh. The scrambler is then advanced to contain E817h (or E917h for eDP Alternate Scrambler Seed).

The data scrambling rules must be as follows:

- LFSR advances on all symbols, both data symbols (D), and special symbols (K).
- Special symbols (K) are not scrambled.
- Data symbols, including “fill data” are scrambled. Fill data is normally zero before scrambling.
- Multi-stream indexed control symbols are scrambled before being encoded as special symbols (K).

Scrambling must be disabled during Link Training and Recovered Link Clock Quality Measurement.

Receivers should implement appropriate robustness to ensure that bit errors that generate a false SR symbol do not result in the de-scrambler LFSR being reset.

A C code reference implementation of the scrambler/de-scrambler is provided in Appendix G. This includes an implementation of methods for the recommended robust detection of scrambler reset.

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3.1.7 Symbol Coding and Serialization/De-serialization

The DP interface uses the ANSI 8b/10b[a] as its channel coding scheme to provide symbol-level DC balancing. It also provides high transition density for link clock phase tracking at the receiver. Using this scheme, 8-bit data characters are treated as three bits and five bits mapped onto a 4-bit code group and a 6-bit code group, respectively.

The control bit in conjunction with the data character is used to identify when to encode one of the Special Symbols included in the ANSI 8b/10b transmission code.

These code groups are concatenated to form a 10-bit symbol.

As shown in Figure 3-14, ABCDE maps to abcdei and FGH maps to fghj.

After coding, the ANSI 8b/10b symbols are serialized so that the least significant bit (lsb) is transported first, and the most significant bit (msb) last.

Figure 3-14: Character to Symbol Mapping

a. *The ANSI 8b/10b coding scheme is as defined in ANSI X3.230-1994, Clause 11 (and also 802.3z, 36.2.4).*

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3.2 DP_PWR for Box-to-Box DisplayPort Connection

DP connectors on DP Source, Sink, and self-powered Branch devices have one power pin and one return current pin on the receptacle connector. This power must be provided by the Source, Sink, or self-powered Branch device any time DP output ports of those devices are enabled. Branch devices that are not self-powered[a] are allowed, which may not provide DP_PWR at its connectors.

The DP_PWR consumer must be connected directly to the power provider's connector. The consumer may be a Branch Device (with or without an additional power source), an Active Cable Assembly or sink with a permanently attached cable.

A downstream device with a permanently attached cable may, optionally, provide DP_PWR on the DP_PWR pin of the plug connector. The downstream device with an attached cable that is capable of providing DP_PWR on the plug connector must verify if a device that uses DP_PWR is connected to the plug connector. The DP_PWR output of a downstream device with a permanently attached cable may only be enabled after the downstream device has determined that a DP_PWR using device is attached. The method for detection of a DP_PWR using device is described in Section 3.2.1.

The voltage on the DP_PWR pin of the upstream device must be in the range of 2.89 to 3.6V (+3.3V ±10% less fuse voltage drop = 0.076V). The minimum power available at the upstream DP_PWR pin must be 1.5W. A downstream device that consumes more than 1.5W of power must have means of getting power from an alternate power source.

The voltage on the DP_PWR pin of the downstream device must be in the range of 2.89 to 3.6V, by default. The higher voltage settings shown in Table 3-2 are optionally available for the downstream DP_PWR pin, as declared in the *x*V_DP_PWR_CAP bits in the NORP & DP_PWR_VOLTAGE_CAP register (DPCD Address 00004h, bits 7:5), and are enabled by an upstream device by setting the corresponding voltage's SET_DN_DEVICE_DP_PWR_*x*V bit in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 7:5),via AUX write transaction.

Upon detecting an upstream device disconnect event (which can be detected by monitoring the AUX+ common mode voltage transitioning from L level to H level, a downstream DP device generating DP_PWR voltage higher than the default +2.89 to +3.6V must reset its output voltage to the default setting. The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 650mA.

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a. *Self-powered capable Branch devices that are physically disconnected from their independent power source are effectively "not self-powered," and need not supply DP_PWR.*

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Table 3-2: DP_PWR Specification for Box-to-Box DisplayPort Connection

Parameter	Min	Nominal	Max	Unit	Comment
Voltage Range for Upstream DP_PWR	2.89	3.3	3.6	V	
Voltage Range for downstream device DP_PWR	2.89	3.3	3.6	V	Default DP_PWR voltage value for a downstream device
	4.9	5.0	5.5	V	"5V setting", enabled through AUX transaction[a]
	10.8	12	13.2	V	"12V setting", enabled through AUX transaction[a]
	16.2	18	19.8	V	"18V setting", enabled through AUX transaction[a]
Noise voltage for DOWNSTREAM DEVICE DP_PWR			100	mV	Peak-to-peak
Power Capacity per Upstream DP_PWR pin	1.5			W	• Full-height PC add-in card with multiple upstream DP connectors must power at least 3.0W per card • Half-height PC add-in card with multiple upstream DP connectors must power at least 1.5W per card • Upstream DP connector on PC motherboard must power 1.5W per connector, regardless of the number of connectors on the motherboard.
Current drawn by a downstream device from upstream DP_PWR pin			0.5	A	
Power Capacity per downstream DP_PWR pin	1.5			W	3.3V (default) setting
	3.2			W	5V setting
	7.0			W	12V setting
	10.5			W	18V setting
Current drawn by an upstream device from Downstream DP_PWR pin			0.5	A	3.3V (default) setting
			0.65	A	5V/12V/18V setting

a. *Self-powered capable Branch devices that are physically disconnected from their independent power source are effectively "not self-powered," and need not supply DP_PWR.*

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3.2.1 DP_PWR User Detection Method

Pins CONFIG1 and CONFIG2 of the box-to-box receptacle connector of upstream and downstream DP devices must be weakly pulled down with resistors. CONFIG1 must always use 1MΩ resistors. CONFIG2 must always use a 5MΩ (or larger) resistor if the upstream device is a dual-mode device and supports HDMI. In other cases, CONFIG2 can use either a 1MΩ or larger resistor. For more information, see VESA DisplayPort Interoperability Guideline v1.1a, Section 5.1.1.

Those two pins of a DP device with an upstream function that uses power from DP_PWR must be shorted by a ≤ 100Ω resistor.

A downstream device with a permanently attached cable that is capable of supplying power on the DP_PWR pin of the plug connector must verify that pins CONFIG1 and CONFIG2 are shorted before enabling its DP_PWR output.

To detect the presence of a DP_PWR User, a downstream device with a permanently attached cable must provide a probe power to Pin CONFIG2. If the Pin CONFIG1 voltage follows the probe power voltage applied to Pin CONFIG2, then, a DP_PWR User is present.

There will be a group of cable adaptors that pulls up Pin CONFIG1. Those cable adaptors with DP receptacle connectors that pull up Pin CONFIG1 must not be a DP_PWR User. When a downstream device with a permanently attached cable detects H level on Pin CONFIG1 before providing a probe power to Pin CONFIG2, it determines that the attached cable adaptor is not a DP_PWR User.

3.2.2 DP_PWR Wire

A standard DP cable must have no wire for the DP_PWR pin.

Only captive cables supplied with cable powered Branch devices or cables permanently attached to downstream devices or resizing adaptors or extension cables are permitted to have the wire for DP_PWR. These captive/attached/resizing/extension cables must have a full-size or mDP plug connector (as specified in Section 4.2.1) on one end only. The other end must either be permanently attached or have a DP receptacle connector or a custom connector.

3.2.3 Inrush Energy

DP devices that consume DP_PWR must limit the inrush energy during Hot Plug to 0.4mJ, to be measured over the time period that the inrush exceeds 0.6A, and measured at the nominal voltage for a given voltage level +10% (the maximum voltage for DP_PWR). It is recommended that the peak current is limited to ≤ 13.5A during the inrush energy window. The SCALE_FACT is equal to:

DEFAULT_VOLTAGE_SETTING / SELECTED_VOLTAGE_SETTING

For example, the SCALE_FACTOR is 1 when the 3.3V setting is selected, and 0.66 when the 5V setting is selected.

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3.2.4 Voltage Droop

DP devices that provide power at DP_PWR pin should have sufficient bypass capacitance per DP connector to be able to charge 56uF of low ESR capacitance plus 7.2Ω constant load across DP_PWR on hot plug of this load. It is recommended that power provider devices should exhibit no obvious system failure and should ensure that any resulting voltage droop is no more than 10% of the DP_PWR supply voltage on any other DP connectors (measured at the connector) on the system on hot plug of this load. Additionally, the device should, under the same condition, be able to support a momentary outrush peak current of 12A.

3.2.4.1 DP_PWR Loss and Recovery on Branch Device

If a Branch device which controls the HPD signal for any reason loses its ability to function normally (such as may happen due to an momentary out-of-spec droop in DP_PWR), it is recommended that the device, before resuming normal operation, either de-assert or disconnect its HPD signal (leaving it terminated to GND as per the HPD Downstream Device Termination requirement) until at such time as the device has fully recovered and can resume all normal operation.

If and when the device resumes normal operation, it should act as if it is coming out of reset or initial power-up with its DPCD registers set accordingly. Before resuming normal operation, the HPD signal should be de-asserted for a minimum of HPD_TimeOut and then re-asserted once the device has returned to normal functionality and can receive AUX communications.

3.2.5 Over-Current Protection

End-user accessible powered connectors must implement over-current protection for safety and regulatory reasons. Detection of an over-current condition and reporting this condition to the system software is optional and implementation-specific.

The preset trip limit must not exceed 3A at the upstream device connector DP_PWR pin and 1.5A at the downstream device connector DP_PWR pin. Limit must be above allowable current transients to avoid false trips. An over-current protection device must be resettable without user mechanical intervention.

A DP device with multiple DP_PWR outputs is permitted to use a single over-current protection device to protect all outputs. For devices using a single over-current protection device, the preset trip limit must be 3A per device with upstream device connectors and 1.5A per device with downstream device connectors. There is no requirement to maintain the DP_PWR specification on one port in the presence of a fault condition on another port.

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3.3 Hot Plug/Unplug Detect Circuitry

The HPD signal is asserted by the downstream DP device whenever the downstream device is connected to either its main power supply or "trickle" power. HPD signal specification is shown in Table 3-3.

Table 3-3: Hot Plug Detect Signal Specification

Parameter	Minimum	Nominal	Maximum	Unit	Comment
HPD Voltage	2.25		3.6	V	HPD signal to be driven by the downstream device.
Hot Plug Detection Threshold	2.0			V	HPD signal to be detected by the upstream device.
Hot Unplug Detection Threshold			0.8	V	
HPD Upstream Device Termination	100			kΩ	Upstream device must pull down its HPD input with a ≥ 100kΩ resistor.
HPD Downstream Device Termination	100			kΩ	When a downstream device is off, it must pull down its HPD output with a ≥ 100kΩ resistor.
IRQ_HPD Pulse Width Driven by Downstream Device	0.5		1.0	ms	Downstream device generates a low-going pulse within this range for IRQ (interrupt request) to the upstream device.
IRQ_HPD Pulse/Glitch Detection Threshold for Upstream Device	0.25			ms	When the pulse width is narrower than this threshold, the upstream device must ignore the pulse as a glitch.
IRQ_HPD Pulse/ Hot Unplug Event Detection Threshold for Upstream Device	2.0			ms	When the pulse width is narrower than this threshold, the upstream device must read the Link/Sink Device Status field (DPCD Addresses 00000h through 000FFh; see Table 2-157) first and take corrective action. When the pulse width is wider than this threshold, it is likely to be actual cable unplug/re-plug event. Upon detecting HPD high, the upstream device must read the Link/Sink Device Status field, and if the link is unstable, read the Link/Sink Capability field of the DPCD before initiating Link Training.
IRQ_HPD Minimum Spacing	2.0			ms	Minimum Time after asserting HPD at the end of IRQ_HPD before de-asserting HPD at the start of the following IRQ_HPD.

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The voltage level of the HPD pin is monitored by the upstream device. TTL levels must be used for the detection.

The downstream device may detect the presence of the upstream device by monitoring the DC voltage level of the AUX CH lines. For a detachable downstream device whose power is not provided by the upstream device's DP_PWR, upstream device detection is a required feature.

Upstream implementations are recommended to implement de-bouncing of the HPD signal on an external connection. A period of 100ms is recommended for the detection of an HPD connect event (i.e., the event, "HPD high", is confirmed only after HPD has been asserted continuously for 100ms). Care should be taken not to implement de-bouncing on an IRQ_HPD and on a downstream device-generated pair of HPD disconnect/reconnect events (typically HPD will be de-asserted for more than 2ms, but less than 100ms in this case). To cover these cases, it is recommended that the HPD de-bounce is only implemented after HPD low has been detected for 100ms. Timing requirements in this Standard related to the detection of HPD high are to be interpreted as applying from the completion of an implementation-dependent de-bounce period.

If the downstream device has been placed in a low-power mode (see Section 5.1.5) but detects an event that it needs to notify to the upstream device, then it asserts IRQ_HPD. The upstream device will attempt to perform AUX transactions to wake the downstream device. It is possible for the upstream device already to be making AUX transactions to wake up the downstream device. In this case, the upstream device must complete the actions that it was already in process of execution (e.g., waking the link and initiating training), and then perform appropriate DPCD register reads to ascertain the cause of the IRQ_HPD.

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3.4 AUX Channel

The DP AUX Channel is a half-duplex, bidirectional channel consisting of one differential pair as shown in Figure 3-15, supporting the bit rate of about 1Mbps.

Note: *The 50Ω termination resistors may be integrated on-chip. The AUX Channel is doubly terminated with 50Ω termination resistors on both ends, and AC-coupled on the DPTX end.*

Figure 3-15: AUX CH Differential Pair

The upstream DP device must weakly pull down the AUX+ line to GND and weakly pull up the AUX- line to DP_PWR each with a resistor in the range 10kΩ to 105kΩ between the AC-coupling capacitor and the upstream device connector to assist detection of the upstream DP device and powered upstream DP device by the downstream device. A nominal 100kΩ resistor value is recommended.

All downstream devices must have AC-coupling capacitors, regardless of whether they implement upstream DP device detection. The downstream devices must very weakly pull up AUX+ line and very weakly pull down AUX- line with 1MΩ (±5%) resistors between the downstream device connector and the AC-coupling capacitors. When AUX+ line DC voltage is L level, it means an upstream DP device is connected. When AUX- line DC voltage is H level, it means that a powered upstream DP device is connected.

The AUX CH uses Manchester-II coding for the self-clocked transmission of signals, as shown in Figure 3-16.

Figure 3-16: Self-clocking with Manchester-II Coding

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3.4.1 AUX Channel Logical Sub-block

Between transactions, the AUX Channel is in an electrical idle state. In the electrical idle state, neither device is driving the channel and, thus, both AUX-CH+ and AUX-CH- are at the termination voltage.

AUX Channel transactions are initiated by the DPTX, which acts as an AUX CH requester. The DPTX, which is the driving end for a request transaction, pre-charges the AUX-CH+ and AUX-CH- to a common mode voltage by transmitting 10 to 16 consecutive 0s in Manchester-II code.

After the active pre-charge, the DPTX sends an AUX Sync pattern. The AUX Sync pattern must be as follows:

- Start with 16 consecutive 0s in Manchester-II code, which results in a transition from low to high in the middle of each bit period. Including active pre-charge pulses, there must be 26 to 32 consecutive 0s before the end of the AUX Sync pattern.
- End with the AUX-CH+ driven to high for a 2-bit period (which is 2us when the bit rate is 1Mbps) and low for a 2-bit period, which is illegal in Manchester-II code. The AUX-CH- must be driven to the opposite polarity.

The receiving end, which is the DPRX for the request transaction, must lock to this Sync pattern.

Following the Sync pattern, the driving end must send data according to the AUX CH syntax as described Section 2.8. When it has finished sending data, the driving node must assert the STOP condition. The STOP condition must be as follows:

- Drives AUX-CH+ to high and AUX-CH- to low for a 2-bit period, then AUX-CH+ to low and AUX-CH- to high for a 2-bit period, which is an illegal sequence for Manchester-II
- Releases AUX CH immediately after the STOP condition
- AUX Sync pattern and STOP condition are shown in Figure 3-17

The DPRX, the AUX CH replier, replies to this request transaction. The DPRX, now acting as a driving end, must let the bus park for at least 10ns, then pre-charges the bus to the common mode voltage with 10 to 16 pre-charge pulses, and initiates the reply transaction. The Sync pattern and the STOP condition are the same for a request and a reply transaction.

Figure 3-17: AUX CH SYNC Pattern and STOP Condition

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3.4.2 AUX Channel Electrical Sub-block

Table 3-4 shows the electrical specification of the DisplayPort AUX Channel.

Table 3-4: DisplayPort AUX Channel Electrical Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI_{MAN}	Manchester transaction unit interval	0.4		0.6	us	Results in the bit rate of 1Mbps including the overhead of Manchester-II coding.
Pre-charge Pulses	Number of pre-charge pulses	10		16		Each pulse is a 0 in Manchester-II code.
$T_{AUX\text{-}BUS\text{-}PARK}$	AUX CH bus park time	10			ns	Period after the AUX CH STOP condition for which the bus is parked.
$T_{cycle\text{-}to\text{-}cycle\ jitter}$	Maximum allowable UI variation within a single transaction at connector pins of a transmitting device			0.08	UI	Equal to 48ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a transmitting device			0.04	UI	Equal to 24ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
	Maximum allowable UI variation within a single transaction at connector pins of a receiving device			0.10	UI	Equal to 60ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
	Maximum allowable variation for adjacent bit times within a single transaction at connector pins of a receiving device			0.05	UI	Equal to 30ns maximum. The transmitting device is an upstream device for a Request Transaction and a downstream device for a Reply Transaction.
$V_{AUX\text{-}DIFFp\text{-}p_TX}$	AUX peak-to-peak voltage at a transmitting device when transmitting	0.29		0.40[a]		$V_{AUX\text{-}DIFFp\text{-}p}$ $= 2 * \lvert V_{AUX_CH_P} - V_{AUX_CH_N} \rvert$
	AUX peak-to-peak voltage at a receiving device when transmitting	0.27		0.38[a]		
$V_{AUX\text{-}DIFFp\text{-}p_RX}$	AUX peak-to-peak voltage at a transmitting device when receiving	0.29		1.38		
	AUX peak-to-peak voltage at a receiving device when receiving	0.27		1.36		
$V_{AUX_TERM_R}$	AUX CH termination DC resistance		100		Ω	Informative.

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Table 3-4: DisplayPort AUX Channel Electrical Specifications (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{AUX\text{-}DC\text{-}CM}$	AUX DC common mode voltage	0		2.0	V	Common mode voltage is equal to Vbias_TX (or Vbias_RX) voltage.
$V_{AUX\text{-}TURN\text{-}CM}$	AUX turn around common mode voltage			0.3	V	Steady state common mode voltage shift between transmit and receive modes of operation.
I_{AUX_SHORT}	AUX short circuit current limit			90	mA	Total drive current of the transmitter when it is shorted to its ground.
C_{AUX}	AUX AC-coupling capacitor	75		200	nF	The AUX CH AC-coupling capacitor placed on both the DP upstream and downstream devices.

a. *To reduce the near-end crosstalk (NEXT) to Main-Link differential signals from AUX reply transactions (where the DPRX is transmitting differential signals over AUX CH lines), the maximum AUX CH differential voltage swing has been reduced to 0.40V_diff_pp at the transmitting connector pins for a DPRX operating at HBR3. In the previous version of this Standard, the maximum voltage swing was 1.38V_diff_pp.*

3.4.2.1 AC-Coupling

The DP AUX Channel must be AC-coupled. The minimum and maximum values for the capacitance are specified in Table 3-4. The requirement for the inclusion of AC-coupling capacitors on the interconnect media is specified at the DPTX.

3.4.2.2 Termination

The DP AUX Channel should meet the termination resistance specified in Table 3-4 at all times when the link is active.

3.4.2.3 DC Common Mode Voltage

To facilitate the minimum bus turnaround delay, the transmitting side must provide between 10 and 16 Manchester-II code 0s as pre-charge pulses at the start of a Manchester-II transaction. The steady state common mode voltage between transmit and receive modes of operation must not exceed $V_{AUX\text{-}TURN\text{-}CM}$, as specified in Table 3-4.

Upstream and downstream devices must be designed to tolerate a power-on, power-off or Hot Plug event presenting the maximum charge redistribution of 720nC caused by $V_{AUX\text{-}DC\text{-}CM}$ (2.0V maximum) and C_{AUX} (200nF maximum) for the maximum period of maximum Pre-charge Pulses x UI_{MAN} (Manchester transaction Unit Interval) or greater.

3.4.2.4 Short Circuit Requirements

Driver and receiver circuits of the AUX CH block must survive the worst-case short-circuit current of 90mA (3.6V over 40Ω).

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3.4.2.5 Differential Voltage/Timing (EYE) Diagram

The AUX CH_EYE mask at the connector pins of the transmitting device and its vertices values are shown in Figure 3-18 and Table 3-5, respectively. The AUX CH_EYE mask at the connector pins of the receiving device and its vertices values are shown in Figure 3-19 and Table 3-6, respectively.

Figure 3-18: AUX CH EYE Mask at Connector Pins of TX Device

Table 3-5: Mask Vertices for AUX CH at Connector Pins of TX Device

Point	Time (from Eye Center) (ns)	Minimum Voltage Value at Six Vertices (mV)
1	-185	0
2	-135	145
3	135	145
4	185	0
5	135	-145
6	-135	-145

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Figure 3-19: AUX CH EYE Mask at Connector Pins of RX Device

Table 3-6: Mask Vertices for AUX CH at Connector Pins of RX Device

Point	Time (from Eye Center) (ns)	Minimum Voltage Value at Six Vertices (mV)
1	-185	0
2	-135	135
3	135	135
4	185	0
5	135	-135
6	-135	-135

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3.5 Main-Link

This section describes the functions of the DP Main-Link PHY Layer.

3.5.1 Main-Link Logic Sub-block

The Logical Sub-block of DP Main-Link PHY Layer performs the following functions:

- Scrambling and de-scrambling (see Section 3.1.6)
- ANSI 8b/10b encoding/decoding (see Section 3.1.7 and Section 3.5.1.1)
- Serialization and de-serialization (see Section 3.1.7)
- Link Training and Link Status Monitor (see Section 3.5.1.2 and Section 3.5.1.3)
- Link Quality Measurement (Testability; see Section 3.5.1.4)
- Forward Error Correction (FEC; see Section 3.5.1.5)

3.5.1.1 ANSI 8b/10b Special Characters used for DP Control Link Symbols

In this Standard, various Control Link Symbols are defined in the Link Layer for use on the Main-Link lanes in SST and MST modes.

Table 3-7 shows which ANSI 8b/10b special characters are used for those Control Link Symbols. Unused special characters are reserved for future use and shall not be used by a DP-compliant link.

Table 3-7: ANSI 8b/10b Special Characters for DP Control Link Symbols

Special Character	Control Link Symbol in SST Enhanced Mode[a]	Control Link Symbol in SST Enhanced Mode with FEC	Control Link Symbol in MST Mode[b]
K23.7	FE	FE[c]	Indexed 0[c]
K27.7	BE	BE	Indexed 1
K28.0	SR	SR	Indexed 2
K28.1	CP	PM[c]	PM[c]
K28.2	SS	SS	Indexed 3
K28.3	BF	BF	Indexed 4
K28.4	RESERVED	CP	Direct RESERVED
K28.5	BS	BS	Direct SR
K28.6	EOC[d]	EOC[d]	Indexed 5
K28.7	RESERVED	RESERVED	Direct RESERVED
K29.7	SE	SE	Indexed 6
K30.7	FS	FS	Indexed 7[c]

a. See Section 2.2.1.1 and Section 2.2.1.2 for definitions of these control symbols in SST mode.
b. See Table 2-139 for definitions of these control symbols in MST mode.
c. Parity Marker (PM) is used when FEC is enabled. K23.7 and K30.7 are used in FEC_DECODE_EN and FEC_DECODE_DIS sequences. (For details regarding FEC, see Section 3.5.1.5.)
d. End of Chunk (EOC) is used for DSC Transport. (For details regarding DSC Transport, see Section 2.7.) In MST mode, EOC is mapped to C2-C2-C2-C2, as listed in Table 2-139.

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3.5.1.2 Link Training

For an open, box-to-box connection, the upstream DP device configures the link through a Link Training sequence. One exception is when the upstream DP device is resuming a transmission. In this condition, the upstream device may skip the AUX transactions for Link Training, as described in Section 2.9.4.3.

For a closed, embedded connection, the DPTX and DPRX may be set to pre-calibrated parameters without going through the full Link Training sequence. In this mode, the upstream DP device may start a normal operation without the AUX transactions for link training, as described in Section 2.9.4.3.

Link training consists of two distinct tasks which must be completed successfully in sequence to establish the link:

- **Clock Recovery** – Locks the DPRX CR (clock recovery) PLL to the repetition of D10.2 data symbols
- **Channel Equalization/Symbol-Lock/Inter-lane Alignment** – When successful, the Symbol-Lock and Inter-lane alignment must be achieved by the end of this sequence

The training sequence is initiated by Link Policy Maker in the upstream device to establish a link with the downstream device. Link Policy Maker must first detect that the HPD signal is asserted high by the downstream device. Before initiating the link training sequence, Link Policy Maker must read the downstream device's Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155) or Extended Receiver Capability field (DPCD Addresses 02200h through 022FFh; see Table 2-165) registers (if the downstream device supports the Extended Receiver Capability field) for the following two conditions:

- Hot Plug Detect event (namely, HPD low-going pulse exceeding 2 ms)
- With a downstream device whose DPCD Revision is 1.2 or higher, an IRQ_HPD pulse with the RX_CAP_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 0) set to 1

Link Policy Maker must read the Receiver Capability and Extended Receiver Capability fields via AUX CH. Link Policy Maker must then determine the link configuration based on the DPRX's capability and its own needs, and then write the following Link Configuration parameters:

- LINK_BW_SET register (DPCD Address 00100h)
- LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0)
- DOWNSPREAD_CTRL register (DPCD Address 00107h)
- MAIN_LINK_CHANNEL_CODING_SET register (DPCD Address 00108h)

After writing Link Configuration parameters, Link Policy Maker must start link training by writing 21h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) via AUX CH, while instructing its transmitter's logical PHY Layer to start transmitting training patterns.

Link Configuration parameters written to by Link Policy Maker must not be changed after training has commenced until the next time the link is trained, except as described below for falling back to lower link bandwidth and/or reduced lane count on training failure.

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Writing 21h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) via AUX CH by an upstream DP device must be preceded by the change of transmitted training pattern over the Main-Link. Whenever the TRAINING_PATTERN_SET register is written to, the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h) of the enabled lane(s) must also be written to.

Note: *The number of enabled lanes is written to the LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0) prior to Link Training. The AUX CH burst write must be used for writing to TRAINING_LANEx_SET register(s) of the enabled lane(s). An upstream device may write to the TRAINING_PATTERN_SET and TRAINING_LANEx_SET registers in one AUX CH burst write transaction.*

A per-lane drive setting adjustability is an optional feature of a DPTX of an upstream device. If a DPRX requests different drive settings among multiple (two or four) lanes, a DPTX may use the setting of highest pre-emphasis level and voltage swing of all the requested settings.

When the combination of the requested pre-emphasis level and voltage swing exceeds the capability of a DPTX, the DPTX must set the pre-emphasis level according to the request and use the highest voltage swing it can output with the given pre-emphasis level.

A DPRX must issue a drive setting adjustment request within limits defined in this Standard.

When a DPTX reads a request beyond the limits of this Standard, the DPTX must set the pre-emphasis level according to the request and set the highest voltage swing level it can output with the given pre-emphasis level. If a DPTX is requested for 9.5dB of pre-emphasis level (the support of which is optional for a DPTX) and cannot support that level, it must set the pre-emphasis level to the next highest level, 6dB.

Table 3-8 shows the link training symbol patterns. All devices must support TPS1 and TPS2. An HBR2-capable device must also support TPS3.

An HBR3-capable device must also support TPS4. A downstream device that is capable of supporting TPS4 must advertise this capability by setting the TPS4_SUPPORTED bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 7). An upstream device that supports TPS4 must inspect the TPS4_SUPPORTED bit in the connected downstream device. If the upstream device finds the bit set, the upstream device must write 07h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and transmit TPS4 during the Channel Equalization phase of link training (regardless of the speed at which the link is being trained).

In all other cases, the upstream device must transmit TPS2 (or TPS3 in case a downstream device supports TPS3) during the Channel Equalization phase of link training. If training without AUX transactions, the use of TPS4 is determined either as the result of a previous training phase on the same connection, or by implementation-dependent system configuration means (e.g., on eDP).

A DPTX must transition from TPS2/3/4 to a non-training pattern at a link symbol boundary without any gap in between. The DPTX is allowed to transition to a non-training pattern in the middle of a link training pattern.

Unless training without AUX transactions, a DPRX may request for adjustment of differential voltage swing, pre-emphasis, or both during the Clock Recovery phase and Channel Equalization phase of the link training procedure, as shown in Figure 3-20 and Figure 3-21.

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Table 3-8: Symbol Patterns of Link Training

Pattern Number	Purpose	Name
TPS1	For locking clock recovery circuit of the DPRX	Repetition of D10.2 characters without scrambling
TPS2	For setting equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, D11.6, K28.5+, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2 without scrambling
TPS3	For setting equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, K28.5+, K28.5-, K28.5+, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, K28.5-, K28.5+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+ without scrambling
TPS4	For setting equalization, determining symbol boundary, and achieving inter-lane alignment	Same as CP2520 Pattern 3 defined in *VESA DisplayPort PHY Compliance Test Specification Version 1.2b* K28.0-, K28.5-, K28.5+, K28.0-, 248 00s after data symbol scrambling and ANSI 8b/10b coding (252 of 10 binary bits listed in Section 3.5.1.2.1 for clarity; the right-most bit is the least significant bit and is transmitted first, and the left-most bit is the most significant bit and is transmitted last)

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3.5.1.2.1 TPS4 Bit Sequence

0010111100

0101111100

1010000011

0010111100

1000110101

0010010111

0110111001

0010110100

0101110010

0111000111

1101010010

1011010010

1100110010

1100001110

1001011000

0101100110

0101011110

1100001101

0101001010

1011001101

0101100001

1010111001

0101111000

1000100110

1001101100

0110010011

1000101101

0101110010

1101000111

1101010010

0011101000

1001101010

0110001101

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1001110100

0101011110

0111000110

0101111000

1010100010

1001101011

0101110001

1011100100

0101010001

0101011101

1001010010

0110110100

1010100101

0010011101

0110010011

0110010111

1000101010

0011010110

0111001110

1001101100

0110011010

0010011010

0111011010

1001011000

1001001101

1001010110

1001011011

1001011010

0010001110

1100111010

1100111000

0110000101

1101100110

1010101100

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1001100110

0110010011

1000101001

1001011010

0110001101

1001000111

0011010110

1001110110

1000011100

1011110100

0100001011

1101100011

0110100001

0110010011

1101100110

1010110010

1000010110

1010111010

1011011000

1011000110

0100010101

0110101011

1100101010

1100100110

1000110010

0100110101

1101101100

0101010001

1001010101

1000101101

1010101110

0110000101

1001000111

0011110100

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1010111001

0011100001

0100011110

0101100101

1010110011

0111100001

1011010100

0010101001

1100111001

1101011000

0101101001

1000110001

1101001011

0011000101

1100101101

1101101000

1010100011

1010011100

0001001101

1010100111

1001011001

1001001010

0110110100

1010011010

0111010101

0010001110

0101010011

0110000111

1101100011

1011100010

1011100100

0100001011

1101001101

0100001110

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1010011100

1001010011

0100110011

1100010111

0101001110

1001001101

0101101100

0010001011

1001011110

0110011010

0010001011

1010101101

1100011010

1100011100

0110110001

0110000101

0101100111

0010011100

1101110010

0001001110

1010101110

0110010010

1001110101

1001001100

0011011010

1101001101

1100101001

1000110100

0010101110

0110011010

1001110001

0011110010

0110100101

0101111001

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0110101000

1011010011

0010001110

0110011100

0101111010

0101010100

1010010101

0111000111

0111001001

1100110010

0010010110

1100100111

0110010101

1001001100

0100101011

0110011101

1101000110

0110001101

1101001100

1011100001

0110101010

1001001001

1010011001

1010101100

0011010101

0010011011

1100010111

1001110001

0110100101

0001001101

0110111010

0100110001

1100101011

1100001110

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1001100010

1000011110

1000100111

1001101001

0010101011

0110111010

1100101100

1000011100

0110101011

0010001011

1010011110

0110011010

0011010010

0101011010

1010011011

0101001011

0110001010

1010011001

0101010111

0011100010

1001010111

1010100001

0111100011

0010011010

0110100110

0100100111

1101110100

1000010101

1010111010

0100001011

0110100111

1010010110

0110001011

0110010011

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1101001001

1010010010

0011100011

0010101011

1011101010

0101110100

0111101000

1011010100

1101010001

0101000110

0010101110

1011100011

1010101001

1100111000

0001001110

The link training sequence, regardless of whether there is an accompanying AUX transactions, must always start with negative disparity. Link Training Pattern of Channel Equalization phase must start with K28.5- for TPS2, K28.5- for TPS3, and K28.0- for TPS4.

For complete DPCD address mapping, see Table 2-154.

3.5.1.2.2 Clock Recovery Sequence

Link training begins with the Clock Recovery (CR) sequence. The link symbols transmitted in this sequence are a repetition of D10.2 data symbols with scrambling disabled (TPS1). In this sequence, the transmitter must normally start signaling at voltage swing level 0, pre-emphasis level 0. The upstream device commences transmission of TPS1, and then writes 21h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and the current drive setting to the TRAINING_LANE*x*_SET register(s) (DPCD Address(es) 00103h through 00106h).

The upstream device may start Full Link Training with non-minimum differential voltage swing and/or non-zero pre-emphasis if the optimal setting is already known, for example, as is the case in embedded application. In this case, the upstream device must write the swing and pre-emphasis settings at which it is starting training to the TRAINING_LANE*x*_SET register(s) as part of the burst write in which it writes 21h to TRAINING_PATTERN_SET register.

In CR sequence, the transmitter must wait for at least 100us before issuing a read request AUX transaction for reading the Lane's LANE*x*_CR_DONE bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate), which are set by the receiver.

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Unless all the LANE*x*_CR_DONE bits are set, the transmitter must do the following:

- Read both ADJUST_REQUEST_LANE*x_y* register(s) (DPCD Address(es) 00206h and 00207h),
- Adjust the voltage swing and/or pre-emphasis level according to the request, and
- Update the TRAINING_LANE*x*_SET register(s) to match the new voltage swing and/or pre-emphasis settings.

The receiver sets the LANE*x*_CR_DONE bit(s) only when its link CDR (clock and data recovery) unit has realized and maintained the frequency lock. For optimizing the drive setting of the transmitter, the receiver may defer setting LANE*x*_CR_DONE bits until the optimization is completed.

The receiver must set the LANE*x*_CR_DONE bit(s) on those lanes for which CR lock is achieved in the DPCD. Otherwise, the receiver must keep the LANE*x*_CR_DONE bits cleared and request an adjustment of the differential voltage swing and/or an adjustment of the pre-emphasis level, by updating the value in the ADJUST_REQUEST_LANE*x_y* register(s).

The transmitter must down-shift to the lower link rate and repeat the CR sequence when any of the following conditions are met:

- Receiver keeps the same value in the ADJUST_REQUEST_LANE*x_y* register(s) while one or more of the LANE*x*_CR_DONE bit(s) remain unset after five AUX_ACKs for read request transactions for reading LANE*x*_CR_DONE bit(s) and ADJUST_REQUEST_LANE*x_y* registers, the transmitter must loop five times with the same voltage swing.
- Receiver fails to set all the LANE*x*_CR_DONE bit(s) after the transmitter has transmitted the maximum voltage swing level, which is the sum of the VOLTAGE_SWING_LEVEL and PREEMPHASIS_LEVEL value.
- Receiver fails to set all the LANE*x*_CR_DONE bit(s) on the enabled lanes following a total of 10 AUX_ACKs for read request transactions for reading LANE*x*_CR_DONE bit(s) and ADJUST_REQUEST_LANE*x_y* register(s).

Section 3.1.5.2 gives the voltage swings that the transmitter must support.

To re-initiate training at a lower link rate, the upstream device does the following:

1. Clears the TRAINING_PATTERN_SET register (DPCD Address 00102h).
2. Starts transmitting TPS1 (D10.2) at the lower rate at the default voltage swing and pre-emphasis (400mV, no pre-emphasis).
3. Writes 21h to the TRAINING_PATTERN_SET register (and appropriate values to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h)) to initiate training

After it reads the LANE*x*_CR_DONE bit(s) set for all enabled lanes, the transmitter's Link Policy Maker must move on to the next stage, namely, Channel Equalization sequence.

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3.5.1.2.2.1 Fallback Requirements in Case of Clock Recovery Failure on Lower-count Lanes

There is a possibility that the number of physical connections between a transmitter in an upstream device and a receiver in a downstream device is lower than the maximum number of lanes that the receiver supports. For example, only Lanes 0 and 1 can be connected even when a receiver supports up to four lanes. In this case, the Clock Recovery sequence of Link Training is likely to fail on higher-count lanes that have no physical connections (Lanes 2 and 3 in the above example).

Figure 3-20 describes the required behavior of an upstream DP device with DPTX's Link Policy Maker in the above scenario.

The behavior of an upstream DP device upon LANE*x*_CR_DONE on all four lanes but fails in the Channel Equalization phase of Link Training is an implementation-specific choice. Attempting of a reduced lane count is a recommended practice.

Figure 3-20: Clock Recovery Sequence of Link Training

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The upstream device, after reducing the link rate to RBR upon failure of the LANE*x*_CR_DONE bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively) on all the enabled lanes, must check whether it is the lowest numbered lanes that have the LANE*x*_CR_DONE bits set. If that is the case, the upstream device must reduce the lane count to match those LANE*x*_CR_DONE lanes and then set the link rate to the highest desirable link rate, then continue with the LANE*x*_CR_DONE sequence of Link Training.

Note that with the reduced lane count, only the following lane combinations are valid:

- 1-lane configuration = Lane 0 enabled and Lanes 1, 2, and 3 disabled
- 2-lane configuration = Lanes 0 and 1 enabled and Lanes 2 and 3 disabled

3.5.1.2.3 Channel Equalization Sequence

The Channel Equalization (EQ) sequence starts with the transmitter drive setting as set at the end of Clock Recovery sequence.

In the EQ sequence, the upstream device transmits the appropriate pattern (TPS2, TPS3, or TPS4) with scrambling disabled for TPS2 and TPS3 and enabled for TPS4. The upstream device then writes 22h for TPS2, 23h for TPS3, or 07h for TPS4 to the TRAINING_PATTERN_SET register (DPCD Address 00102h) and the current drive setting to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h).

The transmitter must wait at least the period of time specified in the TRAINING_AUX_RD_INTERVAL field in the TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bits 6:0) after programming 22h for TPS2, 23h for TPS3, or 07h for TPS4 to the TRAINING_PATTERN_SET register before reading the link status bits.

The bits are transported from the left most bit first (lsb) to the right most bit last (msb). The transmitter must insert a two-link-symbol inter-lane skew between adjacent lanes, as shown in Figure 2-15.

The receiver must use the recognition of this training pattern to decide whether the channel equalization is successful or not. How to measure the equalization result is implementation-specific.

Section 3.1.5.2 gives the voltage swings and pre-emphasis level combinations that the transmitter must support. The receiver must indicate success by setting the following register bits:

- Lane's LANE*x*_CHANNEL_EQ_DONE bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 1 and 5, and DPCD Address 00203h, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
- Lane's LANE*x*_SYMBOL_LOCKED bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 2 and 6, and DPCD Address 00203h, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively, as appropriate)

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- INTERLANE_ALIGN_DONE bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively)

The receiver sets the LANE*x*_SYMBOL_LOCKED bit(s) only when it has properly detected and aligned the ANSI 8b/10b symbol boundaries. Given the bit error rate target of $1E^{-9}$ and the duration of the link training period (which can be 10ms or less, though it might take a few hundreds of milliseconds, depending on the number of iterations needed for completion), the receiver should detect no more than a single symbol error during the link training to set the LANE*x*_SYMBOL_LOCKED bits. To optimize the DPTX's drive setting, the DPRX can defer setting the LANE*x*_SYMBOL_LOCKED bits until optimization is complete.

The receiver sets the INTERLANE_ALIGN_DONE bits only when its PHY Layer digital sub-block has successfully aligned the symbol boundaries of all the enabled lanes with one another so that the Link Layer block can handle the incoming symbol patterns. For optimizing the drive setting of the DPTX, the DPRX may defer setting INTERLANE_ALIGN_DONE bit until the optimization is completed.

During the normal operation following the link training, the receiver must clear the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits when its Link Layer block can no longer process the incoming symbol patterns due to symbol errors, and thus causing noticeable visible/audible glitches to the regenerated streams. The receiver must otherwise maintain these bits during normal operation. The receiver must not clear these bits upon isolated Symbol errors. Guidelines for Symbol-error resiliency of the receiver are given in Appendix C.

The transmitter must read the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits, as well as the ADJUST_REQUEST_LANE*x*_*y* register(s) (DPCD Address(es) 00206h and 00207h). Unless all status bits are 1, the transmitter must then adjust the drive setting according to the receiver's request, and write the new setting to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h).

The minimum loop count in this sequence is one, while the maximum loop count in this sequence (see Figure 3-21) is five. When not training at RBR and one or more of the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits remain unset in the sixth loop, the transmitter must down-shift to the next lower bit rate. To re-initiate training at a lower bit rate, the upstream device does the following:

1. Clears the TRAINING_PATTERN_SET register (DPCD Address 00102h).
2. Starts transmitting TPS1 (D10.2) at the lower rate at the default voltage swing and pre-emphasis (400mV, no pre-emphasis).
3. Writes 21h to the TRAINING_PATTERN_SET register (and appropriate values to the TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h)) to initiate training.

At the end of the successful EQ sequence (with all the LANE*x*_SYMBOL_LOCKED and INTERLANE_ALIGN_DONE bits set by the receiver), the transmitter must clear the TRAINING_PATTERN_SET register to 00h.

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The receiver, with its own equalizer (optional), may adjust its equalizer setting(s) in each training loop. The receiver may optionally issue up to seven consecutive AUX DEFERs, if needed. However, it is strongly recommended that usage of AUX DEFER be minimized to meet the Link Training completion time target of 10ms. When the transmitter receives more than seven consecutive AUX DEFERs, it may terminate the Link Training.

It is recommended that the receiver not set the following register bits right after the successful reception of training patterns:

- Lane's LANE*x*_CHANNEL_EQ_DONE bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 1 and 5, and DPCD Address 00203h, bits 1 and 5, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
- Lane's LANE*x*_SYMBOL_LOCKED bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 2 and 6, and DPCD Address 00203h, bits 2 and 6, for Lanes 0, 1, 2, and 3, respectively, as appropriate)
- INTERLANE_ALIGN_DONE bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively)

Rather, the receiver should either increase its own equalization level or request a stronger pre-emphasis. When such action results in loss of successful reception, the receiver must restore or request the last setting. The purpose of this methodology is to ensure the maximum operating margin.

3.5.1.2.3.1 Fallback Requirements in Case of Symbol Lock Failures in 2- and 4-Lane Configurations

There is a possibility for Symbol Lock failure in a 2- or 4-lane configuration because only one lane (2-lane configuration) or two lanes (4-lane configuration) are available for a DP Main-Link. In such a condition, the LANE*x*_CR_DONE sequence over two or four lanes should have failed. However, it is known that that there are DPRX implementations that erroneously set LANE*x*_CR_DONE bit on all lanes.

In the event of the Symbol Lock failure in a 4-lane configuration, the DPTX shall attempt to return to the LANE*x*_CR_DONE sequence after reducing the lane count to two lanes (i.e., writing the value of 02h to the LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0) at the same link rate, as illustrated in Figure 3-21.

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Figure 3-21: Channel Equalization Sequence of Link Training

Upon verifying that the Channel Equalization/Symbol-Lock/Inter-lane Alignment are all done, the transmitter must write 00h to the TRAINING_PATTERN_SET register (DPCD Address 00102h) to indicate the end of training, and then start transmission of stream data.

If the Clock Recovery circuit loses lock during the Channel Equalization sequence, the receiver must clear the Lane's LANE*x*_CR_DONE bit in the LANE*x*_*y*_STATUS register(s) (DPCD Address 00202h, bits 0 and 4, and DPCD Address 00203h, bits 0 and 4, for Lanes 0, 1, 2, and 3, respectively, as appropriate). If it is in the high bit-rate mode, the transmitter must then reduce the bit-rate and return to the CR training sequence. If it is already in the RBR mode, then the transmitter must end the training by writing 00h to the TRAINING_PATTERN_SET register, without establishing the link.

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3.5.1.2.4 POST-LT_ADJ_REQ (Post-Link Training Adjust Request) Sequence

A downstream device can optionally support the Post-Link Training Adjust Request sequence to further fine-tune the transmitter drive setting and its own receiver equalization setting in case the upstream device does not support TPS4. Post-LT_ADJ_REQ uses a randomized ANSI 8b/10b transmission pattern instead of TPS2/TPS3.

A downstream device supporting this feature sets the POST_LT_ADJ_REQ_SUPPORTED bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 5) to declare the support to the upstream device. The upstream device grants the Post-LT_ADJ_REQ process by setting the POST_LT_ADJ_REQ_GRANTED bit in the LANE_COUNT_SET register (DPCD Address 00101h, bit 5).

The downstream device, upon setting Link/Sink Device Status registers DPCD Addresses 00202h through 00204h and DPCD Addresses 0200Ch through 0200Eh to indicate the completion of link training, sets the POST_LT_ADJ_REQ_IN_PROGRESS bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 1, respectively) to initiate the process, as described in Figure 3-22.

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Figure 3-22: POST_LT_ADJ_REQ Sequence

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3.5.1.3 Link Maintenance

The downstream device must maintain the Link Status flags in the following registers during normal operation:

- LANE*x*_*y*_STATUS register(s) (DPCD Address(es) 00202h and 00203h)
- LANE_ALIGN__STATUS_UPDATED register (DPCD Address 00204h)

Upon loss of synchronization with the upstream device for any reason other than after receiving a request to program the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) to 10b, or to request re-training the link for any reason, the downstream device must do the following:

1. Clear the INTERLANE_ALIGN_DONE bit in the LANE_ALIGN__STATUS_UPDATED register (DPCD Address 00204h).
2. Generate a distinct IRQ_HPD (i.e., distinct from an IRQ_HPD generated for any other reason).

The transmitter must check the link status whenever it detects a low-going IRQ_HPD pulse during normal operation and perform re-training of the link as needed. See Appendix C for recommendations for Link Quality Maintenance.

3.5.1.4 Link Quality Measurement (Testability)

The DPTX must be able to transmit test patterns for link quality measurement purposes as indicated in Section 2.9.4.5. The DPTX indicates which test pattern (if any) is currently active on each lane, by writing to the LINK_QUAL_LANE*x*_SET register(s) (DPCD Address(es) 0010Bh through 0010Eh). Using these registers to determine which test pattern is being received, the DPRX must support the following:

- **Recovered Link Clock Quality Measurement** – Outputs the recovered link clock from a test pad when the upstream DP device writes to the RECOVERED_CLOCK_OUT_EN bit in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bit 4). The output clock frequency must be 1/40 of the link clock frequency.

  The purpose of this test output is to enable a simple EYE test for jitter measurements with minimal equipment for embedded applications using the recovered clock from the CDR circuits in the receiver. This output is not intended to be used for compliance purposes. Such testing is specified in the PHY CTS.

  This test output should support a minimum of 10pF of parasitic capacitance including the capacitance of the test probe. The test output should add no more than the following peak-to-peak jitter, accumulated for a period of 250UI to facilitate 3% measurement accuracy (±1.5%):

  - **HBR3** – 4ps
  - **HBR2** – 6ps
  - **HBR** – 11ps
  - **RBR** – 18ps

  For example, if a single-ended output pad is desired, the test pad would need a minimum slew rate of 1.82V/ns into the maximum expected capacitive load, and can have no more than 20mVp-p of total power supply noise. If the same pad can support 3.64V/ns, then 40mVp-p power supply noise can be tolerated.

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- **Link Symbol Error Rate Measurement** – Count of the number of unscrambled data symbols that are not 00h when the upstream DP device writes 010b to each enabled lane's LINK_QUAL_LANE*x*_SET register, and stores that count in the SYMBOL_ERROR_COUNT_LANE*x* registers (DPCD Addresses 00210h through 00217h; each register is comprised of two bytes, within which the error count is stored in the 15 least significant bits). Link quality can be estimated using the procedure listed in Section 2.9.4.5.
- When the downstream device is receiving the PRBS7 pattern or CP2520 PHY Layer Compliance EYE pattern, it must count the number of bits (PRBS7) or symbols (CP2520 PHY Layer Compliance EYE pattern) that do not match the appropriate pattern. This count is also stored in the SYMBOL_ERROR_COUNT_LANE*x* registers.

  Any time the link is trained and the downstream device is not receiving the Symbol Error Rate Measurement Pattern, the PRBS7 pattern, or the CP2520 PHY Layer Compliance EYE pattern, the downstream device must increment the counter(s) in the SYMBOL_ERROR_COUNT_LANE*x* registers whenever an invalid ANSI 8b/10b symbol is received. The SYMBOL_ERROR_COUNT_SEL field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 7:6) determines which errors to include:

  - 00 = Count Disparity and Illegal Symbol errors
  - 01 = Count Disparity errors only
  - 10 = Count Illegal Symbol errors only
  - 11 = RESERVED

3.5.1.5 RS (254, 250) FEC

New to *DP v1.4*, the Reed-Solomon code Forward Error Correction (FEC) function RS (254, 250), with a symbol size of 10 bits capable of correcting up to two RS symbol errors per FEC block of 254 RS symbols, is an optional feature that can be added to the Main-Link PHY Layer Logical Sub-block.

FEC is required for transporting DSC bitstreams. Because FEC is a Main-Link PHY Layer Logical Sub-block function, it is agnostic to the contents of Link Symbols. Therefore, it is applicable to:

- SST format
- MST formats
- Uncompressed video stream transport
- DSC bitstream transport

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3.5.1.5.1 FEC Encoding in DPTX

New to *DP v1.4*.

FEC encoding in a DPTX is a DP Main Link PHY Logical Sub-block function that occurs after 8b/10b encoding, as illustrated in Figure 3-23. When FEC encoding is enabled, the Link Layer block of a DPTX generates Link Layer Symbols (LL Link Symbols; either Stream Valid/Stuffing Data Link Symbols or Stream Framing Control Link Symbols), FEC_PARITY_MARKER Link Symbols, and FEC_PARITY_PH (FEC Parity Place Holder) Link Symbols. Neither an HDCP encryption cipher nor scrambler LFSR (including the DP MST Control Symbol Index scrambler) advances in Link Symbol Clock Cycles carrying FEC_PARTIY_PH Link Symbols that are replaced with 8b/10b-encoded FEC parity symbols in the FEC encoder within the Main Link PHY Layer Logical Sub-block, as illustrated in Figure 3-23.

Figure 3-23: FEC Encoding in DPTX

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3.5.1.5.2 FEC Decoding in DPRX

New to *DP v1.4*.

FEC decoding in a DPRX is a DP Main Link PHY Logical Sub-block function that occurs before 8b/10b decoding, as illustrated in Figure 3-24. When FEC decoding is enabled, the Main Link PHY Layer Logical Sub-block of a DPRX replaces the 8b/10b-decoded RS Parity Symbols with FEC_PARITY_PH Link Symbols. Neither an HDCP encryption cipher nor scrambler LFSR (including the DP MST Control Symbol Index scrambler) advances in Link Symbol Clock Cycles carrying FEC_PARTIY_PH Link Symbols that are discarded by the Link Layer block, as illustrated in Figure 3-24.

Figure 3-24: FEC Decoding in DPRX

3.5.1.5.3 RS(254, 250) FEC Polynomial and Test Vectors

New to *DP v1.4*.

The following equation represents the polynomial of *DP v1.4* RS(254, 250) FEC:

$$G(x) = (x - 1)\,(x - \alpha)\,(x - \alpha^2)\,(x - \alpha^3) = x^4 + g_3 * x^3 + g_2 * x^2 + g_1 * x + g_0$$

where:

- $G(x) = x^{10} + x^3 + 1$ is a primitive polynomial over $GF(2^{10})$
- α is a root of the primitive polynomial

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- $g_3 = 15$, $g_2 = 54$, $g_1 = 120$, and $g_0 = 64$ (all in decimal)

Figure 3-25 illustrates the schematic RS encoder representation. Before starting the calculation, DPTX shall initialize all registers to 0s and shall transmit the register contents when the data ends.

Figure 3-25: Schematic RS Encoder Representation (INFORMATIVE)

In Figure 3-25, Data0 is the first 10 bits and Data249 is the last 10 bits. P3 is the most significant parity symbol and P0 the least significant parity symbol.

The following four test vectors are provided for informative purposes.

- Test Vector 1:
  - FEC_ENC_D = [0,0,…,0,1]
  - FEC_ENC_Par3 = 15
  - FEC_ENC_Par2 = 54
  - FEC_ENC_Par1 = 120
  - FEC_ENC_Par0 = 64
- Test Vector 2:
  - FEC_ENC_D = [1,0,…,0]
  - FEC_ENC_Par3 = 40
  - FEC_ENC_Par2 = 447
  - FEC_ENC_Par1 = 252
  - FEC_ENC_Par0 = 362
- Test Vector 3:
  - FEC_ENC_D = [1,2,3,4,…,249,250]
  - FEC_ENC_Par3 = 77
  - FEC_ENC_Par2 = 905
  - FEC_ENC_Par1 = 863
  - FEC_ENC_Par0 = 96

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- Test Vector 4:
  - FEC_ENC_1ST_D = [251,252,253,254…,499,500]
  - FEC_ENC_Par3 = 311
  - FEC_ENC_Par2 = 356
  - FEC_ENC_Par1 = 836
  - FEC_ENC_Par0 = 536

3.5.1.5.4 Two-way Interleaving

New to *DP v1.4*.

To improve immunity against transport bit errors that can become bursty errors due to the DPRX's Decision Feedback Equalizer (DFE), DisplayPort shall use two-way interleaving for RS (254, 250) FEC.

For 1-lane configuration, a DPTX shall combine two FEC blocks of 254 RS symbols each to formulate an interleaved FEC block consisting of 512 8b/10b codes, as listed in Table 3-9.

For 2- and 4-lane configurations, a DPTX shall generate the interleaved FEC block consists of 256 8b/10b codes. A DPTX shall insert an FEC parity marker (FEC_PM, K28.1) every 128th interleaved FEC block for 1-lane configuration, and every 256th interleaved FEC block for 2- and 4-lane configurations.

The resulting total FEC overhead is 2.3% (that is, an FEC-enabled DP link has 2.3% less link bandwidth available for transport of stream(s)).

Table 3-9: Interleaved FEC Block for 1-, 2-, and 4-lane Configurations

Configuration	Interleaved FEC Block Generated	Interleaved FEC Block Transported	FEC_PM Insertion
1-lane	2 × 250 RS data symbols + 2 × 4 RS parity symbols	2 × 250 LL codes [a] + 12 FEC parity codes + CD_ADJ code	Every 128th interleaved FEC block transported (= every 65537th 8b/10b code[b])
2- and 4-lane	250 RS data symbols + 4 RS parity symbols	250 LL codes[a] + 5 FEC parity codes + CD_ADJ code	Every 256th interleaved FEC block transported (= every 65537th 8b/10b code[b])

a. 8b/10b-encoded LL link symbols.
b. Every 81us at 8.1Gbps/lane and every 121us at 5.4Gbps/lane.

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Figure 3-26 illustrates the interleaved FEC block transport for 1-lane configuration.
Figure 3-27 illustrates the interleaved FEC block transport for 2- and 4-lane configurations.

Figure 3-26: Interleaved FEC Block Transport for 1-lane Configuration

Figure 3-27: Interleaved FEC Block Transport for 2- and 4-lane Configurations

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Figure 3-28 and Figure 3-29 illustrate two-way interleaving in a DPTX and DPRX, respectively, for a 1-lane configuration. Figure 3-30 and Figure 3-31 illustrate two-way interleaving in a DPTX and DPRX, respectively, for 2- and 4-lane configurations. For 4-lane configuration, the diagram shown in those figures is duplicated.

Figure 3-28: Two-way FEC Interleaving for 1-lane Configuration in DPTX

Figure 3-29: Two-way FEC Interleaving for 1-lane Configuration in DPRX

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Figure 3-30: Two-way FEC Interleaving for 2- and 4-lane Configurations in DPTX

Figure 3-31: Two-way FEC Interleaving for 2- and 4-lane Configurations in DPRX

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As illustrated in Figure 3-28 through Figure 3-31, a DPTX shall interleave LL codes to be transported for FEC encoding. As for FEC parity symbols:

- **1-lane configuration** – A DPTX shall interleave the four FEC parity symbols from two FEC encoders, split them into 11 parity bytes and four extra parity bits as listed in Table 3-10, and 8b/10b-encode for transport.
- **2- and 4-lane configurations** – A DTPX shall interleave the four FEC parity symbols from two FEC Encoders, split each to five parity bytes four extra parity bits as listed in Table 3-11, and 8b/10b-encode for transport.

The 8b/10b data code, *DX.Y*, before 8b/10b encoding is 5-bit *X* (*EDCBA*) concatenated with 3-bit *Y* (*HGF*). For example, D5.1 is 00101 001 before encoding. When a single FEC parity byte has parity symbol bits from multiple parity symbols, the bits from one parity symbol are mapped to *EDCBA* bits and the bits from the remaining parity symbols are mapped to *HGF* bits.

DPTX shall determine the first Parity code immediately following the last LL code based on the currently running disparity at the end of the last LL code.

Table 3-10: Parity Symbols Interleaving and Splitting in 1-lane Configuration

Parity Bytes and Extra Bits	Parity Symbols Bits Contained	Parity Codes
PB0	PE0[9:2]	PC0
PB1	PO0[9:5] | PE0[1:0] | 0	PC1
PB2	PO0[4:0] | 000	PC2
PB3	PE1[9:2]	PC3
PB4	PO1[9:5] | PE1[1:0] | 0	PC4
PB5	PO1[4:0] | 000	PC5
PB6	PE2[9:2]	PC6
PB7	0 | PO2[9:3]	PC7
PB8	PE3[9:5] | PO2[2:0]	PC8
PB9	PE3[4:0] | 000	PC9
PB10	PO3[7:0]	PC10
Extra four bits	PO3[9:8] | PE2[1:0]	Part of CD_ADJ

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Table 3-11: Parity Symbols Interleaving and Splitting in 2- and 4-lane Configurations

Parity Bytes and Extra Bits	Parity Symbols Bits Contained	Parity Codes
Lane 0 (or Lane 2)		
PB00	PE0[9:2]	PC00
PB01	0 | PO1[9:3]	PC01
PB02	PE2[9:5] | PO1[2:0]	PC02
PB03	PE2[4:0] | 000	PC03
PB04	PO3[7:0]	PC04
Extra four bits	PO3[9:8] | PE0[1:0]	Part of CD_ADJ0
Lane 1 (or Lane 3)		
PB10	PO0[9:2]	PC10
PB11	0 | PE1[9:3]	PC11
PB12	PO2[9:5] | PE1[2:0]	PC12
PB13	PO2[4:0] | 000	PC13
PB14	PE3[7:0]	PC14
Extra four bits	PE3[9:8] | PO0[1:0]	Part of CD_ADJ1

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As for CD_ADJ code determination, a DPTX shall incorporate the four extra parity bits into CD_ADJ, as listed in Table 3-12. The case number is defined by both the currently running disparity (i.e., the number of accumulated 1s relative to the number of accumulated 0s, the disparity is either two extra 1s or equal as per the 8b/10b coding rule) at the end of LL codes and that at the end of Parity Codes.

Table 3-12: CD_ADJ Code Selection

Extra Four Bits (PXx[9:8]|PYy[1:0])[a]		Case Number[b]			
		1	2	3	4
00	00	D3.1	D3.0-	D3.1	D3.0+
00	01	D5.1	D5.0-	D5.1	D5.0+
00	10	D10.1	D10.0-	D10.1	D10.0+
00	11	D12.1	D12.0-	D12.1	D12.0+
01	00	D3.2	D2.3-	D3.2	D2.3+
01	01	D5.2	D4.3-	D5.2	D4.3+
01	10	D10.2	D8.3-	D10.2	D8.3+
01	11	D12.2	D15.3-	D12.2	D15.3+
10	00	D3.5	D3.4-	D3.5	D3.4+
10	01	D5.5	D5.4-	D5.5	D5.4+
10	10	D10.5	D10.4-	D10.5	D10.4+
10	11	D12.5	D12.4-	D12.5	D12.4-
11	00	D3.6	D3.7-	D3.6	D3.7+
11	01	D5.6	D5.7-	D5.6	D5.7+
11	10	D10.6	D10.7-	D10.6	D10.7+
11	11	D12.6	D12.7-	D12.6	D12.7+

a. See Table 3-10 and Table 3-11 for parity symbol bit mapping.
b. See Table 3-13 for the case number definitions.

Table 3-13: CD_ADJ Selection Case Definition

Case #	Case Number			
	1	2	3	4
Current Running Disparity after the last LL Code	Two extra 1s	Equal	Equal	Two Extra 1s
Current Running Disparity after the last Parity Code	Two extra 1s	Two Extra 1s	Equal	Equal

The extra two bits, PXx[9:8], shall be mapped to HG bits of CD_ADJ. The other extra two bits, PYy[1:0], shall be mapped to DC bits of CD_ADJ.

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With the FEC parity codes interleaving and splitting method described above, only one FEC parity symbol per FEC block becomes corrupted when two consecutive FEC parity codes are corrupted over the DP link. Furthermore, a single bit error, either in the FEC parity code or CD_ADJ code, corrupts only one FEC parity symbol. This is because of the way parity symbol bits from two parity symbols are mapped to parity bytes and the CD_ADJ byte.

To account for the overhead of FEC parity codes and CD_ADJ code per interleaved FEC block, a DPTX shall insert FEC parity place holder (FEC_PARITY_PH) link symbols in the Link Layer block, as follows:

- **1-lane configuration** – After every 500 Link Layer link symbols
- **2 and 4-lane configurations** – After every 250 Link Layer link symbols

Additionally, a DPTX shall insert an FEC_PM link symbol in the Link Layer block, as follows:

- **1-lane configuration** – Once every 128th interleaved FEC block
- **2 and 4-lane configurations** – Once every 256th interleaved FEC block

A DPTX shall ***not*** advance either HDCP cipher or scrambler LFSR (both Data Link Symbol scrambler and MST Control Symbol Index scrambler) in those link symbol clock cycles for FEC_PARITY_PH link symbols. Furthermore, a DPTX shall remove the FEC_PARITY_PH link symbols before the main 8b/10b encoding to generate a gap in which to insert FEC parity codes and the CD_ADJ code.

A DPRX shall interleave the received LL codes and FEC parity codes for FEC decoding. It shall then 8b/10b decode the five FEC parity codes per FEC decoder to five FEC parity bytes and four FEC parity symbols for FEC decoding.

A DPRX shall remove FEC parity codes and the CD_ADJ code and insert FEC_PARITY_PH link symbols in their place. A DPRX shall ***not*** advance either scrambler LFSR (both Data Link Symbol scrambler and MST Control Symbol Index scrambler) or HDCP cipher into those link symbol clock cycles for FEC_PARITY_PH link symbols.

A DPRX Link Layer block shall discard both FEC_PARITY_PH link symbols and the FEC_PM link symbol.

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3.5.1.5.5 Enabling/Disabling FEC Encoding/Decoding

New to *DP v1.4*.

An FEC-capable DPTX discovers whether a plugged DPRX is FEC-capable by reading the FEC_CAPABLE bit in the FEC_CAPABILITY register (DPCD Address 00090h, bit 0).

A DPTX that is plugged to an FEC-capable DPRX and anticipates enabling FEC encoding shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training.

After the FEC_READY bit is set, a DPRX shall delay LL code forwarding to the Main 8b/10b decoder and descrambler block by the same amount of time required for FEC decoding, even when it is not performing FEC decoding (that is, a DPRX shall ensure that enabling and disabling of FEC decoding is transparent to its HDCP decryption block and Link Layer block).

To prompt a DPRX to enable FEC decoding, a DPTX shall transmit the FEC_DECODE_EN sequence listed in Table 3-14. Figure 3-32 illustrates the FEC_DECODE_EN sequence for 2- and 4-lane configurations.

To prompt a DPRX to disable FEC decoding, a DPTX shall transmit the FEC_DECODE_DIS sequence listed in Table 3-14. Figure 3-33 illustrates the FEC_DECODE_DIS sequence for 2- and 4-lane configurations.

For all lane counts and for both enabling and disabling of FEC encoding/decoding, a DPTX shall place the last K28.1 of the sequence to coincide with FEC_PM.

Neither the FEC_DECODE_EN nor FEC_DECODE_DIS symbol sequence shall be interrupted by the insertion of LL Link Symbols. Both a DPTX and DPRX shall advance HDCP cipher and scrambler LFSR in those Link Symbol Clock Cycles carrying those FEC_DECODE_EN/ FEC_DECODE_DIS symbol sequence time slots.

Table 3-14: FEC_DECODE_EN/FEC_DECODE_DIS Sequences

Configuration	FEC_DECODE_EN Sequence	FEC_DECODE_DIS Sequence
1-lane	K28.1 – K30.7 – K30.7 – K28.1 – K23.7 – K23.7 – K28.1 – K30.7 – K30.7 – K28.1 – K23.7 – K23.7 – K28.1	K28.1 – K23.7 – K23.7 – K28.1 – K30.7 – K30.7– K28.1 – K23.7 – K23.7 – K28.1 – K30.7 – K30.7 – K28.1
2- and 4-lane Configurations	K28.1 – K30.7 – K30.7 – K28.1 – K23.7 – K23.7 – K28.1	K28.1 – K23.7 – K23.7 – K28.1 – K30.7 – K30.7 – K28.1

Figure 3-32: FEC_DECODE_EN Sequence Transmission (2- and 4-lane Configuration Example)

Figure 3-33: FEC_DECODE_DIS Sequence Transmission (2- and 4-lane Configuration Example)

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3.5.1.5.6 DPCD Registers Used for FEC

The following DPCD registers are used for FEC support:

- FEC_CAPABILITY register (DPCD Address 00090h)
- FEC_CONFIGURATION register (DPCD Address 00120h)
- FEC_STATUS register (DPCD Address 00280h)
- FEC_ERROR_COUNT0 register (DPCD Address 00281h)
- FEC_ERROR_COUNT1 register (DPCD Address 00282h)

FEC-related policy requirements are discussed in the following sections:

- Accounting for FEC overhead in SST mode – Section 2.2
- Accounting for FEC overhead in MST mode – Section 2.6
- Accounting for FEC overhead in DSC bitstream transport, both in SST and MST modes – Section 2.6.1.1
- FEC support requirement – Section 5
  - Devices supporting DSC (compression and/or decompression) – Required
  - MST Branch device – Recommended
  - PHY Repeater – Not required

3.5.1.5.7 DPCD Registers Used for FEC for LT-tunable Bit-level PHY Repeater

Support of FEC decoding and re-encoding by LT-tunable bit-level PHY repeater is optional.
The following DPCD registers are used for FEC support for LT-tunable Bit-level PHY Repeaters:

- LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV register (DPCD Address F0000h)
- MAX_LINK_RATE_PHY_REPEATER register (DPCD Address F0004h)
- FEC_STATUS_PHY_REPEATER1 register (DPCD Address F0290h)
- FEC_ERROR_COUNT_PHY_REPEATER1 register (DPCD Addresses F0291h and F0292h)
- FEC_PHY_REPEATER2 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F0298h through F029Fh)
- FEC_PHY_REPEATER3 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F02A0h through F02A7h)
- FEC_PHY_REPEATER4 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F02A8h through F02AFh)
- FEC_PHY_REPEATER5 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F02B0h through F02B7h)
- FEC_PHY_REPEATER6 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F02B8h through F02BFh)
- FEC_PHY_REPEATER7 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F02C0h through F02C7h)
- FEC_PHY_REPEATER8 CONFIGURATION AND STATUS FIELD register (DPCD Addresses F02C8h through F02CFh)

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3.5.2 Main-Link Electrical Sub-block

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DPTX drives doubly terminated, AC-coupled differential pairs, as shown in Figure 3-34 in a manner compliant with the Main-Link Transmitter electrical specification.

Note: *The 50Ω termination resistors may be integrated on the chip. The DPRX receives incoming differential signals and extracts data with its link clock and data recovery (CDR) circuits.*

Figure 3-34: Main-Link Differential Pair

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Table 3-15, Table 3-16, and Table 3-17 define the Main-Link transmitter electrical parameters. Table 3-18 and Table 3-19 define the Main-Link receiver electrical parameters.

Table 3-15: DisplayPort Main-Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
System Parameters						
f_{HBR3}	Frequency for high bit rate 3	8.05707	8.1	8.10243	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR2}	Frequency for high bit rate 2	5.37138	5.4	5.40162	Gbps	
f_{HBR}	Frequency for high bit rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for reduced bit rate	1.611414	1.62	1.620486	Gbps	
UI_HBR3	Unit Interval for high bit rate 3 (8.1Gbps/lane)		123		ps	Informative (approximate values)
UI_HBR2	Unit Interval for high bit rate 2 (5.4Gbps/lane)		185		ps	
UI_HBR	Unit Interval for high bit rate (2.7Gbps/lane)		370		ps	
UI_RBR	Unit Interval for reduced bit rate (1.62Gbps/lane)		617		ps	
Down_Spread _Amplitude	Link clock down-spreading	0		0.5	%	Range: 0 to 0.5% when down-spread enabled
Down_Spread _Frequency	Link clock down-spreading frequency	30		33	kHz	Range: 30 to 33kHz when down-spread enabled
C_{TX}	AC-coupling Capacitor	75		265	nF	All DP Main-Link lanes as well as AUX CH must be AC-coupled. AC-coupling capacitors must be placed on the transmitter side. Placement of AC-coupling capacitors on the receiver side is optional.

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Table 3-16: DisplayPort Main-Link Transmitter TP2 Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
TP2 (TX External Connector – Normative)						
$V_{TX\text{-}OUTPUT\text{-}RATIO_RBR_HBR}$[a]	Ratio of Output Voltage Level 1/Level 0	0.8		6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting. Support for Voltage Level 3 is optional.
	Ratio of Output Voltage Level 2/Level 1	0.1		5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8		6.0	dB	
$V_{TX\text{-}PREEMP\text{-}OFF}$	Maximum Pre-emphasis when disabled			0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX\text{-}PREEMP\text{-}DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2			dB	Applies to all valid voltage settings. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6			dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6			dB	
$V_{TX\text{-}DIFF_REDUCTION}$	Non-transition reduction Output Voltage Level 2			3	dB	V_{TX_DIFF} at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than V_{TX_DIFF} at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1			3	dB	
	Non-transition reduction Output Voltage Level 0			1.4	dB	
$V_{TX\text{-}DIFFp\text{-}p\text{-}MAX}$	Maximum Output Voltage Level			1.38	V	For all Output Level and Pre-emphasis combinations.
$t_{TX\text{-}SKEW\text{-}INTER_PAIR}$	Lane-to-Lane Output Skew			1250	ps	Applies to transmitters capable of 2- and 4-lane operation. Applies to all pairwise combinations of supported lanes for all data rates.
$t_{TX\text{-}SKEW\text{-}INTRA_PAIR}$	Lane Intra-pair Output Skew			30	ps	Applies to all supported lanes.

a. *Earlier versions of this Standard had the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the required range of output voltage levels. For HBR2 and higher, the output ratio need not be explicitly specified or tested because the compliance test point is moved to TP3_EQ. That is why the ratio of output voltage levels is removed from the above table for HBR2 and above.*

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Table 3-17: DisplayPort Main-Link Transmitter TP3_EQ Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
TX TP3_EQ (Compliance Cable Model with HBR2 Reference Receiver Equalization – Normative)						
$t_{TX\text{-}TJ_TPS4_HBR3}$	Maximum TX Total Jitter			0.65	UI	For HBR3. Measured at $1E^{-9}$ BER.
$t_{TX\text{-}NonISI_TPS4_HBR3}$	Maximum TX Non-ISI Jitter			0.56	UI	
$t_{TX\text{-}TJ_CP2520_HBR2}$	Maximum TX Total Jitter			0.62	UI	For HBR2. Measured at $1E^{-9}$ BER using the CP2520 PHY Layer Compliance EYE pattern.
$t_{TX\text{-}DJ_CP2520_HBR2}$	Maximum TX Deterministic Jitter			0.49	UI	
$t_{TX\text{-}TJ_D10.2_HBR2}$	Maximum TX Total Jitter			0.40	UI	For HBR2. Measured at $1E^{-9}$ BER using the D10.2 Compliance pattern.
$t_{TX\text{-}DJ_D10.2_HBR2}$	Maximum TX Deterministic Jitter			0.27	UI	
$t_{TX\text{-}RJ_D10.2_HBR2}$	Maximum TX Random Jitter			0.13	UI	
$V_{TX\text{-}DIFFp\text{-}p_HBR3}$ [a]	TX Differential Peak-to-Peak EYE Voltage	75			mV	For HBR3. Measured at $1E^{-9}$ BER using TPS4.
$V_{TX\text{-}DIFFp\text{-}p_HBR2}$ [a]	TX Differential Peak-to-Peak EYE Voltage	90			mV	For HBR2. Measured at $1E^{-9}$ BER using the CP2520 PHY Layer Compliance EYE pattern.
$t_{TX\text{-}DIFFp\text{-}p_RANGE_HBR2_HBR3}$	TX Differential Peak-to-Peak EYE Voltage Measurement Range	0.375		0.625	UI	For HBR2 and HBR3. Uses 0.5 Cumulative Distribution Function (CDF) of the jitter distribution as the 0UI reference point. TX Differential Peak-to-Peak EYE Voltage requirement can be met anywhere within this UI range.

a. *The downstream EYE masks describe the EYE that a DPTX is to deliver to TP3_EQ under normal operating conditions. The upstream EYE mask describes the EYE that a DPRX is to receive at TP3_EQ under normal operating conditions. Consult with the VESA DisplayPort PHY Compliance Test Specification for the proper measurement technique and associated compliance EYE requirements.*

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Table 3-18: DisplayPort Main-Link Receiver System Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
System Parameters						
f_{HBR3}	Frequency for high bit rate 3	8.05707	8.1	8.10243	Gbps	Frequency high limit = +300ppm
f_{HBR2}	Frequency for high bit rate 2	5.37138	5.4	5.40162	Gbps	Frequency low limit = -5300ppm
f_{HBR}	Frequency for high bit rate	2.68569	2.7	2.70081	Gbps	DP link RX does not require local crystal for link clock generation.
f_{RBR}	Frequency for reduced bit rate	1.611414	1.62	1.620486	Gbps	
UI_HBR3	Unit Interval for high bit rate 3 (8.1Gbps/lane)		123		ps	Informative (approximate values)
UI_HBR2	Unit Interval for high bit rate 2 (5.4Gbps/lane)		185		ps	
UI_HBR	Unit Interval for high bit rate (2.7Gbps/lane)		370		ps	
UI_RBR	Unit Interval for reduced bit rate (1.62Gbps/lane)		617		ps	
Down_Spread _Amplitude	Link clock down-spreading	0		0.5	%	Up to 0.5% down-spread support is required. Modulation frequency range of 30 to 33kHz must be supported.

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Table 3-19: DisplayPort Main-Link Receiver TP3 Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
TP3 (RX External Connector – Normative)						
$t_{RX\text{-}EYE_CONN}$	Minimum Receiver EYE Width at RX-side connector pins	0.25			UI	For Reduced Bit Rate (1 - $T_{RX\text{-}EYE_CONN}$) specifies the allowable TJ.
$t_{RX\text{-}SKEW\text{-}INTRA_PAIR\ HBR3}$	Lane Intra-pair Skew Tolerance			50	ps	For HBR3. Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3_EQ.
$t_{RX\text{-}SKEW\text{-}INTRA_PAIR\ HBR2}$	Lane Intra-pair Skew Tolerance			50	ps	For HBR2. Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3_EQ.
$t_{RX\text{-}SKEW\text{-}INTRA_PAIR\ High\text{-}Bit\text{-}Rate}$	Lane Intra-pair Skew Tolerance			60	ps	Represents the skew (between D+ and D- of the same lane) contribution from the cable in addition to the stressed EYE at TP3.
$t_{RX\text{-}SKEW\text{-}INTRA_PAIR\ Reduced\text{-}Bit\text{-}Rate}$				260	ps	
$f_{RX\text{-}TRACKING\text{-}BW_HBR3}$	Jitter Closed-Loop Tracking Bandwidth	15			MHz	Minimum CDR closed-loop tracking bandwidth at the receiver when the input is an ANSI 8b/10b pattern, such as a TPS4.
$f_{RX\text{-}TRACKING\text{-}BW_HBR2}$		10			MHz	
$f_{RX\text{-}TRACKING\text{-}BW_HBR}$		10			MHz	
$f_{RX\text{-}TRACKING\text{-}BW_RBR}$		5.4			MHz	

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Table 3-20: DisplayPort Main-Link Receiver TP3_EQ Parameters

Symbol	Parameter	Min	Nom	Max	Units	Comments
RX TP3_EQ (RX External Connector after Reference Receiver Equalizer – Normative[a])						
$t_{RX\text{-}TJ_TPS4_HBR3}$	Minimum Receiver EYE Width	0.35			UI	For HBR3. Measured at $1E^{-9}$ BER using TPS4.
$V_{RX\text{-}DIFFp\text{-}p_HBR3}$	RX Differential Peak-to-Peak EYE Voltage	75			mV	
$t_{RX\text{-}NonISI_TPS4_HBR3}$	Minimum Receiver Non-ISI Jitter	0.56			UI	For HBR3. Measured at $1E^{-9}$ BER.
$t_{TX\text{-}RJ_TPS4_HBR3}$	Random Jitter Contribution from TX	0.16			UI	For HBR3 without cross talk. Measured at $1E^{-9}$ BER.
$t_{RX\text{-}TJ_CP2520_HBR2}$	Minimum Receiver EYE Width	0.38			UI	For HBR2. Measured at $1E^{-9}$ BER using the CP2520 PHY Layer Compliance EYE pattern.
$V_{RX\text{-}DIFFp\text{-}p_HBR2}$	RX Differential Peak-to-Peak EYE Voltage	70			mV	
$t_{RX\text{-}DIFFp\text{-}p_RANGE_HBR2_HBR3}$	RX Differential Peak-to-Peak EYE Voltage Measurement Range	0.375		0.625	UI	For HBR2 and HBR3. Uses 0.5 CDF of the jitter distribution as the 0UI reference point. RX Differential Peak-to-Peak EYE Voltage requirement can be met anywhere within this UI range.

a. *In this Standard, a test mode option is added to enable the continuous transmission of an 80-bit pattern by the AUX CH block of a DPRX as controlled by the TEST_80BIT_CUSTOM_PATTERN register (DPCD Addresses 00250h through 0025Bh. The purpose of this test mode is to enable further impairment of the incoming stressed EYE with the continuous presence of a near end crosstalk (NEXT) aggressor. The AUX CH signal differential voltage swing is a downstream device implementation-specific choice. The lower the voltage swing set by the downstream device, the lower the effect of NEXT aggression to the incoming Main-Link signal. The only requirement is that the AUX CH differential voltage swing at the transmitting-end connector pins (which are UFP connector pins) must be greater than or equal to 290mV_diff_pp.*

3.5.2.1 AC-coupling

Each lane of a DP link must be AC-coupled. The minimum and maximum values for the capacitance are specified in Table 3-15. The requirement for the inclusion of AC-coupling capacitors is specified at the DPTX.

3.5.2.2 Termination

Care should be taken to minimize emissions and crosstalk from unused lanes. It is recommended that unused lanes be parked at an implementation-dependent fixed voltage and any active termination be enabled.

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3.5.2.3 DC Common Mode Voltage

For the DP Main-Link, transmitter DC common mode voltage must be held at the same value during transmission. A downstream device must keep the common mode voltage at the UFP connector pins within the range of 0 to 2.0V while the DPRX is in the ACTIVE or STANDBY power state. (See Section 5.2.5 for downstream device power states.) If the downstream device has AC-coupling capacitors on the Main-Link lanes as shown in Main-Link Topology B of Figure 3-34, the downstream device must pull the Main-Link's UFP connector pins to ground (using 100kΩ to 1MΩ pull-down resistors) to prevent those pins from floating.

The DPTX must pre-charge the bus to a common mode voltage for 10us or longer before starting the Link Training sequence.

3.5.2.4 Short Circuit Requirements

The driver and receiver circuits of the Main-Link block must survive the worst-case short-circuit current of 50mA (2.0V over 40Ω).

3.5.2.5 Bandwidth of Transmitter/Receiver PLLs

No reference clock is required to be forwarded over the DP link. An accurate local time reference (e.g., a local crystal) is optional for a downstream (receiving) device. The Training Sequence must be used to establish the proper clock recovery by the DPRX.

This Standard requires that the downstream device clock-recovery PLL have a closed-loop bandwidth of no less than 15MHz for HBR3, 10MHz for HBR2/HBR, and 5.4MHz for RBR, all with respect to the PRBS7 pattern.

Compliance to the upstream device jitter specification described in Section 3.5.2.7 is measured at the upstream device connector pins, using a signal analyzer that has a second-order clock recovery function with a closed-loop tracking bandwidth of 15MHz with a damping factor of 1.00 for HBR3, 10MHz with a damping factor of 1.00 for HBR2, 10MHz with a damping factor of 1.51 for HBR, and 5.4MHz with a damping factor of 1.51 for RBR, all with respect to the PRBS7 pattern

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3.5.2.6 Down-spreading of Link Clock

Downstream devices must support down-spreading of the link clock. The down-spread amplitude must be either disabled (0.0%) or up to 0.5%, as written by the upstream device to the DOWNSPREAD_CTRL register (DPCD Address 00107h). The modulation frequency range must be 30 to 33kHz.

3.5.2.7 DisplayPort Jitter Specifications

This section describes the jitter budget for upstream and downstream devices. For HBR and RBR, jitter specification compliance is measured at the upstream device connector pins (TP2) and downstream device connector pins (TP3). For HBR3 and HBR2, jitter specification compliance is measured at the downstream device connector pins after the Reference Receiver Equalizer (TP3_EQ), as shown in Section 3.5.2.9.

The jitter specifications at the transmitter and receiver integrated circuit package pins are informative.

3.5.2.7.1 Receiver Jitter Tolerance

The DP spectral jitter used for receiver compliance testing must comply with the requirements described in this section.

3.5.2.7.1.1 HBR3 Receiver Jitter Tolerance

The HBR3 jitter tolerance equations apply after the application of the HBR2 reference equalizer described in Section 3.5.2.9 and with a response not exceeding the response curve shown in Figure 3-35.

The HBR3 jitter tolerance is calculated using the following equations:

$$s(f) = 2\cdot\pi\cdot f\cdot j \qquad \zeta = 1 \qquad BW = 2\cdot\pi\cdot 1.5\cdot 10^7$$

$$\omega_n = \frac{BW}{\sqrt{1+2\zeta^2+\sqrt{\left(1+2\zeta^2\right)^2+1}}}$$

$$JTF(f) = \frac{s(f)^2}{s(f)^2+2\cdot s(f)\cdot\zeta\cdot\omega_n+\omega_n^2}$$

$$JTHBR2(f) = \frac{SJ_{SWEEP}}{|JTF(f)|} + SJ_{FIXED} + ISI + RJ$$

$$SJ_{SWEEP}(f) = \frac{SJ_{SWEEP}}{|JTF(f)|}$$

where (recommended): SJ_{SWEEP} = 0.1UI, SJ_{FIXED} = 0.3UI, ISI = 0.09UI, RJ = 0.16UI

The HBR3 TJ is divided into SJ, ISI, and RJ terms. SJ is comprised of a fixed tone SJFIXED placed above 100MHz and a swept tone SJSWEEP placed between 0.1 to 100MHz. The relative trade-off between SJSWEEP, SJFIXED, ISI, and RJ is not required by this Standard, but is determined by the corresponding test within the DP PHY CTS Specification.

Note: *The budgeting of the SJ/ISI/RJ terms was determined empirically and is not the result of a rigorous analysis or derivation.*

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Figure 3-35 provides an example of the JTHBR3 curve used for testing the Jitter tolerance at HBR3 of a downstream device (receiver).

Figure 3-35: HBR3 Receiver Jitter Output/Input Tolerance Mask

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3.5.2.7.1.2 HBR2 Receiver Jitter Tolerance

The HBR2 jitter tolerance equations apply after the application of the HBR2 reference equalizer described in Section 3.5.2.9 and with a response not exceeding the response curve shown in Figure 3-44.

The HBR2 jitter tolerance is calculated using the following equations:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \zeta = 1 \qquad BW = 2 \cdot \pi \cdot 10^7$$

$$\omega_n = \frac{BW}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}}$$

$$JTF(f) = \frac{s(f)^2}{s(f)^2 + 2 \cdot s(f) \cdot \zeta \cdot \omega_n + \omega_n^2}$$

$$JTHBR2(f) = \frac{SJ_{SWEEP}}{|JTF(f)|} + SJ_{FIXED} + ISI + RJ$$

$$SJ_{SWEEP}(f) = \frac{SJ_{SWEEP}}{|JTF(f)|}$$

where (Recommended): SJ_{SWEEP} = 0.1UI, SJ_{FIXED} = 0.1UI, ISI = 0.22UI, RJ = 12.3*16.3mUI.

The HBR2 TJ is divided into SJ, ISI, and RJ terms. SJ is comprised of a fixed tone SJ_{FIXED} placed above 100MHz and a swept tone SJ_{SWEEP} placed between 0.1 to 100MHz. The relative trade-off between SJSWEEP, SJFIXED, ISI, and RJ is not required by this Standard, but is determined by the corresponding test in the DP PHY CTS Specification.

Note: *The budgeting of the SJ/ISI/RJ terms was determined empirically and is not the result of a rigorous analysis or derivation.*

Figure 3-36 gives an example of the JTHBR2 curve used for testing the Jitter tolerance at HBR2 of a downstream device (receiver).

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Figure 3-36: HBR2 Receiver Jitter Output/Input Tolerance Mask

3.5.2.7.1.3 HBR Receiver Jitter Tolerance

The HBR mask applies after the application of the HBR reference equalizer described in Section 3.5.2.9, and with a response not exceeding the response curve shown in Figure 3-45. The HBR jitter tolerance mask is calculated as follows:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \tau_z = 1.656 \cdot 10^{-7} \qquad \tau_{p2} = 6.596 \cdot 10^{-10} \qquad G = 3.421 \cdot 10^{14}$$

$$G_o(f) = \frac{G}{s(f)^2} \cdot \frac{(s(f) \cdot \tau_z + 1)}{(s(f) \cdot \tau_{p2} + 1)} \qquad Hs(f) = \frac{G_o(f)}{1 + G_0(f)}$$

$$JTHBR(f) = \left(\left| \frac{0.2}{1 - Hs(f)} \right| - 0.2 \right) + ISI_HBR + non_ISI_HBR$$

where: $ISI_HBR = 0.161$, $non_ISI_HBR = 0.330$

The ISI_HBR is equal to (TJ - non-ISI) as specified in Table 3-21. The non-ISI is divided into a frequency-independent term represented by non_ISI_HBR and a frequency-dependent term that reaches an invariant value of zero at frequencies much greater than the closed-loop bandwidth of the CDR (i.e., frequencies approximately 1.35GHz and greater for HBR).

Note: *Budgeting of the non-ISI was determined empirically and is not the result of a rigorous analysis or derivation.*

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At HBR, a compliant downstream device (receiver) jitter tolerance must be at or above the JTHBR curve shown in Figure 3-37.

Figure 3-37: HBR Jitter Output/Input Tolerance Mask

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3.5.2.7.1.4 RBR Receiver Jitter Tolerance

The Reduced Bit Rate (RBR) jitter tolerance mask is calculated as follows:

$$s(f) = 2 \cdot \pi \cdot f \cdot j \qquad \tau_z = 1.656 \cdot 10^{-7} \qquad \tau_{p2} = 6.596 \cdot 10^{-10} \qquad G = 1.673 \cdot 10^{14}$$

$$G_o(f) = \frac{G}{s(f)^2} \cdot \frac{(s(f) \cdot \tau_z + 1)}{(s(f) \cdot \tau_{p2} + 1)} \qquad Hs(f) = \frac{G_o(f)}{1 + G_0(f)}$$

$$JTRBR(f) = \left| \frac{ISI_RBR + non_ISI_RBR}{1 - Hs(f)} \right|$$

where: *ISI_RBR* = 0.570, *non_ISI_RBR* = 0.180

The ISI_RBR is equal to (TJ - non-ISI) as specified in Table 3-21. The non-ISI is divided into a frequency-independent term represented by non_ISI_RBR and a frequency-dependent term that reaches an invariant value of zero at frequencies much greater than the closed-loop bandwidth of the CDR (i.e. frequencies approximately 810MHz and greater for RBR).

Note: *Budgeting of the non-ISI was determined empirically and is not the result of a rigorous analysis or derivation.*

At RBR, a compliant downstream device (receiver) jitter tolerance must be at or above the JTRBR curve shown in Figure 3-38.

Figure 3-38: RBR Jitter Output/Input Tolerance Mask

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3.5.2.7.2 Differential Noise Budget

Jitter specifications relate to the phase relationship between an idealized reference clock and the data. Any phase error that results in the sample being improperly read (i.e., prior bit or following bit sampled) will result in a bit error.

These error components have been broken up into ISI and non-ISI jitter for HBR/RBR and broken into DJ and TJ for HBR2. The TJ (total jitter) is the total peak-to-peak phase variation in the 0V differential crossing point of the data stream for a given BER, and is defined as:

*DJ + (RJ * scale factor)*

where the scale factor is determined by the BER and data transition edge density.

The DP interface jitter characteristics must comply with the jitter budget allocations in Table 3-21.

Table 3-21: Differential Noise Budget

	Transmitter Pads (Informative)		Transmitter Connector (TP2) (N/A)		Receiver Connector (TP3_EQ) [Normative]		Receiver Silicon Pads (RX_EQ) (Informative)		Notes
	Non-ISI	TJ	Non-ISI	TJ	Non-ISI	TJ	Non-ISI	TJ	
HBR3 (8.1Gbps/lane)									
$A_{,p-p}$	0.17	0.27	N/A	N/A	0.56	0.65	0.56	0.66	2, 3
	Transmitter Package Pins (Informative)		**Transmitter Connector (TP2) (N/A)**		**Receiver Connector (TP3_EQ) [Normative]**		**Receiver Silicon Pads (Informative)**		**Notes**
	DJ	**TJ**	**DJ**	**TJ**	**DJ**	**TJ**	**DJ**	**TJ**	
HBR2 (5.4Gbps/lane)									
$A_{,p-p}$	0.17	0.27	N/A	N/A	0.49	0.62	0.57	0.70	3, 4
	Transmitter Package Pins (Informative)		**Transmitter Connector (TP2) [Normative]**		**Receiver Connector (TP3) [Normative]**		**Receiver Package Pins (Informative)**		**Notes**
	Non-ISI	**TJ**	**Non-ISI**	**TJ**	**Non-ISI**	**TJ**	**Non-ISI**	**TJ**	
HBR (2.7Gbps/lane)									
$A_{,p-p}$	0.260	0.294	0.276	0.420	0.330	0.491	0.339	0.530	1, 2, 3
RBR (1.62Gbps/lane)									
$A_{,p-p}$	0.160	0.180	0.170	0.27	0.180	0.750	0.186	0.780	1, 2, 3

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Table 3-21: Differential Noise Budget (Continued)

Parameters Applying to All Bit Rates			
f_{SSC} Spread-Spectrum Modulation Frequency	30 to 33kHz		
SSC_{tol} Spread-Spectrum Modulation Deviation	Minimum = -5000ppm Maximum = 0ppm		
f_{tol} TX Frequency Long-term Stability	Minimum = -5300ppm Maximum = +300ppm		

Notes:

1 *TP2 jitter budget must be met with the DPTX drive setting set to 800mV_diff_pp of voltage swing and 0dB of pre-emphasis for HBR/RBR.*

2 *TP3 jitter budget is used for conducting a DPRX jitter tolerance test. The difference in jitter budget between TP3 and TP2 must not be regarded as the budget for a DP cable connecting an upstream device connector to a downstream device connector. Cable qualification is performed in frequency domain as long as a frequency domain test is applicable. When it is not applicable (e.g., Hybrid devices using an optical cable as interconnect media), TP3 EYE mask may be referenced for the interconnect media qualification. In this case, pre-emphasis of an upstream device may be enabled if needed to meet the TP3 EYE mask specification.*

3 *The EYE diagram must be measured with a Compliance Test Load using a signal analyzer whose Link CDR emulation function matches the DPRX Jitter Output/Input Tolerance Mask specifications as shown in Figure 3-35 through Figure 3-38 for HBR3, HBR2, HBR, and RBR, respectively. The EYE diagram must be measured using the TPS4 for HBR3, CP2520 PHY Layer Compliance EYE pattern for HBR2, and PRBS7 for HBR/RBR.*

4 *The Transmitter Package Pin informative specs for HBR2 are based on a D10.2 pattern.*

3.5.2.8 Differential Voltage/Timing (EYE) Diagram

An EYE diagram is used to measure compliance of upstream devices and to calibrate the stressed signal for jitter tolerance testing of downstream devices.

3.5.2.8.1 HBR3/HBR2 EYE Diagrams

HBR3 and HBR2 EYE diagram masks are defined with a variable EYE height placement. The EYE height is measured at the optimal location within a 0.25UI window located at EYE center, 0.375 to 0.625UI. The upstream device can select any supported Voltage and Pre-Emphasis level combination to achieve an EYE that complies with the following mask limits:

1 EYE diagram width is established at any passing location along 0mV.

2 EYE diagram height (symmetric around 0mV) is established at any passing location between 0.375 to 0.625UI.

Note: *0.5 of the jitter histogram CDF is used as the 0UI reference point.*

3 Perimeter formed around EYE diagram width/height vertices established in steps 1 and 2 to check for violations.

4 Steps 1 through 4 are repeated, as necessary, until a passing configuration is found.

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Figure 3-39: HBR3/HBR2 EYE Mask at TP3_EQ

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Table 3-22: HBR3 Downstream and Upstream Device EYE Mask Vertices at TP3_EQ

Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + **0.35UI**	0.0000
2	Any Passing UI location between 0.375 and 0.625UI	0.0375
3	Point 1 + **0.35UI**	0.0000
4	Same as Point 2	-0.0375

Table 3-23: HBR2 Upstream Device EYE Mask Vertices at TP3_EQ

Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + **0.38UI**	0.000
2	Any Passing UI location between 0.375 and 0.625UI	0.045
3	Point 1 + **0.38UI**	0.000
4	Same as Point 2	-0.045

Table 3-24: HBR2 Downstream Device EYE Mask Vertices at TP3_EQ

Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + **0.38UI**	0.000
2	Any Passing UI location between 0.375 and 0.625UI	0.035
3	Point 1 + **0.38UI**	0.000
4	Same as Point 2	-0.035

The measured EYE must be equal to or larger than the appropriate EYE mask.

The EYE diagram must be measured at TP3_EQ for HBR3/HBR2 (with a Compliance Test Load), using a signal analyzer whose Link CDR emulation function meets the requirements specified in Section 3.5.2.5 and matches the DPRX Jitter Output/Input Tolerance Mask specifications in Section 3.5.2.7.1.1 (HBR3) and Section 3.5.2.7.1.2 (HBR2) within ±10% of accuracy.

All Main-Link lanes must be on and driving the TPS4 for HBR3 and CP2520 for HBR2 with a two-symbol (20UI) skew between each lane and adjacent lane(s). For HBR3 and HBR2, at least one combination of differential voltage swing and pre-emphasis must result in an EYE that meets the TP3_EQ EYE mask specification. This measurement is to be performed using HBR3 CTLE and DEF for the upstream device EYE opening test at HBR3 and HBR2 CTLE at HBR2. The same differential voltage swing and pre-emphasis must be used for all Main-Link lanes for HBR3 or HBR2, unless per-lane settings (optional) are supported.

Those upstream devices that support down-spreading of the link clock must produce a compliant EYE, both with and without down-spreading enabled.

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This EYE Mask is used for testing the jitter tolerance of downstream device. A test pattern generator, while transmitting the TPS4 for HBR3 and CP2520 for HBR2, must be adjusted to realize the minimum EYE, after traveling through the appropriate (TP1-TP3) channel and application of the appropriate reference equalizer, as defined in Section 3.5.2.9.

Once the test pattern generator (or the stressed signal generator) is adjusted, the bit stream must be sent to the downstream device connector pins (TP3) of the downstream device. With this input, the downstream device must realize a BER of $1E^{-9}$ or better.

For a downstream device with a permanently tethered cable, the test pattern generator is adjusted to provide a signal equal to the TP3_EQ EYE mask after passing through a compliance test cable model based on the electrical parameters for cable type E1. The permanently tethered HBR3/HBR2 downstream device is then tested by removing the compliance test cable model from the calibrated test setup and replacing it with the tethered downstream device.

3.5.2.8.2 HBR/RBR EYE Diagrams

HBR/RBR use pre-defined polygons for the EYE diagram. The polygon in Figure 3-40 represents the upstream device EYE mask at the upstream device connector pins (TP2) for HBR and RBR. Table 3-25 and Table 3-26 contain the values to be used for the vertices of the upstream device mask for HBR and RBR, respectively.

Figure 3-40: EYE Mask at Upstream Device Connector Pins

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Table 3-25: Upstream Device Mask Vertices for HBR

Point	Time (UI)	Voltage (V)
1	0.210	0.000
2	0.355	0.140
3	0.500	0.175
4	0.645	0.175
5	0.790	0.000
6	0.645	-0.175
7	0.500	-0.175
8	0.355	-0.140

Table 3-26: Upstream Device Mask Vertices for RBR

Point	Time (UI)	Voltage (V)
1	0.127	0.000
2	0.291	0.160
3	0.500	0.200
4	0.709	0.200
5	0.873	0.000
6	0.709	-0.200
7	0.500	-0.200
8	0.291	-0.160

The measured EYE must be equal to or larger than the appropriate EYE mask.

The EYE diagram must be measured at TP2 for HBR/RBR, using a signal analyzer whose Link CDR emulation function meets the requirements specified in Section 3.5.2.5 and matches the DPRX Jitter Output/Input Tolerance Mask specifications in Section 3.5.2.7.1.3 (HBR) and Section 3.5.2.7.1.4 (RBR) within ±10% of accuracy.

All Main-Link lanes must be on and driving the PRBS7 test pattern for HBR/RBR with a two-symbol (20UI) skew between each lane and adjacent lane(s). The differential voltage swing must be set to Level 2 Pre-emphasis level 0 to meet the TP2 EYE mask specification for HBR/RBR. This measurement is to be performed using a signal analyzer that embeds a worst-case (TP2-TP3) HBR cable model with the insertion loss profile defined in Section 4.1.5.1.1

Those upstream devices that support down-spreading of the link clock must produce a compliant EYE, both with and without down-spreading enabled.

The polygon in Figure 3-41 represents the minimum entry EYE into the downstream device at TP3_EQ for HBR and at TP3 for RBR.

Table 3-27 and Table 3-28 contain the values to be used for the vertices of the downstream device mask for high bit rate and reduced bit rate, respectively.

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This EYE Mask is used for testing the jitter tolerance of downstream device. A test pattern generator, while transmitting the PRBS7 bit stream, must be adjusted to realize the minimum EYE, after traveling through the appropriate (TP1-TP3) channel and application of the appropriate reference equalizer, as defined in Section 3.5.2.9.

Once the test pattern generator (or the stressed signal generator) is adjusted, the bit stream must be sent to the downstream device connector pins (TP3) of the downstream device. With this input, the downstream device must realize a BER of $1E^{-9}$ or better.

For a downstream device with a permanently tethered cable, the BER specification must be met with an input EYE to the plug connector that is equal to the TP2 EYE mask for RBR. For HBR, the test pattern generator is adjusted to provide a signal equal to the TP3_EQ EYE mask after passing through a compliance test cable model based on the electrical parameters for cable type E1. The permanently tethered HBR downstream device is then tested by removing the compliance test cable model from the calibrated test setup and replacing it with the tethered downstream device.

Figure 3-41: Downstream Device Mask at TP3_EQ (HBR) or TP3 (RBR)

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Table 3-27: Downstream Device EYE Vertices for TP3_EQ at HBR

Point	Time (UI)	Voltage (V)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

Table 3-28: Downstream Device EYE Vertices at TP3 for RBR

Point	Time (UI)	Voltage (V)
1	0.375	0.000
2	0.500	0.023
3	0.625	0.000
4	0.500	-0.023

3.5.2.9 Reference Equalizers

The HBR3, HBR2, and HBR EYE diagrams are defined after application of a corresponding reference equalizer with a response curve as defined below. The Reference Receiver Equalizer's primary function is to open the EYE for compliance measurements and does not define the Downstream Device Receiver Equalizer implementation. A downstream device that implements receiver equalization similar to the Reference Receiver Equalizer is not guaranteed to pass downstream device compliance tests.

Note: *The application of an equalizer with a response curve at the receiver may degrade the receive EYE in some configurations. It is recommended that an equalizer be designed to adapt to the received signal during link training with a maximum response granularity of 2dB at data rate frequencies.*

3.5.2.9.1 HBR3 Reference Equalizer

The HBR3 Reference Receiver Equalizer is modeled as a first-order CTLE cascaded with a one-tap Decision Feedback Equalizer (DFE).

The Reference Receiver Equalizer's primary function is to open the EYE for compliance measurements and does not define the Downstream Device Receiver Equalizer implementation. A downstream device that implements receiver equalization similar to the Reference Receiver Equalizer is not guaranteed to pass Downstream Device Compliance tests.

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The HBR3 CTLE Reference Equalizer transfer function is given by:

$$H(s) = \frac{\omega p1\ \omega p2}{\omega z} \cdot \frac{s + \omega z}{(s + \omega p1)(s + \omega p2)}$$

Which has magnitude given by:

$$|H(j\omega)| = \frac{\omega p1\ \omega p2}{\omega} \cdot \frac{\sqrt{\omega^2 + \omega z^2}}{\sqrt{\omega^2 + \omega p1^2} \cdot \sqrt{\omega^2 + \omega p2^2}}$$

where:

$$\omega z = 2\pi(0.505 \times 10^9)$$

$$\omega p1 = 2\pi(3.033 \times 10^9)$$

$$\omega p2 = 2\pi(6.000 \times 10^9)$$

Figure 3-42: Reference HBR3 Receiver Equalizer Transfer Function

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3.5.2.9.2 HBR3 Reference DFE

The HBR3 Reference equalizer includes a CTLE cascaded with a one-tap adaptive DFE with a feedback coefficient limited to < 50mV. The DFE behavior is described below.

$$yk = x_k - d1\, sgn(y_{k-1})$$

where:

yk is the DFE differential output voltage

y_k^* is the decision function output voltage

x_k is the differential input voltage after CTLE

$d1$ is the feedback coefficient

k is the UI sample

Figure 3-43: Reference HBR3 Receiver Equalizer DFE

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3.5.2.9.3 HBR2 Reference Equalizer

The HBR2 Reference Receiver Equalizer is modeled as a CTLE with a 0 at 640MHz and poles at 2.7GHz, 4.5GHz, and 13.5GHz, as shown in Figure 3-44.

The Reference Receiver Equalizer's primary function is to open the EYE for compliance measurements and does not define the Downstream Device Receiver Equalizer implementation. A downstream device that implements receiver equalization similar to the Reference Receiver Equalizer is not guaranteed to pass Downstream Device Compliance tests.

The HBR2 Reference Equalizer transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by:

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2} \cdot \sqrt{\omega^2+\omega_{p2}^2} \cdot \sqrt{\omega^2+\omega_{p3}^2}}$$

where:

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 3-44: Reference HBR2 Receiver Equalizer Transfer Function

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3.5.2.9.4 HBR Reference Equalizer

The HBR Reference Receiver Equalizer is modeled as a continuous time linear equalizer (CTLE) with a 0 at 725MHz and poles at 1.35GHz and 2.5GHz, as shown in Figure 3-45.

The HBR Reference Equalizer transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

which has magnitude given by:

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2} \cdot \sqrt{\omega^2+\omega_{p2}^2}}$$

where:

$$\omega_z = 2\pi(0.725\times10^9)$$
$$\omega_{p1} = 2\pi(1.35\times10^9)$$
$$\omega_{p2} = 2\pi(2.5\times10^9)$$

Figure 3-45: Reference HBR Receiver Equalizer Transfer Function

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3.5.2.9.5 Enhanced HBR Reference Equalizer

The insertion loss of the HBR cable specification at the Nyquist frequency of HBR (= 1.35GHz) is approximately 70% of that of HBR2 (= 2.7GHz). Given this, it makes a logical sense to have an HBR reference CTLE whose peak gain at 1.35GHz is 6dB, which is approximately 70% of the HBR2 CTLE peak gain at 2.7GHz, instead of 2.4dB as defined in Section 3.5.2.9.4. This section defines the Enhanced HBR Reference CTLE that is proportional to that of HBR2.

For a new DPRX design, use of the Enhanced HBR Reference CTLE is strongly recommended because it is expected that the Enhanced HBR Reference CTLE will be used in the future revision of PHY CTS.

The Enhanced HBR Reference Equalizer transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \times \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by:

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega} \times \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2}\sqrt{\omega^2 + \omega_{p2}^2}}$$

where:

- $\omega_z = 2\pi\ (0.38 \times 10^9)$
- $\omega_{p1} = 2\pi\ (1.15 \times 10^9)$
- $\omega_{p2} = 2\pi\ (2.0 \times 10^9)$

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Figure 3-46: Enhanced HBR Reference CTLE Relative to HBR and HBR2 Reference CLTE

3.5.2.10 Embedded Connection (Informative)

See eDP v1.4, Section 4, for applicable electrical specifications. While there is no required formal industry compliance test for the eDP connection compliance to the electrical performance described in eDP v1.4 helps ensure embedded Source and Sink devices will interoperate.

3.5.3 ESD and EOS Protection

All signal and power pins of associated DP components (transmitter IC, receiver IC, and associated I/O circuitry) must withstand at least JEDEC JESD22-A114-B Class 2 (2kV Human Body Model, 200V Machine Model) strikes.

DisplayPort devices implementing this specification may swing the I/O lines as high as ±0.3V single-ended with respect to the common mode bias reference level. The designer must carefully select clamping devices and clamping rail voltages, such that ESD devices will not cause clipping of normal signals.

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3.6 Link Training-tunable PHY Repeater

Support for Link Training (LT)-tunable PHY Repeaters is new to DP v1.3.

3.6.1 Introduction

A device containing only the PHY Layer of the DPRX and DPTX (i.e., DPRX_PHY and DPTX_PHY, respectively) is referred to as a "PHY Repeater." A PHY Repeater is placed between a DPTX and DPRX, both of which have PHY and Link Layer blocks with Link Policy Maker. Multiple PHY Repeaters can be placed between a DPTX and DPRX.

This section defines relevant terminologies and numbering rules and describes the means of discovery and tuning of up to eight LT-tunable PHY Repeaters between a DPTX and DPRX.

Note: *Non-LT-tunable PHY Repeaters are beyond the scope of this Standard.*

3.6.1.1 Two Data Path Types

There are two data path types:

- Redriver data path
  - Serial bitstream into the DPRX_PHY is optionally equalized and sent directly to the DPTX_PHY for retransmission with optional Voltage Swing/Pre-emphasis adjustment.
  - PHY Repeater with Redriver data path only is referred to as a "Redriver."
- Retimer data path
  - Serial bit stream into the DPRX_PHY is optionally equalized, sent to a clock and data recovery (CDR) block for retiming, and then sent to the DPTX_PHY for retransmission with optional Voltage Swing/Pre-emphasis adjustment
  - PHY Repeater with Retimer data path is referred to as a "Retimer" (RT).
  - A properly implemented Retimer is better equipped to output less jittery serial bitstream than Redriver.

3.6.1.2 Two Capability Types

Orthogonal to data path types, PHY Repeater has two capability types:

- LT-tunable
  - Provides for means for a DPTX aware of an LT-tunable PHY Repeater to tune the PHY parameters (i.e., receiver EQ and DPTX drive setting) during Link Training (LT) procedure.
- Non-LT tunable
  - Does not provide for means for a DPTX to tune the PHY parameters.

Note: *The use of Non-LT-tunable PHY Repeaters are beyond the scope of this Standard.*

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3.6.1.3 Two Operating Modes

LT-tunable PHY Repeater has two operating modes:

- Non-transparent mode
  - PHY Repeater replies to AUX request transactions from DPTX to DPCD LT-tunable PHY Repeater field while passing through other AUX request transactions.
- Transparent mode
  - When the upstream DPTX is unaware of the LT-tunable PHY Repeater, it never generates AUX request transactions to the LT-tunable PHY Repeater, resulting in the LT-tunable PHY Repeater's passing through all the AUX transactions (while snooping AUX transactions to certain Link Configuration registers). This operating condition is referred to as "Transparent mode."
  - The LT-tunable PHY Repeater transitions from Transparent mode to Non-transparent mode when the DPTX issues an AUX transaction to the PHY_REPEATER_MODE register (DPCD Address F0003h) to program the register's value to AAh.

Note: *A Non-LT tunable PHY Repeater is considered to always be operating in Transparent mode.*

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3.6.1.4 LT-tunable PHY Repeater Numbering for Multiple Repeaters between DPTX and DPRX

When multiple LT-tunable PHY Repeaters are placed between a DPTX and DPRX, the one closest to the DPRX is annotated as LT-tunable PHY Repeater1 and the next up as LT-tunable PHY Repeater2, as shown in the example topology illustrated in Figure 3-47.

Figure 3-47: DP Topology Example with LT-tunable PHY Repeaters

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3.6.2 Signal Routing Requirements

An LT-tunable PHY Repeater must have its DP Main-Link lanes, AUX CH, and HPD signal lines routed through as shown in Figure 3-48.

Figure 3-48: Signal Routing Requirements

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3.6.3 DPCD Address Mapping for LT-tunable PHY Repeater

Figure 3-49 illustrates how the DPCD LT-tunable PHY Repeater field is partitioned for multiple repeaters between a DPTX and DPRX.

Figure 3-49: Partitioning within DPCD LT-tunable PHY Repeater Field

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Upon discovering its location between the DPTX and DPRX, the PHY Repeater replies to AUX request transactions to its DPCD address range within LT-tunable PHY Repeater field. The PHY Repeater passes through all other AUX request transactions with one exception – an LT-tunable PHY Repeater must snoop AUX request transactions to those DPCD Addresses listed in Table 3-29 and take necessary actions as specified in the table. (For complete register descriptions, see Table 2-156.)

Table 3-29: DPCD Addresses Snooped by LT-tunable PHY Repeater

DPCD Address	Definition	Read/Write over AUX CH
00100h	LINK_BW_SET LT-tunable PHY Repeater both in non-transparent or transparent mode must snoop this field.	Write/Read
00101h	LANE_COUNT_SET LT-tunable PHY Repeater both in non-transparent or transparent mode must snoop this field.	Write/Read
00102h	TRAINING_PATTERN_SET All LT-tunable PHY Repeater must snoop this field (specifically the TRAINING_PATTERN_SELECT field, bits 3:0) to know when link training has ended.	Write/Read
00103h	TRAINING_LANE0_SET LT-tunable PHY Repeaters in Transparent mode must snoop this field and update output levels as specified. RT1 in Non-transparent mode must snoop this field and update output levels as specified.	Write/Read
00104h	TRAINING_LANE1_SET LT-tunable PHY Repeaters in Transparent mode must snoop this field and update output levels as specified. RT1 in Non-transparent mode must snoop this field and update output levels as specified.	Write/Read
00105h	TRAINING_LANE2_SET LT-tunable PHY Repeaters in Transparent mode must snoop this field and update output levels as specified. RT1 in Non-transparent mode must snoop this field and update output levels as specified.	Write/Read
00106h	TRAINING_LANE3_SET LT-tunable PHY Repeaters in Transparent mode must snoop this field and update output levels as specified. RT1 in Non-transparent mode must snoop this field and update output levels as specified.	Write/Read

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3.6.4 LT-tunable PHY Repeater DPCD Registers

The LT-tunable PHY Repeater transitions to Non-transparent mode only when the DPTX programs the PHY_REPEATER_MODE register (DPCD Address F0003h) value to AAh.

3.6.4.1 LT-tunable PHY Repeater DPCD Capability and ID Field

Table 3-30 lists the registers that are shared by all LT-tunable PHY Repeaters between a DPTX and DPRX. Therefore, all LT-tunable PHY Repeaters must reply to AUX read request transactions to these registers. (For complete register descriptions, see Table 2-169.)

Table 3-30: LT-tunable PHY Repeater DPCD Capability and ID Field

DPCD Address	Register
F0000h	LT_TUNABLE_PHY_REPEATER_FIELD_DATA_STRUCTURE_REV
F0001h	MAX_LINK_RATE_PHY_REPEATER
F0002h	PHY_REPEATER_CNT
F0003h	PHY_REPEATER_MODE

Per DP v1.3 requirements, the DPRX replies to the above AUX request transactions with an AUX_ACK followed by the value of 00h. The DPRX's failure to respond with 0s can result in undefined system behavior.

An LT-tunable PHY Repeater that receives a reply of all 0 data from its downstream device (i.e., the one closest to the DPRX) must replace the received data with its own data. An LT-tunable PHY Repeater that receives a reply of non-zero data must update the received data based on the required behavior for each DPCD register.

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3.6.4.2 LT-tunable PHY Repeater DPCD Link Configuration and Status Field(s)

Table 3-31 lists the DPCD LT-tunable PHY Repeater CONFIGURATION AND STATUS fields for all eight PHY Repeaters (PHY Repeater[8:1]). Only the repeater that matches the AUX request address must modify the reply from the downstream device. (For complete register descriptions, see Table 2-169.)

Table 3-31: LT-tunable PHY Repeater DPCD Link Configuration and Status Field(s)

DPCD Address	Register
F0010h through F005Fh	PHY_REPEATER1 CONFIGURATION AND STATUS FIELD
F0060h through F00AFh	PHY_REPEATER2 CONFIGURATION AND STATUS FIELD
F00B0h through F00FFh	PHY_REPEATER3 CONFIGURATION AND STATUS FIELD
F0100h through F014Fh	PHY_REPEATER4 CONFIGURATION AND STATUS FIELD
F0150h through F019Fh	PHY_REPEATER5 CONFIGURATION AND STATUS FIELD
F01A0h through F01EFh	PHY_REPEATER6 CONFIGURATION AND STATUS FIELD
F01F0h through F023Fh	PHY_REPEATER7 CONFIGURATION AND STATUS FIELD
F0240h through F028Fh	PHY_REPEATER8 CONFIGURATION AND STATUS FIELD

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3.6.5 AUX Transactions Handling Requirements

This section details the AUX transaction handling of the DPTX, DPRX, and LT-tunable PHY Repeaters. The DPTX requirements are applicable only for DPTXs that support LT-Tunable PHY Repeaters. These devices must meet the AUX transactions handling requirements defined in Section 2.8 unless stated otherwise within the following sub-sections.

3.6.5.1 DPTX

The DPTX must behave as defined in Section 2.8, with the exception that AUX Reply timeout must be 3.2ms instead of 400us after the LT-tunable PHY Repeaters are set in non-transparent mode. The timer for the Reply timeout starts ticking after the DPTX finishes sending the AUX STOP condition. If the DPTX's AUX Reply timeout expires for an AUX request targeting an LT-tunable PHY Repeater, it is recommended that the DPTX transition the repeater from Non-transparent mode to Transparent mode by writing 55h to the PHY_REPEATER_MODE register (DPCD Address F0003h).

3.6.5.2 DPRX

DPRX must behave as defined in Section 2.8. The timeout remains the same at 300us.

3.6.5.3 LT-tunable PHY Repeater

An LT-tunable PHY Repeater must pass all AUX request transactions (read or write) received on its UFP to its DFP. An LT-tunable PHY Repeater must have one of the following behaviors for the reply to the AUX request transaction.

Reply to AUX read request:

- Pass untouched if the AUX read request did not target the LT-tunable PHY Repeater.
- If AUX read request targeted LT-tunable PHY Repeater's DPCD register, the LT-tunable PHY Repeater replaces the DPRX's DPCD data with its own DPCD data.

Reply to AUX write request:

- Pass untouched if the AUX write request did not target the LT-tunable PHY Repeater
- If AUX write request targeted the LT-tunable PHY Repeater's DPCD register:
  - Changes the DPRX's reply of AUX_NACK with M = 0 with AUX_ACK,
  - Changes the DPRX's reply of AUX_DEFER with AUX_ACK, and then
  - Passes the DPRX's reply of AUX_ACK through.

The LT-tunable PHY Repeater must maintain the required number of pre-charge and SYNC pulses as defined in this Standard as AUX transactions traverse through the LT-tunable PHY Repeater in either the upstream or downstream direction.

When operating in Transparent mode, the LT-tunable PHY Repeater must not negatively impact the DPTX AUX Reply timeout unless the AUX request transaction addresses LT-tunable PHY Repeater DPCD register space. For example, a DPTX unaware of the LT-tunable PHY Repeater sets the DPTX AUX Reply timeout to 400us per this Standard. The LT-tunable PHY Repeater must not behave in a manner that negatively impacts the DPTX AUX Reply timeout.

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3.6.5.3.1 AUX Error Conditions

- No reply to an AUX request targeting the LT-tunable PHY Repeater field:
  - This will result in a Reply timeout within the DPTX. If the DPTX decides to issue another AUX request, the LT-tunable PHY Repeater must discard the previous transaction and act on the new request.
- DPRX replies with non-zero data to an AUX read request to its reserved space:
  - This non-compliant DPRX behavior might result in undefined system behavior.
- DPRX replies with an AUX_ACK to an AUX write request to its reserved space:
  - LT-tunable PHY Repeater must pass AUX_ACK upstream.
- Corrupted AUX request transaction:
  - Pass through to a DFP is implementation-specific.
  - If pass through, must not fix the cause of corruption.
  - Will result in an AUX Reply timeout in the DPTX.
- Corrupted AUX reply:
  - Pass through to a UFP is implementation-specific.
  - If pass through, must not fix the cause of corruption.
  - Will result in an AUX Reply timeout in the DPTX.

3.6.5.3.2 LT-tunable PHY Repeater AUX UFP (Informative)

The DPTX is likely to periodically issue AUX request transactions. The UFP of an LT-tunable PHY Repeater must continuously monitor the address of the AUX request transaction to determine whether the request targets the LT-tunable PHY Repeater. When the request address matches the LT-tunable PHY Repeater's address, the LT-tunable PHY Repeater must set an internal AUX_PEND flag. The AUX_PEND flag must remain set until the LT-tunable PHY Repeater has updated or modified the reply from the DPRX or a new AUX request transaction is received on the LT-tunable PHY Repeater's UFP.

Figure 3-50: LT-tunable PHY Repeater AUX UFP State Machine (Informative)

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3.6.5.3.3 LT-tunable PHY Repeater AUX DFP (Informative)

The DFP of an LT-tunable PHY Repeater will typically pass all AUX replies, untouched, to its UFP. In the case in which the internal AUX_PEND flag is set, the LT-tunable PHY Repeater must wait until the DPRX replies to an AUX request transaction. For a reply to an AUX read request, the LT-tunable PHY Repeater must either replace or modify the DPRX data with its own DPCD data. For a reply to an AUX write request, the LT-tunable PHY Repeater must modify the AUX reply acknowledge type (AUX_NACK M = 0 or AUX_DEFER) to an AUX_ACK. The internal AUX_PEND flag must be cleared after the reply is transmitted on the LT-tunable PHY Repeater's UFP.

Figure 3-51: LT-tunable PHY Repeater AUX DFP State Machine (Informative)

3.6.5.3.4 AUX Read Examples

The example depicted in Figure 3-52 shows the LT-tunable PHY Repeater's behavior when an AUX read request does not target the LT-tunable PHY Repeater. In this example, the DPRX's DPCD data 11h and 22h is passed, untouched, through the LT-tunable PHY Repeater to the DPTX.

Figure 3-52: AUX Read that Does Not Target LT-tunable PHY Repeater

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The example depicted in Figure 3-53 shows the LT-tunable PHY Repeater's behavior when an AUX read request targets an LT-tunable PHY Repeater's DPCD register. The DPRX responds to the AUX read request targeting its reserved space with 0s. The LT-tunable PHY Repeater changes the DPRX's data with its own data (AAh and BBh), then sends that data to the DPTX.

Figure 3-53: AUX Read that Targets LT-tunable PHY Repeater Only

3.6.5.3.5 AUX Write Examples

The reply to an AUX write request that does not target the LT-tunable PHY Repeater is always passed, untouched, through LT-tunable PHY Repeater. In Figure 3-54, the LT-tunable PHY Repeater forwards the AUX_ACK from the DPRX to DPTX.

Figure 3-54: AUX Write that Does Not Target LT-tunable PHY Repeater

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The example depicted in Figure 3-55 shows an AUX write request that targets the LT-tunable PHY Repeater. Because the LT-tunable PHY Repeater's DPCD registers are RESERVED in the DPRX, the DPRX will reply to the AUX write request with an AUX_NACK M = 0 –or– AUX_DEFER. The LT-tunable PHY Repeater must change the DPRX's reply to an AUX_ACK, which is then sent to the DPTX.

Figure 3-55: AUX Write Targets LT-tunable PHY Repeater

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3.6.6 Link Training

3.6.6.1 DPTX Training Requirements

This section describes the Link Training requirements for a DPTX that supports LT-Tunable PHY Repeaters (i.e., that chooses to place the repeaters into Non-transparent mode). DP upstream devices that do not enable the Non-transparent mode of LT-Tunable PHY Repeaters do not need to meet the requirements indicated within this section.

- DPTX must always provide a training pattern (TPS1, TPS2, TPS3, so forth).
- DPTX must only change its Main-Link Voltage Swing and Pre-emphasis levels when communicating with the most immediate downstream LT-tunable PHY Repeater. For example, if the PHY_REPEATER_CNT register (DPCD Address F0002h) is programmed to 08h, the DPTX must change its Main-Link levels based on values returned from the ADJUST_REQUEST_LANE0_1_LT_TUNABLE_PHY_REPEATER5 and ADJUST_REQUEST_LANE2_3_LT_TUNABLE_PHY_REPEATER5 DPCD registers.
- Before performing link training with LT-tunable PHY Repeater(s), the DPTX must place the LT-tunable PHY Repeater(s) into Non-transparent mode by writing AAh to the PHY_REPEATER_MODE register (DPCD Address F0003h).
- DPTX must write the DPRX's LINK_BW_SET and LANE_COUNT_SET registers (DPCD Addresses 00100h and 00101h, respectively) with the appropriate link rate and lane count, respectively.
- DPTX must not write to the DPRX's TRAINING_PATTERN_SET register (DPCD Address 00102h) unless the LT-tunable PHY Repeater closest to the DPRX has achieved CR.
- DPTX must complete the CR phase between itself and the downstream DPRX, including all LT-tunable PHY Repeaters in the path, before moving to the EQ phase of link training.
  - Achieve LANE*x*_CR_DONE on the first LT-tunable PHY Repeater before starting link training with next LT-tunable PHY Repeater.
  - Training pattern (TPS1) must remain active throughout the entire CR phase.
- DPTX must complete the EQ phase between itself and the downstream DPRX, including all LT-tunable PHY Repeaters in the path.
  - Achieve EQ and Symbol Lock, and align with the first LT-tunable PHY Repeater before moving to the next downstream device.
  - Training pattern (TPS2, TPS3, and so forth) must remain active throughout the entire EQ phase.
- DPTX must terminate Link Training by writing 00 to the TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 3:0) to notify the LT-tunable PHY Repeaters and DPRX that Link Training is complete.
- The LT-tunable PHY Repeater does not have a register that sets the Link Status/ Adjust Request read interval (TRAINING_AUX_RD_INTERVAL field in the TRAINING_AUX_RD_INTERVAL register (DPCD Address 0000Eh, bits 6:0)). Because of this, the DPTX must use a TRAINING_AUX_RD_INTERVAL of 100us for its Main-Link Clock Recovery phase and 400us for its Main-Link Channel Equalization phase when communicating with an LT-tunable PHY Repeater. This requirement does not impact communication with the DPRX. The TRAINING_AUX_RD_INTERVAL reported by the DPRX must be used when communicating with the DPRX.

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3.6.6.2 LT-Tunable PHY Repeater Training Requirements

- LT-tunable PHY Repeater must support up to four DP Main-Link lanes. Although the LT-tunable PHY Repeater can be trained to fewer than four lanes, it must support the DPRX's maximum lane capability.
- LT-tunable PHY Repeater must support all required Voltage Swing and Pre-emphasis combinations defined in Section 3.5.2.
- LT-tunable PHY Repeater does not create training patterns. The LT-tunable PHY Repeater will pass training patterns received on its UFP to its DFP.
- IRQ_HPD received on the LT-tunable PHY Repeater's DFP must be passed through to the LT-tunable PHY Repeater's UFP. The delay from "received on DFP" to "output on UFP" must be no greater than 200us.
- HPD unplug event on the LT-tunable PHY Repeater's DFP must be passed through to the LT-tunable PHY Repeater's UFP. The delay from "received on DFP" to "output on UFP" must be no greater than 200us.
- LT-tunable PHY Repeater's output must remain in an electrical idle state until LANE*x*_CR_DONE is achieved on its UFP.
- All LT-tunable PHY Repeaters must snoop AUX writes to DPRX's LINK_BW_SET and LANE_COUNT_SET registers (DPCD Addresses 00100h and 00101h, respectively). LT-tunable PHY Repeaters must use the information written to these two DPCD registers to enable the specified number of link rate and lanes, respectively.
- LT-tunable PHY Repeater must adjust its output levels (Voltage Swing and Pre-emphasis) based on an AUX write request to the TRAINING_LANE*x*_SET_PHY_REPEATER*y* DPCD register, where x = 0, 1, 2, or 3 and y = the PHY_REPEATER_CNT register's (DPCD Address F0002h) count of its immediate downstream device. For example, LT_TUNABLE_PHY_REPEATER3 must adjust its output levels based on AUX writes to LT_TUNABLE_PHY_REPEATER2.
- LT_TUNABLE_PHY_REPEATER1 with the PHY_REPEATER_CNT register (DPCD Address F0002h) programmed to 80h must adjust its output levels (Voltage Swing and Pre-emphasis) based on AUX writes to the DPRX's TRAINING_LANE*x*_SET_PHY_REPEATER1 DPCD register, where x = 0, 1, 2, or 3.
- LT-tunable PHY Repeater must consider link training to be complete when the DPRX's TRAINING_PATTERN_SELECT field in the TRAINING_PATTERN_SET register (DPCD Address 00102h, bits 3:0) transitions from non-zero to 00.

3.6.6.3 Error Cases

- Errors that occur during the LANE*x*_CR_DONE phase should follow Figure 3-20.
- Errors that occur during the EQ phase should follow Figure 3-21.

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3.6.6.4 Example Use Case

Figure 3-56 shows an LT-tunable PHY Repeater in both a notebook and docking station. This section will step through what the DPTX (GPU), LT-tunable PHY Repeater1, LT-tunable PHY Repeater2, and DPRX (Sink) behavior will be during link training. This example assumes that DPTX and DPRX are both DP v1.3-capable at a link rate of HBR3 (8.1Gbps/lane). It also assumes that the DPRX supports up to two lanes.

Figure 3-56: Notebook and Docking Station Example

3.6.6.4.1 LT-tunable PHY Repeater Recognition

Upon inserting the DPRX into a docking station, the DPRX will assert HPD upon detection of the DPTX. LT-tunable PHY Repeater1 will detect the assertion of HPD on its DFP and pass HPD assertion to its UFP. LT-tunable PHY Repeater2 will detect the assertion of HPD on its DFP and pass HPD assertion to its UFP.

After HPD has been propagated from the DPRX to the DPTX, a DP Source device with a DPTX will read the capability of the DP Sink device with a DPRX by reading EDID and the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155) of the DPRX. (EDID is not mapped to DPCD address space.) A DP1.3 LT-tunable PHY Repeater-aware DPTX is also required to read the LT-tunable PHY Repeater field (DPCD Addresses F0000h through F02FFh; see Table 2-169) to determine if and how many LT-tunable PHY Repeater(s) are present. This read must be in the form of a native AUX read transaction of 4 bytes.

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Figure 3-57: LT-tunable PHY Repeater Recognition

Because PHY_REPEATER_CNT = 40h, the DPTX knows that there are two LT-tunable PHY Repeaters between itself and the DPRX. The LT-tunable PHY Repeater with the smallest PHY_REPEATER_CNT value is closest to the DPTX while the LT-tunable PHY Repeater with largest PHY_REPEATER_CNT value is furthest from the DPTX but closest to the DPRX.

The DPTX will use the link rate returned by MAX_LINK_RATE_PHY_REPEATER and MAX_LINK_RATE of the DPRX to determine the supported link rates. The DPTX will then enable Non-transparent mode in all LT-tunable PHY Repeaters by changing the PHY_REPEATER_MODE DPCD register. The DPTX must then write to the DPRX's LINK_BW_SET and LANE_COUNT_SET within those that are indicated as HBR3 in the DPRX's MAX_LINK_RATE and MAX_LANE_COUNT registers (i.e., 8.1Gbps/lane) and a lane count of 2 in this example.

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3.6.6.4.2 CR Phase with LT-tunable PHY Repeater2

The DPTX will start LANE*x*_CR_DONE phase of Link Training with LT-tunable PHY Repeater2. Because all AUX transactions are passed through, LT-tunable PHY Repeater1 will also detect the start of LANE*x*_CR_DONE phase of Link Training. Because the DPRX's Link Training registers are located in the 100h range, however, the Sink device will not know that Link Training has begun.

DPTX will set in the LT-tunable PHY Repeater2:

- TRAINING_PATTERN_SET_PHY_REPEATER2 = 2h
- TRAINING_LANE0_SET_PHY_REPEATER2 = 00h (Voltage Swing Level 0 and Pre-emphasis Level 0)
- TRAINING_LANE1_SET_PHY_REPEATER2 = 00h (Voltage Swing Level 0 and Pre-emphasis Level 0).

In Figure 3-58, LT-tunable PHY Repeater1 passes the AUX reply from the DPRX untouched because the AUX write request targeted LT-tunable PHY Repeater2 registers, not LT-tunable PHY Repeater1 registers. It is LT-tunable PHY Repeater2's responsibility to modify the reply from the DPRX.

Figure 3-58: Start of CR Phase with LT-tunable PHY Repeater2

Figure 3-59 shows that LT-tunable PHY Repeater2 has not achieved LANE*x*_CR_DONE for either Lane 0 or Lane 1 and thus requested a change in voltage swing level and pre-emphasis level from the DPTX.

Figure 3-59: Read Status of LT-tunable PHY Repeater2 Lane0 and Lane1

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Figure 3-60: DPTX Adjust Output Voltage Swing and Pre-emphasis

Figure 3-61 depicts LT-tunable PHY Repeater2 achieving LANE*x*_CR_DONE on Lanes 0 and 1. Immediately after achieving LANE*x*_CR_DONE, LT-tunable PHY Repeater2 starts transmitting TPS1 on its DFP.

Figure 3-61: LT-tunable PHY Repeater2 LANE*x*_CR_DONE Achieved

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3.6.6.4.3 LANE*x*_CR_DONE Phase with LT-tunable PHY Repeater1

After confirming LANE*x*_CR_DONE is accomplished with LT-tunable PHY Repeater2, DPTX will then verify if LANE*x*_CR_DONE occurs with LT-tunable PHY Repeater1.

In Figure 3-62, LT-tunable PHY Repeater1 LANE*x*_CR_DONE status flags are not set and ADJUST_REQ_LANE0_1 indicates LT-tunable PHY Repeater1 is requesting Swing Level 2 and pre-emphasis level 0.

Figure 3-62: Determine LT-tunable PHY Repeater1's LANE*x*_CR_DONE Status

DPTX will write swing level 2 and pre-emphasis level 0 to LT-tunable PHY Repeater1 TRAINING_LANE0_SET and TRAINING_LANE0_SET registers as depicted in Figure 3-63. LT-tunable PHY Repeater2 will snoop this write and adjust its output levels to voltage swing level 2 and pre-emphasis level 0.

Figure 3-63: LT-tunable PHY Repeater2 Adjust Output Voltage Swing and Pre-Emphasis

The DPTX swing and pre-emphasis level always stays fixed. Only LT-tunable PHY Repeater2 will adjust its output levels.

After receiving the acknowledge to the AUX Write request, the DPTX will then check to see if LT-tunable PHY Repeater1 has achieved LANE*x*_CR_DONE on Lanes 0 and 1.

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Figure 3-64: LT-tunable PHY Repeater1 LANE*x*_CR_DONE Achieved

After LANE*x*_CR_DONE is achieved at LT-tunable PHY Repeater closest to the DPRX, the DPTX can then initiate LANE*x*_CR_DONE phase of link training with DPRX.

It is possible that the LT-tunable PHY Repeater 1 LANE*x*_CR_DONE on both Lanes 0 or 1 is never achieved. This could happen if all combinations of voltage swing are exhausted as defined by Figure 3-20. If this occurs, the DPTX shall terminate link training by writing 00h to TRAINING_PATTERN_SET_PHY_REPEATER. Because this DPCD field is mirrored in all LT-tunable PHY repeaters between a DPTX and DPRX, all LT-tunable PHY repeaters will detect an end to link training. A DPTX must then attempt to train the link between itself and the LT-tunable PHY Repeater2 at a lower rate. For this particular use case, the next rate is HBR2. A DPTX must write a 14h to the LINK_BW_SET register (DPCD Address 00100h) and then perform a LANE*x*_CR_DONE phase with the LT-tunable PHY Repeater2, as described in Section 3.6.6.4.2. After LANE*x*_CR_DONE is achieved on both LT-Tunable PHY Repeater1 and Repeater2, the DPTX should begin the LANE*x*_CR_DONE phase with the DPRX.

3.6.6.4.4 CR Phase with DPRX

DPTX will start LANE*x*_CR_DONE phase of link training with DPRX by writing to DPRX's DPCD registers. The LT-tunable PHY Repeater closest to DPRX (LT-tunable PHY Repeater1) will snoop writes to DPRX's link training DPCD registers.

LT-tunable PHY Repeater1 will adjust its output based on aux write request to DPRX's DPCD registers TRAINING_LANE*x*_SET, where $x = 0$ and 1. In the example shown in Figure 3-65, the DPTX began with a Voltage Swing Level 0 and Pre-emphasis Level 0.

Figure 3-65: Start CR Phase with DPRX

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In Figure 3-66, the DPTX determines that the DPRX has achieved LANE*x*_CR_DONE. After LANE*x*_CR_DONE is achieved with the DPRX, the DPTX can then begin the EQ phase of Link Training with LT-tunable PHY Repeater1 and LT-tunable PHY Repeater2.

Figure 3-66: DPRX LANE*x*_CR_DONE Achieved

3.6.6.4.5 EQ Phase with LT-tunable PHY Repeater2

A DPTX will switch from LANE*x*_CR_DONE phase to the EQ phase of Link Training by changing the training pattern to TPS3 (or TPS4 if supported by both DPTX and DPRX) and writing to LT-tunable PHY Repeater2's TRAINING_PATTERN_SET and TRAINING_LANE*x*_SET, where $x = 0$ and 1.

In Figure 3-67, that LT-tunable PHY Repeater1 detects the EQ phase has begun by monitoring the AUX write that targeted LT-tunable PHY Repeater2. Both LT-tunable PHY Repeater1 and LT-tunable PHY Repeater2 are in the EQ phase and will update their respective ADJUST_REQUEST_LANE0_1_LT-tunable PHY Repeater DPCD register as needed.

Figure 3-67: Initiate EQ Phase with LT-tunable PHY Repeater1 and 2

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Figure 3-68 shows that LT-tunable PHY Repeater2 has not achieved LANE*x*_SYMBOL_LOCKED. LT-tunable PHY Repeater2 requests an increase in pre-emphasis-level.

Figure 3-68: Determine LT-tunable PHY Repeater2 EQ Status

The DPTX will increase the pre-emphasis level to one and write appropriate value to LT-tunable PHY Repeater2's TRAINING_LANE*x*_SET, where *x* = 0 and 1 as shown in Figure 3-69.

Figure 3-69: DPTX Adjust Pre-emphasis Level

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Figure 3-70 shows that LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE are all achieved for LT-tunable PHY Repeater2. A DPTX can then move to EQ phase with LT-tunable PHY Repeater1. Because LT-tunable PHY Repeater1 has been in EQ phase while LT-tunable PHY Repeater2 was in EQ phase, LT-tunable PHY Repeater1 also achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE near the time LT-tunable PHY Repeater2 achieved the same.

Figure 3-70: LT-tunable PHY Repeater2 EQ Phase Achieved

3.6.6.4.6 EQ Phase with LT-tunable PHY Repeater1

The DPTX will read the lane status for Lanes 0 and 1 for LT-tunable PHY Repeater1. As noted in the previous section, LT-tunable PHY Repeater1 has achieved LANE*x*_CR_DONE, LANE*x*_SYMBOL_LOCKED, CHANNEL_EQ_DONE, and INTERLANE_ALIGN_DONE.

Figure 3-71: LT-tunable PHY Repeater1 EQ Phase Achieved

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3.6.6.4.7 EQ Phase with DPRX

Once DPTX has completed EQ phase with LT-tunable PHY Repeater1 and LT-tunable PHY Repeater2, it then will initiate EQ phase with the DPRX.

DPTX will write to the DPRX's TRAINING_PATTERN_SET (DPCD 00102h), TRAINING_LANE0_SET (DPCD 00103h), and TRAINING_LANE1_SET (DPCD 00104h) to notify DPRX the start of EQ phase of Link Training.

Figure 3-72: Start EQ Phase with DPRX

LT-tunable PHY Repeater1 monitors all AUX writes to TRAINING_LANE*x*_SET, where *x* = 0 and 1, and will update its output levels as specified in the AUX write.

In Figure 3-73, the DPTX reads the DPRX's lane status and adjust request DPCD registers (00202h thru 00206h).

Figure 3-73: Determine DPRX's EQ Phase Status

The DPRX's lane status registers do not indicate LANE*x*_SYMBOL_LOCKED and request an increase in pre-emphasis level.

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In Figure 3-74, the DPTX writes to the DPRX's TRAINING_LANE*x*_SET, where *x* = 0 and 1) to indicate an increase to level 1 pre-emphasis. LT-tunable PHY Repeater1 monitors this write and increases the pre-emphasis level.

Figure 3-74: LT-tunable PHY Repeater1 Adjust Pre-emphasis Level

Figure 3-75: EQ Phase Achieved at DPRX

EQ phase is achieved in DPRX as well as with LT-tunable PHY Repeater1 and LT-tunable PHY Repeater2. The DPTX can now end link training and start transmitting an Idle Pattern.

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3.6.6.4.8 End of Link Training

The DPTX ends link training by writing to the DPRX's TRAINING_PATTERN_SET (DPCD 00102h) to a 0 value. All the LT-tunable PHY Repeaters continuously monitor writes to this register. Any time the TRAINING_PATTERN_SELECT field within DPCD 00102h transitions to a 0 value, the LT-tunable PHY Repeaters know that link training is finished. The DPTX changes pattern to the Idle Pattern.

Figure 3-76: End Link Training

3.6.7 Dual Mode Requirements

Support of Dual Mode adaptors is optional. However, if the LT-tunable PHY Repeater supports Dual Mode adaptors being connected to their DFP, the LT-tunable PHY Repeater must meet the requirements outlined in this section.

1. CONFIG1 must be connected to each LT-tunable PHY Repeater between the Dual Mode adaptor and DPTX
   a. LT-tunable PHY Repeater must use CONFIG1 to know if downstream traffic is standard DP or DP++ (TMDS over DisplayPort).
2. DDC communication (whether in the form of I^2C-over-AUX trans action syntax or in 3.3V I^2C) between DPTX and Dual Mode adaptor must not be negatively impacted.
3. LT-tunable PHY Repeater output electrical levels must comply with Dual Mode standard requirement for a Dual Mode DPTX.
4. LT-tunable PHY Repeater must be able to accept a 25 to 300MHz TMDS clock as required by the Dual Mode standard and pass through to its DFP.
5. The LT-tunable PHY Repeater must not implement the Dual Mode Adaptor ID unless it implements the AC-coupling to DC-coupling level shift on its output port.

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3.6.8 LT-tunable PHY Repeater Electrical Specification Requirements

3.6.8.1 LT-tunable PHY Repeater DPTX_PHY Electrical Compliance

An LT-tunable PHY Repeater that is connected to a DisplayPort connector must meet the electrical requirements defined in Section 3.5.2.

Before any TX electrical testing can be performed, the link between the DPTX and DPRX (in this case, a piece of test equipment), including all LT-tunable PHY Repeaters within the path, must be trained as defined in this Standard. After the link is trained to a specific link rate, the DPTX can change the LT-tunable PHY Repeater's output levels (TX voltage swing and pre-emphasis levels) by writing to the DPRX's TRAINING_LANE*x*_SET register(s) (DPCD Addresses 00103h through 00106h). A change in the TEST_LANE_COUNT or TEST_LINK_RATE register (DPCD Address 00220h or 00219h, respectively) requires that the link be re-trained between the DPTX and DPRX.

3.6.8.2 LT-tunable PHY Repeater DPRX_PHY Electrical Compliance

An LT-tunable PHY Repeater that is connected to a DisplayPort connector must meet the electrical requirements defined in Section 3.5.2.

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4 Mechanical

This section describes the mechanical specifications of a DP link. Cable assembly specification for external connection and connector specification are covered in this section. Applications requiring a larger or longer box-to-box application space than supported by a passive cable assembly as defined in this section may be supported by the use of an active Hybrid device or any other such device as provided for under Section 2.1.4. The interfaces of these devices must meet the interface requirements of a Source and Sink device.

4.1 Cable-Connector Assembly Specifications (for Box-to-box)

The cable assembly specification is divided into two categories reflecting the high bit rate (2.7Gbps/lane, 5.4Gbps/lane, and 8.1Gbps/lane) and the low bit rate (1.62Gbps/lane), respectively.

The high bit rate specification generally has higher performance electrical requirements and is usually represented by one or more of the following: shorter lengths, larger wire gauges, lower dielectric loss insulation materials.

The low bit rate specification generally has lower performance electrical requirements and is usually represented by one or more of the following: longer lengths, smaller wire gauges, higher dielectric loss insulation materials.

Among the cable-connector assembly parameters, IL (insertion loss), RL (reflection loss), skew (both intra- and inter-pair), and Near-End Noise (NEN) differ between high bit rate and low bit rate specifications. The PSELFEN (power sum equal level far-end noise) parameter applies to the high bit rate cable assembly specification only.

Both categories represent the box-to-box application space sometimes referred to as external/ desktop and consumer electronics (CE).

The embedded cable application space which is characterized by its inaccessibility to the end-user and is sometimes referred to as internal/mobile is not explicitly specified here. Instead, the system integrator is required to meet the EYE mask requirements at the receiver pins by making appropriate trade-offs between circuit trace performance and cabling performance.

In general the high bit rate and low bit rate electrical specification presented below still apply to the internal/mobile cable assemblies given the same PCB traces at both ends of the channel except that the physical dimensions are much smaller.

The cable-connector assembly is tested with test fixtures that have receptacle connectors, as described in PHY Compliance Test Specification v1.2b.

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4.1.1 Cable-Connector Assembly Definition

A DP Cable Assembly is comprised of two plug-type connectors terminating both ends of a bulk cable.

The plug on either end may be a full-size DP plug or an mDP plug.

Table 4-1 lists the supported Cable Assembly types.

Table 4-1: Supported Cable Assembly Types

Type	Description
C1	Cable Assembly with a full-size DP plug on each end. The Type C1 Cable Assembly is depicted in Figure 4-1.
C2	Cable Assembly with an mDP plug on one end and a full-size DP plug on the other end. The Type C2 Cable Assembly is depicted in Figure 4-2.
C3	Cable Assembly with an mDP plug on each end. The Type C3 Cable Assembly is depicted in Figure 4-3.

Figure 4-1: Type C1 Cable Assembly

Figure 4-2: Type C2 Cable Assembly

Figure 4-3: Type C3 Cable Assembly

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A DP Connector Resizing Adaptor is comprised of a plug-type connector terminating one end of a bulk cable and a receptacle type connector terminating the other end of the same cable.

Table 4-2 lists the supported Resizing Adaptor Assembly types.

Table 4-2: Supported Resizing Adaptor Types

Type	Description
A1	Resizing Adaptor with an mDP plug on one end and a full-size DP receptacle on the other end. The Type A1 Resizing Adaptor is depicted in Figure 4-4.
A2	Resizing Adaptor with a full-size DP plug on one end and an mDP receptacle on the other end. The Type A2 Resizing Adaptor is depicted in Figure 4-5.

Figure 4-4: Type A1 Resizing Adaptor

Figure 4-5: Type A2 Resizing Adaptor

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In addition, a Sink may have a permanently attached cable with a full-size DP plug or a permanently attached cable with an mDP plug.

A DP Extension Cable is designed specifically to be used in conjunction with displays (or adaptors) with a permanently attached cable with an mDP plug.

Table 4-3 lists the supported Extension Cable type.

Table 4-3: Supported Extension Cable Type

Type	Description
E1	Cable Assembly with an mDP plug on one end and an mDP receptacle on the other end. The Type E1 Extension Cable is depicted in Figure 4-6.

Figure 4-6: Type E1 Extension Cable

The following configurations of Cable Assemblies and Resizing Adaptors are supported:

- Upstream Device (TP2) -> Cable Assembly type C1 -> Downstream Device (TP3)
- Upstream Device (TP2) -> Cable Assembly type C2 -> Downstream Device (TP3)
- Upstream Device (TP2) -> Cable Assembly type C3 -> Downstream Device (TP3)
- Upstream Device (TP2) -> full-size DP plug permanently attached to Downstream Device
- Upstream Device (TP2) -> mDP plug permanently attached to Downstream Device
- Upstream Device (TP2) -> Resizing Adaptor type A1 -> full-size DisplayPort plug permanently attached to Downstream Device
- Upstream Device (TP2) -> Resizing Adaptor type A2 -> mDP plug permanently attached to Downstream Device
- Upstream Device (TP2) -> Extension Cable type E1 -> mDP plug permanently attached to Downstream Device

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The following configurations of Cable Assemblies and Resizing Adaptors are supported for RBR and HBR only:

- Upstream Device (TP2) -> Resizing Adaptor type A1 -> Cable Assembly type C1 -> Downstream Device (TP3)
- Upstream Device (TP2) -> Resizing Adaptor type A2 -> Cable Assembly type C3 -> Downstream Device (TP3)

In addition to the above Cable Assembly types, active versions of Cable Assemblies of types C1, C2, C3, and E1 are supported, denoted C1A, C2A, C3A, and E1A, respectively. See Section 5.8.3 for active cable assembly details.

4.1.1.1 Cable Construction Guideline for EMI Reduction (Informative)

The following recommendations for the construction of DP cable assemblies should be followed to prevent EMI issues:

- The intra-pair skew for differential pairs in the cable assembly should be made as small as possible and should meet the defined limits defined by the cable assembly electrical specification.
- The termination of the cable shielding to the connector shield should cover a full 360° around the cable and be of low impedance.
- The shielding between the device chassis, DP receptacle shield, DP plug shield, and cable shielding should form a unified low impedance link in order to maximize the efficiency of the shielding and minimize EMI. To facilitate this, the use of multiple grounding points and contact points between shield parts is recommended.
- As a general rule, unnecessary apertures in the shields may cause leakage. It is strongly recommended that the gaps between shielding components be eliminated. It is also strongly recommended that the shell cover as much of the connector as possible to yield the maximum EMI protection of the signal pins.
- As a recommendation, the shielding construction of the bulk cable should follow general high-speed practices of including both a foil and braid shielding materials in its construction. A further recommendation is that the foil layer be an Al/Mylar wrap (spiral or longitudinal) with a minimum 20% overlap, and that the conductive braid have a minimum 75% coverage over the inner foil layer to ensure effective EMI shielding.

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4.1.2 Type of Bulk Cable

The bulk cable must be chosen to meet or exceed all of the electrical and mechanical requirements described below. A reference construction is depicted in Figure 4-7.

Figure 4-7: Bulk Cable Construction (Informative – for Reference Only)

The following is the description of the reference bulk cable construction. This description is for reference only.

- Overall shielded (braid) structure coated with jacket above;
- **Unit "A"** – P1-P5 'STP' or 'Twinax' #30 AWG insulated stranded conductors, with #30 AWG drain conductor for use in Cable Assembly Type C1 and displays with permanently attached cables with full-size DisplayPort connectors, and #36 or #38 AWG insulated stranded conductors, with #36 or #38 AWG drain conductor for use in all other Cable Assemblies, Resizing Adaptors and Extension Cables (for use for Main-Link and AUX connections);
- **Unit "B"** – Unshielded, #30 AWG single insulated stranded conductors (for GND). #30 - #8 AWG single insulated stranded conductor (for use for CONFIG1, CONFIG2 and HPD connections).

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Examples of differences:

- Wire gauge selection is implementation-specific provided all appropriate electrical cable specifications are met.
- A cable permanently attached to a DP device may have less than four Main-Link Lanes.
- Downstream devices with permanently attached cables may have an extra #24 to #28 AWG single insulated stranded conductor for power.
- Resizing Adaptors must have a #30 to #36 AWG single insulated stranded conductor for power.
- Extension Cables must carry all four lanes and include a #24 AWG single insulated stranded conductor for power.

4.1.3 Impedance Profile

The impedance profile is intended to provide confidence in the system and connector design. The return loss specification given later in this chapter provides the limit on the electrical performance resulting from impedance excursions and mismatches.

The impedance specification is defined in the time domain. The impedance profile must be measured using a controlled impedance fixture and TDR with a differential sampling head. The fixture rise time must be 50ps (20 to 80%) or faster while the readout of measurement must be filtered to tr = 130ps (20 to 80%). Two impedance profiles are defined:

- One for when the impedance is measured through a full-size DP connector
- One for when the impedance is measured through an mDP Connector

Impedance values attributed in part or in whole to the connector on the Cable Assembly under test must conform to those listed in Table 4-4 or Table 4-5, as appropriate. Figure 4-8 and Figure 4-9 shows examples of measured data.

The Impedance Profile as it applies to the test fixture is Informative. The test fixture requirements are defined in DP PHY CTS Specification.

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4.1.3.1 Impedance Profile through a DP Connector

Table 4-4: Impedance Profile Values for Cable Assembly

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100Ω	±10%	Fixture should have trace lengths of no more than 50mm (2 inches)
Connector	100Ω	±10%	
Wire management	100Ω	±10%	Transition from ±10% to ±5% must have a slope of 5Ω / 80ps
Cable	100Ω	±5%	

Figure 4-8: Differential Impedance Profile Measurement Data Example

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4.1.3.2 Impedance Profile through an mDP Connector

Table 4-5: Impedance Profile Values for Cable Assembly

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100Ω	±10%	Fixture should have traces lengths of no more than 50mm (2 inches)
Connector	100Ω	±15%	Exception window peak duration of 200ps, Transition from ±15% to ±5% must have a slope of 10Ω / 200ps
Wire management	100Ω	±10%	
Cable	100Ω	±5%	

Figure 4-9: mDP Differential Impedance Profile Measurement Data Example

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4.1.4 Insertion Loss and Return Loss

Insertion Loss and Return Loss specified in this section are the mixed mode S-Parameters known as SDD21 and SDD11, respectively. Unlike Single-Ended case, SDDij refers to differential stimulus and differential response as illustrated in the following matrix of all mixed modes in differential case as shown in Table 4-6.

Table 4-6: Mixed Mode Differential/Common Relations of S-Parameters

Response	Stimulus			
	Differential		Common	
Differential	SDD11	SDD12	SDC11	SDC12
	SDD21	SDD22	SDC21	SDC22
Common	SCD11	SCD12	SCC11	SCC12
	SCD21	SCD22	SCC21	SCC22

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4.1.5 High Bit Rate Cable-Connector Assembly Specification

4.1.5.1 Insertion Loss and Return Loss

The following equations represent the reference lines that limit the Insertion Loss and Return Loss measured results. Insertion loss limits are provided for Cable Assembly types C1, C2, and C3, for Resizing Adaptors and for Extension cables. Return loss limits are provided for cable assemblies and resizing adaptors when measured through the full-size DP connector and when measured through the mDP connector.

4.1.5.1.1 Insertion Loss – Lower Limit for High Bit Rate Cable Assembly Type C1, C2, and C3

$$IL_{\min.}[dB] = \begin{cases} -8.7 \times \sqrt{\dfrac{f}{f_0}} - 0.072; & 0.1 < f \le \dfrac{f_0}{3} \\ 5.68\sqrt{f} - 5.3 * f - 6.52; & \dfrac{f_0}{3} < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 1.35GHz$

Figure 4-10 depicts the charts that represents the above equation's Insertion Loss, and must be referenced as the lower limit. The cable assembly measured results must comply with this limit.

Figure 4-10: Mixed Mode Differential Insertion Loss for HBR Cable Assembly Types C1, C2, and C3

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4.1.5.1.2 Insertion Loss – Lower Limit for High Bit Rate Resizing Adaptors

$$IL_{\min.}[dB] = \begin{cases} -1.6 \times \sqrt{\dfrac{f}{f_0}}; & 0.1 < f \le \dfrac{f_0}{3} \\ 1.75\sqrt{f} - 1.65 * f - 1.31; & \dfrac{f_0}{3} < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 1.35 GHz$

Figure 4-11 depicts the chart that represents the above equation's Insertion Loss, and must be referenced as the lower limit. The resizing adaptor measured results must comply with this limit.

Figure 4-11: Mixed Mode Differential Insertion Loss for HBR Resizing Adaptor

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4.1.5.1.3 Insertion Loss – Lower Limit for Extension Cables

$$IL_{\min.}[dB] = \begin{cases} -5.22 \times \sqrt{\dfrac{f}{f_0}} - 0.043\,; & 0.1 < f \le \dfrac{f_0}{3} \\ 3.41\sqrt{f} - 3.18 * f - 3.91; & \dfrac{f_0}{3} < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 1.35GHz$

Figure 4-12 depicts the chart that represents the above equation's Insertion Loss, and must be referenced as the lower limit. The Extension Cable measured results must comply with this limit.

Figure 4-12: Mixed Mode Differential Insertion Loss for Extension Cable

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4.1.5.1.4 Return Loss – Upper Limit for HBR Cable Assembly/Adaptor (Full-sized DP Connector)

The return loss for a HBR Cable Assembly or Resizing Adaptor measured through a full-sized DP connector is given by:

$$RL_{\max.}[dB] = \begin{cases} -15; & 0.1 < f \le \frac{f_0}{2} \\ -15 + 12.3\, Log_{10}\left(\frac{2f}{f_0}\right); & \frac{f_0}{2} < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 1.35GHz$

Figure 4-13 shows the chart that represents the above Return Loss equation and must be referenced as the upper limit for Return Loss.

The measured cable assembly results must comply with this limit.

Figure 4-13: Mixed Mode Differential RL for HBR Cable Assembly/Adaptor (DP Connector)

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4.1.5.1.5 Return Loss – Upper Limit for HBR Cable Assembly/Adaptor/Extension Cable

The return loss for a HBR Cable Assembly, Resizing Adaptor or Extension Cable measured through an mDP connector is given by:

$$RL_{\max.}[dB] = \begin{cases} -15; \quad 0.1 < f \le \dfrac{f_0}{2} \\ -15 + 12.3\, Log_{10}\left(\dfrac{2f}{f_0}\right); \quad \dfrac{f_0}{2} < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 1.35GHz$

Figure 4-14 shows the chart that represents the above Return Loss equation and must be referenced as the upper limit for Return Loss.

The measured cable assembly results must comply with this limit.

Figure 4-14: Mixed Mode Differential RL for HBR Cable Assembly/Adaptor (mDP Connector)

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4.1.5.2 Near End Noise

The Near End Noise (NEN) specification applies to all cable assembly types. It is defined in the frequency domain and covers the bandwidth up to 7GHz. The NEN must be lower than the upper limit in the Isolation equation and depicted in Figure 4-15.

4.1.5.2.1 Near End Noise – Upper Limit for High Speed Cable Assembly

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\dfrac{f}{f_0}\right) & ; \quad f_0 < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 1.35GHz$

Figure 4-15: Near-End Total Noise (peak) for HBR Cable Assembly

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4.1.5.3 Power Sum Equal Level Far-End Noise

The Power Sum Equal Level Far-End Noise (PSELFEN) specification applies to all cable assembly types. The PSELFEN represents the difference between cable insertion loss and the total power sum far-end noise from aggressor cable lanes.

$$PSFEN(f) = 10 \times \log \sum_{1}^{n} 10^{\left(\frac{FENn(f)}{10}\right)}$$

$$PSELFEN(f) = PSFEN(f) - IL(f)$$

Where:

FENn(f) is the far-end noise in dB

IL(f) is the victim lane insertion loss in dB

The Power Sum Equal Level Far-End Noise must be lower than the upper limit depicted in Figure 4-16.

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4.1.5.3.1 Power Sum Equal Level Far-End Noise – Upper Limit for High Speed Cable Assembly

$$PSELFEN_{\max.}[dB] = \begin{cases} -22 + 6Log_{10}\left(\frac{f}{f_0}\right); & 0.1 < f \le f_0 \\ -22 + 40Log_{10}\left(\frac{f}{f_0}\right); & f_0 < f \le 8.1 \end{cases}$$

Where:

f is given in GHz

$f_0 = 2.7GHz$

Figure 4-16: Power Sum Equal Level Far-End Total Noise (peak) for HBR Cable Assembly

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4.1.5.4 Intra- and Inter-Pair Skew

Both intra-pair and inter-pair skew are measured in the time domain with Differential TDR at the fixture rise/fall time, i.e., 50ps measured (20 to 80%).

4.1.5.4.1 Intra-Pair Skew

Table 4-7 lists the intra-pair skew limits, when measured as depicted in Figure 4-17.

Table 4-7: Intra-Pair Skew Limits

Component Type	Limit
Cable Types C1, C2, and C3	≤ 50ps
Resizing Adaptors Types A1 and A2	≤ 10ps
Extension Cables Type E1	≤ 35ps

Figure 4-17: Intra-Pair Skew Measurement Method

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4.1.5.4.2 Inter-Pair Skew

Table 4-8 lists the inter-pair skew limits, when measured as depicted in Figure 4-18.

Table 4-8: Inter-Pair Skew Limits

Component Type	Limit
Cable Types C1, C2, and C3	≤ 2UI
Resizing Adaptors Types A1 and A2	≤ 2UI
Extension Cables Type E1	≤ 1UI

Figure 4-18: Inter-Pair Skew Measurement Method

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4.1.6 Reduced Bit Rate Cable-Connector Assembly Specification

4.1.6.1 Insertion Loss and Return Loss

The following equations represents the reference line that limits the Insertion Loss and Return Loss measured results.

4.1.6.1.1 Insertion Loss – Lower Limit for Reduced Bit Rate Cable Assembly

$$IL_{\min.}[dB] = \begin{cases} -1 - 13.5 \times \sqrt{\dfrac{f}{f_0}} & ; \quad 0.01 < f \le \dfrac{f_0}{3} \\ -2.1 - [12(f - \dfrac{f_0}{3}) + 6.8] & ; \quad \dfrac{f_0}{3} < f \le 4 \end{cases}$$

Where:

f is given in GHz

$f_0 = 0.825 GHz$

Figure 4-19 shows the chart representing the above Insertion Loss and must be referenced as the lower limit. The measured cable assembly results must comply with this limit.

Figure 4-19: Mixed Mode Differential Insertion Loss (SDD21) Mask of RBR Cable

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4.1.6.1.2 Return Loss – Upper Limit for Reduced Bit Rate Cable Assembly

$$RL_{\max.}[dB] = \begin{cases} -15 & ; \quad 0.1 < f \le \frac{f_0}{2} \\ -15 + 12\ Log_{10}\left(2x\frac{f}{f_0}\right) & ; \quad \frac{f_0}{2} < f \le 4 \end{cases}$$

Where:

f is given in GHz

$f_0 = 0.8GHz$

Figure 4-20 shows the chart representing the above Return Loss and must be referenced as the upper limit.

The cable assembly measured results must comply with these limits.

Figure 4-20: Mixed Mode Differential Return Loss (SDD11) of RBR Cable

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4.1.6.2 Near-End Noise

Near-End Noise (NEN) must be lower than the upper limit in the Isolation equation and depicted in Figure 4-21.

4.1.6.2.1 Near-End Noise – Upper Limit for Reduced Bit Rate Cable Assembly

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\dfrac{f}{f_0}\right) & ; \quad f_0 < f \le 4 \end{cases}$$

Where:

f is given in GHz

$f_0 = 0.8GHz$

Figure 4-21: Near-End Total Noise (peak) for RBR Cable Assembly

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4.1.6.3 Far-End Noise

Far-End Noise (FEN) must be lower than the upper limit depicted in Figure 4-22.

Figure 4-22: Far-End Total Noise (peak) for RBR Cable Assembly

4.1.6.4 Intra- and Inter-Pair Skew

Both intra- and inter-pair skew are measured in the time domain with Differential TDR at fixture rise/fall time (i.e., 50ps measured (20 to 80%)).

4.1.6.4.1 Intra-Pair Skew

Intra-pair skew must be no more than 250ps.

See Figure 4-17 for the measurement method.

4.1.6.4.2 Inter-Pair Skew

Inter-pair skew must be no more than 2UI at RBR for Cable Types C1, C2, and C3. See Figure 4-18 for the measurement method.

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4.2 Connector Specification

This section describes the specifications of the external and internal DP connectors.

4.2.1 External Full-size Connector

4.2.1.1 Connector Pin Assignment

Table 4-9 shows the pin assignments of the DP external connector on a downstream-facing port (DFP) on an upstream device. Table 4-10 shows the pin assignments of the DP external connector on an upstream-facing port (UFP) on an downstream device.

Table 4-9: DFP Connector Pin Assignment

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	Out	ML_Lane 0(p)	Top	
2	GND	**GND**	Bottom	
3	Out	ML_Lane 0 (n)	Top	
4	Out	ML_Lane 1 (p)	Bottom	
5	GND	GND	Top	
6	Out	ML_Lane 1 (n)	Bottom	
7	Out	ML_Lane 2 (p)	Top	
8	GND	**GND**	Bottom	
9	Out	ML_Lane 2 (n)	Top	
10	Out	ML_Lane 3 (p)	Bottom	
11	GND	**GND**	Top	
12	Out	ML_Lane 3 (n)	Bottom	
13	CONFIG[a]	**CONFIG1**	Top	
14	CONFIG[a]	**CONFIG2**	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	**GND**	Bottom	
17	I/O	AUX CH (n)	Top	
18	In	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out[b]	DP_PWR	Bottom	

a. Pins 13 and 14 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low-impedance ground path from these pins.

b. Pin 20, PWR Out, must provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.

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Table 4-10: UFP Connector Pin Assignment

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	In	ML_Lane 3(n)	Top	
2	GND	**GND**	Bottom	
3	In	ML_Lane 3 (p)	Top	
4	In	ML_Lane 2 (n)	Bottom	
5	GND	**GND**	Top	
6	In	ML_Lane 2 (p)	Bottom	
7	In	ML_Lane 1 (n)	Top	
8	GND	**GND**	Bottom	
9	In	ML_Lane 1 (p)	Top	
10	In	ML_Lane 0 (n)	Bottom	
11	GND	**GND**	Top	
12	In	ML_Lane 0 (p)	Bottom	
13	CONFIG[a]	**CONFIG1**	Top	
14	CONFIG[a]	**CONFIG2**	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	**GND**	Bottom	
17	I/O	AUX CH (n)	Top	
18	Out	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out[b]	DP_PWR	Bottom	

a. *Pins 13 and 14 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low-impedance ground path from these pins.*

b. *Pin 20, PWR Out, must provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.*

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Figure 4-23 shows the wiring of an external cable connector assembly. The standard external cable connector assembly must not have a wire on pin 20, DP_PWR.

Figure 4-23: External Cable Connector Assembly Wiring

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4.2.1.2 Contact Sequence

Table 4-11 shows the legend for signal name/type mating level.

Table 4-11: Mating Sequence Level

Signal Type			Level
Connector Shell			First Mate
DP_PWR	Return	GND	Second Mate
Auxiliary (+) / (-)	ML_Lane (i) (+) / (-)	Hot Plug Detect	Third Mate

Figure 4-24: Connector Mating Levels

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4.2.1.3 Connector Mechanical Performance

Table 4-12 shows the mechanical performance requirements for a DP external connector.

Table 4-12: Connector Mechanical Performance

Item	Test Condition	Requirement	
Vibration	Amplitude: 1.52mm P-P or 147m/s^2 {15G} Sweep time: 50-2000-50Hz in 20 minutes. Duration: 12 times in each of X, Y, Z axes (Total of 36 times) Electrical load: DC 100mA current must be conducted during the test. (ANSI/EIA-364-28 Condition III, Method 5A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
		Discontinuity	1us maximum
Durability	Measure contact and shell resistance after the following. Automatic cycling: 10,000 cycles at 100 ±50 cycles/hr. (ANSI/EIA-364-09)	Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Insertion/ Withdrawal Force (no latches)	Insertion and withdrawal speed: 25mm/minute. (ANSI/EIA-364-13)	Withdrawal force	9.8N {1.0kgf} minimum 39.2N {4.0kgf} maximum
		Insertion force	44.1N {4.5kgf} maximum
Latch Strength	Mate connectors, apply axial pull-out force at a rate of 13mm / minute until the latch is disengaged or damaged. (ANSI/EIA-364-98)	Appearance	No damage on either part of connector
		Pull force	49.0N {5.0kgf} minimum
Cable Flex	100 cycles in each of 2 planes. Dimension: X = 3.7 x Cable Diameter. (ANSI/EIA-364-41, Condition I)	Discontinuity	1us maximum
		Dielectric Withstanding Voltage and Insulation Resistance.	Conform to item of dielectric withstanding voltage and insulation resistance

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4.2.1.4 Connector Electrical Performance

Table 4-13 shows the electrical performance requirements for a DP external connector.

Table 4-13: Connector Electrical Performance

Item	Test Condition	Requirement
Low Level Contact Resistance	Mated connectors Contact: measured by dry circuit, 20mV maximum, and 10mA. Shell: measured by open circuit, 5V maximum, 100mA. (ANSI/EIA-364-23)	Contact: Change from initial value = 30mΩ maximum Shell: Change from initial value = 50mΩ maximum
Dielectric Strength	Unmated connectors, apply 500V RMS between adjacent terminal and ground. (ANSI/EIA 364-20, Method 301) Mated connector, apply 300V RMS between adjacent terminal and ground.	No Breakdown
Insulation Resistance	Unmated connectors, apply 500V DC between adjacent terminal and ground. (ANSI/EIA 364-21, Method 302)	Unmated: 100MΩ minimum
	Mated connectors, apply 150V DC between adjacent terminal and ground.	Mated: 10MΩ minimum
Contact Current Rating	55°C, maximum ambient 85°C, maximum temperature change (ANSI/EIA-364-70, TP-70)	0.5A minimum
Applied Voltage Rating	40V RMS continuous maximum, on any signal pin with respect to the shield.	No Breakdown
Electrostatic Discharge	Test unmated connectors from 1 to 8kV, in 1kV steps, using 8mm ball probe. (IEC61000-4-2)	No evidence of discharge to contacts at 8kV

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4.2.1.5 Connector Environment Performance

Table 4-14 shows the environment performance requirements for a DP external connector.

Table 4-14: Connector Environment Performance

Item	Test Condition	Requirement	
Thermal Shock	10 cycles of: • -55°C for 30 minutes • +85°C for 30 minutes (ANSI/EIA-364-32, Condition I)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Humidity	A) Mate connectors together and perform the test as follows: • Temperature: +25 to +85°C • Relative Humidity: 80 to 95% • Duration: Four cycles (96 hours) Upon completion of the test, specimens must be conditioned at ambient room conditions for 24 hours, after which the specified measurements must be performed. (ANSI/EIA-364-31)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
	B) Unmate connectors and perform the test as follows: • Temperature: +25 to +85°C • Relative Humidity: 80 to 95% • Duration: Four cycles (96 hours) Upon completion of the test, specimens must be conditioned at ambient room conditions for 24 hours, after which the specified measurements must be performed. (ANSI/EIA-364-31)	Appearance	No Damage
		Dielectric Withstanding Voltage and Insulation Resistance	Conform to item of Dielectric Withstanding Voltage and Insulation Resistance
Thermal Aging	Mate connectors and expose to (+105 ±2)°C for 250 hours. Upon completion of the exposure period, the test specimens must be conditioned at ambient room conditions for one to two hours after which the specified measurements must be performed. (ANSI/EIA-364-17, Condition 4, Method A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum

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4.2.1.6 Connector Performance Test Sequence

To evaluate the connector performance, the test sequence must follow test groups 1, 2, 3, and 7 in the ANSI/EIA Standard (EIA-364-1000.01).

4.2.1.7 Connector Drawings

Figure 4-25 shows the DP external connector. All dimensions are in mm.

Figure 4-25: DisplayPort External Connector Drawings

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4.2.1.8 Cable Connector Drawings

Figure 4-26 shows the DP external cable-connector assembly.

Recommendations for plug connector construction:

- Locate the thumb button on the opposite side to the interface chamfer corner.
- Provide the thumb button on the plug's top cover whether latches are fitted or not. This will provide the user with a good indicator of plug orientation.
- A plug without latches may have an alternate feature providing the same orientation indicator as the thumb button of the standard plug.

Figure 4-26: DisplayPort External Cable-Connector Assembly Drawings

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Figure 4-27 shows the recommended orientations of the external connector.

Figure 4-27: Recommended Orientation of External Connector

4.2.1.9 Plug Overmold Dimensions for Non-Latch Plug Connector

For non-latching plug connectors, the following overmold dimension parameters in Figure 4-28 must be met.

X: max 10mm from connector centerline
Z1: max 5mm from connector centerline
Z2: max 5mm from connector centerline for Y from overmold face
Y: X and Z2 apply for 25mm from overmold face or depth of plug (if less);
Designs intended for use on portable systems are encouraged to use smaller dimensions for Z1 and Z2 wherever practical

Figure 4-28: Plug Overmold Dimensions for Non-Latch Plug Connector

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4.2.1.10 Plug Connector and Board Connector Fully-Mated Condition

Figure 4-29 shows the fully mated condition of the plug and board connectors.

Figure 4-29: Fully Mated Condition for DisplayPort External Connectors

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4.2.1.11 Recommended PCB Layout

Figure 4-30 shows the DP external cable-connector assembly.

Figure 4-30: Recommended PCB Layout for DP External Connector

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4.2.1.12 Reference Design for Four DisplayPort External Connectors on a PCI Card

Figure 4-31 is a reference application design for four external connectors on a standard PCI card. Figure 4-32 shows the panel cut-out reference dimensions.

Figure 4-31: Reference Design for Four DP External Connectors on a PCI Card

Figure 4-32: Panel Cut Out Reference Dimensions

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4.2.2 Mini DisplayPort External Connector

The mDP connector is intended for use as an external connector on Source devices where a small form factor connector is advantageous.

4.2.2.1 Mini DisplayPort Connector Pin Assignment

Table 4-15 shows the pin assignments of the mDP external connector on a DFP on an upstream device.

Table 4-15: DFP mDP Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	**Signal Type**	**Pin Name**	**Pin Number**	**Signal Type**	**Pin Name**
1	GND	**GND**	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG[a]	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG[a]	CONFIG2
7	GND	**GND**	8	GND	**GND**
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	**GND**	14	GND	**GND**
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	**GND**	20	PWR Out[b]	DP_PWR

a. Pins 4 and 6 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low-impedance ground path from these pins.

b. Pin 20, PWR Out, must provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.

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It is recommended that downstream devices should use the full-size DP connector on their UFPs. However, if a downstream device implements the mDP connector on a UFP, then it must use the pinout specified in Table 4-16.

Table 4-16: UFP mDP Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	**Signal Type**	**Pin Name**	**Pin Number**	**Signal Type**	**Pin Name**
1	GND	**GND**	2	Out	Hot Plug Detect
3	In	ML_Lane 3 (n)	4	CONFIG[a]	CONFIG1
5	In	ML_Lane 3 (p)	6	CONFIG[a]	CONFIG2
7	GND	**GND**	8	GND	**GND**
9	In	ML_Lane 2 (n)	10	In	ML_Lane 0 (n)
11	In	ML_Lane 2 (p)	12	In	ML_Lane 0 (p)
13	GND	**GND**	14	GND	**GND**
15	In	ML_Lane 1 (n)	16	I/O	AUX_CH (p)
17	In	ML_Lane 1 (p)	18	I/O	AUX_CH (n)
19	GND	**GND**	20	PWR Out[b]	DP_PWR

a. *Pins 4 and 6 must be connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low-impedance ground path from these pins.*
b. *Pin 20, PWR Out, must provide +3.3V ±10% with a maximum current of 500mA and minimum power capability of 1.5W.*

A cable assembly may be constructed with an mDP plug at both ends, or an mDP plug at one end and a full-size DP plug at the other end, or a full-size DP plug at both ends. The standard external cable connector assembly must not have a wire on pin 20, DP_PWR.

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Figure 4-33 shows wiring of an external cable connector assembly when an mDP plug is used at both ends.

mDP DFP Connector			mDP-to-mDP Cable Assembly			mDP UFP Connector		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Plug Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	**GND**	1	1	↔	8	8	**GND**	GND
Out	ML_Lane 0 (p)	3	3	↔	12	12	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	5	5	↔	10	10	ML_Lane 0 (n)	In
GND	**GND**	7	7	↔	13	13	**GND**	GND
Out	ML_Lane 1 (p)	9	9	↔	17	17	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	11	11	↔	15	15	ML_Lane 1 (n)	In
GND	**GND**	13	13	↔	7	7	**GND**	GND
Out	ML_Lane 2 (p)	15	15	↔	11	11	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	17	17	↔	9	9	ML_Lane 2 (n)	In
GND	**GND**	19	19	↔	19	19	**GND**	GND
In	Hot Plug Detect	2	2	↔	2	2	Hot Plug Detect	Out
CFG	CONFIG1	4	4	↔	4	4	CONFIG1	CFG
CFG	CONFIG2	6	6	↔	6	6	CONFIG2	CFG
GND	**GND**	8	8	↔	1	1	**GND**	GND
Out	ML_Lane 3 (p)	10	10	↔	5	5	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	↔	3	3	ML_Lane 3 (n)	In
GND	**GND**	14	14	↔	14	14	**GND**	GND
I/O	AUX_CH (p)	16	16	↔	16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	18	18	↔	18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 4-33: mDP Cable Connector Assembly Wiring

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Figure 4-34 and Figure 4-35 show the wiring of an external cable connector assembly when an mDP plug is used at one end and a full-size DP plug is used at the other end.

mDP DFP Connector			mDP-to-DP Cable Assembly			DP UFP Connector		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Plug Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	**GND**	1	1	↔	11	11	**GND**	GND
Out	ML_Lane 0 (p)	3	3	↔	12	12	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	5	5	↔	10	10	ML_Lane 0 (n)	In
GND	GND	7	7	↔	8	8	**GND**	GND
Out	ML_Lane 1 (p)	9	9	↔	9	9	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	11	11	↔	7	7	ML_Lane 1 (n)	In
GND	**GND**	13	13	↔	5	5	**GND**	GND
Out	ML_Lane 2 (p)	15	15	↔	6	6	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	17	17	↔	4	4	ML_Lane 2 (n)	In
GND	GND	19	19	↔	19	19	**GND**	GND
In	Hot Plug Detect	2	2	↔	18	18	Hot Plug Detect	Out
CFG	CONFIG1	4	4	↔	13	13	CONFIG1	CFG
CFG	CONFIG2	6	6	↔	14	14	CONFIG2	CFG
GND	**GND**	8	8	↔	2	2	**GND**	GND
Out	ML_Lane 3 (p)	10	10	↔	3	3	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	↔	1	1	ML_Lane 3 (n)	In
GND	**GND**	14	14	↔	16	16	**GND**	GND
I/O	AUX_CH (p)	16	16	↔	15	15	AUX_CH (p)	I/O
I/O	AUX_CH (n)	18	18	↔	17	17	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 4-34: mDP-to-DP Cable Connector Assembly Wiring

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DP DFP Connector			DP-to-Mini DP Cable Assembly			mDP UFP Connector		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Plug Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	**GND**	2	2	↔	8	8	**GND**	GND
Out	ML_Lane 0 (p)	1	1	↔	12	12	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	3	3	↔	10	10	ML_Lane 0 (n)	In
GND	**GND**	5	5	↔	13	13	**GND**	GND
Out	ML_Lane 1 (p)	4	4	↔	17	17	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	6	6	↔	15	15	ML_Lane 1 (n)	In
GND	**GND**	8	8	↔	7	7	**GND**	GND
Out	ML_Lane 2 (p)	7	7	↔	11	11	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	9	9	↔	9	9	ML_Lane 2 (n)	In
GND	**GND**	19	19	↔	19	19	**GND**	GND
In	Hot Plug Detect	18	18	↔	2	2	Hot Plug Detect	Out
CFG	CONFIG1	13	13	↔	4	4	CONFIG1	CFG
CFG	CONFIG2	14	14	↔	6	6	CONFIG2	CFG
GND	**GND**	11	11	↔	1	1	**GND**	GND
Out	ML_Lane 3 (p)	10	10	↔	5	5	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	↔	3	3	ML_Lane 3 (n)	In
GND	**GND**	16	16	↔	14	14	**GND**	GND
I/O	AUX_CH (p)	15	15	↔	16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	17	17	↔	18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 4-35: DP-to-mDP Cable Connector Assembly Wiring

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A resizing adaptor may be constructed with an mDP plug at one end and a full-size DP connector at the other end. Such an adaptor must carry all 20 signals (including DP_PWR) and must make the signal connections so that the mDP plug adapts to a full-size DP connector. Figure 4-36 shows the wiring of a passive adaptor with an mDP plug at one end and a full-size DP connector at the other end.

mDP DFP Connector			mDP-to-DP Adaptor			DP Cable Plug		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Connector Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	GND	1	1	↔	2	2	GND	GND
Out	ML_Lane 0 (p)	3	3	↔	1	1	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	5	5	↔	3	3	ML_Lane 0 (n)	In
GND	GND	7	7	↔	5	5	GND	GND
Out	ML_Lane 1 (p)	9	9	↔	4	4	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	11	11	↔	6	6	ML_Lane 1 (n)	In
GND	GND	13	13	↔	8	8	GND	GND
Out	ML_Lane 2 (p)	15	15	↔	7	7	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	17	17	↔	9	9	ML_Lane 2 (n)	In
GND	GND	19	19	↔	19	19	GND	GND
In	Hot Plug Detect	2	2	↔	18	18	Hot Plug Detect	Out
CFG	CONFIG1	4	4	↔	13	13	CONFIG1	CFG
CFG	CONFIG2	6	6	↔	14	14	CONFIG2	CFG
GND	GND	8	8	↔	11	11	GND	GND
Out	ML_Lane 3 (p)	10	10	↔	10	10	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	↔	12	12	ML_Lane 3 (n)	In
GND	GND	14	14	↔	16	16	GND	GND
I/O	AUX_CH (p)	16	16	↔	15	15	AUX_CH (p)	I/O
I/O	AUX_CH (n)	18	18	↔	17	17	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	↔	20	20	DP_PWR	PWR Out

Figure 4-36: mDP-to-DP Adaptor Wiring

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A resizing adaptor may be constructed with a DP plug at one end and an mDP connector at the other end. Such an adaptor must carry all 20 signals (including DP_PWR) and must make the signal connections so that the full-size DP plug adapts to an mDP connector. Figure 4-37 shows wiring of a passive adaptor with a DP plug at one end and an mDP connector at the other end.

DP DFP Connector			DP-to-mDP Cable Adaptor			mDP Cable Plug		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Connector Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	GND	2	2	←	1	1	GND	GND
Out	ML_Lane 0 (p)	1	1	←	3	3	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	3	3	←	5	5	ML_Lane 0 (n)	In
GND	GND	5	5	←	7	7	GND	GND
Out	ML_Lane 1 (p)	4	4	←	9	9	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	6	6	←	11	11	ML_Lane 1 (n)	In
GND	GND	8	8	←	13	13	GND	GND
Out	ML_Lane 2 (p)	7	7	←	15	15	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	9	9	←	17	17	ML_Lane 2 (n)	In
GND	GND	19	19	←	19	19	GND	GND
In	Hot Plug Detect	18	18	←	2	2	Hot Plug Detect	Out
CFG	CONFIG1	13	13	←	4	4	CONFIG1	CFG
CFG	CONFIG2	14	14	←	6	6	CONFIG2	CFG
GND	GND	11	11	←	8	8	GND	GND
Out	ML_Lane 3 (p)	10	10	←	10	10	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	←	12	12	ML_Lane 3 (n)	In
GND	GND	16	16	←	14	14	GND	GND
I/O	AUX_CH (p)	15	15	←	16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	17	17	←	18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	←	20	20	DP_PWR	PWR Out

Figure 4-37: DP-to-mDP Adaptor Wiring

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An Extender may be constructed with an mDP plug at one end and an mDP connector at the other end. Such an adaptor must carry 20 signals and make the signal connections so that the mDP plug connects to an mDP connector. Figure 4-38 shows the wiring of a passive extender with an mDP plug at one end and an mDP connector at the other end.

mDP DFP Connector			mDP Plug-to-mDP Connector Cable Assembly			mDP Cable Plug		
Signal Type	**Pin Name**	**Pin**	**Plug Pin**	**Direction**	**Connector Pin**	**Pin**	**Pin Name**	**Signal Type**
GND	GND	1	1	↔	1	1	GND	GND
Out	ML_Lane 0 (p)	3	3	↔	3	3	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	5	5	↔	5	5	ML_Lane 0 (n)	In
GND	GND	7	7	↔	7	7	GND	GND
Out	ML_Lane 1 (p)	9	9	↔	9	9	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	11	11	↔	11	11	ML_Lane 1 (n)	In
GND	GND	13	13	↔	13	13	GND	GND
Out	ML_Lane 2 (p)	15	15	↔	15	15	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	17	17	↔	17	17	ML_Lane 2 (n)	In
GND	GND	19	19	↔	19	19	GND	GND
In	Hot Plug Detect	2	2	↔	2	2	Hot Plug Detect	Out
CFG	CONFIG1	4	4	↔	4	4	CONFIG1	CFG
CFG	CONFIG2	6	6	↔	6	6	CONFIG2	CFG
GND	GND	8	8	↔	8	8	GND	GND
Out	ML_Lane 3 (p)	10	10	↔	10	10	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	↔	12	12	ML_Lane 3 (n)	In
GND	GND	14	14	↔	14	14	GND	GND
I/O	AUX_CH (p)	16	16	↔	16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	18	18	↔	18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	↔	20	20	DP_PWR	PWR Out

Figure 4-38: mDP Cable Extender Wiring

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4.2.2.2 Mini DisplayPort Connector Mechanical Performance Requirements

Table 4-17 shows the mechanical performance requirements for an mDP connector.

Table 4-17: mDP Connector Mechanical Performance Requirements

Item	Test Condition	Requirement	
Vibration	Amplitude: 1.52mm P-P or 147m/s^2 {15G} Sweep time: 50-2000-50Hz in 20 minutes. Duration: 12 times in each of X, Y, Z axes (Total of 36 times). Electrical load: DC 100mA current must be conducted during the test. (ANSI/EIA-364-28 Condition III Method 5A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
		Discontinuity	1us maximum
Durability	Measure contact and shell resistance after the following. Automatic cycling: 10,000 cycles at 100 ± 50 cycles per hour (ANSI/EIA-364-09)	Contact Resistance	**Contact:** Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Insertion/ Withdrawal Force	Insertion and withdrawal speed: 25mm / minute. (ANSI/EIA-364-13)	Withdrawal force	9.8N {1.0kgf} minimum 39.2N {4.0kgf} maximum
		Insertion force	44.1N {4.5kgf} maximum
Cable Flex	100 cycles in each of 2 planes. Dimension: X = 3.7 x Cable Diameter. (ANSI/EIA-364-41, Condition I)	Discontinuity	1us maximum
		Dielectric Withstanding Voltage and Insulation Resistance.	Conform to item of dielectric withstanding voltage and insulation resistance

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4.2.2.3 Mini DisplayPort Connector Electrical Performance Requirements

Table 4-18 shows the electrical performance requirements for an mDP connector.

Table 4-18: mDP Connector Electrical Performance Requirements

Item	Test Condition	Requirement
Low-Level Contact Resistance	Mated connectors. Contact: Measured by dry circuit, 20mV maximum, and 10mA. Shell: Measured by open circuit, 5V maximum, 100mA. (ANSI/EIA-364-23)	Contact: Change from initial value = 30mΩ maximum Shell: Change from initial value = 50mΩ maximum
Dielectric Strength	Unmated connectors, apply 500V RMS between adjacent terminal and ground. (ANSI/EIA 364-20, Method 301) Mated connector, apply 300V RMS between adjacent terminal and ground.	No Breakdown
Insulation Resistance	Unmated connectors, apply 500V DC between adjacent terminal and ground. (ANSI/EIA 364-21, Method 302)	Unmated: 100MΩ minimum
	Mated connectors, apply 150V DC between adjacent terminal and ground.	Mated: 10MΩ minimum
Contact Current Rating	55°C, maximum ambient 85°C, maximum temperature change. (ANSI/EIA-364-70, TP-70)	0.5A minimum
Applied Voltage Rating	40V RMS continuous maximum, on any signal pin with respect to the shield.	No Breakdown
Electrostatic Discharge	Test signal and power pins of associated DP components (transmitter IC, receiver IC and associated I/O circuitry) to withstand JEDEC JESD22-A114-B Class 2 (2kV Human Body Model, 200V Machine Model) strikes.	After test, the DP component meets the part drawing requirements using parametric and functional testing.

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4.2.2.4 Mini DisplayPort Connector Environmental Performance Requirements

Table 4-19 shows the environmental performance requirements for an mDP connector.

Table 4-19: mDP Connector Environment Performance Requirements

Item	Test Condition	Requirement	
Thermal Shock	10 cycles of: • -55°C for 30 minutes • +85°C for 30 minutes (ANSI/EIA-364-32, Condition I)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
Humidity	A) Mate connectors together and perform the test as follows: Temperature: +25 to +85°C Relative Humidity: 80 to 95% Duration: Four cycles (96 hours) Upon completion of the test, specimens must be conditioned at ambient room conditions for 24 hours, after which the specified measurements must be performed. (ANSI/EIA-364-31)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum
	B) Unmate connectors and perform the test as follows: Temperature: +25 to +85°C Relative Humidity: 80 to 95% Duration: Four cycles (96 hours) Upon completion of the test, specimens must be conditioned at ambient room conditions for 24 hours, after which the specified measurements must be performed. (ANSI/EIA-364-31)	Appearance	No Damage
		Dielectric Withstanding Voltage and Insulation Resistance	Conform to item of Dielectric Withstanding Voltage and Insulation Resistance
Thermal Aging	Mate connectors and expose to (+105 ±2)°C for 250 hours. Upon completion of the exposure period, the test specimens must be conditioned at ambient room conditions for one to two hours after which the specified measurements must be performed. (ANSI/EIA-364-17, Condition 4, Method A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value = 30mΩ maximum Shell Part: Change from initial value = 50mΩ maximum

4.2.2.5 Connector Performance Test Sequence

To evaluate connector performance, the test sequence must follow test groups 1, 2, 3, and 7 in the ANSI/EIA Standard (EIA-364-1000.01).

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4.2.2.6 Mini DisplayPort Cable-Connector (Plug) Dimensions

Figure 4-39 and Figure 4-40 show the mDP plug dimensions, including maximum external dimensions for the overmold. The external shape of the overmold cross-section is shown for illustration purposes only and is not part of this Standard. A plug must meet all dimensions and tolerances shown.

All dimensions are in mm. Except where otherwise specified, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

Figure 4-39: mDP Cable-Connector Dimensions – 1

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Figure 4-40: mDP Cable-Connector Dimensions – 2

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4.2.2.7 Mini DisplayPort Connector (Receptacle) Dimensions

Figure 4-41 and Figure 4-42 show the mDP connector dimensions. A connector must meet all dimensions and tolerances shown.

All dimensions are in mm. Except where otherwise specified, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

See also Section 4.2.2.8 for the required mating sequence, Section 4.2.2.9 for the required panel allowance, and Section 4.2.2.10 for an appropriate PCB layout.

Figure 4-41: mDP Connector Dimensions – 1

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Figure 4-42: mDP Connector Dimensions – 2

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4.2.2.8 Mini DisplayPort Contact Sequence

An mDP receptacle must be designed to ensure the correct mating sequence. Table 4-20 shows the legend for signal name/type mating level.

Table 4-20: Mating Sequence Level

Signal Type		Level
Connector Shell		First Mate[a]
DP_PWR	GND	Second Mate
Auxiliary (+) / (-) ML_Lane (i) (+) / (-)	Hot Plug Detect, CONFIG1, CONFIG2	Third Mate

a. EMC fingers on the shell may mate after all contacts have mated.

Figure 4-43 shows the mating levels of the fully mated mDP receptacle and plug. All dimensions are in mm. Except where otherwise specified, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

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Figure 4-43: Fully-Mated mDP Connector Showing Mating Levels

4.2.2.9 Mini DisplayPort Panel Allowances

The figure in the previous section shows the plug protrusion in the fully-mated condition of the plug and the board receptacles. The system design incorporating an mDP receptacle must be designed so that an mDP plug fully mates with the mDP receptacle with appropriate margin, but with sufficient control to prevent an incorrect contact sequence due to angled insertion. The receptacle design must provide an appropriate allowance for a panel, bezel or similar (when used) so that this requirement is met. To meet these requirements, the distance from datum E in the receptacle to the externally accessible mating interface on the device shall be at least 5.7mm and shall not exceed 8.0mm.

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4.2.2.10 Recommended PCB Mounting

The recommended mounting for the mDP connector to a PCB uses surface-mount contacts for the mating interface top row of pins and thru-hole contacts for the mating interface bottom row of pins. Figure 4-44 shows the mDP connector's PCB interface, i.e. the sizes and positions of the surface mount contacts, the thru-hole contacts and the locating lugs. The actual landing pad design to receive these contacts will be system-dependent.

All dimensions are in mm. Except where otherwise specified, tolerances are x.x ±0.2, x.xx ±0.10, x.xxx ±0.050, angles ±0.5°.

Figure 4-44: Recommended mDP Connector PCB Contacts and Mounting

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4.2.2.11 Reference Design for Four mDP Connectors on a Reduced Height PCI Card

Figure 4-45 and Figure 4-46 show a reference application design for four mDP connectors on a low-profile PCI/PCIe card.

Figure 4-45: Reference Design for Four mDP Connectors on a Reduced Height PCI Card – 1

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Figure 4-46: Reference Design for Four mDP Connectors on a Reduced Height PCI Card – 2

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4.2.3 Panel-side Internal Connector (Informative)

This section covers the specifications for DP panel-side internal connector for reference purposes.

The panel-side internal connector consist of a two-piece, 30-position, low-profile, cable-to-board, co-planar connector. One piece terminates the cable (Plug) and the other is attached to the PCB (Receptacle).

The connector supports up to four Main-Link lanes (Lanes 0, 1, 2, and 3). In an embedded connection, the cable connector assembly may support one, two, or four lanes, depending on the bandwidth requirement of the application.

For one lane and two lane Main-Link configurations, the stuffing rule must be:

- When only two lanes are needed, Lanes 0 and 1 must be populated, while Lanes 2 and 3 are unpopulated.
- When only one lane is needed, Lane 0 must be populated, while Lanes 1, 2, and 3 are unpopulated.

Only the panel TCON (timing controller) side of the connector is defined in this specification. While some cables may have the same connectors on both ends of the cable-connector assembly, others may have more pins for the Source device side (e.g., the side of graphics processor, LCD controller, etc.) for LCD backlight control, for instance.

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4.2.3.1 Panel-side Internal Connector Pin Assignment

Table 4-21 shows the pin assignment of the DP panel-side internal connector. Pin assignment of those pins other than the DP Main-Link and AUX CH in Table 4-21 is for reference purpose only. For pin 1 location, see Figure 4-47.

Table 4-21: DisplayPort Panel-side Internal Connector Pin Assignment

Pin #	Pin Name	Pin Definition
Frame		Outer shell
1	RESERVED	
2	LCDVCC	Power to LCD panel
3	LCDVCC	
4	LCDVCC	
5	LCDVCC	
6	GND	Power Return (Ground)
7	GND	
8	GND	
9	GND	
10	HPD	Hot Plug Detect Optional
11	RESERVED	
12	RESERVED	
13	H_GND	High Speed (Main-Link) Ground
14	ML_Lane 3(n)	‘Complement’ Signal-Main-Link
15	ML_Lane 3(p)	‘True’ Signal-Main-Link
16	H_GND	High Speed (Main-Link) Ground
17	ML_Lane 2(n)	‘Complement’ Signal-Main-Link
18	ML_Lane 2(p)	‘True’ Signal-Main-Link
19	H_GND	High Speed (Main-Link) Ground
20	ML_Lane 1(n)	‘Complement’ Signal-Main-Link
21	ML_Lane 1(p)	‘True’ Signal-Main-Link
22	H_GND	High Speed (Main-Link) Ground
23	ML_Lane 0(n)	‘Complement’ Signal-Main-Link
24	ML_Lane 0(p)	‘True’ Signal-Main-Link
25	H_GND	High Speed (Main-Link) Ground
26	AUX_CH (p)	‘True’ Signal – Auxiliary channel
27	AUX_CH (n)	‘Complement’ Signal – Auxiliary channel
28	H_GND	High Speed (Main-Link) Ground
29	AUX_PWR	+3.3 Trickle PWR
30	RESERVED	
Frame		Outer shell

Figure 4-47: Panel-side Internal PCB Mount Receptacle Connector with Pin 1 Shown

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4.2.3.2 Panel-side Internal Receptacle Connector

Figure 4-48 through Figure 4-50 show the DP panel-side internal PCB receptacle connector and the recommended footprint layout, respectively.

Note: *This dimension shows ground contact.*

Figure 4-48: Panel-side Internal PCB Mount Receptacle Connector (in mm) – 1

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Figure 4-49: Panel-side Internal PCB Mount Receptacle Connector (in mm) – 2

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Figure 4-50: PCB Mount Connector Recommended Footprint Layout (in mm)

4.2.3.3 Panel-side Internal Plug Connector

Figure 4-51 shows the DP panel-side internal cable plug connector.

Note: *This is ground area.*

Figure 4-51: Panel-side Internal Cable Plug Connector (in mm)

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4.2.3.4 Panel-side Internal Plug Connector – Contact and Mechanical Guide Details

Figure 4-52 and Figure 4-53 show the contact and mechanical guide details.

Note 1: *This area is ground area.*

Note 2: *This area is signal contact area.*

Figure 4-52: Contact and Mechanical Guide Details (in mm)

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Figure 4-53: Mating Condition (Reference) of Panel Side Internal Cable Connector (in mm)

4.2.3.5 Panel Side Connector Mechanical Requirements

Table 4-22 shows the mechanical requirements of the panel-side connector.

Table 4-22: Panel-side Connector Mechanical Requirements

Item	Test Condition	Requirement
Vibration (random)	Frequency: 10 to 2000Hz Acceleration Velocity: 30.38m/s^2 (3.1G) RMS. Action direction: In each of three mutually perpendicular planes. Duration: 15 minutes each sample. (EIA-364-28, Test condition VII, Test condition D)	100mA applied with no electrical discontinuity greater than 1us.
Physical shock	Sample should be mounted on the test jig as mounted on the PCB. Acceleration velocity: 490m/s^2 or 50G. Waveform: half sine Duration: 11ms. Number of drops: Three drops each to normal and reversed directions of X,Y, and Z axes. Total 18 drops. (EIA-364-27B, Method A)	No electrical discontinuity greater than 1us must occur.
Durability (mating and unmating)	Number of cycles: 50 Automatic Cycling: 100 ±50 cycles per hour (EIA-364-09C)	R = 40mΩ maximum (initially) ΔR = 20mΩ maximum (final)
Durability (preconditioning)	Number of cycles: 20 (EIA-364-09C)	No physical damage.
Connector insertion force	Operation speed: 12.5mm/minute Measure the force required to mate the connector including the latching mechanism. (EIA-364-13B)	35N maximum per connector (30 pin).
Connector withdrawal force	Operation speed: 12.5mm/minute Measure the force required to unmate the connector excluding the latching mechanism. (EIA-364-13B)	5N minimum to 25N maximum per connector (30 pin).

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4.2.3.6 Panel Side Connector Electrical Requirements

Table 4-23 shows the electrical requirements of the panel-side connector.

Table 4-23: Panel-side Connector Electrical Requirements

Item	Test Condition	Requirement
Dielectric withstanding voltage	0.25kV AC for 1 minute. Test between adjacent circuits of unmated connectors. (EIA-364-20C)	No creeping discharge or flashover must occur. Current leakage: 0.5mA maximum
Insulation resistance	Impressed voltage: 100V DC Test between adjacent circuits of unmated connectors for 2 minutes. (EIA-364-21C)	100MΩ minimum (initial) 50MΩ minimum (final)
Low-level contact resistance	Subject mated contacts assembled in housing measured by dry circuit 20mV maximum open circuit at 10mA (EIA-364-23B)	R = 40mΩ maximum (initial) ΔR = 40mΩ maximum (final)
Temperature rise	Measure temperature rise by energizing current. (EIA-364-70A, Method 1)	30ºC maximum ΔT over ambient at maximum rated current (0.50A) per contact.

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4.2.3.7 Panel Side Connector Environmental Requirements

Table 4-24 shows the environmental requirements of the panel-side connector.

Table 4-24: Panel-side Connector Environmental Requirements

Item	Test Condition	Requirement

Humidity and Temperature Cycling	Cycle Mated connector:
	25 to 65ºC and 50 to 80% relative humidity 10 cycles and 10 cycles of cold shock at -10ºC.
	(EIA-364-31B, Method 4)
		Mating Condition:
		• Contact Resistance:
		  • R = 80mΩ maximum (final)
		Unmating condition:
		• Insulation resistance:
		  • R = 50MΩ maximum (final)
		  • ΔR = 50MΩ maximum

Thermal Shock	Cycle mated connector from -55ºC for 30 minutes to 85ºC for 30 minutes, repeat for 10 cycles. (EIA-364-32)	R = 40mΩ minimum (initial) ΔR = 40mΩ maximum (final)
Temperature Life (heat age)	Submit mated connector to 105ºC for 168 hours. (EIA-364-17B)	R = 40mΩ minimum (initial) ΔR = 40mΩ maximum (final)
Temperature Life (preconditioning)	Submit mated connector to 105ºC for 92 hours. (EIA-364-17B)	No physical damage

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5 Source/Sink/Branch Device Policy Requirements for Interoperability

This section describes the requirements for DisplayPort devices and cable-connector assemblies to maximize the interoperability between Source and Sink devices over an open, box-to-box DP link.

For embedded connection, it is the responsibility of the system integrator to ensure that the DP link meets the requirement of a given application. A closed, box-to-box connection between a captive Source device and Sink device pair (designed to only work with each other) is regarded as an embedded connection. The Source and Sink device pair must discover each other by checking the OUI and other device-specific values at the Source Device-specific field (DPCD Addresses 00300h through 003FFh; see Table 2-158) and Sink Device-specific field (DPCD Addresses 00400h through 004FFh; see Table 2-159), or Branch Device-specific field (DPCD Addresses 00500h through 005FFh; see Table 2-160) via AUX transactions.

The DisplayPort Logo is available only for devices that meet the requirements for the open, box-to-box DP connection. These products must be certified and a license agreement with VESA completed before this logo may be used on products/packaging.

5.1 Source Device in SST Mode

This section describes the Source device requirements for box-to-box connections operating in SST mode.

For embedded connections, it is the responsibility of the system integrator to ensure that the Source device meets the requirements of a given application.

5.1.1 Stream Source Requirement

This sub-section describes the requirements for the Stream Source in terms of video colorimetry, video timings, and audio formats.

The Stream Source is required to support parsing of EDID v1.4 and, when feasible, strongly recommended to support parsing of the Sink device's extension blocks (both CEA Extension Block DisplayID Extension Block).

5.1.1.1 Video Colorimetry

DP Source devices must support sourcing of both RGB and YCbCr colorimetry formats shown in Table 5-1. A Source device must indicate the colorimetry format (including dynamic range) of the transmitted stream in the DisplayPort Main Stream Attributes as described in Section 2.2.4.

In determining the colorimetry format, the Source device must check the capability of the Sink device via an EDID read. When the Sink device capability is unknown, for example due to the corruption of EDID, the Source device must fall back to 18bpp RGB, with full dynamic range (called "VESA range" as described in Section 5.1.1.1.1).

When a Source device is transmitting an RGB stream with a video timing format called out in *CEA-861-F*, *Section 5* (except 640x480p) as using CEA range RGB, it should use CEA range RGB.

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When a Source device is transmitting 640x480p 24-bit RGB, it will always use the full dynamic range.

Table 5-1: DisplayPort Colorimetry Format Support

Colorimetry Format	Bit-depth per Pixel (bpp)	Bit-depth per Component (bpc)	Dynamic Range[a]	Mandatory vs. Optional
RGB	18	6	"VESA range" only	Mandatory Used in "fall-back" modes when Sink device capability is unknown
	24	8	"VESA range" or "CEA range"	Mandatory
	30	10		Optional
	36	12		
	48	16		
Y-only	8	8	"VESA range"	Optional
	10	10		
	12	12		
	16	16		
YCbCr 4:2:0	12	8	"CEA range" ("VESA range" is also allowed if a DP Sink supports pixel encoding and colorimetry format indication by way of VSC SDP and declares support of the VESA range YCbCr by way of EDID)	Optional
	15	10		
	18	12		
	24	16		
YCbCr 4:2:2	16	8		Mandatory if YCbCr is supported on any other display interface
	20	10		Optional
	24	12		
	32	16		
YCbCr 4:4:4	24	8		Mandatory if YCbCr is supported on any other display interface
	30	10		Optional
	36	12		
	48	16		
RAW	6	6	–	Optional
	7	7		
	8	8		
	10	10		
	12	12		
	14	14		
	16	16		

a. See the following sub-sections for definitions of VESA and CEA ranges.

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5.1.1.1.1 RGB Colorimetry

All DP Source devices must support RGB colorimetry with pixel depths of 18 and 24bpp. Support for 30, 36, and 48bpp RGB is optional.

"VESA range" and "CEA range" are defined as follows:

- VESA range must have:
  - Nominal zero intensity level at code value 0
  - Maximum intensity level at maximum code value allowed for bit depth (i.e., 63 for 18bpp RGB, 255 for 24bpp RGB, 1023 for 30bpp RGB, 4095 for 36bpp RGB, and 65535 for 48bpp RGB)
- CEA range must have:
  - Nominal zero intensity level at 16 for 24bpp, 64 for 30bpp, 256 for 36bpp, and 4096 for 48bpp
  - Maximum intensity level at maximum code value allowed for bit depth, namely, 235 for 24bpp RGB, 940 for 30bpp RGB, 3760 for 36bpp RGB, and 60160 for 48bpp RGB

Note: *The RGB CEA range is defined for 24, 30, 36, 48bpp RGB only, not for 18bpp RGB.*

When a Source device is transmitting an RGB stream with a video timing format called out in *CEA-861-F*, the device may source RGB in VESA range.

It is the responsibility of the Sink device to limit the pixel value range as needed.

Note: *The Source device falls back to 18bpp, VESA range RGB when the sink capability is unknown.*

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5.1.1.1.2 YCbCr Colorimetry

Support for YCbCr colorimetry is required for DP Source devices that support YCbCr or YPbPr on any other display interface, except where the Source device would be required to convert RGB video to YCbCr to meet this requirement.

Source devices that support YCbCr must support at least 24bpp YCbCr 4:4:4 and 16bpp YCbCr 4:2:2 in both 601 (defined in ITU-R BT.601-5, Section 3.5, or EIA/CEA-770.2-C, Section 3.3) and 709 (defined by ITU-R BT.709-4 Part 1, Section 4, or EIA/CEA-770.3-C, Sections 5.4 to 5.7).

In addition to the required minimum above, the pixel depth may optionally be 30, 36, and 48bpp for YCbCr 4:4:4 and 20, 24, and 32bpp for YCbCr 4:2:2.

YCbCr dynamic range is recommended to be as defined in *CEA-861-F*, *Section 5* (CEA range):

- Y has nominal zero intensity level at 16 for 8 bits, 64 for 10 bits, 256 for 12 bits, and 4096 for 16 bits per component
- Y has nominal maximum intensity level at 235 for 8 bits, 940 for 10 bits, 3760 for 12 bits, and 60160 for 16 bits per component
- Cb and Cr have their zero levels at 128 for 8 bit, 512 for 10 bit, 2048 for 12 bits, and 32768 for 16 bits per component
- Cb and Cr have nominal ranges of 16 to 240 for 8 bits, 64 to 960 for 10 bits, 256 to 3840 for 12 bits, and 4096 to 61440 for 16 bits per component

However, a Source device may transmit all code values from zero to the maximum value. It is the responsibility of the Sink device to limit the pixel value range as needed.

5.1.1.1.3 Y-only Colorimetry

Support for Y-Only is optional on DisplayPort devices. If they support it, they must support pixel bit depths of 8, 10, 12, and 16bpp.

The purpose of this format is to reduce the amount of DP bandwidth by 1/3 over RGB to transmit grayscale video from Source to Sink. The main intended application for this format is for ultra high-resolution medical displays.

For colorimetry, in the medical market, it is common to use the “DICOM Part 14 Grayscale Display Function” to describe the mapping of values to luminance on the monitor. This standard defines a “perceptual linearized” standard, including a calibration of the monitor to ensure the standard is met. While this is the most common usage, it is not the only use. As such, the only required luminance mappings are VESA range.

5.1.1.2 Video Timing Format

In determining the video timing format, the stream Source of the Source device must check the capability of the Sink device via an EDID read after the Hot Plug Detect signal goes active. When the Sink device cannot handle the incoming stream, it must toggle the HPD signal to notify the Source device of this condition. Upon detecting a HPD pulse, the Source device must determine the Sink device status by reading the SINK_STATUS register (DPCD Address 00205h).

When the Sink device capability is unknown (e.g., due to corruption of an EDID), the Source device may fall back to a set of fall-back video timing formats of its choice (except for the Fail Safe mode). When none of the fall-back video timing formats is acceptable (as indicated by the Sink device via the SINK_STATUS register), the Source device must fall back to the Fail Safe mode, which is 640x480 at 60Hz (defined in *DMT v1 r13*).

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5.1.1.3 Audio Format

Audio support is optional for DP Source devices. The Source devices that support audio must support stereo (two channel) 16-bit per sample LPCM at one or more of 32, 44.1, or 48kHz.

It is optional for audio-capable Source devices to support other coding types, sample rates, sample sizes, and/or number of channels within the limits of the audio capability of the Sink device indicated in its EDID.

The Source device must check via EDID or the CEA Timing Extension to EDID which audio formats the Sink can support before sending any audio stream data.

The Source device is recommended to find out whether the Sink device is able to sink the audio stream by checking the SINK_STATUS register (DPCD Address 00205h) and take corrective action, as needed.

5.1.2 Source Device Link Configuration Requirement

A DP Source device must establish the Main-Link between its DPTX and DPRX through the Link Training sequence upon Hot Plug event detection, as described in Section 3.5.1.2.

After Link Training successfully completes (which means that the DPRX is synchronized to incoming Main-Link data) and before transport of a main video stream starts, the Source device must be sending the Idle Pattern consisting of the BS symbol sequence followed by the NoVideoStream_Flag bit in the VB-ID (bit 3) set to 1 every 2^{13} (or 8192) link symbols. Every 512th occurrence of the BS symbol sequence must be replaced by the corresponding scrambler reset (SR) symbol sequence.

The Source device must start sending the Idle Pattern after it has cleared the TRAINING_PATTERN_SET register (DPCD Address 00102h).

The Source device of a box-to-box DP connection must support the number of Main-Link lanes that provide for sufficient bandwidth, even at a reduced bit rate-per-lane.

For example, if a required application bandwidth is provided both with two lanes at a high bit rate and four lanes at a reduced bit rate, then the detachable Source device is required to support four lanes.

Note: *The Source device for an embedded connection is not required to follow this rule.*

Upon detecting a Hot Plug event, the Source Link Policy Maker must read the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155) of the Sink device and configure the link accordingly, using Link Training procedure as described in Section 2.9.4.3 and Section 3.5.1.2.

As for the handling of Link Training failure, see Section 3.5.1.2.1 and Section 3.5.1.2.2.

After the link is configured, the Source Link Policy Maker must check the link status whenever it detects an IRQ_HPD pulse. When it detects that the link has lost lock, the Source Link Policy Maker must re-train the link. A link can be re-trained for any reason. A Source device must be tolerant to the available bandwidth resulting from re-training being lower than the bandwidth resulting from prior Link Training, and this in turn might require a video mode set change.

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Upon detecting one of the conditions listed below, the Source device Link Policy Maker must re-read the Receiver Capability field and take corrective action.

- Low-going HPD pulse wider than 2ms (Hot Plug event HPD pulse)
- RX_CAP_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 0) is set
- Downstream device is a DP Branch device and its DOWNSTREAM_PORT_STATUS_CHANGED bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 6, respectively) are set

When a DP Source device is resuming the transmission (e.g., after waking from sleep), the Source device can skip the AUX transactions for the Link Training if both of the following conditions are met:

- The Source device has determined that the HPD signal has remained continuously asserted (apart from IRQ_HPD notifications) since the link was last in full operation.
- The Source device has read 1 in the NO_AUX_TRANSACTION_LINK_TRAINING bit in the MAX_DOWNSPREAD register (DPCD Address 00003h, bit 6) after initial Sink device detection.

If both of the conditions listed above are met, and if the Source device determines that the bandwidth to be used is the same as that used when the link was last in full operation, the Source device can transmit TPS1 for 500us minimum and one of TPS2, TPS3, or TPS4 (depending on what is supported by both the DPTX and DPRX) for 500us minimum, using the last known good Voltage Swing and Pre-emphasis settings before switching to normal operation without AUX transactions for Link Training. Regardless of whether the full Link Training is skipped, the DP Sink device must send an IRQ_HPD pulse over the HPD signal line when the device fails to synchronize to the incoming Main-Link stream.

A Source device increases the Main-Link lane count during normal operation, as follows:

1. Stops the transmission of symbols over the Main-Link lanes.
2. Writes the desired lane count to the LANE_COUNT_SET field in the LANE_COUNT_SET register (DPCD Address 00101h, bits 4:0).
3. Performs link training. Source may use the known-good drive current and pre-emphasis level setting to accelerate the link training sequence.
4. Once all the lanes are trained, starts the transmission of Idle Pattern or a stream.

A Source device decreases the Main-Link lane count during normal operation, as follows:

1. Switches the transmitted symbols to Idle Pattern on all active lanes.
2. Writes the desired lane count to the Link Configuration field via AUX CH.
3. Stops the transmission of the Idle Pattern over the lanes that are to be disabled.
4. Verifies that the DP receiver is symbol-locked and inter-lane aligned (unless it is 1-lane configuration).
5. Starts the transmission of a stream.

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5.1.2.1 Source Device Link Requirement when Other Interfaces are Supported

An objective of the DisplayPort Standard is to provide a high-performance display interface that meets end user expectations. End user expectations may be established by other non-DisplayPort video display interfaces that co-exist on a device. As such, for a Source device that provides standard connectors for VGA, DVI, HDMI, Thunderbolt, analog component, or composite video, any DisplayPort standard receptacles on the same Source must meet the requirements described below. The non-DisplayPort connectors enumerated above will be referred to collectively as "non-Native connectors" throughout this section. For a Source with non-Native connectors and multiple DisplayPort outputs, it is only required that each DisplayPort output meets these requirements when tested individually.

For a Source device providing non-Native connectors, the DisplayPort output(s) must support up to the maximum video display mode (determined as the maximum bandwidth product from supported pixel clock and color depth combinations) provided on the non-Native connector(s), up to maximum capability of the supported link rate in four-lane configuration. Support of RBR and HBR is required. Support of HBR2 and HBR3 is optional.

If audio is supported on a non-Native connector, the DisplayPort output of a Source device providing non-Native connectors must support audio.

If HDCP is supported on a non-Native connector, the DisplayPort output of a Source device providing non-Native connectors must support HDCP.

The Audio and HDCP requirements stated above also apply to DisplayPort outputs when operating in dual-mode (if supported), unless explicitly precluded by other governing standards or licenses.

5.1.3 Source Device Behavior on Stream Timing Change

5.1.3.1 Video Stream Timing Change

Before changing the timing of the main video stream, the Source device must transmit the "idle pattern" (BS symbol followed by the NoVideoStream_Flag and VerticalBlanking_Flag bits in the VB-ID (bits 3 and 0, respectively) both set to 1 every 2^{13} or 8192 LS_Clk cycles) until it is ready to insert the new Main Stream Attribute data during the vertical blanking period of the main video stream. At the very minimum, the Source device must repeat the idle pattern five times before inserting the new Main Stream Attribute.

For eDP connections, the number of inserted idle patterns may be fewer than five.

If the Source device chooses to stop the transmission of Main-Link Symbols during the video timing change, it is required to run Link Training before starting the transport of the new main video stream.

Note: *The Source device is allowed to continue transmitting Audio_Stream SDP framed by SS and SE symbols, even when it is no longer transmitting the main video stream. When the video stream is absent, the Source device must transmit Audio INFOFRAME and Audio_TimeStamp SDPs after every 512th BS symbol set after SR symbol.*

5.1.3.2 Audio Stream Format/Timing Change

As for audio format/timing change, the Source device must set and keep the AudioMute_Flag bit in the VB-ID (bit 4) to 1 until after the new Audio INFOFRAME and Audio_TimeStamp SDPs have been sent. Those SDPs may be sent as soon as the next frame boundary (when the main video stream is present) or after the next 512th BS symbol set (when the main video stream is absent).

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5.1.4 Source Device Behavior upon HPD Pulse Detection

The HPD signal notifies the Source device that one of the following events has occurred:

- **IRQ** – A downstream DP Sink device might generate an IRQ_HPD pulse to prompt the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read DPCD Addresses 00200h through 00205h or DPCD Addresses 02002h through 0200Fh
- **Unplug** – The Sink device is no longer connected to the Source device and the Source device may then disable its Main-Link as a power-saving measure
- **Plug/Re-plug –** The Sink device is now connected to the Source device, forcing the Source device to read the Receiver Capabilities and stream sink capability in EDID

Figure 5-1 illustrates the different events signaled via the HPD signal.

Figure 5-1: HPD Events

Note: *In the subsequent discussions the state of the Source device is assumed to be ON, as the Source device in the OFF state (e.g., powered off or blocked waiting for user input) will obviously not be capable (or required) to respond to a HPD signal status changes.*

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The Source device must respond to an IRQ_HPD pulse by starting to read the DPCD Addresses 00200h through 00205h or DPCD Addresses 02002h through 0200Fh, via AUX read transactions within 100ms of the rising edge of the HPD signal. The Source device must then perform the necessary corrective action based on the current Link/Sink status.

The Source device is not required to have an explicit response to Hot Unplug events. The Source may choose to enter a power saving mode where it disables its Main-Link after HPD has been de-asserted for longer than the HPD_TimeOut (2 ms).

Note: *False events may occur due to signal bounce upon cable-assembly unplugging. In this condition, AUX read operations will likely fail, and the HPD signal will eventually settle in a de-asserted state for an extended period of time, allowing accurate detection of the Hot Unplug event.*

The Source device must respond to Hot Plug event/Hot Re-plug event by first reading DPCD Link/ Sink Device Status registers at DPCD Addresses 00200h through 00205h or DPCD Addresses 02002h through 0200Fh. If the link is unstable or lost, the Source device then reads the DPCD Receiver Capabilities registers at DPCD Addresses 00000h through 0000Fh to ascertain the appropriate information to train the link. The Source device must then initiate Link Training.

There is no mandatory time constraint on the Source device's response to a Hot Plug event/Hot Re-plug event, but a Source device vendor may want to impose a voluntary constraint similar to that for IRQ_HPD pulse (e.g., 100ms) to ensure a good user experience via prompt discovery and configuration of newly connected devices.

5.1.5 Downstream Device DPRX Power Management by a Source Device

A Source device must write the value of 2h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) of a Sink device, via AUX CH to place the DPRX of a downstream device in a power-save mode. In a power-save mode, the DP Source device may disable Main-Link transmitter for power saving.

The Source device must write the value of 1h to the SET_POWER & SET_DP_PWR_VOLTAGE register of the downstream device, via AUX write transaction to switch the DPRX of the downstream device out of power-save mode. A DPRX of a downstream device in a power-save mode may not reply to this AUX request transaction. The DPRX of a downstream device in a power-save mode for an open, box-to-box connection is allowed to take up to 1ms till it is ready to reply to the AUX request transaction. Therefore, the Source device must retry until the 1ms wake-up timeout period of the Sink device expires.

Note: *For embedded connections, a Sink device may take up to 20ms from a power-save mode till it is ready to reply to AUX request transaction.*

Before restarting the Main-Link transmission, the Source device must verify that the Sink device replies to an AUX transaction. When restarting the Main-Link transmission, the Source device must initiate Link Training first.

The Source device may keep transmitting Idle Pattern over Main-Link even when there is no stream to transmit. The Source device may start the transmission of a stream without initiating Link Training. Therefore, the downstream device must keep the Main-Link receiver active as long as it is receiving either a stream or Idle Pattern and as long as it keeps the HPD signal asserted.

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5.1.6 Source Device Connected to a Branch Device

Upon detecting HPD signal assertion, the DisplayPort Source device must read the DFP_PRESENT bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 0) to find out whether the downstream device is a Sink device (bit 0 = 0) or Branch device (bit 0 = 1). If it is a Branch device, the Source device must read the following register bits, depending on the number of ports, to determine:

- Number of downstream-facing ports (DFPs) at the DFP_COUNT field in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bits 3:0)
- Type of DFP and Port types at the DFP_TYPE field in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bits 2:1)
- DFP capabilities at the Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh)

To determine whether the Source device is connected to the active protocol converter adaptor, the Source device must read the SINK_COUNT field in the SINK_COUNT register (DPCD Address 00200h, bits 7, 5:0). Upon detecting IRQ_HPD pulse, a Source device interfacing with an active protocol converter must check SINK_COUNT to see whether there is a change in the count.

The Source must generate timings that are consistent with the output timings of an Active Protocol Converter Adaptor. For example, HDCP for HDMI requires the minimum of 56 blanking pixel clock cycles during horizontal blanking period. It is a responsibility of a source device to generate a stream with sufficient blanking pixel clock cycles.

The Source must not transmit Frame Sequential 3D format unless the adaptor has set the FRAME_SEQ_TO_FRAME_PACK bit (Byte 3, bit 0 in the Detailed Capabilities Info register for the HDMI DFP type) to 1.

When the Source device is connected to an Active Protocol Converter Adaptor that advertises a DP++ DFP, if a Source attempts to transmit a resolution that requires a TMDS clock rate or color depth exceeds the advertised capabilities of the Branch device or 165MHz TMDS clock rate (whichever is less), then it should display a warning message to the user requesting confirmation of acceptability of the image and revert to a resolution that requires a TMDS clock rate or color depth that does not exceed the lesser of the advertised capabilities or 165MHz if no confirmation is received after a timeout.

When the Source device is connected to an Active Protocol Converter Adaptor that advertises a VGA DFP, Source devices are recommended to support full plug-and-play (PnP) experience, when possible, and revert to non-plug-and-play (non-PnP) experience with manual user intervention for other cases when the Sink device connectivity state cannot be identified.

Table 5-2 describes the recommended DP Source device behavior when connected to a Branch device.

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Table 5-2: Recommended DP Source Device Behavior when Connected to a Branch Device

HPD	Sink Count	Valid EDID Read?	Recommended Source Device Behavior
High	1 or 0 → 1	Yes	PnP experience, automatically drive the sink.
TBD	IRQ_HPD	***TBD***	Video format (video timing, pixel bit depth, colorimetry format) support based on the EDID, link and convertor capability reported in the DPCD. Automatically disable driving the Sink device on transition from 1 → 0 on IRQ_HPD.
High	1 or 0 → 1 on IRQ_HPD	No	Non-PnP experience. Allows a user to manually enable the port and drive video format up to the link and convertor capability reported in the DPCD. It is recommended that a DP Source device should not limit video support to only 640x480 for a DP-to-VGA convertor if EDID cannot be obtained. Support for higher video format is based on the DP Source device policy. Disabling of the converter's VGA output port requires manual user intervention.
High	0	No	Non-PnP experience, as described for the case above.
High	0	Yes	Non-PnP experience; however, when a user manually enables the converter's VGA output port, a DP Source device should drive the output based on the EDID, link and convertor capability reported in the DPCD.
Low	Don't Care	Don't Care	Active Protocol Convertor Adaptor is not discovered, and therefore, is not driven by a DP Source device.

The DP Source device should not transmit non-RGB color encoding, INFOFRAME, or audio-related SDPs unless one of the following conditions is true:

- DFP type is DisplayPort
- DFP type is HDMI
- DFP type is DP++ and the Source device detects that the DFP is connected to an HDMI level-shifting adaptor

5.1.7 Source Device DSC Bitstream Transport and FEC Policy

New to *DP v1.4*.

A DSC bitstream sourcing-capable DP Source device shall have FEC encoding capability. (See Section 3.5.1.5.) Before enabling DSC bitstream transmission, the DP Source device operating in SST mode shall check that the plugged DPRX is capable of both DSC decompression and FEC decoding by reading from DPCD registers.

To enable FEC encoding/decoding, the DP Source device shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training.

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The DP Source device that is enabling FEC encoding shall take into account the 2.3% transport overhead of FEC when it calculates the maximum transportable AV stream bandwidth over an FEC-enabled DP link. As is the case without FEC encoding/decoding, the DP Source device shall fill each TU with valid pixel data symbols at the pixel rate.

5.1.8 MSA Horizontal Blanking Expansion Operation Support

New to *DP v1.4*.

A DP Source discovers whether a plugged DPRX supports MSA Horizontal Blanking Expansion operation by reading the RECEIVE_PORT0_CAP_1 and RECEIVE_PORT0_CAP_0 registers (DPCD Address(es) 00009h and 00008h, respectively).

When plugged to a DPRX capable of Horizontal Blanking Expansion operation, a DP Source device may prompt the DPRX to enable Horizontal Blanking Expansion operation by programming the MSA SDP HTotal[15:0], HStart[15:0], HSyncPolarity[0] (HSP), and HSyncWidth[14:0] (HSW) values after the expansion, instead of those of the DP Source device video as described in Section 2.2.4.1.2. In this operation, the DP Source device shall program the Mvid and Nvid values corresponding to the regenerated pixel clock frequency after the expansion.

When plugged to a DPRX capable of Horizontal Blanking Expansion operation, a DP Source device may prompt the DPRX to enable Horizontal Blanking Expansion operation by programming the OUTPUT_HTOTAL, OUTPUT_HSTART, and OUTPUT_HSP_HSW registers (DPCD Addresses 03054h through 03059h, respectively) prior to the video transmission that needs to be expanded.

5.2 Sink Device in SST Mode

This section describes the requirements for the SST-only mode Sink device for a box-to-box connection.

For embedded connections, it is the responsibility of the system integrator to ensure that the Sink device meets the requirement of a given application.

5.2.1 Stream Sink Requirement

This sub-section describes the requirements for the stream Sink in terms of video colorimetry, video timings, and audio formats. A Sink device must describe its capabilities (supported Video Colorimetry Formats, Video Timing Formats and Audio Formats) in the base EDID and/or the *CEA-861-F* Timing Extension Block (optional). The Sink device is required to support EDID v1.4.

5.2.1.1 Video Colorimetry

DP Sink devices support sinking of RGB, YCbCr, and Y-only colorimetry formats, as shown in Table 5-1. Sink devices must read the colorimetry format of the transmitted stream from the DP Main Stream Attributes.

When receiving a CEA range video stream, the Sink device should anticipate that all the code values may be used by the Source device and clamp the dynamic range if needed.

5.2.1.2 Video Timing Format

A DP Sink device must indicate whether it is able to sink the transmitted video stream by setting or clearing its RECEIVE_PORT_1_STATUS and RECEIVE_PORT_0_STATUS bits in the SINK_STATUS register (DPCD Address 00205h, bits 1:0).

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All detachable DP Sink devices must support 640x480 @ 60Hz as the Fail Safe mode. The Sink device is not required to scale 640x480 to full screen or center the image, but all pixels are required to be visible.

5.2.1.3 Audio Format

A DP Sink device that outputs audio must support an audio input stream via DP link. The audio output may be sound waves (speakers) or electrical analog or digital audio output.

Sink devices that support audio must support stereo 16-bit LPCM at 32, 44.1, and 48kHz. It is optional for all audio capable Sink devices to support other sample rates, sample sizes or number of channels.

Sink device must indicate via EDID or the CEA Timing Extension to EDID which audio formats are supported.

Note: *As of this writing, only the CEA Timing Extension to EDID provides this information, but it is anticipated that future versions of VESA EDID may also specify audio capabilities of the Sink device, and these would be acceptable to a DP Source device.*

As is the case with sinking a video stream, the Sink device must indicate whether it is able to sink the transmitted audio stream, by setting or clearing its RECEIVE_PORT_1_STATUS and RECEIVE_PORT_0_STATUS bits in the SINK_STATUS register (DPCD Address 00205h, bits 1:0).

5.2.2 Sink Device Link Configuration Requirement

The Sink device requirement for a supported link configuration depends on whether the device is a "lean-back" display or a "lean-in" display. A lean-back Sink device is a display device that is meant to be viewed from more than 1.2m (approximately 4 feet) away. For the purposes of this standard, a lean-back Sink is any display device capable of supporting an image that has a diagonal measurement of 30 inches or greater. A lean-in Sink is any display device that is not capable of supporting an image with a diagonal measurement of 30 inches or greater.

A lean-back Sink device must support the number of Main-Link lanes that provides for sufficient bandwidth even at a reduced bit rate per lane. This way, the lean-back display device can support a long cable length over which support of only a reduced bit rate is required.

Some examples of lean-back Sink devices are TV displays and projectors. Table 5-3 and Table 5-4 show examples of required lane counts for these lean-back display devices.

The Sink device of an eDP connection is regarded as a lean-in Sink and is not required to follow the rule of the lean-back Sink described above.

Table 5-3: Required Lane Count for Typical TV Timings at RBR

Timing	Lane Count	Remark
Up to 480p/576p @ 50/60Hz	One	
Up to 720p/1080i @ 50/60Hz	One @ 50Hz Two @ 60Hz	 One @ 60Hz if 16bpp YCbCr 4:2:2
Up to 1080p @ 50 / 60Hz	Four	

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Table 5-4: Required Lane Count for Typical Data Projector Timings at RBR

Timing	Lane Count	Remark
Up to 1024x768	One	18bpp
Up to 1680x1050 and 1600x1200	Two	18bpp 18bpp with reduced blanking
Up to 2048x1536	Four	18bpp with reduced blanking

A lean-in display device such as a desktop monitor may choose to minimize the lane count for lowest cost.

For example, a 1400x1050 desktop monitor may have only one Main-Link lane.

Note: *This example monitor cannot receive its Native input resolution over the one lane at the reduced bit rate.*

A Sink device with a captive cable assembly is regarded as a lean-in device, and may choose to minimize the lane count.

5.2.2.1 Sink Device Link Requirement when Other Interfaces are Supported

For a Sink device that supports other display interfaces in addition to DisplayPort, the DP input interface must provide performance equal to or better than the other display input interfaces. However, there is no requirement for the DP interface to support beyond HBR with four lanes. This display interface performance requirement includes pixel resolution, color depth, and refresh rate.

Link support beyond HBR over four lanes is not required Support of HBR2 and HBR3 is optional. RBR support is also required for "lean-back" displays as defined in Section 5.2.2; if fewer that than four lanes are supported for RBR, the number of lanes available when using RBR must support the highest display performance capability, including pixel resolution, color depth, and refresh rate.

HDCP must be supported through the DP interface if HDCP is supported through any other digital display input interface.

5.2.3 Sink Device Behavior on Stream Timing Change

5.2.3.1 Main Video Stream Timing Change

As described in Section 5.1.3, the DP Source device must insert the "idle pattern" (BS + VB-ID + Mvid7:0 + Maud7:0 with the NoVideoStream_Flag and VerticalBlanking_Flag bits in the VB-ID (bits 3 and 0, respectively) both set to 1 every 2^{13} or 8,192 LS_Clk cycles) at least five times before switching to a new video timing. Upon detecting this condition, a Sink device must get ready to receive the new Main Stream Attribute and main video stream data.

Note: *The number of inserted idle patterns may be fewer than five for an eDP connection.*

Whether to blank the display during this transition is implementation-specific. Whatever method is selected, showing a visual image that is neither the incoming video stream nor a blank screen should be avoided.

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5.2.3.2 Audio Stream Format/Timing Change

As for audio format/timing change, the Source device should set and keep the AudioMute_Flag bit in the VB-ID (bit 4) set to 1 until after the new Audio INFOFRAME and Audio_TimeStamp SDPs have been sent. An audio format change is caused by any of the following:

- Change between the compressed and non-compressed audio
- Change in the sampling rate
- Change in the number of channels

Those packets may be sent as soon as the next frame boundary (when the main video stream is present) or after the next 512th BS symbol set (when the main video stream is absent).

The Sink device must mute the audio when the AudioMute_Flag bit in the VB-ID (bit 4) is set, and should be ready to receive a new audio format upon detecting the change in Audio INFOFRAME and Audio_TimeStamp SDPs.

5.2.4 Toggling of HPD Signal for Status Change Notification

When there is a change either in the link status (e.g., loss of link synchronization) or the device status (e.g., remote control command pending), the Sink device must clear the HPD signal to low for (0.5 to 1ms) before setting it to high again, thus generating IRQ_HPD pulse, to notify the Source device of the status change. A Hot Plug event, detected by an upstream DP device as a long HPD pulse (wider than 2ms), prompts the DP Source device to take many actions, such as reading of EDID in DPCD, as well as the Receiver Capability field (DPCD Addresses 00000h through 000FFh; see Table 2-155), and the communication to its operating system. Therefore, a DP Sink device must use IRQ_HPD pulse to notify its upstream device of link status and device status change, instead of generating a long HPD pulse to emulating a Hot Plug event, unless it is prompting the DP Source device to re-read EDID and the Receiver Capability field. Especially, a DP Sink device must abstain periodic generation of long HPD pulses until the upstream device's initiating AUX transactions, because such actions may lead to soft lock-up condition of a DP Source device.

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5.2.5 Sink Device DPRX Power State

This section describes the power state of a DP Sink device consisting of Active, Standby, Sleep, and Off. The extensions to the power state specification added in this Standard are discussed in Section 5.2.5.1.

The power state specification applies to all the DP devices with DPRX, namely, DP Sink devices and DP Branch devices.

A Source device will write the value of 2h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) of a Sink device via AUX CH to place the DPRX of the Sink device in a power-save mode. In a power-save mode, the Sink device may disable Main-Link receiver of DPRX for power saving.

The Sink device must keep HPD signal asserted unless it is powered off. Therefore, the HPD signal must stay asserted when the Sink device is in a power-save mode.

When the Sink device receives the AUX request transaction while it is in a power-save mode, the Sink device is not required to reply immediately. However, the Sink device must monitor the presence of differential signal on AUX CH. The Sink device for an open, box-to-box connection must fully enable the AUX CH circuit within 1ms after detection of a differential signal so it can reply to the request transaction retry by Source device.

Note: *For an embedded connection, a Sink device may take up to 20ms from a power-save mode until it is ready to reply to an AUX request transaction.*

The Source device will write the value of 1h to the SET_POWER & SET_DP_PWR_VOLTAGE register via AUX CH to switch the Sink device out of power-save mode. Upon this AUX write transaction, the Sink device must be ready for the Source device to initiate Link Training.

The Source device may keep transmitting Idle Pattern over Main-Link even when there is no stream to transmit. The Source device may start the transmission of a stream without initiating Link Training. Therefore, the Sink device must keep the Main-Link receiver of DPRX active as long as it is receiving either a stream or Idle Pattern and as long as it keeps the HPD signal asserted.

The Sink must implement the power state machine shown in Figure 5-2.

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Figure 5-2: Sink Device Power State Machine

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Table 5-5: Sink Device Power State Machine Notes

PM_State	Description
1	**ACTIVE** The Sink device has asserted HPD, and enabled AUX CH and Main-Link RX, and is receiving an AV stream. While optionally supporting PSR as defined by eDP Standard (version 1.3 and above), a Source device may stop Main-Link signal transmission while in a PSR active state. When in a PSR active state, the Sink device will not generate IRQ_HPD to indicate the loss of LANE*x*_CR_DONE and LANE*x*_SYMBOL_LOCKED, and will continue to refresh the display from its internal Remote Frame Buffer. When the Source device stops the Main-Link signal transmission, the Sink device may disable the Main-Link RX, but must monitor the AUX CH. See eDP Standard (version 1.3 and above) for further details on Sink and Source device behavior when supporting PSR. This state is entered from one state: • State 2 (STANDBY), upon either a Source device switching from IDLE PATTERN to an AV stream transmission (Link Training required to switch from no Main-Link transmission to IDLE PATTERN at the conclusion of successful Link Training, to AV stream transmission: If the Link is already established with IDLE PATTERN transmitted, no Link Training is required). This state exits to one of three states: • State 2 (STANDBY), when the Source device starts Link Training or stops transmitting an AV stream; either transmitting IDLE PATTERN or no Main-Link signal at all. • State 3 (SLEEP), AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h). • State 4 (OFF), due to some events within the Sink device itself (e.g., soft power-off).
2	**STANDBY** The Sink device has asserted HPD, and enabled AUX CH and Main-Link RX, but is receiving either IDLE PATTERN or no Main-Link signal (LANE*x*_CR_DONE and LANE*x*_SYMBOL_LOCKED both lost). This state is entered from one of three states: • State 4 (OFF), due to some events in the Sink device itself (e.g., soft power-on). (Sink device programs its SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h) to 01h upon exiting from State 4 (OFF) and entering State 2 (STANDBY). The IRQ_HPD pulse generation is not needed, because the action of HPD assertion notifies the Source device of Hot Plug event.) • State 3 (SLEEP), upon AUX write transaction by the Source device to write 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register. • State 1 (ACTIVE), when the Source device stops transmitting an AV stream (Sink device must generate an IRQ_HPD pulse sometime (e.g., 200ms) after it has stopped receiving the Main-Link signal, that is, neither AV stream nor IDLE PATTERN). This state exits to one of three states: • State 4 (OFF), due to some events in the Sink device itself (e.g., soft power-off). • State 3 (SLEEP), upon AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register. • State 1 (ACTIVE), upon either the Source device's switching from IDLE PATTERN to an AV stream transmission (Link Training required to switch from no Main-Link transmission to IDLE PATTERN at the conclusion of successful Link Training, to AV stream transmission: If the Link is already established with IDLE PATTERN transmitted, no Link Training required).

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Table 5-5: Sink Device Power State Machine Notes (Continued)

PM_State	Description
3	**SLEEP** The Sink device has asserted HPD, and sufficiently enabled the AUX CH to at least monitor incoming AUX CH differential signals. The Main-Link RX disabled. This state is entered from one of two states: • State 2 (STANDBY), upon AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h). • State 1 (ACTIVE), upon AUX write transaction by the Source device to write 02h to the SET_POWER & SET_DP_PWR_VOLTAGE register. This state exits to one of two states: • State 4 (OFF), due to some events within the Sink device itself (e.g., soft power-off). • State 2 (STANDBY), upon AUX write transaction by the Source device to write 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register.
4	**OFF** The Sink device has de-asserted HPD, and disabled AUX CH/Main-Link. This state is entered from one of three states: • State 3 (SLEEP), due to some events in the Sink device itself (e.g., soft power-off). • State 2 (STANDBY), due to some events in the Sink device itself (e.g., soft power-off). • State 1 (ACTIVE), due to some events in the Sink device itself (e.g., soft power-off) (the Sink device may enter this state upon detecting Source disconnect or Powered-Source disconnect). This state exits to one state: • State 2 (STANDBY), due to some events in the Sink device itself (e.g., soft power-on) (the Sink device may exit this state upon detecting Source connect or Powered-Source connect).

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5.2.5.1 DP Sink Device Power State Specification Extensions

This section covers two extensions added to the DP Sink device power state specification in this Standard:

- Extended wake timeout from SLEEP power state
- CONNECTED_OFF power state addition

5.2.5.1.1 Extended Wake Timeout from SLEEP Power State

A DP Sink device can request an extended timeout for the wake from SLEEP power state. Unless the request for the extended timeout is granted by the upstream DP device, the DP Sink device must wake up in 1ms after receiving the first AUX transaction over AUX CH while in the SLEEP power state, using the registers listed in Table 5-6. (For complete register descriptions, see Table 2-156 and Table 2-165 for DPCD Addresses 00119h and 02211h, respectively.)

Table 5-6: Extended Wake Timeout from SLEEP Power State Request/Grant Registers

DPCD Address	Register
00119h	EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_GRANT
02211h	EXTENDED_DPRX_SLEEP_WAKE_TIMEOUT_REQUEST

5.2.5.1.2 CONNECTED_OFF Power State

The CONNECTED_OFF Power State is identical to the OFF Power State defined above, with one exception. In the CONNECTED_OFF power state, the DP Sink Device will keep its HPD asserted.

An upstream DP device cannot prompt a downstream device (including a DP Sink device) in the CONNECTED_OFF power state to exit the state, just as the upstream device cannot prompt the DP Sink device in the OFF power state to exit the state. When to exit the CONNECTED_OFF power state is a decision that must be made by the downstream DP device (e.g., another soft power button press on a DP display by a user).

5.2.5.1.2.1 Entry into CONNECTED_OFF Power State

To request an entry into CONNECTED_OFF power state, a DP Sink device sets the CONNECTED_OFF_ENTRY_REQUESTED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 4) to 1 and generates an IRQ_HPD pulse. The DP Sink device enters into the CONNECTED_OFF power state only after the upstream device writes 1 to clear the bit. If the upstream device does NOT clear the bit within 1s after IRQ_HPD generation, the DP Sink device de-asserts HPD, clears the bit, and then enters into the OFF power state (not the CONNECTED_OFF power state).

During the CONNECTED_OFF state, the DP Sink device must continue to monitor the presence of an upstream device and whether the upstream device is powered.

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5.2.5.1.2.2 Exit from CONNECTED_OFF Power State

The power state to which a DP Sink device in the CONNECTED_OFF power state can transition is the STANDBY power state. When a DP Sink device decides to exit the CONNECTED_OFF power state, it notifies the event by generating an IRQ_HPD. The DP device must be able to handle AUX transactions from the upstream DP device by the time it generates an IRQ_HPD. Because the IRQ_HPD is simply a notification of exit to the STANDBY power state to the upstream device, an IRQ_HPD flag bit does not need to be set.

The DP Sink device also exits the CONNECTED_OFF power state upon detecting a disconnect of the upstream device and transitions to the OFF power state.

Upon detection of an upstream DP device connection, the DP Sink device supporting the CONNECTED_OFF power state must first transition to the STANDBY power state. Once in the STANDBY power state, the DP Sink device may request re-entry into the CONNECTED_OFF state by generating an IRQ_HPD after setting the CONNECTED_OFF_ENTRY_REQUESTED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 4).

5.2.6 Sink Device DSC Bitstream Handling and FEC Policy

New to *DP v1.4*.

A DSC bitstream decompression-capable DP Sink device shall have FEC decoding capability. (See Section 3.5.1.5.)

When a DP Source device sets the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training, the DP Sink device shall delay Link Layer Code forwarding to the 8b/10b decoder and descrambler blocks by the same amount required for FEC decoding, even when it is not performing FEC decoding (that is, the DP Sink device shall ensure that enabling and disabling of FEC decoding is transparent to its HDCP decryption block and Link Layer block).

The DP Sink device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

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5.3 Branch Device in SST-only Mode

This section describes the requirement for SST-only mode DP Branch devices. Branch device types are summarized in this section.

5.3.1 EDID Access Handling Requirement

A Branch device must make sure that the stream transmitted by the Source device can be sunk by at least one Sink device in the link. Therefore, a Branch device without its own local stream sink must forward the EDID access request from its upstream device to its downstream device.

When a Branch device has multiple DFPs, it has multiple choices regarding which downstream device(s) should receive the EDID access request.

The DP Branch device must route the EDID access to the lowest numbered, unassigned, DFP to which a downstream device is connected. If the DP Branch device is a matrix switch with multiple input and output ports capable of multiple connections (e.g., Input Port *N* to Output Port *M*, Input Port *N* + 1 to Output Port *M* + 1), then the subsequent SST Source devices connected must be assigned the lowest numbered, unassigned, connected DFP among the remaining ones. If there is no unassigned, connected DFP, the Branch device must wait until a DFP becomes connected or another SST DP Source device is disconnected before assigning a port to the SST DP Source device. The adaptor must neither cache nor modify the EDID contents.

5.3.2 Branch Device Link Configuration Requirements

As for the requirement link configuration of a DP Branch device with DP output port, see Section 2.1.4.1. In case a DP Branch device operating in SST mode needs to change the DPCD Receiver Capability register values based on the capability of the connected DP device to its DFP, the Branch device must generate a long HPD pulse from its UFP. The long HPD pulse prompts the upstream DP device in SST mode to read the updated Receiver Capability registers values.

Converters (either from DisplayPort-to-Legacy or Legacy-to-DisplayPort) may have fewer than four Main-Link lanes as long as the DP link provides sufficient bandwidth for the Legacy link at the DP Main-Link rate of HBR or RBR.

The converters must support the lane count that meets the bandwidth requirement at a reduced bit rate per lane.

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5.3.2.1 Branch Device's Power State Transition Handling

A Branch device must ensure that Source is correctly updated if a connect or disconnect event occurs on one of the Branch's DFPs while it is in a power-saving mode. If the Branch device detect a change in HPD on a DFP or is a protocol converter and keeps its DFP connect/disconnect detection circuitry (where implemented) active during low power mode, then it must update the SINK_COUNT register (DPCD Address 00200h) and issue an interrupt (IRQ_HPD) whenever it detects a connect/disconnect event on a DFP.

Note: *The Source can decide whether to ignore the interrupt or bring the Branch device out of low power to read the new value in the SINK_COUNT register. The Branch device must not exit low-power mode when it detects connect/disconnect. If the Branch device has downstream connect/disconnect detection circuitry but disables it during low-power mode or disables its HPD detection circuitry during power-save mode (as appropriate), then the Branch device must preserve the sense of the connected display during sleep, and on exit from low-power mode, the Branch device must reactivate its DFP connect/disconnect detection or HPD detection circuitry, update the SINK_COUNT register (only if necessary), and generate an IRQ_HPD if the result of this update is to change the preserved value stored in the SINK_COUNT register.*

5.3.2.2 Branch Device DSC Bitstream Handling and FEC Policy

New to *DP v1.4*.

A DSC bitstream decompression-capable DP Branch device in SST mode (i.e., DP-in, DP-out Link Rate/Lane Count Converter and Active Protocol Converter) is a DP DSC Sink device and shall have FEC decoding capability (see Section 3.5.1.5).

When a DP Source device sets the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training, the DP Branch device shall delay Link Layer Code forwarding to the 8b/10b decoder and descrambler blocks by the same amount required for FEC decoding, even when it is not performing FEC decoding (that is, the DP Branch device shall ensure that enabling and disabling of FEC decoding is transparent to its HDCP decryption block and Link Layer block).

The DP Branch device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

5.3.3 Active Protocol Converter Adaptors

5.3.3.1 General Requirements

An active protocol converter adaptor must assert HPD signal whenever it is plugged into the Source device that has its DP_PWR enabled, whether or not the converter has a connected display (Sink device) on its DFP.

The adaptor must set the DFP_PRESENT bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 0) to 1 to indicate the presence of DFPs to its upstream device. It must also set the DFP_COUNT field in the DOWN_STREAM_PORT_COUNT register (DPCD Address 00007h, bits 3:0) to indicate the number of DFPs.

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The adaptor must set the DFP_TYPE field bits in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bits 2:1) to indicate the type of the main DFP (DFP 0). In addition, the adaptor must set the Detailed Capabilities Info registers (DPCD Addresses 00080h through 0008Fh) to show all the downstream types, including DFP 0. Either one or four bytes are used, per DFP type indication. Therefore, up to 16 (with 1-byte descriptor) or 4 (with 4-byte descriptor) DFP capabilities can be stored.

Note: *For DP protocol converters with DPCD r1.4 (or higher), support for the Detailed Capabilities Info register is required. Even for those with DPCD r1.3 (or lower), support for the Detailed Capabilities Info register's four-byte format to provide detailed capability information is strongly recommended.*

The adaptor must implement a circuitry to detect plug/unplug status of its Sink device if the DFP type provides for the means for detection. When the plug/unplug detection is possible, the adaptor must dynamically update the number of connected Sink devices in the SINK_COUNT field in the SINK_COUNT register (DPCD Address 00200h, bits 7, 5:0). Whenever the Sink device count is changed, the adaptor must do the following:

1 Update the SINK_COUNT register.

2 Set the DOWNSTREAM_PORT_STATUS_CHANGED bit in the LANE_ALIGN__STATUS_UPDATED register (DPCD Address 00204h, bit 6).

3 Issue an IRQ_HPD pulse.

The adaptor must clear the DOWNSTREAM_PORT_STATUS_CHANGED bit immediately after the Source device reads it.

The adaptor must indicate whether the Receive Ports of the DPRX within the adaptor are properly receiving and regenerating the incoming streams, using the RECEIVE_PORT_1_STATUS and RECEIVE_PORT_0_STATUS bits in the SINK_STATUS register (DPCD Address 00205h, bits 1:0, respectively).

Note: *This definition of SINK_STATUS bits is in contrast with that for a Sink device, for which these bits indicate whether the Sink device is in synchronization with the receiving streams.*

The adaptor must allow the DP Source device to drive display modes that are not specified in the EDID mode list and to drive display modes that are outside the range specified in EDID (if EDID is accessible).

The adaptor must put the connected Sink device into a low power state (means of which is dependent on the type of downstream display interface of the cable converter) whenever there is both no video transmitted by the DP Source device and the Source device has written the value of 02h to its SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h).

It is recommended that the adaptor have an ability to adjust the DDC bit rate down to 1k to 10kbps on its DFP(s). Furthermore, it is recommended that the adaptor have the ability to indicate its default I^2C bit rate and supported bit rates to the Source device and that it allows the Source device to select the bit rate (using the I2C Speed Control Capabilities Bit Map and I2C Speed Control/ Status Bit Map registers (DPCD Addresses 0000Ch and 00109h), respectively)).

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The Detailed Capabilities Info registers apply when the FORMAT_CONVERSION bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 3) is 0. In this case, the responsibility of an active protocol converter is to transmit a stream it has received from a DP Source device as is, without timing format change or pixel data processing. The corollary is that the Source device must limit the audio/video formats and resolutions to those that the Sink device advertises that it supports.

A Branch device with DFP type of DisplayPort must implement at least two Receive Ports, must be capable of transporting an audio stream, and must support HBR audio.

5.3.3.2 VGA Protocol Converter Adaptors

When the DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) is 0 and DFPX_TYPE field in the Detailed Capabilities Info register (DPCD Address 00080h, bits 2:0) = 001 (Analog VGA), the Analog VGA DAC must support the maximum pixel rate for 24-bits-per-pixel color depth (= 3 Bytes/pixel, 8 bits per component) within the maximum Link Bandwidth of its upstream DPRX.

Example: The maximum Link Rate is HBR (2.7Gbps/lane) and the maximum Lane Count is two lanes. The maximum Link Bandwidth = 540MBps. The maximum pixel rate for 24-bits-per-pixel (= 3 Bytes per pixel) is 180MP/s.

The adaptor must permit the VGA outputs to be driven with an image provided by the DP Source device as long as it is receiving a valid DisplayPort video stream even when it does not detect a connected display and before the DP Source device has attempted an EDID read.

A VGA protocol convertor shall only update the SINK_COUNT fields in the SINK_COUNT and SINK_COUNT_ESI register(s) (DPCD Address(es) 00200h and 02002h, respectively, bits 7, 5:0) when the converter can identify a connectivity state change by way of load detection, I^2C probe, or other method.

The adaptor is required to implement load sensing on the VGA pins or an equivalent method to make a best-effort detection of the presence of a connected display. The adaptor must advertise this capability in the ADAPTOR_CAP register (DPCD Address 0000Fh). Additionally, the adaptor shall set the FORCE_LOAD_SENSE bit in the ADAPTOR_CTRL register (DPCD Address 001A0h, bit 0) to 1, by default.

Note: *Given the wide variation of display implementations, VGA load sensing may not be reliable.*

5.3.3.3 DVI, HDMI, and DP++ Protocol Converter Adaptors

These Protocol Converter Adaptors must support capabilities as indicated in Table 5-7. The table covers additional requirements for converters with DPCD r1.4 (and higher).

The DPCD r1.4 (and higher) data structure includes the Protocol Converter Extension field (DPCD Addresses 03000h through 030FFh; see Table 2-166). Furthermore, two IRQ_HPD vector bits are added:

- CEC_IRQ bit in the DEVICE_SERVICE_IRQ_VECTOR_ESI1 register (DPCD Address 02004h, bit 2)
- HDMI_LINK_STATUS_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 3)

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A DP Source device shall source an under-scanned image. A DP-to-HDMI protocol converter shall indicate an under-scanned image type by way of an AVI INFOFRAME SDP.

When the HDMI_AUTONOMOUS_SCRAMBLING_DISABLE and HDMI_EDID_PROCESSING_DISABLE bits in the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h, bits 2:1, respectively) are both cleared to 0, an HDMI Protocol Converter shall process the HDMI Sink device's EDID to determine appropriate support for HDMI scrambling and population of the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h).

When the HDMI_EDID_PROCESSING_DISABLE is set to 1, an HDMI Protocol Converter shall ***not*** process the HDMI Sink device's EDID to determine appropriate support for HDMI scrambling (scrambling must ***not*** be automatically enabled if the TMDS Character Rate is less than 340TMDS Character Rate is less than 340Mcps), –or– population of the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h should read 00h).

When the HDMI_AUTONOMOUS_SCRAMBLING_DISABLE bit is set to 1, HDMI scrambling for the TMDS Character Rate is less than 340 Mcps) will be controlled by HDMI_FORCE_SCRAMBLING bits in the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h, bit 3). However, the Protocol Converter shall not perform an autonomous EDID read that might collide (or overlap) with an attempt by the DP Source device to read the HDMI Sink device's EDID. The Protocol Converter may either perform an autonomous EDID read before programming the SINK_COUNT field in the SINK_COUNT register (DPCD Address 00200h, bits 7, 5:0) to a value greater than 0, –or– may snoop an EDID read performed by the DP Source device (recommended behavior). The DP Source device shall perform a full EDID read of all the EDID blocks before initiating video signaling.

Table 5-7: DVI, HDMI, and DP++ Protocol Converter Adaptor Requirements

Requirement	DFP Type[a]		
	DVI	HDMI	DP++
Must support I^2C-over-AUX to facilitate an EDID read of an HDMI Sink device by a DP Source device.	Y	Y	Y
Must support all TMDS character clock rates on its DFP between 25MHz and the maximum declared TMDS character clock rate supported on the DFP of the adaptor.	Y	Y	Y
The input DP bandwidth must support the maximum TMDS character clock rate supported on the DFP of the adaptor.	Y	Y	Y
Must support all blank, total and active combinations that are valid within the maximum TMDS clock rate supported on the DFP of the adaptor. For example, if 594MHz is reported as maximum TMDS character clock rate on the DFP, the protocol converter must support 4kx2k at 60Hz with RGB/YCbCr444 pixel encoding format at 8bpc (24bpp).	Y	Y	Y
When the DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register (DPCD Address 00005h, bit 4) is 0 the maximum TMDS character clock rate supported on the DFP must be at least 165MHz, and the maximum color depth supported must be 8 bits per component.	Y	Y	Y
Must support RGB, YCbCr 4:4:4, and YCbCr 4:2:2 formats. Color format conversion (e.g. YCbCr <-> RGB, or YCbCr 4:4:4 <-> YCbCr 4:2:2) is not required.	N/A	Y	Y

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Table 5-7: DVI, HDMI, and DP++ Protocol Converter Adaptor Requirements (Continued)

Requirement	DFP Type[a]		
	DVI	HDMI	DP++
Must support all color depths (bits per component) up to the declared Maximum Bits per component as long as the declared Maximum TMDS character clock rate on the DFP is not exceeded.	N/A	Y	Y
Must generate INFOFRAME SDPs to the downstream device.	N/A	Y	Y
Must be able to accept and pass through the following 3D formats: • Frame pack using CEA INFOFRAME • Side by side, and top and bottom	N/A	Y	Y
May support converting DP 3D frame sequential format (with left/right field indicated by the MISC1 field, bits 2:1) to frame pack HDMI 3D format. If supported, the adaptor must set the FRAME_SEQ_TO_FRAME_PACK bit in the Detailed Capabilities Info register (DPCD Address 0008Fh, bit 0) to 1 for the appropriate port type. If supported, the adaptor must be able to detect 3D frame sequential and automatically perform the conversion to frame pack. For a DP-to-HDMI converter with DPCD r1.4 (or higher), support is required.	N/A	O/Y	O/Y
Must implement at least two receive ports, be capable of transporting an audio stream, and support HBR audio.	N/A	Y	Y
May support DVI Dual Link on its DFP. If supported, the adaptor sets the DUAL_LINK bit in the Detailed Capabilities Info register (DPCD Address 0008Fh, bit 1) to 1 for DVI DFPs. Additionally, the adaptor must be capable of supporting higher pixel clocks and/or deeper color consistent with the Dual Link requirements of *DVI r1.0*. Note that the declared maximum TMDS clock rate capability is not the same as the maximum pixel rate in Dual Link configurations.	O	N/A	N/A
Must be able to operate as an HDCP1.x repeater.	Y	Y	Y

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Table 5-7: DVI, HDMI, and DP++ Protocol Converter Adaptor Requirements (Continued)

Requirement	DFP Type[a]		
	DVI	HDMI	DP++
Additional Requirements for DP-to-HDMI/DP++ Converter with DPCD r1.4 for the UFP DPRX for Supporting HDMI2.0[b]			
600MHz TMDS character clock support.	N/A	Y	Y
Must have the DETAILED_CAP_INFO_AVAILABLE bit in the DOWN_STREAM_PORT_PRESENT register(s) (DPCD Addresses 00005h and 02205h, bit 4) set to 1 with all the detailed info (at Bytes 1 through Byte 3).	N/A	Y	Y
Must be able to convert to DVI (instead of HDMI) when instructed by an upstream DP Source device with the PROTOCOL_CONVERTER_CONTROL_0 register (DPCD Address 03050h) value.	N/A	Y	Y
Must monitor and report downstream HDMI2.0 link status including the generation of IRQ_HPD with the HDMI_LINK_STATUS_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 3). This capability is reported in the DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED bit in the DOWNSTREAM_LINK_ERROR_REPORTING_SUPPORTED register (DPCD Address 03030h, bit 0).	N/A	Y	Y
Must autonomously enable HDMI2.0 scrambling and TMDS CLK CH clock frequency division by 4 when needed. Whenever the downstream HDMI2.0 sink device is capable of supporting scrambling, the converter must enable scrambling without any instruction from a DP Source device. (See also the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h)).	N/A	Y	Y
Must interpret a portion of HDMI2.0 EDID to determine the YCbCr420 component bit depth support capability and update the HDMI_SINK_YCBCR420_COMPONENT_BIT_DEPTH_SUPPORT register (DPCD Address 03034h). (See also the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h)).	N/A	Y	Y
Must support pixel encoding format conversion to YCbCr420 from YCbCr444 as instructed by an upstream DP Source device; the INFOFRAME SDPs must match the converted pixel encoding format with the PROTOCOL_CONVERTER_CONTROL_1 register (DPCD Address 03051h) value.	N/A	Y	Y
Must support pixel encoding format conversion to YCbCr422 from YCbCr444 as instructed by an upstream DP Source device; the INFOFRAME SDPs must match the converted pixel encoding format with the PROTOCOL_CONVERTER_CONTROL_2 register (DPCD Address 03052h) value.	N/A	O	O
YCbCr420 pass-through from DP input port to HDMI2.0 output port.	N/A	Y	Y
Must support CEC-Tunneling-over-AUX as described in this section (see Section 5.3.3.3.1).	N/A	Y	Y
Must be able to operate as an HDCP2.2 repeater.	N/A	O	O

a. Y = Required, O = Optional, N/A = Not Applicable.

b. When a DP Source and DP-to-HDMI converter are placed within a device of a single physical enclosure, such a device functions as an HDMI Source device. Which features to enable at the HDMI connector of an HDMI Source device is an HDMI Source device implementer-specific choice. Therefore, the feature support requirement indicated within this table does not apply.

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5.3.3.3.1 CEC-Tunneling-over-AUX

5.3.3.3.1.1 Terminologies

Table 5-8: CEC-Tunneling-over-AUX Terminologies

Terminology	Definition
CEC Frame	The representation of a CEC Message on the CEC Line as defined in HDMI spec. A start bit followed by a number of data bits (including all EOM and ACK bits).
CEC Message	Addressing and data content of a CEC Frame (excluding the START bit and EOM/ACK bits). An array of 8-bit bytes consisting of a Header Block and 0 to 15 Data Blocks. The (first) block of the CEC Frame with EOM=1 is the last block of the CEC Message. In case any block of a CEC frame is negatively acknowledged, then that block becomes the last block of the CEC Message, even if EOM = 0.
Broadcast Message	As defined in the HDMI Specification.
CEC Line Error	
Destination	
Follower	
Initiator	
Logical Address (LA)	
Logical HPD	Pertains to the HDMI HPD input signal for the DFP of a DP-to-HDMI converter. De-asserted only after 100ms of a low period on the HDMI HPD signal, which is required upon an EDID change and is otherwise de-bounced to avoid spurious a state transition.
Snooping	Receiving CEC messages where the DP-to-HDMI converter does not act as a Follower on the CEC bus (in the CEC standard sense, which carries obligations of controlling ACK and CEC Line Error reporting).

5.3.3.3.1.2 Overview

CEC-Tunneling-over-AUX is the tunneling of CEC messages using Native AUX transactions across DP AUX CH between a DP Source device and a DP-to-HDMI protocol converter. The DP Source device operates as a CEC message consumer and producer, while the DP-to-HDMI protocol converter capable of CEC-Tunneling-over-AUX operation tunnels CEC messages between the DP Source device and CEC bus, as illustrated in Figure 5-3. DPCD address mapping for CEC-Tunneling-over-AUX is valid only for DPCD r1.4 (or higher).

Besides tunneling CEC messages that are targeted at the CEC logical address of the DP-to-HDMI converter (i.e., the DP-to-HDMI converter is the Follower) or broadcast (which has the logical address of Fh as the destination address), CEC-Tunneling-over-AUX as defined in this Standard allows for the DP Source device to monitor all CEC messages, regardless of whether they are successfully ended/acknowledged, as long as the DP-to-HDMI converter is capable of Snooping mode. Additionally, the DP Source can assign multiple logical addresses to which the DP-to-HDMI converter must act as the Follower if the DP-to-HDMI converter supports multiple logical addresses.

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Because the first block of the CEC message contains both the destination logical address and initiator's logical address, the DP Source device, upon receiving the message, can determine whether the message was targeted to the DP-to-HDMI converter.

For a DP-to-HDMI protocol converter with DPCD r1.4 (or higher), CEC-Tunneling-over-AUX support is mandatory. For a DP Source device, CEC-Tunneling-over-AUX support is optional. It is recommended that if a DP Source device supports CEC-Tunneling-over-AUX, the DP Source device complies with HDMI2.0 CEC functionality.

A DP-to-HDMI protocol converter with more than one HDMI DFP must use only one of the HDMI DFPs for CEC-Tunneling-over-AUX.

Figure 5-3: CEC Topology

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5.3.3.3.1.3 CEC-Tunneling-over-AUX Field

Table 5-9 lists the registers that are used for CEC-Tunneling-over-AUX. (For complete register descriptions, see Table 2-166.)

Table 5-9: CEC-Tunneling-over-AUX Field

DPCD Address	Register
03000h	CEC_TUNNELING_CAPABILITY
03001h	CEC_TUNNELING_CONTROL
03002h	CEC_RX_MESSAGE_INFO
03003h	CEC_TX_MESSAGE_INFO
03004h	CEC_TUNNELING_IRQ_FLAGS
0300Eh and 0300Fh	CEC_LOGICAL_ADDRESS_MASK
03010h and 0301Fh	CEC_RX_MESSAGE_BUFFER
03020h and 0302Fh	CEC_TX_MESSAGE_BUFFER

5.3.3.3.1.4 Power Management Considerations

The Source device might support CEC power management, in which case the Source device must interpret CEC power management commands, either directed or broadcast standby, and must put the DP-to-HDMI protocol converter into a lower power state by writing to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h).

The DP-to-HDMI protocol converter must not enter a low power state by interpreting the CEC power management command. Rather, the protocol converter is placed into a lower power state (DPRX SLEEP power state) only by the Source device's programming of the SET_POWER & SET_DP_PWR_VOLTAGE register to 02h. Even when placed into the DPRX SLEEP power state, the DP-to-HDMI protocol converter must keep the HPD output to the DP Source device to a high level and keep the CEC-tunneling-related block sufficiently active so that the protocol converter can receive a CEC message and generate an IRQ_HPD with the corresponding IRQ flag bits set.

The Source device supporting CEC-Tunneling-over-AUX must support being awakened by an IRQ_HPD from the DP-to-HDMI protocol converter. It should be noted that it is a matter of a Source device's policy the extent to which it implements a low-power state. Typically, the Source device would do no more than place the GPU sourcing a stream into a low-power state while maintaining the unrelated functionality in full operation.

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5.3.3.4 S-Video/Composite/Other Analog Video Protocol Converter Adaptors

An adaptor from DisplayPort to S-Video, composite video or other analog video may implement a method of detecting a connected display. Such an adaptor must not support I^2C-over-AUX to DDC pass-through for EDID.

5.3.3.5 Dual-link DVI Protocol Converter Adaptors

A DP to dual-link DVI protocol converter adaptor is used for connecting a DP Source device to a dual-link DVI Sink device as shown in Figure 5-4. The adaptor must use HPD on the DVI port to detect the presence of a connected display.

Figure 5-4: DisplayPort-to-Dual-link DVI Cable Adaptor

5.3.3.6 MSA Horizontal Blanking Expansion Operation Support

New to *DP v1.4*.

As described in Section 2.2.4.1.2, a DP Branch device capable of supporting MSA Horizontal Blanking Expansion operation shall express its capability in the RECEIVE_PORT0_CAP_1 and RECEIVE_PORT0_CAP_0 registers (DPCD Addresses 00009h and 00008h, respectively).

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5.3.4 Link Rate and Lane Count

New to *DP v1.4*.

PHY Repeaters (i.e., Redrivers and Retimers) shall have the same link rate and lane count between the DPRX PHY UFP and DPTX PHY DFP. The PHY Repeaters shall use the serial bit rate of the upstream DP link to drive the downstream DP link.

5.3.5 Forward Error Correction

New to *DP v1.4*.

Forward Error Correction (FEC) support of LT-tunable bit-level PHY Repeaters is optional.

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5.4 Source Device in MST Mode

Entire section rewritten for *DP v1.4*.

An MST-capable Source device shall support either TPS4 or POST_LT_ADJ_REQ, as described in Section 3.5.1.2, to avoid link fragility upon switching from Link Training to AV stream transmission.

5.4.1 Prompting the MST/SST Capabilities Transition of the Downstream Device

The downstream device is in SST mode, by default, as described in Section 5.5.1.1 and Section 5.6.1.1.

An MST-capable Source device shall discover whether the downstream device is MST-capable by reading the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0). The MST-capable DP Source device shall set the UPSTREAM_IS_SRC, UP_REQ_EN, and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 2:0, respectively) to program the MST-capable downstream device to MST mode and indicate itself as an MST-capable device. The Source device shall then change the value of the MSTM_CTRL register, after it has inactivated the link, to the MST-capable downstream device.

To set the downstream device back to SST mode, the MST-capable DP Source device shall clear the MST_EN bit after inactivating the link to the MST-capable downstream device.

5.4.2 Atomic Message Transaction Generation

There are MST-capable Sink/Branch devices in the field that do ***not*** handle interleaved message transactions.

To facilitate message transaction handling by downstream devices, an MST-capable Source device shall generate message transactions in an atomic manner (i.e., the MST-capable Source device shall not concurrently interleave multiple message transactions). Therefore, an MST-capable Source device shall clear the Message_Sequence_No value in the Sideband_MSG_Header to 0.

MST-capable Source devices that support field policy updates by way of software are strongly recommended to update the policy to forego the generation of interleaved message transactions.

5.4.3 Power Management

An MST-capable DP Source device in MST mode shall use the PWR_DOWN_PHY message transaction to power-down the DPRX ports connected to the entire path. Additionally, the MST-capable DP Source device in MST mode shall write 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) to its immediate downstream device, to prompt ***only*** that downstream device's DPRX port to transition to the D3 (power-down mode) state.

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5.4.4 DSC Bitstream Transport and FEC Policy

An MST-capable Source device with DSC bitstream sourcing capability shall support FEC encoding. (See Section 3.5.1.5.) An MST-capable DP Source device in MST mode shall enable DSC bitstream transport and FEC encoding only after discovering the following:

- Presence of a DSC decompression-capable device at the end of the path (either the last MST Branch or SST Sink device), by reading DSC Capability DPCD registers through a REMOTE_DPCD_RD transaction
- FEC capability of the entire path by reading the FEC_Capability field of the reply to an ENUM_PATH_RESOURCES message transaction

To enable FEC encoding and decoding, the MST-capable DP Source shall first set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training.

An MST-capable DP Source device in MST mode that enables FEC encoding shall take into account the 2.3% transport overhead of FEC when it calculates the PBN value of the AV stream it is about to transmit.

5.5 Sink Device in MST Mode

Entire section rewritten for *DP v1.4*.

5.5.1 MST Sink Device with a Single DPRX Upstream-Facing Port

An MST-capable Sink device shall set the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) to 1 to indicate its MST capability to the upstream device.

An MST-capable Source device shall support either TPS4 or POST_LT_ADJ_REQ, as described in Section 3.5.1.2, to avoid link fragility upon switching from Link Training to AV stream transmission.

5.5.1.1 Transition to SST Mode

If any of the following four conditions exist, the MST-capable Sink device shall configure itself to SST mode:

- Power is cycling
- Disconnection of an upstream device is detected
  - An MST-capable Sink device shall implement the detection of both an upstream device connection and a powered upstream device connection
- Upstream device's MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is cleared to 0
  - An MST-capable Sink device shall consistently monitor the MSTM_CTRL register value
- User selects SST mode through the Sink device's user interface (e.g., by way of a menu option)
  - An MST-capable Sink device shall generate a long HPD pulse to the upstream device when this condition occurs

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The MST Branch device shall take the following actions to configure itself to SST mode:

- Clear its own MSTM_CTRL register (DPCD Address 00111h)
- Clear its own VC Payload Mapping Table registers
  - PAYLOAD_ALLOCATE_SET register (DPCD Address 001C0h)
  - PAYLOAD_ALLOCATE_START_TIME_SLOT register (DPCD Address 001C1h)
  - PAYLOAD_ALLOCATE_TIME_SLOT_COUNT register (DPCD Address 001C2h)
  - PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h)
  - VC_PAYLOAD_ID_SLOT_*x* registers (DPCD Addresses 002C0h through 002FFh)
- Clear outstanding request fragments from the Sideband MSG buffer fields in the following registers
  - DOWN_REP registers (DPCD Addresses 01400h through 015FFh)
  - UP_REQ registers (DPCD Addresses 01600h through 017FFh)

In SST mode, the MST-capable Sink device shall follow the policy requirement of an SST Sink device, as described in Section 5.2.

5.5.1.2 Transition to MST Mode

After an upstream device sets the UP_REQ_EN and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 1:0, respectively), the MST-capable Sink device shall configure itself to MST mode and be ready for receiving message transactions from an upstream device and for Link Training to MST transport format.

5.5.1.3 Issuance of Connection Status Notify Message Transactions

Because the local stream sinks are permanently connected to its MST Branching Unit (BU), the MST-capable Sink device shall not issue a Connection Status Notify (CSN) message transaction. In other words, a CSN shall never be issued for Logical ports (i.e., Port Numbers 8h through Fh). The issuance of a CSN is limited to Physical ports (i.e., Port Numbers 0h through 7h).

5.5.1.4 Issuance of Resource Status Notify Message Transactions

The DP MST Source devices currently available in the market handle CSN message transactions, but not Resource Status Notify (RSN) message transactions. Therefore, an MST Sink device shall ***not*** issue RSN message transactions.

5.5.1.5 Power Management Handling

After an upstream device writes 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0), an MST-capable Sink device in MST mode shall disable the Main-Link RX of the upstream-facing DPRX.

The MST Branch device shall keep the VC Payload Mapping Table registers (see Section 5.5.1.1) set while in a lower power state. The MST Branch device shall clear the VC Payload Mapping Table registers only after the device receives a CLEAR_PAYLOAD_ID_TABLE message transaction, –or– when the device transitions to SST mode (as described in Section 5.5.1.1).

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5.5.1.6 Mvid/Nvid and Maud/Naud Handling

The link rate between the MST-capable Sink device and its immediate-upstream MST Branch device may be different from that which the DP Source device in MST mode is driving. In other words, the Mvid/Nvid and Maud/Naud values that the MST-capable Sink device receives may not match the ratio between the Link Symbol clock rate and pixel clock rate, and Link Symbol clock rate and audio clock rate, respectively.

The MST-capable Sink device in MST mode shall be able to regenerate the pixel clock and the audio clock without re-sorting Mvid/Nvid and Maud/Naud values.

5.5.1.7 Split SDP Handling

An MST-capable Sink device shall support handling of a split SDP.

5.5.1.8 DSC Bitstream Handling and FEC

An MST-capable Sink device with DSC bitstream decompression capability shall support FEC decoding (see Section 3.5.1.5).

When the upstream DPTX sets the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 before initiating Link Training, the MST-capable DP Sink device shall delay forwarding of Link Layer codes to the 8b/10b decoder and descrambler blocks by the same amount required for FEC decoding, even when the device is not performing FEC decoding.

The MST-capable Sink device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

5.5.1.9 Interleaved Message Transactions Handling

As described in Section 5.4.2, an MST-capable Source device is no longer allowed to generate interleaved message transactions. However, there are MST-capable Source devices out in the field that issue interleaved message transactions. Therefore, an MST-capable Sink device shall continue being able to handle interleaved message transactions.

5.5.2 MST-Capable Sink Device with Multiple DPRX Upstream-Facing Ports

The policy of an MST-capable Sink device with multiple DPRX UFPs is an implementation-specific choice. For example, the device may either choose to map fixed local stream sinks to each DPRX UFP without any overlap among the ports, –or– take a first-come, first-serve policy.

5.6 Branch Device in MST Mode

Entire section rewritten for *DP v1.4*.

5.6.1 MST-capable Branch Device with a Single DPRX Upstream-Facing Port

An MST-capable Branch device shall set the MST_CAP bit in the MSTM_CAP register (DPCD Address 00021h, bit 0) to 1 to indicate its MST capability to the upstream device. The MST-capable Branch device shall support four lanes, both on the DPRX UFP and DPTX DFPs.

An MST-capable Branch device shall support either TPS4 or POST_LT_ADJ_REQ, as described in Section 3.5.1.2, to avoid link fragility upon switching from Link Training to AV stream transmission.

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Additionally, it is recommended that an MST-capable Branch device support FEC decoding on the DPRX UFP and re-encoding on the DPTX DFPs to support routing of VC Payloads containing the DSC bitstream.

5.6.1.1 Transition to SST Mode

If any of the following three conditions exist, the MST-capable Branch device shall configure itself to SST mode:

- Power is cycling
- Disconnection of an upstream device is detected
  - An MST Branch device shall implement the detection of both an upstream device connection and a powered upstream device connection
- Upstream device's MST_EN bit in the MSTM_CTRL register (DPCD Address 00111h, bit 0) is cleared to 0
  - An MST-capable Branch device shall consistently monitor the MSTM_CTRL register value

The MST-capable Branch device shall take the following actions to configure itself to SST mode:

- Clear its own MSTM_CTRL register (DPCD Address 00111h)
- Clear its own VC Payload Mapping Table registers
  - PAYLOAD_ALLOCATE_SET register (DPCD Address 001C0h)
  - PAYLOAD_ALLOCATE_START_TIME_SLOT register (DPCD Address 001C1h)
  - PAYLOAD_ALLOCATE_TIME_SLOT_COUNT register (DPCD Address 001C2h)
  - PAYLOAD_TABLE_UPDATE_STATUS register (DPCD Address 002C0h)
  - VC_PAYLOAD_ID_SLOT_*x* registers (DPCD Addresses 002C0h through 002FFh)
- Clear the MSTM_CTRL register (DPCD Address 00111h) of all MST-capable downstream devices
- Clear outstanding request fragments from the Sideband MSG buffer fields in the following registers
  - DOWN_REP registers (DPCD Addresses 01400h through 015FFh)
  - UP_REQ registers (DPCD Addresses 01600h through 017FFh)

In SST mode, the MST-capable Branch device shall follow the policy requirement of an SST Branch device, as described in Section 5.3.

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5.6.1.2 Transition to MST Mode

After an upstream device sets the UP_REQ_EN and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 1:0, respectively), the MST-capable Branch device shall configure itself to MST mode by doing the following:

- Be ready for receiving message transactions from an upstream device and for Link Training to MST transport format
- Sets the UP_REQ_EN and MST_EN bits of the MSTM_CTRL register (DPCD Address 00111h, bits 1:0, respectively) of the MST-capable downstream devices after disabling the Main-Link signal transmission before initiating Link Training

The MST-capable Branch device in MST mode shall always set the downstream links to the MST-capable devices to the maximum link bandwidth and initiate Link Training with the MST_EN bit set to enable MST transport format. Additionally, the MST Branch device capable of FEC decoding and re-encoding shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 when it trains the downstream DPRX that is capable of FEC decoding.

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5.6.1.3 Issuance of Connection Status Notify Message Transactions

The HPD input is used to detect the plugging and unplugging of downstream devices. A Sink device, regardless of whether it is a DP Sink device or other type of Sink device (e.g., an HDMI Sink device), has a tendency of toggling its HPD output for various reasons. An MST Branch device shall avoid issuing a CSN message transaction for a hot unplug or a hot plug in immediate response to the HPD input level change. Rather, the Sink device shall scatter and possibly minimize the number of CSN message transactions that it issues, using the policy described in this sub-section.

An MST Branch device shall issue a CSN message transaction for hot unplug of a DFP. An MST Branch device shall then wait for the unplug CSN message transaction to be ACKed by its immediate upstream device before issuing the CSN message transaction for hot plug of the DFP should the DFP's HPD signal go active before the ACK. It is recommended that the MST Branch device, in addition to waiting for the ACK from its immediate upstream device, either wait for the ALLOCATE_PAYLOAD message transaction with a PBN value equal to 0 from the MST Source device for de-allocating the time slot assigned to the VC Payload that is routed to the unplugged DFP or for 2 seconds, whichever occurs first.

The MST Branch device shall generate a CSN message transaction corresponding to the HPD signal's status at the time the device is ready to generate the CSN. If, for example, the DFP HPD signal goes low (which prompts the issuance of a CSN message transaction for hot unplug), goes high, and then goes low again, by the time the MST Branch device has confirmed that the upstream devices have handled the hot unplug CSN message transaction, the device shall not generate CSN message transactions that indicate hot plug and hot unplug events that have occurred since the last hot unplug CSN message transaction. Rather, the MST Branch device shall not issue any CSN message transaction because the current connection status is unplug, which matches the status conveyed by the last CSN message transaction.

Additionally, some DP Sink devices in low-power mode are known to not reply to AUX transactions while asserting the HPD signal (which is non-compliant with *DP v1.4*). The MST-capable Branch device is recommended to check that the connected downstream DP device replies to AUX transactions before issuing CSN message transactions for hot plug. In case the downstream DP Sink device does not respond to an AUX transaction, the MST Branch device shall periodically issue an AUX transaction so that it can detect when the DP Sink device becomes responsive.

5.6.1.4 Issuance of Resource Status Notify Message Transactions

The DP MST Source devices currently available in the market handle CSN message transactions, but not Resource Status Notify (RSN) message transactions. Therefore, an MST-capable Branch device shall ***not*** issue RSN message transactions.

If, for example, the link bandwidth of a downstream happens to get reduced, the MST-capable MST Branch device in MST mode shall issue a CSN message transaction for "disconnection" notification, and another CSN message transaction for "connection" notification, and reply to the ENUM_PATH_RESOURCES message transaction with the current link bandwidth capability. As noted earlier in this section, an MST-capable Branch device shall support either TPS4 or POST_LT_ADJ_REQ to avoid the fragility of the link quality that could lead to the reduction of the link rate.

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5.6.1.5 Power Management Handling

After an upstream device writes 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0), an MST-capable Branch device in MST mode shall disable the Main-Link RX of the upstream-facing DPRX while keeping the DPTX DFPs to the MST-capable downstream ports active with the transmission of VCPF symbol sequences in the allocated time slots.

The MST Branch device, upon receiving a PWR_DOWN_PHY message transaction, forwards the transaction to the downstream path and then writes 010b to the SET_POWER_STATE field in the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h, bits 2:0) of its immediate downstream devices.

The MST Branch device shall hold the VC Payload Mapping Table registers (see Section 5.5.1.1) set while in a lower power state. The MST Branch device shall clear the VC Payload Mapping Table registers only after the device receives a CLEAR_PAYLOAD_ID_TABLE message transaction, –or– when the device transitions to SST mode (as described in Section 5.6.1.1).

5.6.1.6 Multi-function MST Branch Device Enumeration

As described in Section 2.6.1.1, a multi-function MST Branch device (i.e., an MST Branch device that is capable of transport protocol conversion and/or pixel processing in the DFPs) shall enumerate the multi-function capability through a virtual DP output port (logical port) and a virtual DP peer device with DPCD registers.

5.6.1.7 Mvid/Nvid and Maud/Naud Handling

An MST-capable Branch device as the last MST Branch shall replace the Mvid/Nvid and Maud/Naud values with its own calculations and/or measurements when generating the SST output stream.

5.6.1.8 Split SDP Handling

An MST-capable Branch device that is the last MST Branch device in the path shall support handling of a split SDP.

5.6.1.9 DSC Bitstream Handling and FEC

A DSC bitstream decompression capable MST-capable DP Branch device as the last MST Branch shall have FEC decoding capability (see Section 3.5.1.5).

An MST-capable Branch device may perform DSC decompression only when it is positioned as the last MST Branch device. The intermediate MST Branch devices shall not perform DSC decompression (and thus, also no re-compression). However, the intermediate MST Branch devices shall perform FEC decoding and re-encoding when routing VC Payloads that carry DSC bitstreams. Therefore, an MST Branch device capable of FEC decoding and re-encoding shall set the FEC_READY bit in the FEC_CONFIGURATION register (DPCD Address 00120h, bit 0) to 1 when the device trains the downstream DPRX that is capable of FEC decoding.

When the upstream DPTX sets the FEC_READY bit prior to Link Training, the MST-capable DP Branch device in MST mode shall delay the Link Layer Codes forwarding to 8b/10b decoder and descrambler blocks by the same amount required for FEC decoding, even when it is not performing FEC decoding.

The last MST Branch device shall be able to regenerate a stable main video, despite the skew of the BE and BS symbol sequence locations caused by FEC parity code insertion.

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5.6.1.10 Interleaved Message Transactions Handling

As described in Section 5.4.2, an MST-capable Source device is no longer allowed to generate interleaved message transactions. However, there are MST-capable Source devices out in the field that issue interleaved message transactions. Therefore, an MST-capable Branch device shall continue being able to handle interleaved message transactions.

5.6.2 MST-Capable Branch Device with Multiple DPRX Upstream-Facing Ports

The policy of an MST Branch device that has multiple DPRX UFPs is an implementation-specific choice. For example, an MST Branch device that combines multiple SST streams into an MST stream with multiple VC Payloads may choose to either pre-allocate an equal number of time slots among the multiple SST DPRX UFPs or take the first-come, first-serve policy.

5.7 Branch-Sink Device in MST Mode

New to *DP v1.4*.

An MST-capable Branch-Sink device (e.g., a daisy-chainable MST display) shall follow the policy requirements of both an MST-capable Sink device and MST-capable Branch device, as described in Section 5.5 and Section 5.6, respectively.

5.8 Cable-Connector Assembly

This section describes the requirement for the cable-connector assembly.

5.8.1 Box-to-Box, End-User-Detachable Cable Assembly

A box-to-box, detachable DP cable assembly must support four Main-Link lanes.

Box-to-box, detachable DP cable assemblies of 2m or less must meet the high bit rate cable specification, as detailed in Section 4.

All box-to-box, detachable DP cable assemblies must meet the low bit rate cable specification, as detailed in Section 4.

Mating connectors of the box-to-box DP connection must meet the connector specification, as detailed in Section 4.

5.8.2 Embedded and Captive Cable Assembly

An embedded or captive DP cable assembly may support fewer than four Main-Link lanes as long as “sufficient” link bandwidth is provided for the design application with fewer lanes.

For embedded and captive connections, it is the responsibility of the system integrator to select the cable assembly with sufficient bandwidth capacity.

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5.8.3 Active Cable Assembly

Active cable assemblies are assemblies that contain integrated active circuitry (e.g., drivers, repeaters, or equalizers). This circuitry may be located in the Source-side plug connector, the Sink-side plug connector, or both, depending on its functionality. The Source-side and Sink-side ends of an active cable assembly generally cannot be reversed; therefore, the manufacturer must clearly identify each end (in a user's manual and/or through labeling). The transmission medium is not explicitly specified, as long as the active cable assembly meets EYE mask requirements described below. Thus, active cable assemblies may be optical, or copper using various types of bulk cable (i.e. there is no requirement to use bulk cable, as described in Section 4.1.2). Active cable assemblies may belong to types C1A, C2A, C3A, or E1A, as described in Section 4.1.1.

Mating connectors of active cable assemblies must meet the connector specification, as detailed in Section 4.

5.8.3.1 Active Cable Assembly Electrical Parameters

Active cable assemblies must support four Main-Link lanes. Active cable assemblies must support the reduced bit rate and high bit rate. An active cable assembly must have an AUX channel meeting the specifications of Section 3.4.

An active cable assembly must provide connection between the Hot Plug Detect pins at the two ends of the assembly. If the active cable assembly has plug connectors at both ends (types C1A, C2A, or C3A), there must be connections between pins CONFIG1 and CONFIG2 of the plug connectors at the two ends of the assembly, similar to the passive external cable assembly wiring shown in Figure 4-23. If the active cable assembly has a receptacle connector on one end (type E1A), then there must be no connections between the pins CONFIG1 and CONFIG2 of the connectors at the two ends of the assembly, and the pins CONFIG1 and CONFIG2 of the receptacle connector end must be shorted by a $\leq$ 100Ω resistor if the active cable consumes power at the receptacle connector end.

The inter-pair skew (time skew between two differential lanes) measurement of Main-Link lanes (0 to 3) and AUX Channel of an active cable assembly must not exceed 2UI_HBR. See DP PHY CTS Specification for detailed test method.

The output on each of the Main-Links of an active cable assembly of types C1A, C2A, or C3A must meet the EYE requirements at TP3 for RBR, as defined in Table 3-28, and at TP3_EQ for HBR, as defined in Table 3-27 and Table 3-21, respectively. Additionally, the output of each of the Main-Links of an active cable assembly of type E1A must match or be better than the EYE output requirements of the Type E1 compliance reference cable model, as described in Section 3.5.2.8, as long as the input matches the minimum stressed EYE requirements at TP2 for HBR and RBR, as defined in Table 3-25 and Table 3-26, respectively (with Voltage Swing Level 2 and Pre-emphasis Level 0). The PRBS7 pattern must be used for active cable assembly testing at HBR and RBR. The input and output EYE masks must meet the jitter requirements defined in Section 3.5.2.7.2 for each of the supported bit rates. See DP PHY CTS Specification for the detailed test method.

5.8.3.2 Active Cable Assembly DP_PWR Requirements

Active cable assemblies are devices that consume DP_PWR. An active cable assembly may use power provided by the upstream device, the downstream device, or both. Active cable assemblies must meet the requirements for devices that consume DP_PWR as detailed in Section 3.2, with the exception of the DP_PWR wire requirement of Section 3.2.2. Even though an active cable assembly may have a power wire running through the cable, there must be no connection between the DP_PWR pins of the plug connectors at the two ends of the assembly.

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A Audio Transport (Informative)

Audio-related secondary-data packets are covered in Section 2.2.5. This appendix, intended to be read along with that section, aims to add clarification to the Standard and reduce ambiguity, to improve the interoperability between audio-capable DP devices.

A.1 Audio Stream Components

An audio stream consists of the following components:

- Audio_Stream SDPs
- Audio_TimeStamp SDPs
- Audio INFOFRAME SDPs (as defined in *CEA-861-F*)
- Some portion of VB-ID

In DisplayPort Standards, all audio-related packets except VB-ID are transported as part of the secondary-data packet stream.

An Audio_Stream SDP includes audio stream itself and some attribute information such as audio coding type and channel count. Depending on the coding type of Audio_Stream SDP, it may contain status information about parameters of the audio stream. For example, the LPCM and specific compressed audio formats follow the *IEC 60958* and transfer this information in serial format, using a block of samples. (See *IEC 60958-1* and *IEC 60958-3*.) One Bit audio and DST audio coding types follow the *IEC 14496-3*, *Subpart 10*, encoding standard. These coding types stream single-bit audio samples as serial blocks (also referred to as "frames") with limited in-band meta data. Additional attribute information for these coding types (e.g., Sample Frequency) must be set in the Audio INFOFRAME SDP.

An Audio INFOFRAME SDP is used for transferring attributes of the audio stream in a separate packet. Depending on the coding type of the Audio_Stream SDP, there is some overlap between the information carried by Audio_Stream SDP and that carried by Audio INFOFRAME SDP. Whenever there is an overlap, the information carried by the Audio_Stream SDP takes precedence. The Audio INFOFRAME SDP must be referred to in limited cases and for limited information in *DP v1.4*:

- Audio channel to speaker mapping for uncompressed coding types with more than two channels (e.g., 8-channel LPCM, 8-channel One Bit, or 16- or 32-channel 3D LPCM)
- Sample Frequency for the One Bit and DST audio coding types

When 1- or 2-channel LPCM or One Bit audio is transported, *CEA-861-F* defines only a single channel-to-speaker mapping. Therefore, the transmission of an Audio INFOFRAME SDP may be omitted altogether.

An Audio_TimeStamp SDP is used for the audio clock regeneration to restore the audio master clock frequency needed for further audio processing.

Additional signals such as "audio mute" signal for disabling audio are carried in the VB-ID byte transmitted next to each BS control symbol.

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Section A.2 describes how the time slot for Audio_Stream SDP transmission must be scheduled. As far as the Audio_TimeStamp SDP and Audio INFOFRAME SDP are concerned, they must be transmitted once per frame. It is recommended that they be transmitted during the main video stream vertical blanking period.

Note: *The Audio_TimeStamp SDP may be transferred more than once per frame. It is up to each DPTX implementation to decide how many times to transfer the Audio_TimeStamp SDP.*

A.2 Association of Three SDP Types via Packet ID

The transport of an audio stream over a DP link involves transmission of three SDP types:

- Audio_Stream SDP
- Audio_TimeStamp SDP
- Audio INFOFRAME SDP

These three types of packets for a single audio stream are associated with one another by having the same Secondary-data Packet ID (00h) carried as HB0 (header byte 0) of each SDP.

A.3 Scheduling of Audio_Stream SDP Transmission

An audio stream is a continuous (i.e., isochronous) stream of audio samples, each of which may contain several channels of audio signals at a pre-defined sample frequency (fs). The sample frequency is typically in the range of 32 to 192kHz for LPCM, 3D LPCM, and non-HBR compressed audio. The sample frequency of HBR audio is within the range of 256 to 1536 kHz. The sample frequency of One Bit and DST audio is within the range of 2048 to 24576 kHz.

The transmission scheduler for an Audio_Stream SDP must wait for a time slot for audio transmission during which there are no main video stream, Main Stream Attribute Packet, and other higher priority secondary-data packets in queue. Therefore, the DPTX and DPRX are required to have some buffer space to hold the audio data while the Audio_Stream SDP is waiting for its time slot.

Figure A-1 shows how the Audio_Stream SDPs are transferred over the DP link when there is no video being transmitted. Figure A-2 shows the Audio_Stream SDP transfer with main video stream being transmitted. The transmission of Audio_Stream SDPs is withheld from BE symbol assertion till BS symbol assertion because the main video stream occupies the link during that period. Instead, Audio_Stream SDPs are transmitted between BS and BE. During the vertical blanking period of the main video stream, the Audio_Stream SDP transfer pattern will be similar to Figure A-1.

Note: *The presence or absence of main video stream is indicated in the NoVideoStream_Flag bit in the VB-ID (bit 3).*

As noted earlier, Audio_Stream SDPs may be transmitted over the link any time, as long as the time slot is available. Because the video line period of a given video format is constant throughout a video vertical frame period and so is the audio sample rate, the number of the audio samples transmitted over DP per a main video stream line period is roughly constant for the given video format. No special audio bandwidth allocation calculation is required to realize this scheduling control.

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The higher the audio data rate (in MBps) and the longer the main video line period, the larger the buffer size requirement. An implementer should determine the buffer size by determining the maximum audio data rate and the longest main video line period that need to be supported.

Figure A-1: Audio_Stream SDPs Transfer with No Video or during Video Vertical Blanking

Figure A-2: Audio_Stream SDPs Transfer with Video during Video Vertical Active Period

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A.3.1 Handling of an Audio Format Change

The transported audio format may be changed at any time. The DPTX should start sending an audio mute signal prior to the audio format change, by setting the AudioMute_Flag bit in the VB-ID (bit 4), which is sent once per main video stream line period (or once per 8192 link symbols when the main video stream is absent). An audio format change is caused by a change in any of the following:

- Between the compressed and non-compressed audio
- Between different coding types
- In the sampling rate
- In the number of channels

This signal indicates to the DPRX that the audio system is in a transient process and the audio stream may be not valid at this time. When the AudioMute_Flag bit is 1, a DPRX must disable its audio output while continuing to receive and process Audio_TimeStamp SDPs.

The DPTX should clear the AudioMute_Flag bit to 0 only after finishing the transient process at the audio source input, finishing audio clock measurement with a correct and stable value and providing information about this change to the DPRX. The DPTX should clear the audio mute signal only after transferring Audio_TimeStamp and Audio INFOFRAME SDP (if needed).

After the DPTX clears the AudioMute_Flag bit to 0, a DPRX should enable its audio output only after the regenerated audio clock becomes stable and after it has collected sufficient audio status information.

A.4 Structure of Audio_Stream SDP

DP v1.4 defines four audio coding types, as specified in the HB3 Coding Type field (bits 7:4) of an Audio_Stream SDP. These audio coding types follow *IEC 60958* or *IEC 14496-3*, *Subpart 10*, encoding standards. Additional coding types are expected to be added in the future. Therefore, a DPRX must check the Coding Type field to remain compatible with future versions/revisions of this Standard.

The HB3 ChannelCount field (bits 2:0) of an Audio_Stream SDP carries information about the count of non-3D LPCM or One Bit audio channels transmitted through a DP Main-Link. This field must have following values:

- 000 for 1-channel LPCM or One Bit audio
- 001 for 2-channel LPCM or One Bit audio
- up to 111 for 8-channel LPCM or One Bit audio

The HB2 3DChannelCount field (bits 4:0) of an Audio_Stream SDP carries information about the number of 3D LPCM audio channels transmitted over the DP Main-Link. The 3DChannelCount field must have the following values:

- 0000 to 1111 for 16-channel 3D LPCM audio
- 10000 to 11111 for 32-channel 3D LPCM audio

The audio stream payload data structure has seven configurations:

- 1- or 2-channel LPCM audio

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- 3- to 8-channel LPCM audio
- 1- or 2-channel One Bit audio
- 3- to 8-channel One Bit audio
- 1- to 16-channel 3D LPCM audio
- 17- to 32-channel 3D LPCM audio
- Compressed DST audio

An Audio_Stream SDP may have a variable payload size. At the minimum, Audio_Stream SDP size is described in the following sub-sections.

A.4.1 1- or 2-Channel Audio

The 1- or 2-channel audio layout structure is composed of four header bytes protected by four ECC parity bytes, followed by 16 payload data bytes protected by four ECC parity bytes. The 16 payload data bytes consist of four 32-bit audio channel samples. Each of the 16 payload data bytes carries two audio samples, each consisting of first and second channel audio samples. For 1-channel audio, the second channel audio sample data must be zero-padded.

A.4.2 3- to 8-Channel Audio

The 3- to 8-channel audio layout structure is composed of four header bytes protected by four ECC parity bytes, followed by two sets of 16 payload data bytes, each protected by four ECC parity bytes (resulting in 32 data bytes plus eight ECC parity bytes). As is the case with 1- or 2-channel audio, each of the 16 payload data bytes consists of four 32-bit audio samples. When the channel count is less than eight, unused audio channel sample data must be zero-padded.

The DPTX may use one common Audio_Stream SDP size for both 1- and 2-channel audio and 3- to 8-channel audio modes. In this case, the SDP payload configuration consisting of 32 data bytes plus eight ECC parity bytes (the payload configuration for 3- to 8-channel audio described in the previous paragraph) must be used.

The DPTX may concatenate multiple sets of minimum SDP payload to form a long packet that has up to 256 data bytes for 1- or 2-channel audio and 1024 data bytes in case of 3- to 8-channel audio.

Regardless of the payload size, each packet must be framed with SS and SE symbols and start with 4 header bytes protected by 4 ECC parity bytes, and then payload is present with sets of 16 bytes of data and 4 bytes of ECC parity.

Note: *All data channels within a single audio sample should be transferred in one packet. Dividing one sample into multiple Audio_Stream SDPs is* ***not*** *allowed.*

Within the 32-bit audio channel data, the least significant 24 bits carry audio sample data while the most significant eight bits carry control, status, and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All channels of one audio sample, whether used or unused, must have the same value for this flag.

For example, even when 1-channel audio is being transported and, therefore, all 24 bits of the second channel sample data are zero-padded, the SP bit of this second channel must be set to 1 whenever the SP bit of the first channel is set to 1. The same situation applies to long packets (more than 32 bytes of data) when gaps between samples can be present marked by the SP bit being cleared to 0.

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When 1- or 2-channel audio is transported, the 16 payload data bytes consist of two audio samples, as noted earlier. Of these two samples, the second sample may have the SP bits cleared to 0. For 3- to 8-channel audio transport, the SP bits must always be set to 1.

Of the remaining seven control, status, and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted only for the first and second channel data, regardless of the channel count. The PR field is omitted from the remainder of the channels.

A.4.3 1- to 2-Channel One Bit Audio

Support for One Bit audio is new to *DP v1.4*.

The 1- to 2-channel One Bit audio layout structure is identical to the 1- to 2-channel LPCM audio layout described in Section A.4.1. The two formats differ, however, in their payload bit definition. As described in Section 2.2.5.3.6, LPCM audio contains LPCM audio data in Bytes 2 through 0, with Byte 3 (bits 7:0) = (SP, R (RESERVED), PR, P, C, U, and V, respectively). One Bit audio contains single-bit audio samples in Byte 3 (bits 3:0) and Bytes 2 through 0, with Byte 3 (bits 7:4) = (SP, V, C, and F, respectively).

A.4.4 3- to 8-Channel One Bit Audio

Support for One Bit audio is new to *DP v1.4*.

The 3- to 8-channel One Bit audio layout structure is identical to the 3- to 8-channel LPCM audio layout described in Section A.4.2. The two formats differ, however, in their payload bit definition. As described in Section 2.2.5.3.6, LPCM audio contains LPCM audio data in Bytes 2 through 0, with Byte 3 (bits 7:0) = (SP, R (RESERVED), PR, P, C, U, and V, respectively). One Bit audio contains single-bit audio samples in Byte 3 (bits 3:0) and Bytes 2 through 0, with Byte 3 (bits 7:4) = (SP, V, C, and F, respectively).

One Bit audio does not have a PR field insertion requirement. Instead, the Frame Start Flag (F) control bit (bit 4 of Byte 3) must be set in the layout for all Byte 3 (28) bits at the frame boundary.

A.4.5 1- to 16-Channel 3D LPCM Audio

Support for 3D LPCM audio is new to *DP v1.4*.

The 1- to 16-channel 3D LPCM audio layout structure is composed of four header bytes that are protected by four ECC parity bytes. These parity bytes are followed by four sets of 16 payload data bytes, each of which is protected by another four ECC parity bytes. The end result is 64 data bytes plus 16 ECC parity bytes. As is the case with 3- to 8-channel LPCM audio, each of the 16 payload data bytes consists of four 32-bit audio samples. When the channel count is less than 16, unused audio channel sample data must be zero-padded.

The DPTX may concatenate multiple sets of minimum SDP payloads to form a long packet that has up to 2048 data bytes in case of 1- to 16-channel audio.

Regardless of the payload size, each packet must be framed with SS and SE symbols and start with four header bytes protected by four ECC parity bytes, and then payload is present with sets of 16 data bytes and four ECC parity bytes.

Note: *All data channels within a single audio sample should be transferred within one packet. Dividing one sample into multiple Audio_Stream SDPs is* ***not*** *allowed.*

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Within the 32-bit audio channel data, the least significant 24 bits carry audio sample data, while the most significant eight bits carry control, status, and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All channels of one audio sample, whether used or unused, must have the same state for this flag.

Of the remaining seven control, status, and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted for only the first and second channel data, regardless of the channel count. The PR field is omitted from the remainder of the channels.

A.4.6 17- to 32-Channel 3D LPCM Audio

Support for 3D LPCM audio is new to *DP v1.4*.

The 17- to 32-channel 3D LPCM audio layout structure is composed of four header bytes that are protected by four ECC parity bytes. These parity bytes are followed by eight sets of 16 payload data bytes, each of which is protected by another four ECC parity bytes. The end result is 128 data bytes plus 32 ECC parity bytes. As is the case with 3- to 8-channel LPCM audio, each of the 16 payload data bytes consist of four 32-bit audio samples. When the channel count is less than 32, unused audio channel sample data must be zero-padded.

The DPTX may concatenate multiple sets of minimum SDP payloads to form a long packet that has up to 4096 data bytes in case of 17- to 32-channel audio.

Regardless of the payload size, each packet must be framed with SS and SE symbols and start with four header bytes protected by four ECC parity bytes, and then payload is present with sets of 16 data bytes and four ECC parity bytes.

Note: *All data channels within a single audio sample should be transferred within one packet. Dividing one sample into multiple Audio_Stream SDPs is* ***not*** *allowed.*

Within the 32-bit audio channel data, the least significant 24 bits carry audio sample data, while the most significant eight bits carry control, status, and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All channels of one audio sample, whether used or unused, must have the same state for this flag.

Of the remaining seven control, status, and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted for only the first and second channel data, regardless of the channel count. The PR field is omitted from the remainder of the channels.

A.4.7 Compressed DST Audio

Support for DST audio is new to *DP v1.4*.

The DST audio layout structure is identical to the 8-channel LPCM audio layout described in Section A.4.2. The two formats differ, however, in their payload bit definition. As described in Section 2.2.5.3.6, LPCM audio contains LPCM audio data in Bytes 2 through 0, with Byte 3 (bits 7:0) = (SP, R (RESERVED), PR, P, C, U, and V, respectively). DST audio contains single-bit audio samples in Byte 3 (bits 3:0) and Bytes 2 through 0, with Byte 3 (bits 7:4) = (SP, V, C, and F, respectively).

The single bit sample data is continuous across all eight sub-layouts, for a total of 224 sample bits per DST layout. The SP bit must be set for all eight sub-layouts. Unlike multi-channel LPCM or 3D LPCM audio, channel allocation is not applicable for the DST layout, and therefore, there are no inactive sub-layouts in the DST layout.

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DST audio does not have a PR field insertion requirement. Instead, the Frame Start Flag (F) control bit (bit 4 of Byte 3) must be set in the layout for all Byte 3 (28) bits at the frame boundary.

A.5 Channel-to-Speaker Mapping

Channel position in the DP stream with more than two channels should exactly correspond to *CEA-861-F* and *CEA-861.2*. This means that gaps between channels can be present. Table A-1 shows channel-placing for the one of the possible channel mappings described in *CEA-861-F*.

Table A-1 describes transmission of 3-channel LPCM audio with CA programmed to 04h in Byte 3 of the Audio INFOFRAME SDP.

Table A-1: Channel-to-Speaker Mapping of 3-Channel Audio with CA = 04h

4-Lane Main-Link			
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**
SS	SS	SS	SS
HB0	HB1	HB2	HB3
PB0	PB1	PB2	PB3
S0_Ch1_B0	S0_Ch2_B0	00h	00h
S0_Ch1_B1	S0_Ch2_B1	00h	00h
S0_Ch1_B2	S0_Ch2_B2	00h	00h
S0_Ch1_B3	S0_Ch2_B3	80h	80h
PB4	PB5	PB6	PB7
S0_Ch5_B0	00h	00h	00h
S0_Ch5_B1	00h	00h	00h
S0_Ch5_B2	00h	00h	00h
S0_Ch5_B3	80h	80h	80h
PB8	PB9	PB10	PB11
SE	SE	SE	SE

Note: *The msb (bit 7 of Byte 3) of the 32-bit audio sample data, the SP bit, indicates if an audio sample is present.*

The channel-to-speaker mapping information is provided in an Audio INFOFRAME SDP, as described in *CEA-861-F*, *Table 31*. When 1-channel audio is transported, it must use the FL channel (Channel 1).

The channel-to-speaker mapping information for 3D LPCM audio is provided as a speaker mask or channel index setting in Audio INFOFRAME SDP Data Bytes 6 through 9, and as a channel ordering instruction (as described in *CEA-861.2*, *Section 3.6* and *Section 3.7*, respectively).

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A.6 Transfer of Sample Frequency Information

Information about audio sampling frequency is transferred in an Audio_TimeStamp SDP, which provides the audio clock frequency information (Maud and Naud), using the following formula:

$$Maud / Naud = 512 * fs / f_LS_Clk$$

where *fs* is the sampling frequency of the audio stream being transported.

In accordance with the DP Standard, this information is transferred at least once per video frame (or following 512th BS symbol when the main video stream is not present). A DPTX is allowed to transmit it more frequently if it chooses to do so. In addition, the Standard allows for the transmission of the least significant eight bits of the Maud value (Maud7:0) once per line of main video stream line and it is up to the DPRX whether to use this information.

How a DPRX regenerates the audio sampling frequency is implementation-specific and is beyond the scope of this Standard.

For example, some implementations may use the Maud and Naud values to set the initial frequency of the audio clock recovery circuit and perform the fine frequency adjustment based on the audio FIFO fill rate. With this method, a DPRX may ignore Maud7:0 data from the VB-ID packet.

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B Sink Event Notification Example (Informative)

This appendix describes a mechanism through which the SST-only mode DP Sink device can notify the DP Source device of a Sink event such as a display orientation switch between portrait and landscape. An MST Sink device connected to an MST upstream device must notify a Sink event, via SINK_EVENT_NOTIFY broadcast message transaction.

B.1 Mutual Identification by Source and Sink

Upon a Hot-Plug Event, the Source and Sink devices may identify one another by accessing the Source Device-specific field (DPCD Addresses 00300h through 003FFh; see Table 2-158) and Sink Device-specific field (DPCD Addresses 00400h through 004FFh; see Table 2-159). A Source device that is interested in enabling its "Extension" feature should write its own 24-bit IEEE_OUI (Organizational Unique ID) to DPCD Addresses 00300h through 00302h, and read the 24-bit IEEE_OUI of the Sink device from DPCD Addresses 00400h through 00402h. The Source device may optionally write and read more than three bytes of IEEE OUI to exchange further identification information (e.g., Chip ID and Revision ID). The "Extension" feature is enabled only when each device recognizes that the other device supports it.

B.2 IRQ_HPD Pulse and Sink Device-Specific IRQ

A Sink device that supports the Sink Device Event Notification feature indicates what Sink device event types are supporting by setting "Sink_Event_Type" byte(s) in the Sink Device-specific field (DPCD Addresses 00400h through 004FFh; see Table 2-159). The Source device, upon reading the Sink_Event_Type byte(s), via the AUX CH, enables certain Sink device events by writing to the "Sink_Event_Mask" byte(s) in the Sink Device-specific field. The address mapping of Sink_Event_Type byte(s) and Sink_Event_Mask byte(s) is implementation-specific.

When the selected Sink device event (e.g., the display orientation switch) occurs, the device takes the following actions:

- Programs a set of parameters to a pre-defined address range of the Sink Device-specific field
- Sets the SINK_SPECIFIC_IRQ bit in the SINK_COUNT register (DPCD Address 00201h, bit 6)
- Generates an IRQ_HPD pulse on the HPD signal line

The Source device, upon detecting the IRQ_HPD pulse, takes the following actions:

- Reads the Link/Sink Device Status field (DPCD Addresses 00200h through 002FFh; see Table 2-157) and identifies that the cause of the IRQ is Sink device-specific
- Reads a set of parameters from the pre-defined address range of the Sink Device-specific field
- Performs an operation according to the read parameters:
  - If the notified Sink device event is a display orientation change, it may change the orientation of video data it is transmitting

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C Link Quality Management (Informative)

This appendix provides guidelines for ensuring link quality, with the goal of providing minimal disruption during normal operation.

C.1 Marginal Link Quality

The link training procedure does not necessarily take sufficient time to be able to perform a full link quality analysis. The consequence is that a connection between a DPTX and DPRX may be fully trained, but operating with marginal performance. This is more likely to occur with long cables, the use of non-retiming repeaters (implementation of which is beyond the scope of this Standard), and systems and cables that for whatever reason are out of specification.

The symptoms are one or more of the following:

- No video (despite successful link training)
- Flickering/flashing video
- Display artifacts, including "sparkling" video (individual pixel errors) and line tears
- Other video distortions

C.2 Analysis

Analysis of configurations demonstrating these symptoms have shown:

- Both low bit error rates (< 10 bit errors per lane per second) and high bit error rates (1000s of bit error rates per second)
- Loss of symbol lock after successful training
- Loss of "INTERLANE_ALIGN_DONE" after training[a]
- Inconsistent training results on multiple re-plugs

Inconsistent training results can result in available bandwidth changing from one training cycle to the next. In particular, it has been observed that the available bandwidth can change over a "sleep-wake" cycle.

a. *INTERLANE_ALIGN_DONE bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively).*

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C.3 Tolerance to Bit Errors

The following guidelines are recommended for tolerance to bit errors:

- An isolated bit error should normally result in nothing worse than single pixel sparkles
- On an isolated bit error during active video, the receiver should not reset the screen
- Receivers should implement robustness supported by control packet redundancy
- Isolated bit errors should not result in any of the following:
  - Loss of symbol lock
  - Clearing of the LANE*x*_*y*_STATUS and LANE*x*_*y*_STATUS_ESI registers (DPCD Addresses 00202h and 00203h, and DPCD Addresses 0200Ch and 0200Dh, respectively)
  - Clearing of the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, respectively)
  - Re-training request
- Transmitters are not expected to monitor bit error counters

C.4 Link Re-training

On loss of clock lock, symbol lock, or inter-lane alignment, the receiver should request re-training by:

1. Clearing the INTERLANE_ALIGN_DONE bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 0, respectively).
2. Setting the LINK_STATUS_UPDATED bits in the LANE_ALIGN__STATUS_UPDATED and LANE_ALIGN__STATUS_UPDATED_ESI registers (DPCD Addresses 00204h and 0200Eh, bit 7, respectively).
3. Generating a distinct IRQ_HPD.

The receiver should avoid using the current voltage swing/pre-emphasis level/bit-rate/RX EQ setting combination in subsequent training.

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C.5 Long-term Link Quality Monitoring (Guidelines)

The receiver should monitor bit error rate for each lane but without clearing the Bit Error DPCDs.

If the bit error rate exceeds an implementation-dependent threshold (e.g., 32 errors within a 10s window), then the receiver should:

- Internally mark the current voltage swing/pre-emphasis level/bit rate/RX EQ setting as "unsupportable"
- Request re-training
- Avoid all unsupportable settings during training

The receiver should reset the "unsupportable" flags on a new connection.

A Sink device may decide to fall back to RBR. To do this it should do the following:

1. Change its capability in MAX_LINK_RATE and/or MAX_LANE_COUNT registers (DPCD Addresses 00001h and 00002h, respectively).
2. Setting the RX_CAP_CHANGED bit in the LINK_SERVICE_IRQ_VECTOR_ESI0 register (DPCD Address 02005h, bit 0).
3. Issue an IRQ_HPD.

A Source device may decide to fall back to RBR. It should do the following:

1. Allow for an initial period (e.g., 30s) during which the Sink device is using "long-term" link quality monitoring to find suitable settings.
2. On receiving a high rate of re-training requests (about two requests in 30s or higher) following training at HBR, a Source device should avoid re-training at HBR, and, instead, should try at RBR as if the RX capability is RBR.

A Source device must never attempt to send a video mode that exceeds the actual trained bandwidth, and so must be tolerant to the result of re-training being lower bandwidth than the bandwidth from prior training.

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D Electrical Specifications (Informative)

D.1 AUX Parameters

The AUX CH_EYE mask at the transmitting IC package pins (informative) is shown in Figure D-1 and its vertices are shown in Table D-1. The normative specification for the AUX CH voltage swing at the transmitting device connector pins (DFP connector pins for AUX request transaction, and UFP connector pins for AUX reply transaction) are 290mV_diff_pp min. At the transmitting IC package pins, the AUX CH voltage swing must be higher than 290mV_diff_pp to account for the voltage drop over the PCB traces.

Figure D-1: AUX CH EYE Mask at Transmitting IC Package Pins (Informative)

Table D-1: Mask Vertices for AUX CH at Transmitting IC Packages Pins (Informative)

Point	Time (UI)	Minimum Voltage Value at Six Vertices (mV)
1	0.01	0
2	0.11	Higher than 145
3	0.89	Higher than 145
4	0.99	0
5	0.89	Lower than -145
6	0.11	Lower than -145

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The AUX CH EYE mask at the receiving IC package pins and its vertices values (informative) are shown in Figure D-2 and Table D-2, respectively. The normative specification for the AUX CH voltage swing at the transmitting device connector pins (UFP connector pins for AUX request transaction, and DFP connector pins for AUX reply transaction) are 270mV_diff_pp. At the receiving IC package pins, the AUX CH voltage swing is bound to be lower than 270mV_diff_pp minimum due to the voltage drop over the PCB traces.

Figure D-2: AUX CH EYE Mask at Receiving IC Package Pins (Informative)

Table D-2: Mask Vertices for AUX CH at Receiving IC Packages Pins (Informative)

Point	Time (UI)	Minimum Voltage Value at Six Vertices (mV)
1	0.01	0
2	0.11	Lower than 135
3	0.89	Lower than 135
4	0.99	0
5	0.89	Higher than -135
6	0.11	Higher than -135

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D.2 Main-Link Parameters

Note: *Informative parameters in this section will be updated to cover HBR3 link rate range in the future version of this Standard.*

Table D-3 and Table D-4 specify informative Transmitter parameters at the silicon pads and TX pins, respectively, that are intended to serve as a reference for Transmitter design. These informative parameter values serve as a reference from which Source TP2 parameters are defined. A Source that passes compliance does not have to meet these parameter values. A Transmitter design that meets these informative parameter values may still fail compliance due to the Source device's system design. Both the Transmitter and the Source device's system should be carefully designed to ensure Source-device compliance.

Table D-3: DP Main-Link TX Silicon Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{BIAS_TX}	TX DC Bias Voltage	0		2.0	V	
$V_{TX\text{-}AC\text{-}CM_HBR_RBR}$	TX AC Common Mode Voltage			20	mV rms	Measured using an ANSI 8b/10b valid pattern with 50% transition density. Measured at supported frequencies within the frequency tolerance range. Time-domain measurement.
$V_{TX\text{-}AC\text{-}CM}$ HBR2	TX AC Common Mode Voltage			30	mV rms	
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Differential Peak-to-peak Output Voltage Swing Level 0	0.34	0.4	0.46	V	See Figure 3-12 for definition of differential voltage. Voltage Swing Level 3 for RBR and HBR is optional. For embedded connection, support of programmable voltage swing levels is optional. Voltage Swing Level 3 must be greater than Voltage Swing Level 2.
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential Peak-to-peak Output Voltage Swing Level 1	0.51	0.6	0.68	V	
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential Peak-to-peak Output Voltage Swing Level 2	0.69	0.8	0.92	V	
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level3_RBR_HBR}$	Differential Peak-to-peak Output Voltage Swing Level 3	0.85-	1.2	1.38	V	
$V_{TX\text{-}PREEMP\text{-}RATIO}$	Pre-emphasis Level 0	0.0	0.0	0.0	dB	Support for Pre-emphasis Levels 0, 1 and 2 is required. Support for Pre-emphasis Level 3 is optional. For an embedded connection, support of programmable pre-emphasis levels is optional.
	Pre-emphasis Level 1	2.8	3.5	4.2	dB	
	Pre-emphasis Level 2	4.8	6.0	7.2	dB	
	Pre-emphasis Level 3	7.5	9.5	11.4	dB	

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Table D-3: DP Main-Link TX Silicon Parameters (Informative) (Continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX\text{-}PREEMP\text{-}POST2\text{-}RATIO}$	Pre-emphasis Post Cursor2 Level 0	0.0	0.0	0.0	dB	See Figure 3-13 for definition of Post Cursor2. Support for Pre-emphasis Post Cursor2 is optional.
	Pre-emphasis Post Cursor2 Level 1	-1.1	-0.9	-0.7	dB	
	Pre-emphasis Post Cursor2 Level 2	-2.3	-1.9	-1.5	dB	
	Pre-emphasis Post Cursor2 Level 3	-3.7	-3.1	-2.5	dB	
$F_{TX\text{-}REJECTION\text{-}BW}$	Clock Jitter Rejection Bandwidth			4	MHz	Transmitter jitter must be measured at source connector pins using a signal analyzer that has a second-order PLL with closed-loop tracking bandwidth of 20MHz (for D10.2 pattern) and damping factor of 1.428.
$C_{TX\text{-}OUTPUT}$	TX Output Capacitance for Return Loss			1.5	pF	For HBR2. Represents only the effective lump capacitance seen at the package/die interface that shunts the on-die TX termination.

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Table D-4: DP Main-Link TX TP1 Package Pin Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{TX\text{-}EYE_CHIP_HBR2}$	Minimum TX EYE Width at TX package pins	0.73			UI	For HBR2 using a D10.2 pattern.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER_CHIP_HBR2}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins			0.135	UI	
$T_{TX\text{-}EYE_CHIP_HBR}$	Minimum TX EYE Width at TX package pins	0.72			UI	For HBR.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER_CHIP_HBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins			0.147	UI	
$T_{TX\text{-}EYE_CHIP_RBR}$	Minimum TX EYE Width at TX package pins	0.82			UI	For RBR.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\ CHIP_RBR}$	Maximum time between the jitter median and maximum deviation from the median at TX package pins			0.09	UI	
$T_{TX\text{-}RISE_CHIP}$, $T_{TX\text{-}FALL_CHIP}$	D+/D- TX Output Rise/Fall Time at TX package pins	50		130	ps	At 20 to 80%.
$V_{TX\text{-}DC\text{-}CM}$	TX DC Common Mode Voltage	0		2.0	V	Common mode voltage is equal to Vbias_TX voltage.
$I_{TX\text{-}SHORT}$	TX Short Circuit Current Limit			50	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{TX\text{-}DIFF}$	Differential Return Loss at 0.675GHz at TX package pins	12			dB	Straight loss line between 0.675 and 1.35GHz.
	Differential Return Loss at 1.35GHz at TX package pins	9			dB	
$L_{TX\text{-}SKEW\text{-}INTRA_PAIR\ CHIP}$	Lane Intra-pair Output Skew at TX package pins			20	ps	Applies to all supported lanes.
$T_{TX\text{-}RISE_FALL_MISMATCH_CHIPDIFF}$	Lane Intra-pair Rise-fall Time Mismatch at TX package pins.			5	%	D+ rise to D- fall mismatch and D+ fall to D- rise mismatch.

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Table D-5 through Table D-7 specify Receiver parameters at the RX pins and silicon pads that are intended to serve as a reference for Receiver design. These informative parameter values serve as a reference from which Sink TP3 parameters are defined. A Sink device that passes compliance does not have to meet these informative parameter values. A Receiver design that meets these informative parameter values may still fail compliance due to the Sink device's system design. Both the Receiver and the Sink device system should be carefully designed to ensure Sink-device compliance.

Table D-5: DP Main-Link RX TP4 Package Pin Parameters (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Peak-to-peak Input Voltage at RX package pins	120			mV	For HBR. See Figure 3-12 for definition of differential voltage.
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Peak-to-peak Input Voltage at RX package pins	40			mV	For RBR. See Figure 3-12 for definition of differential voltage.
$T_{RX\text{-}EYE_CHIP}$	Minimum Receiver EYE Width at RX package pins	0.47			UI	For HBR. $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specifies the total allowable DJ.
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}ITTER_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at RX package pins			0.265	UI	
$T_{RX\text{-}EYE_CHIP}$	Minimum Receiver EYE Width at RX package pins	0.22			UI	For RBR. $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specifies the total allowable DJ.
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}ITTER_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at RX package pins			0.39	UI	
$V_{RX\text{-}DC\text{-}CM}$	RX DC Common Mode Voltage	0		2.0	V	Common mode voltage is equal to Vbias_RX voltage.
$I_{RX\text{-}SHORT}$	RX Short Circuit Current Limit			50	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{RX\text{-}DIFF}$	Differential Return Loss at 0.675GHz at RX package pins	12			dB	Straight loss line between 0.675 and 1.35GHz.
	Differential Return Loss at 1.35GHz at RX package pins	9			dB	
$C_{RX\text{-}INPUT}$	RX Input Capacitance for Return Loss			1.1	pF	For HBR2.

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Table D-6: DP Main-Link RX Silicon Pads with HBR/RBR (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{BIAS_RX}	RX DC Bias Voltage	0		2.0	V	

Table D-7: DP Main-Link RX Silicon Pads with HBR2 (Informative)

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{BIAS_RX}	RX DC Bias Voltage	0		2.0	V	
$T_{RX-TJ_8b10b_HBR2}$	Minimum Receiver EYE Width	0.30			UI	For HBR2. Measured at $1E^{-9}$ BER using the HBR2 Compliance EYE pattern.
$T_{RX-DIFFp-p_HBR2}$	RX Differential Peak-to-Peak EYE Voltage	50			mV	For HBR2. Measured at $1E^{-9}$ BER using the HBR2 Compliance EYE pattern.

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D.3 Dual-Dirac Jitter Model[a]

It should be understood that although jitter can be described using a Dual-Dirac model, it should not be understood that the jitter in the system really is Dual-Dirac. Typically, jitter will be distributed or structured, and the Dual-Dirac description is merely the linearization of the CDF at a particular BER. It should also be understood that the use of the Dual-Dirac model here, and in the system budgeting, is only a language to help define the jitter in the system, and does not imply that this should be the normative derivation methodology for the derivation of the jitter in the system.

Three tools are needed to describe the Dual-Dirac model:

1st: The Dirac-delta function:

$$\delta(x - x_0) \equiv \begin{cases} 0, & x \neq x_0 \\ \rightarrow \infty, & x = x_0 \end{cases} \quad \text{with} \quad \int \delta(x - x_0)dx = 1$$

2nd: The RJ PDF is a Gaussian:

$$PDF_{RJ}(x) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left[-\frac{x^2}{2\sigma^2}\right]$$

3rd: The different jitter components combine through convolution:

$$\begin{aligned} \mathrm{PDF}(x) &= \mathrm{PDF}_{DJ}(x) * \mathrm{PDF}_{RJ}(x) \\ &= \int \mathrm{PDF}_{DJ}(u) * \mathrm{PDF}_{RJ}(x-u)du \end{aligned}$$

a. *Referenced and reused with permission from Ransom Stevens on "What The Dual-Dirac Model is and What it is Not," available on www.ransomstephens.com.*

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The Dual-Dirac is made up from the following elements:

$$[\delta(x-\mu_L)+\delta(x-\mu_R)] * \frac{1}{\sqrt{2\pi}\sigma}\exp\left(-\frac{x^2}{2\sigma^2}\right) = \frac{1}{\sqrt{2\pi}\sigma}\left[\exp\left(-\frac{(x-\mu_L)^2}{2\sigma^2}\right)+\exp\left(-\frac{(x-\mu_R)^2}{2\sigma^2}\right)\right]$$

Dual-Dirac DJ

$DJ(p\text{-}p) = \mu R - \mu L$

Gaussian RJ

$RJ = \sigma$

The derivation of TJ(BER) in Dual-Dirac: Generally we can define the bathtub plot.

$$\mathrm{BER}(x) = \rho_T \int_x^{\infty} \mathrm{PDF}(x')dx' + \rho_T \int_{-\infty}^{x} \mathrm{PDF}(x'-T)dx'$$

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Plug in Dual-Dirac:

$$\mathrm{BER}_{\delta\delta}(x) = \rho_T \left[\mathrm{erfc}\left(\frac{x - \mu_L}{\sqrt{2}\sigma} \right) + \mathrm{erfc}\left(\frac{(x - T) - \mu_R}{\sqrt{2}\sigma} \right) \right]$$

Evaluate the complementary error functions, erfc(x), and get:

$$TJ(BER) = 2Q_{BER} \times RJ(\delta\delta) + DJ(\delta\delta)$$

For 50% density patterns such as PRBS7 and the HBR2 compliance pattern at BER = 10^{-9}, Q_{BER} = 5.884.

The jitter model under these conditions would be:

$$11.77RJ + DJ = TJ$$

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E Scrambler C Code Reference (Informative)

The following C code provides an informative reference to the scrambler definition.

```
/*
 *  lfsr.h
 *  Scrambler
 *
 */

void resetLfsr();

void advanceLfsr();

extern unsigned short lfsr;
extern unsigned short lfsrSeed;

/*
 *  lfsr.c
 *  Scrambler
 *
 */

#include "DPScramble.h"
#include "lfsr.h"

/*
 this routine implements the serial scrambling/descrambling algorithm
in parallel form
 for the internal LFSR polynomial: X^16+x^5+x^4+x^3+1
 this advances the LFSR 8 bits every time it is called
 this requires fewer than 25 xor gates to implement (with a static
register)

 The XOR required to advance 8 bits/clock is
 bit   0   1   2   3   4   5   6   7   8   9  10  11  12  13  14  15

       8   9  10  11  12  13  14  15   0   1   2   3   4   5   6   7
                   8   9  10  11  12  13  14  15
                       8   9  10  11  12  13  14  15
                           8   9  10  11  12  13  14  15
*/

unsigned short lfsr;
unsigned short lfsrSeed;
```


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```
void resetLfsr() {
  lfsr = lfsrSeed;
}

void advanceLfsr() {

  int i;
  int bit[16];
  int bitOut[16];
  for (i=0; i<16; i++)                  // convert LFSR to bit array
for legibility
    bit[i] = (lfsr >> i) & 1;

  //  Advance the LFSR 8 serial clocks
  bitOut[ 0] = bit[ 8];
  bitOut[ 1] = bit[ 9];
  bitOut[ 2] = bit[10];
  bitOut[ 3] = bit[11] ^ bit[ 8];
  bitOut[ 4] = bit[12] ^ bit[ 9] ^ bit[ 8];
  bitOut[ 5] = bit[13] ^ bit[10] ^ bit[ 9] ^ bit[ 8];
  bitOut[ 6] = bit[14] ^ bit[11] ^ bit[10] ^ bit[ 9];
  bitOut[ 7] = bit[15] ^ bit[12] ^ bit[11] ^ bit[10];
  bitOut[ 8] = bit[ 0] ^ bit[13] ^ bit[12] ^ bit[11];
  bitOut[ 9] = bit[ 1] ^ bit[14] ^ bit[13] ^ bit[12];
  bitOut[10] = bit[ 2] ^ bit[15] ^ bit[14] ^ bit[13];
  bitOut[11] = bit[ 3]           ^ bit[15] ^ bit[14];
  bitOut[12] = bit[ 4]                     ^ bit[15];
  bitOut[13] = bit[ 5];
  bitOut[14] = bit[ 6];
  bitOut[15] = bit[ 7];

  lfsr = 0;
  for (i=0; i<16; i++)              // convert the LFSR back to an
integer
    lfsr += (bitOut[i] << i);
}

/*
 *
 *  DisplayPort Scrambler
 *
 *  Includes scrambling of DP control symbols, and conversion between
 *  DP control symbols and K codes
 *
 */

extern bool TrainingSequence;      // TRUE if in training sequence
extern bool Multistream;          // TRUE if using Multi-stream format
extern bool DP_TX;                // TRUE at DP transmitter, FALSE at
DP receiver
extern bool EnhancedFraming;       // TRUE for SST-mode connection
using Enhanced Framing
```


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```
extern int srSeq[4];


//      K-code            Single-stream Multi-stream
#define K28d0   0x11c //  SR            GP1 index 2
#define K28d1   0x13c //  CP       GP2 rsvd
#define K28d2   0x15c //  SS            GP1 index 3
#define K28d3   0x17c //  BF       GP1 index 4
#define K28d4   0x19c //  rsvd          GP2 rsvd
#define K28d5   0x1bc //  BS            GP2 SR
#define K28d6   0x1dc //  rsvd          GP1 index 5
#define K28d7   0x1fc //  rsvd          GP2 rsvd
#define K23d7   0x1f7 //  FE            GP1 index 0
#define K27d7   0x1fb //  BE            GP1 index 1
#define K29d7   0x1fd //  SE            GP1 index 6
#define K30d7   0x1fe //  FS            GP1 index 7

// Control symbols for single stream operation

enum {SR=K28d0, CP=K28d1, SS=K28d2,
      BF=K28d3, BS=K28d5, FE=K23d7, BE=K27d7, SE=K29d7, FS=K30d7 };

// Control symbols for multi stream operation

enum {MS_SR=K28d5};

extern const int scrControlToKcode[8];

void resetSRSeq();

enum MS_SR_States {MS_SR_Reset, MS_SR_Lock1, MS_SR_Lock2,
MS_SR_Locked, MS_SR_Error1, MS_SR_Error2};

int scrambleByte(int inByte);

/*
 *
 *  DisplayPort Scrambler
 *
 */

#include "DPScramble.h"
#include "lfsr.h"

/*
  this routine implements the scrambling/descrambling algorithm in
parallel form
  The data is scrambled with the top byte of the lfsr. Note that the
effect of scrambling
  in parallel form is to bit reverse the top byte of the lfsr
  data bit      7   6   5   4   3   2   1   0
  lfsr bit      8   9  10  11  12  13  14  15
```


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```
 this routine is called on the TX side to scramble the outgoing symbol
 and on the RX side to descramble the incoming symbol

 the parameter inByte is either
   a data value in the range 0 - 255
   a representation of a K-code, represented as 0x100+val
   a representation of a DP Control Symbol, represented by 0x200+index
     (applies only on the transmit/scrambling side)
   a representation of an errored symbol, represented by 0x400

 the return value is encoded similarly
   a data value in the range 0 - 255
   a representation of a K-code, represented as 0x100+val
   a representation of a DP Control Symbol, represented by 0x200+index
     (applies only on the receive/descrambling side)

 for robustness scrambler reset purposes, this function maintains the
state variable
 inEnhSRSeq between calls

*/

// the following defines the conversion between scrambled symbol index
to K code
//                                    0      1      2      3      4
5      6      7
const int scrControlToKcode[8] = { K23d7, K27d7, K28d0, K28d2, K28d3,
K28d6, K29d7, K30d7 };

int srSeq[4];
bool inEnhSRSeq;         // TRUE if have recognized the start of an
Enhanced Framing scrambler reset sequence

enum MS_SR_States MS_SR_State = MS_SR_Reset;
unsigned short int MS_SR_symbol_count = 0;  // 16 bit, wraps to zero
after counting to 65535

void resetSRSeq() {
  int i;
  for (i=0; i<4; i++)
    srSeq[i] = 0;
}


int scrambleByte(int inByte)
{

  int scrambit[16];
  int bit[16];
  int i, outbyte;
  int temp; // for debugging
```


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```
  if (inByte < 0)  // called after the end of stream has been met
    return -1;
  // on descramble at the receiver in multistream mode, convert Kcodes
in group 1 to control symbol indices

  if (Multistream && !DP_TX)
  {
    for (i=0; i<8; i++)
      if (inByte==scrControlToKcode[i])
      {
        inByte=i+0x200;
        break;
      }
  }

  for (i=0; i<16; i++) {                 // convert LFSR to bit array
for legibility
    bit[i] = (lfsr >> i) & 1;
  }

  for (i=0; i<11; i++)                   // convert byte to be
(un-)scrambled for legibility
    scrambit[i] = (inByte >> i) & 1;     // preserve Kcode and control
symbol distinctive bits

  if ((!((inByte & 0x100) == 0x100)) && // if not a Kcode,
      (!((inByte & 0x400) == 0x400)) && // and not an errored symbol
      (!(TrainingSequence == TRUE)))    // and not in the middle of
a training sequence
  {                                 // scramble or unscramble the data
    scrambit[0] ^= bit[15];       // data and multistream control
symbol bit 0
    scrambit[1] ^= bit[14];           // data and multistream control
symbol bit 1
    scrambit[2] ^= bit[13];           // data and multistream control
symbol bit 2
    scrambit[3] ^= bit[12];             // data bit 3
    scrambit[4] ^= bit[11];             // data bit 4
    scrambit[5] ^= bit[10];             // data bit 5
    scrambit[6] ^= bit[9];              // data bit 6
    scrambit[7] ^= bit[8];              // data bit 7
  }

  advanceLfsr();

  // reset scrambler at scrambler reset time

 if (Multistream)
  { // Multistream as defined in DP Standard
    MS_SR_symbol_count++;
    if (inByte == MS_SR)
```


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```
    {
      // robustness scrambler reset mechanism here, based on SR
reception
      // at the correct interval (every 65536 symbols) - see DP MST
section
      switch (MS_SR_State)
      {
        case MS_SR_Reset:
          resetLfsr();
          MS_SR_symbol_count = 0;  // reset counter on entry to Lock1
          MS_SR_State = MS_SR_Lock1;
          break;
        case MS_SR_Lock1:
          if (MS_SR_symbol_count == 0)
          {
            resetLfsr();
            MS_SR_State = MS_SR_Lock2;
          }               // else stay in this state
         MS_SR_symbol_count = 0; // reset counter on re-entry to state
          break;
        case MS_SR_Lock2:
          if (MS_SR_symbol_count == 0)
          {
            resetLfsr();
            MS_SR_State = MS_SR_Locked;
          } else {       // Invalid position for a reset symbol
           MS_SR_symbol_count = 0;  // reset counter on entry to Lock1
            MS_SR_State = MS_SR_Lock1;
          }
          break;
        case MS_SR_Locked:
          if (MS_SR_symbol_count == 0)
          {
            resetLfsr();
          } else {      // Invalid position for a reset symbol
            MS_SR_State = MS_SR_Error1;
            // don't adjust symbol count
          }
          break;
        case MS_SR_Error1:
          if (MS_SR_symbol_count == 0)
          {
            resetLfsr();
            MS_SR_State = MS_SR_Locked;
          } else {      // Invalid position for a reset symbol
            MS_SR_State = MS_SR_Error2;
            // don't adjust symbol count
          }
        case MS_SR_Error2:
          if (MS_SR_symbol_count == 0)
          {
            resetLfsr();
```


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```
            MS_SR_State = MS_SR_Locked;
          } else {      // Invalid position for a reset symbol
            MS_SR_symbol_count = 0;  // on entry to Lock1
            MS_SR_State = MS_SR_Lock1;  // to restart the sync
          }
          break;
      } // end of MS_SR robustness state machine
    } // end of processing SR
   } else
  { // Single stream
    if (EnhancedFraming) {
      if (((inByte == SR) || (inByte == CP)) || (inByte == BF) ||
inEnhSRSeq)
      {
        // robustness scrambler reset mechanism here for enhanced
framing, based on
        // detection of two correctly placed symbols in the sequence
SR+BF+BF+SR or SR+CP+CP+SR
        // note that ??+BF+BF+?? is assumed to be BS, not SR
        if ((inByte == SR) || (inByte == CP) || (inByte == BF))
          inEnhSRSeq = TRUE;
        for (i=0; i<3; i++)
          srSeq[i]=srSeq[i+1]; // shuffle up
        srSeq[3]=((inByte == SR) || (inByte == CP) || (inByte == BF))
? inByte : 0;
        if (((srSeq[0] == SR) && ((srSeq[1] == BF) || (srSeq[1] ==
CP))) ||
            ((srSeq[0] == SR) && ((srSeq[2] == BF) || (srSeq[2] ==
CP))) ||
           ((srSeq[0] == SR) && (srSeq[3] == SR))
||
            (((srSeq[1] == CP) || (srSeq[1] == BF)) && (srSeq[3] ==
SR)) ||
            (((srSeq[2] == CP) || (srSeq[2] == BF)) && (srSeq[3] ==
SR)))
        { // reset scrambler
          resetLfsr();
          resetSRSeq();
          inEnhSRSeq = FALSE;
        }
        if ((srSeq[0] == 0) && (srSeq[1] == 0) && (srSeq[2] == 0) &&
(srSeq[3] == 0))
         inEnhSRSeq = FALSE;   // must have got into this as a result
of
                               // a bit error generating an isolated
CP or SR
      } // end of robustness mechanism
    } else
    { // Default Framing
    if (inByte == SR)
      resetLfsr();
    }
```


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```
  }

  outbyte = 0;
  for (i=0; i<11; i++) {       // convert data back to an integer
    temp = scrambit[i] << i;
    outbyte += (scrambit[i] << i);
  }

  // Convert control symbol to Kcode in multistream mode at the
transmitter

  if (Multistream && DPTX && ((outbyte & 0x200) == 0x200))
    outbyte = scrControlToKcode[outbyte & 0x7];

  return outbyte;
}
```


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F Topology Management/Payload Bandwidth Management Usage Examples (Informative)

This subject matter is to be covered in *MST Use Case Example Ver.1* for informative purposes.

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G Link Management during System Initialization (Informative)

G.1 Background

Some DP Source device solutions rely heavily on an operating system video/display driver to handle many of the higher-level functions in the DP protocol.

Immediately after boot (before the operating system is loaded) and in operating system safe mode, the product-specific video driver is not loaded. In these scenarios, the Video BIOS or equivalent is used to configure the graphics outputs. However, VBIOS does not typically implement interrupt handling, and as a result it cannot respond to link state changes that occur after the BIOS was initially invoked.

Implementing BIOS exception handling causes system incompatibility issues for discrete graphics cards, so this is not a feasible long-term solution.

G.2 Problem Statements

G.2.1 Problem #1 – Sink Connected and Powered, but HPD Low

Description – If a Sink device does not keep HPD asserted at all times when powered, then the Source may not detect the Sink when the VBIOS is invoked. In this case, the Source will not enable the output in question, even if that output is available.

Solution – The DP Sink device must keep HPD asserted unless it is in the OFF state. See Section 5.2.5.

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G.2.2 Problem #2 – Sink HPD Unplug Event Followed by Plug Event

Description – If a Sink device is turned on, or is unplugged and re-plugged after a Source device is turned on and VBIOS invoked, the Source device that depends on VBIOS to do Link Training will not be able to train the link

Solution Case 1 – In this case, the DP Source can detect HPD, but can run Fast Link Training only (training without using AUX transactions).

DP Source Device

- If video needs to be transmitted, run Fast Link Training to 1-lane RBR Link Configuration, and transmit 640x480 Safe Mode over the link
  - 1-lane RBR/640x480 is supported by all DP Sink devices, and is the most likely to work without Full LT (Link Training)
  - For this to work, the solution requires the DP Sink device to support Fast Link Training anticipating 1-lane RBR link configuration

DP Sink Device

- If capable of supporting Fast Link Training (optional RX feature in DP Standard)
  - Be ready to receive Fast Link Training to 1-lane RBR link configuration and, upon LANE*x*_CR_DONE/LANE*x*_SYMBOL_LOCKED, a 640x480 video stream

This Standard:

- Defines 1-lane RBR as the "default" link configuration for both the DP Source and DP Sink devices when no "last-known-good" link configuration exists, and

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- Has no impact on operation of or interoperation with a DP Source device fielding HPD and capable of running Full Link Training

Figure G-1: Link Quality Management with Fast Link Training

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Solution Case 2: In this case, the DP Source cannot detect HPD.

DP Source Device

- If no known-good link configuration (monitor connected or powered up after DP Source is powered up) AND need to transmit video, transmit 640x480 Safe Mode over 1-lane RBR Main-Link
  - 1-lane RBR/640x480 supported by all DP Sink devices, and the most likely to work without Full LT (Link Training)
  - To avoid No Display requires DP Sink capable of receiving Main-Link signal without LT anticipating 1-lane RBR link configuration
- If cable unplugged and plugged after the link was established, DP Source will continue transmitting video over previously established link configuration
  - To avoid No Display requires DP Sink capable of receiving Main-Link signal without LT anticipating the "last-known-good" link configuration; works if the same DP Sink is plugged back

DP Sink Device

- If capable of receiving Main-Link signal without LT (RX feature not described in DP v1.1a)
  - Be ready to receive Main-Link signal either to 1-lane RBR or the last-known-good link configuration

This proposal has no impact on operation of interoperation with a DP Source device fielding HPD and capable of running Full Link Training.

Figure G-2 shows the Source-side behavior and Figure G-3 shows the Sink-side Power State machine. In this case, the Sink Power State diagram is extended by the addition of State 2S for avoiding No Display when the DP Source is not capable of fielding HPD.

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Figure G-2: Link Quality Management Source Safe Mode

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Figure G-3: DisplayPort Sink Device Power Management State Diagram with State 2S for a DP Upstream Device Not Capable of HPD Assertion Handling

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H Protocol Support for 3D Stereo Display

With 10.8Gbps over four lanes, DisplayPort provides sufficient bandwidth for transporting up to 1080p (FHD) 3D Stereo video data at 120Hz (i.e., 60Hz each for left and right frames). At 32.4Gbps over four lanes, the bandwidth is sufficient for 1080p 3D Stereo video at 240Hz (i.e., 120Hz each for left and right frames).

H.1 In-band 3D Stereo Signaling Methods

In addition, this Standard provides for two in-band mechanisms through which a Source device can specify the attribute of the 3D stereo video format it is transmitting:

- First method uses an MSA MISC1 field
- Second method uses a Secondary-Data packet, called VSC packet

A Sink device with DPCD Revision 1.2 or higher must support both methods.

H.1.1 MSA MISC1 Method

MISC1 field, bits 2:1, are defined in Table H-1.

Table H-1: MISC1 Field, bits 2:1 Definitions

Value	Definition
00	• 3D Stereo in-band signaling does not use this field; either no 3D Stereo is being transmitted or 3D Stereo is being transmitted with the VSC packet in-band signaling mechanism
01	• For progressive video, the next (upcoming) video frame is RIGHT EYE • For interlaced video, TOP field is RIGHT EYE, BOTTOM field is LEFT EYE
10	RESERVED
11	• For progressive video, the next (upcoming) frame is LEFT EYE • For interlaced video, TOP field is LEFT EYE, BOTTOM field is RIGHT EYE

H.1.2 Video_Stream_Configuration Packet Method

A DP Source device may send 3D Stereo in-band signaling using VSC Packet by clearing MSA Packet MISC1 field, bits 2:1, to 00.

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H.1.2.1 VSC Packet Header

Table H-1 describes the packet header bytes of a VSC packet.

Table H-1: Header Bytes of VSC Packet

Byte #	Bit #	Content
HB0	7:0	Secondary-data Packet ID = 0
HB1	7:0	07h
HB2	4:0	**Revision Number** 01h = VSC packet supporting 3D stereo only 02h = VSC packet supporting 3D stereo and PSR (applies to eDP Standard version 1.3 and above)
	7:5	**RESERVED** Read all 0s.
HB3	4:0	**Number of Valid Data Bytes** 01h = VSC packet supporting 3D stereo only (when HB2 = 01h) 08h = VSC packet supporting 3D stereo and PSR (when HB2 = 02h)
	7:5	**RESERVED** Read all 0s.

H.1.2.2 VSC Packet Payload

Table H-2 shows the bit definitions of Byte 0 (DB0) for a VSC Packet payload.

Table H-2: VSC Packet Payload

DB0, bits 3:0 = Stereo Interface Method Code	DB0, bits 7:4 = Stereo Interface Method Specific Parameter
0 = Non Stereo Video	Must be cleared to 0x0.
1 = Frame/Field Sequential	**Frame/Field Sequential Type** **Value 0x0:** Left and Right view indication based on MISC1 field, bits 2:1. **Value 0x1:** Right when Stereo Signal = 1 **Value 0x2:** Left when Stereo Signal = 1 All other values for this field (0x3-0xF) are reserved for future use. ***Note:*** *Stereo Signal refers to an out-of-band signaling, indicating the left and right frame and can be conveyed using VESA stereo connector or some other equivalent means.*
2 = Stacked Frame	**Stacked Frame Type** **Value 0x0:** Left view is on top and right view on bottom All other values for this field (0x1-0xF) are reserved for future use.

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Table H-2: VSC Packet Payload (Continued)

DB0, bits 3:0 = Stereo Interface Method Code	DB0, bits 7:4 = Stereo Interface Method Specific Parameter
3 = Pixel Interleaved	**Interleave Pattern Type** For interleave pattern type 1 through 4, a 2x2 pattern grid (as shown in **Figure 2**) is used to illustrate the interleaving pattern of the composited stereo frame. **Value 0x0:** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below. **Value 0x1:** Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below. **Value 0x2:** Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below.

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Table H-2: VSC Packet Payload (Continued)

DB0, bits 3:0 = Stereo Interface Method Code	DB0, bits 7:4 = Stereo Interface Method Specific Parameter
3 = Pixel Interleaved (continued)	**Value 0x3:** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below. **Value 0x4:** Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below. All other values for this field (0x5-0xF) are reserved for future use.
4 = Side-by-side	**Value 0x0:** A value of 0x0 indicate left half of the image represents left EYE view and right half represents right EYE view. **Value 0x1:** A value of 0x1 indicate left half of the image represents right EYE view and right half represents left EYE view. All other values for this field (0x2-0xF) are reserved for future use.
Values 0x5-0xF are reserved	RESERVED

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Figure H-1 shows the pixel pattern representation for the Pixel Interleaved method.

Figure H-1: Pixel Pattern Representation for Pixel Interleaved Method

Figure H-2 shows the interleave pattern corresponding to 2-way interleaved stereo, where the right image pixels are on even lines.

Figure H-2: Interleave Pattern Corresponding to 2-way Interleaved Stereo, where Right Image Pixels are on Even Lines

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Figure H-3 shows the interleave pattern corresponding to a checkerboard pattern, with alternating left and right view image pixels.

Figure H-3: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels

Figure H-4 shows side-by-side stereo format, with left view followed by right view.

Figure H-4: Side-by-Side Stereo Format with Left View Followed by Right View

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Figure H-5 shows field sequential stereo format with left view and right view indicated, via MISC1 field, bits 2:1, of the MSA packet.

Figure H-5: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 field, bits 2:1, of the MSA

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Figure H-6 shows stacked top, bottom stereo format with left view on top and right view on bottom.

Figure H-6: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom

H.2 3D Stereo Display Capability Declaration

The 3D stereo capability can be exposed in EDID and DisplayID. A 3D stereo format is usually associated with specific timing and hence it is desirable to indicate which timings support 3D stereo format and which do not. Furthermore, for a given timing that supports 3D stereo format, it is required to indicate which stereo format is supported. Both EDID and DisplayID have the ability to expose 3D stereo capability per timing, but DisplayID provides for a more-efficient and flexible format declaration.

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H.2.1 EDID 3D Stereo Display Capability Declaration

The 18-byte detailed timing descriptor has a field that provides information about stereo viewing support. The field described in Table H-3 allows a timing to be declared without any stereo 3D support or a specific stereo 3D format.

Table H-3: EDID v1.4 3D Stereo Display Capability Declaration

Byte #	# of Bytes	Bit Definitions					Detailed Timing Definitions
17	1	**7**	**6 5**	**4 3 2 1**		**0**	**Signal Interface Type:**
		0	_ _	_ _ _ _		_	Non-Interlaced (1 frame = 1 field)
		1	_ _	_ _ _ _		_	Interlaced (1 frame = 2 fields)
		_	**6 5**	**_ _ _ _**		**0**	**Stereo Viewing Support:**
			0 0	_ _ _ _		x	Normal Display – No Stereo. The value of bit 0 is "don't care"
			0 1	_ _ _ _		0	Field sequential stereo, right image when stereo sync signal = 1
			1 0	_ _ _ _		0	Field sequential stereo, left image when stereo sync signal = 1
			0 1	_ _ _ _		1	2-way interleaved stereo, right image on even lines
			1 0	_ _ _ _		1	2-way interleaved stereo, left image on even lines
			1 1	_ _ _ _		0	4-way interleaved stereo
			1 1	_ _ _ _		1	Side-by-Side interleaved stereo
		_	**_ _**	**4 3 2 1**		**_**	**Analog Sync Signal Definitions:**
				0 0 _ _		_	Analog Composite Sync:
				0 1 _ _		_	Bipolar Analog Composite Sync:
				0 _ 0 _		_	---------- Without Serrations;
				0 _ 1 _		_	---------- With Serrations (Hsync during Vsync);
				0 _ _ 0		_	---------- Sync On Green Signal only
				0 _ _ 1		_	---------- Sync On all three (RGB) video signals
		_	**_ _**	**4 3 2 1**		**_**	**Digital Sync Signal Definitions:**
				1 0 _ _		_	Digital Composite Sync:
				1 0 0 _		_	---------- Without Serrations;
				1 0 1 _		_	---------- With Serrations (Hsync during Vsync);
				1 1 _ _		_	Digital Separate Sync:
				1 1 0 _		_	---------- Vertical Sync is Negative;
				1 1 1 _		_	---------- Vertical Sync is Positive;
				1 _ _ 0		_	---------- Horizontal Sync is Negative (outside of Vsync)
				1 _ _ 1		_	---------- Horizontal Sync is Positive (outside of Vsync)

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H.2.1.1 Side-by-Side Interleaved Stereo for Horizontally and Vertically Packed Formats

In the scan-out format shown in Figure H-4 and Figure H-6, the frame contains both Left and Right EYE fields packed together side-by-side in a single frame. In the left-over-right packing, a Vertical Space Region (VSR) must separate the Left and Right EYE views. While the VSR is within the Vertical Active Region, the region must not contain active video raster, and must be equal in size to the total Vertical Blank (VBL, including vertical sync (VS), vertical front porch (VFP), and vertical back porch (VBP), and not including border). This region must be pre-encoded by the stream source transmitter into the packed buffer and may be used by a Sink device to generate timing or EYE-view control.

The formula to determine the size of the VSR is:

$$VSR = VBL = VFP + VS + VBP$$

The formula for the active Vertical Height (VA) is:

$$VA = 2 \times VEV + VSR$$

Note: *Vertical Eye View (VEV) and VSR are related to padding inside the frame raster, neither of which affects any frame. Therefore, VTOTAL, VACTIVE, and other MSA timing fields must be computed and conveyed as a normal, single-EYE-view (i.e., 2D) display.*

In a display with EDID only, the Source device may determine whether the Sink device supports use of Left-beside-Right or Left-over-Right in side-by-side by examining the display Aspect Ratio as well as the VA and active Horizontal Height (HA) fields in the EDID Display Timing Data (DTD). If the aspect ratio in EDID Bytes 15 and 16 indicates a normal 4:3 or 16:9 H vs. V ratio for the Landscape/Portrait mode, and yet the HA vs. VA indicates HA > 2x VA, this is a Left-beside-Right mode. Similarly, if the VA indicates at least twice the expected size for a given aspect ratio, it is a Left-above-Right mode.

With respect to the Addressable Image Size fields in EDID Bytes 12, 13, and 14 for the Left-beside-Right packing, the Vertical Addressable Image size is set as normal, and the Horizontal size is set to the size of one EYE view only. In the case of Left-above-Right packing, the Horizontal size is set as normal while Vertical size is set to the size of one EYE view only.

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H.2.2 DisplayID 3D Stereo Display Capability Declaration

In DisplayID, the timing option field of Type I and Type II detailed timing descriptor (shown in Table H-4) exposes the capability indicating whether the timing is displayed with no stereo, with stereo, or dynamically configured based on the content that is being shown.

Table H-4: DisplayID v1.1, 3D Stereo Display Capability Declaration

3	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Timing Options** **FLAGS**
	1	_	_	_	_	_	_	_	Preferred ”Detailed” Timing
	_	**6**	**5**	_	_	_	_	_	**3D Stereo Support** **FLAG**
	_	0	0	_	_	_	_	_	This timing is always displayed monoscopic (no stereo)
	_	0	1	_	_	_	_	_	This timing is always displayed in stereo
	_	1	0	_	_	_	_	_	This timing is displayed in mono or stereo depending on a user action (wearing the stereo glasses, etc.)
	_	1	1	_	_	_	_	_	RESERVED
	_	_	_	**4**	_	_	_	_	**Interface Frame Scanning Type** **FLAG**
	_	_	_	0	_	_	_	_	Progressive Scan Frame
	_	_	_	1	_	_	_	_	Interlaced Scan Frame
	_	_	_	_	3	_	_	_	**Reserved Bit**
	_	_	_	_	0	_	_	_	Clear to 0
	_	_	_	_	_	**2**	**1**	**0**	**Aspect Ratio**
	_	_	_	_	_	0	0	0	1:1
	_	_	_	_	_	0	0	1	5:4
	_	_	_	_	_	0	1	0	4:3
	_	_	_	_	_	0	1	1	15:9
	_	_	_	_	_	1	0	0	16:9
	_	_	_	_	_	1	0	1	16:10
	_	_	_	_	_	_	_	_	All other values are RESERVED

Apart from declaring per timing stereo 3D capability, DisplayID has a more flexible format for declaring the various 3D stereo formats. The Stereo Display Interface Data Block section of the DisplayID Standard describes the various 3D stereo formats.

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Table H-5 describes the 3D stereo formats, including the newly added Stacked Frame Stereo supported in DisplayID v1.2.

Table H-5: 3D Stereo Display Format Supported in DisplayID v1.2

Code	Interface Method
00h	Field Sequential Stereo
01h	Side-by-Side Stereo
02h	Pixel Interleaved Stereo
03h	Dual Interface, Left and Right Separate
04h	Multi-view
05h	Stacked Frame Stereo
06h through FEh	RESERVED
FFh	Proprietary

H.3 DisplayPort Stereo 3D Policy Requirements for Interoperability

This section describes the requirements of Source and Sink devices that support DP Stereo 3D. These requirements must be met to ensure 3D Stereo interoperability between 3D Stereo enabled Source and Sink devices over an open, box-to-box DP link.

H.3.1 Required Support for a DisplayPort Stereo 3D Sink Device

This section describes the requirements for a DisplayPort Stereo 3D Sink device. Support of Stereo 3D is optional for a DP Sink device.

A DP Stereo 3D Sink device must support at least one of the following display resolutions in Stereo 3D mode:

- 1920x1080
- 1600x900
- 1440x900
- 1366x768
- 1280x720

Timing requirements for the above display resolutions are described in the sections that follow. Sinks must support HBR and RBR link rates, HBR2/HBR3 support is optional. Sink devices may also support other Stereo 3D display resolutions; however, such resolutions may or may not be supported by a given Source device.

A DP Stereo 3D Sink device must support both of the following timing formats:

- Field Sequential Stereo Format, as described in Figure H-5
- Stack Frame mode, as described by Figure H-6

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H.3.1.1 Stereo 3D Sink Field Sequential Mode

A DisplayPort Stereo 3D sink must support field sequential stereo format, as described in Figure H-5. The field sequential stereo format must support at least one of the display resolutions listed in Table H-6, using RBR or HBR, with a specified pixel rate within the range indicated. The Sink will expose supported timing in the detailed timing structure. The minimum and maximum pixel rates shown in Table H-6 are derived from *CVT v1.2*:

- Minimum pixel clock frequency is the same as *CVT v1.2* reduced blanking
- Maximum pixel clock frequency is the same as *CVT v1.2* normal blanking

The minimum vertical and horizontal blanking times must be limited as follows:

- Minimum horizontal blanking will be that specified by *CVT v1.2* reduced blanking
- Minimum vertical blanking will be that specified by *CVT v1.2* reduced blanking

Table H-6: Allowed Timing Range for 3D Stereo Sink, for Field Sequential Stereo Format

Display Resolution	Vertical Blank Rate (Hz)[a]	Pixel Rate (MP/s)[b]	
		Min	Max
1920x1080	120Hz	285.5	369.5[c]
1600x900		201.25	254.25
1440x900		182.75	228.25
1366x768		148.75	185.0
1280x720		131.75	162.0

a. Vertical blanks occur for each frame, as described in Figure H-5. The 120Hz vertical blank rate provides one left and right frame pair at a 60Hz rate.

b. Minimum and maximum pixel rate values have a tolerance of ±0.5%, as per DMT v1 r13.

c. For 4-lane HBR implementations, 360MP/s is the maximum achievable pixel rate when using 24bpp. Rates beyond 360MP/s can be achieved by using 18bpp.

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H.3.1.2 Stereo 3D Sink Stacked Top, Bottom Stereo Format

A DisplayPort Stereo 3D Sink device must support stacked top, bottom stereo format (also known as stacked frame format) as described in Figure H-6. The stacked top, bottom stereo format must support at least one of the display resolutions listed in Table H-7, using RBR or HBR, with a specified pixel rate within the range indicated. The Sink device will expose supported timing in the DisplayID extension, as described in VESA DisplayID Standard, Version 1.2 or later. With the exception of the 1920x1080 24Hz format, the minimum and maximum pixel rates listed in Table H-7 are derived from *CVT v1.2*:

- Minimum pixel clock frequency is the same as *CVT v1.2* reduced blanking
- Maximum pixel clock frequency is the same as *CVT v1.2* normal blanking

The minimum vertical and horizontal blanking times must be limited as follows:

- Minimum horizontal blanking will be that specified by *CVT v1.2* reduced blanking
- Minimum vertical blanking will be that specified by *CVT v1.2* reduced blanking

Table H-7: Allowed Timing Range for 3D Stereo Sink, for Stacked Top, Bottom Stereo Format

Display Resolution	Vertical Blank Rate (Hz)[a]	Pixel Rate (MP/s)[b]	
		Min	Max
1920x1080	23.976/24	74.176	74.25
1920x1080	59.94/60	285.5	369.5[c]
1600x900	60	201.25	254.25
1440x900		182.75	228.25
1366x768		148.75	185.0
1280x720		131.75	162.0

a. *One vertical blank occurs for each left and right view pair, as described in Figure H-6. The 24Hz vertical blank rate delivers one left frame and one right frame at a 24Hz rate. The 60Hz vertical blank rate delivers one left frame and one right frame at a 60Hz rate.*
b. *Minimum and maximum pixel rate values have a tolerance of ±0.5%, as per DMT v1 r13.*
c. *For 4-lane HBR implementations, 360MP/s is the maximum achievable pixel rate when using 24bpp. Rates beyond 360MP/s can be achieved by using 18bpp.*

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H.3.2 Required Support for a DisplayPort Stereo 3D Source Device

This section describes the requirements for a DisplayPort Stereo 3D Source device. Support of 3D Stereo is optional for a DP Source device.

A DP Stereo 3D Source device must support one of the following timing formats:

- Field Sequential Stereo Format, as described in Figure H-5
- Stacked Top, Bottom Stereo Format, as described by Figure H-6

Note: *In keeping with the above stated requirements, the Source device must support 4-lane Main-Link operation up to HBR. It is optional for a DP Stereo 3D Source device to support HBR2 and HBR3.*

For a Source device that supports field sequential stereo format, the Source device must support any Sink device that meets the timing criteria described in Section H.3.1.1. The field sequential stereo format from the Source device will be identified with the MISC1 field, bits 2:1, of the MSA packet. Use of the VSC Packet is optional.

For Source device that supports stacked top, bottom stereo format, the Source device must support any Sink device that meets the timing criteria described in Section H.3.1.2. The stacked top, bottom stereo format will be identified through use of the VSC packet, and MISC1 field, bits 2:1, of the MSA packet must be cleared to 00.

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I QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

Prior to the introduction MST transport format and MST topology features in the DP Standard, each of one or multiple DP display output ports was controlled by each transmitter of a Source device (e.g., a GPU), and the status of content on each display output port was known and controlled by the GPU.

Because the GPU is typically a "licensed source component" of Content Protection (CP) technology, it has been required to robustly convey the status of the CP protocols on those output ports to content players supporting approved output protection protocols. In an MST topology, however, the routing of content streams happen outside the GPU, typically by unsecured software control through insecure Sideband MSGs over AUX CH.

I.1 Self-checking by Branch Devices

By CP license, Branch devices are likely to be required to apply a "Self-Checking" policy. Complying with the policy, Branch devices are to detect misconfigurations and apply license policy control directly, for example, by disabling an unauthenticated output port or by down sampling at the Branch device level, and reflect the success/failure to the upstream transmitter, for example, by aborting authentication upon failure.

The difficulty with Self-Checking at the Branch device level is that the policy varies among content licenses and CP technology. Some content licenses (DTCP, for example) prohibit the devices from interfering with the displaying of content (by disabling a display output port, for example), regardless if the authentication has been successfully established or not, when a "copy-always" policy is presented even when the content itself may be protected. Other licenses (AACS, for example) require the down-sampling of content when the connected display does not support the approved CP protocols.

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I.2 Merit of QUERY_STREAM_ENCRYPTION_STATUS Message Transaction

The QUERY_STREAM_ENCRYPTION_STATUS message transaction has the advantage of allowing the stream routing status to be robustly conveyed to the Source device of MST topology while keeping DisplayPort Standard agnostic of any particular CP protocol and/or policy.

CP-licensed Source component devices such as GPUs are responsible for indicating the presence of CP-capable endpoints and the Authentication/Revocation status to Content Player applications with the level of robustness required by the CP Licenses and additional API Licenses supporting Licensed Content.

As a usage model, it is desirable that the encryption state of independent output streams in an MST topology not affect the other output streams. For example, consider the scenario in which a non-CP device is hot plugged to an MST Branch device while the link driven by a Source device of the MST topology has already been authenticated and stream outputs from the Source device have been encrypted. In this usage scenario, it is desirable that the failure to authenticate a newly added, non-CP device not cause authentication to be aborted on unrelated stream outputs; such behavior would not be consistent with the behavior of a Source device outputting multiple display streams from multiple physical display output ports, or display connectors (i.e., one display stream per display connector).

Conversely, when a CP-capable device is hot plugged to an MST Branch device and authentication succeeds, the input stream to the MST Branch device may enable encryption on the specific stream routed to the newly plugged CP-capable device, and this enablement of encryption to that specific stream output should not require unrelated output streams to become also encrypted.

An MST Branch device may be considered as the collection of multiple independent virtual repeater devices. CP policy must be applied to a repeater function of each stream output. To facilitate the authentication status of a stream output as discernible from its upstream (or parent) link state, QUERY_STREAM _ENCRYPTION_STATUS message transaction provides for this information on a per stream basis with robustness to a Source device.

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I.3 QUERY_STREAM_ENCRYPTION_STATUS Message Transaction Handling in a CP Tree Topology

At any point any device is plugged in to already authenticated CP tree topology containing an MST Source device and MST devices with Branching Unit (with the one Source device being the most upstream transmitter), CONNECTION_STATUS_NOTIFY message transaction is propagated upstream all the way to the Transmitter. The device immediately upstream of the newly added device must initiate authentication with the new device. If authentication fails, it must not disable authentication on its upstream link. When a stream is added to the new device, the Source device may query the authentication status of the stream by originating QUERY_STREAM_ENCRYPTION_STATUS request message transaction.

Source device targets the QUERY_STREAM_ENCRYPTION_STATUS message transaction at the MST Branch device directly connected to the Source. MST devices with Branching Unit supporting QUERY_STREAM_ENCRYPTION_STATUS message transaction, upon receiving the message transaction, prepare the status and securely pass it to the upstream device until it reaches the Source device, upon which the Source device may enable encryption on the output stream to the newly added device, in compliance with CP license policy. The Source device shall wait for the reply of the QUERY_STREAM_ENCRYPTION_STATUS message before initiating another such message. The Source can only have one outstanding QUERY_STREAM_ENCRYPTION_STATUS message at a time.

In preparing for reply to QUERY_STREAM_ENCRYPTION_STATUS request message transaction, an MST Branch device uses the secret shared only by itself and its immediate upstream device connected via a single DP link to generate a signature. To populate the fields of the message reply, the Branch device must query the status of all connected downstream devices to which the specified Stream ID is being sent. The reply is a summary of all downstream status.

Note: *The QUERY_STREAM_ENCRYPTION_STATUS message does not affect encryption status on any other streams within the tree. However, a Branch device must re-initiate any authentication processes, as necessary, to include the latest (not stale) terms in the computation of L. This may be necessary if a link is currently in the unauthenticated state.*

I.3.1 IDs Provided by Source Device for QUERY_STREAM_ENCRYPTION_STATUS Request Message Transaction

Upon originating a QUERY_STREAM_ENCRYPTION_STATUS message transaction, the Source device must provide for the IDs listed in Table I-1.

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Table I-1: IDs Provided by Source Device for QUERY_STREAM_ENCRYPTION_STATUS Request Message Transaction

Bit #	Definition
7:0	**Stream ID** The Client (the Source device) specifies an ID of the Stream (S_id) for which Status is requested. MST Branch devices, as they forward the request message transaction, must update the Stream ID, because the Stream ID is governed by Branch Payload Bandwidth Manager of each MST Branch device and is bound to be unique on each link, as described in Section 2.6. Each MST Branch device uses the Stream ID it has received from the immediate upstream device (i.e., incoming VC Payload ID) when computing the signature as the downstream device. The MST Branch device uses the Stream ID it has updated to as it forwarded the message transaction (i.e., outgoing VC Payload ID) when computing the signature as the upstream device.
63:8	**Client ID** A 56-bit Client (the Source device) supplied nonce (Q_id), which an MST Branch device supporting QUERY_STREAM_ENCRYPTION_STATUS message transaction includes when computing the signature. The nonce is provided in Little Endian format, and must be non-repeatable (e.g., pseudo random number).
65:64	**Stream Event** 00 = CP_IRQ event generated on stream status change. Stream status is defined in Table I-2. 01 = No event generated on stream status change. 10, 11 = RESERVED for future use. The default state of this field after initial power-on is 00. If a Branch device supports the QUERY_STREAM_ENCRYPTION_STATUS method, it must support both options within this field.
66	**Stream Event Mask** 0 = Ignore Stream Event field in this message. 1 = Indicates that the Stream Event field has valid changes to be applied.
68:67	**Stream Behavior** Reflects the policy to apply to the stream contents. 00 = Force re-authentication of the parent link. 01 = Block flow of encrypted content to unauthenticated outputs (e.g., black raster). 10, 11 = RESERVED for future use. This may influence the Branch device's behavior when encrypted content (e.g., using HDCP encryption) is directed toward an unauthenticated output (e.g., not HDCP-capable, not authenticated, etc.). The default state of this field after initial power-on is 00. If a Branch device supports the QUERY_STREAM_ENCRYPTION_STATUS method, it must support both options in this field.
69	**Stream Behavior Mask** 0 = Ignore Stream Behavior field in this message. 1 = Indicates that the Stream Behavior field has valid changes to be applied.
71:70	**RESERVED for future use**

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I.3.2 Stream Status in QUERY_STREAM_ENCRYPTION_STATUS Reply Transaction

MST Branch devices must reply to QUERY_STREAM_ENCRYPTION_STATUS message transaction with the status information as shown in Table I-2.

Table I-2: Stream Status Information Replied by the Branch Device

Bit #	Definition[a]
1:0	**Stream State** This field reports the state of the stream specified in the Stream ID field of the QUERY_STREAM_ENCRYPTION_STATUS message. This field is not a summary of downstream status. It is only based on the Branch device's state which is forming the reply. 00 = Stream does not exist. The stream ID specified in the request message is not present in the Payload Allocation table. All other fields in the reply other than Signed and the Signature can be ignored. 01 = Stream Not Active. The stream exists in the Payload Allocation Table, but it is not being driven to an output port (possibly due to a POWER_DOWN_PHY request). If all downstream-facing ports (DFPs) report this status, then the Branch device must report this status in the reply. All other fields in the reply other than Signed and the Signature can be ignored. 10 = Stream Active. The stream exists and is being actively driven to an output port. 11 = RESERVED
2	**Stream Repeater Function Present** 0 = A simple Sink termination within the Branch device. For example, the Branch device has a display, and the stream terminates in this device, and is not subsequently presented on any other physical output ports on this Branch device. Physical output ports are described in Section 2.5.1. 1 = A Repeater Function is present on this stream in this Branch device. The stream is directed to one or more outputs of the Branch device
3	**Stream Encryption** 0 = Stream Encryption is Off. 1 = Stream Encryption is On (i.e., the combination of Link Encryption and VC Payload Encryption as described in ECF (Encryption Control Field) as described in Section 2.6).
4	**Stream Authentication** 0 = Stream has not completed authentication. 1 = Stream completed all parts of authentication. Indicates all the downstream Branch devices and Leaf devices connected to this stream have completed all applicable parts of authentication.
7:5	**RESERVED** Must be 0.

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Table I-2: Stream Status Information Replied by the Branch Device (Continued)

Bit #		Definition[a]
10:8		**Stream Output Sink Type** Reports the Branch Device Output connected to this stream. Stream unconnected state is indicated when all the output type bits are cleared to 0.
	8	1 = Stream is connected via a Branch Device Output to has one or more non-authenticable Legacy Devices (e.g., analog CRT, TV) devices connected.
	9	1 = Stream has one or more devices connected that do not support content protection on DP links or the QUERY_STREAM_ENCRYPTION_STATUS message. This includes DVI/ HDMI Sink devices or Sink/Repeater devices designed for DisplayPort v1.1a (or lower).
	10	1 = Stream has one or more DP MST-capable Sink/Branch devices connected that support the QUERY_STREAM_ENCRYPTION_STATUS message.
12:11		**Stream Output CP Type** Reports the type of Content Protection supported on all devices connected to this stream. This field is a bit mask. All bits that apply to the specified stream must be set appropriately. Each Branch device must include its own capabilities, as well as the capabilities reported from downstream devices, in the reply.
	11	1 = HDCP 1.x (no 2.x support) devices connected to the stream.
	12	1 = HDCP 2.x capable devices attached to the stream.
14:13		**RESERVED** Must be cleared to 0.
15		**Signed** 0 = Signature L' is not provided. 1 = Signature L' is provided.
23:16		**Stream ID** The Stream ID of the stream for which status is being reported. This should match the Stream ID contained in the QUERY_STREAM_ENCRYPTION_STATUS request message.

a. Stream refers to VC Payload.

I.3.3 Stream Status Signature in QUERY_STREAM_ENCRYPTION_STATUS Reply Message Transaction

MST Branch devices that support QUERY_STREAM_ENCRYPTION_STATUS message transactions are required to assemble the signature together with the status, using the format shown in Table I-3.

Table I-3: Stream Status Signature

Bytes	Definitions
19:0	**Stream State Signature L'** The SHA-1 signature of the message digest, Presented in Little Endian format: *Stream-Status* | *Q_id* | *S_id* | *Link_id* | *Link_Pk* | *Link_S* | *Link_s*

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I.3.4 Usage of Sink Type in Stream Status by a Source Device

The purpose of the Stream Sink Type in the Status Information of a QUERY_STREAM_ENCRYPTION_STATUS reply message transaction is to allow a Source device to identify whether the connected device is a simple DVI/HDMI, SST-mode Sink device, or Repeater device, or an MST device. In cases where the stream is cloned onto more than one Branch device output, the type field present is a bitmask of all the connected types.

I.3.5 Status Query

The Source device may use QUERY_STREAM_ENCRYPTION_STATUS message transaction to query the downstream status for a particular stream (i.e., VC Payload). Every query is initiated with a 64-bit unique ID which is a 56-bit query nonce (Q_Id) and 8-bit Stream ID (S_Id). The downstream MST Branch device forwards the request message transaction to its next immediate downstream device after having updated the Stream_ID to the outgoing VC Payload ID it has assigned (as described in Section 2.6).

The general equation for computing the 20-Byte Signature, L, for a Simple Sink device is as follows:

$$L' = SHA\text{-}1(Stream\text{-}Status \mid Q_id \mid S_id \mid Link_id \mid Link_Pk \mid Link_s)$$

The general equation for Sink devices with one or more Repeater functions:

$$L' = SHA\text{-}1(Stream\text{-}Status \mid Q_id \mid S_id \mid Link_id \mid Link_Pk \mid Link_S \mid Link_s)$$

Table I-4 lists the values computed by the Branch device.

Table I-4: Branch Device Status Query Computed Values

Value	Description
Stream-Status (16 bits)	Branch device determined status value as defined above.
Q_id (56 bits)	Client (Source device) supplied nonce, which the Branch device includes in computing the signature.
S_id (8 bits)	Client specifies an ID of the Stream for which Status is requested; the downstream MST Branch device updates the S_id to the outgoing VC Payload ID it has assigned to the stream.
Link_id	Link session identifier, a nonce that was generated when link encryption was first initiated.
Link_Pk	Public key of the Sink device receiver on the link.
Link_S	Hash-signature of all the authenticated Sink devices connected to this Branch device, if this Branch device includes any repeater functions (as indicated by Status bit 2).
Link_s	Secret link value, which is held confidential and not available except as derived internally by transmitter and receiver.

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Figure I-1 through Figure I-3 illustrate how QUERY_STREAM_ENCRYPTION_STATUS message transactions are forwarded and executed in various CP topologies.

Figure I-1: QUERY_STREAM_ENCRYPTION _STATUS Message Transaction Execution when Source Device Is Directly Connected to MST Sink Device

When a Source device is connected to a Sink device via MST Branch device(s), the Source device targets the QUERY_STREAM_ENCRYPTION_STATUS request message transaction at the MST Branch device (Repeater B in Figure I-2) directly connected to the Source. Each Branch will generate its own QUERY_STREAM_ENCRYPTION_STATUS messages downstream until the status request reaches the last Branch device. As replies are generated, the upstream device (Repeater C) generates L and verifies it against the returned L'. If Repeater C has multiple DFPs (to Repeater D and Repeater E in Figure I-2), the Repeater C performs the L-to-L' verification on all the DFPs. If that status signature verification passes, new status is prepared with its own status and a new L' is calculated to respond to the query from the upstream device (between Repeater B and Repeater C in Figure I-2). The upstream device repeats the process until it reaches the Source device.

Figure I-2: QUERY_STREAM_ENCRYPTION _STATUS Message Transaction Forwarding and Execution when Source Device Is Connected to Sink Device via MST Branch Devices

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At each level, the Encryption Status and Authentication Status in Stream Status reported upwards must be the AND of all of the Branch device output ports connected to this stream, and the status provided from the immediate downstream device. If Repeater C authenticated the output port connected to Repeater D, but if any of the stream's output ports on Repeater D were not authenticated, then the collective Stream Status presented by Repeater C to Repeater B must reflect that the stream is not authenticated. By this means, the Stream Status replied to the Source device is always the lowest common denominator of the topology.

If at any stage the L verification fails, the device may continue to provide the Stream Status, but must not provide the query signature (L') upstream (Figure I-3). QUERY_STREAM_ENCRYPTION _STATUS message transaction will then eventually time out or will be replied with a null signature (as indicated by Bit 15 of the Status). Failure to provide the Status Query L' must be considered as Authentication failure. Moreover, upstream devices must also fail to sign their status, and similarly fail to provide status signature L' to their upstream devices.

Figure I-3: QUERY_STREAM_ENCRYPTION _STATUS Message Transaction Forwarding and Execution when L-to-L' Verification Error Is Present

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I.3.6 Application of QUERY_STREAM_ENCRYPTION _STATUS Message Transaction to HDCP

When QUERY_STREAM_ENCRYPTION_STATUS message transaction is applied to an HDCP tree topology, it is anticipated that the usage of this message transaction does not affect the encryption status on any other streams in the HDCP tree topology.

When a new device is plugged to an HDCP tree, it is anticipated that the Branch device to the DFP of which a new device is hot plugged will cause at least the first part of the authentication with the new device, as long as such behavior is compliant with HDCP specification and license policy. Furthermore, if a change in the Branch device's physical topology has not already resulted in fresh Stream Status values, the Branch device is expected to initiate any relevant portions of authentication upon receiving the QUERY_STREAM _ENCRYPTION_STATUS request message transaction as necessary to ensure the latest Bksv-List is collected, and re-computing a fresh (Link_S) signature V' (and asserting READY as appropriate) for inclusion in the Stream Status result L', as long as such a behavior of the Branch device is done in a manner compliant with HDCP specification and license policy.

As for the Authentication Status in Stream Status, the bit 4 equal to 1 indicates the passing of An and Aksv, and generation and checking of R_0, and as well as the collection and checking of the KSV lists and signature, as defined in HDCP authentication parts 1, 2, and 3.

As for the Stream State Signature generation, the following values must be used for HDCP:

- Link-id (64 bits) = An
- Link_Pk (40 bits) = Link Public Key = Bksv
- Link_s (64 bits) = Link Secret = M_0
- Link_S (160 bits) = Link Signature = V'

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J 16-Bit Frame CRC Example

The CRC calculation is performed on the entire frame. A 16-bit CRC is generated per color component, based on the following polynomial:

$$f(x) = x16 + x15 + x2 + 1$$

The CRC calculation is only performed on active pixels. The msb is shifted in first. For any color format that is less than 16 bits per component, the lsb is zero-padded.

The following is an example of a parallel 16-bit CRC generation for one color component.

```
module crc16_16(
// Outputs
dout,

// Inputs
reset, clk, d, enable
);

// Inputs and Outputs
input  [ 15: 0] d;
input  clk;
input  reset;
input  enable;
output [ 15: 0] dout;

// Internal Signals
reg    [ 15: 0] b;
wire   [ 15: 0] dout;

// Internal Assignments
assign dout = b;
// Define LFSR
always @(posedge clk)
begin
      if (reset)
      begin
            b <= 16'h0;
      end
      else
      begin
            if (enable)
             begin
b[15] <= b[ 0] ^ b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^
b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[14] ^ b[15] ^
d[ 0] ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^
d[ 8] ^ d[ 9] ^ d[10] ^ d[11] ^ d[12] ^ d[14] ^ d[15];

b[14] <= b[12] ^ b[13] ^ d[12] ^ d[13];
```


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```
b[13] <= b[11] ^ b[12] ^ d[11] ^ d[12];
b[12] <= b[10] ^ b[11] ^ d[10] ^ d[11];
b[11] <= b[ 9] ^ b[10] ^ d[ 9] ^ d[10];
b[10] <= b[ 8] ^ b[ 9] ^ d[ 8] ^ d[ 9];
b[ 9] <= b[ 7] ^ b[ 8] ^ d[ 7] ^ d[ 8];
b[ 8] <= b[ 6] ^ b[ 7] ^ d[ 6] ^ d[ 7];
b[ 7] <= b[ 5] ^ b[ 6] ^ d[ 5] ^ d[ 6];
b[ 6] <= b[ 4] ^ b[ 5] ^ d[ 4] ^ d[ 5];
b[ 5] <= b[ 3] ^ b[ 4] ^ d[ 3] ^ d[ 4];
b[ 4] <= b[ 2] ^ b[ 3] ^ d[ 2] ^ d[ 3];
b[ 3] <= b[ 1] ^ b[ 2] ^ b[15] ^ d[ 1] ^ d[ 2] ^ d[15];
b[ 2] <= b[ 0] ^ b[ 1] ^ b[14] ^ d[ 0] ^ d[ 1] ^ d[14];

b[ 1] <= b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^ b[ 7] ^
b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[13] ^ b[14] ^ d[ 1] ^
d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^ d[ 8] ^ d[ 9] ^
d[10] ^ d[11] ^ d[12] ^ d[13] ^ d[14];

b[ 0] <= b[ 0] ^ b[ 1] ^ b[ 2] ^ b[ 3] ^ b[ 4] ^ b[ 5] ^ b[ 6] ^
b[ 7] ^ b[ 8] ^ b[ 9] ^ b[10] ^ b[11] ^ b[12] ^ b[13] ^ b[15] ^
d[ 0] ^ d[ 1] ^ d[ 2] ^ d[ 3] ^ d[ 4] ^ d[ 5] ^ d[ 6] ^ d[ 7] ^
d[ 8] ^ d[ 9] ^ d[10] ^ d[11] ^ d[12] ^ d[13] ^ d[15];
            end
      end
end
endmodule
```


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K Adaptive-Sync

New to *DP v1.4*.

For many years, the display industry has operated with the understanding that displays run at a fixed refresh rate (e.g., 60Hz). This is in contrast with the fact that there are many types of content that can be sent to a display, each with its own unique, and sometimes varying, frame rate. When the display refresh rate is not synchronized to the content frame rate, the user can experience undesirable effects (e.g., tearing and stutter). For mobile applications (e.g., table and notebook PC), unnecessarily high display refresh rates for static and video content can increase power draw and reduce battery life. These factors have given rise to the need for a technology that seamlessly allows the display's refresh rate to adapt to the content's frame rate. VESA has developed an industry standard that enables interoperable, variable refresh rate capabilities over DP and Embedded DisplayPort (eDP) interfaces, referred to as "Adaptive-Sync." Adaptive-Sync, an optional feature supported by *DP v1.4* (and higher), leverages the Ignore MSA option described in Section 2.2.4.1.1 to enable Source and Sink devices to seamlessly and dynamically vary the refresh rate.

This appendix describes the Source and Sink device requirements and recommendations for Adaptive-Sync:

- Source and Sink devices shall support the Ignore MSA option, as described in Section 2.2.4.1.1 and *eDP v1.4b*, *Section 3.7*.
- Source device shall pass the test cases of the Source device test procedures described in *DP EDID CTS v1.2*, *Section 3.3.5*.
- Sink device shall pass the test cases of the Sink device test procedures described in *DP EDID CTS v1.2*, *Section 4.8*.
    - As part of this test, the Sink device is required to render the Source device frame within a fraction of a frame time immediately upon receiving the frame from the Source device, without delay.
- Sink devices that support Adaptive-Sync are required to indicate support for the Adaptive-Sync range in EDID, and the Ignore MSA option in DPCD.
- Source devices that support Adaptive-Sync are required to read the Sink device DPCD capability and Adaptive-Sync range capability from EDID and ensure that the Source device frame duration falls within the range.
- If audio support is reported in EDID along with Adaptive-Sync capability, the Sink device shall support audio rendering while the Ignore MSA option is enabled.

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- If multiple resolution support is reported in EDID, for all resolutions that are within the Adaptive-Sync range of the stream Sink device, a Sink device shall support operation of the resolution in Normal mode, both with and without the Ignore MSA option enabled.
  - For example, if a Sink device reports an Adaptive-Sync vertical refresh rate range of 30 to 100Hz by declaring it in the Display Range Limit Descriptor, timings reported in EDID's established, standard and detailed DisplayID timing blocks that lie within the range (i.e., vertical refresh rate for those timings within the 30 to 100Hz range), shall be able to support the Adaptive-Sync range from the nominal vertical refresh rate defined by the timing in EDID to the minimum supported range.

Note: *Timing exposed in EDID is usually optimized for bandwidth by using minimum horizontal and vertical blank (i.e., using CVT v1.2 timing standards). To achieve a lower refresh rate at same pixel and line rate, vertical blank is extended.*

  - If timing exposed in EDID is beyond the Sink device's Adaptive-Sync range (i.e., 24Hz timing for the above example), the Source device shall not enable the Ignore MSA option on that timing.
  - For a timing that can be supported both with the Ignore MSA option and conventional non-ignore MSA operation, it is the Source device's responsibility to determine which operation mode it enables, based on the use cases that the Source device supports.

Adaptive-Sync Refresh rate range and use cases for which Adaptive-Sync operation is enabled is beyond the scope of this Standard and is Source device policy-dependent.

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L Information and Examples for DSC Slice Per Line Calculations

New to *DP v1.4*.

L.1 Derivation of Slice Count Requirements

The normative slices per Display Line listed in Table 2-141 are derived from the following calculations:

- Total pixel throughput rate (display peak pixel rate (ppr)), in units of MP/s, is the cumulative rate for all streams that feed a single display
- DSC engines are required to support, at a minimum, one of two maximum encoder throughput rates, depending on the display's ppr:
  - **Throughput rates less than or equal to 2720MP/s** – Use 340MP/s
  - **Throughput rates greater than 2720MP/s** – Use 400MP/s (assumes that these high-end displays will be built with a faster processor)
- Formula used:
  - Final slice count shall be rounded up to one of the following values – 1, 2, 4, 8, 12, 16, 20, or 24
  - **If ppr is less than or equal to 2720** – Slice count = ppr / 340 (round up if needed)
  - **If ppr is greater than 2720** – Slice count = ppr / 400 (round up if needed)

Note: *See Table 2-141 and information related to the table in Section 2.7.3. Section 2.7.3 addresses a maximum slice width, as well as a special case for display modes that support only native 4:2:0 mode (DSC v1.2 or higher).*

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L.2 Usage Example

The example provided here assumes a maximum slice width (MaxSliceWidth) of 2560 pixels. If the DSC Maximum Slice Width register (DPCD Address 0006Ch) allows for a larger slice width, the DP DSC Source device can optionally use that width instead of the 2560 value.

For a display that supports the modes listed in Table L-1, the display shall support the number of slices indicated in Table 2-141 for each mode that it advertises.

Table L-1: Sample Display Configurations

Sample Configuration	Resolution	Refresh Rate (Hz)	Mode[a]	Peak Pixel Rate (ppr) (MP/s)[b]
a	8Kx4K	120	4:2:0	~ 4260
b	8Kx4K	60	4:4:4, 4:2:0	~ 2100
c	5Kx2880	60	4:4:4, 4:2:0	~ 940
d	5Kx2880	15	4:4:4, 4:2:0	~ 230
e	4Kx2K	60	4:4:4, 4:2:0	~ 525
f	4Kx2K	30	4:4:4	~ 260

a. 4:2:0 mode is supported only by DSC v1.2 (or higher).
b. Actual ppr values will vary; numbers used here are for illustrative purposes only.

Therefore, walking through this example:

a **8Kx4K / 120Hz / 4:2:0, ppr ~ 4260MP/s**

Because this mode is available only in 4:2:0, assuming that it can use native 4:2:0 mode (*DSC v1.2* or higher), it can use the "Alternative Slice per Display Line Requirement" column in Table 2-141, which allows 8 slices per line.

Dividing the line width (7680 pixels) by 8 slices results in a slice width of 960 pixels, which is less than 2560 pixels = okay.

Note that if this display also offered the resolution/refresh rate in anything other than 4:2:0 it would then have to support 12 slices.

b **8Kx4K / 60Hz / 4:4:4 and 4:2:0, ppr ~ 2100MP/s**

Because this display mode supports a mode other than 4:2:0, it shall use the value from Table 2-141 with no modifications. At 2100MP/s, Table 2-141 indicates that the display shall support 8 slices per pixel-line, which is an allowed value.

Dividing the line width (7680 pixels) by 8 slices results in a slice width of 960 pixels, which is less than 2560 pixels = okay.

c 5Kx2880 / 60Hz / 4:4:4 and 4:2:0, ppr ~ 940MP/s

Because this display mode supports a mode other than 4:2:0, it shall use the value from Table 2-141 with no modifications. At 940MP/s, Table 2-141 indicates that the display shall support 4 slices per pixel-line, which is an allowed value.

Dividing the line width (5120 pixels) by 4 slices results in a slice width of 1280 pixels, which is less than 2560 pixels = okay.

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d 5Kx2880 / 15Hz / 4:4:4 and 4:2:0, ppr ~ 230MP/s

Because this display mode supports a mode other than 4:2:0, it shall use the value from Table 2-141 with no modifications. At 230MP/s, Table 2-141 indicates that the display shall support 1 slice per pixel-line, which is an allowed value.

Dividing the line width (5120 pixels) by 1 slice results in a slice width of 5120 pixels. This is greater than the maximum of 2560 pixels. Therefore, the next higher slice count from the acceptable values shall be used. In this case, it is 2 slices per line which results in a slice width of 2560 pixels = okay.

e 4Kx2K / 60Hz / 4:4:4 and 4:2:0, ppr ~ 525MP/s

Because this display mode supports a mode other than 4:2:0, it shall use the value from Table 2-141 with no modifications. At 525MP/s, Table 2-141 indicates that the display shall support 2 slices per pixel-line, which is an allowed value.

Dividing the line width (3840 pixels) by 2 slices results in a slice width of 1920 pixels which is less than 2560 pixels = okay.

f **4Kx2K / 30Hz / 4:4:4 and 4:2:0, ppr ~ 260MP/s**

Because this display mode supports a mode other than 4:2:0, it shall use the value from Table 2-141 with no modifications. At 260MP/s, Table 2-141 indicates that the display shall support 1 slice per pixel-line, which is an allowed value.

Dividing the line width (3840 pixels) by 1 slice results in a slice width of 3840 pixels. This is greater than the maximum of 2560 pixels. Therefore, the next higher slice count from the acceptable values shall be used. In this case, it is 2 slices per line which results in a slice width of 1920 pixels = okay.

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M Main Contributor History (Previous Versions)

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