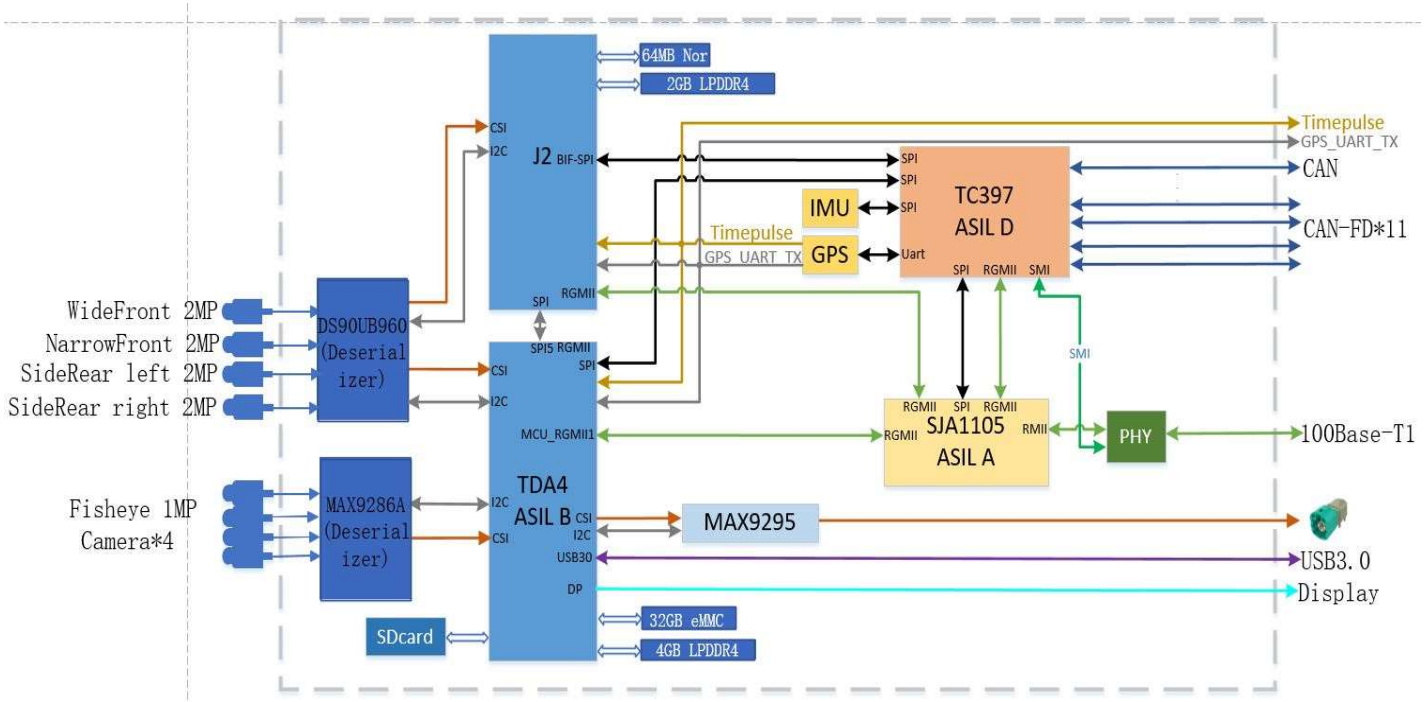
P01-system block
P02_Main_Power
P03-TDA 3V3 power
P04-TDA0 SOC General
P05-TDA0 MCU RGMII
P06-TDA0 SOC USB0/1
P07-TDA0 DSI CSI
P08-TDA0 DP port
P09-TDA0 Serdes
P10-TDA0 Serdes CLK
P11-TDA0 LPDDR4
P12-TDA0 SOC power1
P13-TDA0 SOC power2
P14-TDA0 SOC power3
P15-TDA0 MCU General
P16-TDA0 SOC GND
P17-TDA0 eMMC SD
P18-TDA0 SOC RGMII
P19-TDA0 Debug uart
P20-TDA0 SoM PMIC A
P21-TDA0 SoM PMIC B
P22_TDA0 PWR_GMSL_9286_TDA0
P23_TDA0 MIPI_GMSL_9286_TDA0
P24_TDA0 MIPI_GMSL2_9296_TDA0
P25_CAN_CONN
P26-TC397 Power
P27-TC397 Peripherals
P28-TC397 CAN/GPIO
P29-TC397 Debug
P30-IMU
P31-GPS
P32-Eth switch
P33_TJA1102S
P34_J2_LPDDR4
P35_J2_SYS
P36-J2-Video
P37_J2_Peripheral
P38_J2_Power&GND
P39_J2_Power for J2
P40-DS90UB960



HoloMatic 禾多科技		
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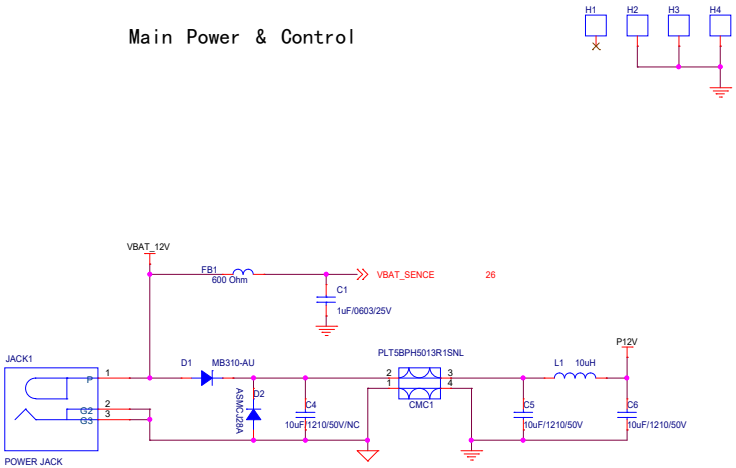
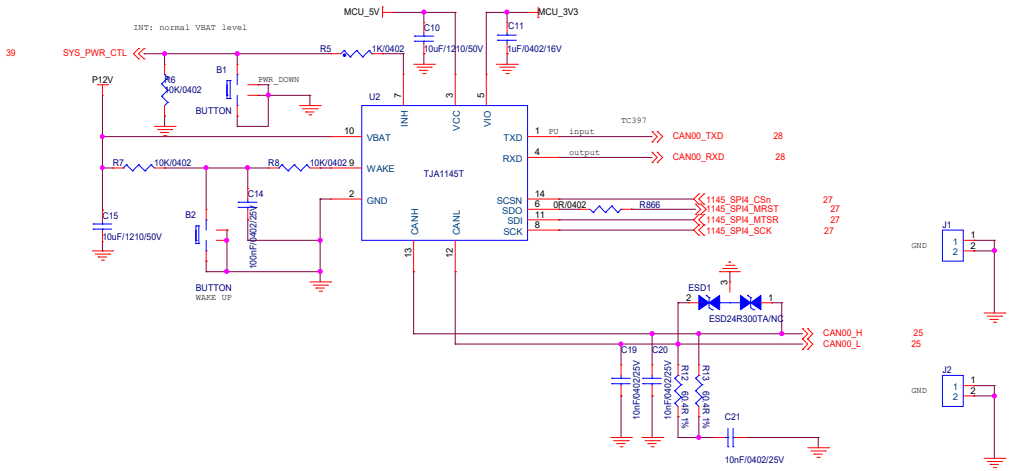
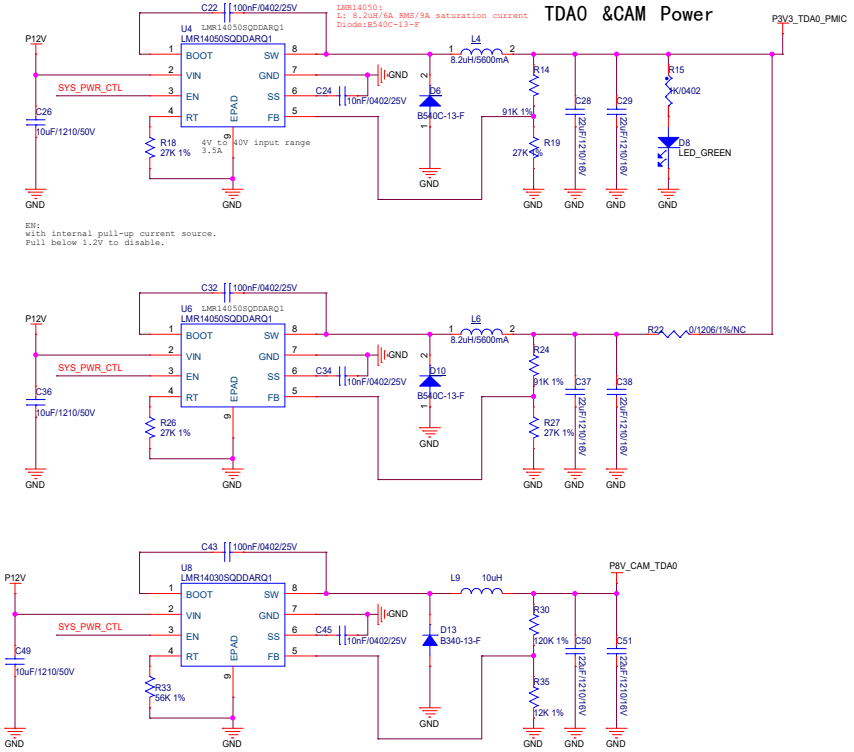
Size: A3	Document Number: P01-system block	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 1 of 40	

Main Power & Control

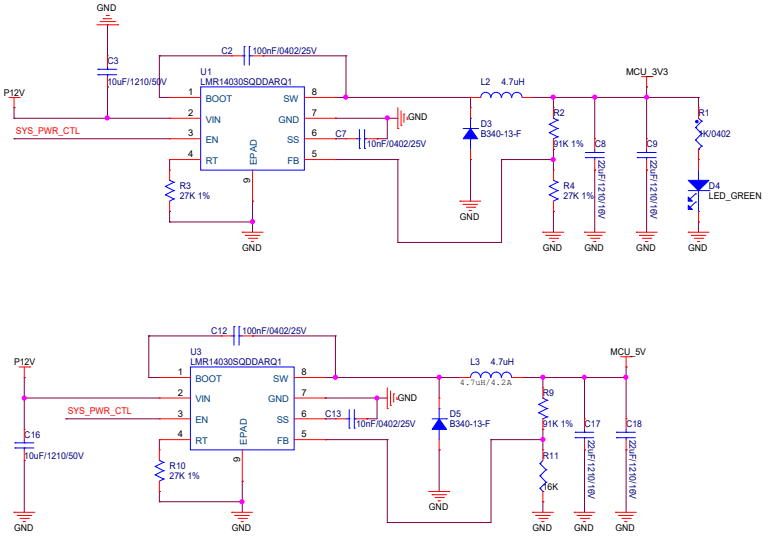




TDA0 &CAM Power



TC397 Power



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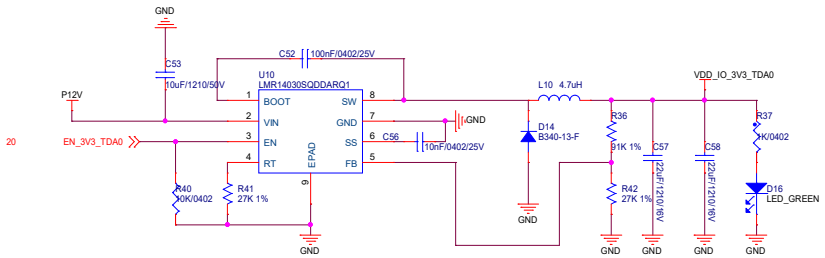
Size: C	Document Number: P02_Main_Power	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 2 of 40	



HoloMatic 禾多科技	
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Size: C	Document Number: P03-TDA 3V3 power
Rev	V4.0
Date: Thursday, September 17, 2020	Sheet 3 of 40

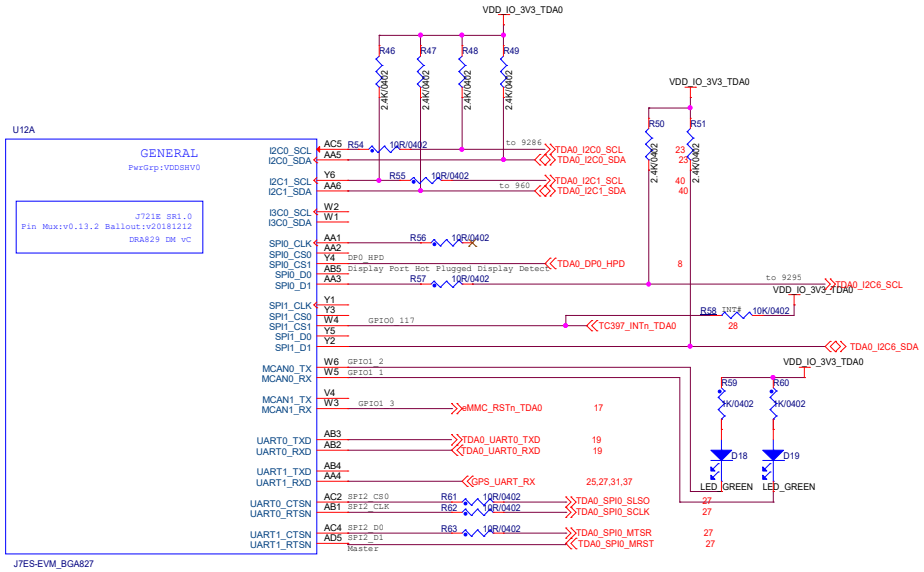
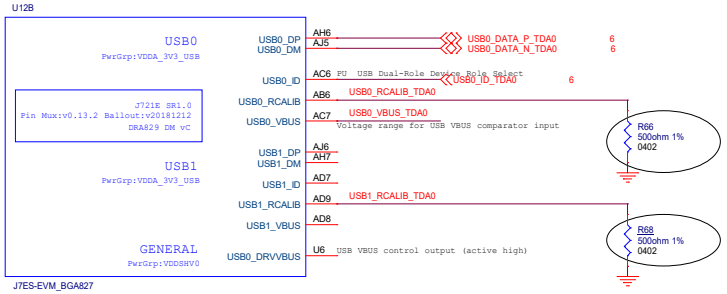


Table 5-1. Speed Grade Maximum Frequency

DEVICE	MAXIMUM FREQUENCY (MHz)									
	MPU	C66x DSP	C7x DSP	MCU	IPU	GPU	CBASS0	ICSSG	DMSC	LPDDR4
TDA4VMxP	1800	1350	1000	1000	1000	750	500	333	333	1600 (DDR-3200) / 1866 (DDR-3733)(1)



USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS

HoloMatic 禾多科技	
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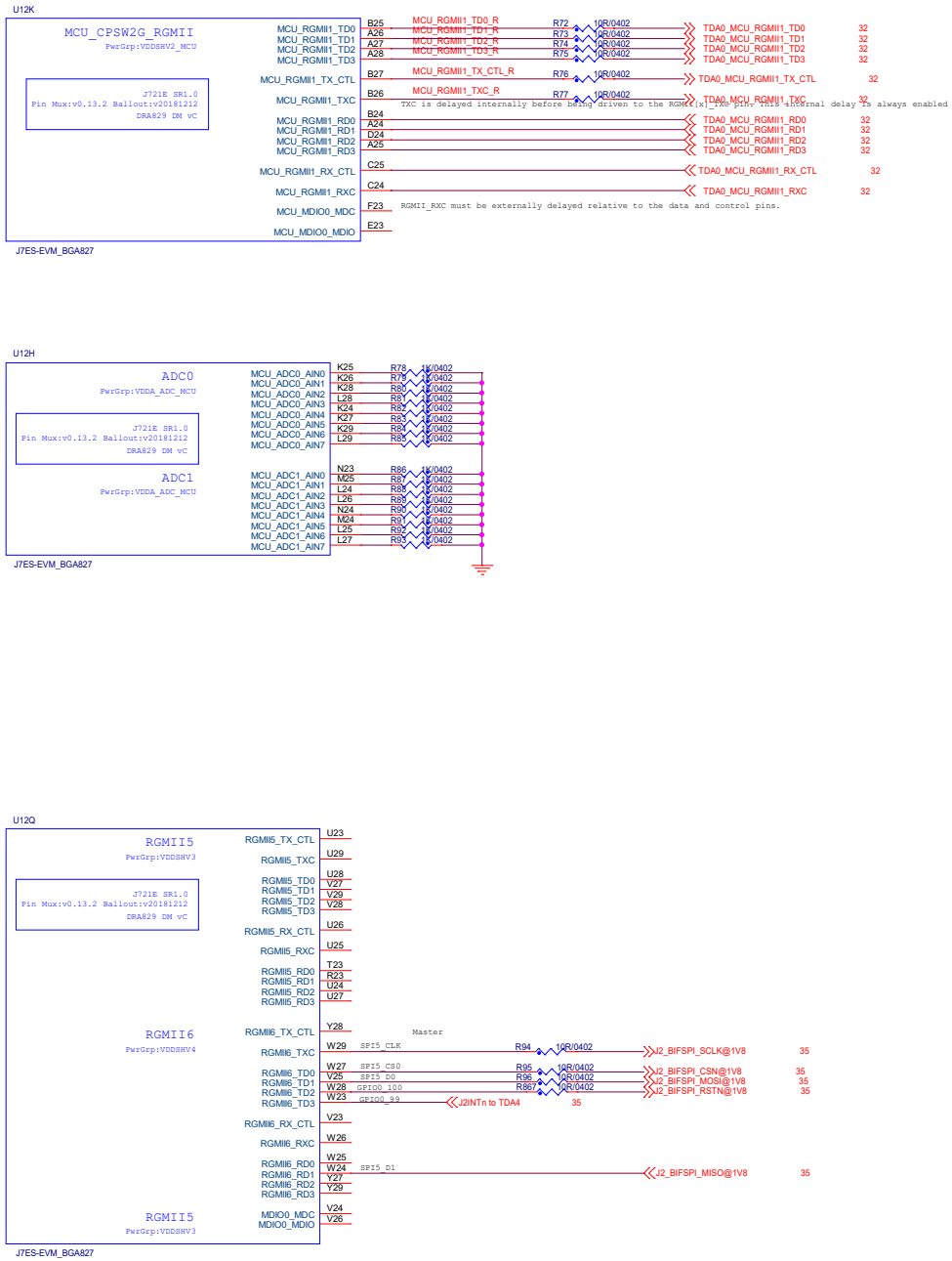
Size C	Document Number P04-TDA0 SOC General — Rev V4.0
Date: Thursday, September 17, 2020	Sheet 4 of 40



HoloMatic 禾多科技			
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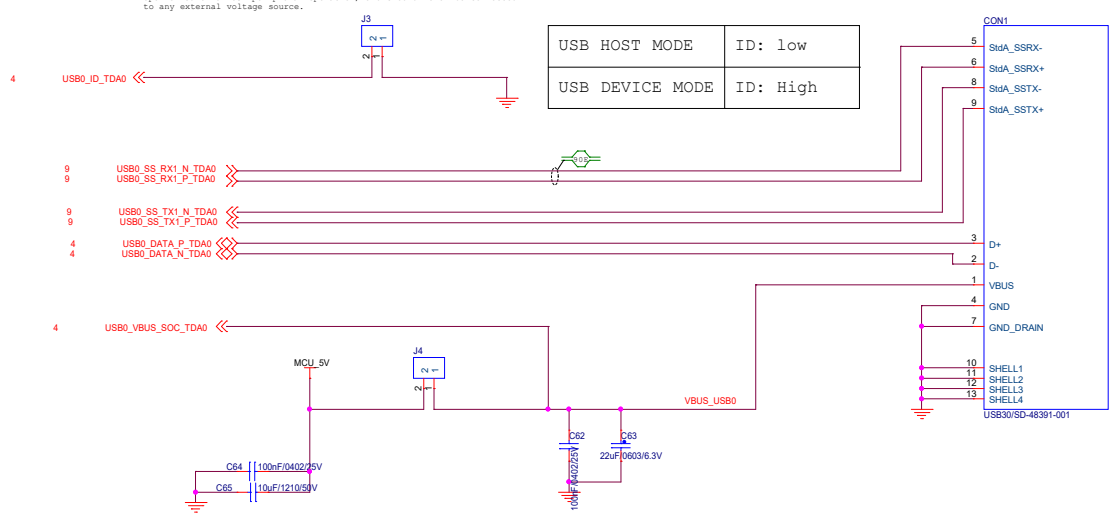
Size C	Document Number P05-TDA0 MCU RGMII		Rev V4.0
Date: Thursday, September 17, 2020	Sheet 5 of 40		



HoloMatic 禾多科技	
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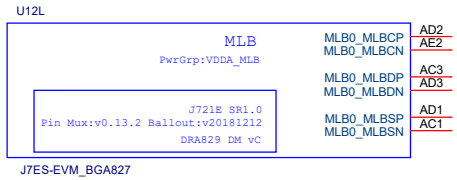
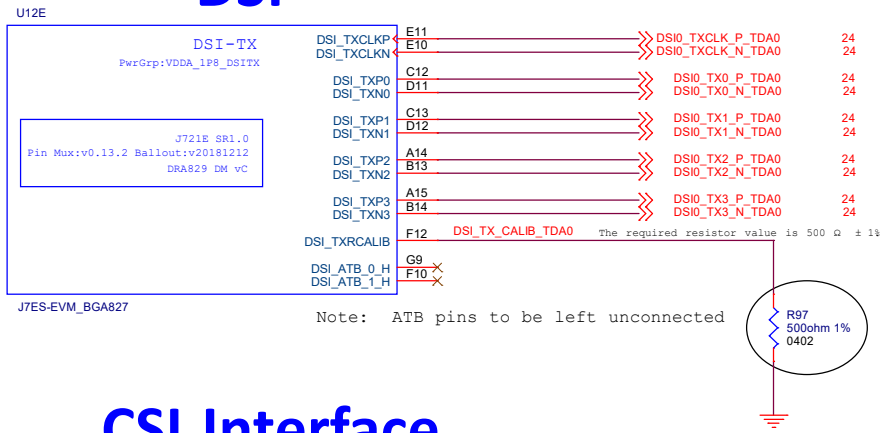
Date: Thursday, September 17, 2020	Sheet 6 of 40



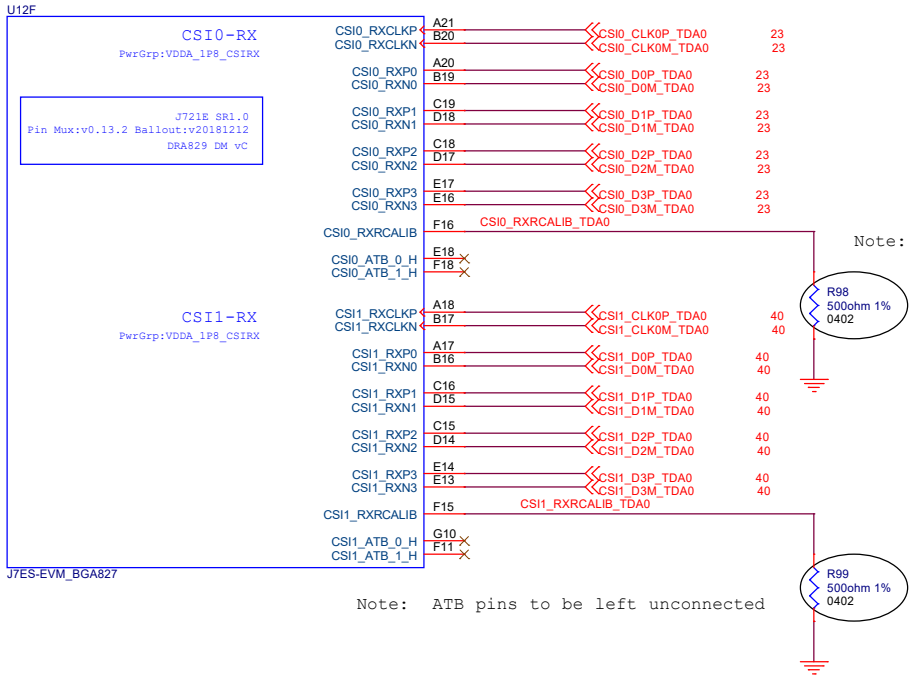
DSI

used as CSI TX



Note: ATB pins to be left unconnected

CSI Interface

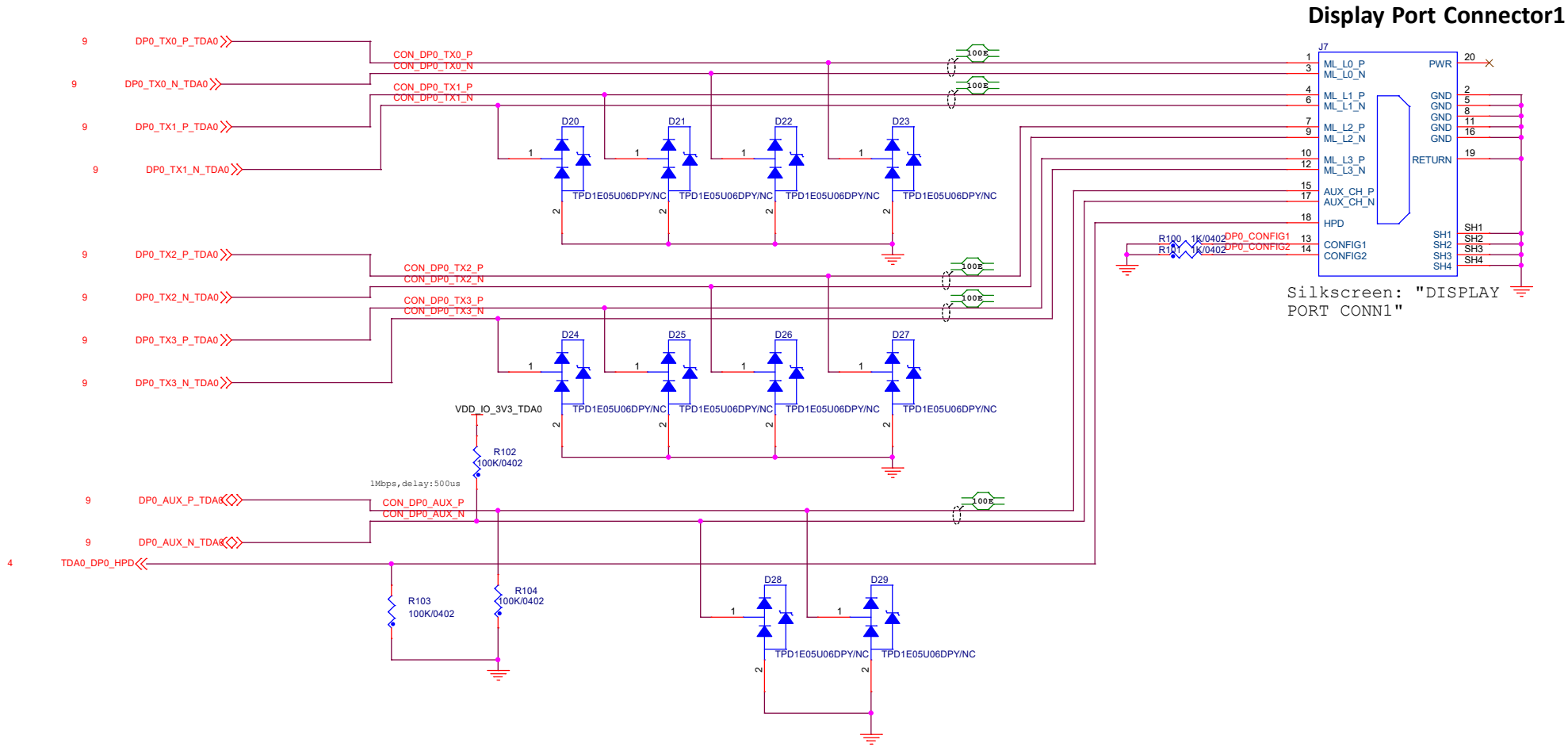


Note: ATB pins to be left unconnected

Note: ATB pins to be left unconnected

HoloMatic 禾多科技		
Title: HoloArk_V40		
Size: A3	Document Number: P07-TDA0 DSI CSI	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 7 of 40	

DISPLAY PORT INTERFACE



HoloMatic 禾多科技		
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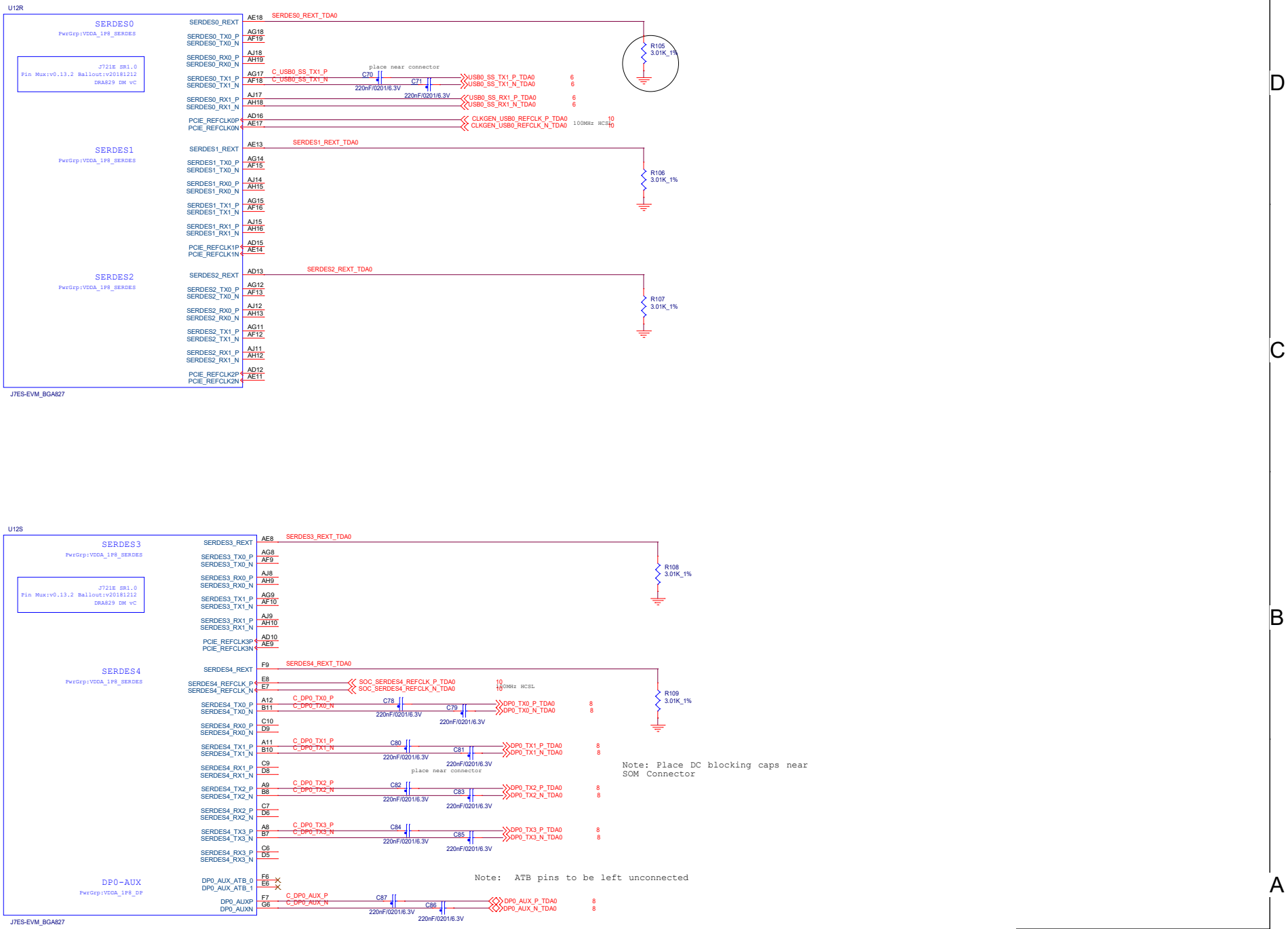
Size: A3	Document Number: P08-TDA0 DP port	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 8 of 40	



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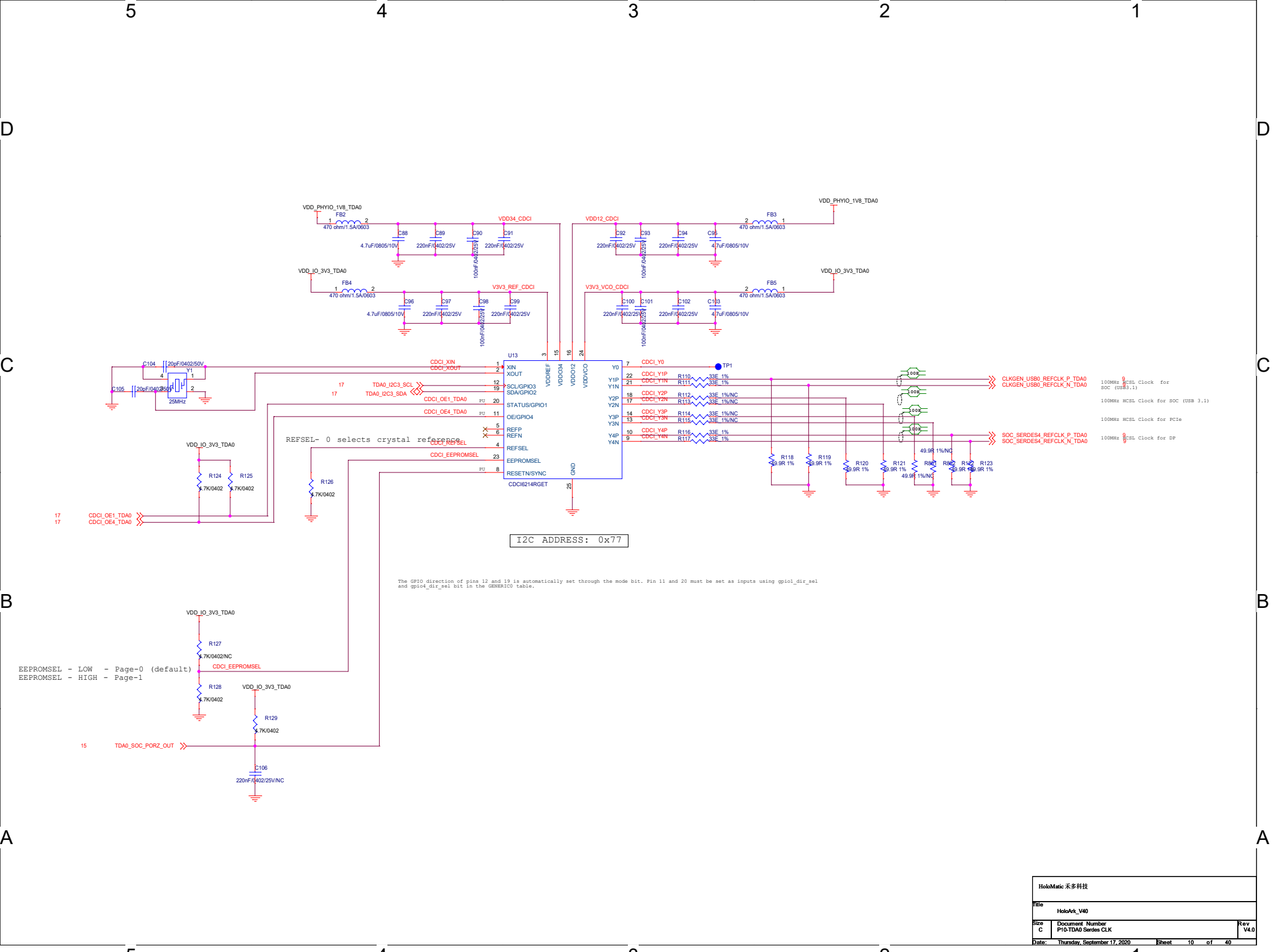
Size C	Document Number P09-TDA0 Serdes	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 9 of 40	



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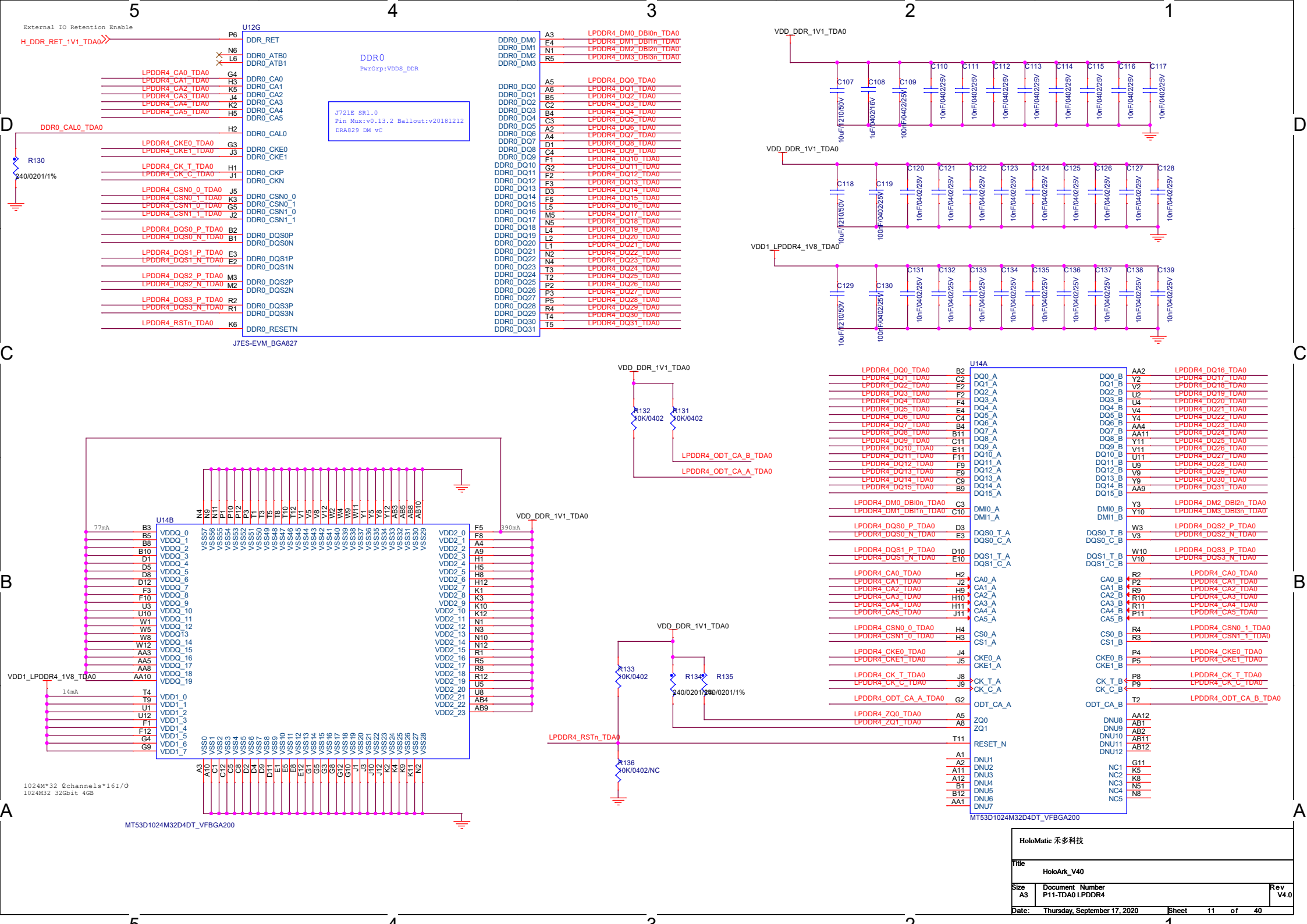
Rev	V4.0
Date:	Thursday, September 17, 2020
Sheet	10 of 40


External IO Retention Enable
H_DDR_RET_1V1_TDA0
U12G
DDR_RET
DDR0_ATB0
DDR0_ATB1
DDR0
PwrGrp:VDDS_DDR
J721E SR1.0
Pin Mux:v0.13.2 Ballout:v20181212
DRA829 DM vC
DDR0_CA0
DDR0_CA1
DDR0_CA2
DDR0_CA3
DDR0_CA4
DDR0_CA5
DDR0_CAL0
DDR0_CKE0
DDR0_CKE1
DDR0_CKP
DDR0_CKN
DDR0_CSN0_0
DDR0_CSN0_1
DDR0_CSN1_0
DDR0_CSN1_1
DDR0_DQS0P
DDR0_DQS0N
DDR0_DQS1P
DDR0_DQS1N
DDR0_DQS2P
DDR0_DQS2N
DDR0_DQS3P
DDR0_DQS3N
DDR0_RESETN
DDR0_DM0
DDR0_DM1
DDR0_DM2
DDR0_DM3
DDR0_DQ0
DDR0_DQ1
DDR0_DQ2
DDR0_DQ3
DDR0_DQ4
DDR0_DQ5
DDR0_DQ6
DDR0_DQ7
DDR0_DQ8
DDR0_DQ9
DDR0_DQ10
DDR0_DQ11
DDR0_DQ12
DDR0_DQ13
DDR0_DQ14
DDR0_DQ15
DDR0_DQ16
DDR0_DQ17
DDR0_DQ18
DDR0_DQ19
DDR0_DQ20
DDR0_DQ21
DDR0_DQ22
DDR0_DQ23
DDR0_DQ24
DDR0_DQ25
DDR0_DQ26
DDR0_DQ27
DDR0_DQ28
DDR0_DQ29
DDR0_DQ30
DDR0_DQ31
LPDDR4_DM0_DBI0n_TDA0
LPDDR4_DM1_DBI1n_TDA0
LPDDR4_DM2_DBI2n_TDA0
LPDDR4_DM3_DBI3n_TDA0
LPDDR4_DQ0_TDA0
LPDDR4_DQ1_TDA0
LPDDR4_DQ2_TDA0
LPDDR4_DQ3_TDA0
LPDDR4_DQ4_TDA0
LPDDR4_DQ5_TDA0
LPDDR4_DQ6_TDA0
LPDDR4_DQ7_TDA0
LPDDR4_DQ8_TDA0
LPDDR4_DQ9_TDA0
LPDDR4_DQ10_TDA0
LPDDR4_DQ11_TDA0
LPDDR4_DQ12_TDA0
LPDDR4_DQ13_TDA0
LPDDR4_DQ14_TDA0
LPDDR4_DQ15_TDA0
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LPDDR4_DQ21_TDA0
LPDDR4_DQ22_TDA0
LPDDR4_DQ23_TDA0
LPDDR4_DQ24_TDA0
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LPDDR4_DQ26_TDA0
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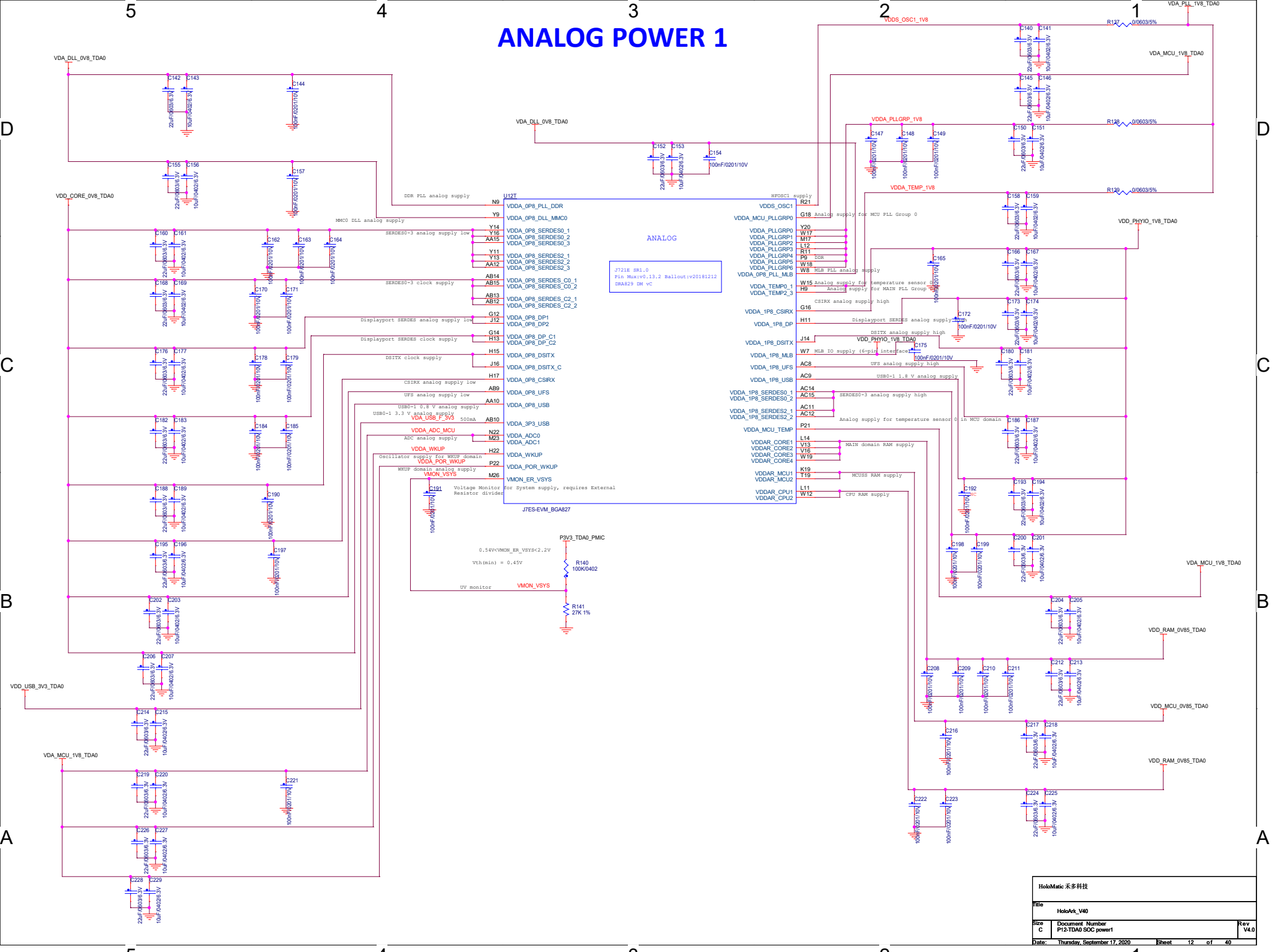
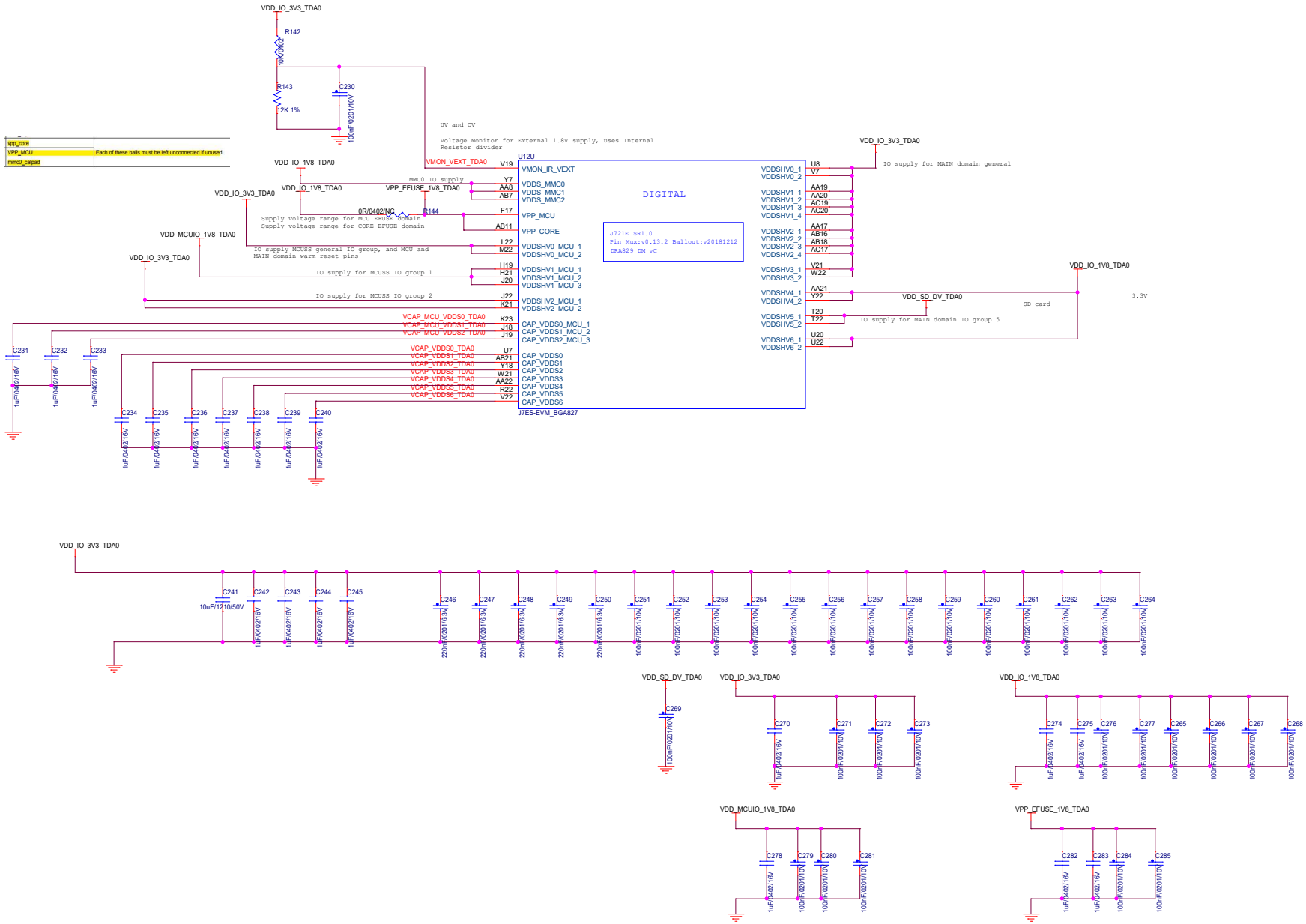
LPDDR4_DQ28_TDA0
LPDDR4_DQ29_TDA0
LPDDR4_DQ30_TDA0
LPDDR4_DQ31_TDA0
LPDDR4_CA0_TDA0
LPDDR4_CA1_TDA0
LPDDR4_CA2_TDA0
LPDDR4_CA3_TDA0
LPDDR4_CA4_TDA0
LPDDR4_CA5_TDA0
LPDDR4_CKE0_TDA0
LPDDR4_CKE1_TDA0
LPDDR4_CK_T_TDA0
LPDDR4_CK_C_TDA0
LPDDR4_CSN0_0_TDA0
LPDDR4_CSN0_1_TDA0
LPDDR4_CSN1_0_TDA0
LPDDR4_CSN1_1_TDA0
LPDDR4_DQS0_P_TDA0
LPDDR4_DQS0_N_TDA0
LPDDR4_DQS1_P_TDA0
LPDDR4_DQS1_N_TDA0
LPDDR4_DQS2_P_TDA0
LPDDR4_DQS2_N_TDA0
LPDDR4_DQS3_P_TDA0
LPDDR4_DQS3_N_TDA0
LPDDR4_RSTn_TDA0
DDR0_CAL0_TDA0
R130
240/0201/1%
J7ES-EVM_BGA827
VDD_DDR_1V1_TDA0
C107
C108
C109
C110
C111
C112
C113
C114
C115
C116
C117
10uF/1210/50V
1uF/0402/16V
100nF/0402/25V
10nF/0402/25V
VDD_DDR_1V1_TDA0
C118
C119
C120
C121
C122
C123
C124
C125
C126
C127
C128
10uF/1210/50V
100nF/0402/25V
10nF/0402/25V
VDD1_LPDDR4_1V8_TDA0
C129
C130
C131
C132
C133
C134
C135
C136
C137
C138
C139
10uF/1210/50V
100nF/0402/25V
10nF/0402/25V
VDD_DDR_1V1_TDA0
R132
10K/0402
R131
10K/0402
LPDDR4_ODT_CA_B_TDA0
LPDDR4_ODT_CA_A_TDA0
U14B
77mA
390mA
14mA
VDD1_LPDDR4_1V8_TDA0
VDD_DDR_1V1_TDA0
1024M*32 2channels*16I/O
1024M32 32Gbit 4GB
MT53D1024M32D4DT_VFBGA200
VDD_DDR_1V1_TDA0
R133
10K/0402
R134
240/0201/1%
R135
240/0201/1%
LPDDR4_RSTn_TDA0
R136
10K/0402/NC
U14A
MT53D1024M32D4DT_VFBGA200
HoloMatic 禾多科技
Title
HoloArk_V40
Size
A3
Document Number
P11-TDA0 LPDDR4
Rev
V4.0
Date:
Thursday, September 17, 2020
Sheet
11
of
40

ANALOG POWER 1





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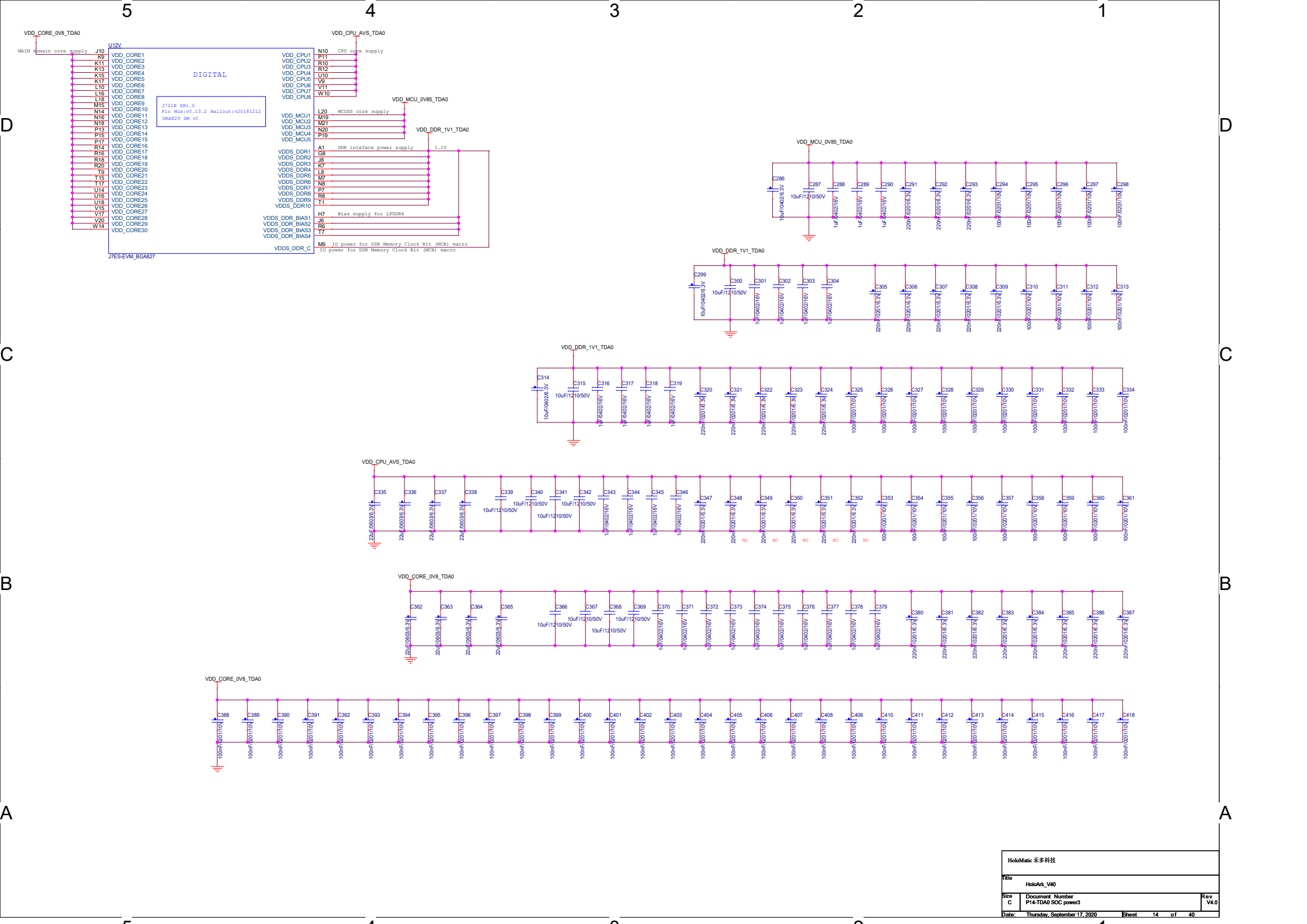
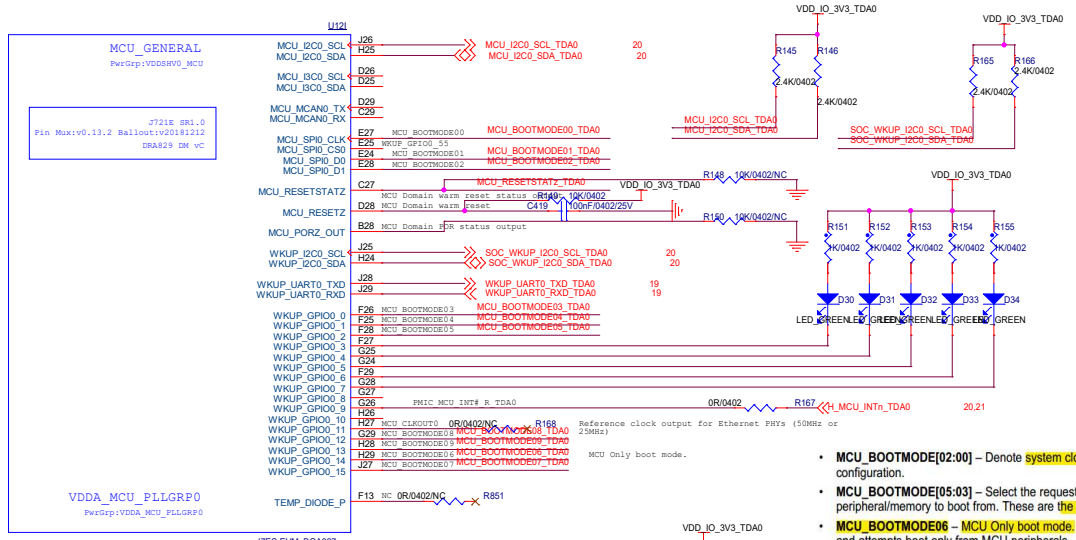
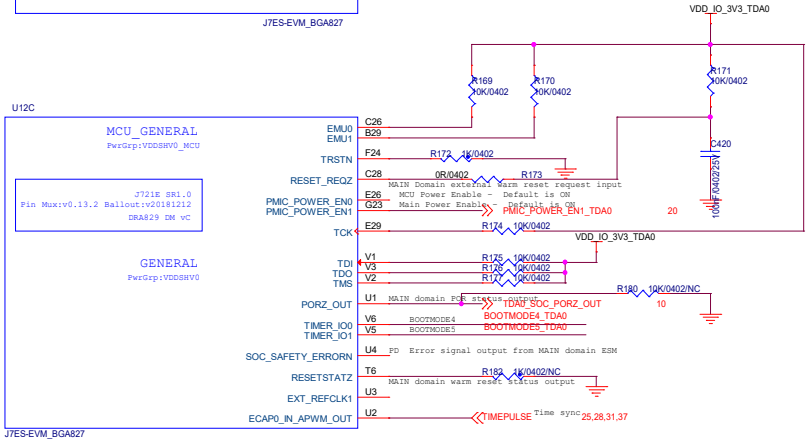
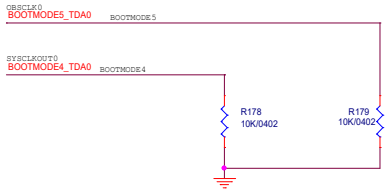
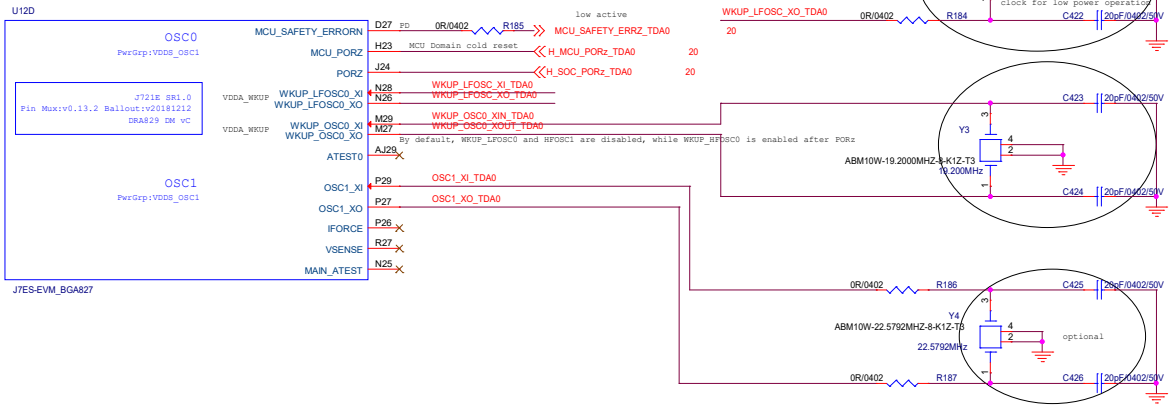
Rev	V4.0
Date: Thursday, September 17, 2020	Sheet 13 of 40


5
4
3
2
1
D
C
B
A
VDD_CORE_0V8_TDA0
MAIN domain core supply
J10
U12V
VDD_CORE1
VDD_CORE2
VDD_CORE3
VDD_CORE4
VDD_CORE5
VDD_CORE6
VDD_CORE7
VDD_CORE8
VDD_CORE9
VDD_CORE10
VDD_CORE11
VDD_CORE12
VDD_CORE13
VDD_CORE14
VDD_CORE15
VDD_CORE16
VDD_CORE17
VDD_CORE18
VDD_CORE19
VDD_CORE20
VDD_CORE21
VDD_CORE22
VDD_CORE23
VDD_CORE24
VDD_CORE25
VDD_CORE26
VDD_CORE27
VDD_CORE28
VDD_CORE29
VDD_CORE30
DIGITAL
J721E SR1.0
Pin Mux:v0.13.2 Ballout:v20181212
DRA829 DM VC
J7ES-EVM_BGA827
VDD_CPU_AVS_TDA0
CPU core supply
VDD_CPU1
VDD_CPU2
VDD_CPU3
VDD_CPU4
VDD_CPU5
VDD_CPU6
VDD_CPU7
VDD_CPU8
VDD_MCU_0V85_TDA0
MCUSS core supply
VDD_MCU1
VDD_MCU2
VDD_MCU3
VDD_MCU4
VDD_MCU5
VDD_DDR_1V1_TDA0
DDR inteface power supply
1.1V
VDDS_DDR1
VDDS_DDR2
VDDS_DDR3
VDDS_DDR4
VDDS_DDR5
VDDS_DDR6
VDDS_DDR7
VDDS_DDR8
VDDS_DDR9
VDDS_DDR10
Bias supply for LPDDR4
VDDS_DDR_BIAS1
VDDS_DDR_BIAS2
VDDS_DDR_BIAS3
VDDS_DDR_BIAS4
IO power for DDR Memory Clock Bit (MCB) macro
VDDS_DDR_C
HoloMatic 禾多科技
Title
HoloArk_V40
Size
C
Document Number
P14-TDA0 SOC power3
Rev
V4.0
Date:
Thursday, September 17, 2020
Sheet
14
of
40









Clock	Ball Mapping	Frequency List / Range
HFOSC1_CLK	OSC1_XI OSC1_XO	19.2, 20, 24, 25, 26, or 27 MHz For audio applications: 22.5792 MHz or 24.576 MHz

- **MCU_BOOTMODE[02:00]** – Denote system clock frequency (WKUP_HFOSC0) to ROM code for PLL configuration.
- **MCU_BOOTMODE[05:03]** – Select the requested boot (primary) mode after POR, that is, the peripheral/memory to boot from. These are the only pins which direct boot on MCU Only boot mode
- **MCU_BOOTMODE06** – MCU Only boot mode. In MCU Only boot, ROM code skips BOOTMODE pins and attempts boot only from MCU peripherals
- **MCU_BOOTMODE[09:08]** – These pins can select tests to be performed on power-up (POST). POST runs in hardware, before the ROM code starts

	BOOTMODE			MCU_BOOTMODE		
	6	5	4	5	4	3
SDcard	1	0	0	0	0	0
eMMC	0	0	0	0	0	1
USB0	0	0	0	0	1	0

SDcard in
J3,J4,SDcard NC
J3,J4 short; SDcard NC

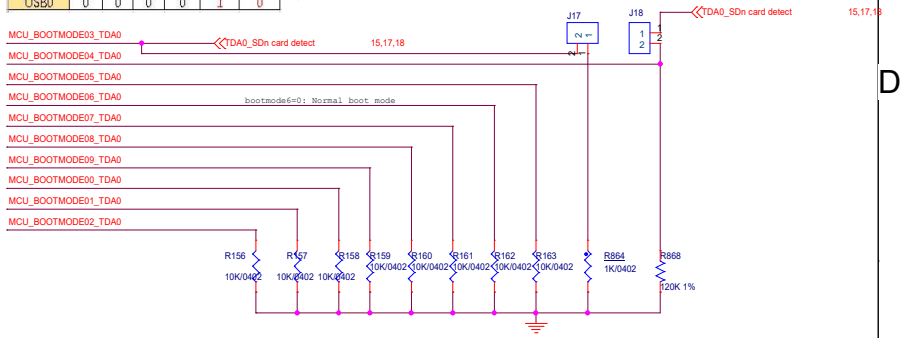


Table 4-10. Primary Boot Mode Configuration

Primary Boot Mode Config Pins			Primary Boot Mode B Pin	Primary Boot Mode A Pins			Primary Boot Mode
6	5	4	0	MCU 5	MCU 4	MCU 3	
Speed	Iclk	Csel	0	0	0	1	OSPI
Port	Iclk	Csel	0	0	1	0	QSPI
Port	Mode	Csel	0	0	1	1	SPI
Clkout	Delay	Link stat	0	1	0	0	Ethernet RGMII
Clkout	Clk src		0	1	0	1	Ethernet RMII
Bus reset	Mode	Addr	0	1	1	0	I2C
		Port	0	1	1	1	UART or No boot
Port	Bus width	Fs/raw	1	0	0	0	MMC/SD card
Port	Bus width	Voltage	1	0	0	1	eMMC
Port	Mode	Lane Swap	1	0	1	0	USB
AD Mux		Csel	1	1	0	0	GPMC NOR
Port	N lanes	sref	1	1	0	1	PCIe
			1	1	1	0	Reserved
			1	1	1	1	Reserved or No boot

MMC/SD Card Boot Device Configuration

Table 4-22 shows configuration pins assignment to functions when boot mode is the MMC/SD card mode.

Table 4-22. MMC/SD Card Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description	MCU Only=1 Value
6 (7)[1]	Port	0	Port 0	N/A
		1	Port 1	
5	Bus Width	0	4 bit	N/A
		1	1 bit	
4	FS/Raw	0	Filesystem mode	N/A
		1	Raw Mode	

eMMC Boot Device Configuration

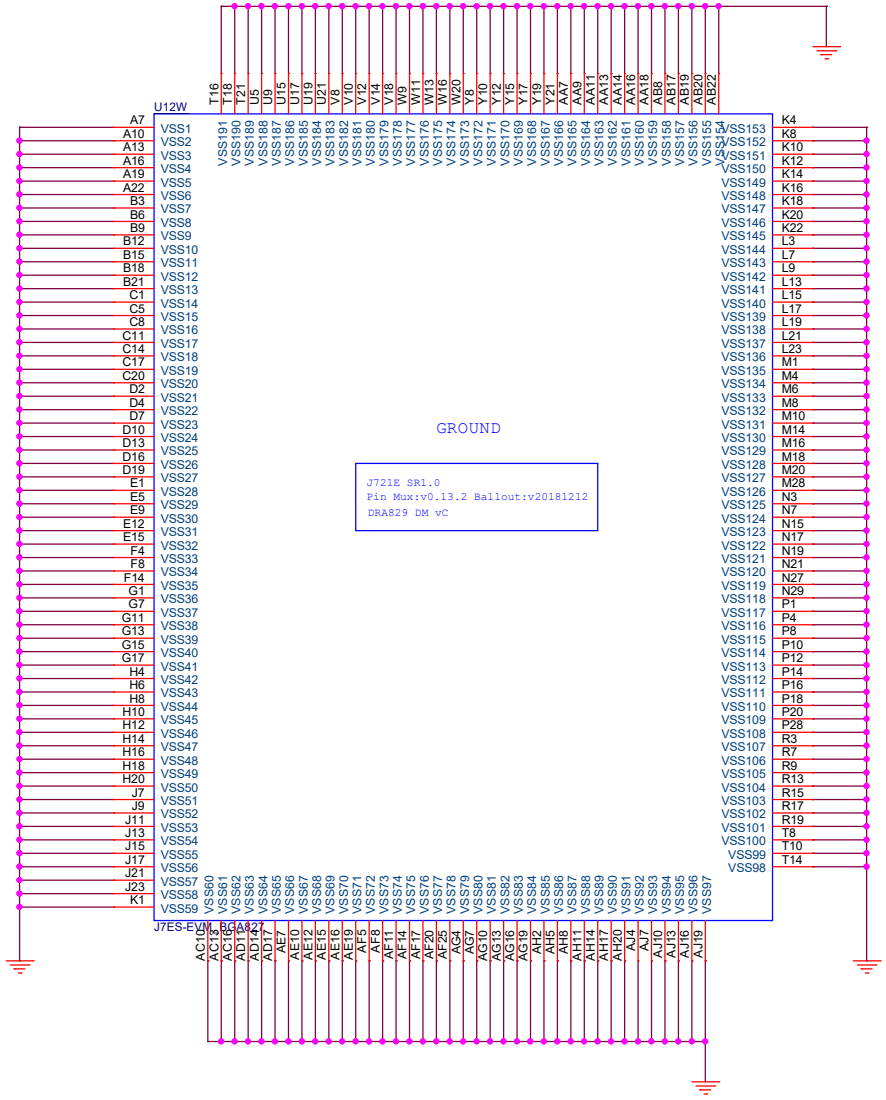
Table 4-40 shows configuration pins assignment to functions when boot mode is the eMMC mode.

Table 4-40. eMMC Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description	MCU Only=1 Valu
6	Port	0	Port 0	N/A
		1	Port 1	
5	Bus Width	0	Max width by port (8-bit on port 0, 4-bit on port 1)	N/A
		1	1-bit only	
4	Voltage	0	1.8V	N/A
		1	3.3V	

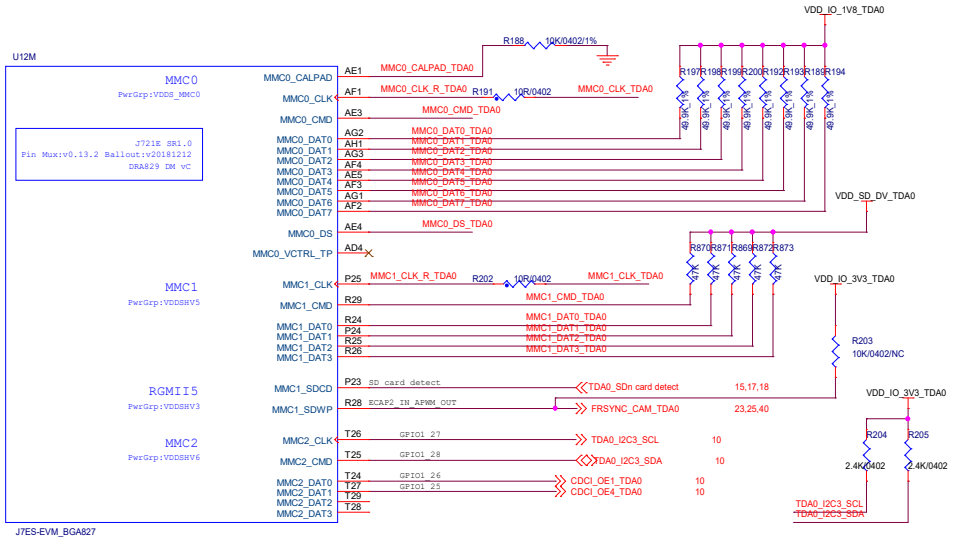
HoloMatic 禾多科技

Title	HoloArk_V40	
Size C	Document Number P15-TDA0 MCU General	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 15 of 40	



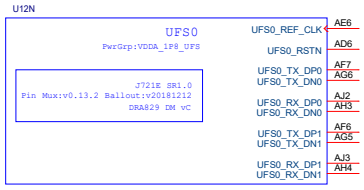
HoloMatic 禾多科技		
Title: HoloArk_V40		
Size: A3	Document Number: P16-TDA0 SOC GND	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 16 of 40	

MMC Interface



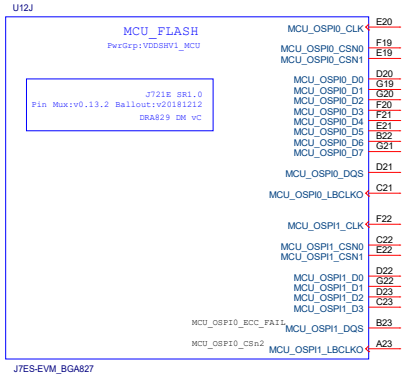
J7ES-EVM_BGA827

UFS Interface



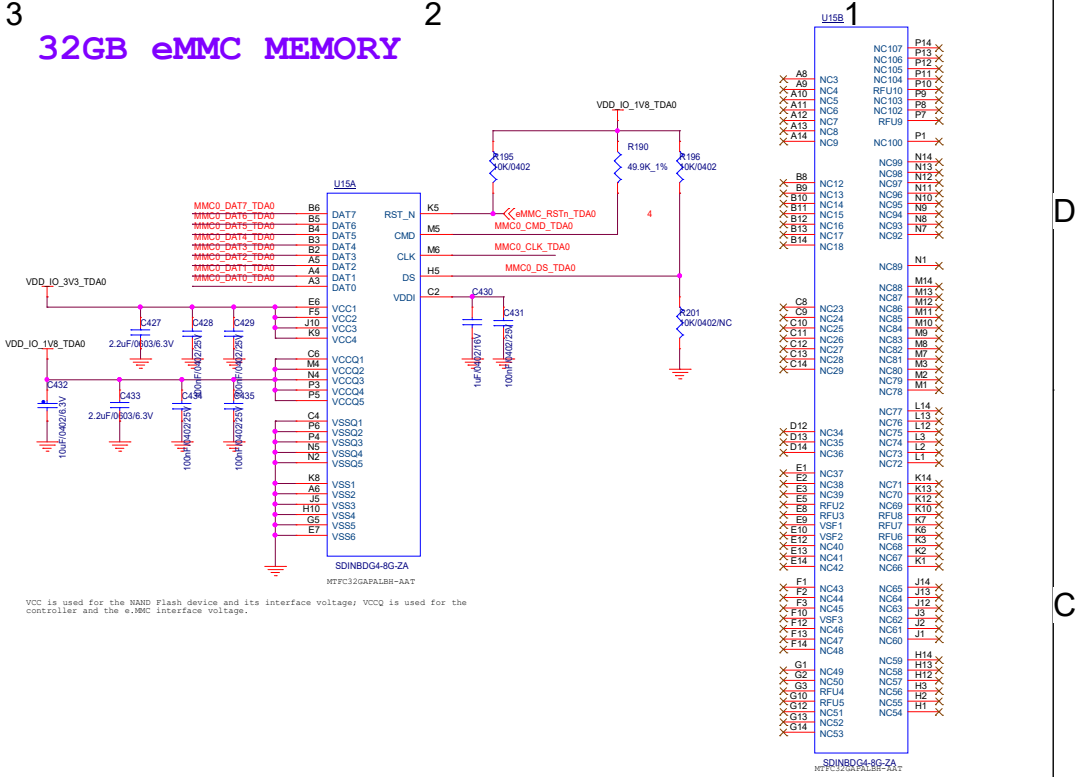
J7ES-EVM_BGA827

MCU FLASH



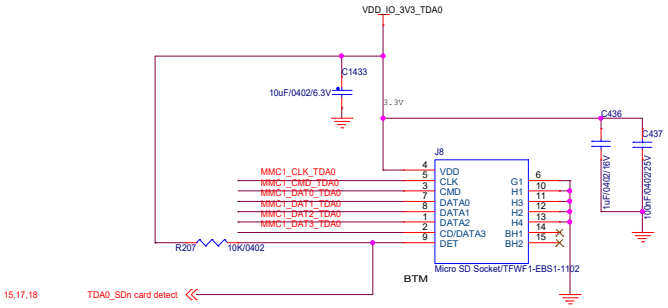
J7ES-EVM_BGA827

32GB eMMC MEMORY

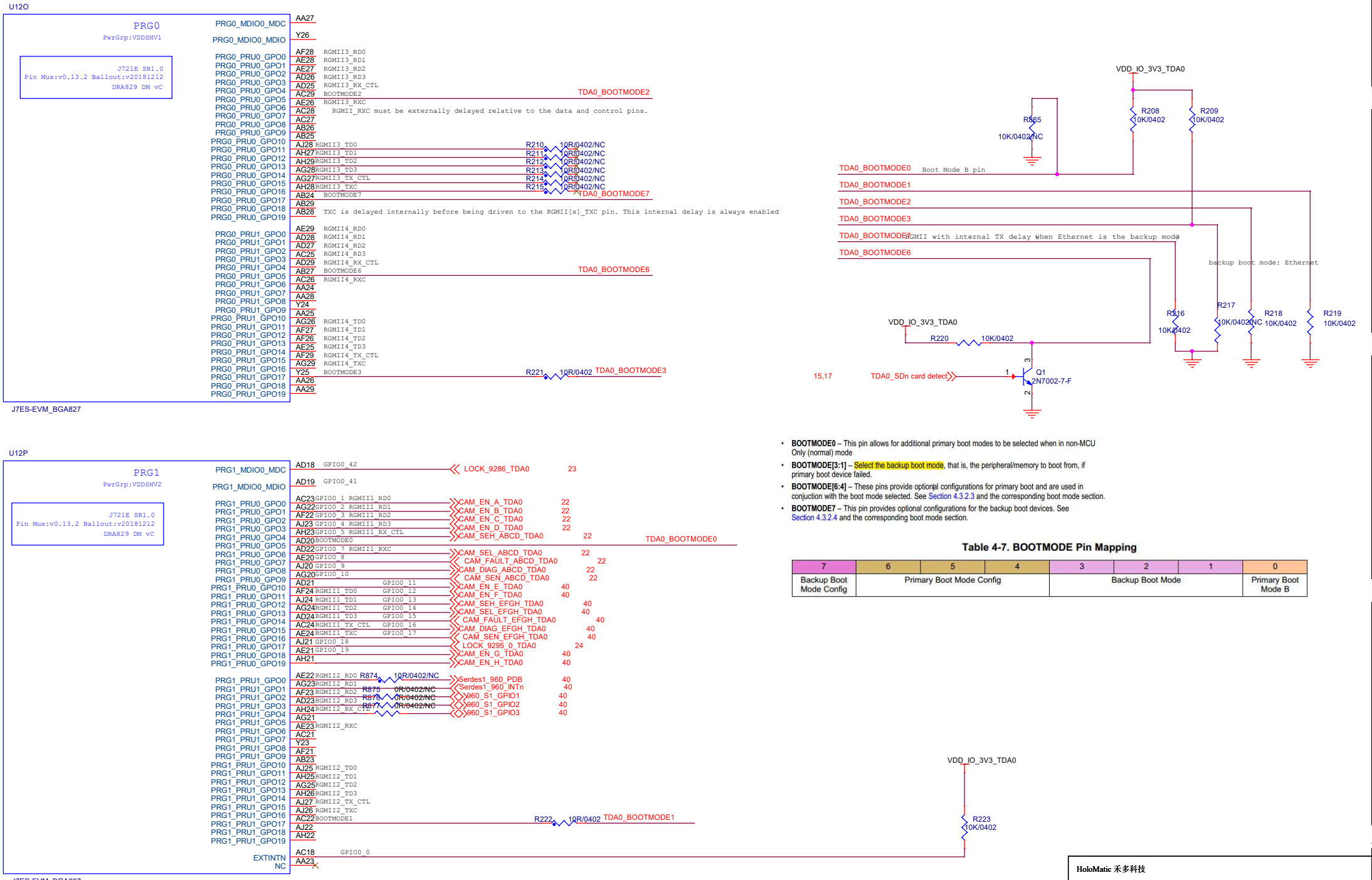


VCC is used for the NAND Flash device and its interface voltage; VCCQ is used for the controller and the e.MMC interface voltage.

TFCard



HoloMatic 禾多科技		
Title	HoloArk_V40	
Size C	Document Number P17-TDA0 eMMC SD	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 17 of 40	



- **BOOTMODE0** – This pin allows for additional primary boot modes to be selected when in non-MCU Only (normal) mode
- **BOOTMODE[3:1]** – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.
- **BOOTMODE[6:4]** – These pins provide optional configurations for primary boot and are used in conjuction with the boot mode selected. See Section 4.3.2.3 and the corresponding boot mode section.
- **BOOTMODE7** – This pin provides optional configurations for the backup boot devices. See Section 4.3.2.4 and the corresponding boot mode section.

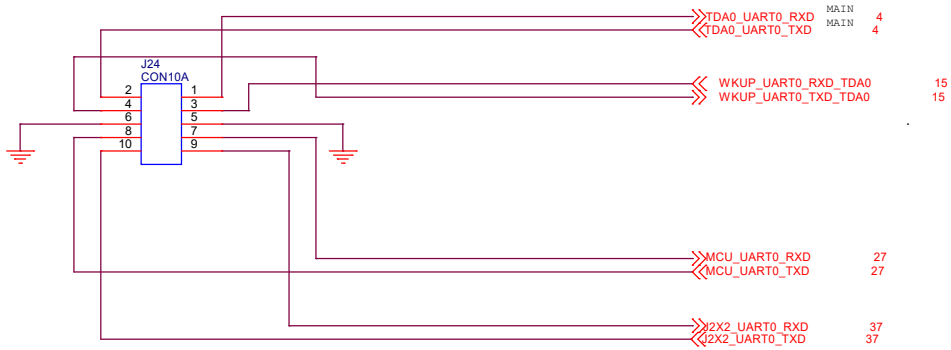
Table 4-7. BOOTMODE Pin Mapping

7	6	5	4	3	2	1	0
Backup Boot Mode Config	Primary Boot Mode Config			Backup Boot Mode			Primary Boot Mode B

HoloMatic 禾多科技

Title	HoloArk_V40	
Size A3	Document Number P18-TDA0 SOC RGMII	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 18 of 40	

UART TO external USB Board



HoloMatic 禾多科技		
Title: HoloArk_V40		
Size: A3	Document Number: P19-TDA0 Debug uart	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 19 of 40	

PMIC- A

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

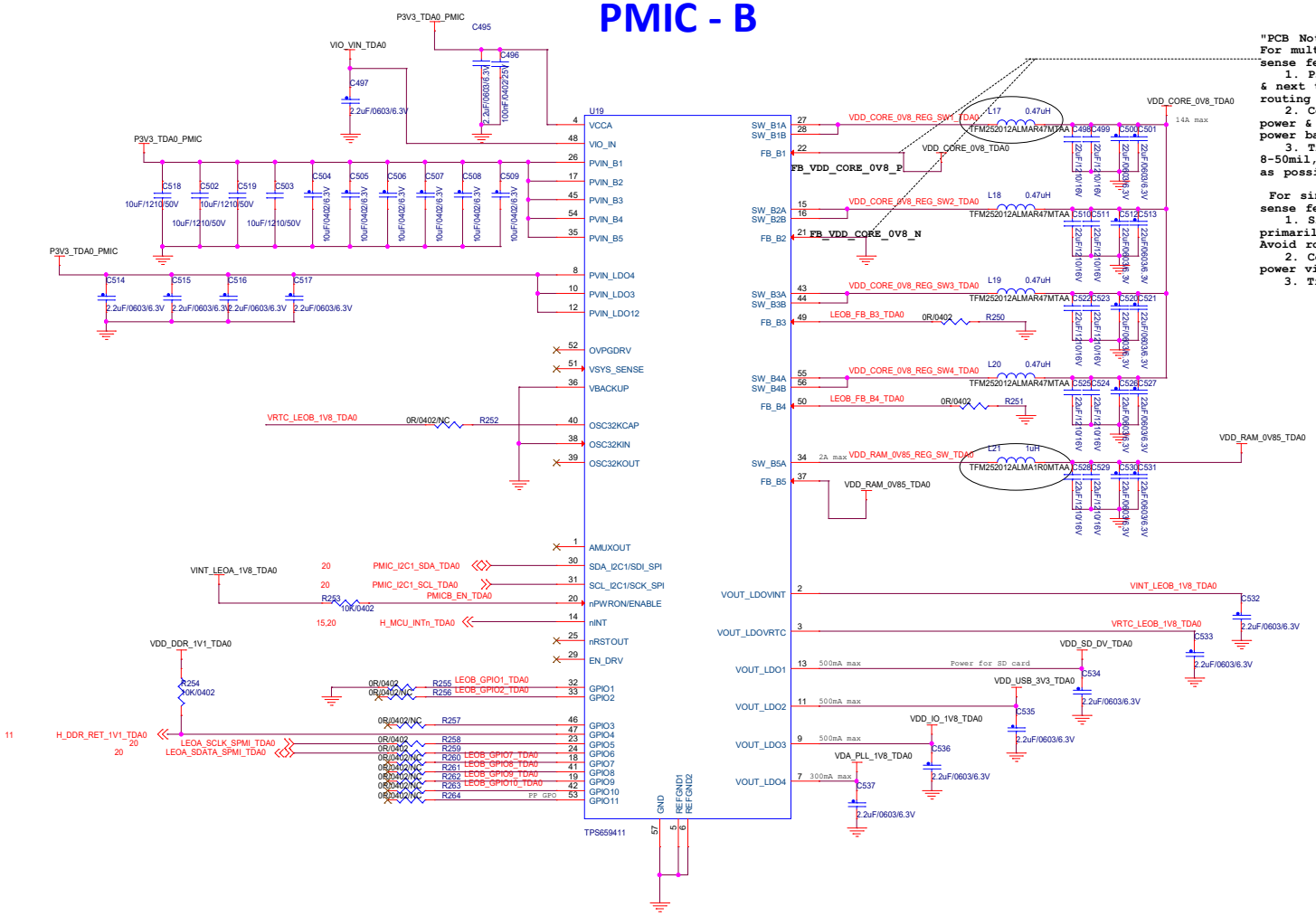
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

Route as Pseudo differential pair trace
(See "PCB Notes")

PMIC-A uses default I2C ADDR:
0x48, 0x49,0x4A,0x4B
0x12

HoloMatic 禾多科技			
Title	HoloArk_V40		
Size C	Document Number P20-TDA0 SoM PMIC A		Rev V4.0
Date: Thursday, September 17, 2020	Sheet 20 of 40		

PMIC - B

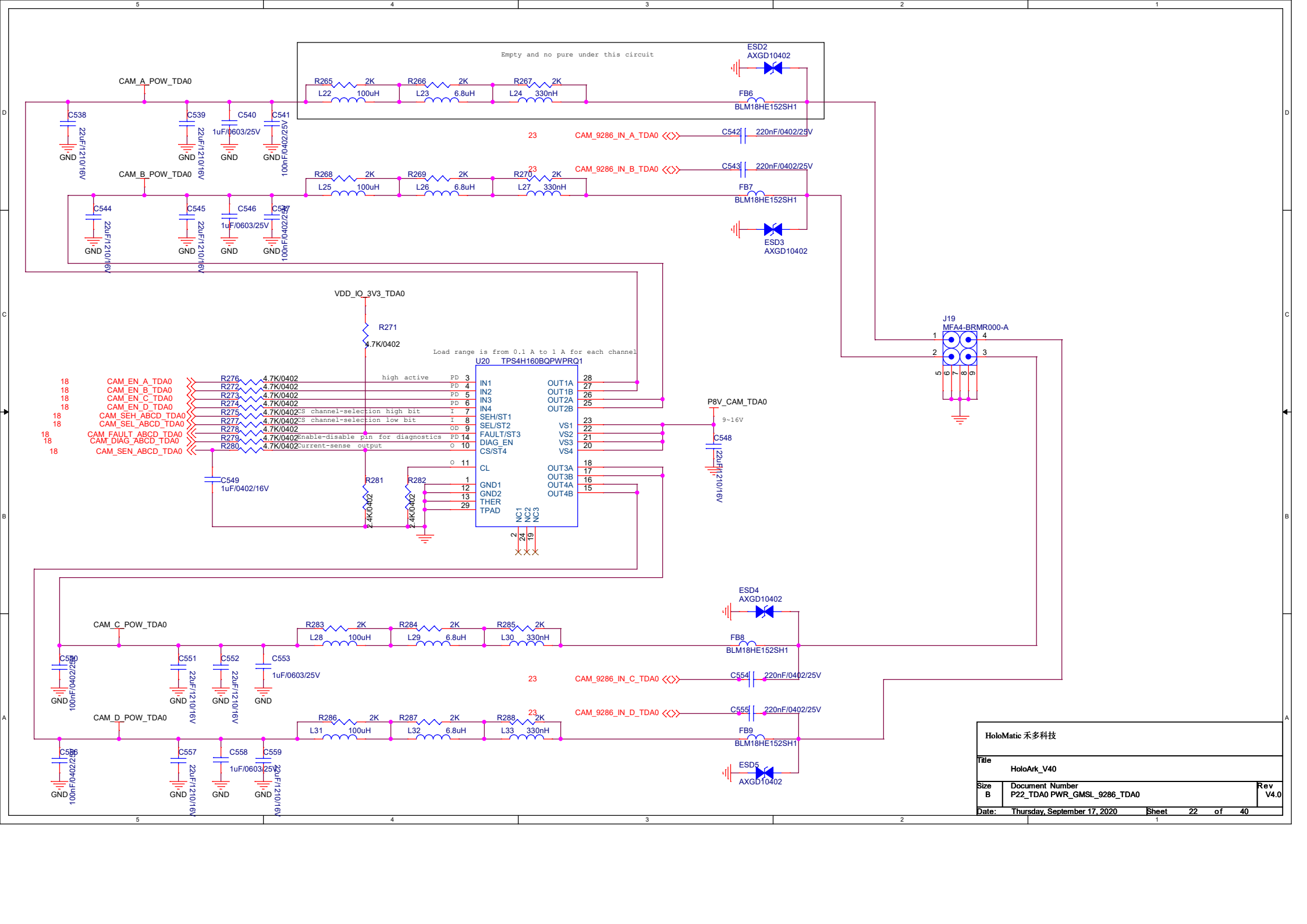


"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

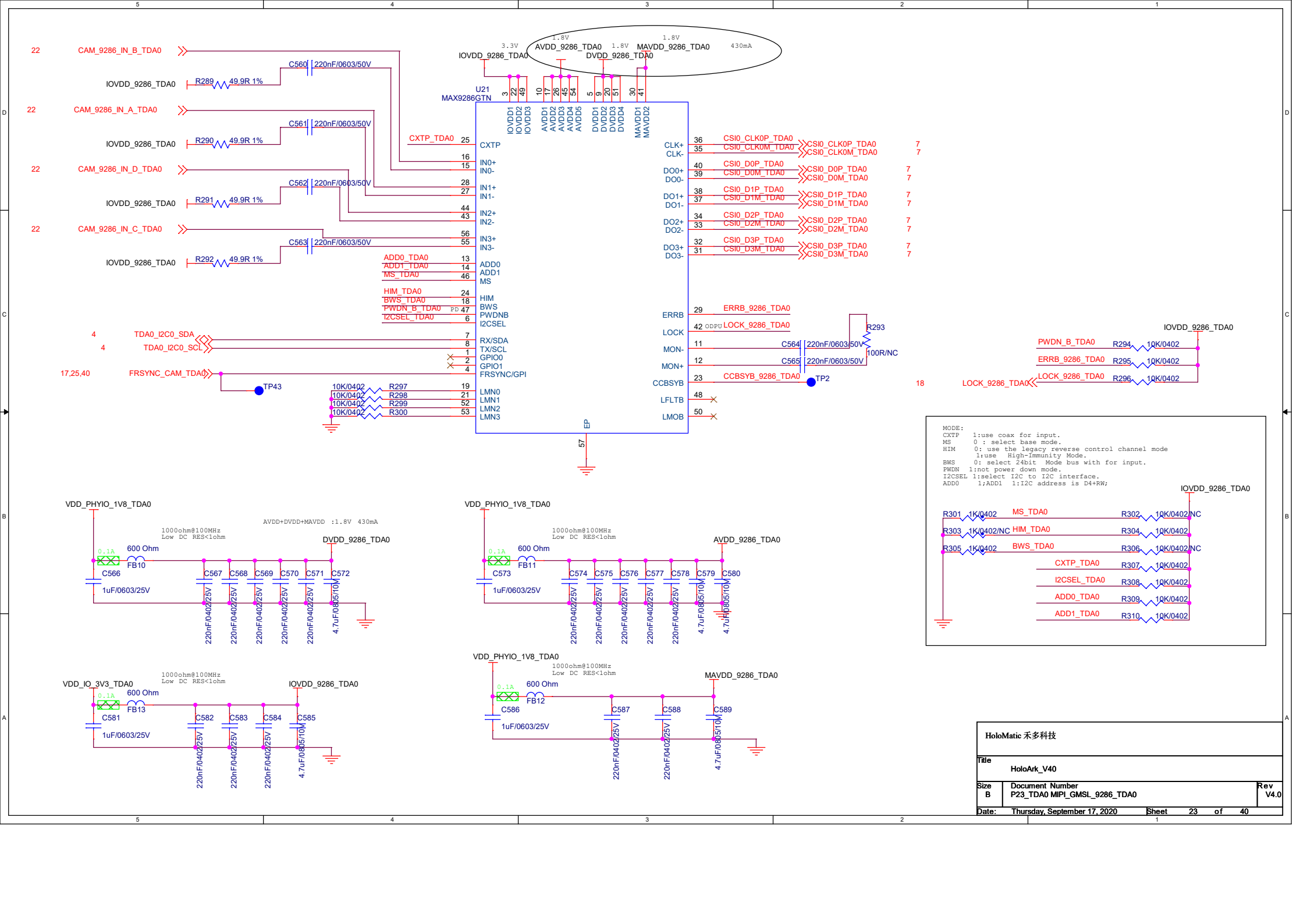
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

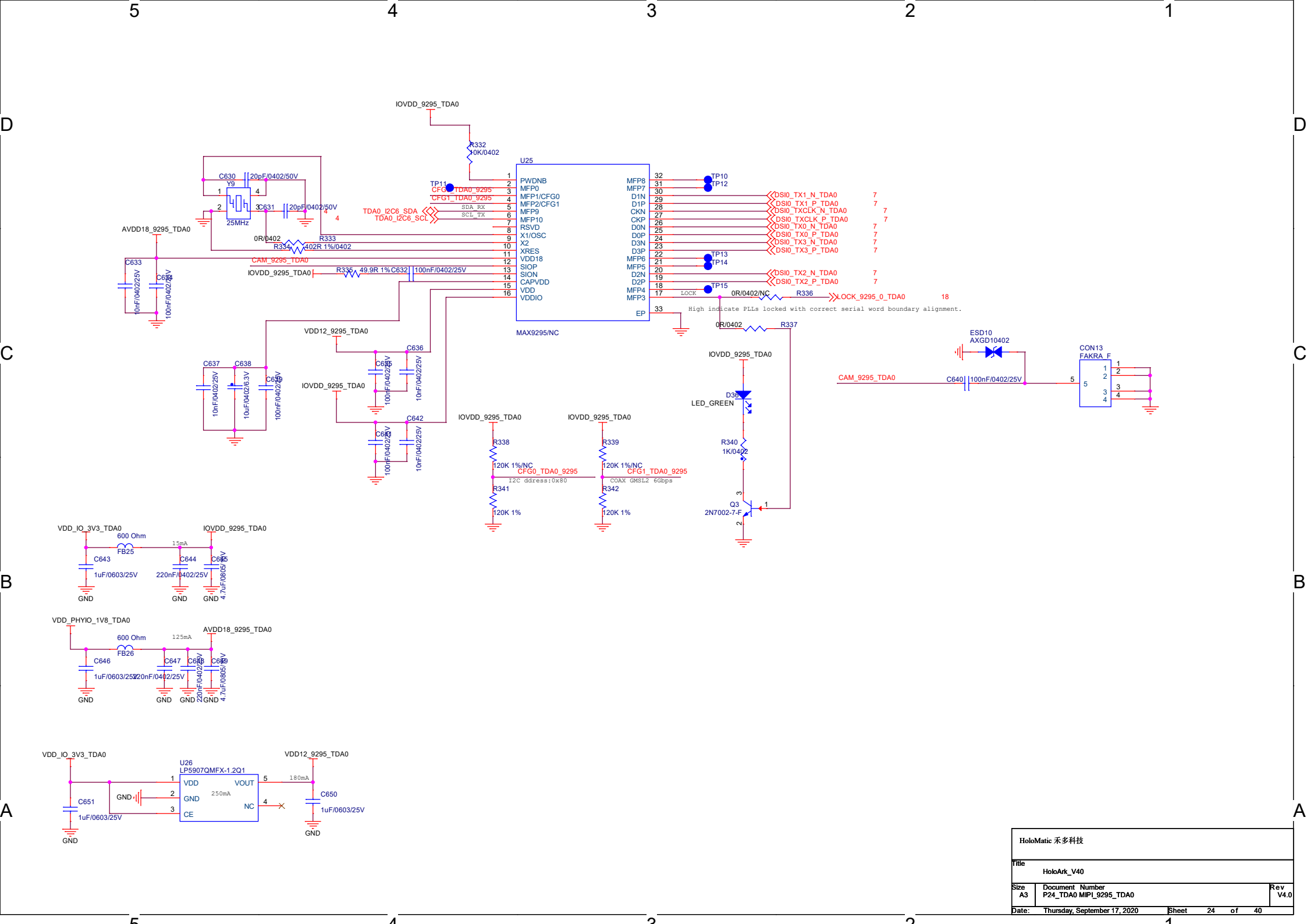
PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

HoloMatic 禾多科技		
Title: HoloArk_V40		
Size: C	Document Number: P21-TDA0 SoM PMIC B	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 21 of 40	



HoloMatic 禾多科技			
Title: HoloArk_V40			
Size: B	Document Number: P22_TDA0 PWR_GMSL_9286_TDA0		Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 22 of 40		


U21
MAX9286GTN
CXTP_TDA0
IN0+
IN0-
IN1+
IN1-
IN2+
IN2-
IN3+
IN3-
ADD0_TDA0
ADD1_TDA0
MS_TDA0
HIM_TDA0
BWS_TDA0
PWDN_B_TDA0
I2CSEL_TDA0
TDA0_I2C0_SDA
TDA0_I2C0_SCL
FRSYNC_CAM_TDA0
TP43
LMN0
LMN1
LMN2
LMN3
CLK+
CLK-
DO0+
DO0-
DO1+
DO1-
DO2+
DO2-
DO3+
DO3-
CSI0_CLK0P_TDA0
CSI0_CLK0M_TDA0
CSI0_D0P_TDA0
CSI0_D0M_TDA0
CSI0_D1P_TDA0
CSI0_D1M_TDA0
CSI0_D2P_TDA0
CSI0_D2M_TDA0
CSI0_D3P_TDA0
CSI0_D3M_TDA0
ERRB_9286_TDA0
LOCK_9286_TDA0
CCBSYB_9286_TDA0
TP2
R293
100R/NC
C564
C565
220nF/0603/50V
LFLTB
LMOB
EP
IOVDD_9286_TDA0
AVDD_9286_TDA0
DVDD_9286_TDA0
MAVDD_9286_TDA0
430mA
PWDN_B_TDA0
ERRB_9286_TDA0
LOCK_9286_TDA0
R294
R295
R296
10K/0402
MODE:
CXTP 1:use coax for input.
MS 0 : select base mode.
HIM 0: use the legacy reverse control channel mode
1:use High-Immunity Mode.
BWS 0: select 24bit Mode bus with for input.
PWDN 1:not power down mode.
I2CSEL 1:select I2C to I2C interface.
ADD0 1;ADD1 1:I2C address is D4+RW;
R301
R302
R303
R304
R305
R306
R307
R308
R309
R310
MS_TDA0
HIM_TDA0
BWS_TDA0
CXTP_TDA0
I2CSEL_TDA0
ADD0_TDA0
ADD1_TDA0
10K/0402/NC
VDD_PHYIO_1V8_TDA0
AVDD+DVDD+MAVDD :1.8V 430mA
1000ohm@100MHz
Low DC RES<1ohm
600 Ohm
FB10
FB11
FB12
FB13
C566
C567
C568
C569
C570
C571
C572
C573
C574
C575
C576
C577
C578
C579
C580
C581
C582
C583
C584
C585
C586
C587
C588
C589
1uF/0603/25V
220nF/0402/25V
4.7uF/0805/10V
VDD_IO_3V3_TDA0
HoloMatic 禾多科技
Title
HoloArk_V40
Size
B
Document Number
P23_TDA0 MIPI_GMSL_9286_TDA0
Rev
V4.0
Date:
Thursday, September 17, 2020
Sheet
23
of
40



HoloMatic 禾多科技		
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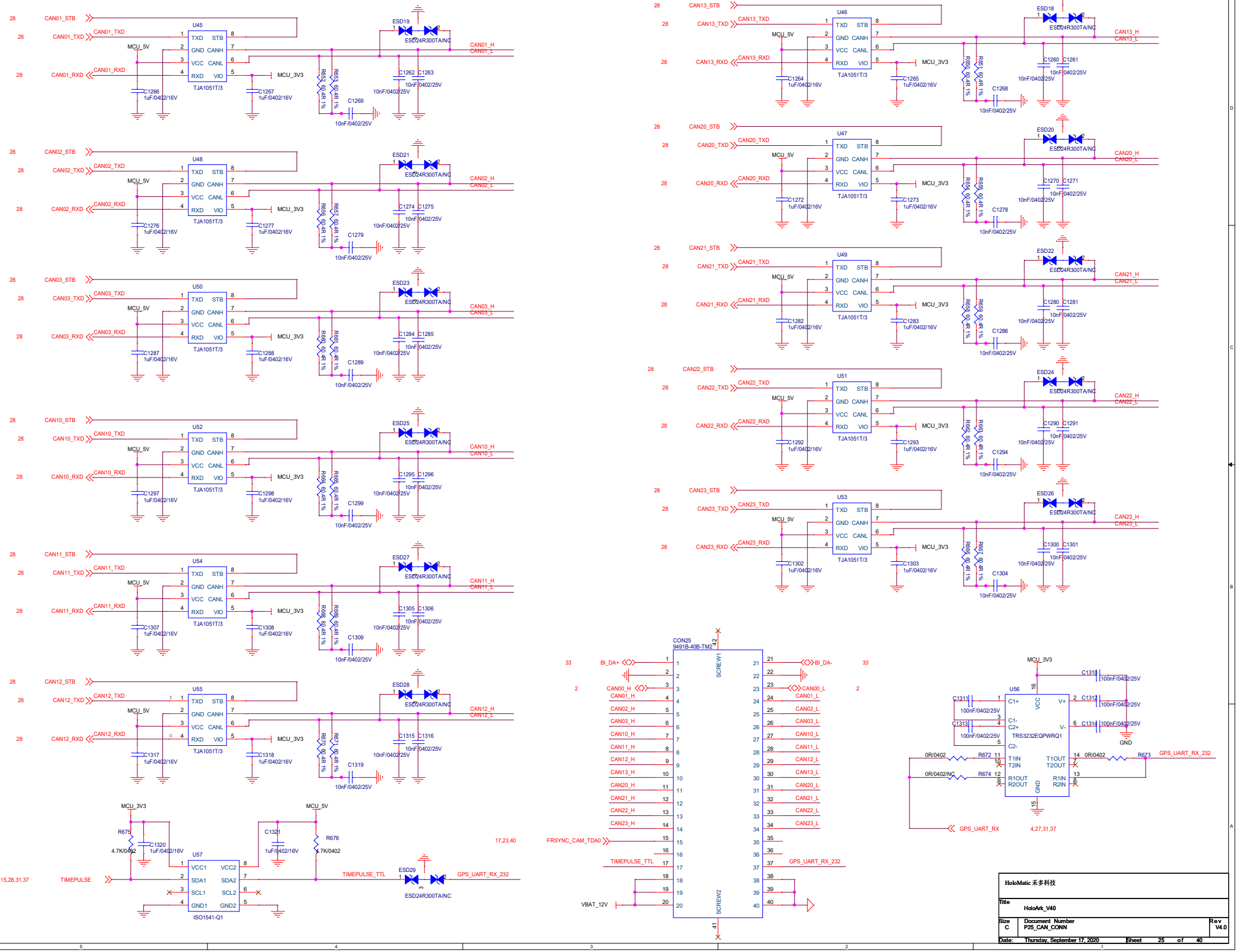
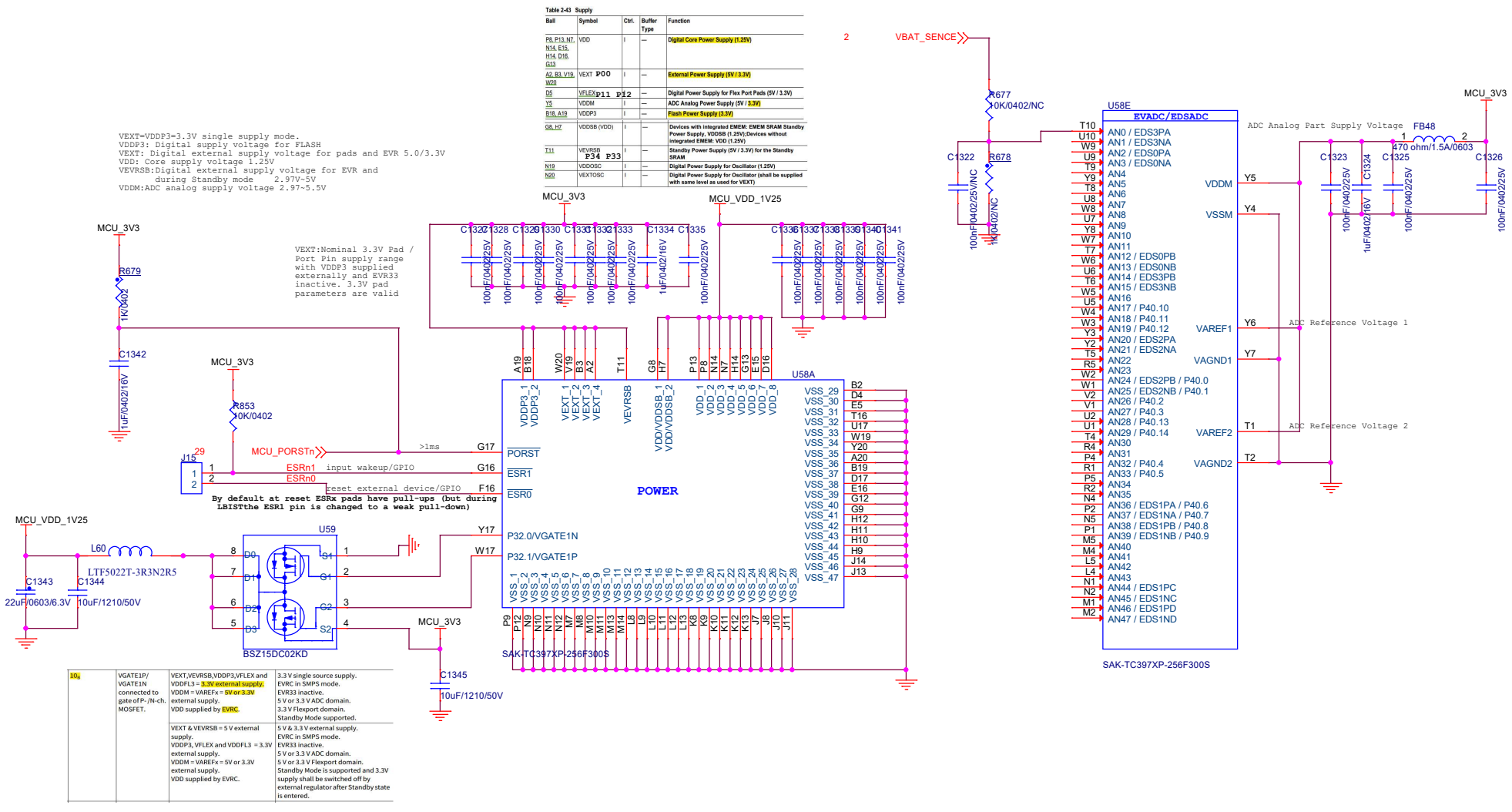
Size A3	Document Number P24_TDA0 MIPI_9295_TDA0	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 24 of 40	


U45
U46
U47
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
TJA1051T/3
ISO1541-Q1
TRS3232EQPWRQ1
CON25
9491B-40B-TM2
ESD24R300TA/NC
MCU_5V
MCU_3V3
CAN01_STB
CAN01_TXD
CAN01_RXD
CAN01_H
CAN01_L
CAN02_STB
CAN02_TXD
CAN02_RXD
CAN02_H
CAN02_L
CAN03_STB
CAN03_TXD
CAN03_RXD
CAN03_H
CAN03_L
CAN10_STB
CAN10_TXD
CAN10_RXD
CAN10_H
CAN10_L
CAN11_STB
CAN11_TXD
CAN11_RXD
CAN11_H
CAN11_L
CAN12_STB
CAN12_TXD
CAN12_RXD
CAN12_H
CAN12_L
CAN13_STB
CAN13_TXD
CAN13_RXD
CAN13_H
CAN13_L
CAN20_STB
CAN20_TXD
CAN20_RXD
CAN20_H
CAN20_L
CAN21_STB
CAN21_TXD
CAN21_RXD
CAN21_H
CAN21_L
CAN22_STB
CAN22_TXD
CAN22_RXD
CAN22_H
CAN22_L
CAN23_STB
CAN23_TXD
CAN23_RXD
CAN23_H
CAN23_L
BI_DA+
BI_DA-
CAN00_H
CAN00_L
FRSYNC_CAM_TDA0
TIMEPULSE
TIMEPULSE_TTL
GPS_UART_RX_232
GPS_UART_RX
VBAT_12V
SCREW1
SCREW2
HoloMatic 禾多科技
HoloArk_V40
Document Number
P25_CAN_CONN
Rev V4.0
Thursday, September 17, 2020
Sheet 25 of 40



HoloMatic 禾多科技	
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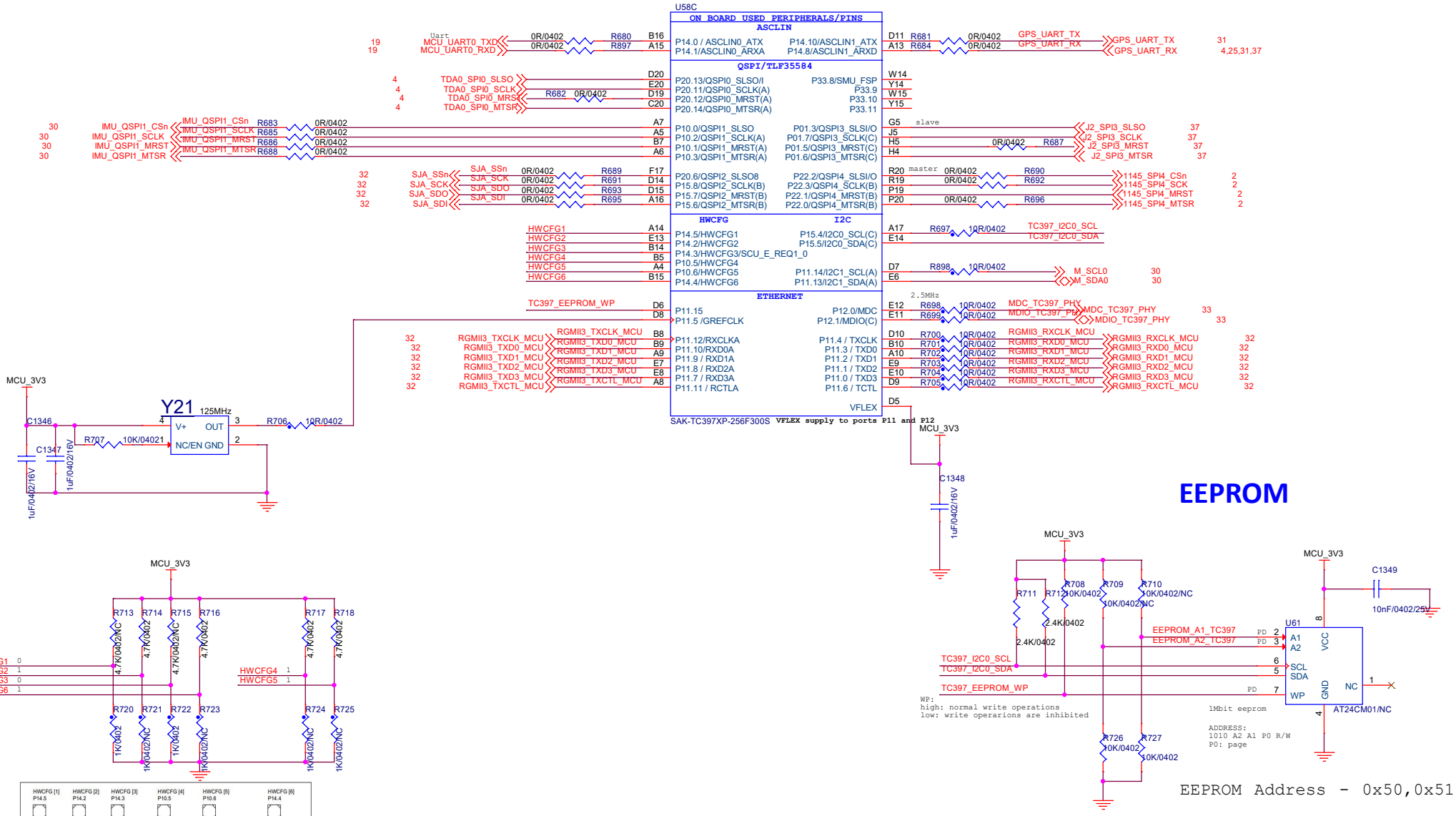
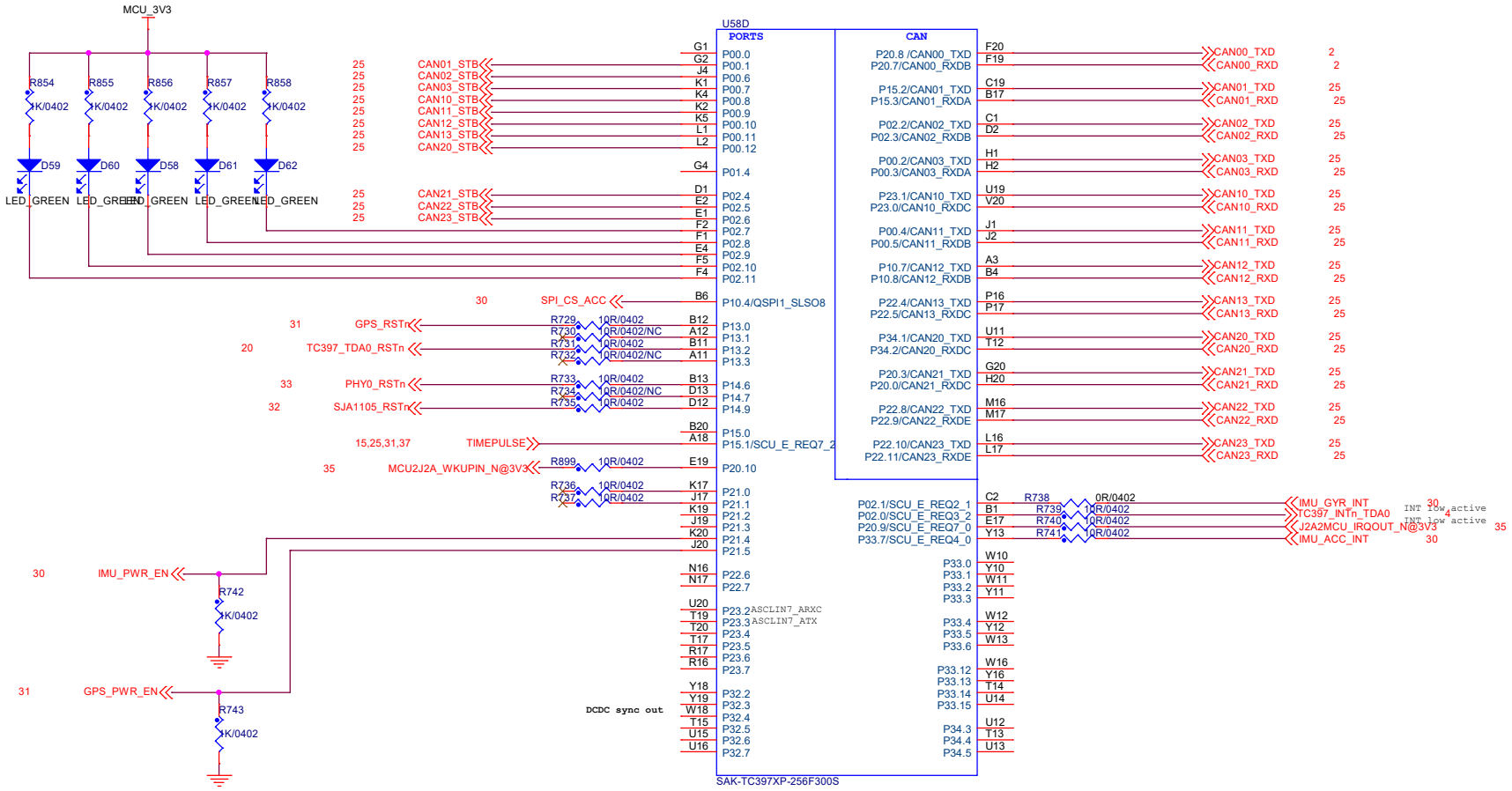
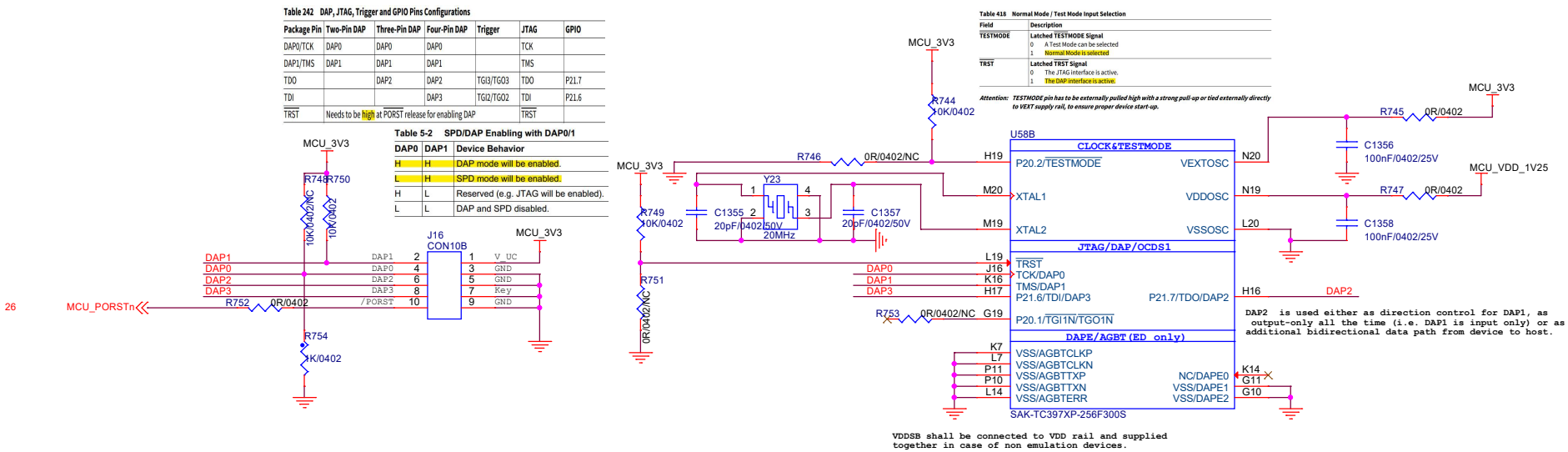
Size A3	Document Number P26-TC397 Power
Rev	V4.0
Date: Thursday, September 17, 2020	Sheet 26 of 40



HoloMatic 禾多科技	
Title	HoloArk_V40
Size A3	Document Number P27-TC397 Peripherals
Rev	V4.0
Date:	Thursday, September 17, 2020
Sheet	27 of 40



HoloMatic 禾多科技	
Title	HoloArk_V40
Size A3	Document Number P28-TC397 CAN/GPIO Rev V4.0
Date: Thursday, September 17, 2020	Sheet 28 of 40



HoloMatic 禾多科技			
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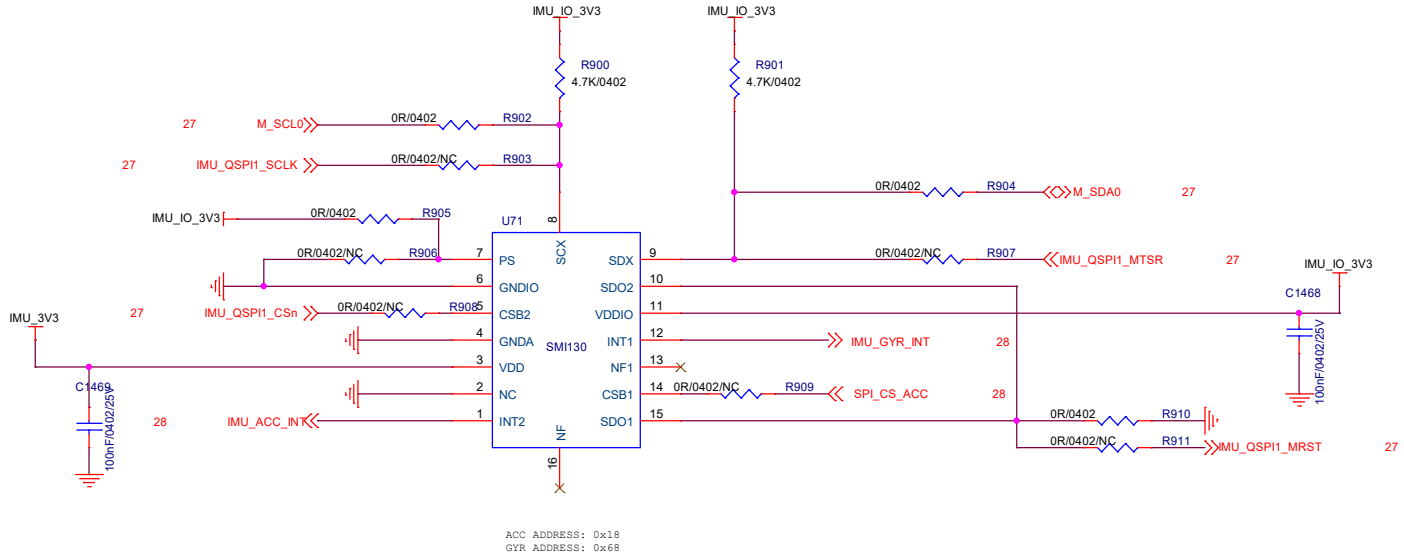
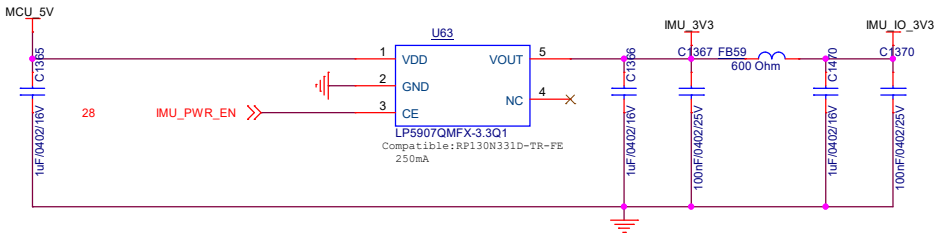
Size: A3	Document Number: P29-TC397 Debug		Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 29 of 40		





HoloMatic 禾多科技		
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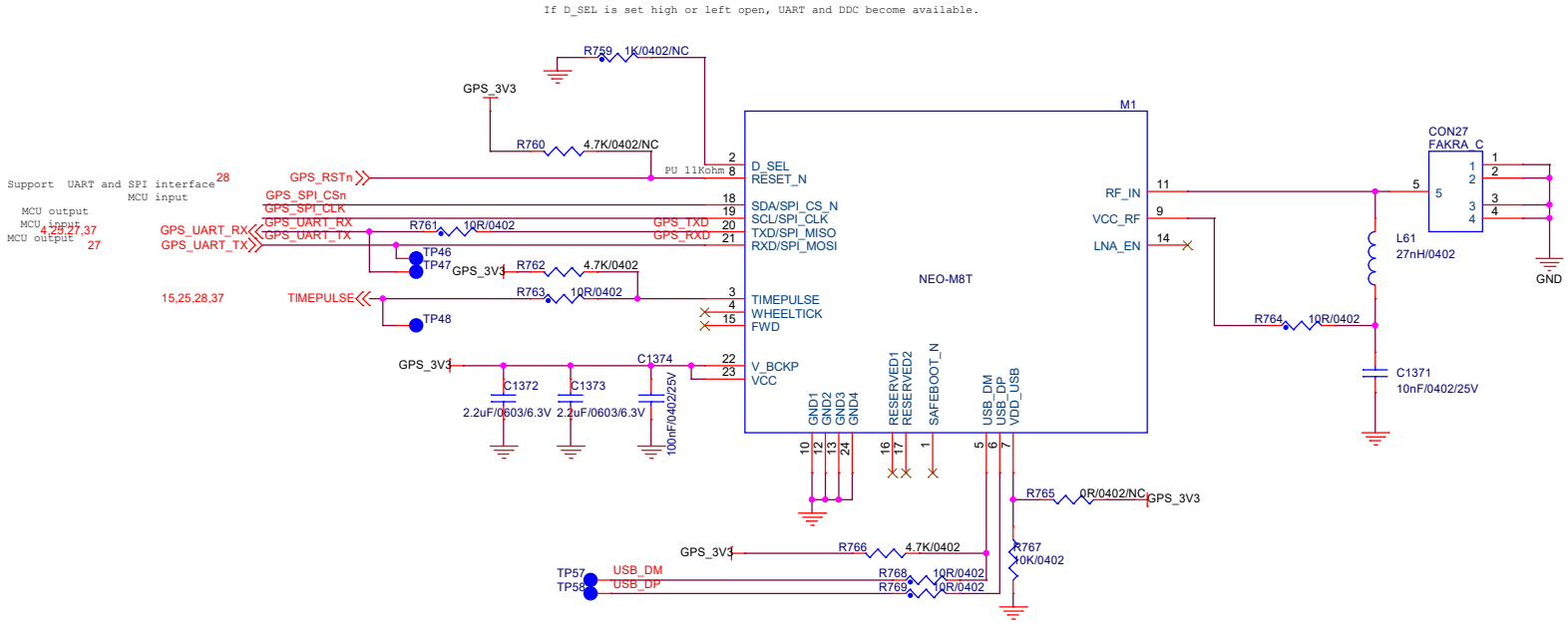
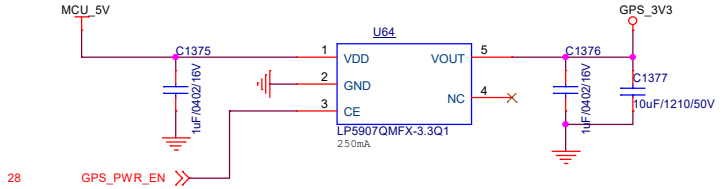
Size: A3	Document Number: P30-IMU	Rev: V4.0
Date: Thursday, September 17, 2020	Sheet 30 of 40	



8 Default messages

Interface	Settings
UART Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only the following NMEA (and no UBX) messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, TXT**
USB Output	Configured to transmit both NMEA and UBX protocols, but only the following NMEA (and no UBX) messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, VTG, TXT** USB Power Mode: Bus Powered
UART Input	9600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: UBX, NMEA, RTCM The GNSS receiver supports interleaved UBX and NMEA messages.
USB Input	Automatically accepts following protocols without need of explicit configuration: UBX, NMEA The GPS receiver supports interleaved UBX and NMEA messages. USB Power Mode: Bus Powered
DDC	Fully compatible with the I²C industry standard, available for communication with an external host CPU or u-blox cellular modules, operated in slave mode only. Default messages activated. NMEA and UBX are enabled as input messages, only NMEA as output messages. Maximum bit rate 400 kb/s.
SPI	Allow communication to a host CPU, operated in slave mode only. Default messages activated. SPI is not available in the default configuration.
TIMEPULSE	disabled



HoloMatic 禾多科技

Title	HoloArk_V40	
Size A3	Document Number P31-GPS	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 31 of 40	

RGMII 50ohm/200mil

MAC to MAC R <-->T T<-->R

The SJA1105S's internal MACs only supports full duples operation.

U65A

SJA1105QEL

U65B

SJA1105QEL

Symbol	Description	Min [V]	Typ [V]	Max [V]
VDD_CORE	1.2 V core voltage	1.14	1.20	1.30
VDDA_OSC	1.2 V oscillator supply	1.10	1.20	1.30
VDDA_PLL	1.2 V PLL supply	1.10	1.20	1.30
VDDIO_MIIx	MII mode	3.00	3.30	3.60
		2.30	2.50	2.70
		1.65	1.80	1.95
	RMII mode	3.00	3.30	3.60
		2.30	2.50	2.70
	RGMII mode	3.00	3.30	3.60
		2.30	2.50	2.70
		1.65	1.80	1.95
VDDA_SGMII	Analog SGMII supply voltage	2.3	2.5	2.7
VDDD_SGMII	Digital SGMII supply voltage	1.14	1.2	1.3
VDDIO_HOST	Host interface supply voltage			
	1.8 V operation	1.65	1.8	1.95
	2.5 V operation	2.3	2.5	2.7
	3.3 V operation	3.0	3.3	3.6
VDDIO_CLO	Voltage supply depends on CLK_OUT pin connection to other chip (i.e. TJA1102 or SJA1105PQRS)			
	1.8 V operation	1.65	1.8	1.95
	2.5 V operation	2.3	2.5	2.7
	3.3 V operation	3.0	3.3	3.6

Table 2. Voltage requirement overview

Fig 10. Reset timing

Title	HoloArk_V40
Size	A3
Document Number	P32-Eth switch
Rev	V4.0
Date:	Thursday, September 17, 2020
Sheet	32 of 40

HoloMatic 禾多科技

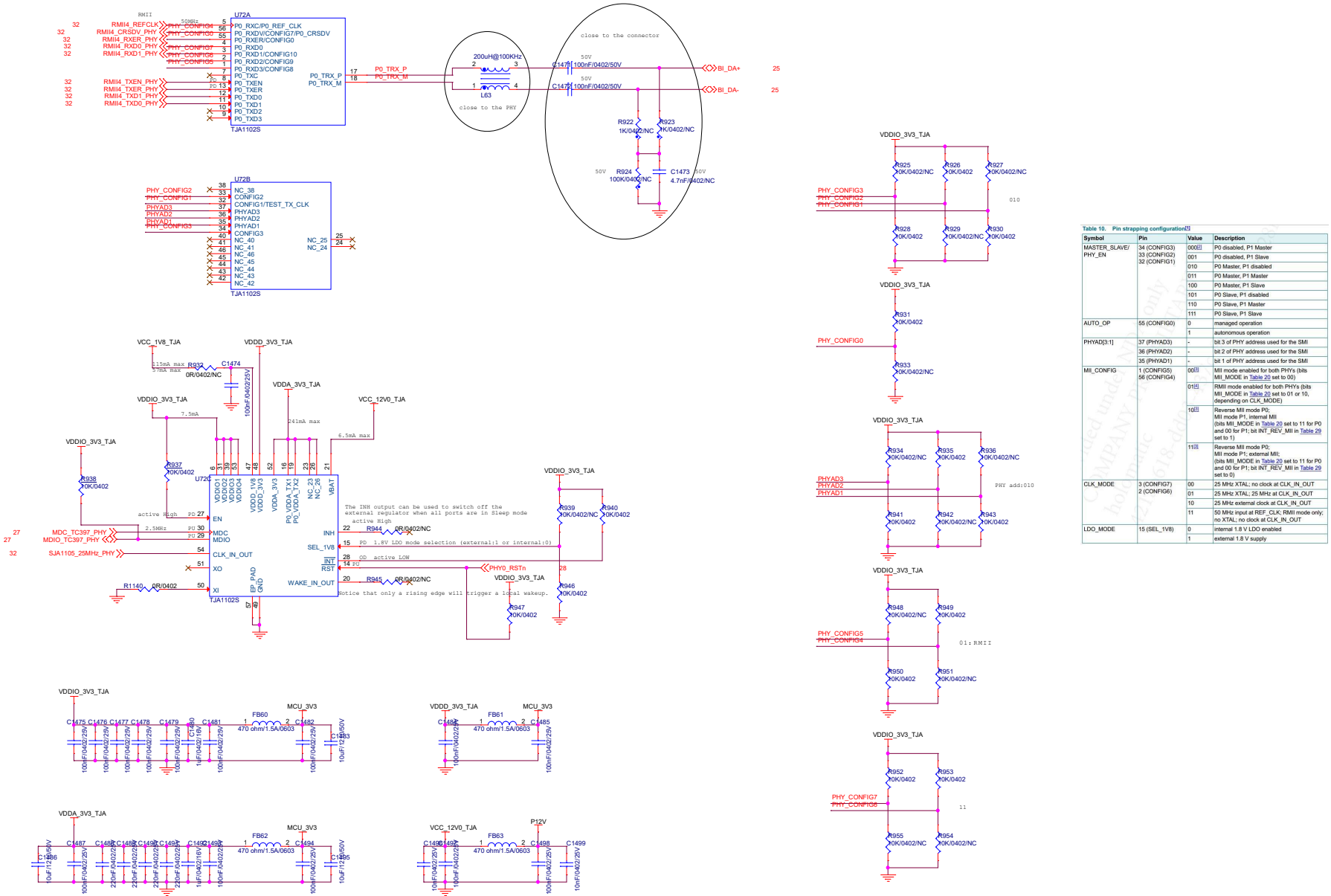
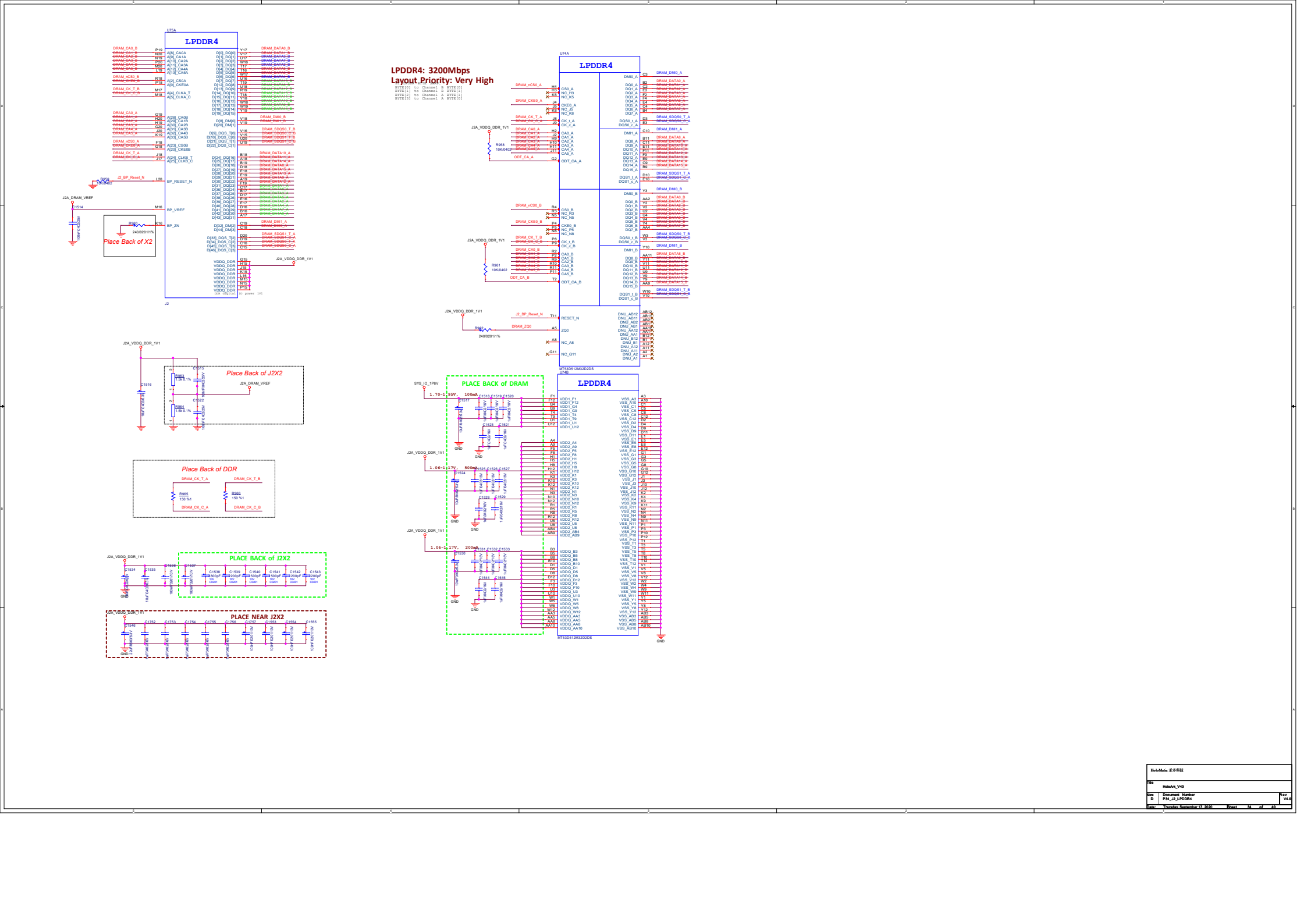


Table 10. Pin strapping configuration[1]			
Symbol	**Pin**	**Value**	**Description**
MASTER_SLAVE/ PHY_EN	34 (CONFIG3) 33 (CONFIG2) 32 (CONFIG1)	000[2]	P0 disabled, P1 Master
		001	P0 disabled, P1 Slave
		010	P0 Master, P1 disabled
		011	P0 Master, P1 Master
		100	P0 Master, P1 Slave
		101	P0 Slave, P1 disabled
		110	P0 Slave, P1 Master
		111	P0 Slave, P1 Slave
AUTO_OP	55 (CONFIG0)	0	managed operation
		1	autonomous operation
PHYAD[3:1]	37 (PHYAD3)	-	bit 3 of PHY address used for the SMI
	36 (PHYAD2)	-	bit 2 of PHY address used for the SMI
	35 (PHYAD1)	-	bit 1 of PHY address used for the SMI
MII_CONFIG	1 (CONFIG5) 56 (CONFIG4)	00[3]	MII mode enabled for both PHYs (bits MII_MODE in Table 20 set to 00)
		01[4]	RMII mode enabled for both PHYs (bits MII_MODE in Table 20 set to 01 or 10, depending on CLK_MODE)
		10[3]	Reverse MII mode P0; MII mode P1; internal MII (bits MII_MODE in Table 20 set to 11 for P0 and 00 for P1; bit INT_REV_MII in Table 29 set to 1)
		11[3]	Reverse MII mode P0; MII mode P1; external MII; (bits MII_MODE in Table 20 set to 11 for P0 and 00 for P1; bit INT_REV_MII in Table 29 set to 0)
CLK_MODE	3 (CONFIG7) 2 (CONFIG6)	00	25 MHz XTAL; no clock at CLK_IN_OUT
		01	25 MHz XTAL; 25 MHz at CLK_IN_OUT
		10	25 MHz external clock at CLK_IN_OUT
		11	50 MHz input at REF_CLK; RMII mode only; no XTAL; no clock at CLK_IN_OUT
LDO_MODE	15 (SEL_1V8)	0	internal 1.8 V LDO enabled
		1	external 1.8 V supply

HoloMatic 禾多科技	
Title	HoloArk_V40
Size: A2	Document Number: P33_TJA1102S
Rev	V4.0
Date: Thursday, September 17, 2020	Sheet 33 of 40


LPDDR4: 3200Mbps
Layout Priority: Very High
LPDDR4
Place Back of X2
Place Back of J2X2
Place Back of DDR
PLACE BACK of J2X2
PLACE NEAR J2X2
PLACE BACK of DRAM
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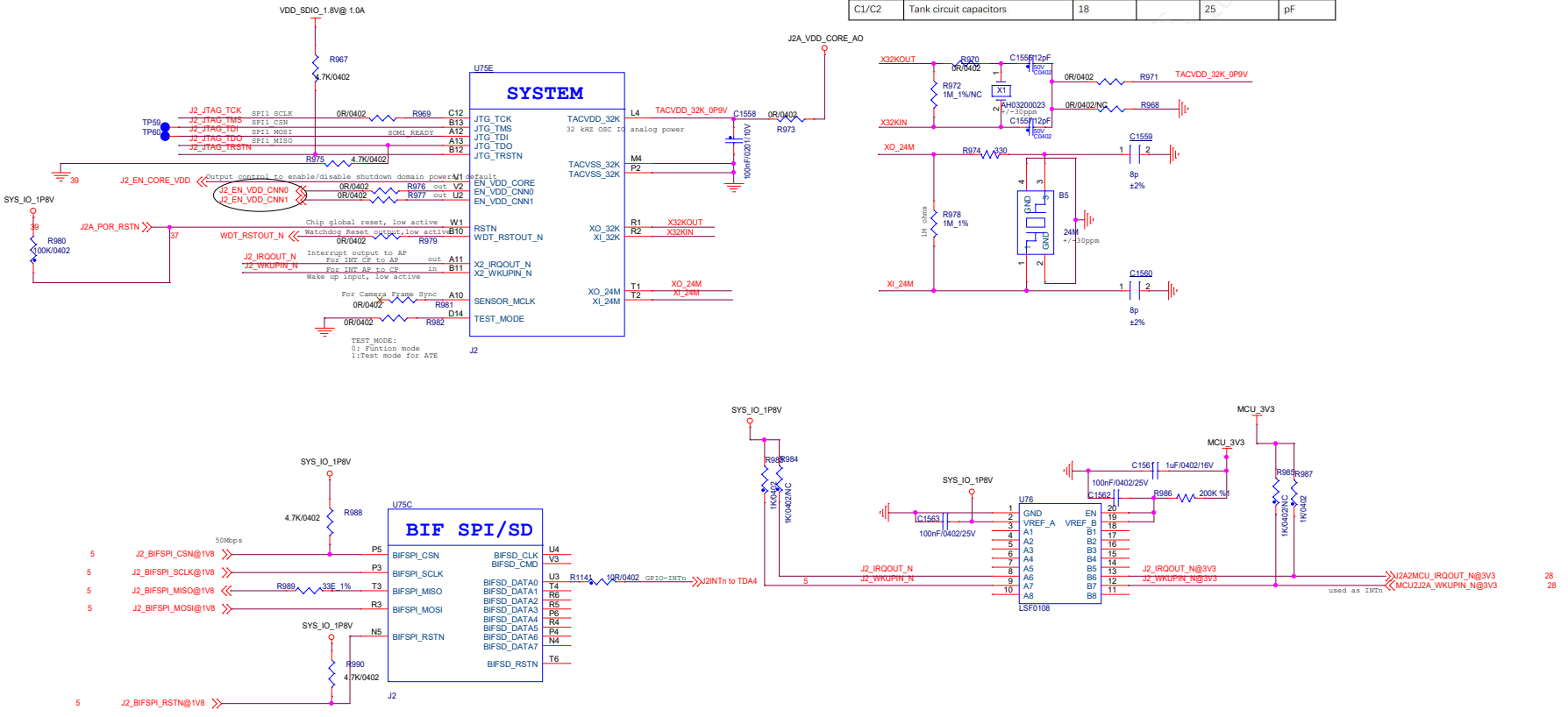
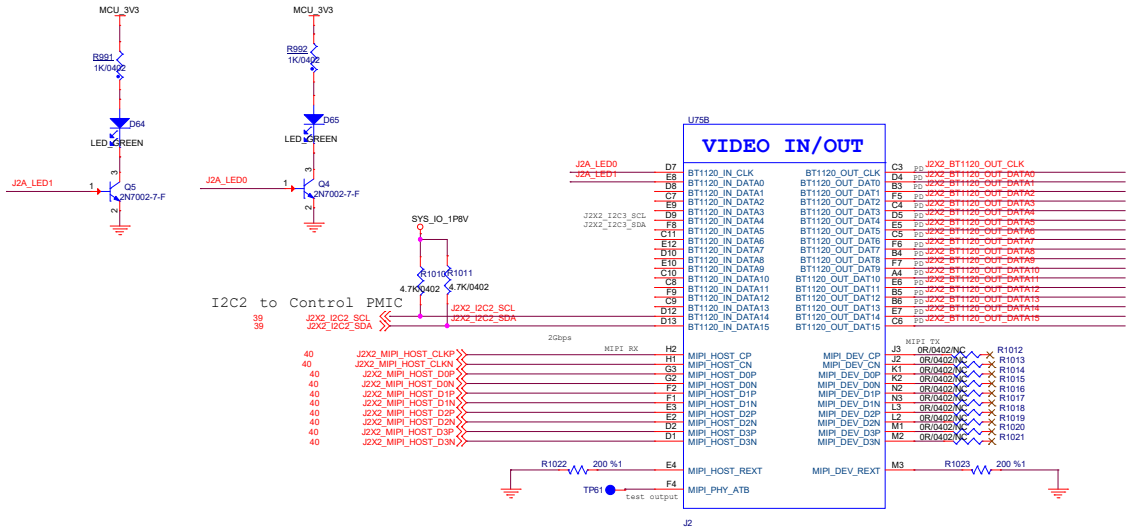
HoloArk_V40
P34_J2_LPDDR4
Thursday, September 17, 2020

Table 2-13 32K OSC IO Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Freq	Frequency		32768		Hz
Duty	Duty cycle	40	50	60	%
ESR	Crystal maximum ESR	90		180	Ω
C1/C2	Tank circuit capacitors	18		25	pF



HoloMatic 禾多科技		
Title	HoloArk_V40	
Size C	Document Number P35_J2_SYS	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 35 of 40	



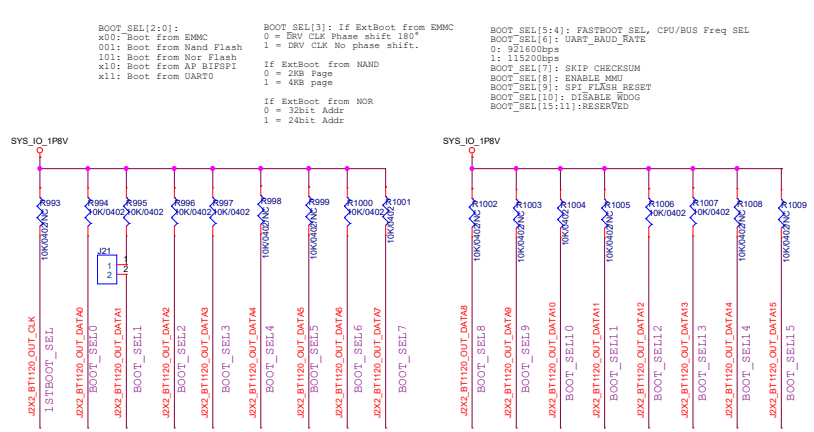
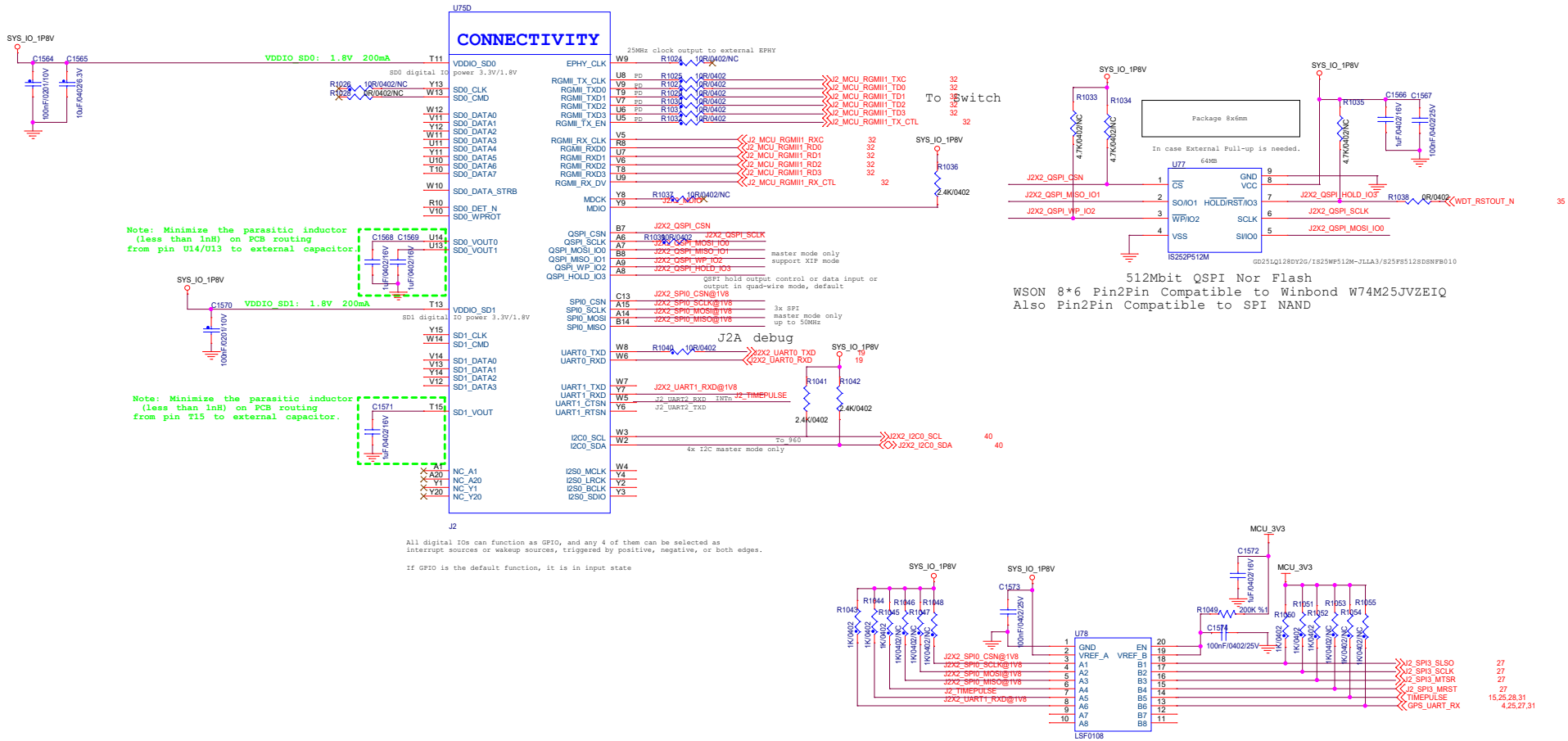


Table 1-1 Strap Pin Definition

Strap Pin	Shared with	Default	Function
1STBOOT_SEL	BT1120_OUT_CLK	0	0 = 1st boot from on-chip ROM. 1 = 1st boot from off-chip SPI NOR XIP.
2NDBOOT_SEL	BT1120_OUT_DAT[1:0]	00	00 = 2nd boot from eMMC (SD0). 01 = 2nd boot from SPI Flash (QSPI). 10 = 2nd boot from AP BIF-SPI. 11 = 2nd boot from UART0 XMODEM.
SPI_FLASH_TYPE	BT1120_OUT_DAT2	0	Only valid if 2NDBOOT_SEL=SPI Flash, 0 = SPI NAND. 1 = SPI NOR.
DEVICE_MODE	BT1120_OUT_DAT3	0	If 2NDBOOT_SEL = eMMC: 0 = Uses negedge drive, posedge capture. 1 = Uses posedge drive, posedge capture. If 2NDBOOT_SEL = SPI NAND: 0 = 2 KB page size. 1 = 4 KB page size. If 2NDBOOT_SEL = SPI NOR: 0 = 32-bit address mode. 1 = 24-bit address mode. If 2NDBOOT_SEL = others: 0 = N/A. 1 = N/A.
FASTBOOT_SEL	BT1120_OUT_DAT[5:4]	00	Switches CPU clock frequency and internal bus clock frequency. 00 = "cpu_clk = 1G, ace_aclk =sys_noc_aclk = 500M, sys_pclk = cx_dbgclk = 333M." 01 = "cpu_clk=500M, ace_aclk = sys_noc_aclk = 250M, sys_pclk = cx_dbgclk = 166M." 10 = "cpu_clk = 333M ace_aclk = sys_noc_aclk = 333M, sys_pclk = cx_dbgclk = 333M." 11 = "No clock switching, cpu_clk=24M, ace_aclk = sys_noc_aclk = 12M, sys_pclk = cx_dbgclk = 8M."
UART_BAUD_RATE	BT1120_OUT_DAT6	0	UART0 baud rate for debug print and XMODEM transfer.
SKIP_CHECKSUM	BT1120_OUT_DAT7	0	Whether validate checksum. 0 = Validates every one. 1 = Ignores checksum, easy for debugging.
RESERVED	BT1120_OUT_DAT8	0	RESERVED
SPI_FLASH_RESET	BT1120_OUT_DAT9	0	Only valid if 2NDBOOT_SEL=SPI Flash. 0 = No reset. 1 = Initiates a reset before accessing SPI NAND/NOR Flash.
DISABLE_WDOG	BT1120_OUT_DAT10	0	Whether enable watchdog protection 0 = Watchdog enabled for clock switching, resets the entire chip when program runaway occurs. 1 = Watchdog disabled.
SPI_NAND_RDID	BT1120_OUT_DAT11	0	Only valid if 2NDBOOT_SEL = SPI NAND. 0 = RDID command has dummy byte. 1 = RDID command has no dummy byte.
NAND_2PLANES	BT1120_OUT_DAT12	0	Only valid if 2NDBOOT_SEL = SPI NAND. 0 = SPI NAND has only 1 plane and no plane select in 03H command. 1 = SPI NAND has 2 planes and the plane select bit in 03H command.
RESERVED	BT1120_OUT_DAT13	0	Reserved for future use (RFU).
RESERVED	BT1120_OUT_DAT14	0	RFU.
RESERVED	BT1120_OUT_DAT15	0	RFU.

HoloMatic 禾多科技	
Title	HoloArk_V40
Size: A2	Document Number: P36-J2-Video
Rev	V4.0
Date: Thursday, September 17, 2020	Sheet 36 of 40



HoloMatic 禾多科技		
Title	HoloArk_V40	
Size C	Document Number P37_J2_Peripheral	Rev V4.0
Date: Thursday, September 17, 2020	Sheet 37 of 40	

Power OF X2_J2

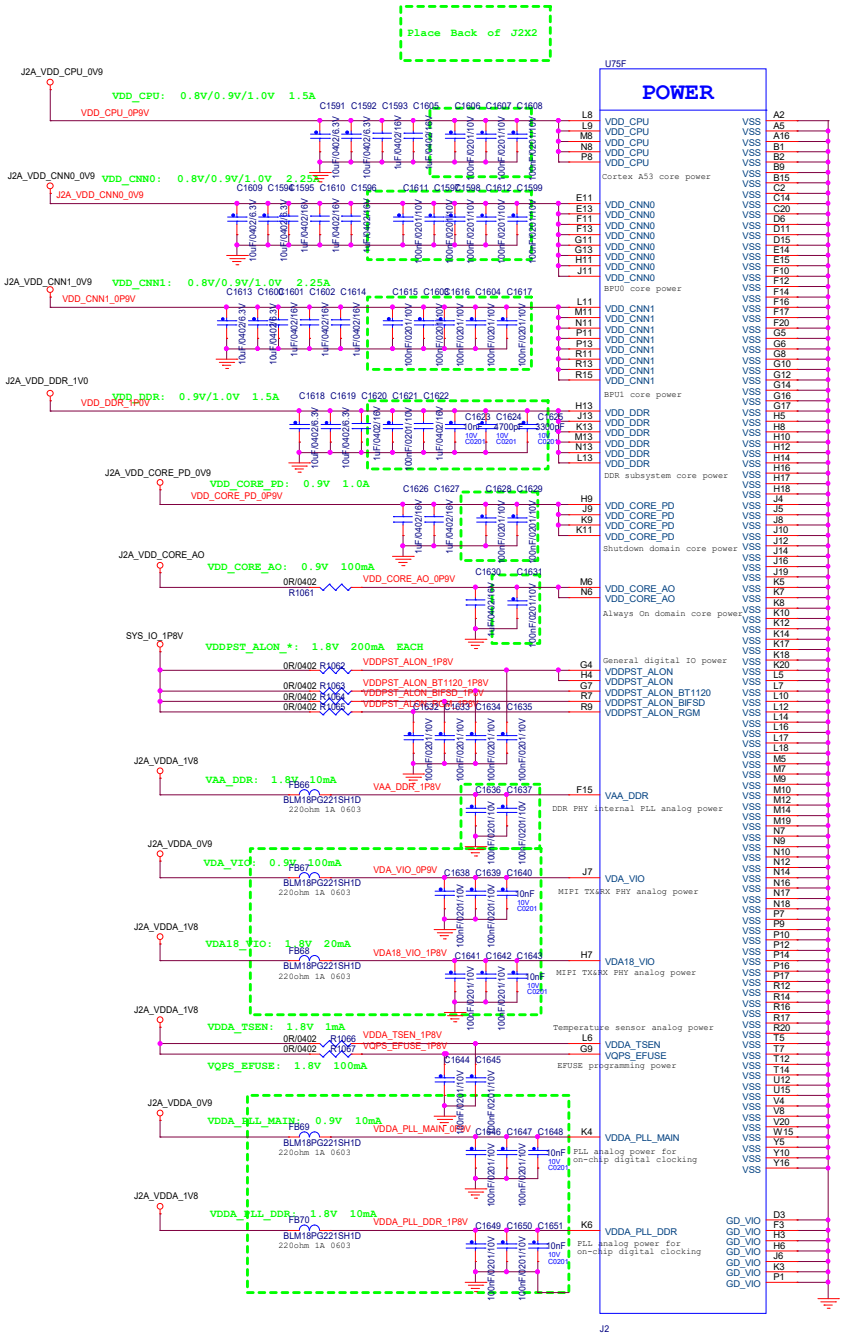


Table 3-9 Power Groups

Power	Voltage	Property	Max Ramp Rate
Group 1			
VDDPST_ALON VDDPST_ALON_BIFSD VDDPST_ALON_RGMII VDDPST_ALON_BT1120OUT	1.8 V	Always-on	< 5 mV/us
VDDIO_SD0 VDDIO_SD1	1.8 V/3.3 V	Always-on	
VDDQ_DDR	1.1 V (LPDDR4)	Always-on	
Group 2			
VDD_CORE_AO TACVDD_32K	0.9 V	Always-on	< 5 mV/us
Group 3			
VDD_CORE_PD	0.9 V	Powered-down	< 5 mV/us
VDD_CPU	0.9/1.0V		
VDD_CNN0	0.9/1.0V		
VDD_CNN1	0.9/1.0V		
VDD_DDR	0.9/1.0 V		
Group 4			
VDDA_PLL_MAIN VDA_VIO	0.9 V	Powered-down	< 5 mV/us
VDDA_PLL_DDR VAA_DDR VDA18_VIO VDDA_TSEN VQPS_EFUSE	1.8 V	Powered-down	

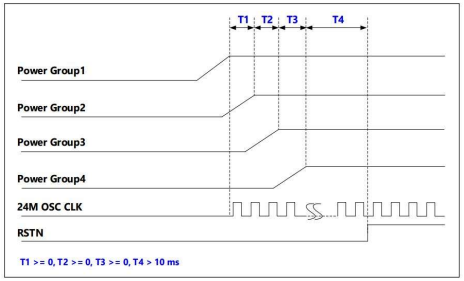
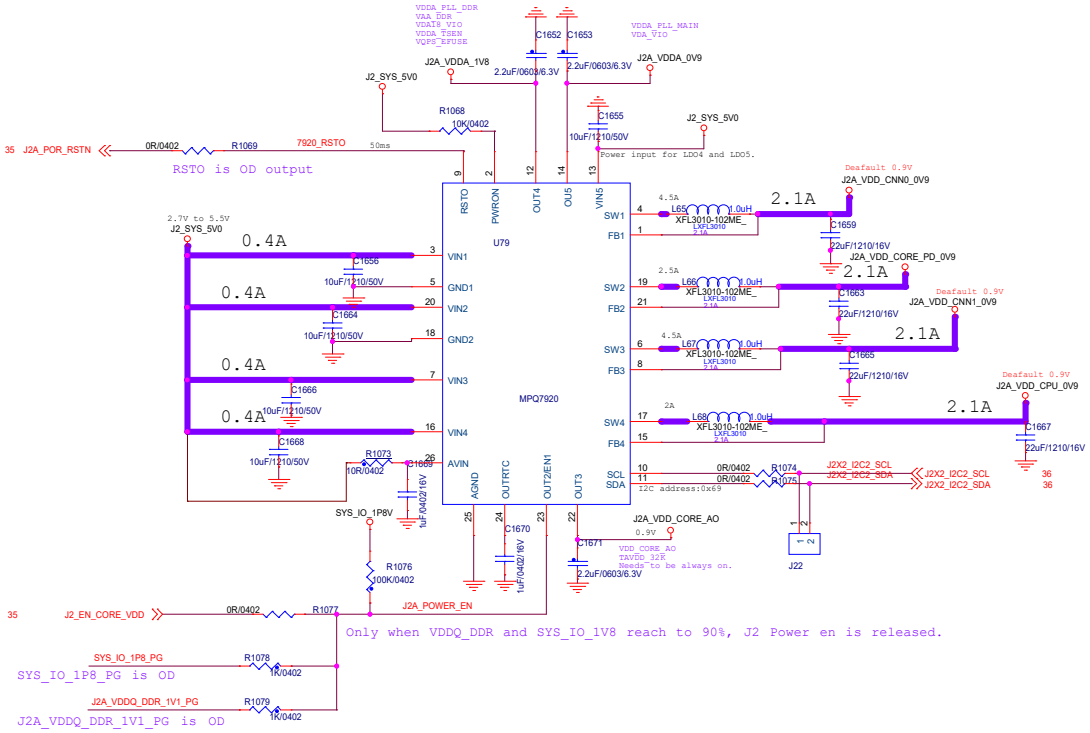
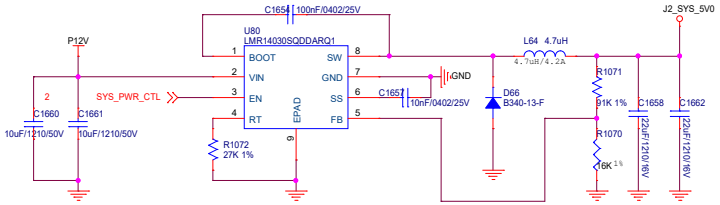


Figure 3-9 Power-Up Sequence

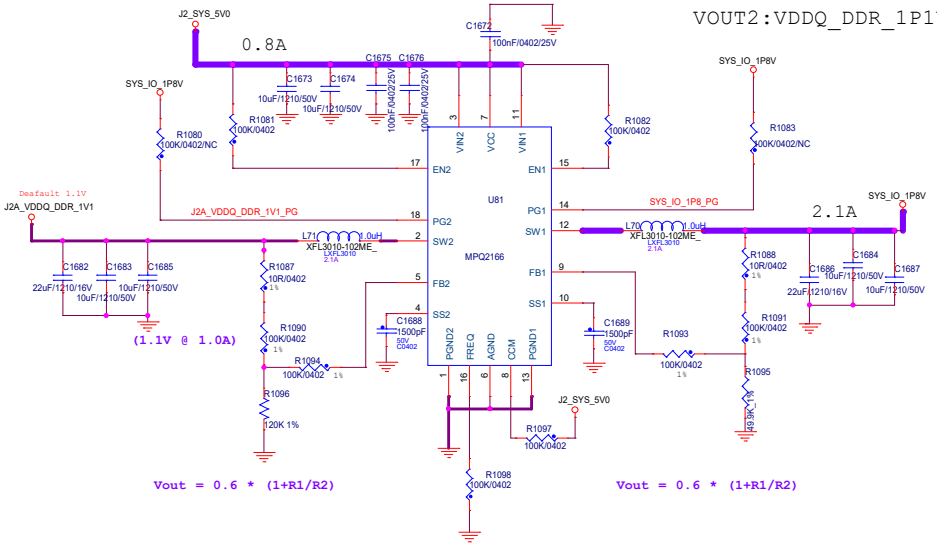
HoloMatic 禾多科技			
Title	HoloArk_V40		
Size C	Document Number P38_J2_Power&GND		Rev V4.0
Date: Thursday, September 17, 2020		Sheet 38 of 40	



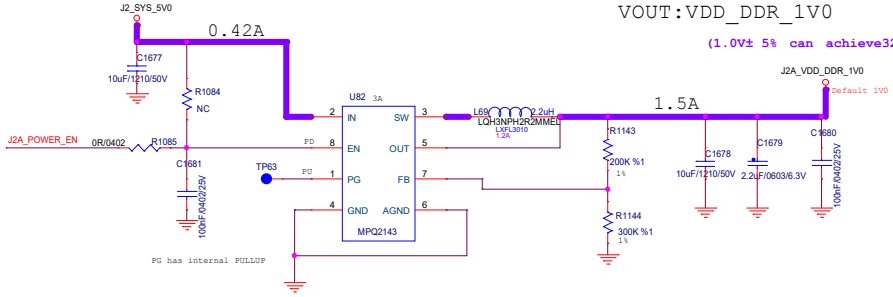


	OTP Items	Buck1	Buck2	Buck3	Buck4	LDORTC	LDO2	LDO3	LDO4	LDO5
2	Switching Frequency(MHz)	1.65								
3	Output Voltage(V)	0.9	0.9	0.9	0.9	3	EN	0.9	1.8	0.9
4	Iout max(A)	2.25	1.5	2.25	2	0.01	xx	0.3	0.3	0.3
5	Initial On/off	ON	ON	ON	ON	ON	xx	ON	ON	ON
6	MODE	FPWM Mode	FPWM Mode	FPWM Mode	FPWM Mode	N/A				
7	Power On Delay	8ms	8ms	8ms	8ms	Always on	xx	0ms	12ms	12ms
8	Automatic turn-on	Yes								
9	PWR_ON	0 (level trigger)								
10	RSTODELAY	50ms								
11	Buck1 Peak current limit	01 (6.6A)								
12	Buck2 Peak current limit	01 (4A)								
13	Buck3 Peak current limit	01 (6.6A)								
14	Buck4 Peak current limit	01 (4A)								
15										
16	Other parameters which user should enter									
17	Input voltage_Min.(V)	3.5								
18	Input voltage_Typ.(V)	5								
19	Input voltage_Max.(V)	6								
20										
21	Other requirement:									
22	1. PWRON will not use.									
23	2. Use LDO2 (OUT2/EN1PIN) as EN to control buck1 buck2 buck3 buck4 LDO4 and LDO5 together.									

VOUT1: SYSTEM 1P8V
VOUT2:VDDQ_DDR_1P1V



VOUT:VDD_DDR_1V0
(1.0V± 5% can achieve3200Mbps)



HoloMatic 禾多科技	
Title	HoloArk_V40
Size C	Document Number P39_J2_Power for J2
Rev	V4.0
Date:	Thursday, September 17, 2020
Sheet	39 of 40

表 18. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.80 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	0x30	0x60
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	0x32	0x64
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	0x34	0x68
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	0x36	0x6C
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	0x38	0x70
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	0x3A	0x74
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	0x3C	0x78
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0x3D	0x7A