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Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits

TIA/EIA-644-A

(Revision of TIA/EIA-644)

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(From Standards Proposal No. 4584, formulated under the cognizance of the TIA TR-30.2 Subcommittee on DTE-DCE Interfaces Protocols.)

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ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS

(From TIA/EIA Standard TIA/EIA-644 and Standards Proposal
No. 4584 formulated under the cognizance of TIA
Subcommittee TR-30.2 on Data Transmission Interfaces and Protocols)

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FOREWORD

(This foreword is not part of this Standard)

This Standard was formulated under the cognizance of TIA Subcommittee TR-30.2 on Data Transmission Interfaces.

This Standard was developed in response to a demand from the data communications community for a general-purpose high-speed interface standard for use in high throughput DTE-DCE interfaces.

The voltage levels specified in this Standard were specified such that maximum flexibility would be provided, while providing a low power, high speed, differential interface. Generator output characteristics are independent of power supply, and may be designed for standard +5 V, +3.3 V or even power supplies as low as +2.5 V. Integrated circuit technology may be BiCMOS, CMOS, or GaAs technology. The low voltage (330 mV) swing limits power dissipation, while also reducing radiation of EMI signals. Differential signaling provides multiple benefits over single-ended signaling, notably common-mode rejection, and magnetic canceling.

Additional specifications for multidrop applications have been incorporated into TIA/EIA-644-A. A full load test measurement for the generator and a balance test of receiver input current have been added to this revision. A survey of devices conforming to TIA/EIA-644 currently available are able to meet the additional requirements of TIA/EIA-644-A.

This Standard includes two Annexes, both are informative only. Annex A provides guidelines for application, addressing data signaling rate and cable length issues. Annex B provides comparison information with other interface standards, and related standards.

1 SCOPE

This Standard specifies the electrical characteristics of low voltage differential signaling interface circuits, normally implemented in integrated circuit technology, that may be employed when specified for the interchange of binary signals between:

Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE),

Data Terminal Equipment (DTE) and Data Terminal Equipment (DTE),

or in any point-to-point, or multidrop interconnection of binary signals between equipment.

The interface circuit includes a generator connected by a balanced interconnecting media to a load consisting of a termination impedance and a receiver(s). The interface configuration is a point-to-point or multidrop interface. The electrical characteristics of the circuit are specified in terms of required voltage, and current values obtained from direct measurements of the generator and receiver (load) components at the interface points.

The logic function of the generator and the receiver is not defined by this Standard, as it is application dependent. The generators and receivers may be inverting, non-inverting, or may include other digital blocks such as parallel-to-serial or serial-to-parallel converters to boost the data signaling rate on the interchange circuit as required by the application.

Minimum performance requirements for the balanced interconnecting media are furnished. Guidance is given in Annex A, Section A.2 with respect to limitations on data signaling rate imposed by the parameters of the cable length, attenuation, and crosstalk for individual installations for a typical cable media interface.

It is intended that this Standard will be referenced by other standards that specify the complete interface (i.e., connector, pin assignments, function) for applications where the electrical characteristics of a low voltage differential signaling interface circuit is required. This Standard does not specify other characteristics of the DTE-DCE interface (such as signal quality, protocol, maximum data signaling rate, bus structure, and/or timing) essential for proper operation across the interface.

When this Standard is referenced by other standards or specifications, it should be noted that certain options are available. The preparer of those standards and specifications must determine and specify those optional features which are required for that application.

2 DEFINITIONS, SYMBOLS AND ABBREVIATIONS

For the purposes of this Standard, the following definitions, symbols and abbreviations apply:

2.1 Data signaling rate

Data signaling rate - expressed in the units b/s (bits per second), is the significant parameter. It may be different from the equipment's data transfer rate, which employs the same units. Data signaling rate is defined as $1/t_{ui}$ where t_{ui} is the minimum interval between two significant instants.

2.2 DTE

Data Terminal Equipment

2.3 DCE

Data Circuit-Terminating Equipment

2.4 LVDS

Low Voltage Differential Signaling

2.5 Star (*)

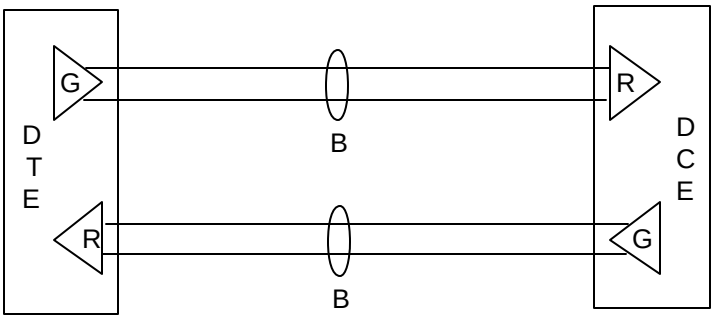
Star (*) - represents the opposite input condition for a parameter. For example, the symbol Q represents the receiver output state for one input condition, while Q* represents the output state for the opposite input state.

3 APPLICABILITY

3.1 General applicability

The provisions of this Standard may be applied to the circuits employed at the interface between equipments where information being conveyed is in the form of binary signals.

Typical points of applicability for this Standard are depicted in Figure 1.



Legend:

DTE = Data Terminal Equipment
DCE = Data Circuit-termination Equipment
G = Generator
R = Receiver
B = Balanced interconnecting media

Figure 1 - Application of LVDS interface circuits

The LVDS interface is intended for use where any of the following conditions prevail:

a. The data signaling rate is too great for effective unbalanced (single-ended) operation.

b. The data signaling rate exceeds the capability of TIA/EIA-422, TIA/EIA-485, or TIA/EIA-612 balanced (differential) electrical interfaces.

c. The balanced interconnecting media is exposed to extraneous noise sources that may cause an unwanted voltage up to ±1 V measured differentially between the signal conductor and circuit common at the load end of the cable with a 50 Ω resistor substituted for the generator.

d. It is necessary to minimize electromagnetic emissions and interference with other signals.

3.2 Data signaling rate

The LVDS interface circuit will normally be utilized on data and timing, or control circuits. Actual maximum data signaling rate is NOT defined by this Standard. The limit is

determined by the generator transition time characteristics, the media characteristics, the distance between the generator and the load, and the required signal quality.

A theoretical maximum limit is calculated at 1.923 Gb/s, and is derived from a calculation of signal transition time at the load assuming a loss-less balanced interconnecting media. The recommended signal transition time (t_r or t_f) at the load should not exceed 0.5 of the unit interval to preserve signal quality. This Standard specifies that the transition time of the generator into a test load be 260 ps or slower. Therefore, with the fastest generator transition time, and a loss-less balanced interconnecting media, and applying the 0.5 restriction, yields a minimum unit interval of 520 ps or 1.923 Gb/s theoretical maximum data signaling rate. Employing a parallel bus structure (4, 8, 16, 32, etc. - bus width) can easily extend the obtainable equivalent bit rate into the multi-Gb/s range.

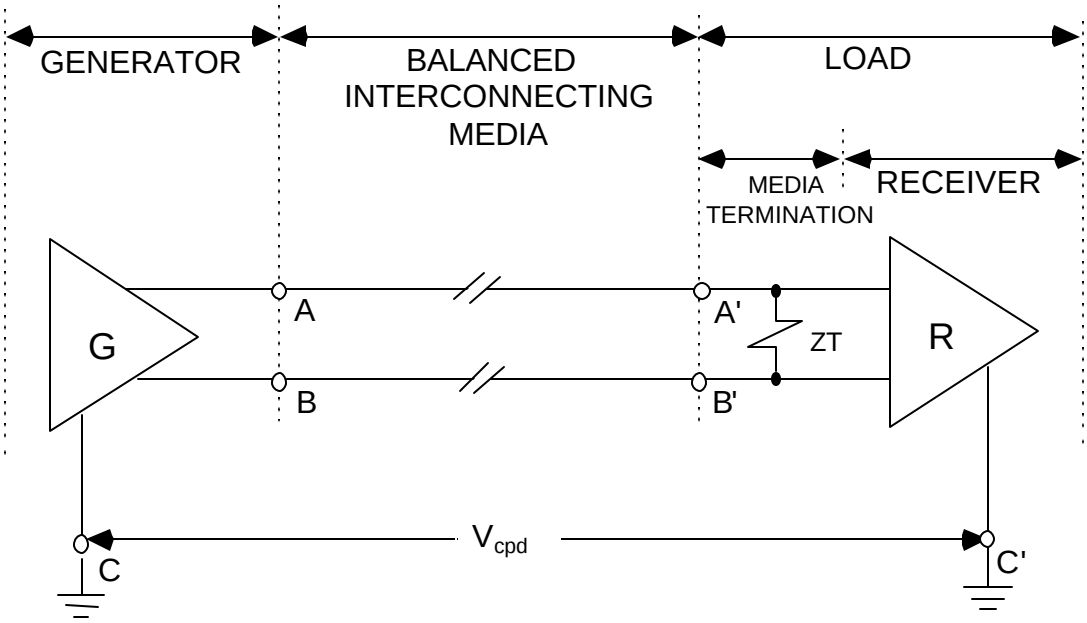
A recommended maximum data signaling rate is derived from a calculation of signal transition time at the load. For example, if a cable media is selected, a maximum signal rise time degradation is assumed to be 500 ps, since cables are not loss-less (500 ps represents a typical amount of rise time distortion on 5 meters of cable media). Therefore, allowing a 500 ps degradation of the signal in the interconnecting cable yields a 760 ps (fastest) signal at the load. Therefore, with the fastest generator transition time, and a cable with only 500 ps of signal degradation (transition time), and applying the 0.5 restriction, yields a minimum unit interval of 1.520 ns or 655 Mb/s recommended maximum data signaling rate based on this set of assumptions. Maximum data signaling rate is thus application dependent.

Generators and receivers meeting this Standard need not operate to the theoretical maximum data signaling rate. They may be designed to operate over narrower ranges that satisfy more economically specified applications, for example at lower data signaling rates. When a generator is limited to a narrower range of data signaling rates, the transition time of the generator may be slowed accordingly to limit noise generation. For example, at 100 Mb/s the generator's transition time should be in the range of 500 ps to 3 ns (5% to 30% of the unit interval), and the signal transition time at the load should not exceed 5 ns (50% of the unit interval).

While a restriction of maximum cable length in not specified, recommendations are given on how to determine the maximum data signaling rate for a typical cable media application (see A.2).

4 ELECTRICAL CHARACTERISTICS

An LVDS interface circuit is shown in Figure 2. The circuit consists of three parts: the generator (G), the balanced interconnecting media, and the load. The load is composed of a termination impedance and receiver(s) (R). A receiver may incorporate the termination impedance internal to the Integrated Circuit package. The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements while the balanced interconnecting media is described in terms of its electrical characteristics.



Legend:

G = Generator
R = Receiver
A = Generator interface point
A' = Receiver interface point
B = Generator interface point
B' = Receiver interface point
C = Generator circuit common
C' = Receiver circuit common
ZT = Termination impedance
V_{cpd} = Common potential difference

Figure 2 - LVDS interface circuit

4.1 Generator characteristics

The generator electrical characteristics are specified in accordance with the measurements illustrated in Figure 4 to Figure 9 and described in 4.1.1 through 4.1.5. The generator circuit meeting these requirements results in a balanced source that will produce a differential voltage across a test termination load of 100 Ω in the range of 250 mV to 450 mV.

The signaling sense of the voltages appearing across the termination resistor is defined in Figure 3 as follows:

a. The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 or OFF state.

b. The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 or ON state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

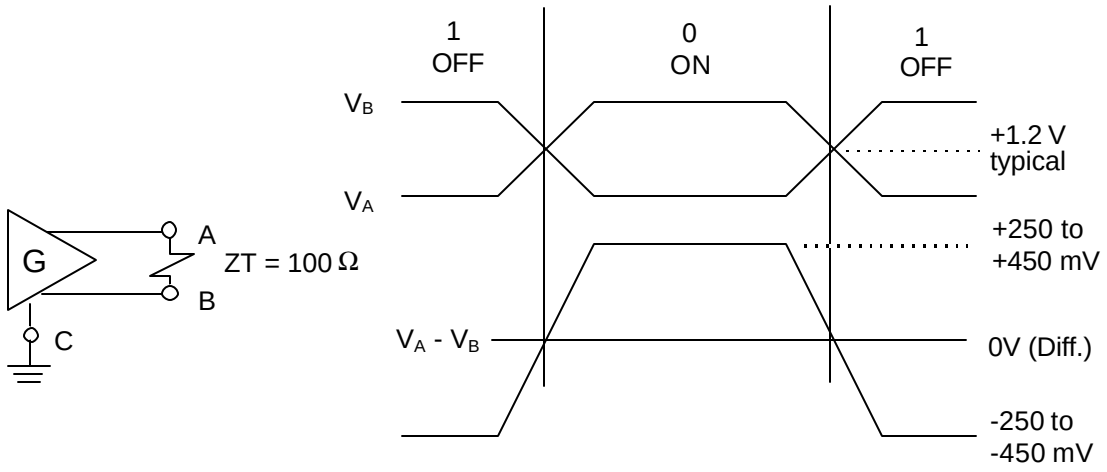


Figure 3 - Signaling sense

4.1.1 Full load test measurements

With a test load of three resistors, 100 Ω ±1% between the A and B generator output terminals, and 3.74 kΩ ±1% between each generator output terminal and a test supply (V_{TEST}), as shown in Figure 4, the steady-state magnitude of the differential output voltage (V_T), shall be greater than or equal to 247 mV and less than or equal to 454 mV with the test voltage varied from 0 V to +2.4 V. For the opposite binary state, the polarity of V_T shall be reversed (V_T *). The steady-state magnitude of the difference between V_T and V_T * shall be 50 mV or less.

$$247\ mV \leq |V_T| \leq 454\ mV$$

$$247\ mV \leq |V_T^*| \leq 454\ mV$$

$$|V_T| - |V_T^*| \leq 50\ mV$$

The 100 Ω resistor represents a typical termination load, and the 3.74 kΩ resistors represent the combined impedance of 32 receiver loads connected to the bus. The V_{TEST} power supply represents the allowable range of biasing that the receivers may present to the bus.

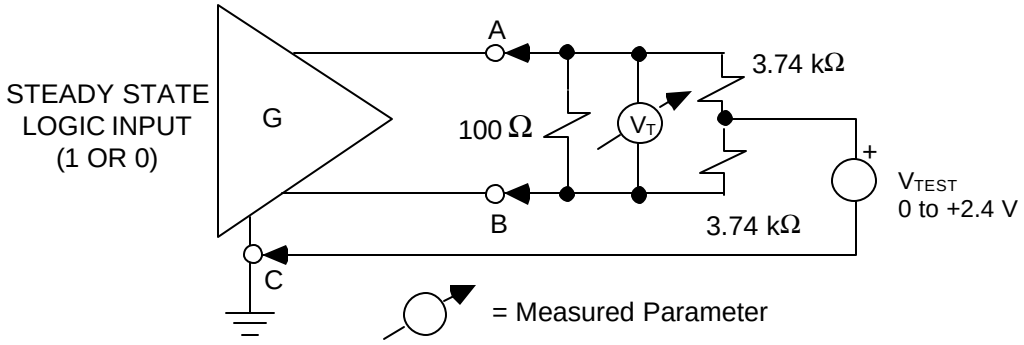


Figure 4 – Full load test measurements

4.1.2 Offset voltage and balance measurements

With a test load of two resistors, 49.9 Ω ±1% each, connected in series between the generator output terminals, the steady-state magnitude of the generator offset voltage (V_{OS}), measured between the center point of the test load and the generator circuit common shall be greater than or equal to 1.125 V and less than or equal to 1.375 V for either binary state. The steady-state magnitude of the difference of V_{OS} for one binary state and V_{OS} * for the opposite binary state shall be 50 mV or less.

$$1.125\ V \le V_{OS} \le 1.375\ V$$

$$1.125\ V \le V_{OS}^* \le 1.375\ V$$

$$|\ V_{OS} - V_{OS}^*\ | \le 50\ mV$$

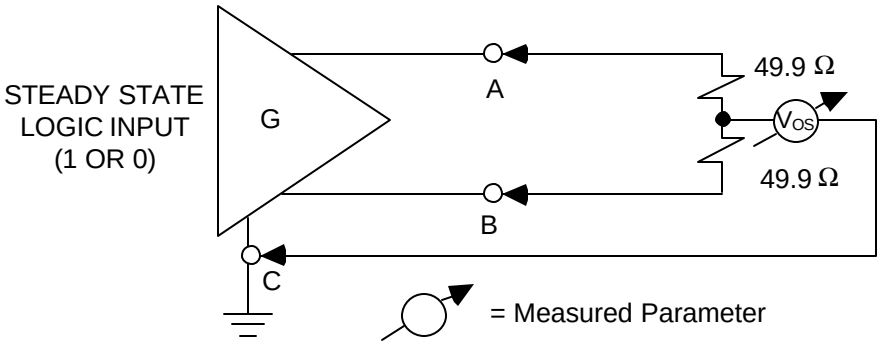


Figure 5 – Offset Voltage measurements

4.1.3 Short-circuit measurements

With the generator output terminals short-circuited to the generator circuit common, the magnitudes of the currents (I_{SA} and I_{SB}) following through each output terminal shall not exceed 24.0 mA for either binary state.

$$| I_{SA} | \leq 24.0 \text{ mA}$$

$$| I_{SB} | \leq 24.0 \text{ mA}$$

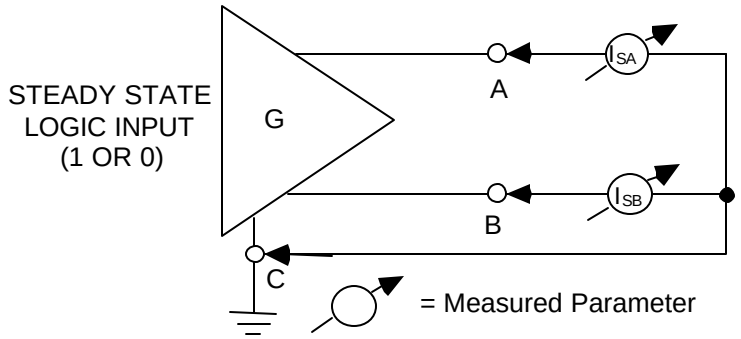


Figure 6 - Short-circuit measurements to circuit common

With the generator output terminals short-circuited to each other, the magnitude of the current (I_{SAB}) following through the output terminals shall not exceed 12.0 mA for either binary state.

$$| I_{SAB} | \leq 12.0 \text{ mA}$$

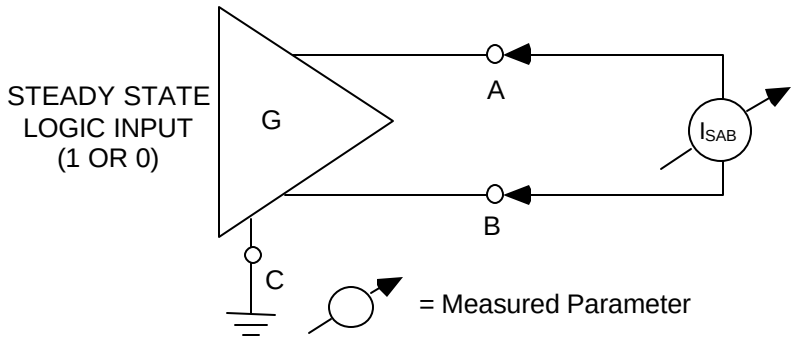


Figure 7 - Short-circuit measurements

4.1.4 Output signal waveform

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured across the 99.8 Ω ±1% test load (RL) connected as shown in Figure 8, shall be such that the voltage monotonically changes between 0.2 and 0.8 of V_{SS} and is less than or equal to 0.3 of the unit interval. Thereafter,

the signal voltage shall not vary more than ±20% of the steady-state value (V_{ring}), until the next binary transition occurs. Transition times shall not be less than 260 ps. Edge rates less than 260 ps are not recommended to minimize adverse effects of switching noise. V_{SS} is defined as the voltage difference between the two steady-state values of the generator output ($V_{SS} = 2|V_t|$). Measurement equipment used for compliance testing shall provide a bandwidth of 5 GHz minimum. Scope probe shall present at least 100 kΩ differential resistance with no more than 1 pF differential capacitance loading.

$$260 \text{ ps} \leq t_r \leq 0.3\ t_{ui}$$

$$260 \text{ ps} \leq t_f \leq 0.3\ t_{ui}$$

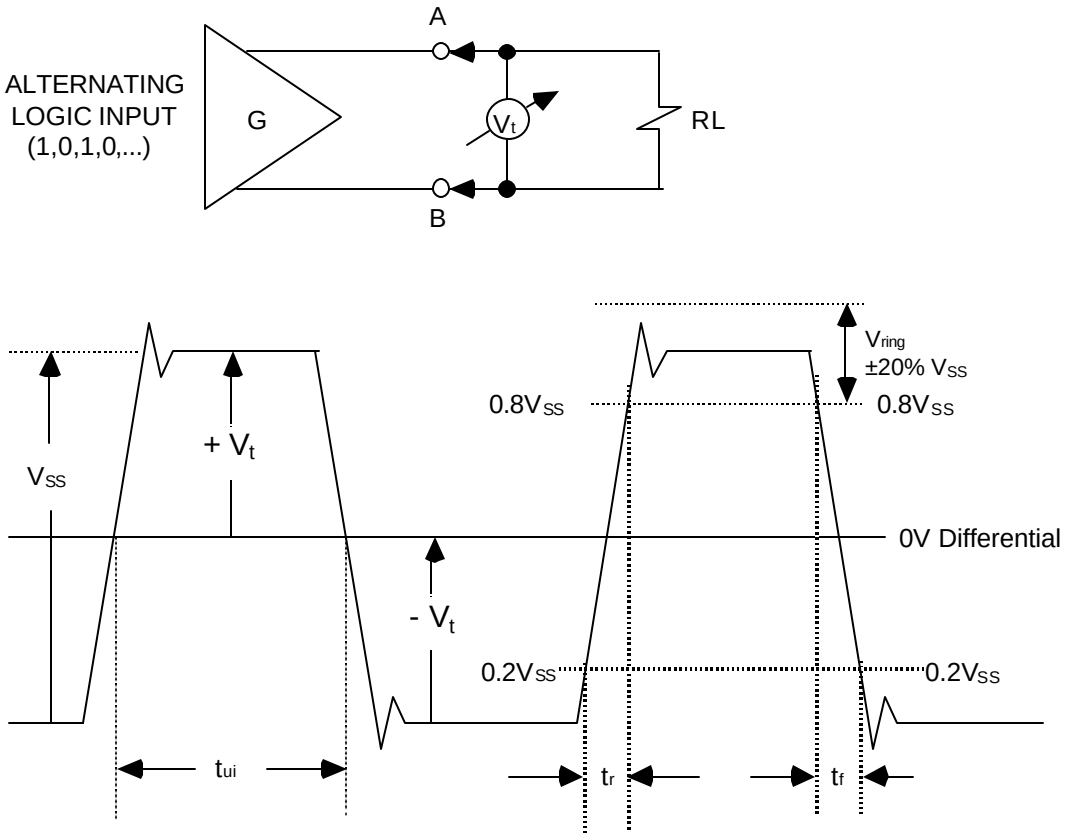


Figure 8 – Output signal waveform

4.1.5 Dynamic output signal balance

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the resulting imbalance of the offset voltage (V_{OS}) measured between the matched 49.9 Ω ±1% test load resistors (RL) to circuit common (C) as shown in Figure 9, should not vary more than 150 mV_{pp} (peak-to-peak). Measurement equipment used for

compliance testing shall provide a bandwidth of 5 GHz minimum. Scope probe shall present at least 100 kΩ differential resistance with no more than 1 pF differential capacitance loading.

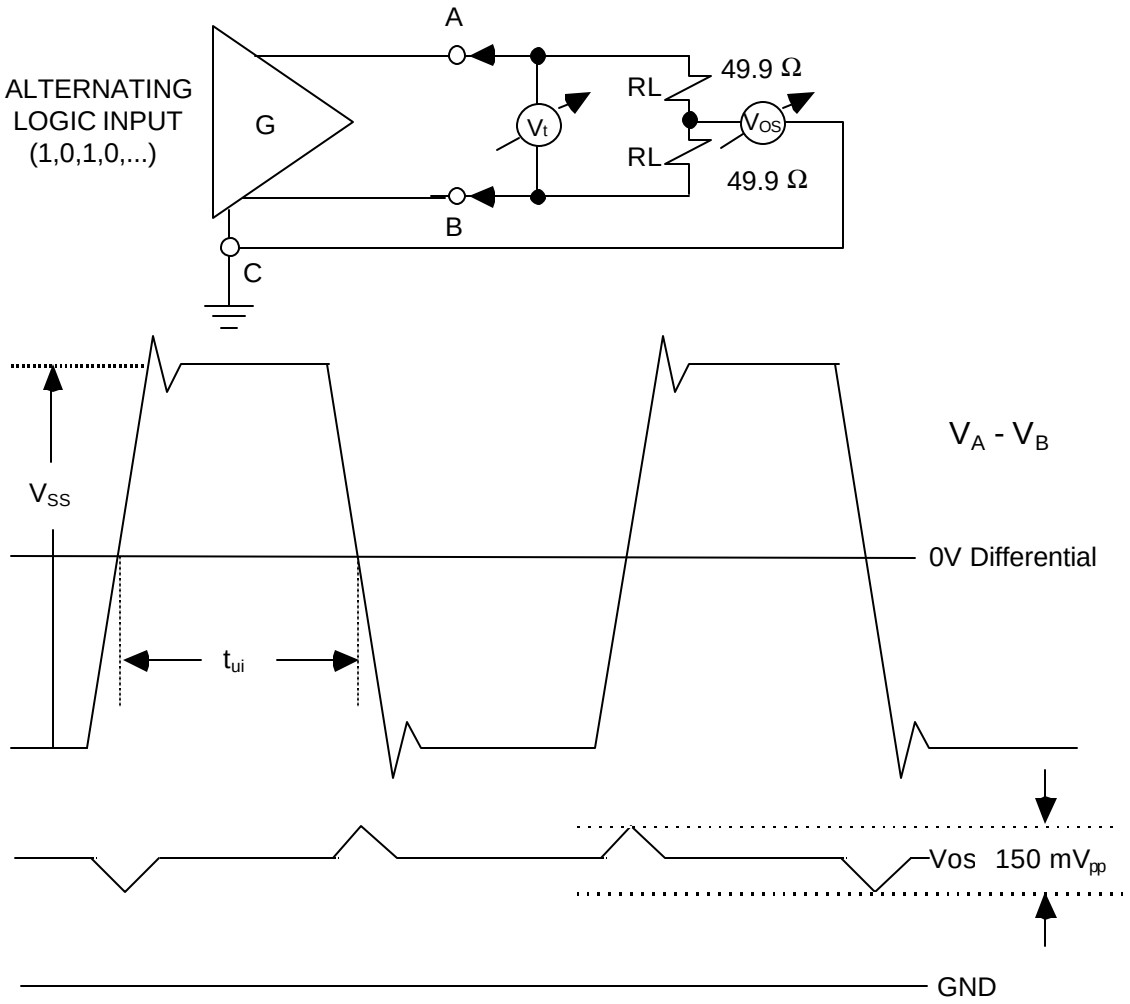


Figure 9 - Dynamic output signal balance waveform

4.2 Load characteristics

The load is defined as an impedance between A' and B' and is composed of a termination impedance and a receiver as shown in Figure 2.

The electrical characteristics of a receiver without an internal termination impedance are specified in terms of measurements illustrated in Figure 10, Figure 11, Figure 14 and Figure 15, and described in 4.2.1, 4.2.2 and 4.2.4. Alternately, the electrical characteristics of a receiver with an internal termination impedance is specified in terms of measurements illustrated in Figure 12 to Figure 15, and described in 4.2.3 through 4.2.4. A

circuit meeting these requirements results in a differential receiver having a high input impedance (non-terminating receiver), and a small input threshold between ± 100 mV.

The media termination is specified in terms of measurements described in 4.2.5 and 4.2.3 for receivers that integrate the termination impedance.

The total load limit is specified in 4.4.3, and additional guidance is provided in 4.4.1 and 4.4.2 on multiple receiver operation and failsafe operation respectively.

4.2.1 Receiver input current - voltage measurements

With the voltage V_{ia} (or V_{ib}) ranging from 0 V to +2.4 V while V_{ib} (or V_{ia}) is held at +1.2 V ± 50 mV, the resultant input current I_{ia} (or I_{ib}) shall be no greater than 20 µA in magnitude. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

NOTE - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

$$| I_{ia} | \leq 20\ \mu A$$

$$| I_{ib} | \leq 20\ \mu A$$

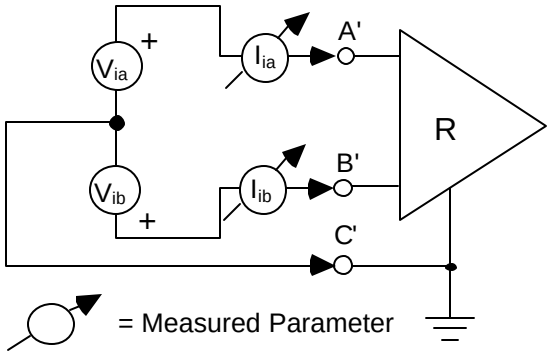


Figure 10 - Receiver input current - voltage measurements

4.2.2 Receiver input balance measurements

The balance of the input currents ($I_{A'}$ and $I_{B'}$) shall be 6 µA or less for all test voltages between 0 V and 2.4 V.

NOTE - Current into a terminal is positive, and current out of a terminal is negative.

$$| I_{A'} - I_{B'} | \leq 6\ uA$$

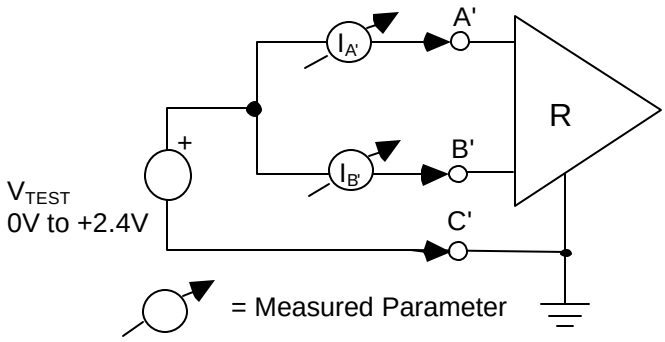


Figure 11 - Receiver input balance measurements

4.2.3 Terminating receiver input current - voltage measurements and input impedance measurements

With the applied voltage (V_{in}) and forced current (I_{in}) listed in Table 1 applied to the corresponding inputs, the resultant differential input voltage magnitude (V_{id}) shall be between the values listed in Table 1. The test circuit is shown in Figure 12 and applies only to receivers that provide an internal termination impedance. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

NOTE - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

$$225\ mV \leq |\ V_{id}\ | \leq 594\ mV$$

Table 1 - Receiver input current - voltage measurements for terminating receivers

Applied Voltage V_{in} (V)	Forced Loop Current I_{in} (mA)	Switch Position S1 - S2	Resulting Input Voltage V_r (V)	Resulting Diff. Input Voltage Range V_{id} (mV)
2.4	- 2.5	A' - B'	2.070 to 2.175	+225 to +330
2.4	- 4.5	A' - B'	1.806 to 1.995	+405 to +594
2.4	- 2.5	B' - A'	2.070 to 2.175	-225 to –330
2.4	- 4.5	B' - A'	1.806 to 1.995	-405 to -594
0	- 2.5	A' - B'	0.225 to 0.330	-225 to –330
0	- 4.5	A' - B'	0.405 to 0.594	-405 to -594
0	- 2.5	B' - A'	0.225 to 0.330	+225 to +330
0	- 4.5	B' - A'	0.405 to 0.594	+405 to +594

NOTE - Current into a terminal is positive, and current out of a terminal is negative.

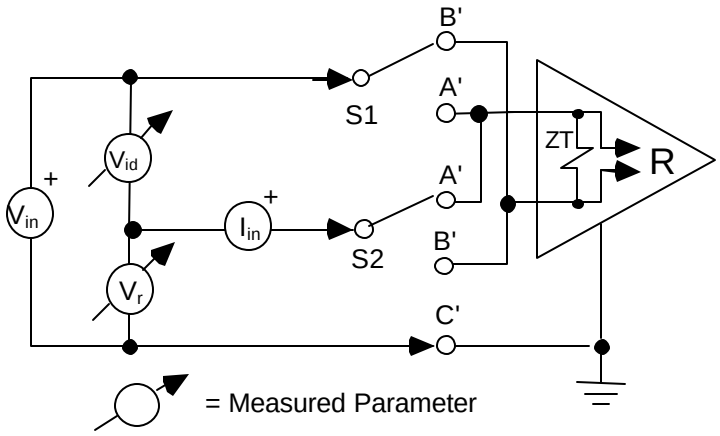


Figure 12 - Terminating receiver input current - voltage measurements

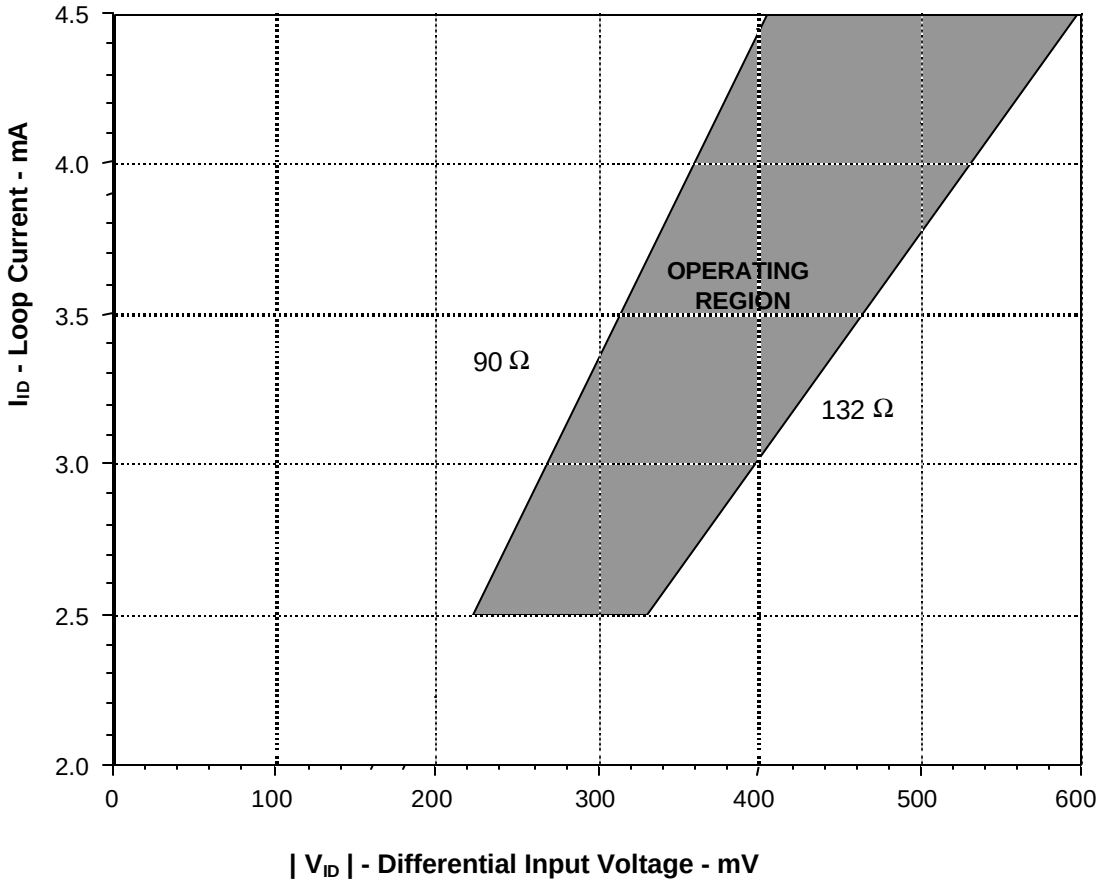


Figure 13 - Terminating receiver input current vs. input voltage range

The input impedance of the terminating receiver is dominated by the low impedance differential termination impedance (ZT). The resulting input resistance calculated from the

measurements describe in Table 1 shall be greater than or equal to 90 Ω, and less than or equal to 132 Ω. See 4.2.5 on media termination, and 4.4.3 on total load limit.

90 Ω ≤ **ZT** ≤ **132** Ω

NOTE - The internal termination impedance may be a simple resistor incorporated into the package, integrated on the die, or composed of active devices on the die. The exact structure and impedance of the termination is beyond the scope of this Standard.

4.2.4 Receiver input sensitivity measurements

Over an entire common-mode voltage range of +0.050 V to +2.350 V (referenced to receiver circuit common), the receiver shall not require a differential input voltage of more than ±100 mV (threshold) to correctly assume the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input voltages ranging between 100 mV and 600 mV in magnitude. The maximum voltage applied to either the A' or B' terminals should not be greater than +2.4 V, or be less than 0 V with respect to receiver circuit common. The maximum differential input voltage applied to the receiver is 2.4 V with no damage occurring to the receiver inputs.

$$100\ mV \leq |V_{ID}| \leq 600\ mV$$

$$0\ V \leq \text{Valid Input Voltage (to circuit common)} \leq +2.4\ V$$

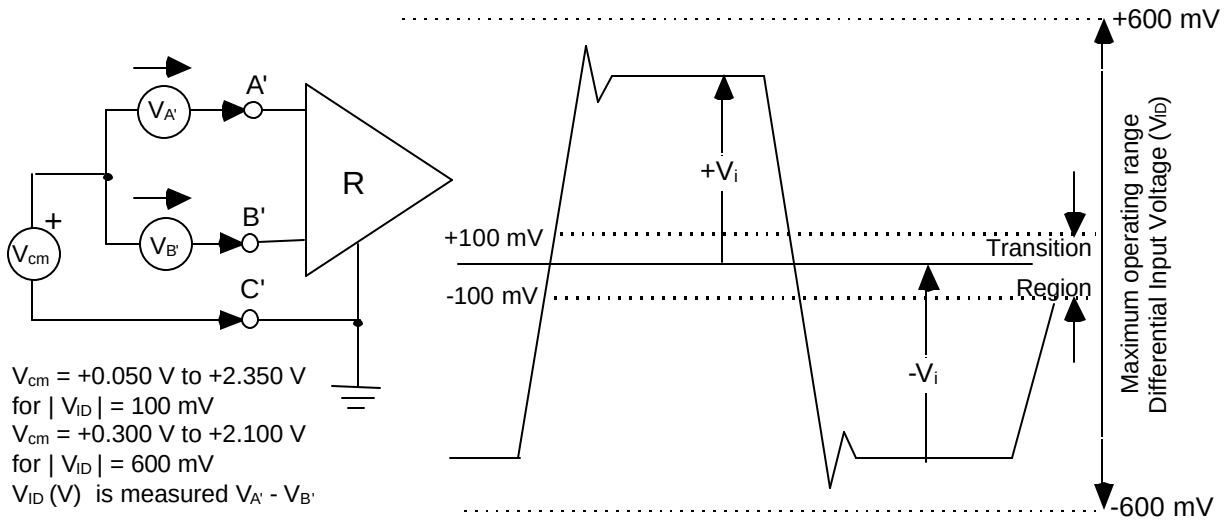


Figure 14 - Receiver input sensitivity measurements

Table 2 lists the minimum and maximum operating voltages of the receiver (input voltage, differential input voltage, and common-mode input voltage), and the test circuit is shown in Figure 15.

NOTE - The logic function of the receiver is not defined by this Standard.

Table 2 - Receiver minimum and maximum operating voltages

Applied Voltages (Input Voltage - referenced to circuit common - C')		Resulting Differential Input Voltage	Resulting Common-mode Input Voltage	Reason of Test
V_{ia}	V_{ib}	V_{ID}	V_{CM}	
+1.250 V	+1.150 V	+100 mV	+1.200 V	To guarantee operation with minimum V_{ID} applied versus V_{CM} range
+1.150 V	+1.250 V	-100 mV	+1.200 V	
+2.400 V	+2.300 V	+100 mV	+2.350 V	
+2.300 V	+2.400 V	-100 mV	+2.350 V	
+0.100 V	0 V	+100 mV	+0.050 V	
0 V	+0.100 V	-100 mV	+0.050 V	
+1.500 V	+0.900 V	+600 mV	+1.200 V	To guarantee operation with maximum V_{ID} applied versus V_{CM} range
+0.900 V	+1.500 V	-600 mV	+1.200 V	
+2.400 V	+1.800 V	+600 mV	+2.100 V	
+1.800 V	+2.400 V	-600 mV	+2.100 V	
+0.600 V	0 V	+600 mV	+0.300 V	
0 V	+0.600 V	-600 mV	+0.300 V	

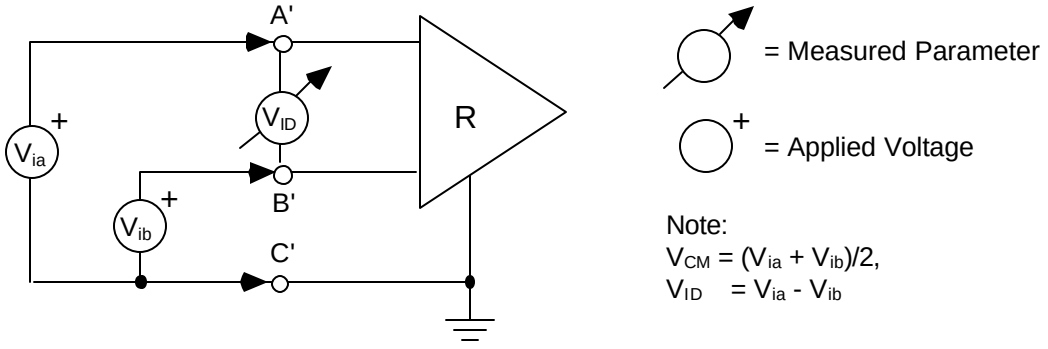


Figure 15 - Receiver input sensitivity test circuit

4.2.5 Media termination

All applications shall use a termination impedance. The recommended value is between 90 Ω and 132 Ω. The actual value should be selected to match the media characteristic

impedance (±10%) at the application frequency. The termination impedance may be integrated onto the receiver integrated circuit, but subject to meeting the requirements of * MERGEFORMAT 4.2.3 instead of 4.2.1. If the termination impedance is not integrated into the receiver circuit, then it shall be located at the load end of the balanced interconnecting media.

NOTE - Due to the high application frequency, care should be taken in choosing proper components such as the termination resistor, and in layout of the printed circuit board. The use of surface mount components is highly recommended to minimize parasitic inductance, and lead length of the termination resistor. Wire wound resistors are not recommended.

The media termination is shown in Figure 16 and Figure 17.

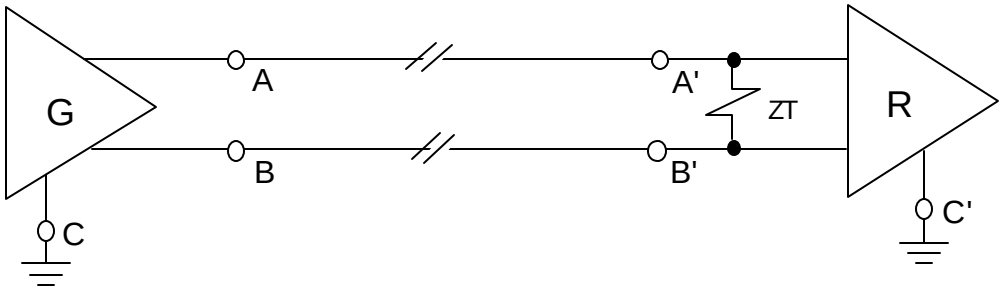


Figure 16 - Point-to-point application with external termination

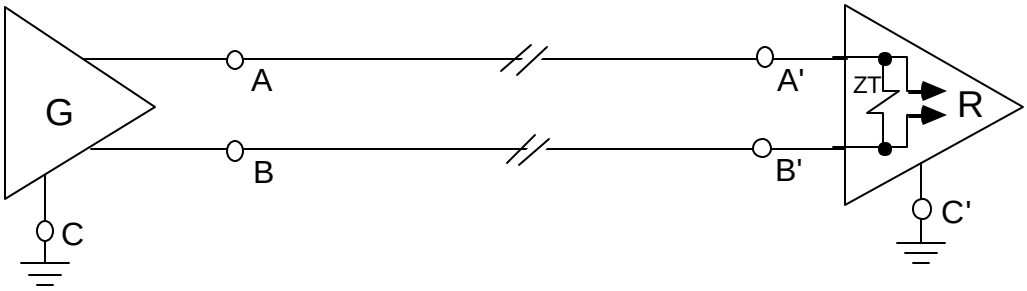


Figure 17 - Point-to-point application with internal termination

NOTE - Matching of impedance of the PCB traces, connectors and balanced interconnect media is highly recommended. Impedance variations along the entire interconnect path should be minimized since they degrade the signal path and may cause reflections of the signal.

4.3 Interconnecting media electrical characteristics

The balanced interconnecting media shall consist of paired metallic conductors in any configuration, which will maintain balanced signal transmission.

NOTE - The actual media of the cable is not specified and may be: twisted pair cable, twin-ax cable (parallel pair), flat ribbon cable, or PCB traces.

The performance of any balanced interconnecting media used shall be such to maintain the necessary signal quality for the specific application. If necessary for system consideration, shielding may be employed (see 7.2).

Annex A to this Standard provides guidance on performance and cable length versus data signaling rate and cable recommendations for typical cable applications.

4.3.1 Cable media

The cable media shall conform to the following electrical requirements:

4.3.1.1 Maximum dc loop resistance (DCR):

135 Ω is the maximum dc loop resistance of the cable. This corresponds to a voltage drop of 150 mV.

4.3.1.2 Characteristic impedance:

Nominal characteristic impedance shall be between 100 Ω and 120 Ω with variation of no more than 10% (90 Ω to 132 Ω) from 10 MHz to the application upper frequency limit.

4.3.1.3 Additional parameters

Additional parameters not specified which are application dependent (see Annex A) are: Maximum Attenuation, Maximum Propagation Delay, Maximum Propagation Delay Skew, Maximum Near-End Crosstalk (NEXT), and Maximum Far-End Crosstalk (FEXT). Crosstalk, skew, and related pair balance parameters may impact applications with multiple signal transmission lines.

4.3.2 PC Board trace media

The electrical requirements of PC Board traces shall also meet the requirements of 4.3.1.1 to 4.3.1.3.

4.3.3 Other media

It may be possible that other media may be employed, the definition and electrical characteristics of such media is beyond the scope of this Standard.

4.4 System parameters

4.4.1 Multiple receiver operation

The generator has the capability to furnish the dc signal necessary to drive multiple (up to 32) parallel connected receivers (without internal termination). However, the physical arrangement of the multiple receivers involves consideration of stub line lengths, location of the termination resistor, number of receivers, data signaling rate, circuit common, etc., that may degrade dynamic characteristics of the signal at the receivers if not properly implemented. It is recommended that stub lengths off the main line be as short as possible. In general, the propagation delay of the stub, should not exceed 30% of the signal transition time to prevent reflections and severe impedance discontinuities. For applications with receivers without internal termination, the external termination resistor must be located at the far end (last receiver) of the interconnect.

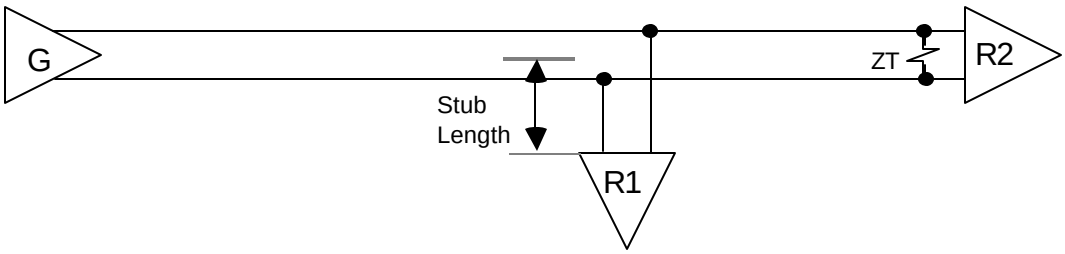


Figure 18 - Multiple receiver operation - multidrop application

NOTE - If the configuration illustrated in Figure 18 is employed, only the receiver at the far end of the cable may be a terminating receiver.

All receivers located between the generator and the final receiver must be non-terminating receiver(s). Multiple terminating receivers would present a low impedance load to the generator which would violate the total load limit (see 4.4.3), and adversely attenuate the signal.

The configuration shown in Figure 19 is composed of two independent uncomplicated point-to-point applications. At the expense of the second balanced interconnecting media, and termination impedance, the problem of stub lengths is eliminated, along with any impedance discontinuities that connectors and stubs may present. Signal quality is superior in an uncomplicated point-to-point configuration over a multidrop configuration. At the highest speeds it may not be possible to meet the 30% recommendation. In this case, a point-to-point configuration is recommended.

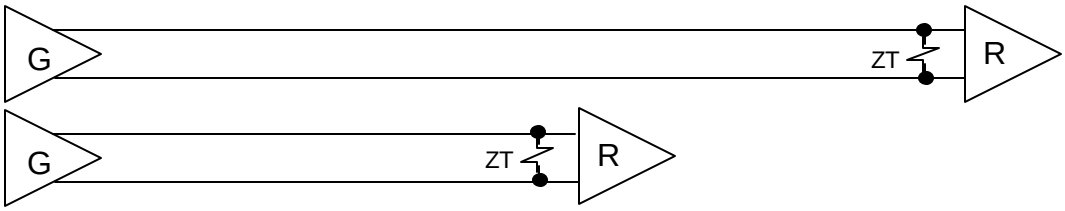


Figure 19 - Uncomplicated point-to-point application

4.4.2 Failsafe operation

Other standards and specifications using the electrical characteristics of the LVDS interface circuit may require that specific interchange circuits be made failsafe to certain fault conditions. Such fault conditions may include one or more of the following:

1) generator in power-off condition
2) receiver not connected with the generator
3) open-circuited interconnecting cable
4) short-circuited interconnecting cable
5) input signal to the load remaining within the transition region (±100 mV) for an abnormal period of time (application dependent)

When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required in the load and the following items must be determined and specified:

1) which interchange circuits require fault detection
2) what faults must be detected
3) what action must be taken when a fault is detected; the binary state that the receiver assumes
4) what is done does not violate this Standard

The method of detection of fault conditions is application dependent and is therefore not further specified as it is beyond the scope of this Standard.

4.4.3 Total load limit

The total load (ZL) including multiple receivers, failsafe provisions, and media termination shall have a total resistance greater than or equal to 90 Ω and less or equal to 132 Ω between its input points A' and B', shown in Figure 2. The receiver(s) shall not require a differential input voltage of more than 100 mV in magnitude for all receiver(s) to assume the intended binary state.

$$90\ \Omega \leq ZL \leq 132\ \Omega$$

5 ENVIRONMENTAL CONSTRAINTS

A LVDS interface circuit conforming to this Standard will perform satisfactorily providing that the following operational constraints are simultaneously satisfied:

a. For cable applications, the cable media meets the recommended cable characteristics, the cable length is within that recommended for the applicable data signaling rate indicated in Annex A, Section A.2 and the cable is properly terminated.

b. For PC Board traces, the traces meets the recommended characteristics for the applicable data signaling rate, and the trace is properly terminated.

c. The input voltage at the receiver (with respect to receiver circuit common) is between 0 V and +2.4 V and either input (A' or B') terminal. The input voltage is defined to be any uncompensated combination of generator-receiver common potential difference, the generator offset voltage (V_{OS}), and longitudinally coupled peak noise voltage.

d. Maximum common potential difference between the receiver circuit common and the generator circuit common is less than ±1 V.

6 CIRCUIT PROTECTION

The LVDS interface generator and receiver devices, under either the power-on or power-off condition, complying to this Standard shall not be damaged under the following conditions:

a. Generator open circuit.
b. Short-circuit across the balanced interconnecting media.
c. Short-circuit to common.

NOTE - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

7 OPTIONAL GROUNDING ARRANGEMENTS

7.1 Signal common (ground)

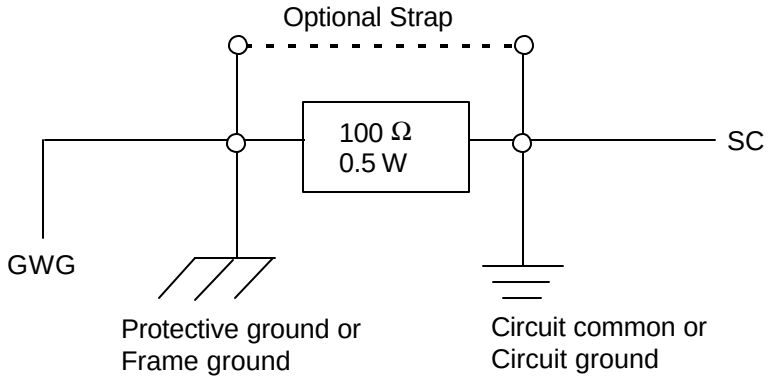
Proper operation of the LVDS interface circuits requires the presence of a signal common path between the circuit commons of the equipment at each end of the interconnection. The signal common interchange lead shall be connected to the circuit common which shall be connected to protective ground by any one of the following methods, shown in Figure 20 and Figure 21, as required by specific application.

The same configuration need not be used at both ends of an interconnection; however, care should be exercised to prevent establishment of ground loops carrying high currents.

7.1.1 Configuration "A"

The circuit common of the equipment is connected to protective ground, at one point only, by a 100 Ω, ±20%, resistor with a power dissipation rating of 0.5 W. An additional provision may be made for the resistor to be bypassed with a strap to connect circuit common and protective ground directly together when specific installation conditions necessitate.

> NOTE - Under certain ground fault conditions in configuration "A", high ground currents may cause the resistor to fail; therefore, a provision shall be made for inspection and replacement of the resistor.

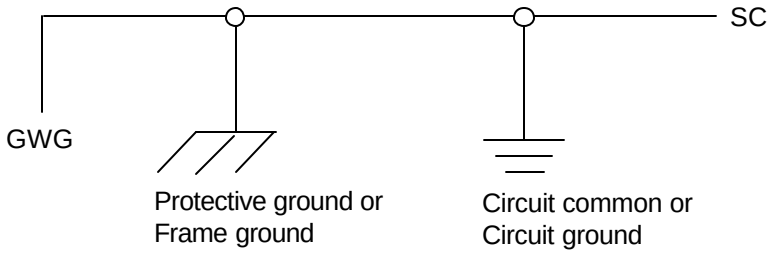


Legend:
GWG = Green wire ground of power system
SC = Signal common interchange circuit

Figure 20 - Optional grounding arrangements - configuration "A"

7.1.2 Configuration "B"

The circuit common shall be connected directly to protective ground.



Legend:
GWG = Green wire ground of power system
SC = Signal common interchange circuit

Figure 21 - Optional grounding arrangements - configuration "B"

7.2 Shield ground - cable applications

Some interface applications may require the use of shielded balanced interconnecting media for EMI or other purposes. When employed, the shield shall be connected only to frame ground at either or both ends depending on the specific application. The means of connection of the shield and any associated connector are beyond the scope of this Standard.

ANNEX A (informative) - Guidelines for Cable Application

(This annex is not a formal part of the attached TIA/EIA Recommended Standard, but is included for information purposes only.)

A.1 Interconnecting cable

The following section provides further information to Section 4.3 and is additional guidance concerning operational constraints imposed by the cable media parameters of length and termination.

Generally, if more than one signal transmission line is required for an interface, twisted pairs are necessary to balance coupling reactance between individual conductors of adjacent pairs and thus reduce crosstalk.

A.1.1 Length

The length of the cable separating the generator and the load is based on a maximum loop resistance of 135 Ω, and a corresponding 150 mV loss of the signal.

The following examples given take only the dc effects into account in determining the maximum cable length. This would pertain to low speed operation only. The ac effects will limit the maximum cable length before the dc resistance for high speed applications. See section A.2.

For the following cables gauges, the corresponding maximum length for a 50 mV signal loss is:

28 AWG 50 meters (164 feet),

24 AWG 150 meters (492 feet)

Longer lengths are possible, if the voltage attenuation is allowed to decrease the minimum generator differential output voltage to the maximum receiver threshold voltage (250 mV to 100 mV) for a 150 mV voltage attenuation or -7.9 db. For the following cables gauges, the corresponding maximum length at a 150 mV signal loss is:

28 AWG 150 meters (492 feet),

24 AWG 450 meters (1,476 feet)

A.1.2 Typical cable characteristics

A.1.2.1 Parallel interface cable

The following characteristics apply to common parallel interface cable (as used for TIA/EIA-613, and other I/O interface standards) consisting of 25 twisted pairs surrounded by an overall shield:

A.1.2.1.1 Parallel cable, physical characteristics

Conductor	28 AWG, 7 strands of 36 AWG, tinned annealed copper, nominal diameter 0.38 mm (0.015 inch)
Insulation	Polyethylene or polypropylene; 0.24 mm (0.0095 inch) nominal wall thickness; 0.86 mm (0.034 inch) outside diameter
Foil Shield	0.051 mm (0.002 inch) nominal thickness aluminum / polyester laminated tape helically wrapped around the core
Braid Shield	braided 36 AWG, tinned copper with 80% minimum coverage, in electrical contact with the aluminum surface of the foil shield
Diameter	nominal overall cable diameter 9.5 mm (0.375 inch)

A.1.2.1.2 Parallel cable, electrical characteristics

dc Resistance	221 Ω / km (67.5 Ω/1000 feet)
Mutual Capacitance	43 pF/m (13 pF/ft) at 1 kHz
Impedance	(characteristic, differential-mode) 110 Ω nominal at 50 MHz
Propagation Delay	4.8 ns/m (1.46 ns/ft)
Attenuation	0.28 dB/m (0.085 dB/ft) at 50 MHz
Skew	(propagation delay) 0.115 ns/m (0.035 ns/ft)
Maximum Crosstalk (Near-End, NEXT)	30 dB at 50 MHz

A.1.2.2 Serial interface cable

The following characteristics apply to a common Category 5 serial interface cable (as used for TIA/EIA-422, and other I/O interface standards) consisting of 4 unshielded twisted pairs surrounded by an overall jacket:

A.1.2.2.1 Serial cable, physical characteristics

Conductor	24 AWG, 7 strands of 32 AWG, tinned annealed copper, nominal diameter 0.61 mm (0.024 inch)
Insulation	Polyethylene or polypropylene; 0.18 mm (0.007 inch) nominal wall thickness; 0.97 mm (0.038 inch) outside diameter
Foil Shield	optional
Braid Shield	optional
Diameter	nominal overall cable diameter 5.6 mm (0.22 inch)

A.1.2.2.2 Serial cable, electrical characteristics

dc Resistance	84.2 Ω / km (25.7 Ω/1000 feet)
Mutual Capacitance	48 pF/m (14.5 pF/ft) at 1 kHz
Impedance	(characteristic, differential-mode) 100 Ω nominal at 50 MHz
Propagation Delay	4.8 ns/m (1.46 ns/ft)
Attenuation	0.17 dB/m (0.051 dB/ft) at 50 MHz
Maximum Crosstalk (Near-End, NEXT)	36.8 dB at 50 MHz

A.1.3 Cable termination

The characteristic impedance of twisted pair cable is a function of frequency, wire size and type as well as the kind of insulating materials employed. For example, the characteristic impedance of average 28 AWG, copper conductor, plastic insulated twisted pair cable, to a 50 MHz sine wave will be on the order of 110 Ω.

The range of 90 Ω to 132 Ω allows for a range of media characteristic impedance to be specified. The nominal media characteristic impedance is restricted to the range of 100 Ω to 120 Ω to allow for impedance variations within the media. Depending upon the balanced interconnecting media specified, the termination impedance should be within 10% of the nominal media characteristic impedance.

A.2 Cable length vs. data signaling rate guidelines

The maximum permissible length of cable separating the generator and the load is a function of data signaling rate and is influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and common potential differences introduced between the generator and the load circuit commons as well as by cable balance. Increasing the physical separation and the interconnecting cable length between the generator and the load interface points increases exposure to common-mode noise, signal distortion, and the effects of cable imbalance. Accordingly, users are advised to restrict cable length to a minimum, consistent with the generator to load physical separation requirements.

To determine the maximum data signaling rate for a particular cable length, the following calculations / testing is recommended. First, the maximum DCR of the cable length (loop resistance) should be calculated, then the resulting signal attenuation should be calculated at the load. The voltage at the load must be greater than the receiver thresholds of 100 mV. For a conservative design, a maximum attenuation of 50 mV is recommended. Next eye patterns are recommended to determine the amount of jitter at the load at the application data signaling rate and comparing that to system requirements. Typically maximum allowable jitters tolerances range from 5% to 20% depending upon actual system requirements. This testing should be done in the actual application if possible, or in a test system that models the actual application as close as possible. Parameters that should be taken in account include: balanced interconnect media characteristics, termination, protocol and coding scheme, and worst case data patterns (pseudo random for example). The generator / receiver manufacturers and also the media manufacturers should provide additional guidance in predicting data signaling rate versus cable length curves for a particular generator / receiver and a particular media as this relationship is very dependent upon the actual characteristics of the selected devices and media.

When generators are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, shall be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply).

ANNEX B (informative) - Compatibility and Related Standards

(This annex is not a formal part of the attached TIA/EIA Recommended Standard, but is included for information purposes only.)

B.1 Compatibility with other interface standards

The LVDS interface circuit is not intended for direct inter-operation with other interface electrical characteristics such as TIA/EIA-422, TIA/EIA-485, TIA/EIA-612, ITU-T Recommendation V.11, emitter coupled logic (ECL) or PECL.

Under certain conditions, inter-operation with circuits of some of the above interfaces may be possible but may require modification in the interface or within the equipment, or may require limitations on certain parameters (such as common-mode range); therefore, satisfactory operation is not assured, and additional provisions not specified herein may be required.

B.1.1 Compatibility with IEEE 1596.3

This Standard features very similar dc electrical specifications to the IEEE 1596.3 standard titled: SCI-LVDS Low Voltage Differential Signals Specifications and Packet Encoding. Direct inter-operation should be possible at certain data signaling rates without the use of intermediate circuitry. This Standard specifies generic electrical characteristics of low voltage differential signaling interface circuits for general purpose applications.

B.1.2 Inter-operation with other interface standards

To determine if direct inter-operation is possible with other interface standards, generator output levels, and receiver input specifications must be compared. Specifically the generator's differential output voltage, and offset voltage must be within the bounds of the receiver's input ranges. Correspondingly, the receiver's input thresholds, and input voltage range must be able to accept the generator's output levels. If this is the case, direct inter-operation is possible. If differences exist, additional provisions and / or precautions may be required. This may include modification or additional circuitry inserted at the interface points or imposing limitations on certain parameters such as maximum common potential difference. The exact circuitry required is beyond the scope of this annex.

B.2 Related TIA/EIA standards

TIA/EIA-422-B *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*

TIA/EIA-485-A *Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems*

TIA/EIA-612 *Electrical Characteristics for an Interface at Data Signaling Rates up to 52 Mbit/s*

B.3 Other related interface standards

IEEE-1596.3 *SCI-LVDS Low Voltage Differential Signals Specifications and Packet Encoding*

ITU-T Recommendation V.11 *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications*