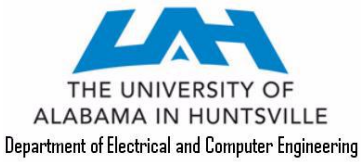


CPE 324 Advanced Logic Design Laboratory
Laboratory #1

(8% of Final Grade)

Part 1: Practical Characteristics of Small Scale Combinational and Sequential Circuits

Purpose

In this laboratory you will prototype simple digital hardware designs and elements using traditional solderless breadboarding techniques. You will then verify that these designs are implemented correctly by using the Terasic DE2-115 FPGA board that has been preconfigured to act as a digital logic trainer. This board will provide the inputs to your design using slide and pushbutton switches that are present on the DE2-115 board and you will monitor your design outputs using various LEDs that are present on the DE2-115 board. The first design is a simple combinational logic design that is to be implemented using two Small Scale Integration (SSI) type integrated circuits. The second and third designs require you to use the DE2-115 to control and observe the operation of two different sequential designs. These designs have already been implemented in separate Medium Scale Integration (MSI) type ICs.

In subsequent laboratories the knowledge gained will aid you in intefacing various external sensor and actuator elements to the DE2-115 that will be driven by your digital logic that is present on the DE2-115 FPGA board. develop Even though these prototyping methods are only used to prototype small relatively slow speed digital designs, a basic unders is here that basic concepts are illustrated that should highlight common design issues that designers have faced in the past many of which are still applicable to modern digital design and prototyping paradigms.

Goals of this Laboratory

- Understand how to interface external digital components to the DE2-115 FPGA board using a solderless breadboard and the UAH ECE Breakout board that is connected to 40 pin general input/output port of the DE2-115
- Understand the need for a common ground and how to connect VCC and the common ground to external components on the solderless breadboard.
- Understand how to wire component elements together using the solderless breadboard
- Understand the basic differences between asynchronous control signals and synchronous control signals

DE2-115 Based Prototyping Environment

The Terasic DE2-115 prototype board is an educational/rapid prototyping board that can be used to implement arbitrary digital designs. These designs are placed within the Intel FPGA Cyclone IV E FPGA that is one of the components on the board. The DE2-115 contains basic switches and LED's as well as many other much more complex devices such as an LCD, a RS232 compatible serial interface, an SD card interface, an infrared LED transmitter/receiver pair, USB, Ethernet, VGA interface and a two way audio interface. The configuration that is being utilized for the first part of this course is that of a basic digital logic trainer. In this mode the DE2-115 can be connected to a solderless protoboard where it can be used to drive the inputs and monitor the outputs of externally constructed digital designs. In subsequent laboratories, you will override this default FPGA configuration to prototype their own digital designs.

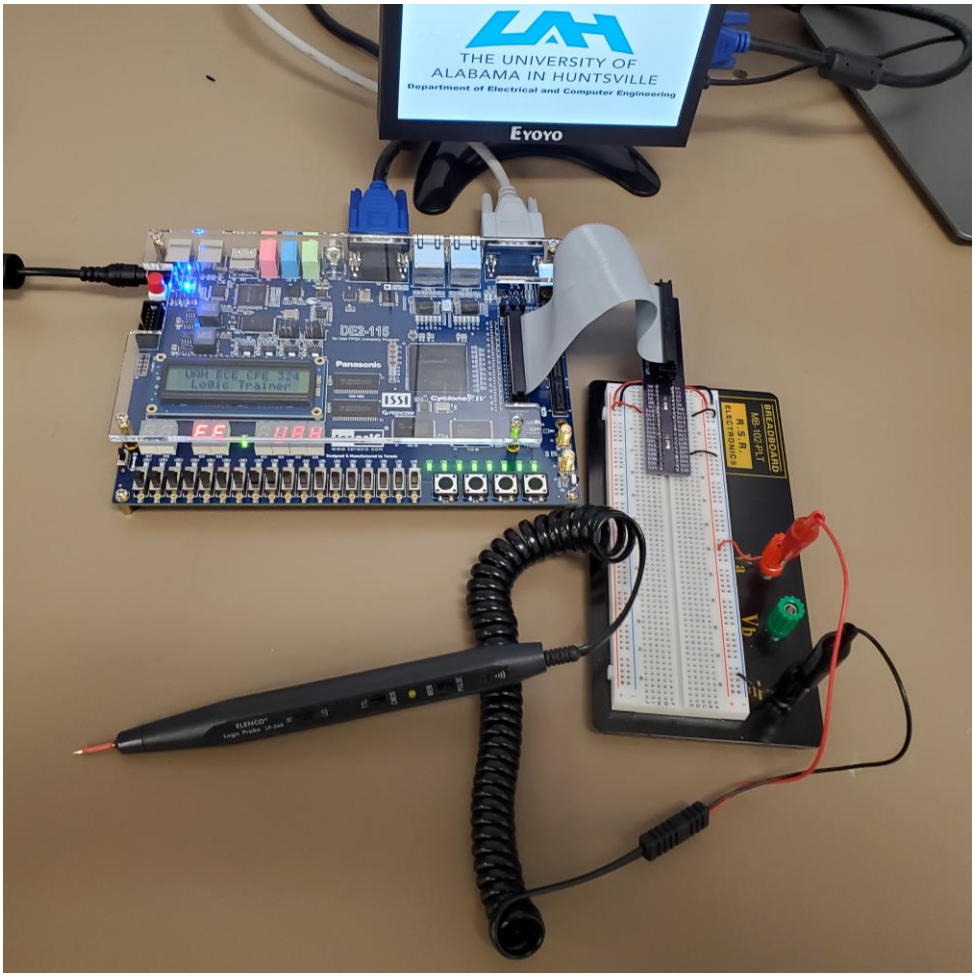
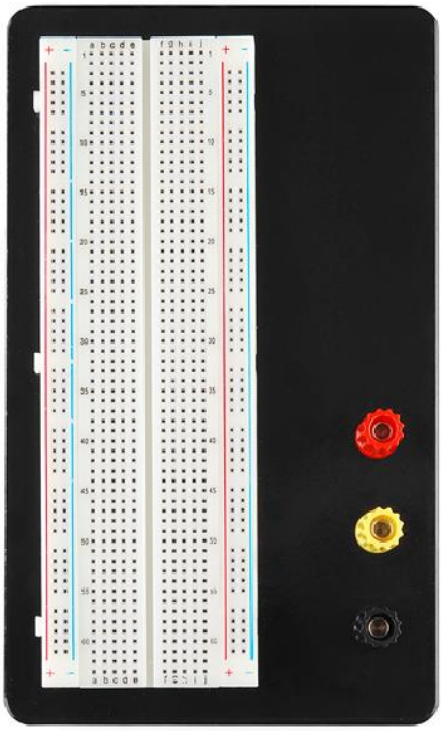


Figure 1: DE2-115 board connected to a solderless bread board through the UAH ECE Breakout Board

In both parts of this first laboratory the Terasic DE2-115 board will be configured to act as a simple digital logic trainer which will drive and monitor the inputs and outputs of a logic circuit that you will implement on an external solderless breadboard which is similar to the one shown in Figure 2.

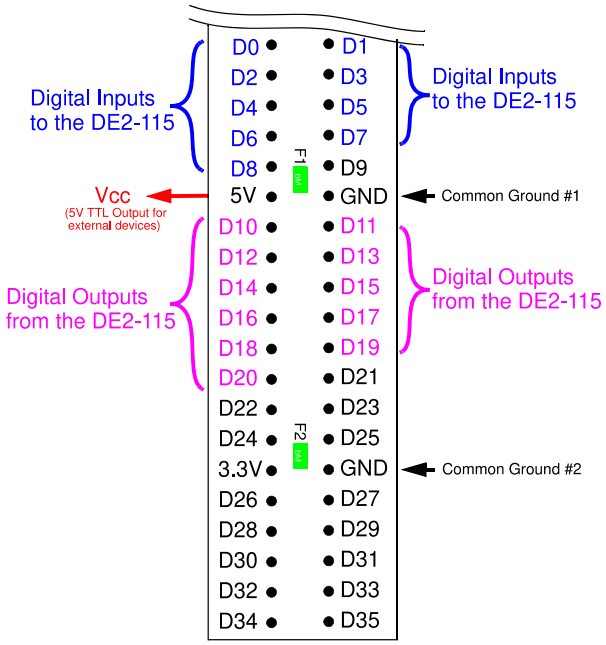


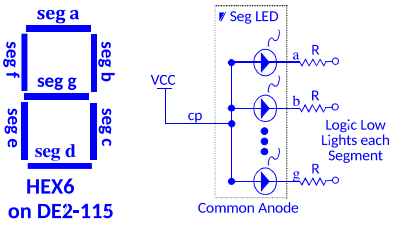
Top View

Bottom View Showing the Conduction Path Pattern

This board allows SSI and MSI integrated circuits, that are housed in Dual-In-Line packages (DIPs) to be electronically connected to the DE2-115 board, and to other IC's in a non-permanent manner. Wiring is done by inserting wires into the appropriate holes in the board. The connection conduction path pattern for the solderless breadboard is shown on the right side of Figure 2. The left side of Figure 2 shows the breadboard from the user's perspective. The five holes that form a row on either side of the center of the board represent separate conduction zones that are insulated from each other. The spacing of the rows along the center line allows the DIP IC's to straddle the center and have four holes which can be used to connect wires to each pin of the IC. The two columns on either side of the board also form four separate conduction zones. These zones are often used as a common point for power and ground which is required for each IC.

The DE2-115 is set to power up in the default logic trainer configuration mode. In this mode the it will provide the controlling input signals and can be used to probe the output signals of the digital circuitry which is implemented on the solderless breadboard. External signals are interfaced through the UAH ECE breakout board which is connected to the DE2-115 FPGA board through the 40 pin I/O port. The following diagrams illustrate the logical connections between the DE2-115 switches and LEDs and the pin numbers that are brought out to the solderless breadboard through the UAH ECE Breakout board.

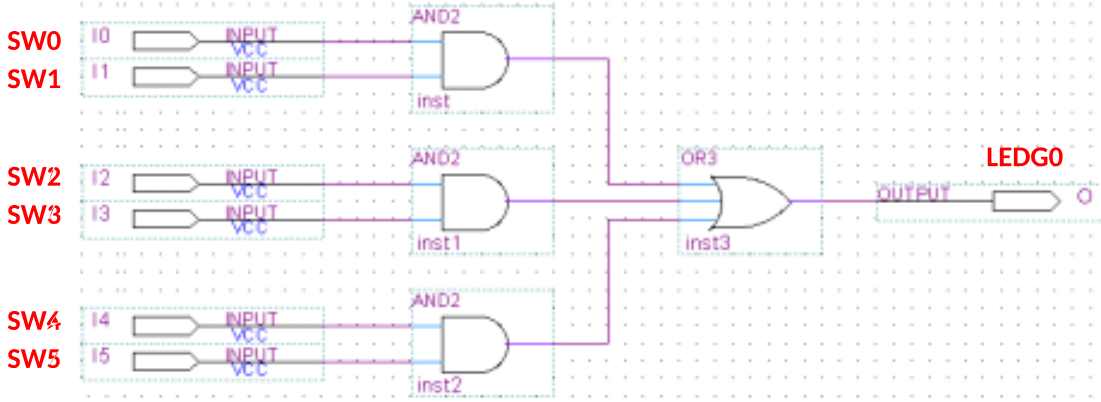


DE2-115 Logic Trainer Mode Inputs to DE2-115 from UAH ECE Breakout Board		
UAH ECE Breakout Board Pin Number	DE2-115 LED(s) 	
D0	LEDG0 & HEX6 (seg a)*	HEX4 (hexadecimal representation of inputs D3-D0)
D1	LEDG1 & HEX6 (seg b)*	
D2	LEDG2 & HEX6 (seg c)*	
D3	LEDG3 & HEX6 (seg d)*	
D4	LEDG4 & HEX6 (seg e)*	HEX5 (hexadecimal representation of inputs D7-D4)
D5	LEDG5 & HEX6 (seg f)*	
D6	LEDG6 & HEX6 (seg g)*	
D7	LEDG7	
D8	LEDG8	
*Note: HEX6 LED segments on the DE2-115 use active low logic meaning a logic 0 is required to illuminate each segment.		

DE2-115 Logic Trainer Mode Outputs from DE2-115 to UAH Breakout Board				
DE2-115 Switch	UAH ECE Breakout Board Pin Number	DE2-115 Switch/ Button	DE2-115 Key Button Inversion Switches	UAH ECE Breakout Board Pin Number
SW0	**D10**	**SW7/KEY0**	**SW11**	**D17**
SW1	**D11**	**SW8/KEY1**	**SW12**	**D18**
SW2	**D12**	**SW9/KEY2**	**SW13**	**D19**
SW3	**D13**	**SW10/KEY3**	**SW14**	**D20**
SW4	**D14**			
SW5	**D15**			
SW6	**D16**			

Assignment #1: Multi-IC Combinational Logic Design

You are to implement the following logic network on the solderless breadboard that is connected to the Terasic DE2-115 Trainer using a 74LS08 (quad 2-input AND gate) IC and a 74LS32 (quad 2-input OR gate) IC.



Connect the DE2-115 to the logic network on the breadboard so that it drives the design inputs I0-I5 using switches SW0-SW5 and have the output drive the DE2-115s discrete LED that is labeled LEDG0. Note that this assignment required that you use two ICs that contained only two-input gates and that one of the gates, the OR gate, in the design is a three-input gate. This requires that you restructure the actual logical implementation on the breadboard so that it is functionally equivalent to the original logic. This means in effect that you need to construct a logically equivalent three-input OR gate using two or more of the 2-Input OR gates that are part of the 74LS32 IC.

Table 1: Partial Truth Table used to test your design

Inputs (Test vectors)						Output, O	
I0	**I1**	**I2**	**I3**	**I4**	**I5**	**Expect**	**Actual**
0	1	0	0	0	0		
1	1	0	0	0	0		
0	0	0	1	0	0		
0	0	1	1	0	0		
0	0	0	0	0	0		
0	0	0	0	1	1		
1	0	1	0	1	0		
0	1	0	1	0	1		

Before you test out your circuit determine its expected behavior by evaluating the network diagram shown in Figure 6 to complete the Expected (output) column of the truth table. Then record the actual value that was produced by your circuit. Assume that a logic 1 will light up the LED. When your expected value and actual truth table columns agree with one another then demonstrate your design to your lab instructor. Include this completed table in your report along with a logic diagram that shows how you actually created this network using the actual implementation using a 74LS08 and 74LS32 IC**. In your laboratory report, comment on how different switch combinations would be needed to test all possible cases for this design. Also in your report comment on any problems and issues you may have had getting this implementation to work and discuss how you were able to overcome them to complete your design.**

DM74LS08
Quad 2-Input AND Gates

FAIRCHILD SEMICONDUCTOR™

General Description

This device contains four independent gates each of which performs the logic AND function.

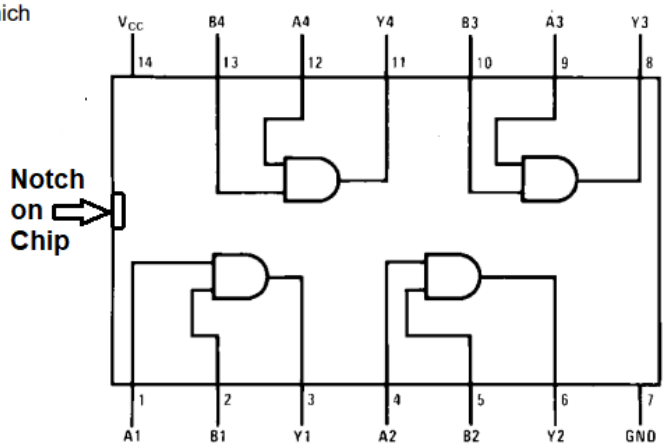
Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Connection Diagram



DM74LS32
Quad 2-Input OR Gate

FAIRCHILD SEMICONDUCTOR™

General Description

This device contains four independent gates each of which performs the logic OR function.

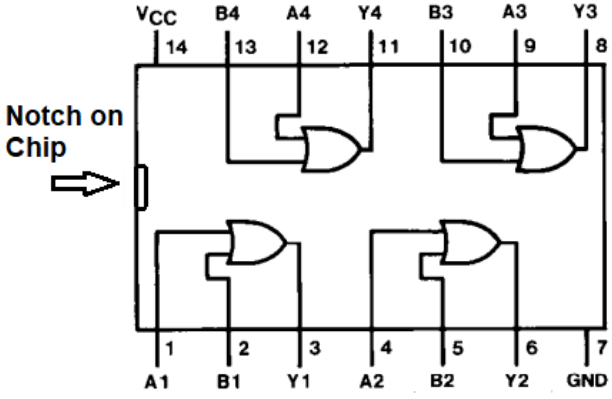
Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Connection Diagram



Assignment #2: Multi-IC Sequential Logic Design

In this assignment you are to cascade two simple 4-bit binary counter ICs to create an 8-bit binary counter which you will observe its associated outputs using the Terasic DE2-115 logic trainer. The two devices are pin compatible with one another but differ from one another by the fact that one counter is a synchronous clear counter and the other is an asynchronous one. Read carefully the following manufacture's partial data sheet on this family of 4-bit counters.

Partial Data Sheet

DM54161/DM74LS161/DM74LS163

Synchronous 4-Bit Counters

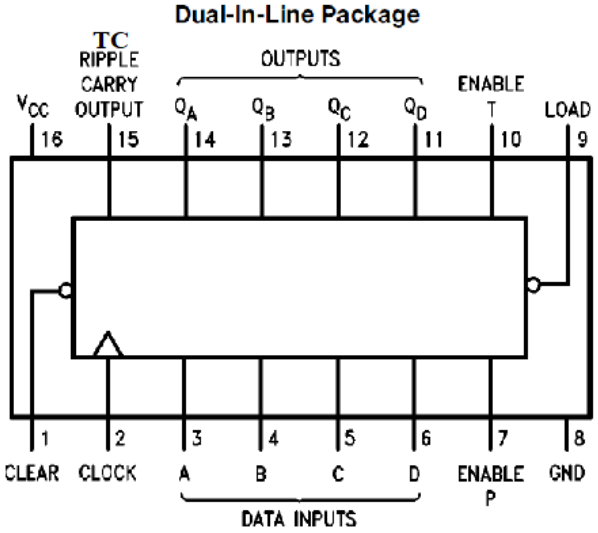
General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 161 and 163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flipflops clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the 161 is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the 163 is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 163 are also permissible, regardless of the logic levels on the clock, enable, or load inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both countenable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the QA output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High to-low-level transitions at the enable P or T inputs of the 161 through 163 may occur, regardless of the logic level on the clock.

National Semiconductor

Connection Diagram

Dual-In-Line Package

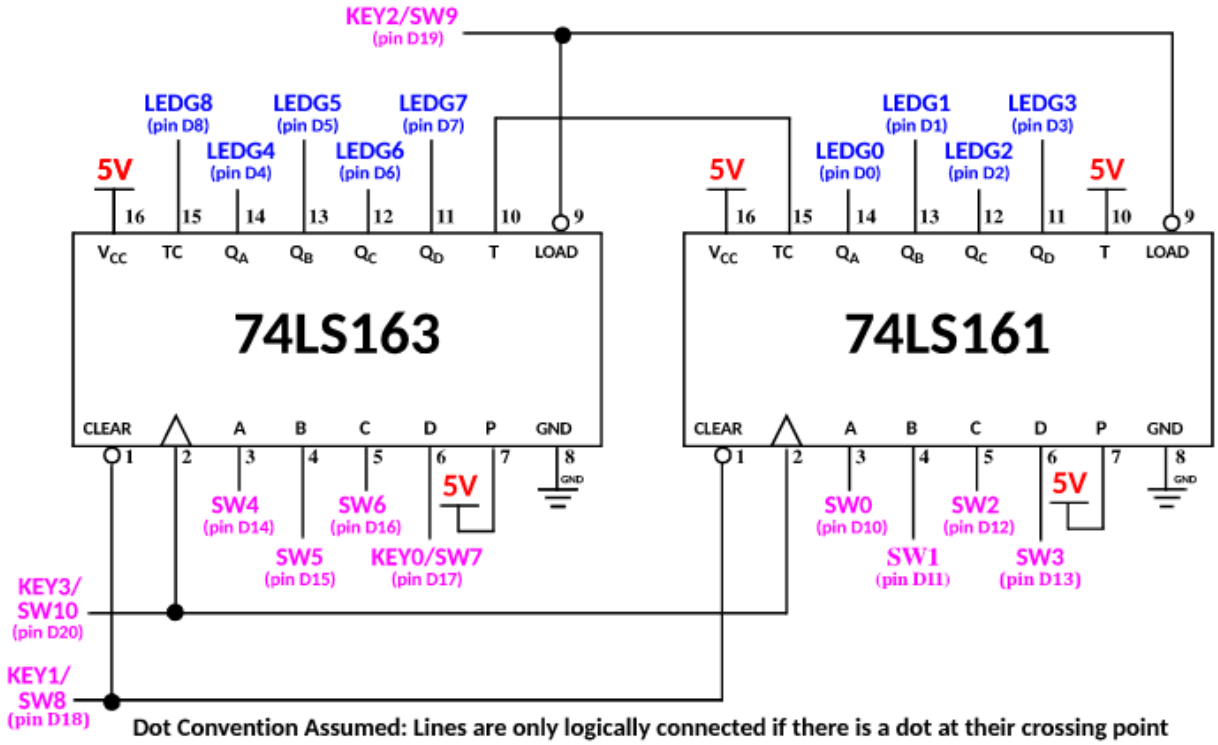


Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- 74LS161 Asynchronous Clear
- 74LS163 Synchronous Clear

Specific Wiring Instructions:

Create an 8-bit binary counter using a single 74LS161 and a 74LS163 IC. The LOAD, CLEAR, and clock inputs of the two ICs should be connected together and driven by the DE2-115 and the 74LS161 should provide the least significant 4 bits and the 74LS163 IC should provide the most significant 4 bits. The complete connection diagram is shown below:



The CLEAR and LOAD inputs to the counter are active low which is indicated by the circle their inputs in the diagram. This means that the desired action occurs when a Logic 0 is applied to the input and the action does not occur when a Logic 1 is applied to the input. So for the CLEAR input this would mean that the CLEAR operation (which sets all the output bits to 0) occurs when the CLEAR input is at a Logic 0 and the counter is not cleared (performs normal counting operation) when CLEAR is set to a Logic 1. The load operation works in the same manner. If LOAD is at a LOGIC 0 the counter outputs are loaded from the A,B,C, and D, inputs erasing the previous outputs. When the LOAD input is a Logic 1 then the load operation is not performed.

Automatic Clocking Control on the DE2-115 Board for Pin D20

SW17			
down	manual clock using KEY3		
up	automatic clock, speed set by SW16 and SW15		
	SW16	SW15	UAH Breakout Board Pin D20
	down	**down**	**very slow 50% duty cycle clock**
	down	**up**	**slow 50% duty cycle clock**
	up	**down**	**medium 50% duty cycle clock**
	up	**up**	**fast 50% duty cycle clock**

Design Verification

Complete the following steps to partially verify the functionality of the 8 bit counter. Begin by setting the LOAD and CLEAR inputs to an inactive.

Then demonstrate the following to your lab instructor:

- Load an initial count value of 00001110 into the counter. Discuss how this was done and when it took effect. Return the LOAD signal to its inactive state.
- With the count value of the counter set initialized to 00001110, generate a manual clock by pressing the KEY3 button for each clock cycle. Record what happens to the count value and the ripple counter (also called the Terminal Count, TC) output as you clock your design for three clock cycles.
- Temporarily rewiring the input P on Pin 7 of the 74LS161 IC so that it is connected to ground instead of 5V. What happens when you manually advance the clock signal five clock cycles? Return the connection of input P on Pin 7 of the 74LS161 so it is at 5V. What happens when you manually advance the clock signal five clock cycles?
- Using an automatically generated but slow speed clock from the DE2-115 demonstrate a forward count starting from 00001100 to at least 00011111. (Note counter will continue past this point if left running – that is okay.)

- Run the clock with IC in automatically generated clocking mode with clock set to a high speed (SW17, SW16, SW15 all in the up position). What happens to the output?

- Return the clocking mode to manual. Initialize the count value to 11111111. Activate CLEAR input without advancing the clock. What happens to the output? Now with the CLEAR input still activated advance the clock one cycle. What happens then to the output? Explain your results. How would you

- What happens if you use the SW10 key to manually clock your design instead of KEY3? Explain why the design behaved in the manner you observed.