CPE 324-03: Advanced Digital Logic Design Laboratory

Lab 3

Electrical and Timing Characteristics of Digital Hardware

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1 Introduction

This laboratory focuses on building familiarity with the measurement tools used in the Advanced Logic Digital Design Laboratory. By applying these tools in a practical setting, students gain insight into the electrical behaviors and constraints that influence digital circuit performance. The instruments used for this experiment were a multimeter and an oscilloscope.

2 Experiment Description

2.1 Theory

2.1.1 Multimeter

A multimeter is a versatile electrical measurement instrument used to measure fundamental circuit quantities such as voltage, current, and resistance. It is commonly used in both troubleshooting and circuit verification, providing essential information about the electrical behavior of components and systems. In digital logic applications, multimeters are frequently used to verify power supply levels, check logic high and logic low voltages, and test continuity in wiring and connections. These measurements help confirm that circuits are properly powered and electrically connected before more detailed signal analysis is performed with instruments such as oscilloscopes.

2.1.2 Oscilloscope

An oscilloscope is an electronic measurement instrument used to visualize time-varying electrical signals. It graphically displays voltage as a function of time, allowing users to observe waveform shape, amplitude, frequency, and timing characteristics. This makes the oscilloscope an essential tool for analyzing and troubleshooting digital and analog circuits. In digital logic applications, oscilloscopes are commonly used to verify logic levels, measure timing relationships, detect noise, and observe transient behavior. These measurements help ensure that circuits operate within required voltage thresholds and timing constraints, which are critical for reliable digital system performance.

2.2 Experiment 1 - Basic Voltage measurements from the DE2-115

To evaluate the electrical characteristics of the DE2-115 (laboratory FPGA) board, basic measurements of the supply voltages were obtained. The voltage levels at the 5V Vcc pin and the 3.3V pin were measured using a digital multimeter.

2.3 Experiment 2 - DE2-115/TTL Device Output Voltage Measurements

Once the baseline logic-high voltage levels were established in Experiment 1, those reference values were used to evaluate the output behavior of logic gates. A DM74LS04 hex inverter IC was connected to the laboratory FPGA board, and voltage measurements were taken at two

points in the circuit: the inverter input and the inverter output. The partial datasheet for the inverter IC and wiring configurations used for these measurements are shown in Figures 1 and 2.

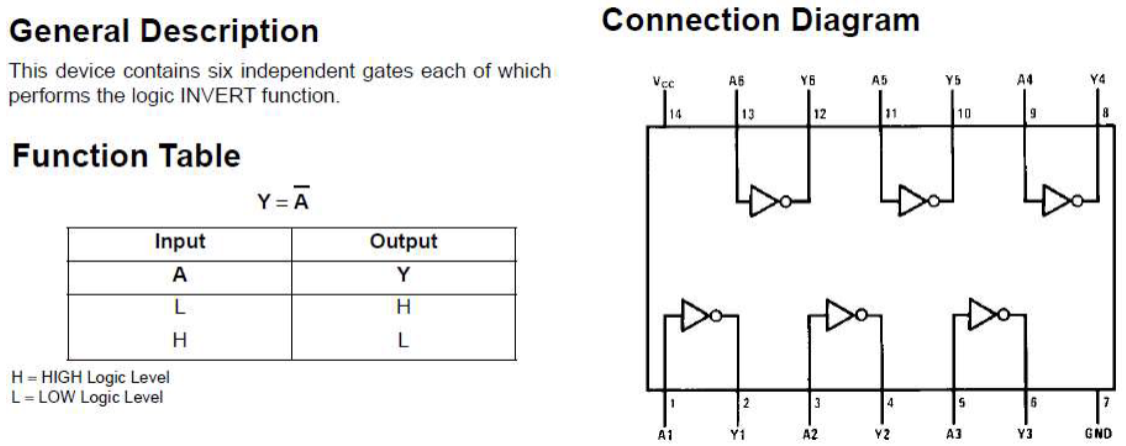


Figure 1: DM74LS04 Partial Datasheet

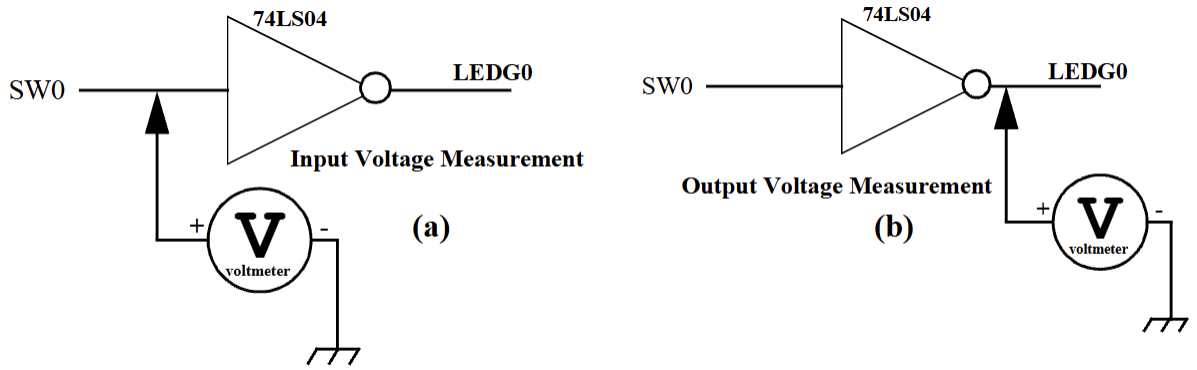


Figure 2: Experiment 2 Wiring Diagrams

After verifying correct wiring, voltages were measured at both locations for logic-low and logic-high input conditions. The input logic level was controlled by toggling Switch 0 on the FPGA board. The measured values are summarized in Tables 2 and 3.

2.4 Experiment 3 - TTL and CMOS Voltage Threshold Evaluation

In this experiment, the input voltage to both a DE2-115 FPGA input pin and an external TTL device input pin was varied to determine the voltage ranges that are interpreted as logic low and logic high. A potentiometer configured as a voltage divider was used to generate an adjustable voltage between 0 V and 5 V. The outer terminals of the potentiometer were connected to 5 V (VCC) and ground, while the center wiper terminal provided the variable input voltage to the test point.

A multimeter and an LP-560 Logic Probe were connected to the potentiometer output simultaneously. As the potentiometer was adjusted, the input voltage was slowly swept from 0 V to 5 V. The voltages at which the logic probe changed its indication were recorded. This process was performed twice: once with the probe set to TTL mode and once in CMOS mode. From

these observations, the values of V_{IL} (maximum input voltage recognized as logic low) and V_{IH} (minimum input voltage recognized as logic high) were experimentally determined for both logic families. The wiring diagram for this experiment is shown in Figure 3.

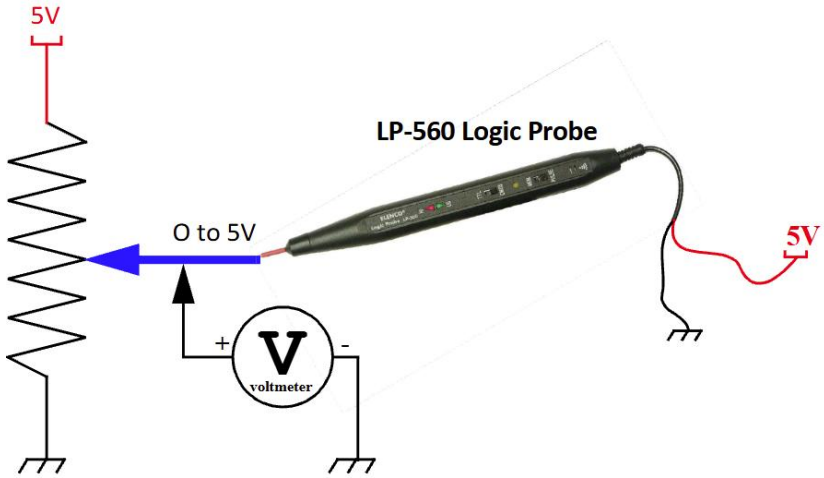


Figure 3: Experiment 3 Wiring Diagram

2.5 Experiment 4 - Connecting Outputs Together Standard TTL

In this experiment, two outputs from the DS74LS04 hex inverter IC used in experiment 4 (see datasheet in Figure 1) were tied together and measured using both a logic probe and digital multimeter. The DS74LS04 was not designed to have its outputs connected. Figure 4 shows the wiring diagram for this experiment. After verifying proper connections, switches 0 and 1 were toggled to produce the 4 possible logic outcomes for this design.

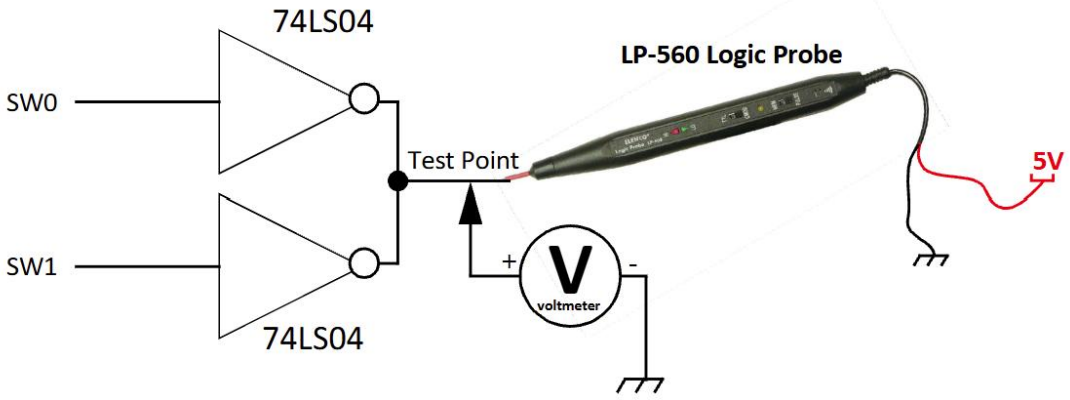


Figure 4: Experiment 4 Wiring Diagram

2.6 Experiment 5 - Connecting Outputs Together Standard Open Collector TTL

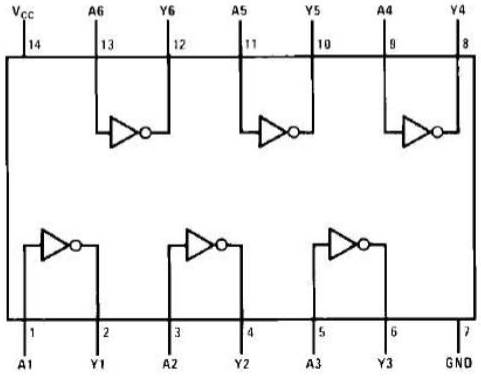
In this experiment, the basic procedure of Experiment 4 was repeated using the DS74LS05 hex inverter IC. This device is specifically designed to allow proper logic operation when two or more outputs are connected because it features open-collector outputs. The measurements taken

in Experiment 4 were repeated to show that open-collector outputs can be safely tied together to implement a valid wired-logic function without producing indeterminate voltage levels. The partial datasheet for the inverter IC and the wiring configurations used for these measurements are shown in Figures 5 and 6. After verifying proper connections, switches 0 and 1 were toggled to produce the 4 possible logic outcomes for this design.

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Connection Diagram



Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Figure 5: DM74LS05 Partial Datasheet

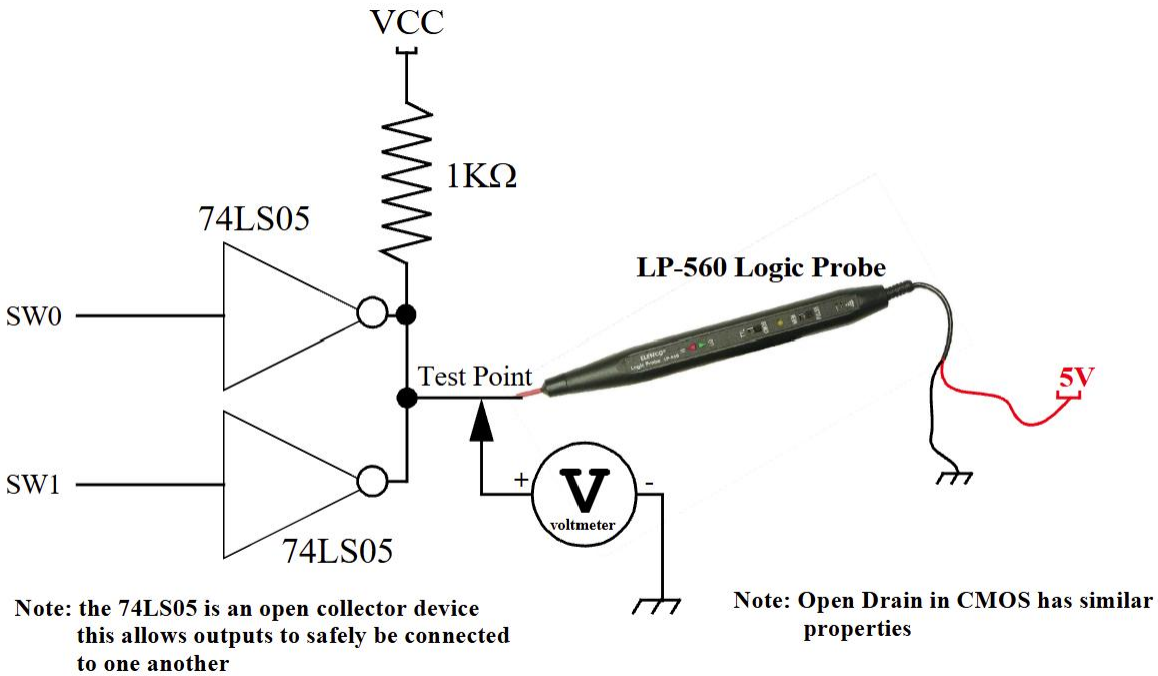
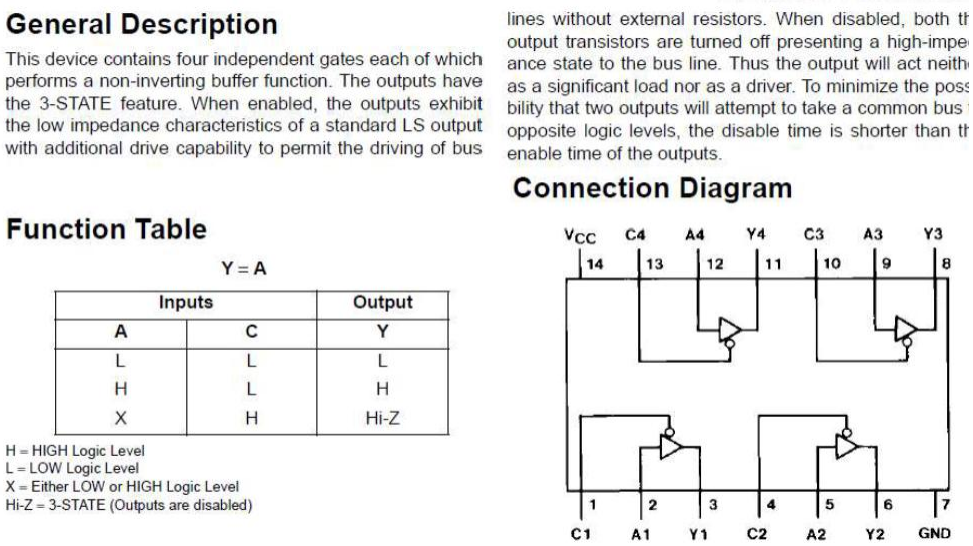


Figure 6: Experiment 5 Wiring Diagram

2.7 Experiment 6 – Tri-State Experiment

In this experiment, the basic procedure of Experiment 4 was again repeated, this time using the DS74LS125 tri-state hex inverter IC. Like the IC in experiment 5, the DS74LS125 allows for outputs to be connected. The partial datasheet for the tri-state inverter IC and the wiring configurations used for these measurements are shown in Figures 7 and 8. After verifying correct connections, switches 0-3 were varied using a given set of test vectors



General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both th output transistors are turned off presenting a high-impe ance state to the bus line. Thus the output will act neith as a significant load nor as a driver. To minimize the poss bility that two outputs will attempt to take a common bus opposite logic levels, the disable time is shorter than th enable time of the outputs.

Function Table

Y = A

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Connection Diagram

Figure 7: DM74LS125 Partial Datasheet

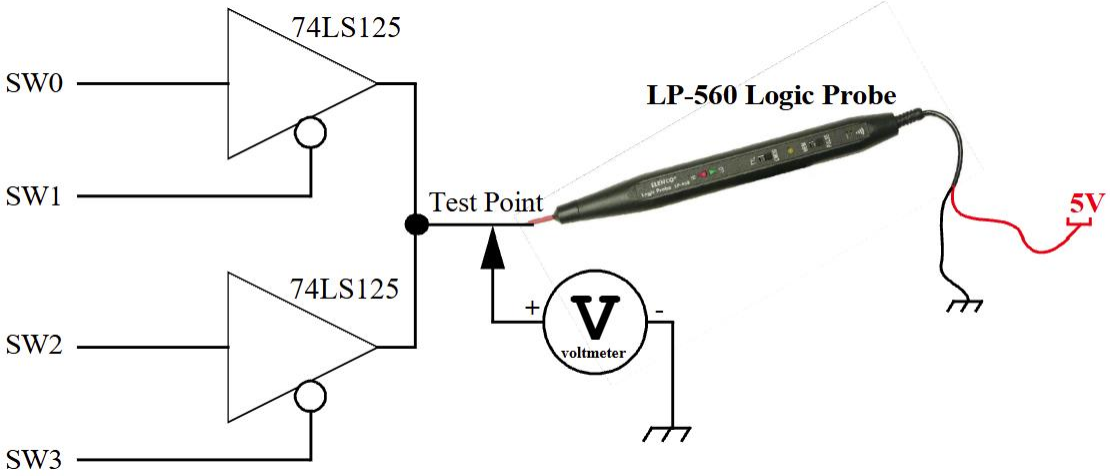


Figure 8: Experiment 6 Wiring Diagram

2.8 Experiment 7 – Signal Integrity, Crosstalk, and Electromagnetic Radiation Issues

The experiment setup involves connecting a speaker to the DE2-115 breakout board through a DC-blocking capacitor and establishing oscilloscope probes across this connection. The D20 clock output of the DE2-115 drives the speaker and a selected HEX6 segment. The

oscilloscope's negative lead is connected to ground, and the main lead is connected to the clock signal. The DE2-115 is configured in Logic Trainer mode to generate automatic clock signals, with SW15 and SW16 used to vary the clock speed and SW17 enabling the clock output. Figure 9 shows the final connected design.

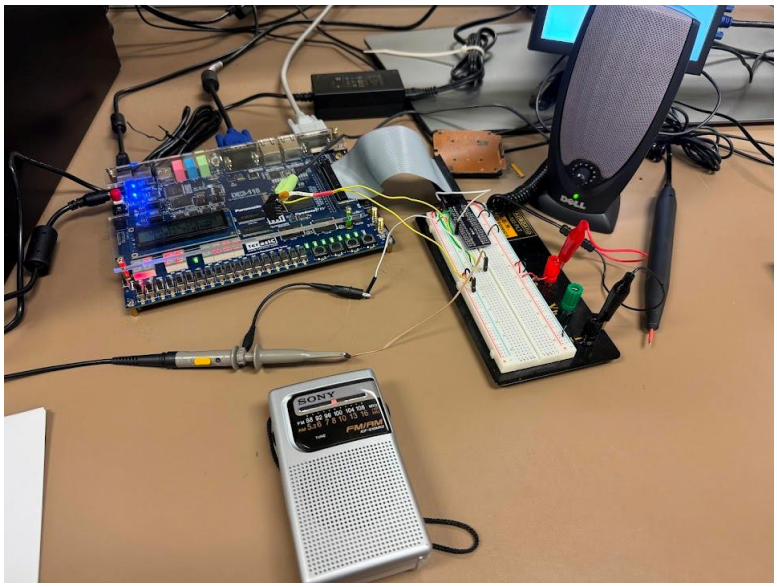


Figure 9: Experiment 7 Physical Setup

During the experiment, the clock frequency is progressively increased, and the following observations were made at each speed: the sound produced by the speaker, the waveform shape on the oscilloscope, the frequency and peak-to-peak voltage, and the effect of disconnecting the speaker load at the highest clock frequency. The output of the HEX6 LED was also observed for expected behavior. Additionally, any electromagnetic radiation emitted by the clock signal was detected using a standard AM receiver, and corresponding frequencies were recorded.

3 Results

3.1 Experiment 1 Results

In Experiment 1, the voltage levels at the 5V Vcc pin and the 3.3V pin were measured using a digital multimeter. The measured values are summarized in Table 1. Both measured values were reasonably close to expected values.

Pin	Voltage Level
5V	4.9185 V
3V3	3.3319 V

Table 1 – Supply Pin Voltage Levels

3.2 Experiment 2 Results

In Experiment 2, voltages were measured at both locations for logic-low and logic-high input conditions. The input logic level was controlled by toggling Switch 0 on the FPGA board. The measured values are summarized in Tables 2 and 3.

Switch 0 Position	Voltage	Logic Probe Level
Down	96.676 mV	Low
Up	3.264 V	High

Table 2: DM74LS04 Inverting Chip Input Measurements

Switch 0 Position	Voltage	LEDG0 State	Logic Probe Level
Down	3.345 V	On	High
Up	224 mV	Off	Low

Table 3: DM74LS04 Inverting Chip Output Measurements

The measured voltage levels show a clear difference between the FPGA board outputs and the TTL inverter outputs. The DE2-115 FPGA board produced a logic high of approximately 3.26 V and a logic low near 0.10 V at the inverter input. In contrast, the DM74LS04 TTL inverter produced a logic high output of approximately 3.35 V and a logic low output near 0.22 V.

Although both devices represent the same logical states, their voltage levels are not identical. The FPGA uses 3.3 V CMOS logic, where a logic high is close to the supply voltage (3.3 V) and a logic low is close to 0 V. TTL logic, however, is based on 5 V supply operation, but its output stages cannot drive all the way to the supply rails. As a result, a TTL logic high is typically between about 2.7 V and 3.5 V, while a TTL logic low is usually between 0 V and 0.4 V. The measured TTL output voltages fall within these expected ranges, explaining why the “high” level is well below 5 V and the “low” level is slightly above 0 V.

TTL logic uses positive logic. In a positive logic system, the higher voltage level represents a logic 1 and the lower voltage level represents a logic 0. This matches the behavior observed in the experiment: higher measured voltages correspond to logic high states, and lower voltages correspond to logic low states.

Overall, while the FPGA and TTL devices operate with different voltage standards, their voltage ranges are still compatible enough to allow correct logic interpretation, which is confirmed by the proper inversion behavior observed in the circuit.

3.3 Experiment 3 Results

In Experiment 3, the values of V_{IL} and V_{IH} were experimentally determined for both TTL and CMOS logic families. The results are summarized in Table 4.

Logic Probe Mode	V_{IL}	V_{IH}
TTL	0.431 V	2.680 V
CMOS	1.363 V	2.963 V

Table 4: Potentiometer V_{IL} and V_{IH} Measurements

The measured output voltages from the DE2-115 (~3.3 V for logic high and near 0 V for logic low) are within the acceptable input range for standard TTL logic—TTL devices typically recognize any voltage above about 2.0 V as a logic high and below about 0.8 V as a logic low, so the DE2-115's outputs were interpreted correctly by the 74LS04 inverter.

Comparing the 74LS04 measurements to the manufacturer's datasheet, the inverter's high-level output (~3.3 V) aligns well with the typical V_{OH} range of 2.7 V–3.5 V expected from LS TTL devices, and the low output (~0.2 V) falls below the typical V_{OL} maximum of ~0.4 V, indicating proper logic low drive. Also, the input switching thresholds ($V_{IH} \geq 2.0$ V, $V_{IL} \leq 0.8$ V) from the datasheet match the observed behavior.

3.4 Experiment 4 Results

In experiment 4, switches 0 and 1 were toggled to produce the 4 possible logic outcomes for the inverter design. The results are summarized in Table 5.

Inputs		Measured Voltage	Logic Probe TTL Logic Level
SW1	SW0		
0	0	4.173 V	High
0	1	1.253 V	Inconclusive
1	0	1.264 V	Inconclusive
1	1	0.181 V	Low

Table 5: Connected Output Inverter Measurements

When two outputs of the DS74LS04 inverter were directly connected, the measured voltages did not always correspond to valid TTL logic levels. For the cases where both inverters attempted to drive the same logic level, the measured voltages were valid: approximately 4.17 V (High) and 0.18 V (Low), respectively. These values fall within normal TTL output ranges.

However, when the two outputs attempted to drive opposite logic levels , the measured node voltage was approximately 1.25 V, which falls between the TTL logic thresholds (VIL ≤ 0.8 V, VIH ≥ 2.0 V). The logic probe therefore indicated an inconclusive state. This occurs because one inverter is trying to drive the line high while the other is trying to drive it low, creating output contention. In this condition, both output transistors conduct simultaneously, forcing the voltage to an intermediate level that is not a valid logic state.

These results demonstrate why standard TTL outputs must not be tied together. Directly connecting outputs can cause unpredictable logic levels, excessive current flow, and potential device damage. Proper bus sharing requires special output structures such as open-collector or

tri-state outputs, which are specifically designed to allow multiple devices to share a common line safely.

3.5 Experiment 5 Results

Similar to Experiment 4, switches 0 and 1 were toggled to produce the 4 possible logic outcomes for an inverting design in Experiment 5. The results are summarized in Table 6.

Inputs		Measured Voltage	Logic Probe TTL Logic Level
SW1	SW0		
0	0	4.719 V	High
0	1	0.656 V	Low
1	0	0.716 V	Low
1	1	0.595 V	Low

Table 6: Connected Output Inverter Measurements

The results show that the output remained at a valid logic high level (≈ 4.7 V) only when both inverter outputs were high (transistors off). When either inverter output was low, the shared node was pulled down to a valid logic low level (≈ 0.6–0.7 V). This confirms correct wired-AND behavior in positive logic, demonstrating that the DS74LS05 can safely share outputs when used with a pull-up resistor.

3.6 Experiment 6 Results

Like Experiments 4 and 5, Experiment 6 results were generated by varying switches 0 through 3 using a given set of test vectors. The results are summarized in Table 7.

Inputs				Measured Voltage	Logic Probe TTL Logic Level
SW3	SW2	SW1	SW0		
0	0	0	0	0.483 V	Low
0	0	0	1	1.273 V	Inconclusive
0	0	1	1	0.223 V	Low
1	0	0	1	3.585 V	High
0	1	0	0	1.056 V	Inconclusive
1	1	0	0	0.283 V	Low
0	1	1	0	3.677 V	High
0	1	0	1	3.551 V	High
1	1	1	0	0.843 V	High Impedance
1	1	1	1	0.854 V	High Impedance
1	0	1	1	0.941 V	High Impedance
1	0	1	0	0.852 V	High Impedance

Table 7: Connected Output Tri-State Inverter Measurements

When both enable inputs are active (likely active-low), the output follows the logic determined by the input switches SW0 and SW2. Measured logic highs ranged from 3.55–4.12 V, and lows were near 0.23–0.26 V, consistent with valid TTL voltage levels. When either enable is inactive,

the output enters a high-impedance (Hi-Z) state, preventing conflicts when multiple devices share the same line. Intermediate voltages around 1–1.25 V were observed in partially enabled cases; these correspond to undefined logic levels.

Tri-state outputs can actively drive a line high, low, or enter Hi-Z, effectively disconnecting from the circuit to allow other devices to drive the line. In contrast, open-collector/open-drain outputs can only pull the line low; logic highs require an external pull-up resistor. Unlike tri-state, open-collector/drain outputs cannot actively drive a high voltage.

Tri-state outputs are commonly used in CPU and memory bus architectures. On shared data buses, multiple devices can connect to the same lines while only one drives the bus at a time, with others in Hi-Z. This prevents bus contention, simplifies circuit layout, and reduces pin count. Examples include memory chips, address/data buffers, and CPU I/O ports.

3.7 Experiment 7 Results

During the experiment, the clock frequency is progressively increased, and the following observations were made at each speed: the sound produced by the speaker, the waveform shape on the oscilloscope, the frequency and peak-to-peak voltage, and the effect of disconnecting the speaker load at the highest clock frequency. The output of the HEX6 LED was also observed for expected behavior. Additionally, any electromagnetic radiation emitted by the clock signal was detected using a standard AM receiver, and corresponding frequencies were recorded.

The results for each clock frequency are summarized in Figures 10 through 13, showing the observed waveform shapes, measured frequencies, and peak-to-peak voltages. These figures illustrate how the clock signals deviate from the ideal square wave as the frequency increases and highlight the influence of connected loads, such as the speaker, and other circuit factors on the signal at different speeds. Each waveform reaches a similar peak-to-peak voltage, however the fastest two clock frequencies do not have enough time to charge the capacitor to the maximum peak-to-peak voltage of 3.5V.

Case 1: Very Slow Clock

Oscilloscope Settings
- Volts per division: 1.66V
- Time per division: 100ms

Measured
- Peak-to-Peak Voltage: 3.5V
- Frequency: 1 Hz

Speaker Observations:

1 Hz beat

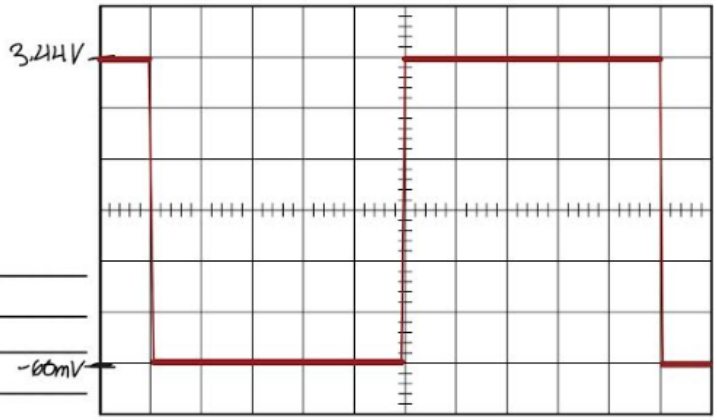
DE2-115 HEX6 7seg LED Observations:

flashing at 1Hz

Electromagnetic Transmission Observations:

out of radio range

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:

very slow square wave
very hard to show on the oscilloscope

Figure 10: Very Slow Clock Measurements and Observations

Case 2: Slow Clock

Oscilloscope Settings
- Volts per division: 1.66V
- Time per division: 200 µs

Measured
- Peak-to-Peak Voltage: 3.5V
- Frequency: 1 kHz

Speaker Observations:

higher pitch constantly emitted

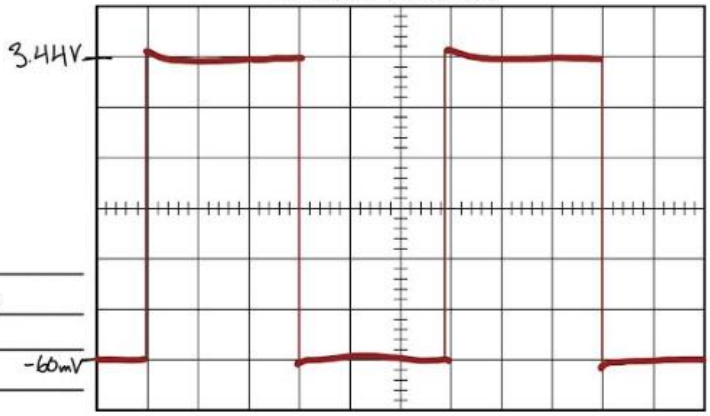
DE2-115 HEX6 7seg LED Observations:

appears on constantly but dim

Electromagnetic Transmission Observations:

out of radio range

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:

corners are slightly curved and not perfectly straight like the previous waveform

Figure 11: Slow Clock Measurements and Observations

Case 3: Medium Clock

Oscilloscope Settings
Volts per division 1.66V
Time per division 2 µs

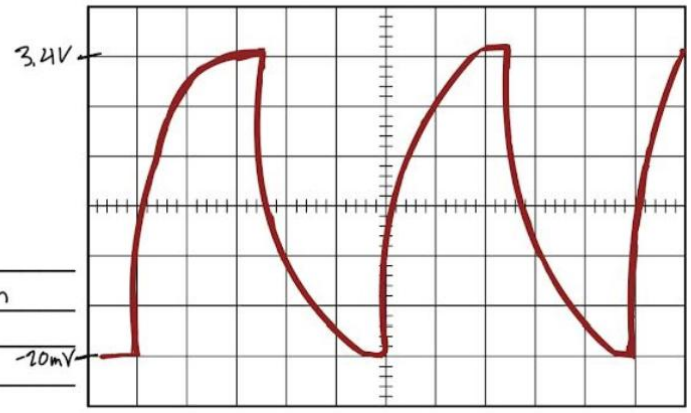
Measured
Peak-to-Peak Voltage 3.4V
Frequency 100 kHz

Speaker Observations:
very low and very quiet hum
almost static sounding

DE2-115 HEX6 7seg LED Observations:
on all the time at a bright level

Electromagnetic Transmission Observations:
out of radio range

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:
no straight edges, instead behaving like an RC circuit

Figure 12: Medium Clock Measurements and Observations

Case 4: Fast Clock

Oscilloscope Settings
Volts per division 1.6 V
Time per division 200 ns

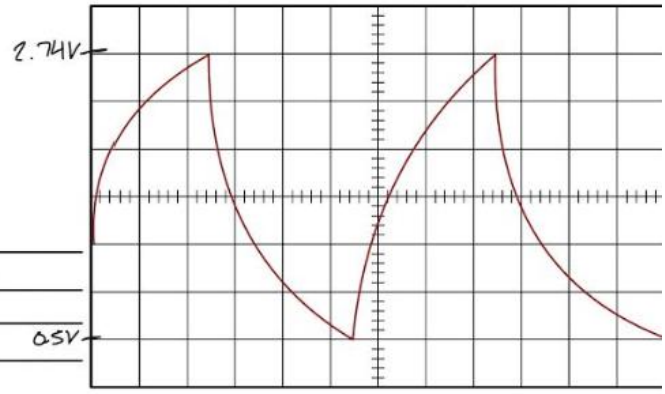
Measured
Peak-to-Peak Voltage 2.22V
Frequency 926 kHz

Speaker Observations:
slightly higher static-like hum
still quiet

DE2-115 HEX6 7seg LED Observations:
always on at the brightest level

Electromagnetic Transmission Observations:
blocks static when on, resumes when off

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:
Very exponential presentation similar to an RC circuit charging and discharging

Waveform Observations when phono plug is removed:
returns to a square waveform with a higher amplitude

Figure 13: Fast Clock Measurements and Observations

The sounds produced by the speaker corresponded directly to the clock signals with a single audible pulse occurring with each clock cycle. When the clock frequency was increased, the speaker produced a faster series of tones, reflecting the higher clock rate. This resulted in a constant tone for the three highest frequencies with the pitch and volume increasing with frequency.

The HEX6 LED exhibited behavior like the speaker. At low frequencies, it blinked visibly with each clock cycle, while at higher frequencies it blinked so quickly that it produced a pulse-width modulated (PWM) effect where the LED appears dimmer or partially on due to the rapid on/off switching. This behavior was expected, and no discrepancies were observed between the LED and the clock frequency.

At the highest clock frequency, disconnecting the speaker caused the waveform on the oscilloscope to change from a sawtooth-like shape to a nearly ideal square wave. This effect occurs because the DC-blocking capacitor in the speaker circuit was removed, eliminating its influence on the waveform.

Using an AM radio, static was detected at a clock frequency of 926 kHz. This indicates that some electromagnetic radiation from the clock signal was being emitted and picked up by the radio, consistent with expectations for high-frequency digital signals. Every other clock frequency was out of range of the radio.

4 Conclusion

This laboratory provided hands-on experience with fundamental digital circuits and the measurement tools used in the Advanced Logic Digital Design Laboratory. Baseline measurements with the FPGA board established expected voltage levels and verified proper operation of supply pins. Experiments with inverters and their interconnected outputs demonstrated how basic logic gates behave individually and in combination, highlighting the effects of loading and signal propagation. The clock signal experiment further illustrated how frequency, connected loads, and circuit components affect waveform shape, observable outputs on LEDs and speakers, and even electromagnetic radiation detectable with an AM radio. Overall, the lab reinforced the importance of careful observation and measurement in understanding the practical behaviors and constraints of digital circuits.