THE UNIVERSITY OF
ALABAMA IN HUNTSVILLE
Department of Electrical and Computer Engineering

CPE 324 Advanced Logic Design Laboratory

Laboratory Assignment #4

Capacitance Tester

(8% of Final Grade)

Purpose

The purpose of this laboratory project is for you to develop a combined digital/analog instrument that can be used to measure the capacitance of a capacitor. The digital portion of this design is to be implemented in Verilog HDL and your design will be tested using the Terasic DE2-115 educational trainer that is interconnected to a 555 IC timer. You will be given the opportunity to develop two different versions of the design using Verilog HDL that vary significantly from one another in terms of the level of abstraction that is employed.

Background

In this laboratory you are to utilize are to use the first principle properties of a RC circuit to experimentally measure the capacitance by accurately measuring the time it takes for the capacitor to discharge through a known high accuracy precision resistance. To accomplish this, the 555 IC timer will be configured as an astable multivibrator. The functional block diagram of the timer is shown in Figure 1 below.

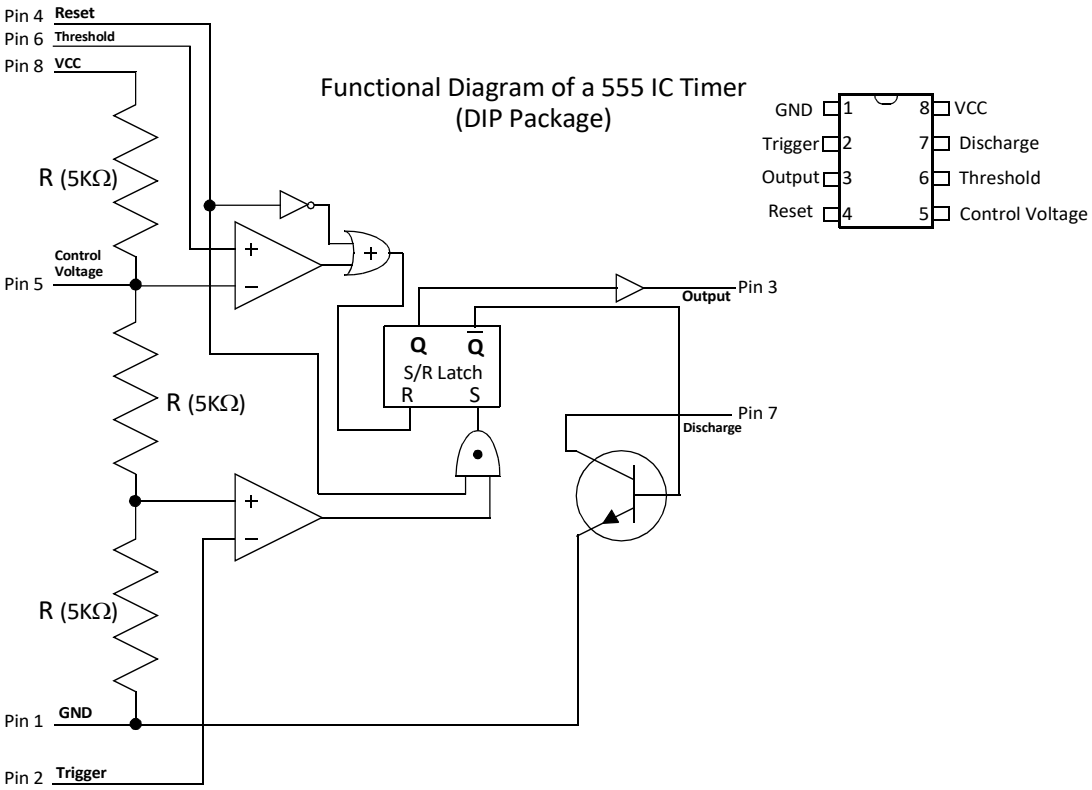


Figure 1: The Functional Block Diagram of the 555 IC Timer

The assumed 555 astable multivibrator circuit and its interface to the DE2-115 trainer are shown in Table 1 which is part of Figure 2.

Table 1: Assumed wiring connections between DE2-115 board and the 555 IC

Signal Name	Cyclone IV E Signal Number	DE2-115 EE2-115 UAH ECE Breakout Board	555 IC Pin Number(s)	555 IC Pin Name
VCC		5V	8, 4	$V_{CC,}$ Reset
GND		GND	1	GND
SIG	PIN_AH23	D34	3	Output

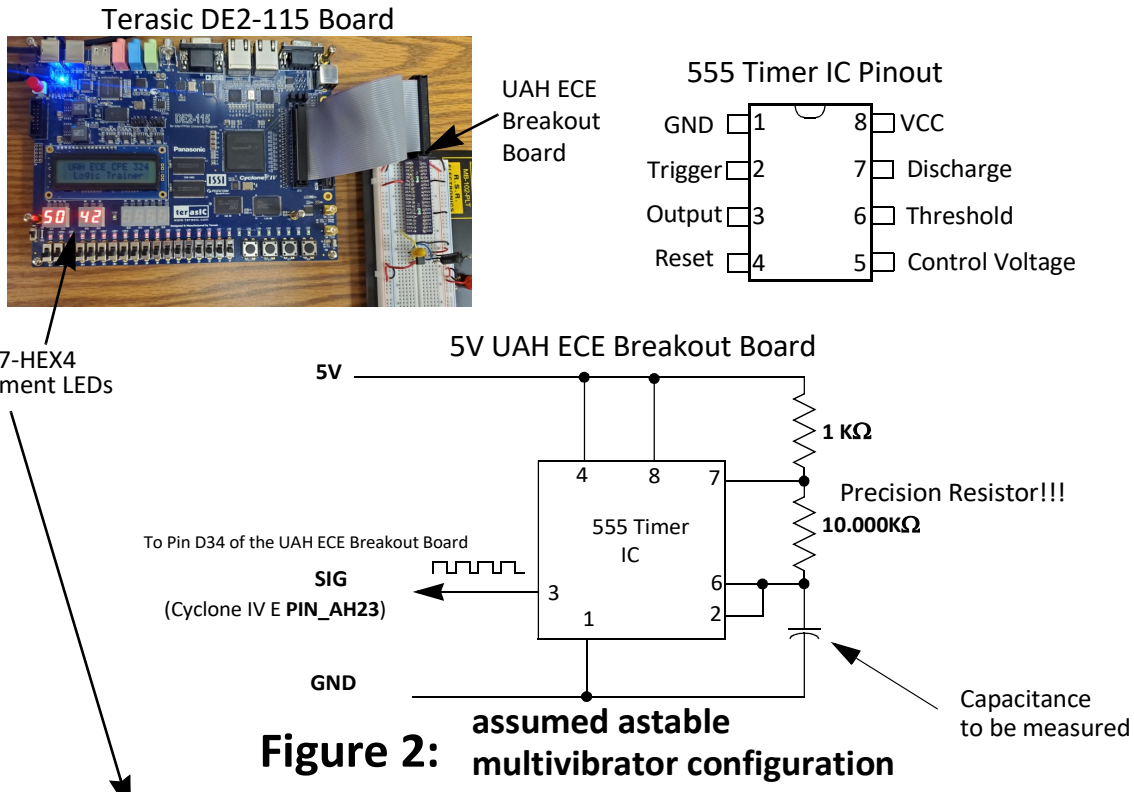


Figure 2: assumed astable multivibrator configuration

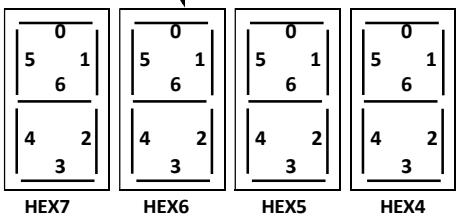


Table 1: Internal DE2-115 Clock

Signal Name	Cyclone IV E Pin Number	Description
CLOCK_50	PIN_Y2	Internal 50 MHz clock input

Table 2: Cyclone IV E Pin Numbers for HEX3-HEX0 7-Seg LEDs on DE2-115 Board

Segment	HEX7		HEX6		HEX5		HEX4	
	Signal Name	Cyclone IV E Pin No.	Signal Name	Cyclone IV E Pin No.	Signal Name	Cyclone IV E Pin No.	Signal Name	Cyclone IV E Pin No.
0	HEX7[0]	PIN_AD17	HEX6[0]	PIN_AA17	HEX5[0]	PIN_AD18	HEX4[0]	PIN_AB19
1	HEX7[1]	PIN_AE17	HEX6[1]	PIN_AB16	HEX5[1]	PIN_AC18	HEX4[1]	PIN_AA19
2	HEX7[2]	PIN_AG17	HEX6[2]	PIN_AA16	HEX5[2]	PIN_AB18	HEX4[2]	PIN_AG21
3	HEX7[3]	PIN_AH17	HEX6[3]	PIN_AB17	HEX5[3]	PIN_AH19	HEX4[3]	PIN_AH21
4	HEX7[4]	PIN_AF17	HEX6[4]	PIN_AB15	HEX5[4]	PIN_AG19	HEX4[4]	PIN_AE19
5	HEX7[5]	PIN_AG18	HEX6[5]	PIN_AA15	HEX5[5]	PIN_AF18	HEX4[5]	PIN_AF19
6	HEX7[6]	PIN_AA14	HEX6[6]	PIN_AC17	HEX5[6]	PIN_AH18	HEX4[6]	PIN_AE18

Assignment

In this assignment you are to explore different design alternatives for creating a capacitance measuring device using the Terasic DE2-115 board with is connected to a 555 timer IC that has been configured as an astable multivibrator. The 555 device will be implemented on a solderless breadboard. The final designs are to continuously display the value of capacitance of a selected capacitor, using four seven-segment LEDs that are present on the DE2-115 board (HEX7 -- HEX4). The design is to support the measurement of capacitances that are in the range of 0.01 μF to 99.99 μF (resolution.01μF).

Part 1 Laboratory Assignment: Structural Design Alternative

The first part of the laboratory assignment is composed of four phases, with each phase culminating with the current state of the design being validated by prototyping it on the Terasic DE2-115 platform. You must successfully complete and demonstrate the valid functionality of a given phase of your design to the lab instructor before proceeding to the next phase. Demonstration will involve configuring the DE2-115 board and verifying that the specified design objectives were met when the specific module was integrated into the overall design. To facilitate design entry a template of the design is provided on the course Canvas website. This template should be first downloaded into your personal file space on the PC's in the laboratory such as your desktop and unzipped. When this is done all the files and subdirectories should be present under the *cpe_lab4* folder. These files include the Quartus project file which includes the pin assignments as well as the top-level file, component files, as well as stub files that are to be completed by you as discussed below.

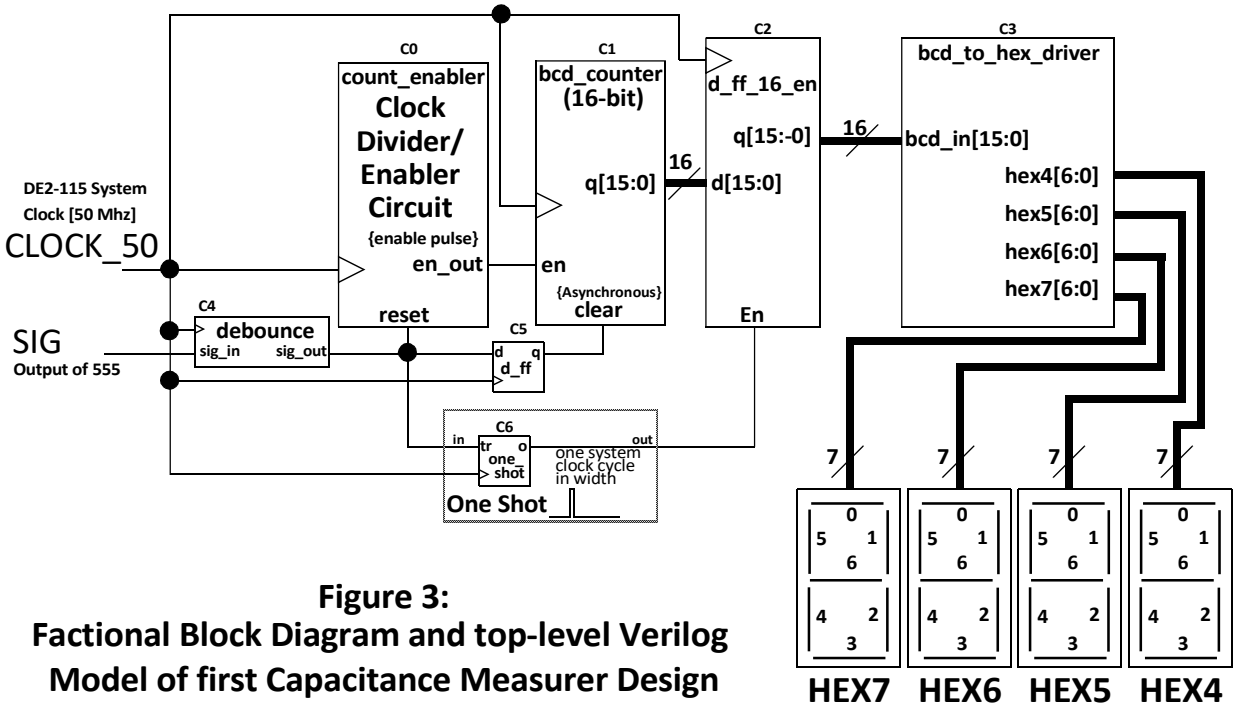


Figure 3:
Factional Block Diagram and top-level Verilog Model of first Capacitance Measurer Design

Phase I: Astable multivibrator design implementation on the solderless breadboard

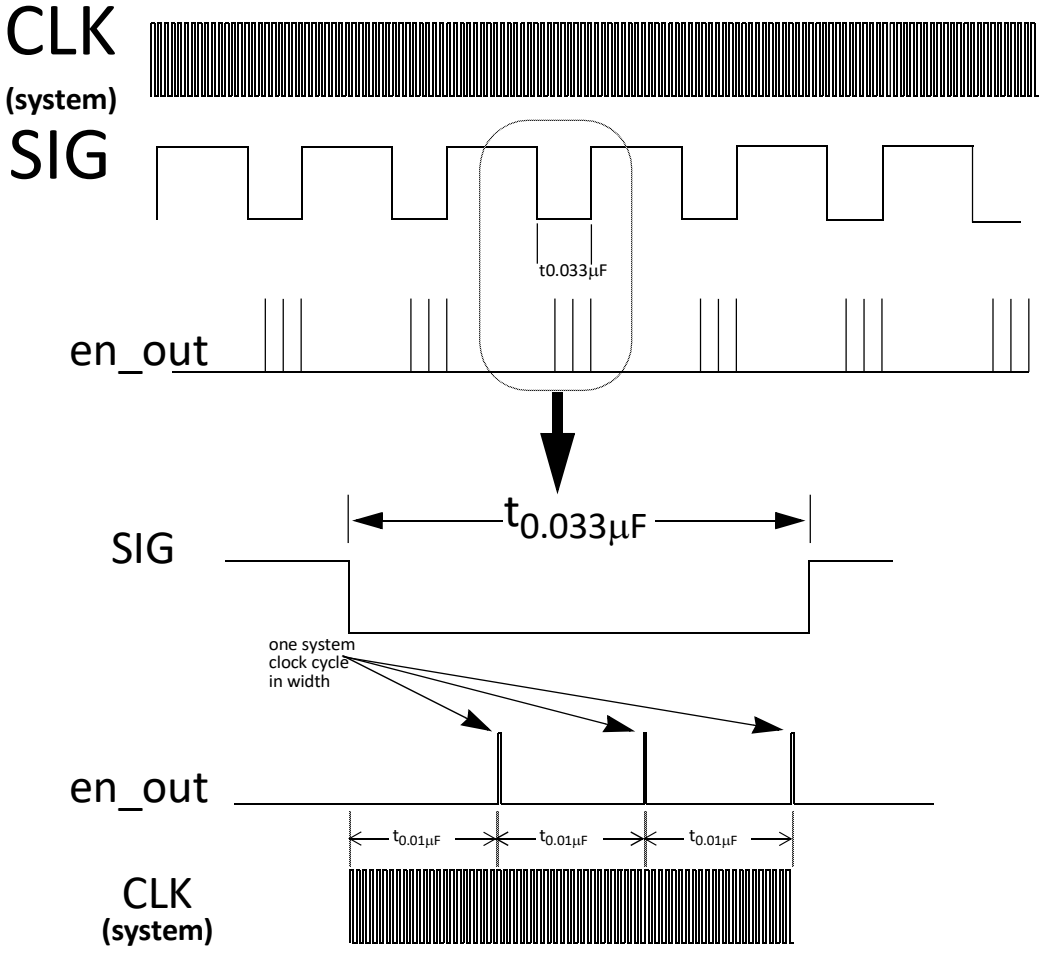
In the first phase of this part you are to implement and verify the operation of astable multivibrator design shown in Figure 2 on the solderless breadboard. Do this by using a capacitor that is rated as 1uF. ***Measure and record the actual value of the 1uF capacitor using the function meter using a multimeter. Also do this for the 10.00 KΩ resister. In your laboratory report, indicate the percent error that your measurement had with respect to the rated value for both cases.*** You will then use the material discussed in class to determine the expected time that the output waveform is at a logic low (this is the time that the capacitor is discharging through the 10.00KΩ

precision resistor). Then use the oscilloscope to display the output waveform and measure this time. ***In your report, include a picture showing one or two periods of the output waveform on the oscilloscope. Also include your measured time of the discharge cycle and compare it with the time you were expecting***.

Phase II: count_enable timing modifications

In this phase you are to are to make the necessary timing changes by to produce the correctly timed enable pulses. You are to do this by modifying the Verilog parameters when the count_enable module is instantiated in the top level of the design. The timing should be determined by calculating the number of complete 50 Mhz clock cycles would occur during the discharge cycle of the 555 IC timer for the case of a 0.01uF capacitor (which is the required resolution of the timer). The **count_enable** module is designed to continue to produce a 50 Mhz pulse for every subsequent 0.01 uF discharge time period allowing the number of **en_out** pulses that occur for capacitors in the range of 99.99uF to 00.01uF to equal the number of discharge time 0.01 uF discharge interval. Figure 4 illustrates that 3 enable pulses would be produced for a 0.033 uF capacitor. Note that the module is designed to produce the first pulse at a discharge time that is 1/2 of the 0.01 uF capacitor time. This is to allow the capacitance to be rounded up on the least significant digit.

Figure 4: Clock Divider/Enabler Waveform Description
(example case when detecting a capacitance of ~0.033μF)



You should see the value of the capacitance on the HEX LEDs but this will be in hexadecimal since the counter is counting in binary not BCD. **In your project report show how you obtained your timing values.** You must obtain the laboratory instructor's approval before going on to Phase III of this laboratory.

Phase III: bcd_counter module modification

Modify the **bcd_counter** module so that it counts in binary coded decimal rather than in binary. When you finish the output on the hex display should show up as decimal, not hexidecimal. ***In your report show you Verilog code that you developed for this module.*** You must obtain the laboratory instructor's approval before going on to Phase IV of this laboratory.

Phase VI: Creation of the *debounce/metastability filter* module using schematic capture design entry techniques

In this phase, you are to develop the basic glitch filtering circuit that filters out short term glitches and reduces the probability of meta-instability that is can occur when non-synchronized inputs drive synchronized logic. This filter is identical to what is often used to remove the effects of switch bounce when the two electrical conducting contacts that are present in a mechanical switch are placed in contact with one another they tend to bounce back and forth causing the electrical connection between them to be made and broken many times before the connection becomes stable.

In this phase of the assignment, you are to develop a structural design connecting eight *D-flip flops* together in a manner that they form an 8-bit *shift register*, and then use an 8-input AND gate and an 8-input NOR gate to cause a J-K flip flop to only change its output when the input signal has been stable for 8 clock cycles. The design should function in the following manner. When an input changes state from high-to-low or low-to-high it must remain at the new state consistently for eight clock cycles before its output makes a similar transformation.

Figure 4 illustrates the desired functionality of the debounce module for both low-to-high and high-to-low transitions. Often simulation is used to verify waveform friendly component elements such as this module but this is not required for this assignment because of the relative simplicity of the design and the time constraints associated with the course.

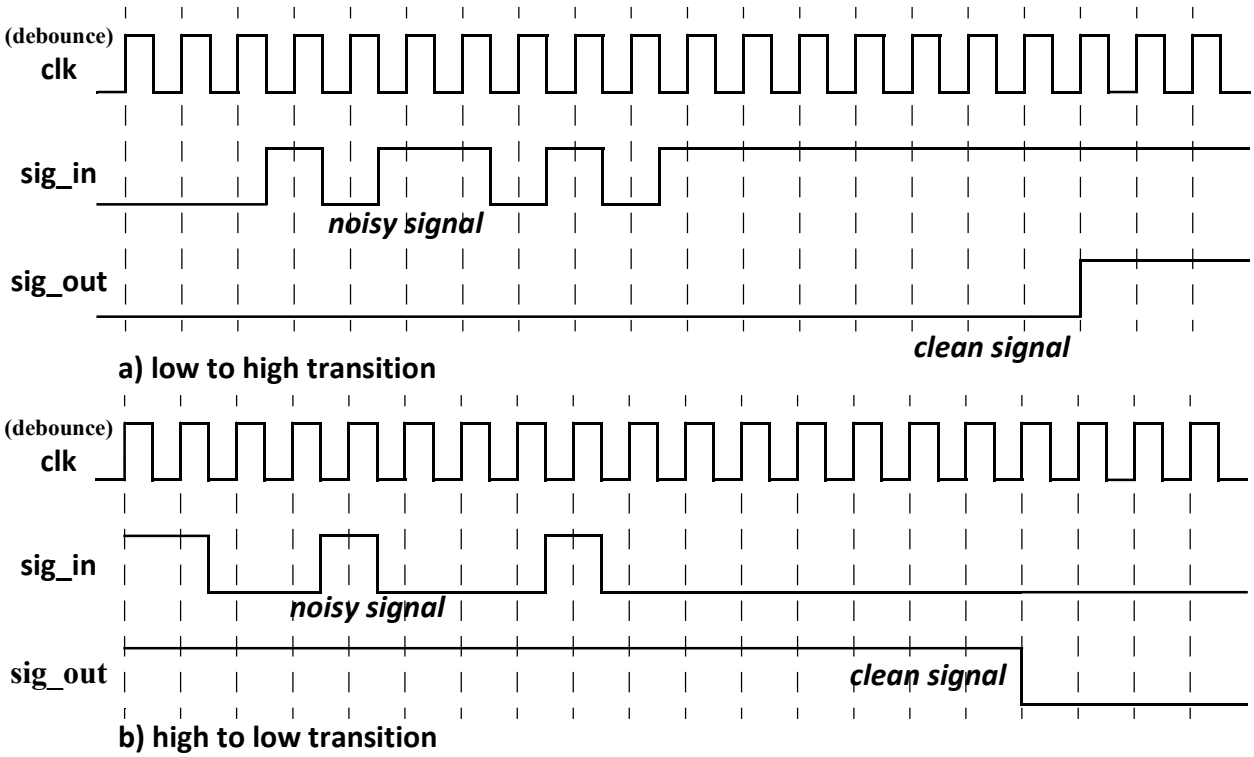


Figure 5: Example Waveforms for *debounce/metastability filter* Module

When you finish your design should have a more constant display. ***In your report show you Verilog code that you developed for this module.*** Demonstrate your complete design to your laboratory instructor. You must obtain the laboratory instructor's approval before going on to Part 2 of this laboratory.

Part 2: Single Module Behavioral Design

The second Verilog model should be a high-level behavioral model that performs the same function but utilizes a single module (i.e. no sub-modules). There are three Verilog HDL templates that are posted on the course's Canvas account. ***Demonstrate you behavioral design to your laboratory instructor. In your lab report compare and contrast these two design alternatives in terms of ease of design entry and their FPGA resource utilization.***

Post Lab Questions

1. Explain the basic operation of the 555 timer when it is placed in multivibrator mode.

2. In terms of accuracy why is it not as important that the 10K resistor have a tight resistance tolerance?

3. How did you modify the parameters to the *count_enabler* module of the mostly structural design? How did you chose the values to use for these parameters that would generate the desired enable rate?

4. In the structural design shown in Figure 3, what is the purpose of the 1-bit D flip-flop? What happens if it is removed?

5. What is the function of a one shot in Figure 3? Why is this important in this design?

6. Describe the thought process for your behavioral design. How did this differ from the mostly structural one?

7. Compare the reported FPGA resource usage of both designs. Which is more efficient in terms of internal logic elements that are utilized? Which was easier to implement? Explain.