THE UNIVERSITY OF
ALABAMA IN HUNTSVILLE
Department of Electrical and Computer Engineering

CPE 324 Advanced Logic Design Laboratory

Laboratory #3

(7% of Final Grade)

Electrical and Timing Characteristics of Digital Hardware

Purpose

The purpose of this part of the laboratory is to give you practical experience in utilizing the test equipment that is present within the Advanced Logic Digital Design Laboratory which you will use to observe and better understand some of the basic electrical considerations that are important to successful digital design.

General Experimental Setup

The following set of experiments will allow you to empirically explore some of the lower-level electrical and timing characteristics that are important to digital design. The tools you will use include the Terasic DE2-115 digital rapid prototyping platform (configured in its default logic trainer configuration), a logic probe, a digital multimeter, an oscilloscope, an amplified speaker and a simple AM radio. ***In this part of the laboratory assignment, you should team up with another student to conduct each of the experiments. The write-up for your laboratory report, though, should be performed by you on an individual basis.***

Experiment #1: Basic Voltage measurements from the DE2-115.

The DE2-115's general purpose input and output pins have been configured to operate at voltage levels that are compatible with Low Voltage Transistor-to-Transistor, LVTTL and the external device all operate at standard Transistor-to-Transistor, TTL logic levels.

- Using the digital multimeter carefully measure the actual 5V and 3V3 DC supply signals that come from the DE2-115 and are brought out to your solderless breadboard through the 40 pin breakout board. (note ALL voltage measurements are always assumed to be measured with respect to GND, the common ground).

Record this measurement: DE2-115 supplied from the 5V pin = _____

Record this measurement: DE2-115 supplied from the 3V3 pin = _____

Experiment #2: DE2-115/TTL Device Output Voltage Measurements

DM74LS04
Hex Inverting Gates

FAIRCHILD SEMICONDUCTOR™

General Description

This device contains six independent gates each of which performs the logic INVERT function.

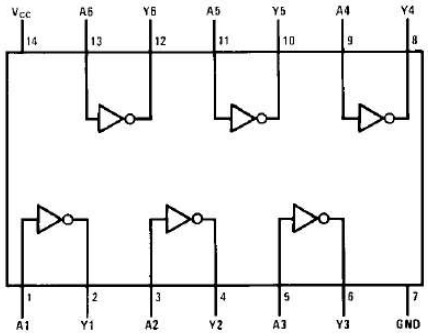
Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Connection Diagram



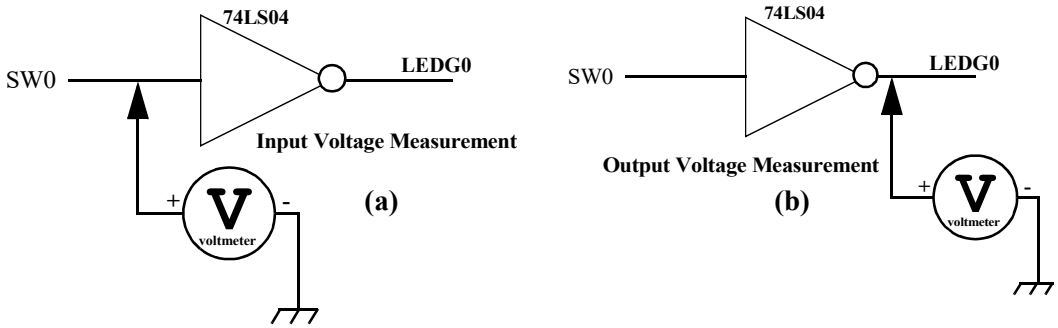


Figure 1: Voltage Measurements on the Inputs and Outputs of the 74LS04 IC

Connect a single 74LS04 hex inverter IC to your design so that the input of one of the inverters is connected to the DE2-115 switch SW0 and the output is connected to the DE2-115 LEDG0 as shown in Figure 1.

- Now use the digital multimeter to measure the output voltage that comes from the DE2-115 Switch SW0 (and into the inverter) as shown in Figure 1a and also probe this signal with the ELENCO LP-560 logic probe in TTL and pulse modes.
  Then record
  when SW0 is down
  Voltage = _____, Logic Probe reported logic level _____
  when SW0 is up
  Voltage = _____, Logic Probe reported logic level _____
- Now use the digital multimeter to measure the output voltage that comes from the selected 74LS04 inverter (and into the DE2-115) as shown in Figure 2b and observe this signal on the red LED of the DE2-115. Use your logic probe to confirm the logic levels reported by the DE2-115.
  Then record
  when SW0 is down
  74LS04 Output Voltage = _____, LED Light (on/off) _____
  when SW0 is up
  74LS04 Output Voltage = _____, LED Light (on/off) _____

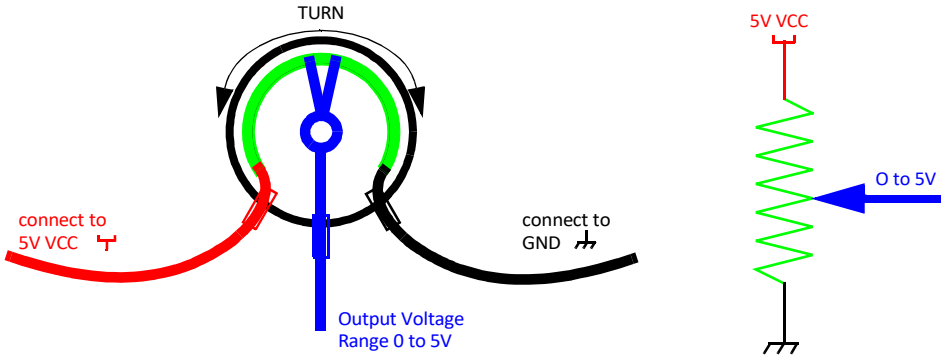
In your laboratory report, comment on these voltage levels. For a given Logic High or Low are the voltage levels from outputs of the DE2-115 the same as those for the TTL logic? Does TTL logic use positive or negative logic? Explain.

Experiment #3: TTL and CMOS Voltage Threshold Evaluation

In the first set of experiment, you are asked to vary the input voltage experimentally on one of the input pins of the DE2-115 platform and one of the input pins of an external device that is placed on the solderless breadboard. This will allow you to empirically determine the range of voltages that will consistently interpreted as a logic high and logic low, respectively.

To vary the voltage at the inputs to both the DE2-115 and an external TTL device you will employ a simple potentiometer which is in effect a three terminal device that implements a voltage divider network, where the tap point along the resister can be moved from the top to bottom. If the two outer leads are connected to the VCC (5 Volt) reference point and to ground, and the load circuit draws a negligible amount of current through the adjustable tab lead (such as is the case when this lead is connected to a VLTTL or TTL logic input), then the potentiometer can be turned to create an arbitrary input voltage that is between 0 and VCC (5 Volts). (This could also be accomplished by employing an external variable voltage power supply that shares a common ground with the DE2-115. Such an experimental setup, though, would carry with it the risk of damaging the DE2-115 and device electronics if the voltage level was inadvertently set to a value that was greater that the 5 Volt range.)

Figure 2 show a diagram that highlights the physical configuration of such a device and its schematic symbol.



Physical Functional Diagram

Schematic Symbol

Figure 2: Basic Potentiometer Configuration

In this laboratory the potentiometer will always be configured with one of the outer two leads connected to the 5V VCC and the other outer lead connected to GND. The middle lead will be used to drive the specified input of the entire voltage range of 0 to 5 volts.

You are to experimentally evaluate the voltage thresholds that are interpreted by the LP-560 Logic Probe. This probe has been designed to only respond to voltages within the range of acceptable voltages for TTL and CMOS. In both cases there is a voltage, V_{IH}, that is defined to be the minimum voltage that a device can be driven that it is guaranteed to be accepted as a logic high. In a similar manner the voltage, V_{IL}, is the maximum voltage that can be applied to an input and it still be interpreted as a logic low. The region in between these two voltages is forbidden. Devices respond unpredictably if their inputs have voltages applied that fall into this region.

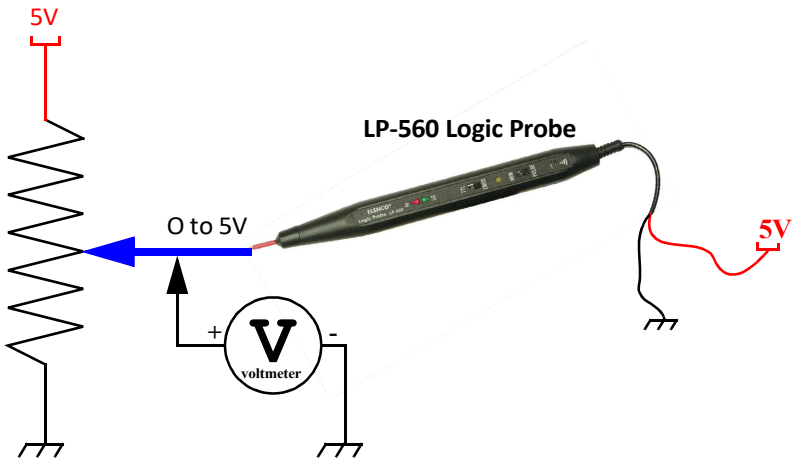


Figure 3: Voltage Measurements on the Inputs and Outputs of the 74LS04 IC

- Simultaneously connect the multimeter and the LP-560 Logic Probe across the middle lead of the potentiometer and as shown in Figure 3. Then carefully turn it so that the voltage across the tab lead varies from 0 to 5 volts. Record V_{IL} and V_{IH} for both TTL and CMOS. This is accomplished by performing the experiment twice -- once with the Logic probe in TTL mode and once when it is in CMOS mode.

Logic Probe Mode	V_{IL}	V_{IH}
TTL		
CMOS		

I***n your report comment on whether the DE2-115 VLTTL output voltage values fall within the acceptable region for a TTL to interpret it as a logic high or a logic low. Also in your report review the complete data sheet on the 74LS04 and compare the readings you obtained with those that are expected***.

Experiment #4: Connecting Outputs Together Standard TTL

Most TTL logic gates are not internally designed to have their outputs connected to the outputs of other similar gates. In this experiment you are to see what happens when is done. The 74LS04 IC contains such standard gates.

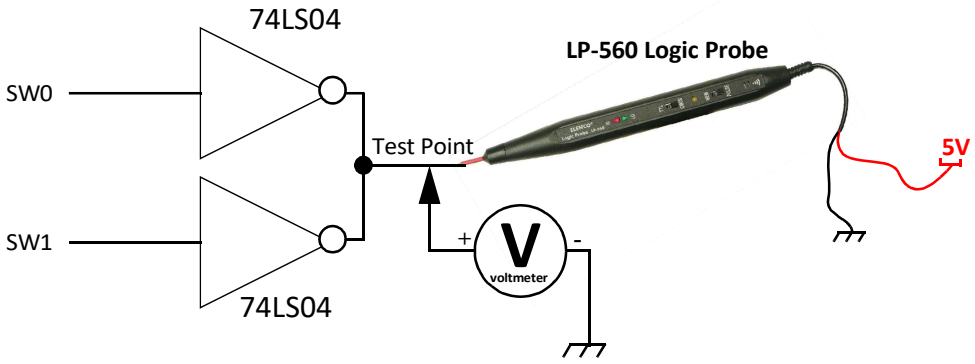


Figure 4: Connecting Multiple Outputs Together Standard TTL

Complete the following table

Inputs		Measured Voltage	LP-560 Logic Probe Indicated TTL Logic Level
SW1	SW0		
0	0		
0	1		
1	0		
1	1		

Are there any voltage levels that are in the so called forbidden region where the voltage present at the input of the logic probe has a value that is in between the range interpreted as a valid logic high or a logic low for TTL logic? If so indicate the cases where these occur. Why do you think that in most cases it is not wise to connect outputs together.

Experiment #5:Connecting Outputs Together Standard Open Collector TTL

In other cases the gates can be specially designed so that connecting outputs together will perform an actual logic function. Such a configuration is called wired logic configuration. The 7405 is such a component that has been designed to allow multiple outputs to be connected together as long as an external pull-up resister is applied. Repeat Experiment #4 but using a 7404 and connecting a 1 KW pull-up resistor from the common output to the 5V VCC as shown in Figure 6.I

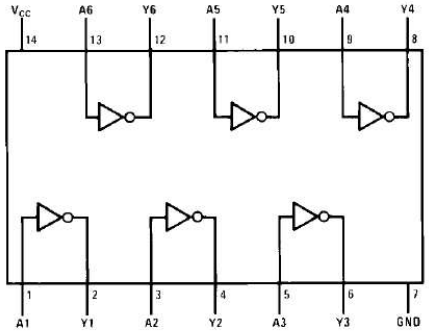
DM74LS05
Hex Inverters with Open-Collector Outputs

FAIRCHILD SEMICONDUCTOR™

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Connection Diagram



Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Figure 5: Partial Data Sheet 74LS05

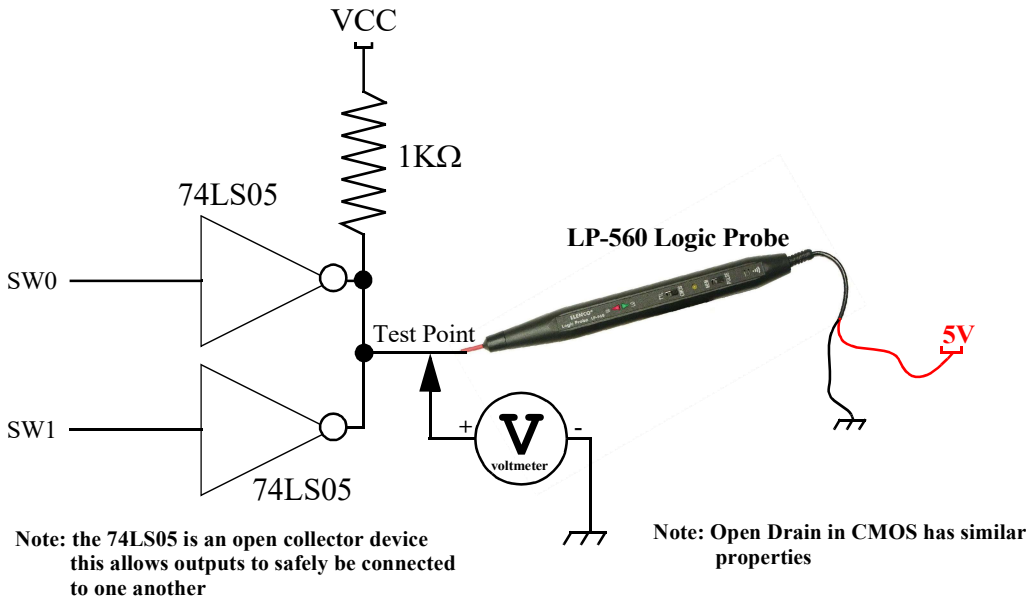


Figure 6: Connecting Multiple Outputs Together
Open Collector TTL

Complete the following table for the 74LS05 Circuit shown in Figure 6.

Inputs		Measured Voltage	LP-560 Logic Probe Indicated TTL Logic Level
SW1	SW0		
0	0		
0	1		
1	0		
1	1		

Are there any voltage levels that are in the forbidden TTL region? If so indicate the cases where these occur. What is the logic function that can be expressed by the table above if we assume positive logic? If TTL logic was negative logic instead of positive logic what logic function would this truth table represent?

*Comment: For most digital designs, modeling and simulation is not performed at the analog level where we are interested in voltages and currents as time progresses. Instead it occurs at a higher level of abstraction using a number of discrete states. Two of these states include the Boolean states of 1 and 0. In these cases the actual voltages produced by the logic devices are somewhere in the voltage range associated with these levels as dictated by the particular logic family. Another discrete state that digital logic simulation employes is the state of **X**. This state indicates that the actual output is unknown. One source of an **X** state being produced in digital logic simulation is when the output of two or more gates are connected together as in Experiment #4 and these gates are not designed to support wired logic. A value of **X** would be produced by the simulation whenever the logic of two gates that share an output drive this output to opposite Logic 0 and 1 states.*

Experiment #6: Tri-State Experiment

Complete the following table for the 74LS125 Circuit shown in Figure 7. This is another special case where outputs can be connected together.

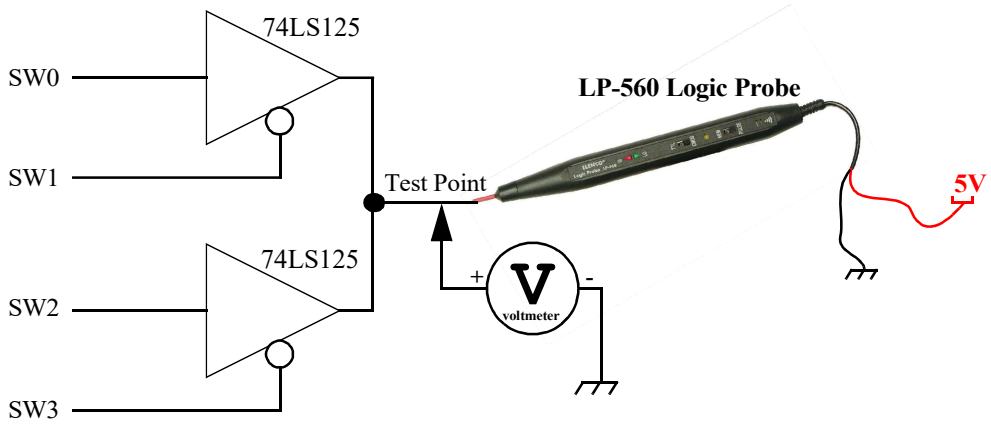


Figure 7: Connecting Multiple Tri-State Outputs Together

DM74LS125A Quad 3-STATE Buffer

FAIRCHILD SEMICONDUCTOR™

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Function Table

Y = A

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Connection Diagram

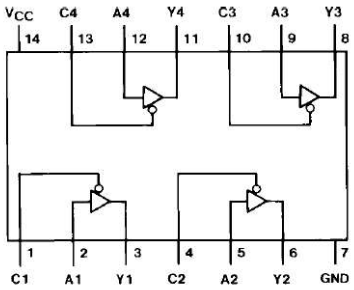


Figure 8: Partial Data Sheet 74LS125

Inputs				Measured Voltage	LP-560 Logic Probe Indicated TTL Logic Level
SW3	SW2	SW1	SW0		
0	0	0	0		
0	0	0	1		
0	0	1	1		
1	0	0	1		
0	1	0	0		
1	1	0	0		
0	1	1	0		

Inputs				Measured Voltage	LP-560 Logic Probe Indicated TTL Logic Level
SW3	SW2	SW1	SW0		
0	1	0	1		
1	1	1	0		
1	1	1	1		
1	0	1	1		
1	0	1	0		

Complete the above table and comment on your observations. Report on how tri-state differs from open-collector or open-drain configurations. Where and how are tri-state devices used in many CPU memory architectures?

Experiment #7: Signal Integrity, Crosstalk, and Electromagnetic Radiation Issues

Modern synchronous designs incorporate a large number high speed periodic clock signals. These signals can differ significantly from the ideal case of 50% duty cycle square waves due to parasitic capacitive and inductive effects associated with the actual implementation. These effects become more pronounced as their frequencies increase and also depend upon such factors as device technology, voltage levels, lead length, trace length, trace widths, and device technology. Conduction paths that are placed physically close to one another can become mutually coupled introducing crosstalk noise in each other. Also long conduction paths can act as small antennas resulting in electromagnetic radiation which can further compromise operations or interfere with other devices. The purpose of this experiment is to empirically observe some of these conditions using the oscilloscope, a speaker and the trainer itself.

The oscilloscope is a very useful tool to view signal quality. In this experiment you are to utilize it to view the shape of the periodic clock signal that is automatically generated by the DE2-115 when it is in Logic Trainer Configuration. You will also be using the oscilloscope to measure the frequency of the clock and peak to peak voltage range.

Experiment Setup

- Obtain an amplified speaker and connect its male 3.5mm phono jack into the cable assembly that has been created for this experiment in the manner shown in Figure 8 below. This assembly is composed of a female receptacle that is connected to a simple DC blocking capacitor which allows AC signals to pass through.

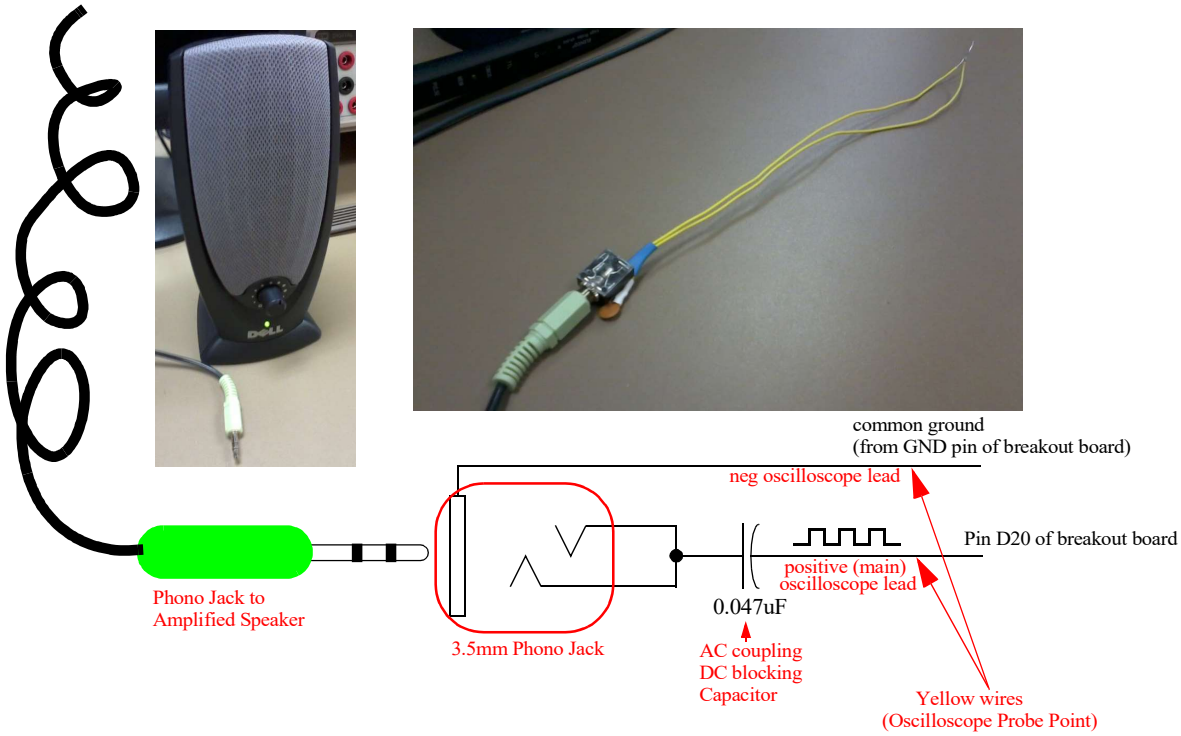


Figure 8: Clock Measurement Setup

- Then connect one of the yellow leads of the 3.5 mm phono cable assembly to the ground connection of the solderless breadboard.
- Connect the other yellow lead of this assembly to the Pin 20 of the DE2-115 breakout board as shown below in Figure 9:

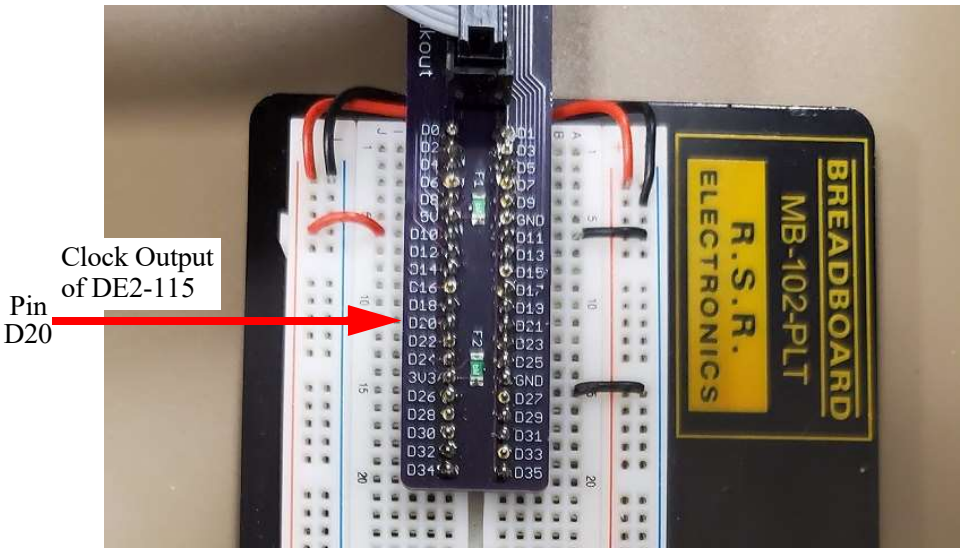


Figure 9: UAH Breakout Board

- Interconnect the breakout board's D20 clock pin to one of the HEX6 segment inputs pin D0 to D6 to connect the clock so it will drive one of the seven segments.
- Connect the oscilloscope's negative lead to the breadboard's ground.
- Connect the oscilloscope's main lead to the D20 clock pin location. The oscilloscope probes should now be across the two yellow wires of the speaker cable assembly.
- Configure the DE2-115's Logic trainer to generate automatic clock signals through the breakout board's D20 pin (SW17 should be in the up position, SW16, and SW15 will be used to vary the clock speed). SW10 must be in the down position for the clock to work.
- Turn on the amplified speaker, the oscilloscope and the DE2-115.

In this experiment you will progressively increase the clock rate of the Terasic DE2-115 trainer by using the SW16 and SW15 slide switches. For each of the four speeds you will then

- Observe any sounds you hear from the speaker. **Explain in your report the source of such sounds.**
- Where possible, sketch the general shape of the waveforms you observed on the oscilloscope. **In your laboratory report discuss how these waveforms deviate from the ideal shape.**
- Measure the frequency and peek-to-peek voltage using the oscilloscope.
- For the highest clock frequency, after making your sketch of the waveform, disconnect the speaker phono plug. **In your report comment on the effect of disconnecting this load from the clock driver. Speculate on the reason for any changes in the waveform.**
- Observe the output of the HEX6 LED on the DE2-115 board. **Describe in your report what you would expect to see and any discrepancies you may have experienced. Speculate on why these may have occurred.**
- Determine if there is any electromagnetic radiation of your clock signal on the broadcast band using a standard AM receiver. To do this, first slowly turn the AM dial until you hear the static disappear. Then check to see if the reason it disappeared is due to the AM radio picking up a signal from the speaker wire. If the static returns when you turn off the DE2-115 using the big red push button, then the signal probably came from the speaker wire. **In this case write down the AM frequency reading on the dial where this occurred? Do any or all of the readings correspond to the predominate frequency that you measured on the oscilloscope? If so report this reading in your report.**

Please Note: The AM radio decodes signals that are Amplitude Modulated. In general the term modulation refers to the act of putting useful information on a radio frequency signal. Amplitude Modulation places voice information on the signal by modifying the amplitude of the signal. AM broadcast band is a relatively low frequency band. This band has the assigned frequency range of 0.535 MHz to 1.705 Mhz.

The telescoping antenna that is part of the AM/FM radio you are using in this experiment is the antenna for the FM radio not the AM radio. Extending this antenna for this experiment will have little or no effect on what is received by the AM radio. The AM antenna is a smaller coil of wire that is inside the enclosure. The reason this type of antenna is used for AM is because the wavelength of the signals on the AM band is so large that making a full size 1/4 wave antenna using telescoping antenna is not feasible. The built-in antenna is not optimal but should be adequate to receive signals that are generated from the DE2-115. Please just orient the AM/FM radio case carefully instead of using the telescoping antenna when performing your experiments.

- **Discuss in your report cases where electromagnetic effects such as are observed could be useful as well as cases where such effects are not desirable and could compromise functionality or even security.**
- Present your observations as part of your Laboratory report. Are

It should be noted that the oscilloscope *AUTO, Measure, Acquire* and *Display* features should be very useful for this experiment.

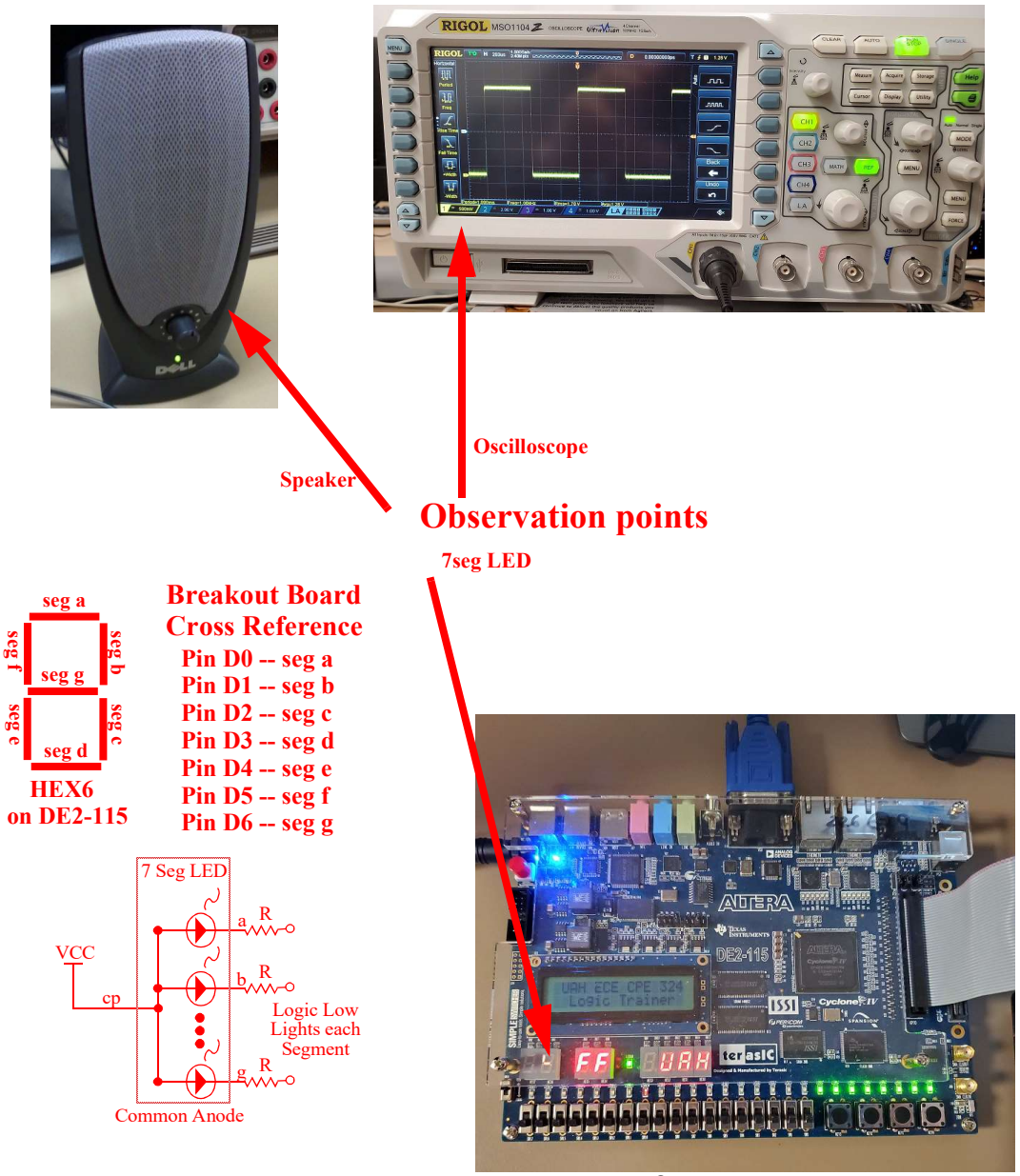


Figure 10: Observation Points for Experiment 7

Case 1: Very Slow Clock

Oscilloscope Settings

Volts per division _____

Time per division _____

Measured

Peak-to-Peak Voltage _____

Frequency _____

Speaker Observations:

_____

_____

_____

_____

DE2-115 HEX6 7seg LED Observations:

_____

_____

_____

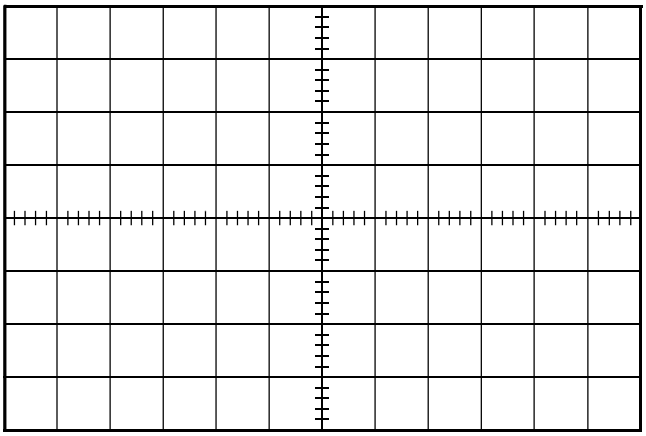
_____

Electromagnetic Transmission Observations:

_____

_____

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:

_____

_____

_____

_____

Case 2: Slow Clock

Oscilloscope Settings

Volts per division _____

Time per division _____

Measured

Peak-to-Peak Voltage _____

Frequency _____

Speaker Observations:

_____

_____

_____

_____

DE2-115 HEX6 7seg LED Observations:

_____

_____

_____

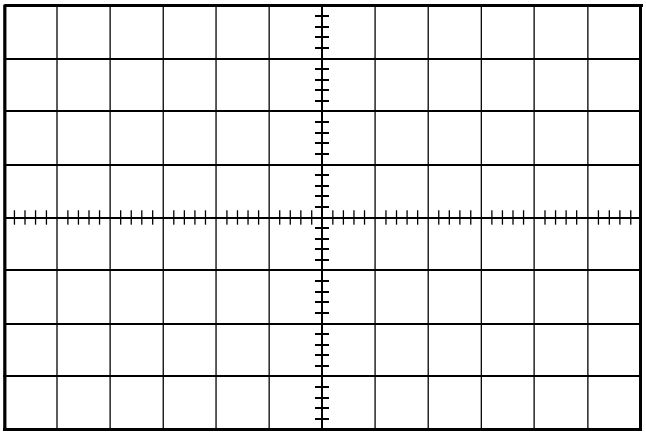
_____

Electromagnetic Transmission Observations:

_____

_____

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:

_____

_____

_____

_____

Case 3: Medium Clock

Oscilloscope Settings

Volts per division _____

Time per division _____

Measured

Peak-to-Peak Voltage _____

Frequency _____

Speaker Observations:

_____

_____

_____

_____

DE2-115 HEX6 7seg LED Observations:

_____

_____

_____

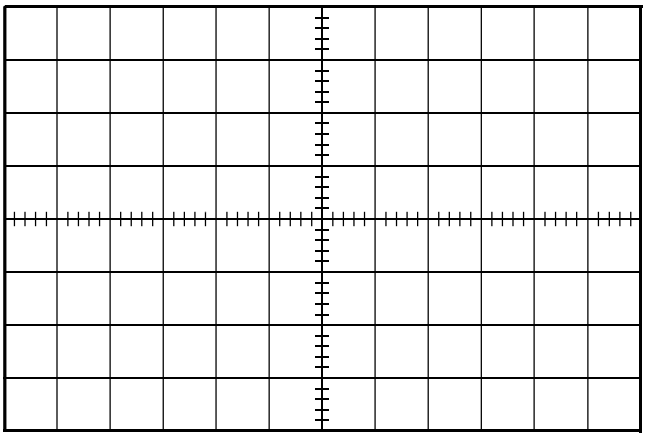
_____

Electromagnetic Transmission Observations:

_____

_____

Waveform Sketch



when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:

_____

_____

_____

_____

Case 4: Fast Clock

Oscilloscope Settings

Volts per division _____

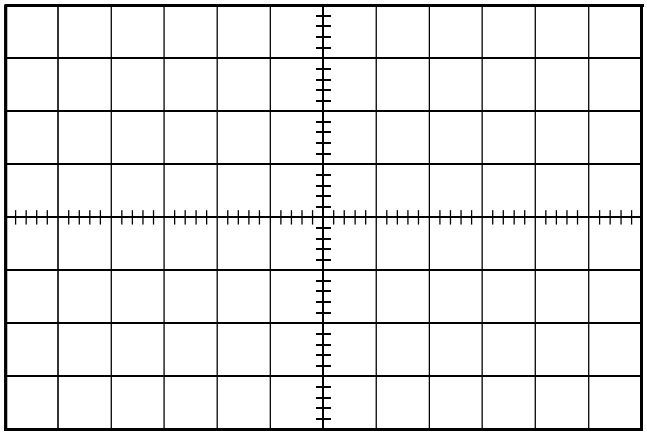
Time per division _____

Measured

Peak-to-Peak Voltage _____

Frequency _____

Waveform Sketch



Speaker Observations:

_____

_____

_____

_____

DE2-115 HEX6 7seg LED Observations:

_____

_____

_____

_____

when possible, adjust time mode so that two complete periods of the waveform are displayed

Waveform Observations:

_____

_____

_____

_____

Electromagnetic Transmission Observations:

_____

_____

Waveform Observations when phono plug is removed:

_____

_____

What are the generally accepted range of audio frequencies and radio frequencies? How do they differ from one another? Use this to explain some of your results in this experiment (Experiment 7) in your report.

Additional Post Laboratory Questions:

Answer all questions presented in this laboratory in the appropriate section of your laboratory report. Include as background the complete definitions of the following general terms that relate to the timing and electrical characteristics of digital logic. These terms are crosstalk, clock skew, rise time, fall time, propagation delay, setup time, and hold time. You may use your class text or other general sources in this portion of the assignment.