Heterogeneous Parallel Programming COMP4901D

Data-Parallel Primitives:

Scatter and Gather

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Overview

- Data-Parallel Primitives
  - Map, Prefix Scan, Scatter, Gather, Split, Sort
  - Others: Reduce, Filter, Search…
- GPU-Based Implementations
  - Gather and Scatter

Processing a Large Number of Data Items

```
//sequential
   for (i = 0; i < N; i++)
           h_C[i] = h_A[i] + h_B[i];

//data-parallel
__global__ void VecAdd(int* A, int* B, int* C)
{
   int i = blockDim.x * blockIdx.x + threadIdx.x;
   C[i] = A[i] + B[i];
}
```

Map and Prefix Scan

Primitive: Map
Input: R_{in} [1, …, n], a map function *fcn*.
Output: $R_{out}[1,\ldots,n]$.
Function: $R_{out}[i]=fcn(R_{in}[i])$.

Primitive: Prefix Scan
Input: R_{in} [1, …, n], binary operator $\oplus$.
Output: $R_{out}[1,\ldots,n]$.
Function: $R_{out}[i]=\bigoplus_{j<i} R_{in}[j]$.

Scatter and Gather

Primitive: Scatter
Input: $R_{in}[1, \ldots, n]$, $L[1, \ldots, n]$.
Output: $R_{out}[1, \ldots, n]$.
Function: $R_{out}[L[i]]=R_{in}[i]$, $i=1, \ldots, n$.

Primitive: Gather
Input: $R_{in}[1, \ldots, n]$, $L[1, \ldots, n]$.
Output: $R_{out}[1, \ldots, n]$.
Function: $R_{out}[i]=R_{in}[L[i]]$, $i=1, \ldots, n$.

Split and Sort

Primitive: Split
Input: $R_{in}[1, \ldots, n]$, $func(R_{in}[i]) \in [1,\ldots,F]$, i=1, …, n.
Output: $R_{out}[1, \ldots, n]$.
Function: $\{R_{out}[i],\ i=1,\ldots,\ n\} = \{R_{in}[i],\ i=1,\ \ldots,\ n\}$ and $func(R_{out}[i]) \le func(R_{out}[j]), \forall i,j \in [1,..,n], i \le j$.

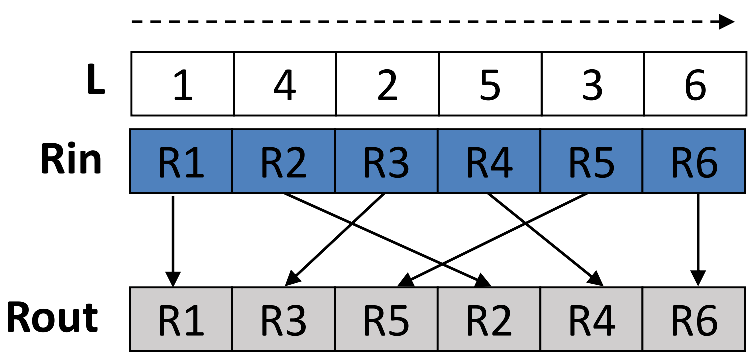
Primitive: Sort
Input: $R_{in}[1, \ldots, n]$.
Output: $R_{out}[1, \ldots, n]$.
Function: $\{R_{out}[i],\ i=1,\ldots,\ n\} = \{R_{in}[i],\ i=1,\ \ldots,\ n\}$ and $R_{out}[i] \le R_{out}[j], \forall i,j \in [1,..,n]$ and $i \le j$.

Scatter and Gather: Overview

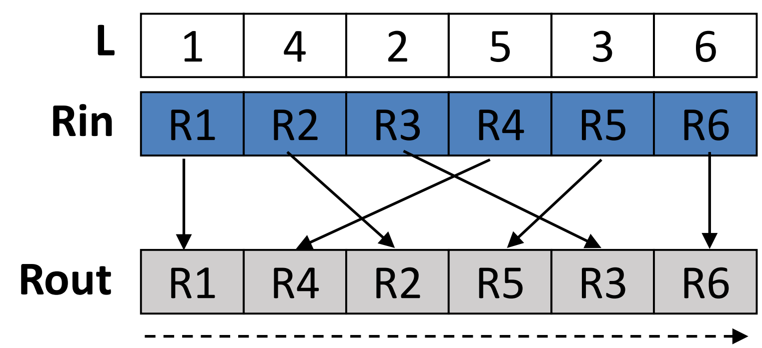
- Widely supported
  - Parallel programming languages, e.g., MPI, NESL, ZPL.
  - Supercomputers, e.g., Cray MTA, Stanford Merrimac
  - Commodity co-processors (IBM Cell, GPUs)
- Irregular access patterns
  - Sparse matrix computations, hashing, searching, etc.
- Performance is memory bandwidth limited
  - Require high bandwidth architectures
  - HPC benchmarks (HPC Challenge, NAS PB, etc.)

Access Patterns

- Scatter: sequential reads and random writes.
- Gather: random reads and sequential writes.



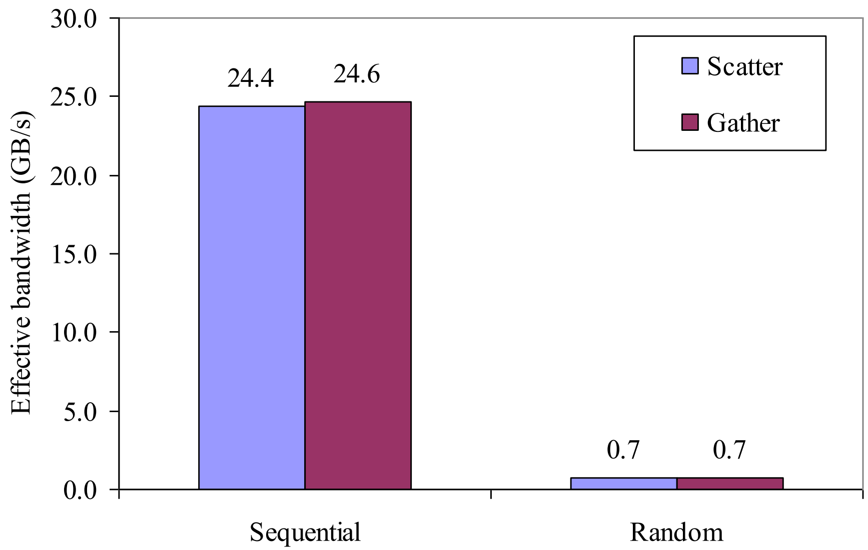
(a) Scatter



(b) Gather

Scatter and Gather on the GPU

- Access pattern makes a 30X difference in performance.



Single-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

Cache

Single-pass Scatter

4 partitions
4 concurrent threads.

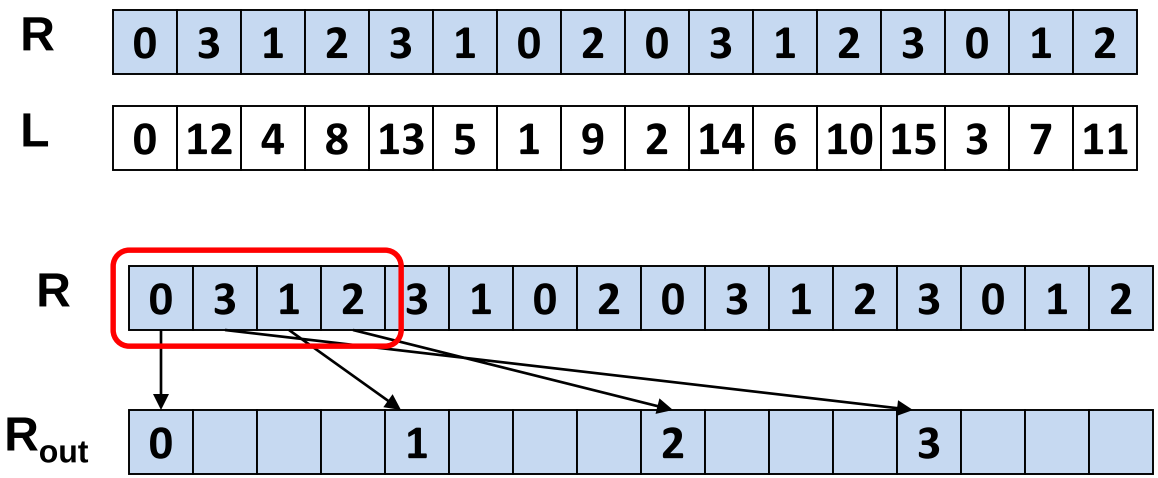
R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

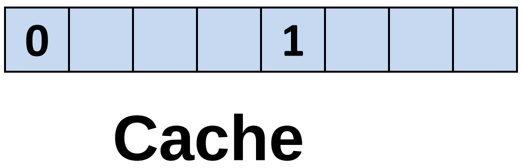
R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}																

Cache

Single-pass Scatter

4 partitions
4 concurrent threads.





Cache Misses = 4
Cache Hits = 0

Single-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

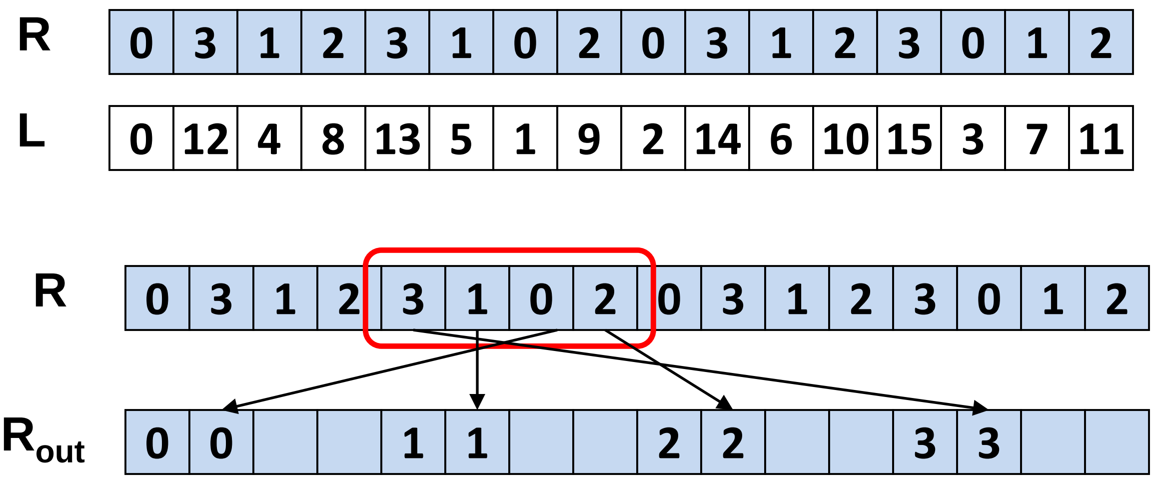
R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0				1				2				3			

0				1			

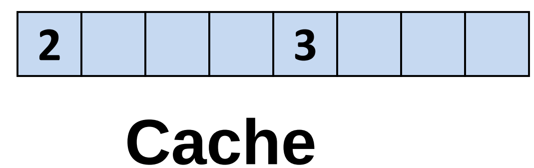
Cache

Cache Misses = 4
Cache Hits = 0

Single-pass Scatter



4 partitions
4 concurrent threads.



Cache Misses = 6
Cache Hits = 2

Single-pass Scatter

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0	0			1	1			2	2			3	3		

2				3			

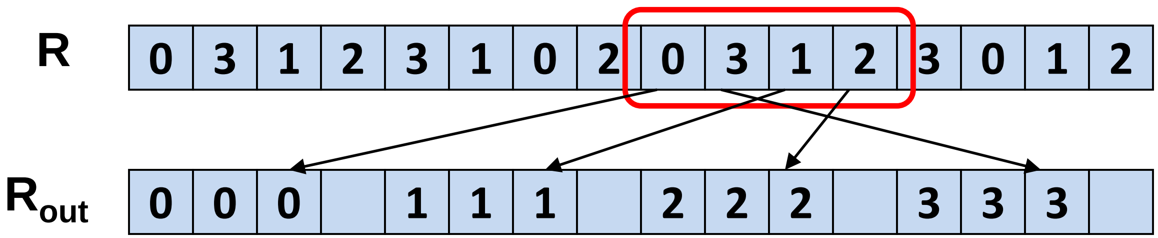
Cache

Cache Misses = 6
Cache Hits = 2

Single-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.



0				3			

Cache

Cache Misses = 8
Cache Hits = 4

Single-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0	0	0		1	1	1		2	2	2		3	3	3	

0				3			

Cache

Cache Misses = 8
Cache Hits = 4

Single-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3

0				3			

Cache

Cache Misses = 10
Cache Hits = 6

Cache miss rate = 62.5%
Effective bandwidth = 0.4 B_{seq}

Multi-pass Scheme

- The entire scatter is performed in multiple passes.
- Each pass writes to a small chunk

Two-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

Cache

Two-pass Scatter

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

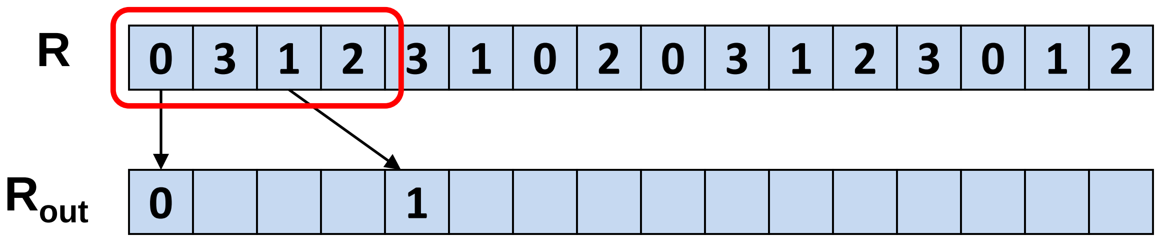
R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}																

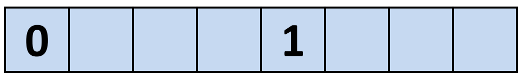
Cache

Two-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.





Cache

Cache Misses = 2
Cache Hits = 0

Two-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

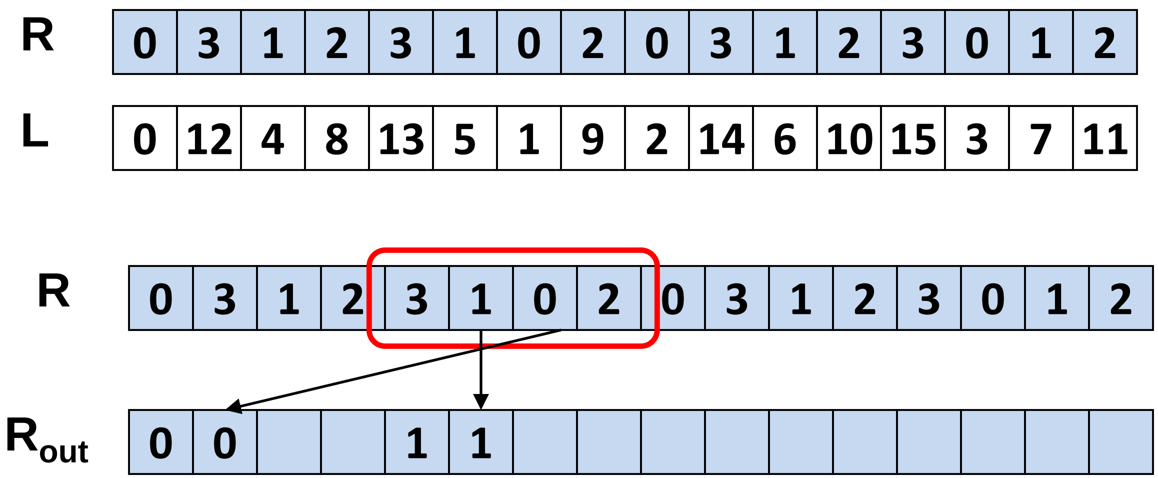
R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0				1											

0				1			

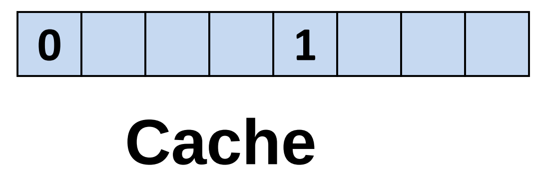
Cache

Cache Misses = 2
Cache Hits = 0

Two-pass Scatter



4 partitions
4 concurrent threads.



Cache Misses = 2
Cache Hits = 2

Two-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0	0			1	1										

0				1			

Cache

Cache Misses = 2
Cache Hits = 2

Two-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0	0	0		1	1	1									

0				1			

Cache

Cache Misses = 2
Cache Hits = 4

Two-pass Scatter

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

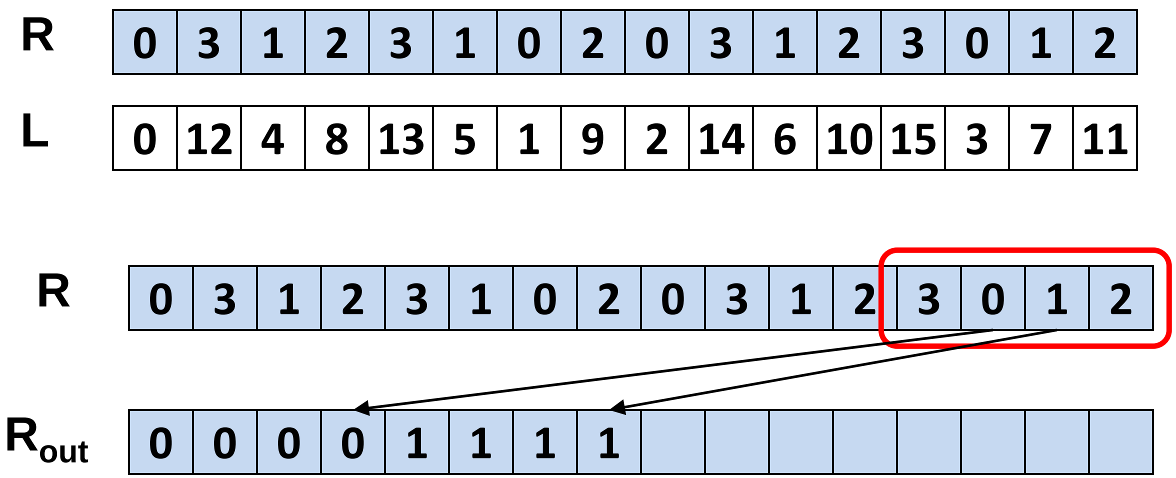
R	0	3	1	2	3	1	0	2	0	3	1	2	$\boxed{3}$	$\boxed{0}$	$\boxed{1}$	$\boxed{2}$
R_{out}	0	0	0		1	1	1									

0				1			

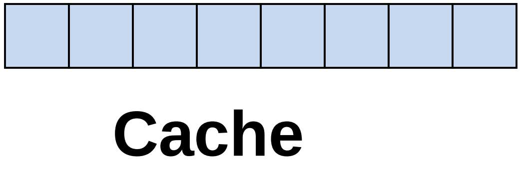
Cache

Cache Misses = 2
Cache Hits = 4

Two-pass Scatter



4 partitions
4 concurrent threads.



Cache Misses = 2
Cache Hits = 6

Two-pass Scatter

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
L	0	12	4	8	13	5	1	9	2	14	6	10	15	3	7	11

4 partitions
4 concurrent threads.

R	0	3	1	2	3	1	0	2	0	3	1	2	3	0	1	2
R_{out}	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3

Cache

Cache Misses = 4
Cache Hits = 12

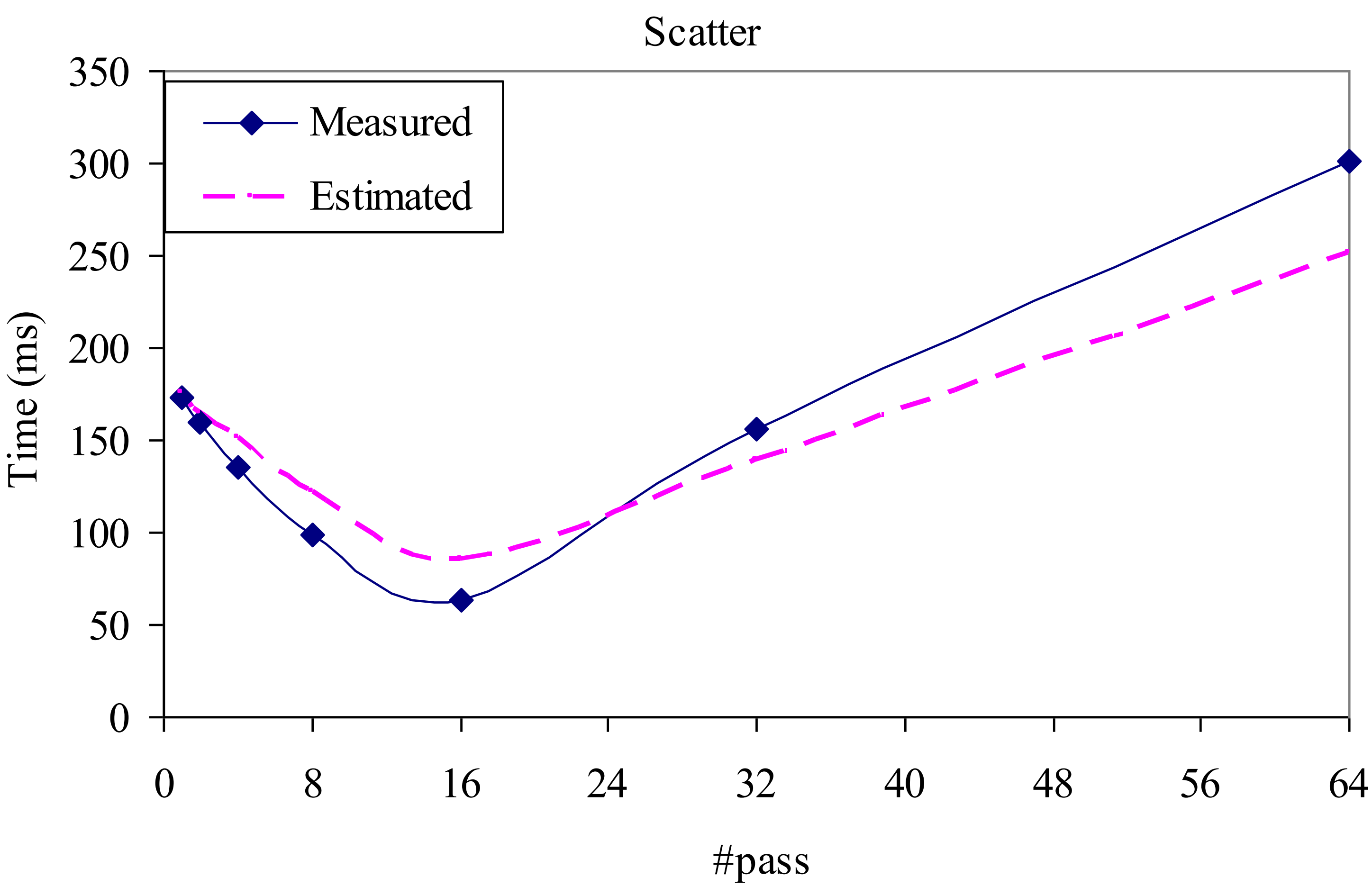
Cache miss rate = 25%
Effective bandwidth = B_{seq}

Cost Model

- Estimate the performance of different access patterns
  – Sequential bandwidth
  – Random bandwidth
- Estimate the total cost of sequential access and random access in the multi-pass scheme.

  $T_{scatter}$= (|R| + |L|) * npasses/B_{seq}+ |R|/B_{rand}
- Determine the optimal number of passes.

Performance Results -- Multi-pass Scatter



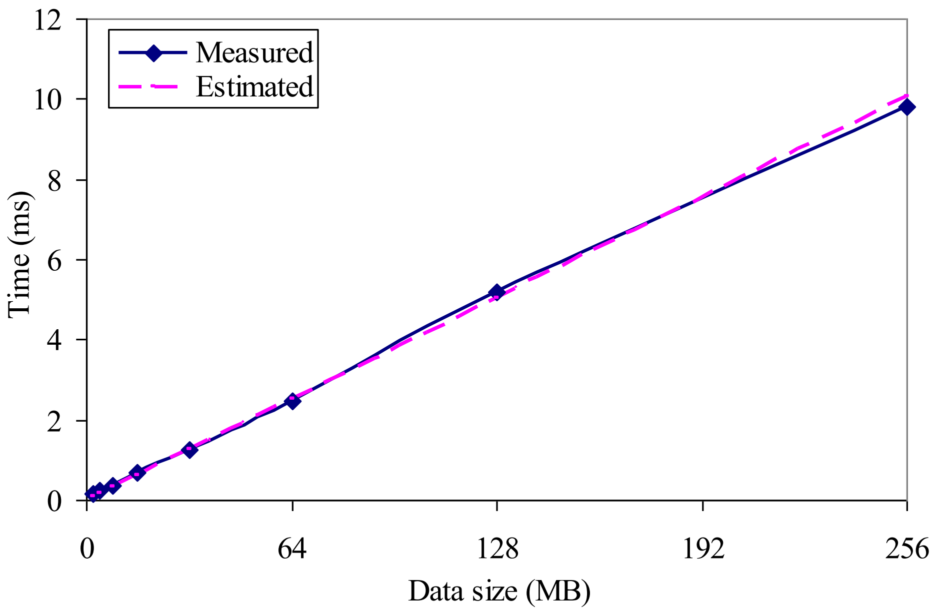
The optimal number of passes is 16.

Applications and Analysis

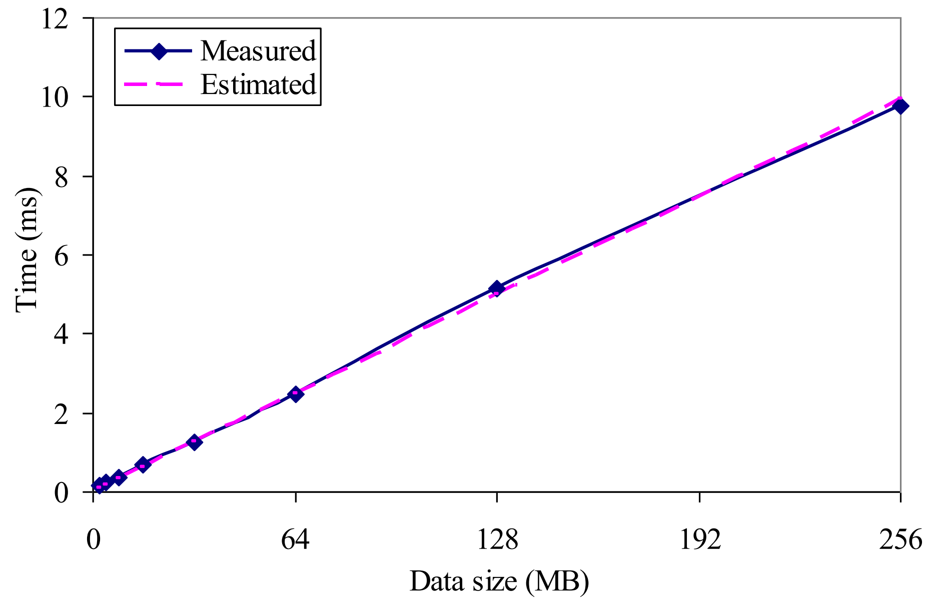
- Applications
  - Radix sort, hash search, and sparse-matrix vector multiplication
- Platforms
  - CPUs: Intel Quad, or two AMD dual-core processors.
  - GPU: Nvidia 8800 GTX.
- Overall results
  - The cost model has an accuracy of over 85%.
  - The multipass scheme improves the application 10%~50%.
  - The GPU-based algorithm outperforms the CPU-based algorithm by 2-7X.

Sequential Scatter/Gather

Scatter



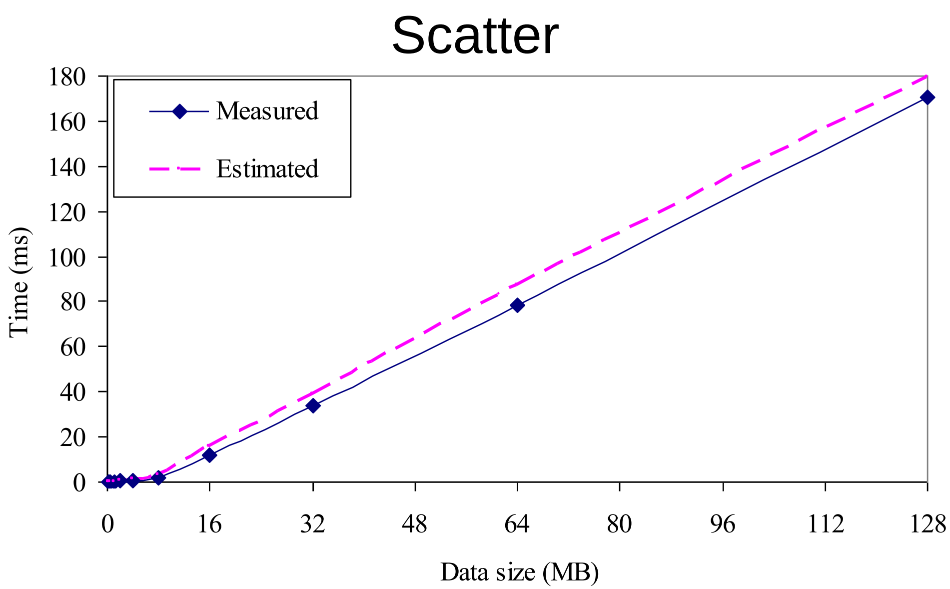
Gather

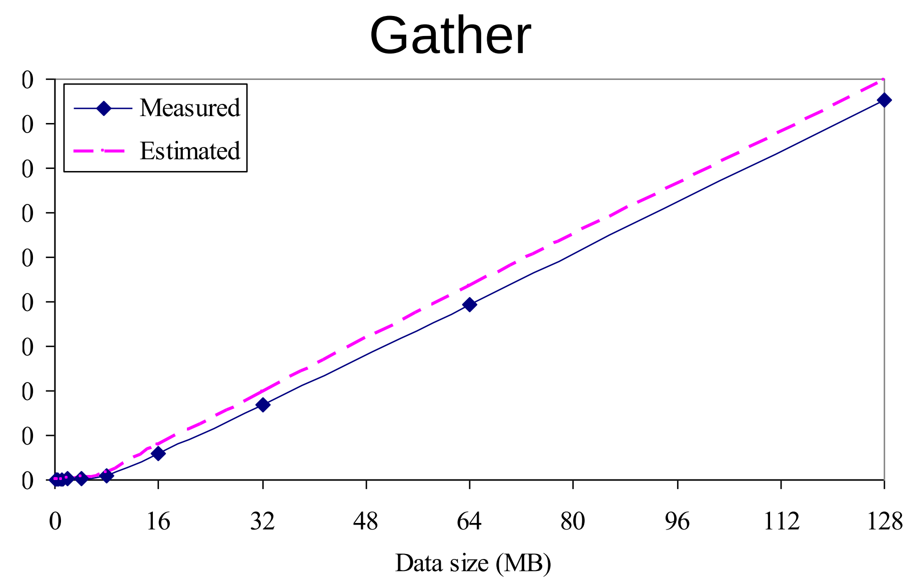


Accuracy of the cost model on the sequential gather and the scatter: 87%

$$\text{Accuracy} = 1 - \frac{|\,Measurement - Estimation\,|}{Measurement}$$

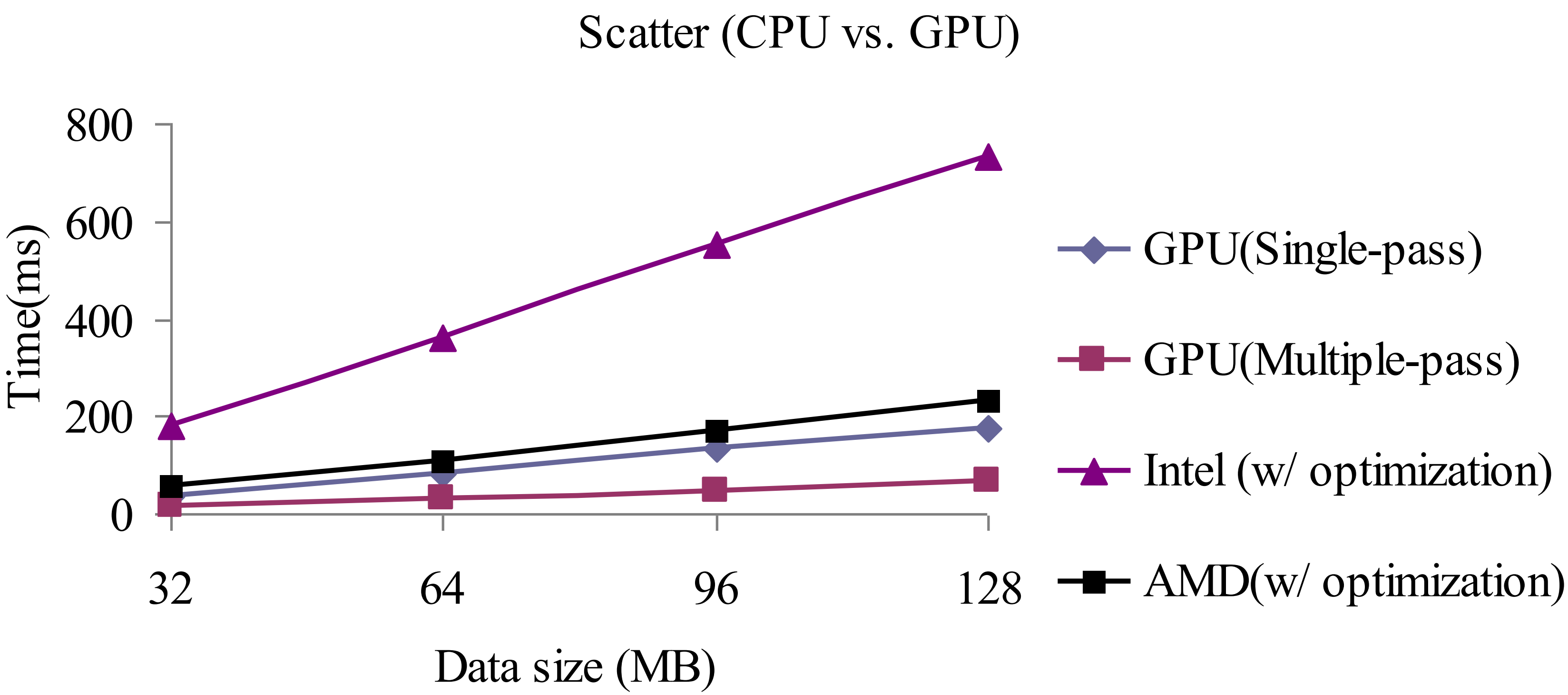
Random Scatter/Gather





Accuracy of the cost model on the random gather and the scatter: 90%.

Performance Impact of Multi-Pass Scatter



(1) The speedup is 7-13X and 2-4X on Intel and AMD, respectively.
(2) The multi-pass scheme improves the GPU-based scatter by 2-4X.

Summary

- Data-parallel primitives are an efficient way of utilizing GPU's parallelism.
- Scatter and gather are memory-bound and can be optimized through multi-pass schemes.

References:

Bingsheng He, Naga K. Govindaraju, Qiong Luo, and Burton Smith. Efficient Gather and Scatter Operations on Graphics Processors. ACM/IEEE SuperComputing (SC), Nov 2007.

http://www.cse.ust.hk/gpuqp