```
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s1200efg320-4

 Number of Slices:                      637  out of   8672     7%
 Number of Slice Flip Flops:            370  out of  17344     2%
 Number of 4 input LUTs:               1169  out of  17344     6%
 Number of IOs:                          63
 Number of bonded IOBs:                  61  out of    250    24%
    IOB Flip Flops:                       1
 Number of GCLKs:                         1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
----------------------------------------------------------------------------------------------------+--
---------------------------------------+-------+
Clock Signal                                                                                        |
Clock buffer(FF name)                  | Load  |
----------------------------------------------------------------------------------------------------+--
---------------------------------------+-------+
clock                                                                                               |
IBUF+BUFG                              | 361   |
arithmetic_logic_unit/results<3>_4_not0000(arithmetic_logic_unit/results<3>_4_not00001:O)|
NONE(*)(arithmetic_logic_unit/flags_3_7)| 10    |
----------------------------------------------------------------------------------------------------+--
---------------------------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST
with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these
buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
-----------------------------------------
-----------------------------------+--------------------------------+-------+
Control Signal                     | Buffer(FF name)                | Load  |
-----------------------------------+--------------------------------+-------+
I_set(control_unit/I_set1:O)       | NONE(status_register/RegOut_7)| 1     |
-----------------------------------+--------------------------------+-------+
```

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 94.509ns (Maximum Frequency: 10.581MHz)
   Minimum input arrival time before clock: 15.503ns
   Maximum output required time after clock: 26.538ns
   Maximum combinational path delay: 11.549ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clock'
  Clock period: 94.509ns (frequency: 10.581MHz)
  Total number of paths / destination ports: 51048354 / 641
-------------------------------------------------------------------------
Delay:               47.255ns (Levels of Logic = 37)
  Source:            instruction_register/IROut_13 (FF)
  Destination:       control_unit/IState_0 (LATCH)
  Source Clock:      clock rising
  Destination Clock: clock falling

  Data Path: instruction_register/IROut_13 to control_unit/IState_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q             27   0.591   1.340  instruction_register/IROut_13
(instruction_register/IROut_13)
     LUT3:I1->O           13   0.704   0.987  control_unit/DOffSelect<0>31
(control_unit/N113)
     LUT4:I3->O           27   0.704   1.296  control_unit/SelB<4>712 (control_unit/N163)
     LUT3:I2->O            6   0.704   0.673  control_unit/SelB<2>84
(control_unit/SelB<2>84)
     LUT4:I3->O           12   0.704   0.996  control_unit/FlagMask_6_mux002411
(control_unit/N154)
     LUT3:I2->O            4   0.704   0.591  control_unit/SelB<0>221 (control_unit/N120)
     LUT4:I3->O            2   0.704   0.451  control_unit/SelB<1>221 (control_unit/N82)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>118
(control_unit/SelB<1>118)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>155
(control_unit/SelB<1>155)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>186
(control_unit/SelB<1>186)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>237_SW0 (N362)
     LUT4:I3->O           64   0.704   1.272  control_unit/SelB<1>237 (SelB<1>)
     MUXF5:S->O            1   0.739   0.000  reg_array/mux8_5_f5 (reg_array/mux8_5_f5)
     MUXF6:I1->O           1   0.521   0.000  reg_array/mux8_4_f6 (reg_array/mux8_4_f6)
     MUXF7:I1->O           1   0.521   0.000  reg_array/mux8_3_f7 (reg_array/mux8_3_f7)
     MUXF8:I1->O           2   0.521   0.451  reg_array/mux8_2_f8 (RegB<0>)
     LUT4:I3->O           21   0.704   1.132  OperandB<0> (OperandB<0>)
     LUT4:I3->O            2   0.704   0.482  arithmetic_logic_unit/tempB_0_mux0002_SW2
(N216)
     LUT3:I2->O            1   0.704   0.455  arithmetic_logic_unit/tempB_0_mux0002
(arithmetic_logic_unit/tempB<0>)
     LUT3:I2->O            2   0.704   0.482
arithmetic_logic_unit/AddSub/Adders[0].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<1>)
     LUT3:I2->O            2   0.704   0.482
arithmetic_logic_unit/AddSub/Adders[1].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<2>)
     LUT3:I2->O            2   0.704   0.482
```