Release 14.7 - xst P.20131013 (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

--> Reading design: AVR_CPU.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "AVR_CPU.prj"
Input Format   : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "AVR_CPU"
Output Format   : NGC
Target Device   : xc3s1200e-4-fg320

---- Source Options
Top Module Name   : AVR_CPU
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Mux Style   : Auto
Decoder Extraction   : YES
Priority Encoder Extraction   : Yes
Shift Register Extraction   : YES
Logical Shifter Extraction   : YES
XOR Collapsing   : YES

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ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 24
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Area
Optimization Effort                : 2
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Compilation                              *
=========================================================================
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/opcodes.vhd" in
Library opcodes.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/iunit.vhd" in Library
work.
Architecture iunit_arch of Entity iunit is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/dunit.vhd" in Library
work.
Architecture dunit_arch of Entity dunit is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/sp.vhd" in Library
work.
Architecture sp_arch of Entity sp is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/reg.vhd" in Library
work.
Architecture reg_arch of Entity reg is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/alu.vhd" in Library
work.
```

```
Architecture dataflow of Entity fulladder is up to date.
Architecture archadder of Entity adder is up to date.
Architecture alu_arch of Entity alu is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/cunit.vhd" in Library
work.
Architecture cunit_arch of Entity cunit is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/sr.vhd" in Library
work.
Architecture sr_arch of Entity sr is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/ir.vhd" in Library
work.
Architecture ir_arch of Entity ir is up to date.
Compiling vhdl file "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/avrcpue.vhd" in
Library work.
Architecture avr_cpu_arch of Entity avr_cpu is up to date.

=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for entity <AVR_CPU> in library <work> (architecture <avr_cpu_arch>).

Analyzing hierarchy for entity <IUNIT> in library <work> (architecture <iunit_arch>).

Analyzing hierarchy for entity <DUNIT> in library <work> (architecture <dunit_arch>).

Analyzing hierarchy for entity <SP> in library <work> (architecture <sp_arch>).

Analyzing hierarchy for entity <REG> in library <work> (architecture <reg_arch>).

Analyzing hierarchy for entity <ALU> in library <work> (architecture <alu_arch>).

Analyzing hierarchy for entity <CUNIT> in library <work> (architecture <cunit_arch>).

Analyzing hierarchy for entity <SR> in library <work> (architecture <sr_arch>).

Analyzing hierarchy for entity <IR> in library <work> (architecture <ir_arch>).

Analyzing hierarchy for entity <Adder> in library <work> (architecture <archadder>) with
generics.
        bitsize = 8

Analyzing hierarchy for entity <FullAdder> in library <work> (architecture <dataflow>).


=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing Entity <AVR_CPU> in library <work> (Architecture <avr_cpu_arch>).
INFO:Xst:1739 - HDL ADVISOR - "C:/Users/Torkom/Dropbox/Caltech/EE
119/HW/B/avr/avrcpue.vhd" line 54: declaration of a buffer port will make it difficult for
you to validate this design by simulation. It is preferable to declare it as output.
INFO:Xst:1739 - HDL ADVISOR - "C:/Users/Torkom/Dropbox/Caltech/EE
119/HW/B/avr/avrcpue.vhd" line 66: declaration of a buffer port will make it difficult for
you to validate this design by simulation. It is preferable to declare it as output.
INFO:Xst:1739 - HDL ADVISOR - "C:/Users/Torkom/Dropbox/Caltech/EE
119/HW/B/avr/avrcpue.vhd" line 42: declaration of a buffer port will make it difficult for
you to validate this design by simulation. It is preferable to declare it as output.
INFO:Xst:1739 - HDL ADVISOR - "C:/Users/Torkom/Dropbox/Caltech/EE
119/HW/B/avr/avrcpue.vhd" line 122: declaration of a buffer port will make it difficult
for you to validate this design by simulation. It is preferable to declare it as output.
INFO:Xst:1739 - HDL ADVISOR - "C:/Users/Torkom/Dropbox/Caltech/EE
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119/HW/B/avr/avrcpue.vhd" line 38: declaration of a buffer port will make it difficult for you to validate this design by simulation. It is preferable to declare it as output.
INFO:Xst:1739 - HDL ADVISOR - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/avrcpue.vhd" line 39: declaration of a buffer port will make it difficult for you to validate this design by simulation. It is preferable to declare it as output.
Entity <AVR_CPU> analyzed. Unit <AVR_CPU> generated.

Analyzing Entity <IUNIT> in library <work> (Architecture <iunit_arch>).
Entity <IUNIT> analyzed. Unit <IUNIT> generated.

Analyzing Entity <DUNIT> in library <work> (Architecture <dunit_arch>).
WARNING:Xst:819 - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/dunit.vhd" line 111: One or more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:
   <ProgDB>
Entity <DUNIT> analyzed. Unit <DUNIT> generated.

Analyzing Entity <SP> in library <work> (Architecture <sp_arch>).
Entity <SP> analyzed. Unit <SP> generated.

Analyzing Entity <REG> in library <work> (Architecture <reg_arch>).
Entity <REG> analyzed. Unit <REG> generated.

Analyzing Entity <ALU> in library <work> (Architecture <alu_arch>).
WARNING:Xst:819 - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/alu.vhd" line 245: One or more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:
   <StatRegIn>
Entity <ALU> analyzed. Unit <ALU> generated.

Analyzing generic Entity <Adder> in library <work> (Architecture <archadder>).
        bitsize = 8
Entity <Adder> analyzed. Unit <Adder> generated.

Analyzing Entity <FullAdder> in library <work> (Architecture <dataflow>).
Entity <FullAdder> analyzed. Unit <FullAdder> generated.

Analyzing Entity <CUNIT> in library <work> (Architecture <cunit_arch>).
WARNING:Xst:819 - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/cunit.vhd" line 227: One or more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:
   <ALU_SR>
WARNING:Xst:819 - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/cunit.vhd" line 1092: One or more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:
   <IState>, <IR>, <IR_en>
WARNING:Xst:819 - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/cunit.vhd" line 1239: One or more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:
   <IR_buf_en>, <ProgDB>
Entity <CUNIT> analyzed. Unit <CUNIT> generated.

```
Analyzing Entity <SR> in library <work> (Architecture <sr_arch>).
WARNING:Xst:819 - "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/sr.vhd" line 44: One or
more signals are missing in the process sensitivity list. To enable synthesis of FPGA/CPLD
hardware, XST will assume that all necessary signals are present in the sensitivity list.
Please note that the result of the synthesis may differ from the initial design
specification. The missing signals are:
   <I_set>
Entity <SR> analyzed. Unit <SR> generated.

Analyzing Entity <IR> in library <work> (Architecture <ir_arch>).
Entity <IR> analyzed. Unit <IR> generated.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <IUNIT>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/iunit.vhd".
WARNING:Xst:647 - Input <IR<15:12>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
    Found 16-bit register for signal <PC>.
    Found 16-bit adder for signal <PC$add0000> created at line 75.
    Found 16-bit 8-to-1 multiplexer for signal <src_mux_out>.
    Summary:
        inferred  16 D-type flip-flop(s).
        inferred   1 Adder/Subtractor(s).
        inferred  16 Multiplexer(s).
Unit <IUNIT> synthesized.


Synthesizing Unit <DUNIT>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/dunit.vhd".
WARNING:Xst:647 - Input <IR<15:14>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <IR<12>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <IR<7:4>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:737 - Found 16-bit latch for signal <IR_delay>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
    Found 16-bit adder for signal <Address>.
    Found 8-bit 4-to-1 multiplexer for signal <DBusOut>.
    Found 16-bit 4-to-1 multiplexer for signal <OSource>.
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred  24 Multiplexer(s).
Unit <DUNIT> synthesized.


Synthesizing Unit <SP>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/sp.vhd".
    Found 16-bit register for signal <SPOut>.
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    Summary:
        inferred  16 D-type flip-flop(s).
Unit <SP> synthesized.


Synthesizing Unit <REG>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/reg.vhd".
    Found 8-bit 32-to-1 multiplexer for signal <RegA>.
    Found 8-bit 32-to-1 multiplexer for signal <RegB>.
    Found 256-bit register for signal <regs>.
INFO:Xst:738 - HDL ADVISOR - 256 flip-flops were inferred for signal <regs>. You may be
trying to describe a RAM in a way that is incompatible with block and distributed RAM
resources available on Xilinx devices, or with a specific template that is not supported.
Please review the Xilinx resources documentation and the XST user manual for coding
guidelines. Taking advantage of RAM resources will lead to improved device usage and
reduced synthesis time.
    Summary:
        inferred 256 D-type flip-flop(s).
        inferred  16 Multiplexer(s).
Unit <REG> synthesized.


Synthesizing Unit <CUNIT>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/cunit.vhd".
WARNING:Xst:647 - Input <ALU_SR<7>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <ALU_SR<5:2>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <ALU_SR<0>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:737 - Found 11-bit latch for signal <IState>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 4-bit latch for signal <count>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 16-bit latch for signal <IR_Buf>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <DataRd>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <DataWr>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
    Using one-hot encoding for signal <count>.
    Using one-hot encoding for signal <IState>.
    Found 1-bit 8-to-1 multiplexer for signal <SR$mux0000> created at line 957.
    Summary:
        inferred   1 Multiplexer(s).
Unit <CUNIT> synthesized.


Synthesizing Unit <SR>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/sr.vhd".
    Found 8-bit register for signal <RegOut>.
    Summary:
        inferred   8 D-type flip-flop(s).
```

```
Unit <SR> synthesized.


Synthesizing Unit <IR>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/ir.vhd".
    Found 16-bit register for signal <IROut>.
    Summary:
        inferred  16 D-type flip-flop(s).
Unit <IR> synthesized.


Synthesizing Unit <FullAdder>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/alu.vhd".
    Found 1-bit xor3 for signal <Sum>.
    Summary:
        inferred   1 Xor(s).
Unit <FullAdder> synthesized.


Synthesizing Unit <Adder>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/alu.vhd".
Unit <Adder> synthesized.


Synthesizing Unit <ALU>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/alu.vhd".
WARNING:Xst:647 - Input <StatRegIn<7>> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <StatRegIn<5:2>> is never used. This port will be preserved and
left unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_4>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead to
setup/hold violations and, as a result, to simulation problems. This situation may come
from an incomplete case statement (all selector values are not covered). You should
carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_5>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead to
setup/hold violations and, as a result, to simulation problems. This situation may come
from an incomplete case statement (all selector values are not covered). You should
carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_6>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead to
setup/hold violations and, as a result, to simulation problems. This situation may come
from an incomplete case statement (all selector values are not covered). You should
carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_7>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead to
```

setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 8-bit latch for signal <flags_3>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_0>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_1>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_2>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <results<3>_3>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.
    Found 8-bit 4-to-1 multiplexer for signal <Result>.
    Found 8-bit 4-to-1 multiplexer for signal <StatRegOut>.
    Found 1-bit 8-to-1 multiplexer for signal <OperandA$mux0000> created at line 308.
    Found 1-bit xor2 for signal <tempB_0$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_0$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_1$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_1$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_2$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_2$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_3$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_3$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_4$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_4$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_5$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_5$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_6$xor0000> created at line 206.
    Found 1-bit xor2 for signal <tempB_6$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempB_7$xor0000> created at line 206.

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    Found 1-bit xor2 for signal <tempB_7$xor0001> created at line 208.
    Found 1-bit xor2 for signal <tempC>.
    Summary:
        inferred  17 Multiplexer(s).
        inferred   1 Xor(s).
Unit <ALU> synthesized.


Synthesizing Unit <AVR_CPU>.
    Related source file is "C:/Users/Torkom/Dropbox/Caltech/EE 119/HW/B/avr/avrcpue.vhd".
WARNING:Xst:647 - Input <INT0> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input <INT1> is never used. This port will be preserved and left
unconnected if it belongs to a top-level block or it belongs to a sub-block and the
hierarchy of this sub-block is preserved.
WARNING:Xst:1780 - Signal <OperandA> is never used or assigned. This unconnected signal
will be trimmed during the optimization process.
    Found 8-bit tristate buffer for signal <DataDB>.
    Found 8-bit 4-to-1 multiplexer for signal <DBBuffer>.
    Summary:
        inferred   8 Multiplexer(s).
        inferred   8 Tristate(s).
Unit <AVR_CPU> synthesized.


=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 2
 16-bit adder                                         : 2
# Registers                                            : 43
 1-bit register                                       : 8
 16-bit register                                      : 3
 8-bit register                                       : 32
# Latches                                              : 15
 1-bit latch                                          : 10
 11-bit latch                                         : 1
 16-bit latch                                         : 2
 4-bit latch                                          : 1
 8-bit latch                                          : 1
# Multiplexers                                         : 10
 1-bit 8-to-1 multiplexer                             : 2
 16-bit 4-to-1 multiplexer                            : 1
 16-bit 8-to-1 multiplexer                            : 1
 8-bit 32-to-1 multiplexer                            : 2
 8-bit 4-to-1 multiplexer                             : 4
# Tristates                                            : 1
 8-bit tristate buffer                                : 1
# Xors                                                 : 31
 1-bit xor2                                           : 22
 1-bit xor3                                           : 9

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================
```

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=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 2
 16-bit adder                                         : 2
# Registers                                            : 312
 Flip-Flops                                           : 312
# Latches                                              : 15
 1-bit latch                                          : 10
 11-bit latch                                         : 1
 16-bit latch                                         : 2
 4-bit latch                                          : 1
 8-bit latch                                          : 1
# Multiplexers                                         : 24
 1-bit 32-to-1 multiplexer                            : 16
 1-bit 8-to-1 multiplexer                             : 2
 16-bit 4-to-1 multiplexer                            : 1
 16-bit 8-to-1 multiplexer                            : 1
 8-bit 4-to-1 multiplexer                             : 4
# Xors                                                 : 31
 1-bit xor2                                           : 22
 1-bit xor3                                           : 9

=========================================================================

=========================================================================
*                          Low Level Synthesis                          *
=========================================================================
INFO:Xst:2261 - The FF/Latch <7> in Unit <LPM_LATCH_18> is equivalent to the following 6
FFs/Latches, which will be removed : <5> <4> <3> <2> <1> <0>
WARNING:Xst:2677 - Node <IState_10> of sequential type is unconnected in block <CUNIT>.

Optimizing unit <AVR_CPU> ...

Optimizing unit <IUNIT> ...

Optimizing unit <SP> ...

Optimizing unit <REG> ...

Optimizing unit <SR> ...

Optimizing unit <IR> ...

Optimizing unit <DUNIT> ...

Optimizing unit <CUNIT> ...

Optimizing unit <Adder> ...

Optimizing unit <ALU> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block AVR_CPU, actual ratio is 7.
Latch control_unit/DataRd has been replicated 1 time(s) to handle iob=true attribute.

Final Macro Processing ...

=========================================================================
```

Final Register Report

Macro Statistics
Registers   : 312
 Flip-Flops   : 312

===

===
*   Partition Report   *
===

Partition Implementation Status

  No Partitions were found in this design.

===
*   Final Report   *
===
Final Results
RTL Top Level Output File Name   : AVR_CPU.ngr
Top Level Output File Name   : AVR_CPU
Output Format   : NGC
Optimization Goal   : Area
Keep Hierarchy   : No

Design Statistics
IOs   : 63

Cell Usage :
BELS   : 1599
GND   : 1
INV   : 1
LUT2   : 56
LUT3   : 591
LUT4   : 521
MULT_AND   : 15
MUXCY   : 30
MUXF5   : 229
MUXF6   : 74
MUXF7   : 32
MUXF8   : 16
VCC   : 1
XORCY   : 32
FlipFlops/Latches   : 371
FDE   : 276
FDPE   : 1
FDRE   : 16
FDS   : 3
FDSE   : 16
LD   : 43
LDE   : 16
Clock Buffers   : 1
BUFG   : 1
IO Buffers   : 61
IBUF   : 19
IOBUF   : 8
OBUF   : 34

```
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s1200efg320-4

 Number of Slices:                      637  out of   8672     7%
 Number of Slice Flip Flops:            370  out of  17344     2%
 Number of 4 input LUTs:               1169  out of  17344     6%
 Number of IOs:                          63
 Number of bonded IOBs:                  61  out of    250    24%
    IOB Flip Flops:                       1
 Number of GCLKs:                         1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
----------------------------------------------------------------------------------------------------+--
---------------------------------------+-------+
Clock Signal                                                                                        |
Clock buffer(FF name)                  | Load  |
----------------------------------------------------------------------------------------------------+--
---------------------------------------+-------+
clock                                                                                               |
IBUF+BUFG                              | 361   |
arithmetic_logic_unit/results<3>_4_not0000(arithmetic_logic_unit/results<3>_4_not00001:O)|
NONE(*)(arithmetic_logic_unit/flags_3_7)| 10    |
----------------------------------------------------------------------------------------------------+--
---------------------------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST
with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these
buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
-----------------------------------------
-----------------------------------+--------------------------------+-------+
Control Signal                     | Buffer(FF name)                | Load  |
-----------------------------------+--------------------------------+-------+
I_set(control_unit/I_set1:O)       | NONE(status_register/RegOut_7)| 1     |
-----------------------------------+--------------------------------+-------+
```

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 94.509ns (Maximum Frequency: 10.581MHz)
   Minimum input arrival time before clock: 15.503ns
   Maximum output required time after clock: 26.538ns
   Maximum combinational path delay: 11.549ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clock'
  Clock period: 94.509ns (frequency: 10.581MHz)
  Total number of paths / destination ports: 51048354 / 641
-------------------------------------------------------------------------
Delay:               47.255ns (Levels of Logic = 37)
  Source:            instruction_register/IROut_13 (FF)
  Destination:       control_unit/IState_0 (LATCH)
  Source Clock:      clock rising
  Destination Clock: clock falling

  Data Path: instruction_register/IROut_13 to control_unit/IState_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q             27   0.591   1.340  instruction_register/IROut_13
(instruction_register/IROut_13)
     LUT3:I1->O           13   0.704   0.987  control_unit/DOffSelect<0>31
(control_unit/N113)
     LUT4:I3->O           27   0.704   1.296  control_unit/SelB<4>712 (control_unit/N163)
     LUT3:I2->O            6   0.704   0.673  control_unit/SelB<2>84
(control_unit/SelB<2>84)
     LUT4:I3->O           12   0.704   0.996  control_unit/FlagMask_6_mux002411
(control_unit/N154)
     LUT3:I2->O            4   0.704   0.591  control_unit/SelB<0>221 (control_unit/N120)
     LUT4:I3->O            2   0.704   0.451  control_unit/SelB<1>221 (control_unit/N82)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>118
(control_unit/SelB<1>118)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>155
(control_unit/SelB<1>155)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>186
(control_unit/SelB<1>186)
     LUT4:I3->O            1   0.704   0.424  control_unit/SelB<1>237_SW0 (N362)
     LUT4:I3->O           64   0.704   1.272  control_unit/SelB<1>237 (SelB<1>)
     MUXF5:S->O            1   0.739   0.000  reg_array/mux8_5_f5 (reg_array/mux8_5_f5)
     MUXF6:I1->O           1   0.521   0.000  reg_array/mux8_4_f6 (reg_array/mux8_4_f6)
     MUXF7:I1->O           1   0.521   0.000  reg_array/mux8_3_f7 (reg_array/mux8_3_f7)
     MUXF8:I1->O           2   0.521   0.451  reg_array/mux8_2_f8 (RegB<0>)
     LUT4:I3->O           21   0.704   1.132  OperandB<0> (OperandB<0>)
     LUT4:I3->O            2   0.704   0.482  arithmetic_logic_unit/tempB_0_mux0002_SW2
(N216)
     LUT3:I2->O            1   0.704   0.455  arithmetic_logic_unit/tempB_0_mux0002
(arithmetic_logic_unit/tempB<0>)
     LUT3:I2->O            2   0.704   0.482
arithmetic_logic_unit/AddSub/Adders[0].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<1>)
     LUT3:I2->O            2   0.704   0.482
arithmetic_logic_unit/AddSub/Adders[1].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<2>)
     LUT3:I2->O            2   0.704   0.482
```

```
arithmetic_logic_unit/AddSub/Adders[2].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<3>)
     LUT3:I2->O            3   0.704   0.566
arithmetic_logic_unit/AddSub/Adders[3].FAx/Cout1 (arithmetic_logic_unit/temp_coh)
     LUT3:I2->O            2   0.704   0.482
arithmetic_logic_unit/AddSub/Adders[4].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<5>)
     LUT3:I2->O            2   0.704   0.451
arithmetic_logic_unit/AddSub/Adders[5].FAx/Cout1 (arithmetic_logic_unit/AddSub/carry<6>)
     LUT4:I3->O            4   0.704   0.622
arithmetic_logic_unit/AddSub/Adders[6].FAx/Cout1 (arithmetic_logic_unit/temp_co6)
     LUT3:I2->O            3   0.704   0.535
arithmetic_logic_unit/AddSub/Adders[7].FAx/Mxor_Sum_xo<0>1
(arithmetic_logic_unit/results<1><7>)
     LUT4:I3->O            1   0.704   0.424  arithmetic_logic_unit/_or0013130
(arithmetic_logic_unit/flags<1><1>)
     LUT4:I3->O            1   0.704   0.000  arithmetic_logic_unit/Mmux_StatRegOut_4
(arithmetic_logic_unit/Mmux_StatRegOut_4)
     MUXF5:I0->O           2   0.321   0.451  arithmetic_logic_unit/Mmux_StatRegOut_2_f5
(StatRegOut<1>)
     LUT4:I3->O            1   0.704   0.424  control_unit/IR_en225_SW0 (N266)
     LUT4:I3->O            1   0.704   0.424  control_unit/IR_en225 (control_unit/IR_en225)
     LUT4:I3->O           23   0.704   1.206  control_unit/IR_en255 (IR_en)
     LUT4:I3->O            5   0.704   0.637  control_unit/IState_mux0017<10>11
(control_unit/N11)
     LUT4:I3->O            4   0.704   0.591  control_unit/IState_mux0017<3>32
(control_unit/N1411)
     LUT4:I3->O            6   0.704   0.673  control_unit/IState_mux0017<10>231
(control_unit/N117)
     LUT4:I3->O            2   0.704   0.451  control_unit/IState_mux0017<10>230
(control_unit/N43)
     LUT4:I3->O            1   0.704   0.000  control_unit/count_mux0017<3>
(control_unit/count_mux0017<3>)
     LD:D                      0.308          control_unit/count_0
    ----------------------------------------
    Total                     47.255ns (26.050ns logic, 21.205ns route)
                                       (55.1% logic, 44.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock
'arithmetic_logic_unit/results<3>_4_not0000'
  Clock period: 3.597ns (frequency: 278.009MHz)
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Delay:               3.597ns (Levels of Logic = 2)
  Source:            arithmetic_logic_unit/flags_3_6 (LATCH)
  Destination:       arithmetic_logic_unit/results<3>_0 (LATCH)
  Source Clock:      arithmetic_logic_unit/results<3>_4_not0000 falling
  Destination Clock: arithmetic_logic_unit/results<3>_4_not0000 falling

  Data Path: arithmetic_logic_unit/flags_3_6 to arithmetic_logic_unit/results<3>_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.676   0.610  arithmetic_logic_unit/flags_3_6
(arithmetic_logic_unit/flags_3_6)
     LUT4:I1->O            1   0.704   0.595  arithmetic_logic_unit/_mux004445_SW1 (N364)
     LUT4:I0->O            1   0.704   0.000  arithmetic_logic_unit/_mux004445
(arithmetic_logic_unit/_mux0044)
     LD:D                      0.308          arithmetic_logic_unit/results<3>_0
    ----------------------------------------
    Total                     3.597ns (2.392ns logic, 1.205ns route)
                                       (66.5% logic, 33.5% route)
```

```
================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'
  Total number of paths / destination ports: 1102 / 382
--------------------------------------------------------------------------------
Offset:              15.503ns (Levels of Logic = 13)
  Source:            ProgDB<2> (PAD)
  Destination:       control_unit/IState_0 (LATCH)
  Destination Clock: clock falling

  Data Path: ProgDB<2> to control_unit/IState_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   1.218   0.808  ProgDB_2_IBUF (ProgDB_2_IBUF)
     LUT4:I0->O            1   0.704   0.000  control_unit/IR_en202 (control_unit/IR_en202)
     MUXF5:I0->O           1   0.321   0.455  control_unit/IR_en20_f5 (control_unit/IR_en20)
     LUT4:I2->O            1   0.704   0.595  control_unit/IR_en46_SW0 (N296)
     LUT4:I0->O            1   0.704   0.000  control_unit/IR_en189_SW01
(control_unit/IR_en189_SW0)
     MUXF5:I1->O           1   0.321   0.424  control_unit/IR_en189_SW0_f5 (N264)
     LUT4:I3->O            1   0.704   0.455  control_unit/IR_en189 (control_unit/IR_en189)
     LUT4:I2->O           23   0.704   1.206  control_unit/IR_en255 (IR_en)
     LUT4:I3->O            5   0.704   0.637  control_unit/IState_mux0017<10>11
(control_unit/N11)
     LUT4:I3->O            4   0.704   0.591  control_unit/IState_mux0017<3>32
(control_unit/N1411)
     LUT4:I3->O            6   0.704   0.673  control_unit/IState_mux0017<10>231
(control_unit/N117)
     LUT4:I3->O            2   0.704   0.451  control_unit/IState_mux0017<10>230
(control_unit/N43)
     LUT4:I3->O            1   0.704   0.000  control_unit/count_mux0017<3>
(control_unit/count_mux0017<3>)
     LD:D                      0.308          control_unit/count_0
    ----------------------------------------
    Total                     15.503ns (9.208ns logic, 6.295ns route)
                                       (59.4% logic, 40.6% route)

================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'
  Total number of paths / destination ports: 310851 / 42
--------------------------------------------------------------------------------
Offset:              26.538ns (Levels of Logic = 20)
  Source:            instruction_register/IROut_13 (FF)
  Destination:       ProgAB<15> (PAD)
  Source Clock:      clock rising

  Data Path: instruction_register/IROut_13 to ProgAB<15>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q             27   0.591   1.340  instruction_register/IROut_13
(instruction_register/IROut_13)
     LUT3:I1->O           13   0.704   0.987  control_unit/DOffSelect<0>31
(control_unit/N113)
     LUT4:I3->O           27   0.704   1.296  control_unit/SelB<4>712 (control_unit/N163)
     LUT3:I2->O            6   0.704   0.704  control_unit/SelB<2>84
(control_unit/SelB<2>84)
     LUT4:I2->O            8   0.704   0.932  control_unit/IR_en_and00031
(control_unit/IR_en_and0003)
     LUT2:I0->O            2   0.704   0.622  control_unit/SelPC_mux0013<1>111
```

```
(control_unit/N811)
     LUT4:I0->O            1   0.704   0.420  control_unit/SelPC<1>68_SW0_SW0 (N386)
     MUXF5:S->O            1   0.739   0.499  control_unit/SelPC<1>68_f5
(control_unit/SelPC<1>68)
     LUT4:I1->O            1   0.704   0.455  control_unit/SelPC<1>121_SW0 (N326)
     LUT3:I2->O           31   0.704   1.297  control_unit/SelPC<1>121 (SelPC<1>)
     LUT4:I2->O            1   0.704   0.499  instruction_unit/Mmux_src_mux_out122_SW2
(N258)
     LUT4:I1->O            6   0.704   0.844  instruction_unit/Mmux_src_mux_out122
(instruction_unit/N11)
     LUT3:I0->O            1   0.704   0.499  instruction_unit/Mmux_src_mux_out834
(instruction_unit/src_mux_out<11>)
     LUT3:I1->O            1   0.704   0.000  instruction_unit/Madd_PC_add0000_lut<11>
(instruction_unit/Madd_PC_add0000_lut<11>)
     MUXCY:S->O            1   0.464   0.000  instruction_unit/Madd_PC_add0000_cy<11>
(instruction_unit/Madd_PC_add0000_cy<11>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<12>
(instruction_unit/Madd_PC_add0000_cy<12>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<13>
(instruction_unit/Madd_PC_add0000_cy<13>)
     MUXCY:CI->O           0   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<14>
(instruction_unit/Madd_PC_add0000_cy<14>)
     XORCY:CI->O           2   0.804   0.526  instruction_unit/Madd_PC_add0000_xor<15>
(instruction_unit/PC_add0000<15>)
     LUT2:I1->O            1   0.704   0.420  instruction_unit/ProgAB<15>1 (ProgAB_15_OBUF)
     OBUF:I->O                 3.272          ProgAB_15_OBUF (ProgAB<15>)
    ----------------------------------------
    Total                     26.538ns (15.199ns logic, 11.339ns route)
                                       (57.3% logic, 42.7% route)

==========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 161 / 25
--------------------------------------------------------------------------
Delay:               11.549ns (Levels of Logic = 23)
  Source:            DataDB<0> (PAD)
  Destination:       ProgAB<15> (PAD)

  Data Path: DataDB<0> to ProgAB<15>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IOBUF:IO->O           3   1.218   0.566  DataDB_0_IOBUF (N171)
     LUT3:I2->O            1   0.704   0.000  instruction_unit/Mmux_src_mux_out_5
(instruction_unit/Mmux_src_mux_out_5)
     MUXF5:I0->O           1   0.321   0.000  instruction_unit/Mmux_src_mux_out_3_f5
(instruction_unit/Mmux_src_mux_out_3_f5)
     MUXF6:I1->O           1   0.521   0.499  instruction_unit/Mmux_src_mux_out_2_f6
(instruction_unit/src_mux_out<0>1)
     LUT3:I1->O            1   0.704   0.000  instruction_unit/Madd_PC_add0000_lut<0>
(instruction_unit/Madd_PC_add0000_lut<0>)
     MUXCY:S->O            1   0.464   0.000  instruction_unit/Madd_PC_add0000_cy<0>
(instruction_unit/Madd_PC_add0000_cy<0>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<1>
(instruction_unit/Madd_PC_add0000_cy<1>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<2>
(instruction_unit/Madd_PC_add0000_cy<2>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<3>
(instruction_unit/Madd_PC_add0000_cy<3>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<4>
(instruction_unit/Madd_PC_add0000_cy<4>)
```

```
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<5>
(instruction_unit/Madd_PC_add0000_cy<5>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<6>
(instruction_unit/Madd_PC_add0000_cy<6>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<7>
(instruction_unit/Madd_PC_add0000_cy<7>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<8>
(instruction_unit/Madd_PC_add0000_cy<8>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<9>
(instruction_unit/Madd_PC_add0000_cy<9>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<10>
(instruction_unit/Madd_PC_add0000_cy<10>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<11>
(instruction_unit/Madd_PC_add0000_cy<11>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<12>
(instruction_unit/Madd_PC_add0000_cy<12>)
     MUXCY:CI->O           1   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<13>
(instruction_unit/Madd_PC_add0000_cy<13>)
     MUXCY:CI->O           0   0.059   0.000  instruction_unit/Madd_PC_add0000_cy<14>
(instruction_unit/Madd_PC_add0000_cy<14>)
     XORCY:CI->O           2   0.804   0.526  instruction_unit/Madd_PC_add0000_xor<15>
(instruction_unit/PC_add0000<15>)
     LUT2:I1->O            1   0.704   0.420  instruction_unit/ProgAB<15>1 (ProgAB_15_OBUF)
     OBUF:I->O                 3.272          ProgAB_15_OBUF (ProgAB<15>)
    ----------------------------------------
    Total                      11.549ns (9.538ns logic, 2.011ns route)
                                       (82.6% logic, 17.4% route)

=========================================================================


Total REAL time to Xst completion: 46.00 secs
Total CPU time to Xst completion: 46.16 secs

-->

Total memory usage is 333804 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   34 (   0 filtered)
Number of infos    :   18 (   0 filtered)
```