**VERMA, HK (HARE KRISHNA)**

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**EXPERIENCE HIGHLIGHTS**

1. 20+ years of experience with excellent breadth in the areas of software engineering including large software development, engineering management and processor/FPGA design knowledge
2. Lead with hands-on experience to bring efficient data center heterogeneous solutions in the application areas of big data, data analytics and machine learning for hyper scale customers optimizing for best utilizations of CPU, memory, networking and storage
3. Developed accelerated Postgres database for Amazon F1 cloud
4. Excellent at developing, analyzing and fixing system, processor and accelerator architecture issues
5. Good knowledge of Big Data Analytics and ML algorithm and tools like Spark
6. Hold 36 issued US patents, more pending. Presented tutorials and papers at conferences.
7. Presented solutions to key hyperscale customers for successful technology adoptions
8. Co-founded Velogix in Bay Area, a next generation floating point accelerator solution company, successfully raised capital from top-tier VCs, delivered successful software and silicon as Chief Architect and VP
9. Defined and led micro-architecture for Intel Xeon-D Server integrating network on processor die
10. Bachelor in Technology in Electrical Engineering from Indian Institute of Technology, Madras; Master in Computer Engineering from University of California at Santa Barbara

**WORK EXPERIENCE**

Jun 2016 – current Xilinx Inc, San Jose

1. *Software Role : Distinguished Engineer, Data Center Group*

Lead for heterogeneous computing data-center software solution for big data analytics, predictive analytics and machine learning applications. Developed SQL accelerated postgres data base and Spark SQL/ML applications. Accelerated modules include hash-join, regular expression, machine learning algorithms such as K-Means. Technical lead for multiple hyper-scale customers successfully enabling accelerator solutions.

Apr 2011 – Jun 2015 Intel India, Bangalore

1. *Processor arch Role : Silicon Architecture, Xeon Server Group, Intel India, Bangalore*

Led Intel micro-architecture and validation for Xeon-D integrating Ethernet with CPU.

March 2007- Mar 2011 Director, IDT, San Jose

1. *Software, IC design Role :Director,Electronic Design*

Joined IDT with Velogix core team to deliver on a programmable application specific standard part solution. Led a team distributed between San Jose and India for successful software release with complex algorithms and silicon delivery.

Oct 2002-Feb 2007 Co-founder Velogix Inc (Formerly Flexlogics), Santa Clara CA, USA

1. *Architecture , Software Role: VP Engg, Chief Architect and Board Observer*

Co-founded and raised $19 million from top-tier VCs for a next generation high performance programmable floating point accelerator. Grew from 2 co-founders to 38+ member team. Designed software tools target designs onto this complex device along with the architecture.

Dec 1993-September 2002 Staff Software Engineer Xilinx Inc, San Jose, CA, USA

1. *Xilinx Synthesis Tool (XST) Development Role: Lead Engineer*

Write C++ based hardware synthesizer for DSP/telecom application

1. *Developed LogiBLOX toolkit Role: Developer*

Specification, development, and delivery of the LogiBLOX toolkit in C++

**EDUCATION**

Sept 1992-Dec 1993 University of California, Santa Barbara, USA

Master of Science in Computer Engineering

July 1988-May 1992 Indian Institute of Technology, Madras, India

Bachelor of Technology in Electrical and Electronics Engineering

**PATENTS, PUBLICATIONS**

1. US 9812180, “Programmable logic accelerator in system on chip”
2. US 7358765, 7836113 & 7414431, “Dedicated Logic Cells Employing Configurable Logic and Dedicated Logic Functions”
3. US 7368941, 7439768, 7417456, 7414431 & 7414432, “Dedicated Logic Cells Employing Sequential Logic and Control Logic Functions”
4. US 8612503, “Methods and apparatuses for flexible and high performance digital signal processing”
5. US 8131909, “System and method of signal processing engines with programmable logic fabric”
6. US 8429214, “Programmable logic systems and methods employing configurable floating point units”
7. US 7970979, “System and method of configurable bus-based dedicated connection circuits”
8. US 6980025 & 7417455, “Programmable function generator and method operating as combinational, sequential, and routing cells”
9. US 7605605 & 7728623, “Programmable Logic Cells with Local Connections”
10. US 7800404, “Field Programmable Application Specific Integrated Circuits”
11. US 7814136, “Programmable logic systems and methods employing configurable floating point units”
12. US 6980029, “Programmable Integrated Circuit Architecture”
13. US 8572151, “Method and apparatuses for cordic processing”
14. US 8085603, “Method and apparatus for compression of configuration bitstream of field programmable logic”
15. US 7111220, “Network physical layer with multi-standard CRC generator”
16. US 7176717, “Programmable logic and routing blocks with dedicated lines”
17. US 7187709, “High Speed Configurable Transceiver Architecture”
18. US 6021423, “A method for parallel-efficient configuring an FPGA for Large FFTs and other Vector Rotation Computations”
19. US 6617877 & 6960933, "Variable Data Width Operation in Multi-Gigabit Transceivers on a Programmable Logic Device".
20. US 7428722 & 7358761, “Versatile Multiplexer-Structures in Programmable Logic Using Serial Chaining and Novel Selection Schemes”
21. US 6711600, 6507860, 6317768 & 6167416, “System and Method for RAM partitioning to exploit parallelism of radix-2 elements in FPGAs”
22. US 6911842, "Low Jitter Clock for a Physical Media Access Sublayer on a Field Programmable Gate Array"
23. “Adding FPGA-based Acceleration to Flash Memory for Real-Time Analytics”, FMS San Jose 2018
24. “Accelerating Data Analytics Using FPGAs and an Integrated Flash Storage ”, Flash Memory Storage Conference, San Jose 2017
25. “Advanced validation methodology for a complex nanometer silicon processor”, half day tutorial at VDAT, 2013
26. “A 180 GFLOP/s, 15 GFLOP/W, 500 million transistor FPGA in 90nm CMOS”, FPGA Conference Monterey, 2006
27. “VLSI Signal Processing in FPGAs,” a full day tutorial at the IEEE International Conference on VLSI, Jan 7-10, 1999 in Goa, India