**Low-Power Scan Testing for Test Data Compression Using a Routing-Driven Scan Architecture,** Dong Xiang, IEEE, JULY 2009

An integrated-circuits testing method called scan testing is useful, but it generates two side-effects—prohibitive test power and test data volume. Meanwhile, routing overhead is another important issue on scan testing. Though many researches are proposed to improve scan testing including clock disabling, transition blocking, capture test power reduction and scan flip-flop ordering, the results are dismal. Xiang et al. proposed a two-stage scan architecture which can effectively reduce average test power, but not peak test power and capture test power. Now, a new routing-aware scan architecture evolved from two-stage scan architecture is introduced to solve the problems mentioned above. Meanwhile, two routing-driven schemes are proposed to reduce the routing overhead for routing-aware scan architecture.

