

1. Description

1.1. Project

Project Name	Cube_PWM_TO_DAC
Board Name	custom
Generated with:	STM32CubeMX 6.13.0
Date	12/19/2024

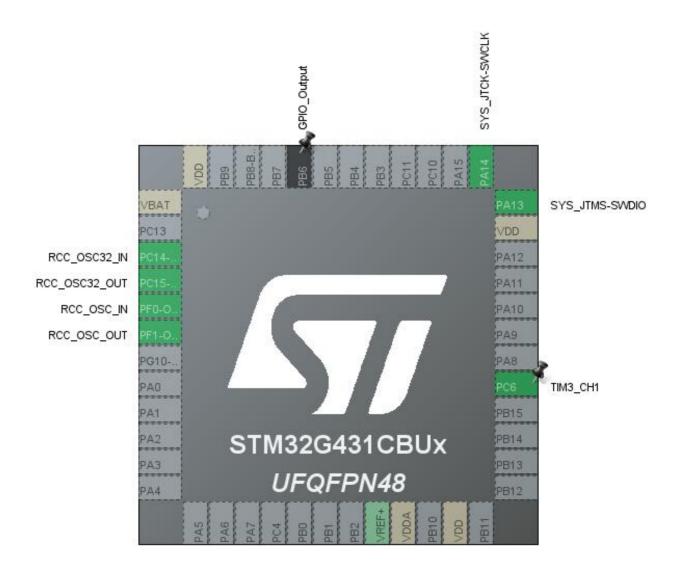
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G431CBUx
MCU Package	UFQFPN48
MCU Pin number	48

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration

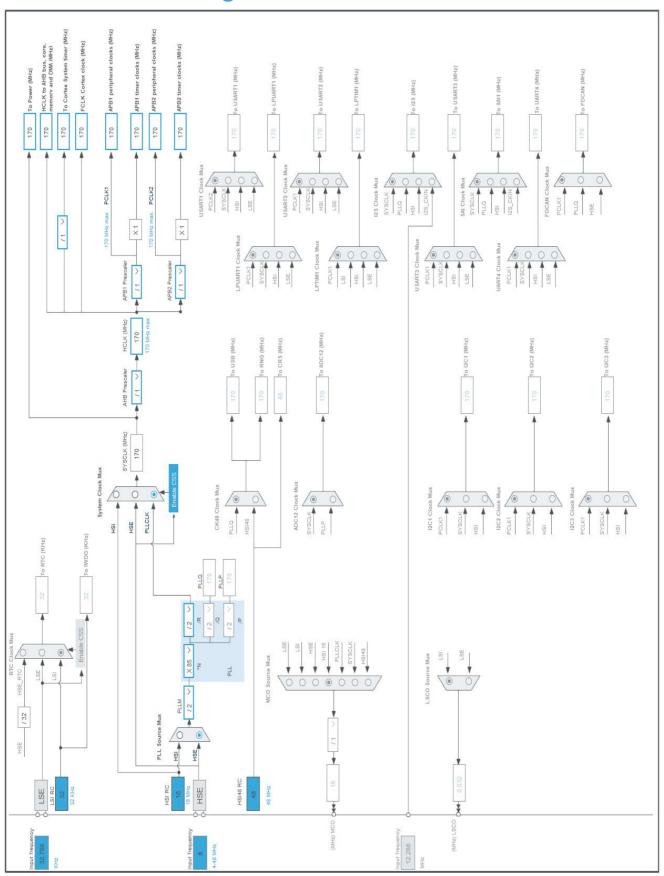


3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
21	VDDA	Power		
23	VDD	Power		
29	PC6	I/O	TIM3_CH1	
35	VDD	Power		
36	PA13	I/O	SYS_JTMS-SWDIO	
37	PA14	I/O	SYS_JTCK-SWCLK	
44	PB6 *	I/O	GPIO_Output	
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
мси	STM32G431CBUx
Datasheet	DS12589_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

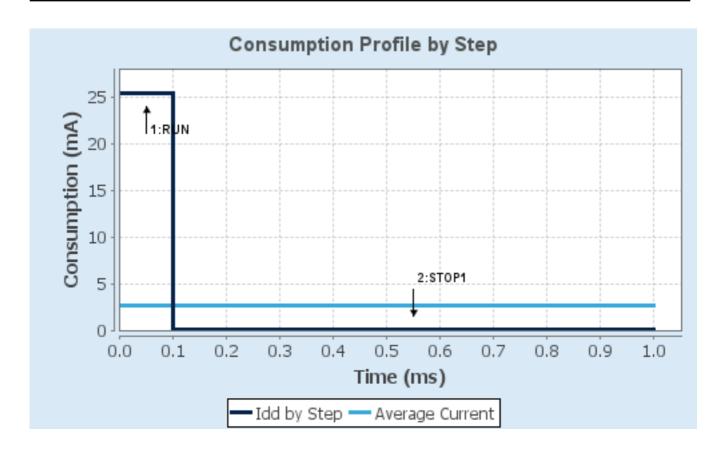
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	25.5 mA	59 μA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	127.71	129.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.6 mA
Battery Life	1 month, 23 days,	Average DMIPS	212.5 DMIPS
	22 hours		

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	Cube_PWM_TO_DAC
Project Folder	C:\fw\stm32\stm32g431\Cube_PWM_TO_DAC
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.6.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM4_Init	TIM4
5	MX_TIM3_Init	TIM3

3. Peripherals and Middlewares Configuration

3.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

3.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value (64
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration TRUE

3.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

3.3. TIM3

Clock Source: Internal Clock
Channel1: PWM Generation CH1

3.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Dithering Disable

Counter Period (AutoReload Register - 16 bits value) 1024-1 *

Internal Clock Division (CKD) No Division

auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

3.4. TIM4

Clock Source : Internal Clock

Channel1: Output Compare No Output

3.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Dithering Disable

Counter Period (AutoReload Register - 16 bits value) 100 *

Internal Clock Division (CKD) No Division auto-reload preload Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

Output Compare No Output Channel 1:

Mode Frozen (used for Timing base)

Pulse (16 bits value) 0

Output compare preload Disable
CH Polarity High

Cube_	_PWM_	_TO_	_DAC	Proje	Cl
	Cor	nfiqu	ration	Repo	ort

* User modified value						

4. System Configuration

4.1. GPIO configuration

IP Pin Signal		GPIO mode GPIO pull/up pull down		Max Speed	User Label	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	SYS PA13 SYS_JTMS- SWDIO		n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO PB6 GPIO_Output C		Output Push Pull	Pull-up *	Low		

4.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM4_CH1	DMA1_Channel1	Memory To Peripheral	High *

TIM4_CH1: DMA1_Channel1 DMA request Settings:

Mode: Circular *
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word *
Memory Data Width: Word *

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
DMA1 channel1 global interrupt	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused			
Flash global interrupt		unused		
RCC global interrupt	unused			
TIM3 global interrupt	unused			
TIM4 global interrupt	unused			
FPU global interrupt	unused			

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler	
Non maskable interrupt	false	true	false	
Hard fault interrupt	false	true	false	
Memory management fault	false	true	false	
Prefetch fault, memory access fault	false	true	false	
Undefined instruction or illegal state	false	true	false	
System service call via SWI instruction	false	true	false	
Debug monitor	false	true	false	
Pendable request for system service	false	true	false	
System tick timer	false	true	true	
DMA1 channel1 global interrupt	false	true	true	

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

	Middleware							
	System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Utilities
	System core	Allalog	Timers	connectivity	Multimoun	Security	computing	oundes
	DMA 🤡		TIM3 🤡					
\succ								
	GPIO ❷		TIM4 ♥					
\succ								
	NVIC ♥							
\succ								
	RCC ❷							
\geq								
	sys 🤡)						
		,						

6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32g4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip

System View https://www.st.com/resource/en/svd/stm32g4_svd.zip

Description

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