Summary of Hand Calculations

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
W/L $\left[\frac{\mu m}{\mu m}\right]$	12.63	12.63	5	5	11.04	50.25	55.461	5.52
g_m **[V/A]**	0.201m	0.201m	0.2m	0.2m	0.266m	2.01m	1.336m	0.133m
V_{ov} **[V]**	0.1989	0.1989	0.2	0.2	0.301	0.2	0.301	0.301

	Q9	Q10	Q11	Q12	Q13
W/L $\left[\frac{\mu m}{\mu m}\right]$	5.52	2.211	2.211	8.844	2.211
g_m **[V/A]**	0.133m	0.133m	0.133m	0.266m	0.133m
V_{ov} **[V]**	0.301	0.301	0.301	0.15	0.301

The design chooses $L = 1\mu m$ *for all devices*

r_{o2}	$500k\Omega$	r_{o6}	$100k\Omega$
r_{o4}	$1M\Omega$	r_{o7}	$50k\Omega$
$R_1 = r_{o2}\|\|r_{o4}$	$333.33k\Omega$	$R_2 = r_{o6}\|\|r_{o7}$	$33.33k\Omega$

$G_{m1} = g_{m1} = g_{m2}$ **[V/A]**	0.201m	
$G_{m2} = g_{m6}$ **[V/A]**	2.01m	
$A_v = G_{m1}G_{m2}R_1R_2$ **[V/V]**	4489	73dB
CMRR	6700	76.52dB
PSSR	13467	82.5dB`
f_{P1} **(kHz)**	1.8	
f_{P2} **(MHz)**	64	
f_t **(MHz)**	8	
f_z **(MHz)**	80	
Phase Margin (deg)	77	
Slew Rate (V/us)	10	

AC Sweep Frequency Response

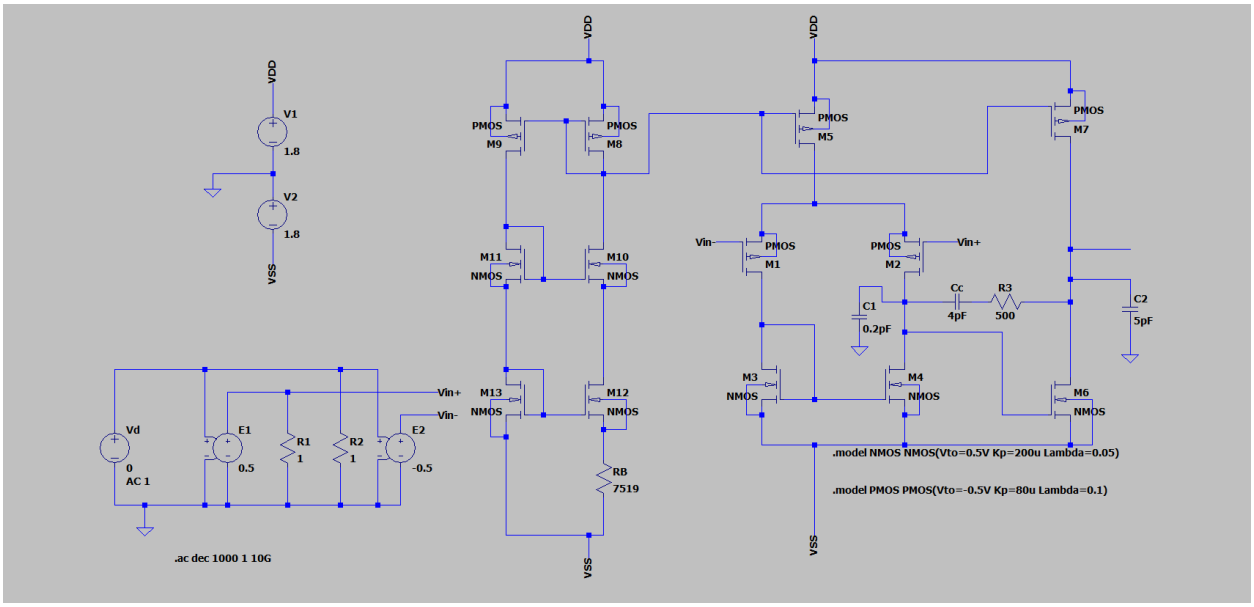

Figure 1: Two stage CMOS operational amplifier with current mirror bias circuit. Differential input circuit is shown and used for AC sweep. Aspect ration of devices are asigned according to values presented in Hand Caculation summary. Note that by selecting $R_3 = \frac{1}{G_{m2}} = 500\Omega$ in series with C_C, we place the transmission zero at infinite frequency. Therefore, we expect $f_z \rightarrow \infty$ in our AC sweep simulation.

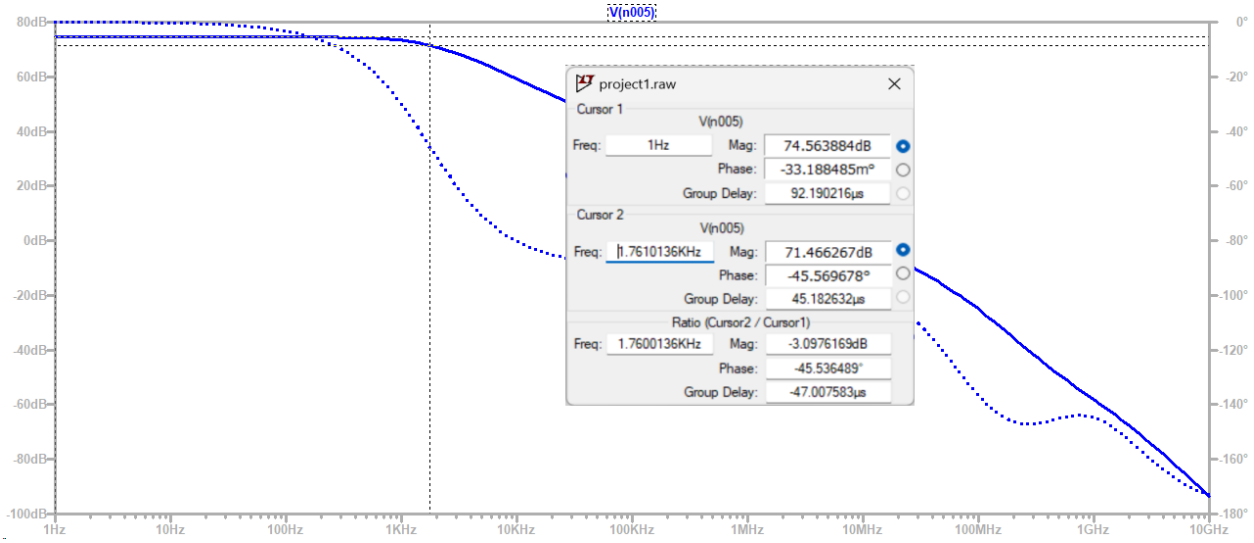

Figure 2: 3-dB frequency f_{P1} is simulated to be $1.76 \approx 1.8kHz$ which matches the hand calculation results. The maximum gain is measured to be $74.56dB \approx 5345\ V/V$ which satisfies the requirements of $A_v > 4000\ V/V$

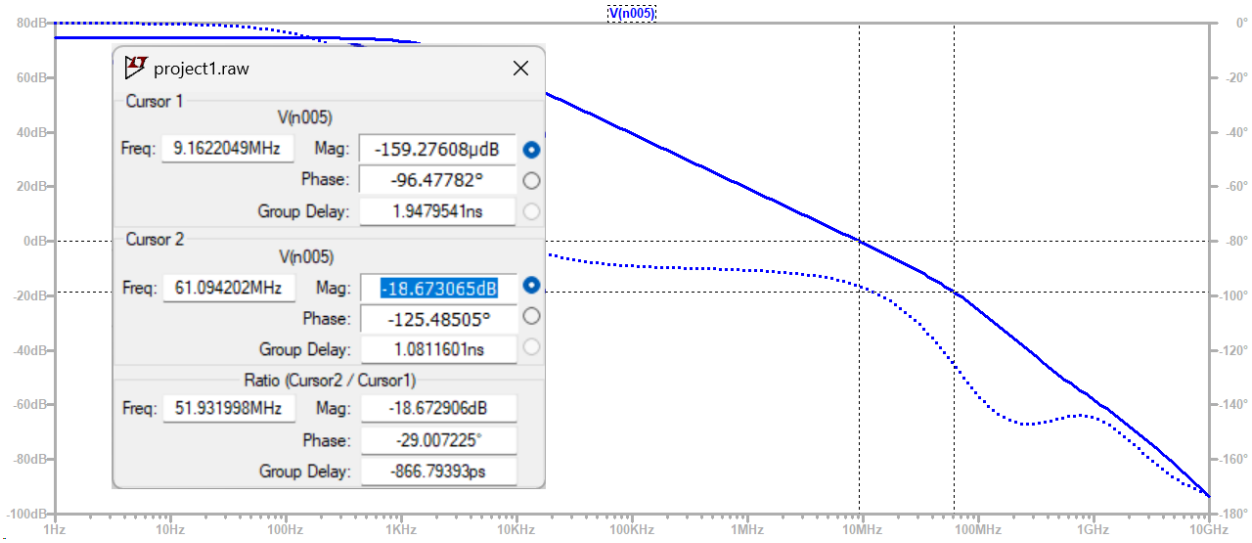

Figure 3: Unity gain frequency f_t is simulated to be $9.2MHz$ while the hand calculation starts with the assumption of $8MHz$. Also shown above is $f_{P2} = 61MHz$ which matches closely the $64MHz$ in hand calculation. The transmission zero is moved to infinity due to R_3 and therefore can not be observed on the plot.

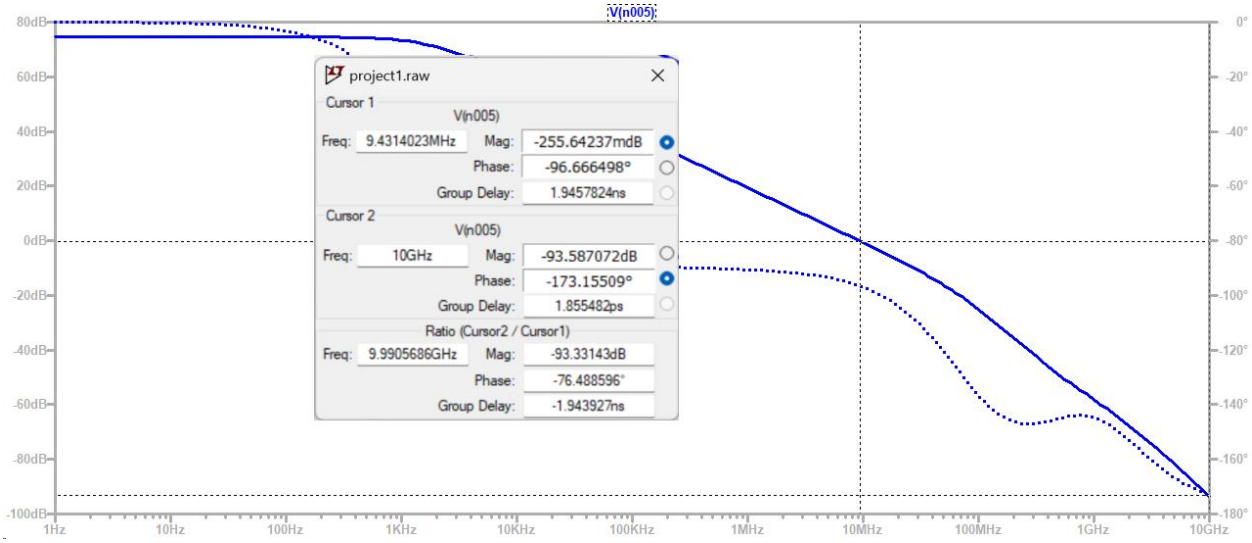

Figure 4: Phase margin is measured to be $76.49°$ which matches the $77°$ from hand calculation result.

Input Common Mode Range and Output Swing

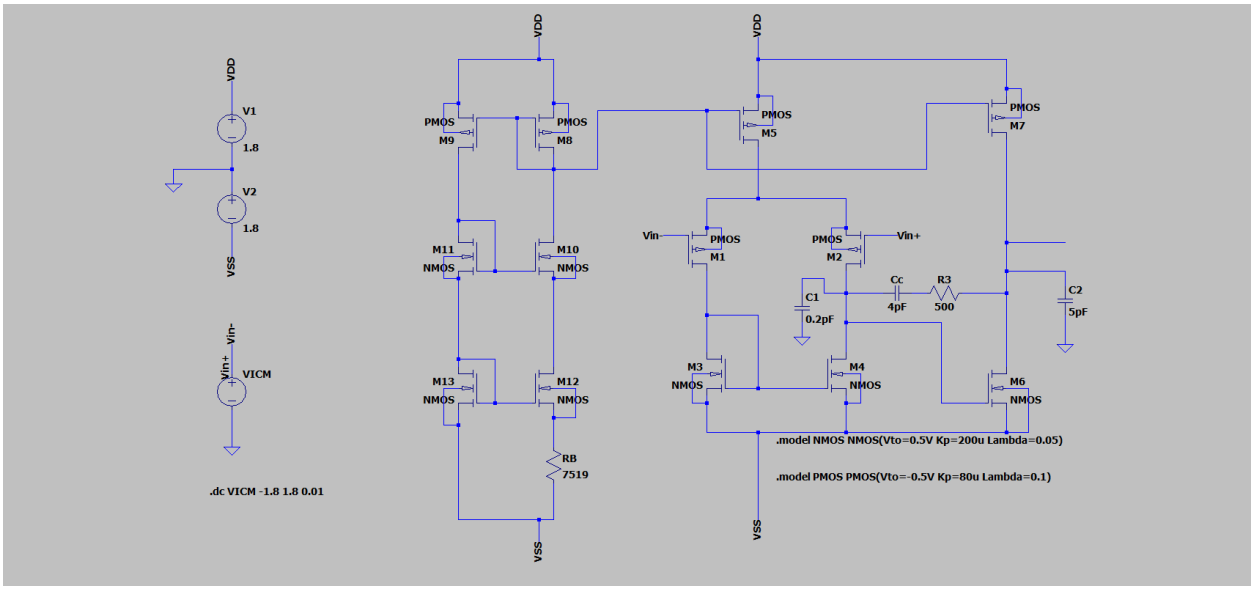

Figure 5: Both differential inputs are tied to the same DC voltage source

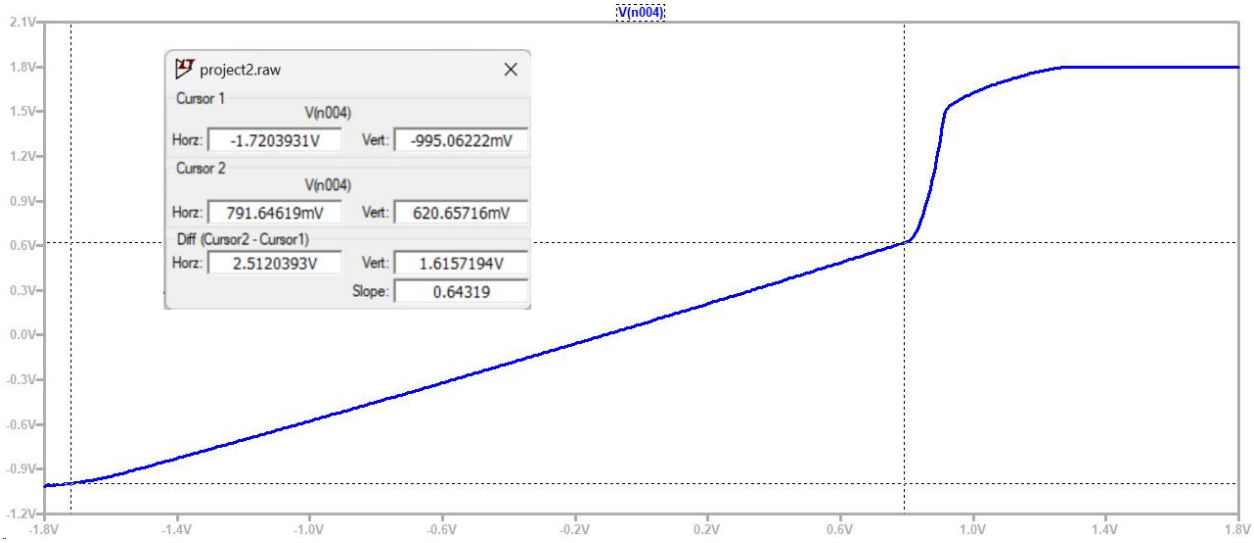

Figure 6: The linear segments is between the dc input voltage of $-1.72V$ to $0.792V$ which satisfy the requirement of $-1.6V \leq V_{ICM} \leq +0.8V$. The overlapping output range for such V_{ICM} is measured on the vertical axis to be $-1V \leq V_o \leq 0.6V$. Since our design allow$-1.5V \leq V_o \leq 1.5V$, the overlapping is substantial. The designed op amp allows output terminal to be connected back to its negative input terminal so that a unity-gain amplifer is obtained.

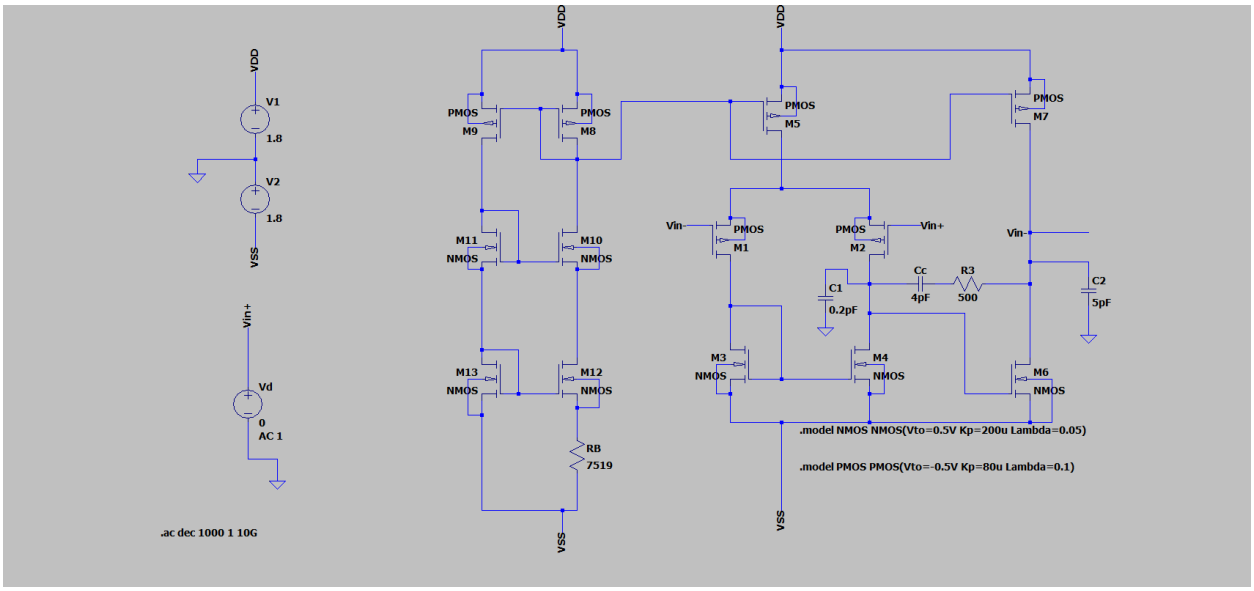

Figure 7: Unity gain amplifer: Output is conencted to negative input terminal.

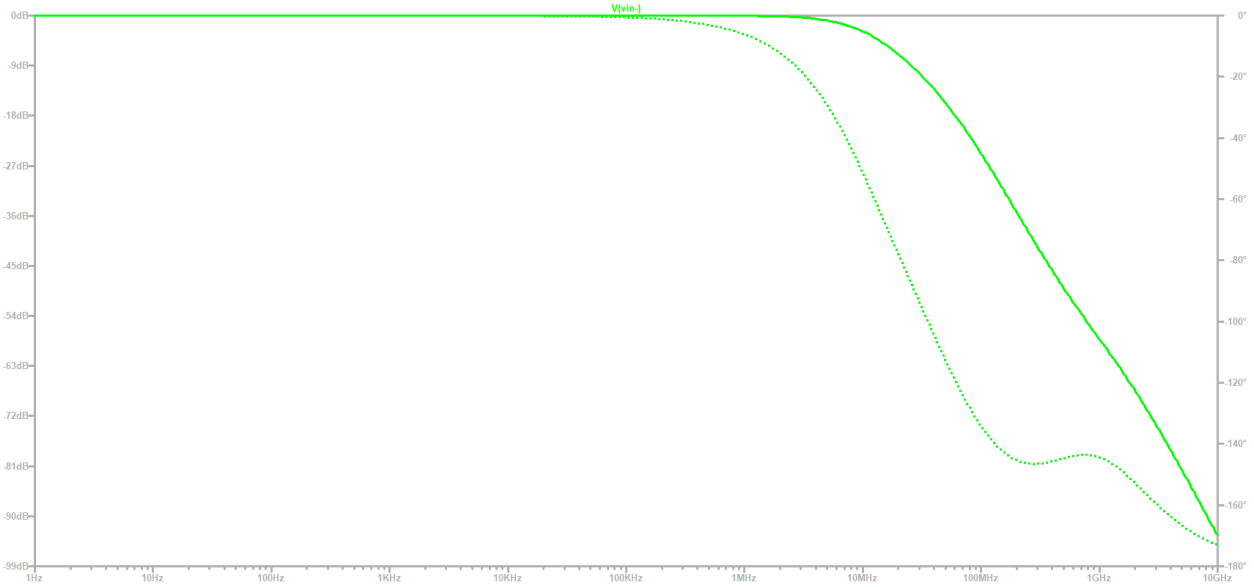

Figure 8: Corresponding unity gain frequency response

Slew Rate

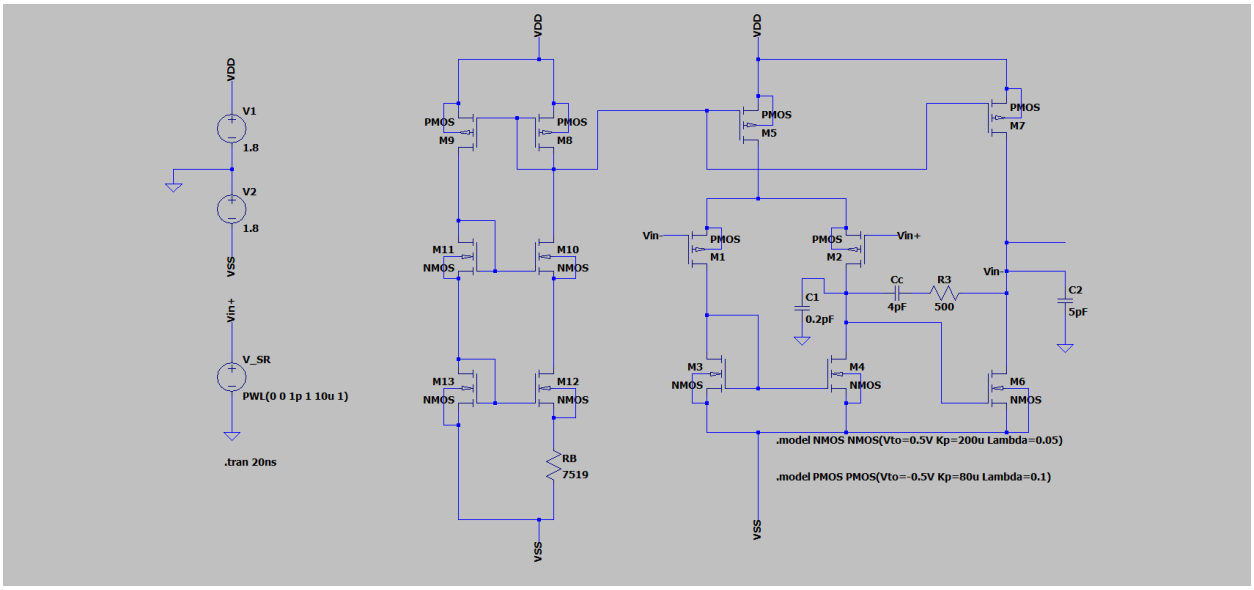

Figure 7: To measure Slew Rate, a pulse is fed into Vin+. The negative differential input Vin- is connected to Vout.

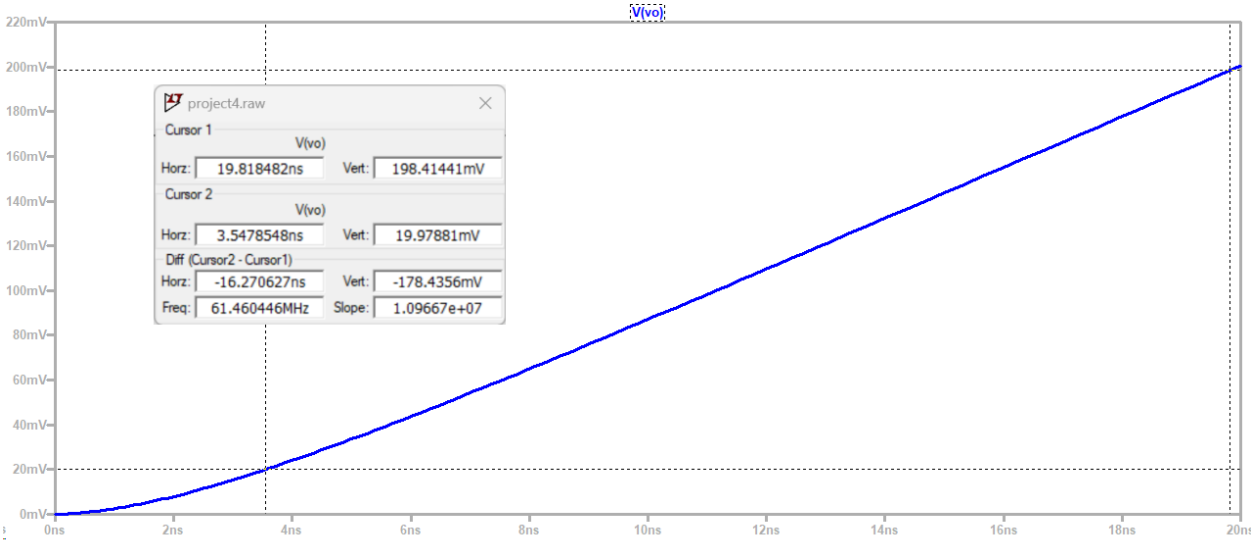

Figure 8: Slew rate is the slope of the linear segment, and measured to be $1.10 \times 10^{-7} = 11V/\mu s$, which satifies the requirement of $SR \geq 10V/\mu s$

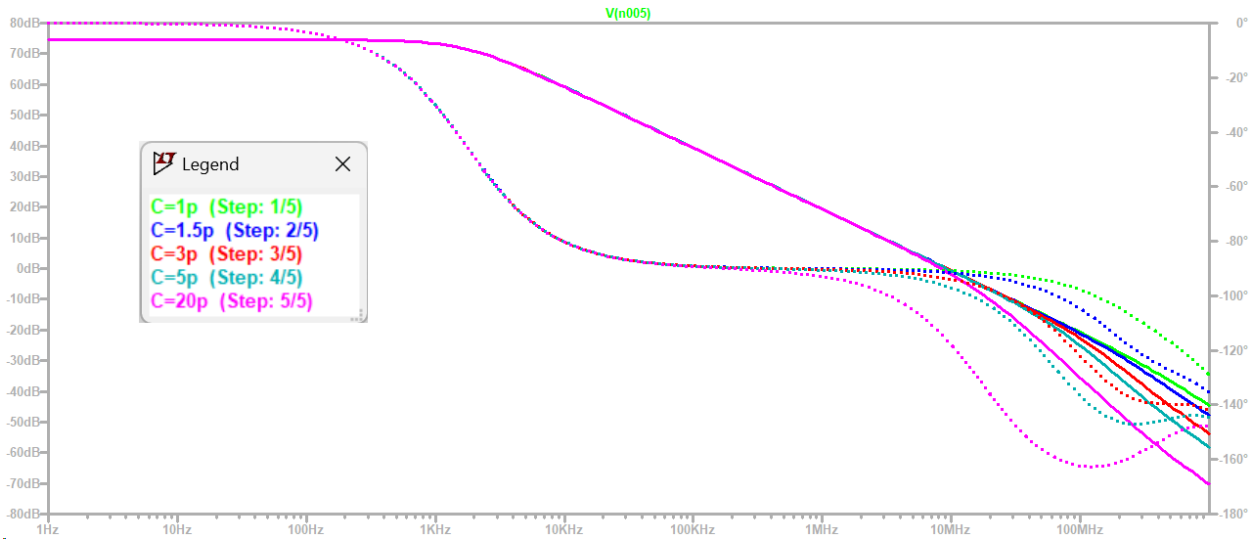

Figure 9: Frequency responses at various C_2 values. In this project, C_2 is assumed to be $5pF$.