Heiner Litz

Curriculum Vitae

January 2025

Address: Department of Computer Engineering
1156 High St, Santa Cruz, CA 95064
Email: heiner.litz@gmail.com
WWW: https://people.ucsc.edu/~hlitz/

Overview

I am an Associate Professor at the University of California Santa Cruz and hold the Kumar Malavalli Endowed Chair of Storage Systems Research. I serve as the Director of the Center for Research in Systems and Storage (CRSS). My research spans computer architecture, storage, and systems to design next-generation microprocessors for scale-out data centers. My current interests revolve around redesigning the processor frontend (Icache, BTB, branch prediction) and the memory system, enabling efficient execution of warehouse-scale computing workloads. I am building full-stack prototypes, including applications, firmware, FPGAs, and ASICs. I have contributed to the Linux kernel. I am currently advising 8 Ph.D. students, and my research is supported by grants totaling $9.1M from NSF, Samsung, Google, Facebook, Intel, Meta, Nutanix, and ARM.

Work Experience

2024	Visiting Professor at the Massachusetts Institute of Technology (MIT), Cambridge
2024-	Kumar Malavalli Endowed Professor for Storage Systems Research, UCSC
2023-	Associate Professor at the University of California, Santa Cruz
2023-	Director of the Center for Research in Systems and Storage at UCSC, Santa Cruz
2022-	Consulting Performance Exploration Engineer, ARM
2018-2023	Assistant Professor at the University of California, Santa Cruz
2018-2020	Consulting Researcher at Google, Mountain View
2017	Visiting Faculty at Google, Mountain View
2015-2016	Lecturer and Postdoctoral Researcher, Stanford University, with Prof. C. Kozyrakis
2012-2015	Postdoctoral Researcher, Stanford University, with Prof. D. Cheriton
2008	Hardware Engineering Intern, SUN Microsystems
2006-2012	Research Assistant, University of Heidelberg and Mannheim University

Education

2015	Postdoc in Electrical Engineering, Stanford University *Advisor*: David Cheriton and Christos Kozyrakis
2011	PhD. in Computer Engineering, Mannheim University *Advisor*: Professor Ulrich Bruening
2010	Visiting Researcher, University of Valencia *Advisor*: Professor Jose Duato
2006	Diplom Informatik (M.Sc), Mannheim University

Honors and Awards

- IEEE MICRO Top Pick 2023 Award
- Best Paper Award, MICRO'22
- Intel Outstanding Researcher Award '21
- NSF CAREER Award
- Google Faculty Award
- Facebook Faculty Award
- IEEE MICRO Top Pick 2019 Award
- Memorable Paper Award, NVMW'17
- Dissertation with honors, Summa Cum Laude

Publications

Refereed Conference Papers

1. Liu, Y., M. Xie, S. Shi, Y. Xu, H. Litz, and C. Qian (2025). Outback: Fast and Communication-efficient Index for Key-Value Store on Disaggregated Memory. In: *Proceedings of the 51st International Conference on Very Large Data Bases (VLDB)*.
2. Zhu, K., Y. Zhao, Y. Gao, P. Braun, T. A. Khan, H. Litz, B. Kasikci, and S. Deng (2025). From Optimal to Practical: Efficient Micro-op Cache Replacement Policies for Data Center Applications. In: *Proceedings of the International Symposium on Computer Architecture (HPCA)*.
3. Chakraborty, J., M. Dorier, P. Carns, R. Ross, C. Maltzahn, and H. Litz (2024). Thallus: An RDMA-based Columnar Data Transport Protocol. In: *Proceedings of the 2nd Workshop on Hot Topics in System Infrastructure (HotInfra)*.
4. Oh, S., M. Xu, T. A. Khan, B. Kasikci, and **Litz, Heiner** (2024). UDP: Utility-Driven Fetch Directed Instruction Prefetching. In: *51st International Symposium on Computer Architecture (ISCA)*. ISCA.
5. Xie, M., C. Qian, and H. Litz (2024). En4S: Enabling SLOs in Serverless Storage Systems. In: *Proceedings of the Symposium on Cloud Computing (SoCC)*.
6. Zhang, Y., N. Sobotka, S. Park, S. Jamilan, T. A. Khan, B. Kasikci, G. A. Pokam, **Litz, Heiner**, and J. Devietti (2024). RPG 2: Robust Profile-Guided Runtime Prefetch Generation. In: *27th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'24)*.
7. Jaliminche, L. N., C. N. Chakraborttii, C. Choi, and **Litz, Heiner** (2023). Enabling Multi-tenancy on SSDs with Accurate IO Interference Modeling. In: *2023 ACM Symposium on Cloud Computing (SoCC'23)*.
8. Liu, Y., S. Shi, M. Xie, **Litz, Heiner**, and C. Qian (2023). Smash: Flexible, Fast, and Resource-efficient Placement and Lookup of Distributed Storage. *ACM on Measurement and Analysis of Computing Systems (SIGMETRICS)*.
9. Ni, Y., P. Mehra, E. Miller, and **Litz, Heiner** (2023). TMC: Near-Optimal Resource Allocation for Tiered-Memory Systems. In: *2023 ACM Symposium on Cloud Computing (SoCC'23)*.
10. Zhang, Y., T. A. Khan, G. Pokam, B. Kasikci, **Litz, Heiner**, and J. Devietti (2023). Online COde Layout OptimizationS via OCOLOS. *IEEE Micro Top Pick*.
11. Jamilan, S., T. A. Khan, G. Ayers, B. Kasikci, and **Heiner Litz** (2022). APT-GET: profile-guided *timely* software prefetching. In: *EuroSys '22: Seventeenth European Conference on Computer Systems (Eurosys'22)*.
12. Khan, T. A., M. Ugur, K. Nathella, D. Sunwoo, **Litz, Heiner**, D. Jiménez, and B. Kasikci (2022). Whisper: Profile-Guided Branch Misprediction Elimination for Data Center Applications. In: *55nd Annual International Symposium on Microarchitecture (MICRO'22)*.
13. **Litz, Heiner**, G. Ayers, and P. Ranganathan (2022). CRISP: Critical Slice Prefetching. In: *Twenty-Seventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'22)*.
14. Song, S., T. A. Khan, S. Mahdizadeh-Shahri, A. Sriraman, N. K. Soundararajan, S. Subramoney, D. A. Jiménez, **Heiner Litz**, and B. Kasikci (2022). Thermometer: profile-guided btb replacement for data center applications. In: *ISCA '22: The 49th Annual International Symposium on Computer Architecture (ISCA'22)*.
15. Yuxuan, Z., T. A. Khan, G. Pokam, B. Kasikci, **Litz, Heiner**, and J. Devietti (2022). OCOLOS: Online COde Layout OptimizationS. In: *55nd Annual International Symposium on Microarchitecture (MICRO'22)*.
16. Chakraborttii, C. and **Litz, Heiner** (2021). Reducing write amplification in flash by death-time prediction of logical block addresses. In: *14th ACM International Conference on Systems and Storage (SYSTOR)*.

17. Kargar, S., **Litz, Heiner**, and F. Nawab (2021). Predict and Write: Using K-Means Clustering to Extend the Lifetime of NVM Storage. In: *37th IEEE International Conference on Data Engineering (ICDE)*.
18. Khan, T. A., D. Zhang, A. Sriraman, J. Devietti, G. Pokam, **Litz, Heiner**, and B. Kasikci (2021). Ripple: Profile-Guided Instruction Cache Replacement for Data Center Applications. In: *48th International Symposium on Computer Architecture (ISCA'21)*.
19. Ayers, G., **Litz, Heiner**, C. Kozyrakis, and P. Ranganathan (2020). Classifying Memory Access Patterns for Prefetching. In: *Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'20)*.
20. Chakraborttii, C. and **Litz, Heiner** (2020a). Improving the accuracy, adaptability, and interpretability of SSD failure prediction models. In: *11th ACM Symposium on Cloud Computing (SoCC)*.
21. Chakraborttii, C. and **Litz, Heiner** (2020b). Learning I/O Access Patterns to Improve Prefetching in SSDs. In: *European Conference on Machine Learning (ECML-PKDD'20)*.
22. Khan, T. A., A. Sriraman, J. Devietti, G. Pokam, **Litz, Heiner**, and B. Kasikci (2020). I-SPY: Context-Driven Conditional Instruction Prefetching with Coalescing. In: *53nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'20)*.
23. Ayers, G., N. P. Nagendra, D. I. August, H. K. Cho, S. Kanev, C. Kozyrakis, T. Krishnamurthy, **Litz, Heiner**, T. Moseley, and P. Ranganathan (2019). AsmDB: understanding and mitigating front-end stalls in warehouse-scale computers. In: *46th International Symposium on Computer Architecture (ISCA'19)*.
24. Ni, Y., J. Zhao, **Litz, Heiner**, D. Bittman, and E. L. Miller (2019). SSP: Eliminating Redundant Writes in Failure-Atomic NVRAMs via Shadow Sub-Paging. In: *52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'19)*.
25. Grossman, S., **Litz, Heiner**, and C. Kozyrakis (2018). Making pull-based graph processing performant. In: *23rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*.
26. Hashemi, M., K. Swersky, J. Smith, G. Ayers, **Litz, Heiner**, J. Chang, C. Kozyrakis, and P. Ranganathan (2018). Learning Memory Access Patterns. In: *35th International Conference on Machine Learning (ICML)*.
27. Klimovic, A., **Litz, Heiner**, and C. Kozyrakis (2018b). Selecta: Learning Heterogeneous Cloud Storage Configuration for Data Analytics. In: *USENIX Annual Technical Conference (ATC'18)*.
28. **Litz, Heiner**, A. Klimovic, and C. Kozyrakis (2017). ReFlex: Remote Flash == Local Flash. In: *22nd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'17)*.
29. **Litz, Heiner**, B. Braun, and D. R. Cheriton (2016). EXCITE-VM: Extending the Virtual Memory System to Support Snapshot Isolation Transactions. In: *25th International Confernce on Parallel Architectures and Compilation Techniques (PACT'25)*.
30. **Litz, Heiner**, D. Cheriton, A. Firoozshahian, O. Azizi, and J. P. Stevenson (2014). SI-TM: reducing transactional memory abort rates through snapshot isolation. In: *19th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'14)*.
31. Fröning, H., M. Nüssle, **Litz, Heiner**, C. Leber, and U. Brüning (2013). On achieving high message rates. In: *13th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid'13)*.
32. Leber, C., B. Geib, and **Litz, Heiner** (2011). High Frequency Trading Acceleration using FPGAs. In: *21st International Conference on Field Programmable Logic and Applications (FPL'21)*.
33. Fröning, H., M. Nüssle, **Litz, Heiner**, and U. Brüning (2010). A Case for FPGA based Accelerated Communication. In: *9th International Conference on Networking (ICN'9)*.
34. **Litz, Heiner**, M. Thürmer, and U. Brüning (2010). TCCluster: A Cluster Architecture Utilizing the Processor Host Interface as a Network Interconnect. In: *2010 IEEE International Conference on Cluster Computing (CLUSTER)*.

35. Fröning, H., **Litz, Heiner**, and U. Brüning (2009). Efficient Virtualization of High-Performance Network Interfaces. In: *8th International Conference on Networks (ICN'8)*.
36. **Litz, Heiner**, H. Froning, M. Thürmer, and U. Brüning (2009). An FPGA based Verification Platform for HyperTransport 3.x. In: *19th International Conference on Field Programmable Logic and Applications (FPL'19)*.
37. **Litz, Heiner**, H. Fröning, M. Nüssle, and U. Brüning (2008). VELO: A Novel Communication Engine for Ultra-low Latency Message Transfers. In: *37th International Conference on Parallel Processing (ICPP'08)*.
38. Fröning, H., M. Nüssle, D. Slogsnat, **Litz, Heiner**, and U. Brüning (2006). The HTX-Board: A Rapid Prototyping Station. In: *3rd annual FPGAWorld Conference*.
39. Ding, Y. and **Litz, Heiner** (2005). Creating Multiplatform User Interfaces by Annotation and Adaption. In: *11th International Conference on Intelligent User Interfaces (IUI'11)*.
40. Ding, Y., **Litz, Heiner**, and D. Pfisterer (2004). A graphical single-authoring framework for building multi-platform user interfaces. In: *9th international conference on Intelligent user interface (IUI'9)*.

Journal Papers

1. **Litz, Heiner**, J. Gonzalez, A. Klimovic, and C. Kozyrakis (2021). RAIL: Predictable, Low Tail Latency for NVMe Flash. In: *ACM Transactions on Storage (TOS)*.
2. Nagendra, N. P., G. Ayers, D. I. August, H. K. Cho, S. Kanev, C. Kozyrakis, T. Krishnamurthy, **Litz, Heiner**, T. Moseley, and P. Ranganathan (2020). AsmDB: Understanding and Mitigating Front-End Stalls in Warehouse-Scale Computers. *IEEE Micro*.
3. **Litz, Heiner**, R. J. Dias, and D. Cheriton (2015). Efficient Correction of Anomalies in Snapshot Isolation Transactions. *ACM Transactions on Architecture and Code Optimization (TACO)*.

Refereed Workshop Papers

1. Klimovic, A., **Litz, Heiner**, and C. Kozyrakis (2018a). Learning Heterogeneous Cloud Storage Configuration for Data Analytics. In: *SysML Conference*.
2. **Litz, Heiner**, A. Klimovic, and C. Kozyrakis (2018). ReFlex: Remote Flash == Local Flash. In: *9th Annual Non-Volatile Memories Workshop (NVMW)*.
3. Wang, B., **Litz, Heiner**, and D. R. Cheriton (2014). HICAMP bitmap: space-efficient updatable bitmap index for in-memory databases. In: *10th International Workshop on Data Management on New Hardware (DAMON'10)*.
4. Chan, M., **Litz, Heiner**, and D. R. Cheriton (2013). Rethinking network stack design with memory snapshots. In: *14th USENIX Conference on Hot Topics in Operating Systems (HotOs'14)*.
5. **Litz, Heiner**, C. Leber, and B. Geib (Nov. 2011). DSL Programmable Engine for High Frequency Trading Acceleration. In: *4th Workshop on High Performance Computational Finance (WHPCF '11)*.
6. Froning, H. and **Litz, Heiner** (2010). Efficient hardware support for the partitioned global address space. In: *24th IEEE International Symposium on Parallel & Distributed Processing, Workshops and Phd Forum (IPDPSW)*,
7. **Litz, Heiner**, H. Fröning, and U. Brüning (2010). HTAX: A Novel Framework for Flexible and High Performance Networks-on-Chip. In: *4th Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC'4)*.
8. Kalisch, B., A. Giese, **Litz, Heiner**, and U. Brüning (2009). HyperTransport 3 Core: A Next Generation Host Interface with Extremely High Bandwidth. In: *1st International Workshop on HyperTransport Research and Applications (WHTRA'09)*.
9. **Litz, Heiner**, H. Fröning, and U. Brüning (2009). A HyperTransport 3 Physical Layer Interface for FPGAs. In: *6th International Symposium on Applied Reconfigurable Computing (ARC'6)*.

10. Nüssle, M., H. Fröning, A. Giese, **Litz, Heiner**, D. Slogsnat, and U. Brüning (2007). A Hypertransport based low-latency reconfigurable testbed for message-passing developments. In: *2nd Workshop Kommunikation in Clusterrechnern und Clusterverbundsystemen (KiCC 2007)*.

Teaching Experience

Instructor, CSE120: "Computer Architecture"	'23, '22, '21, '20, '19, '18
Instructor, CSE226: "Advanced Parallel Computing"	'21, '20, '19
Instructor, CSE125: "Logic Design with Verilog"	'22, '21, '20, '19
Instructor, CSE220: "Advanced Computer Architecture"	'23, '22

Grants

I have acquired as PI or Co-PI $9.2 million in external research grants since 2017.

2023	H. Litz “Google gift”	$90,000
2022	H. Litz “Google gift”	$90,000
2022	R. Sanfelice, H. Litz, A. Halder “CPS Frontier NSF Large”	$5,758,472
2022	H. Litz “Intel research contract”	$150.000
2022	H. Litz “Samsung gift”	$75.000
2021	H. Litz “Google gift”	$60,000
2021	H. Litz “Facebook gift”	$60,000
2020	H. Litz “NSF CAREER award”	$529,995
2020	D. Long and H. Litz “NSF IUCRC Phase II grant”	$500,000
2020	H. Litz “Samsung gift”	$70,000
2020	H. Litz “Samsung research contract”	$120,000
2020	R. Sanfelice, H. Litz, A. Halder “UCSC center-scale seed funding award”	$75,000
2018	H. Litz and B. Paten “Accelerating Genomics Workloads with Smart SSDs”. WD	$960,000
2018	H. Litz “FoMR: Improving Microprocessor IPC for Data Center Workloads”. NSF/Intel	$360,000
2018	H. Litz and R. Felice “Optimized Trajectory planning for Automotive Vehicles”, NXP	$50,000
2017	H. Litz “NVMe Device Level support for Quality of Service”. Samsung	$100,000
2017	H. Litz “Data Center Flash Storage Disaggregation”. Broadcom	$100,000

Patents

Benjamin Geib, Heiner Litz, Mondrian Nuessle. ”Circuit arrangement for connection interface”. DE102011009518B4, EP2668763A2, US20140207881, filed 2011, assigned 2014.

Graduated Students

Ph.D. Students

2022 Yuanjian Ni (Meta)
2021 Chandranil Chakraborttii (Trinity College)

MS Students

2024 Peter Braun (ARM)
2022 Karthik Rajesh Kain (Intel)
2021 Maxwell Bradley (ScaleUpStream)
2020 Sachet Mittal (Amazon AWS)

Current Students

Saba Jamilan (PhD)
Minghao Xie (PhD), co-advised with Chen Qian
Lokesh Jaliminche (PhD)
Surim Oh (PhD)
Inje Kim (PhD)
Yinyuan Zhao (PhD)
Jayjeet Chakraborti (PhD)
Mingsheng Xue (MS)

Service

Chair

NVMW’24 - Program Chair
HOTCHIPS’23 - Program Chair

ASPLOS'23 - Sponsorship Co-Chair

Editor

IEEE MICRO - Associate Editor

Technical Program Comittee

HPCA'25
ASPLOS'25
ISCA'24
ASPLOS'24
MICRO'24
HPCA'24
ISCA'23
HPCA'23
ASPLOS'23
IISWC'22
MICRO'22
ISCA'22
HOTCHIPS'22
NSF'22 Panelist
NVMW'22
Eurosys'22
MICRO'21
ISCA'21
MICRO'20
Usenix ATC'21
Systor'20
Usenix ATC'20
SOCC'19
MICRO'19
HotOS'19
ISCA'19
HPCA-IS'19
PPoPP'19
SOCC'18
Micro'17
TACO'16
HPCA'15
ReCoSoC'11-16
HUCAA'13-15

Panelist

NSF'22 Panel DoE Basic Research Needs Panel NSF'19 Panel

Invited Talks

Datacenter Microprocessors

September 2022	Texas A&M University
May 2022	UC San Diego
May 2022	Stanford University
May 2022	UC Santa Barbara
May 2022	UIUC
May 2022	Industry Academia Partnership (IAP) Workshop
April 2022	UT Austin
April 2022	UC Berkeley
March 2022	Google
Jan 2022	Intel
Nov 2021	ARM

Data center Operating Systems

October 2020	Intel
August 2020	IBM
August 2020	Nutanix
August 2020	VMWare
October 2019	Intel
August 2019	Samsung
August 2019	VMWare
March 2019	Facebook
December 2018	IAP Industry Academia Partnership
August 2018	ITU University Kopenhagen
June 2018	Heidelberg University
June 2018	SAP, Walldorf
March 2017	UCSC
Dec 2016	Facebook
July 2016	Amazon AWS
July 2016	CNEX
July 2016	Google
July 2016	Cavium
Apr 2016	Ericsson
Feb 2016	Broadcom
Feb 2016	Stanford Platform Lab

Snapshot Isolation based Transactional Memory

Sep 2015	Samsung
July 2015	VMWare
July 2014	Heidelberg University
Jun 2013	HP Labs
Nov 2012	Stanford CIS

In Memory Deduplication

Nov 2013	SAP Labs
Oct 2013	High Performance Transaction Systems (HPTS)

High Frequency Trading with FPGAs

May 2012	Oracle Labs

HyperTransport Cache Coherent Interconnect and its Applications

Aug 2011 University of Valencia
Aug 2011 University of Albacete
Mar 2011 KLA-Tencor
Mar 2008 SUN Microsystems

Status

US, German Dual-Citizenship