

18×12 MATRIX LED DRIVER WITH AUTO BREATH

FEATURES

- 18 current sinks, 12 current switches, up to drive 216 LEDs or 72 RGBs.
- Programmable matrix size
- 3 pattern controllers for auto breathing or group PWM control
- Global 256-level DC current configuration
- Individual 256-level PWM for dimming
- Individual 256-level scaling current for color-mixing
- High-precision current sinks
 - Device-to-device error: $\pm 5\%$
 - Channel-to-channel error: $\pm 5\%$
- EMI and audible noise reduction
 - Phase control
 - Spread spectrum function
 - Programmable slew rate control
- Individual 216 LEDs open/short detection
- Multiple-device clock synchronization by SYNC pin
- UVLO and over-temperature protection
- De-Ghost
- 10MHz SPI interface
- Power supply: 2.7V~5.5V
- QFN 5mmx5mmx0.75mm-44L package

APPLICATIONS

Smart speaker, Bluetooth speaker
Gaming device (Keyboard, Mouse etc.)
Mobile phone, PAD

GENERAL DESCRIPTION

AW20216S is an 18x12 matrix LED driver programmed via an SPI compatible interface. Each channel has individual 8-bit DC current setting for color-mixing and 8-bit PWM current setting for brightness control. The global current of each channel is configured via register GCCR and external resistor R_{EXT} .

Three integrated pattern controllers provide auto breathing or group dimming control. Each pattern controller can work in auto breathing or manual control mode. All breathing parameters are configurable, including rising/falling slope, on/off time, repeat times, and minimum/maximum brightness, etc. Each LED's PWM parameter can be sourced from any one of the 3 pattern controllers optionally.

Phase-delay, phase-inverting, selectable three phase, spread spectrum and slew rate control technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW20216S can be turned off with minimum current consumption by either pulling the EN pin low or using the software reset.

AW20216S is available in QFN 5mmx5mmx0.75mm-44L package. It operates from 2.7V to 5.5V over the temperature range of -40°C to $+85^{\circ}\text{C}$.

TYPICAL APPLICATION CIRCUIT

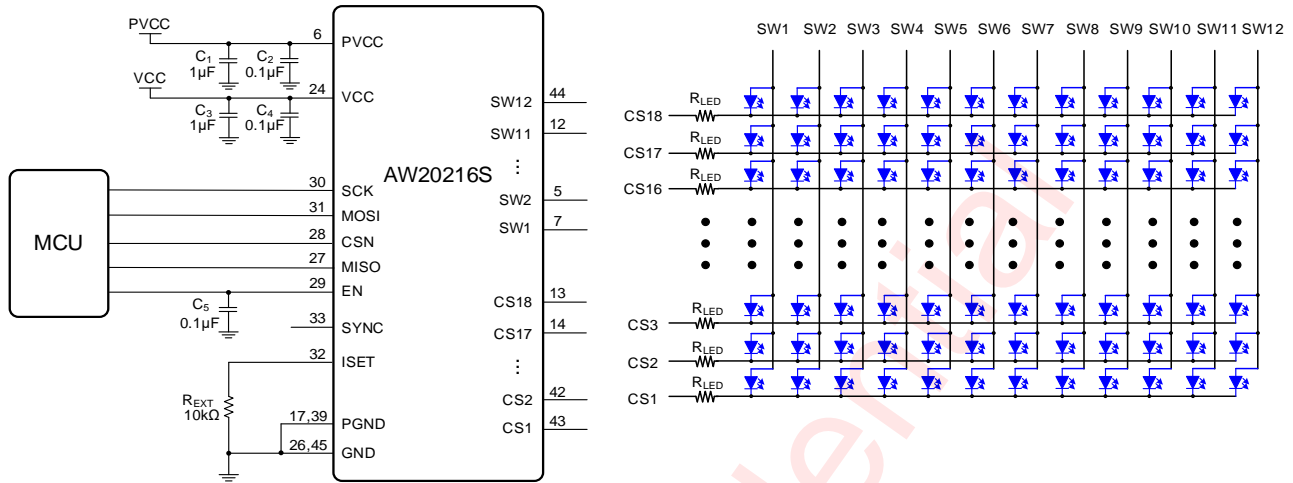
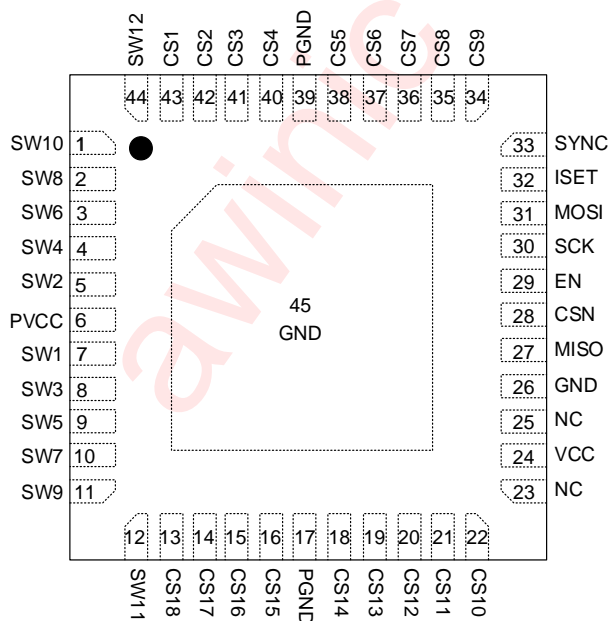
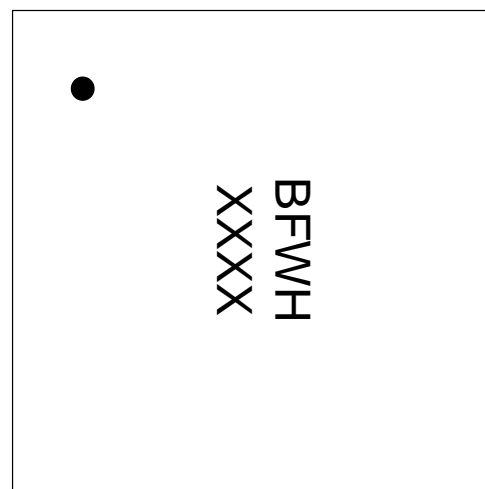


Figure 1 AW20216S Application Circuit

Note1: The resistance R_{LED} is determined by $PVCC$, V_F of LED, I_{LED} , V_{HR} of CS_x and SW_x . $R_{LED} = (PVCC - V_F - V_{HR_{CS}} - V_{HR_{SW}}) / I_{MAX}$.

PIN CONFIGURATION AND TOP MARK

AW20216SQNR
(Top View)AW20216SQNR Marking
(Top View)

BFWH-AW20216SQNR
XXXX-Production Tracing Code

Figure 2 Pin Configuration and Top Marking

PIN DEFINITION

No.	NAME	DESCRIPTION
1~5	SW10, SW8, SW6, SW4, SW2	Current switches
6	PVCC	Current source power supply, 2.7V~5.5V
7~12	SW1,SW3, SW5,SW7, SW9,SW11	Current switches
13~16	CS18~CS15	Current sink
17	PGND	Power ground
18~22	CS14~CS10	Current sink
23	NC	No connection
24	VCC	Power supply, 2.7V~5.5V
25	NC	No connection
26	GND	Ground
27	MISO	Serial output data for SPI interface
28	CSN	Chip select for SPI interface
29	EN	Standby the chip when EN is low, internally pulled down to GND with a resistor of 1M Ω
30	SCK	Serial clock input for SPI interface
31	MOSI	Serial input data for SPI interface
32	ISET	When R _{EXT} =10k Ω , global current of LED is 40mA
33	SYNC	Synchronize pin, used to synchronize clock in multiple devices application, internally pulled down to GND with a resistor of 1M Ω
34~38	CS9~CS5	Current sink
39	PGND	Power ground
40~43	CS4~CS1	Current sink
44	SW12	Current switch
45	GND	Thermal pad

FUNCTIONAL BLOCK DIAGRAM

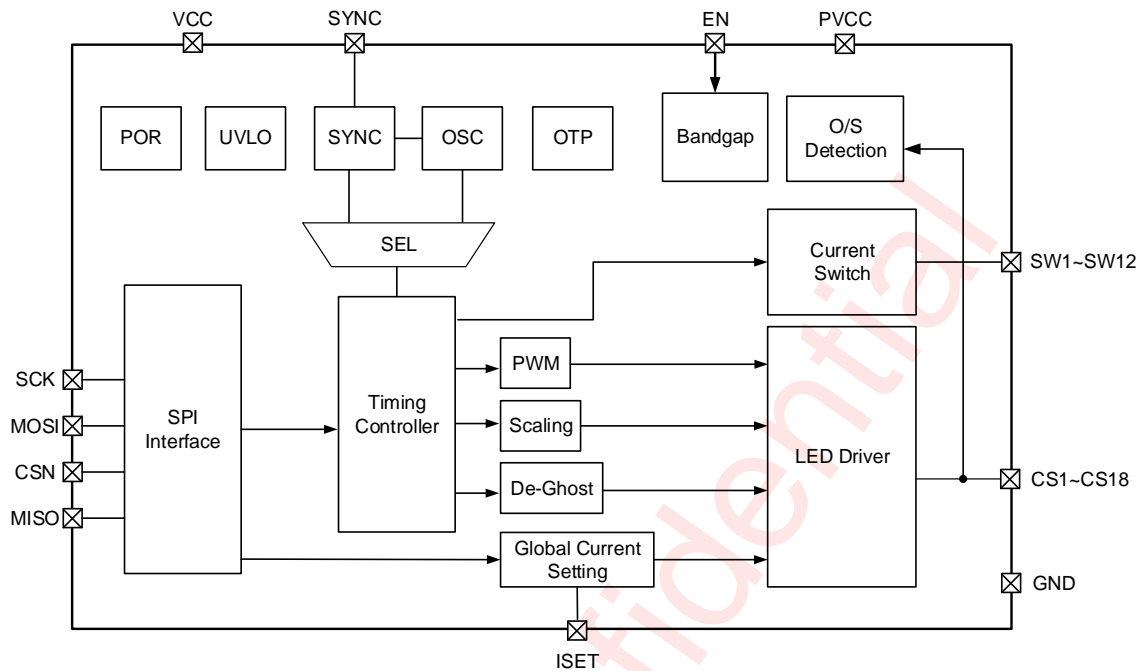


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUIT

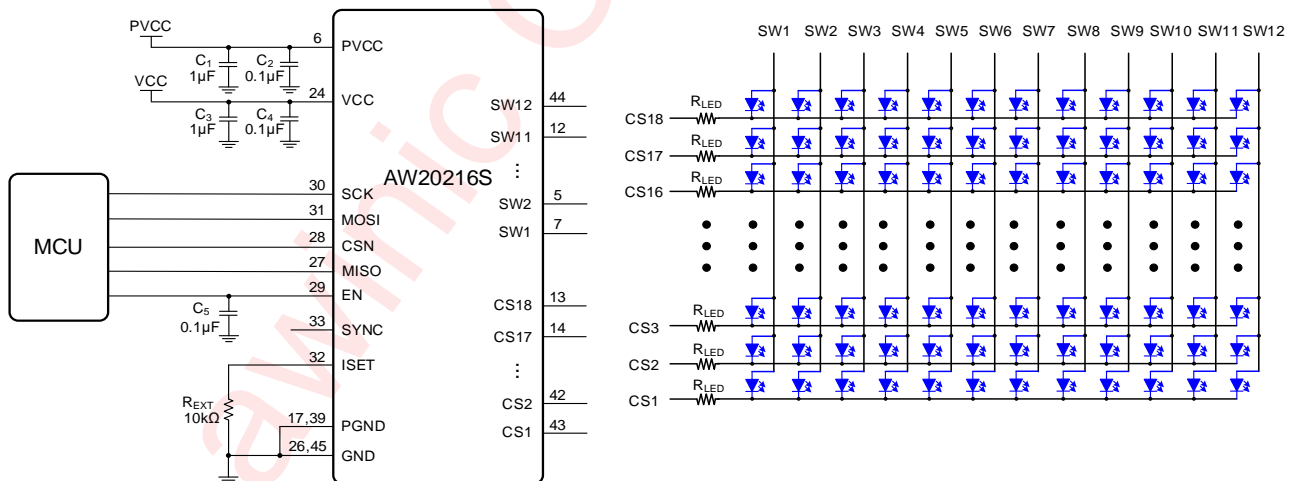


Figure 4 Typical Application Circuit

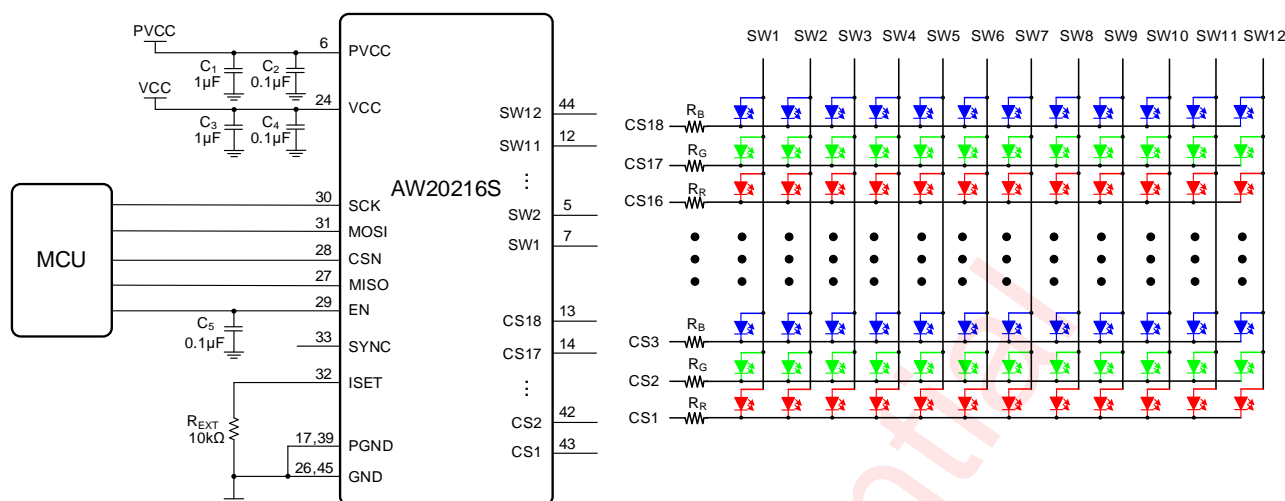


Figure 5 Typical Application Circuit (RGB)

Note2: The resistance $R_R / R_G / R_B$ is determined by $PVCC$, $V_{F(R/G/B)}$ of LED, V_{HR} of CSx and SWx. $R_R / R_G / R_B = (PVCC - V_{F(R/G/B)} - V_{HR_{CS}} - V_{HR_{SW}}) / I_{MAX}$.

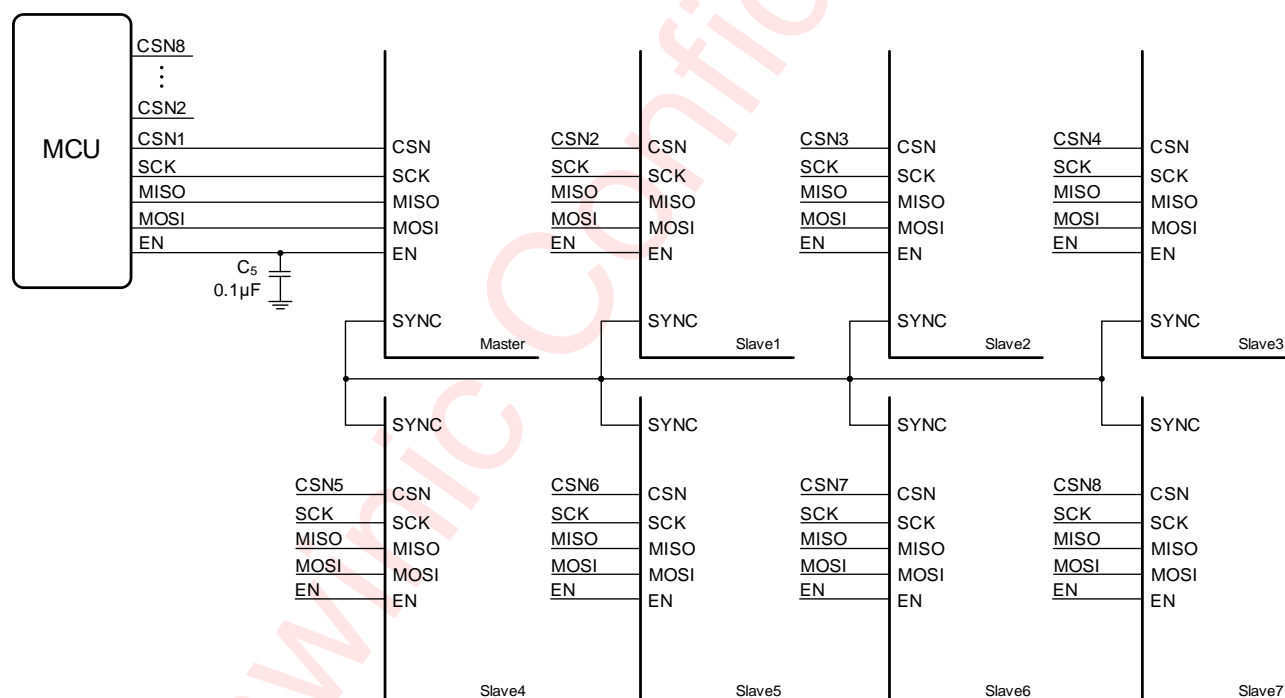


Figure 6 Typical Application Circuit (Eight Parts Synchronization)

Note3: One part is set as master mode, and all the other 7 parts set as slave mode (set master after set all slaves). Master mode or slave mode set by register SSCR (page0, address=0x28). Master part output master clock, and all slaves input the master clock.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW20216SQNR	-40°C~85°C	QFN 5mmX5mm-44L	BFWH	MSL3	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS (NOTE4)

PARAMETERS		RANGE
Supply voltage range VCC		-0.3V to 6V
Supply voltage range PVCC		-0.3V to 6V
Input voltage range	SCK, MOSI, EN, CSN, MISO	-0.3V to VCC
Output voltage range	SW1~SW12, CS1~CS18	-0.3V to PVCC
Voltage on ISET	ISET	-0.3V to 2V
Junction-to-ambient thermal resistance θ_{JA}		33°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		160°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (NOTE5)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78E		±IT: 200mA

NOTE4: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9 (HBM). JEDEC EIA/JESD22-C101F (CDM)

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Input voltage	2.7	3.6	5.5	V
PVCC	Input voltage	2.7	5	5.5	V
C ₁ , C ₃	Input capacitance	1	1	22	μF
C ₂ , C ₄ , C ₅	Input capacitance	0.1	0.1	1	μF
R _{EXT}	External resistor for setting sink current	5	10	20	kΩ
T _A	Operating free-air temperature range	-40	25	85	°C

ELECTRICAL CHARACTERISTICS

T_A=25°C, PVCC=VCC=3.6V (unless otherwise noted), R_{EXT}=10kΩ

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
VCC	Input operating range		2.7		5.5	V
I _{STB_VCC}	Standby current	V _{EN} =0V or CHIPEN = 0		1.3		μA
I _{ACT_VCC}	Quiescent current in active mode	V _{EN} =VCC,CHIPEN=1, all LEDs off		1.8		mA
I _{MAX}	Maximum sink current(CS1~CS18)	V _{LED} =0.5V, GCC= 0xFF, SL= 0xFF		40		mA
V _{HR}	Current switch headroom voltage SWx	I _{SWITCH} =720mA, GCC=0xFF, SL=0xFF		750		mV
	Current sink headroom voltage CSx	I _{SINK} =40mA, GCC=0xFF, SL=0xFF		300		mV
I _{LIM}	Internal sink current limit	R _{EXT} =0,UVCR.OCPTH=0		75		mA
		R _{EXT} =0,UVCR.OCPTH=1		120		
I _{MATCH}	Device to device current error	All Channels' current set to 40mA	-5		5	%
ΔI _{LED}	Channel to channel current error	All Channels' current set to 40mA	-5		5	%
F _{OSC}	OSC clock frequency		14.88	16	17.12	MHz
T _{SD}	Thermal shutdown threshold			165		°C
	Thermal shutdown hysteresis			25		°C
LOGIC (SCK, MOSI, EN, CSN, MISO)						
V _{IL}	Input logic low	VCC=2.7V~5.5V			0.6	V
V _{IH}	Input logic high	VCC=2.7V~5.5V	2.4			V
Timing						
T _{SCAN}	Period of scanning	PCCR.PWMFRQ[2:0] = 000, GCR.SWSEL[3:0] = 1011		216		μs
T _{DG}	Non-overlap time between SW			1		μs
T _{HOLD}	Delay time between the falling edge of CS18 and SWx			125		ns

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T _{SETUP}	Delay time between the rising edge of SWx and CS1	PCCR.PWMFRQ[2:0] = 000		250		ns
T _{DLY}	Delay time of each CS group, there are 6 groups of CS	PCCR.PWMFRQ[2:0] = 000		125		ns

SPI INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Units
f_c	Clock frequency			10	MHz
T_{CSAS}	CS active setup time	30			ns
T_{CSAH}	CS active hold time	15			ns
T_{CSNS}	CS not active setup time	15			ns
T_{CSNH}	CS not active hold time	15			ns
T_{CH}	SCK high time	20			ns
T_{CL}	SCK low time	35			ns
T_{DS}	Data in setup time	10			ns
T_{DH}	Data in hold time	15			ns
T_{DO}	SCK falling edge to MISO data update time		12	42	ns

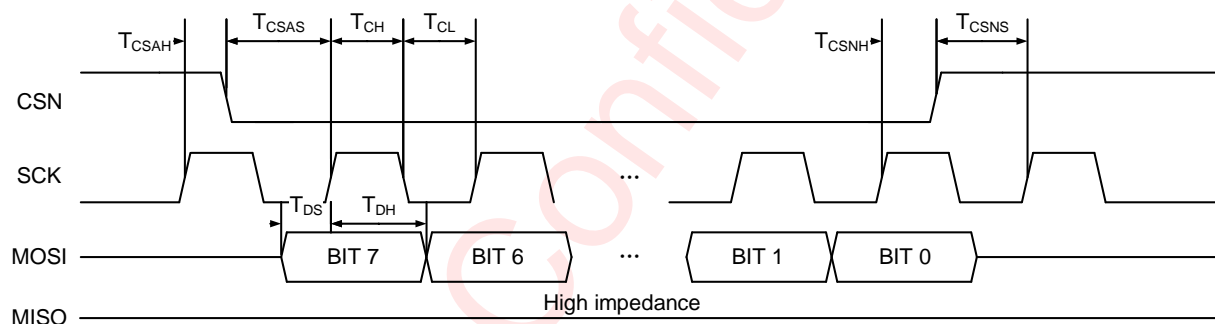


Figure 7 SPI Interface Input Timing

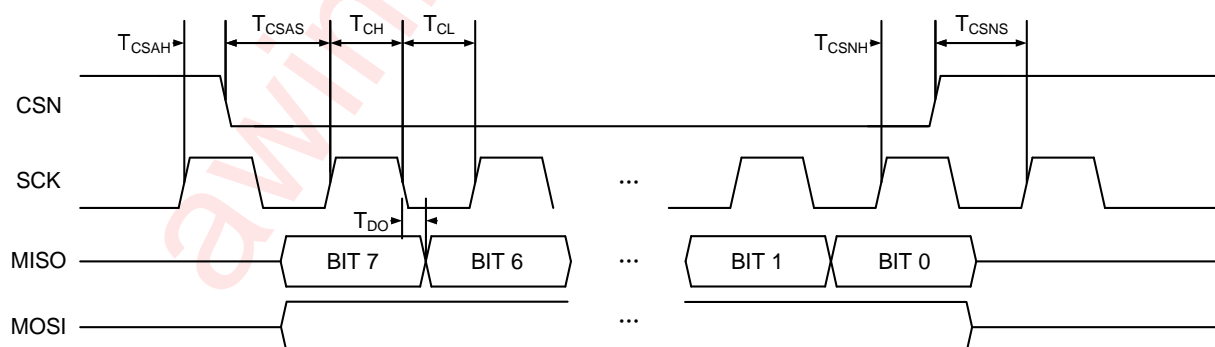


Figure 8 SPI Interface Output Timing

DETAILED FUNCTIONAL DESCRIPTION

OPERATION MODE AND RESET

POWER ON RESET (POR)

During initial power-up, AW20216S is reset, and all registers are reset to default value, and LED driver is shut down.

Once the supply voltage VCC drops below the threshold voltage V_{POR_VCC} (2.0V), the power-on-reset will be activated to reset the device again. By reading the bit PUST of the register UVCR (page0, address=0x2A), it can be determined whether the device has been reset.

Below is the recommended operation timing:

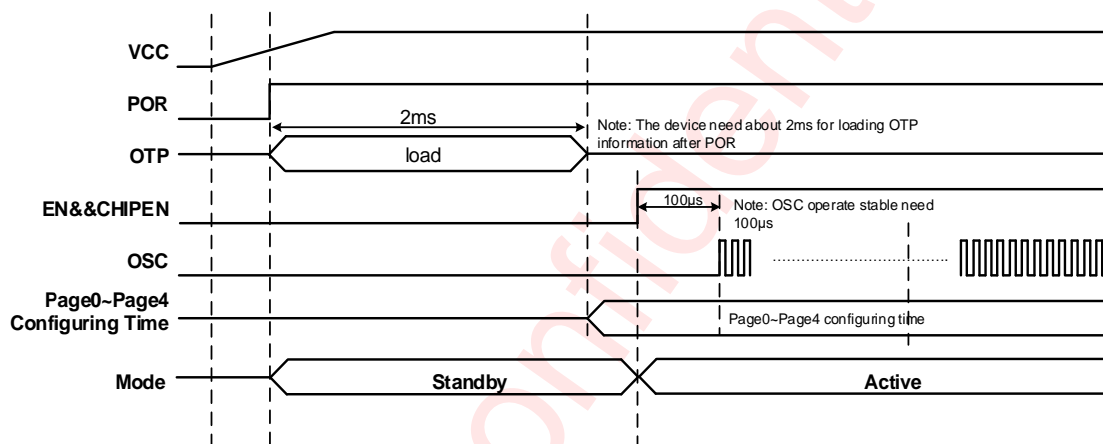


Figure 9 Power up Timing

SOFTWARE RESET

By writing 0xAE to register RSTN (page0, address=0x2F), the software reset is triggered. After software reset, all registers will be reset to the default value and enter into standby mode.

After the software reset command is input through SPI or power on reset, it needs to wait at least 2ms before any other SPI command can be accepted.

STANDBY MODE

When EN is pulled low or the bit CHIPEN of the register GCR (page0, address=0x00) is set to "0" or UVLO is triggered (UVFLG=1) in active mode or OT is active, AW20216S enters into standby mode automatically. In standby mode, all analog blocks are power down but the registers retain the data and keep it available via SPI. When POR is triggered, the device enters into standby mode and all registers will be reset (more information is showed in POWER ON RESET).

ACTIVE MODE

When EN is in high level, and the bit CHIPEN of the register GCR (page0, address=0x00) is set to "1", AW20216S enters into the active mode.

LOW POWER MODE

The bit LPEN of the register MIXCR (page0, address=0x46) is set to "1", the low power mode is enabled. When all PWM[7:0] are 0x00 in active frame, AW20216S automatically enters into low power mode for power saving.

If any bit of PWM[7:0] is not 0 in active frame, the device exits low power mode immediately.

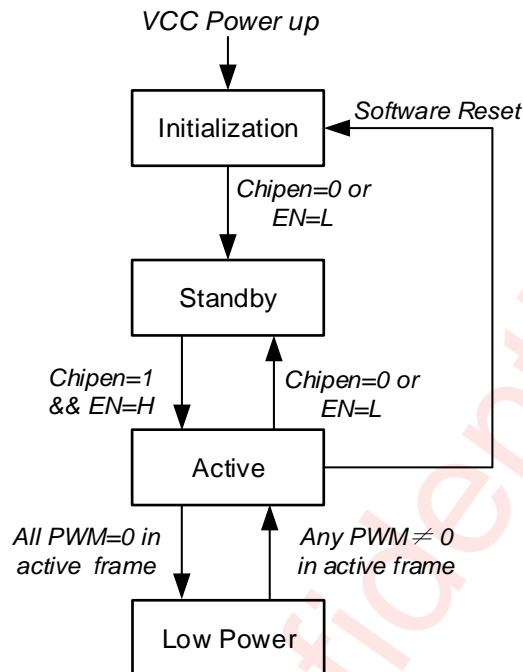


Figure 10 AW20216S Operating Mode Transition

SPI INTERFACE

AW20216S supports the SPI serial bus and data transmission protocol in fast mode from 1MHz to 10MHz. This device operates as a slave on the SPI bus. SPI master controls write or read register of the device.

The SPI data format is 8-bit long. The first command byte is composed by 4-bit chip ID, 3-bit page ID and W/R bit, the command byte must be sent first, then is followed by register address and then the register data. In AW20216S, the 4-bit chip ID is always 4'b1010, the 3-bit page ID can be set from 0 to 4. If W/R is 0, which will be write operation and master can write data into the register, If W/R is 1, which will be read operation and master can read data from the register.

BITS	D7:D4	D3:D1	D0
Value	1010	000: Page 0 001: Page 1 010: Page 2 011: Page 3 100: Page 4	0: Write 1: Read

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, data is sent from the master device to the slave device in MOSI, MISO will be unchanged.

Typical write:

- (1) First of all, master sets CSN to low, to enable operation to the device.
- (2) Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and write command.

- (3) Then master sends the register address.
- (4) Then master sends the data to write into register address sent before.
- (5) Finally master pulls CSN high to finish the operation.

Automatic address increment write:

- (1) – (3) Same as above.
- (4) During the 8th rising edge of receiving the first data byte, the internal address pointer will increment by one. The next data byte sent to AW20216S will be placed in the next address, and so on. The auto increment of the address will continue as long as data continues to be written to AW20216S.
- (5) Finally master pulls CSN high to finish the operation.

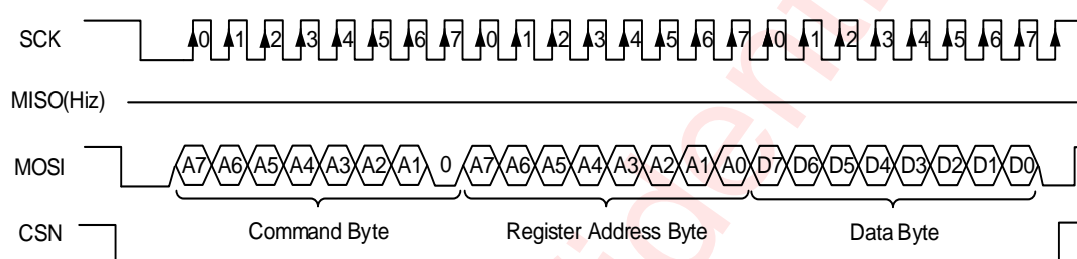


Figure 11 SPI Writing to AW20216S (Typical)

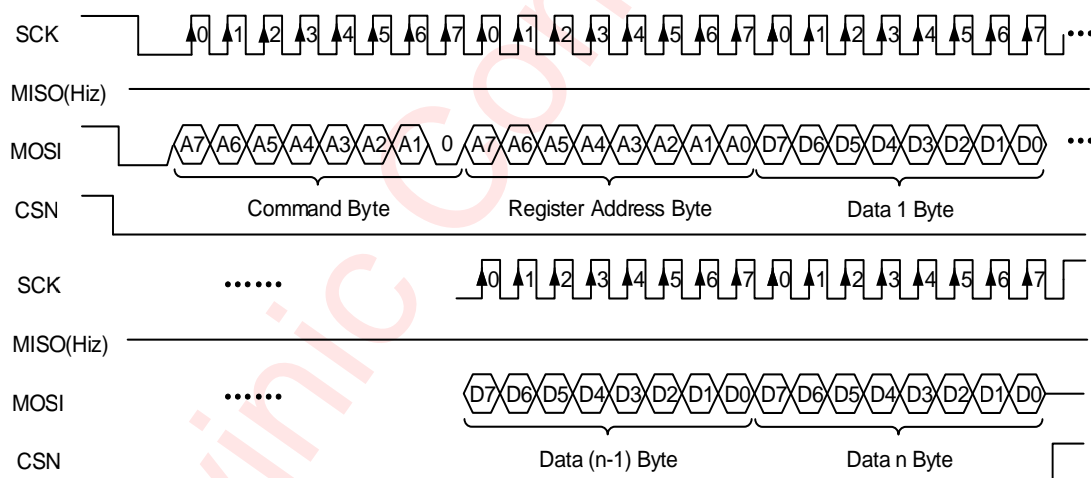


Figure 12 SPI Writing to AW20216S (Automatic Address Increment)

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the read command data and register address will send in MOSI and read data will send back to master in MISO.

Typical read:

- (1) First of all, master sets CSN to low, to enable operation to the device.
- (2) Then master sends eight bits of command, including 4-bit chip ID, 3-bit page register and read command.
- (3) Then master sends the register address.
- (4) Then the device sends the data read out from register address sent before in MISO.
- (5) Finally master pulls CSN high to finish the operation.

Automatic address increment read:

- (1) – (3) Same as above.
- (4) During the 8th rising edge of sending the first data byte, the internal address pointer will increment by one. The next data byte sent from AW20216S will be placed in the next address, and so on. The auto increment of the address will continue as long as data continues to be read from AW20216S.
- (5) Finally master pulls CSN high to finish the operation.

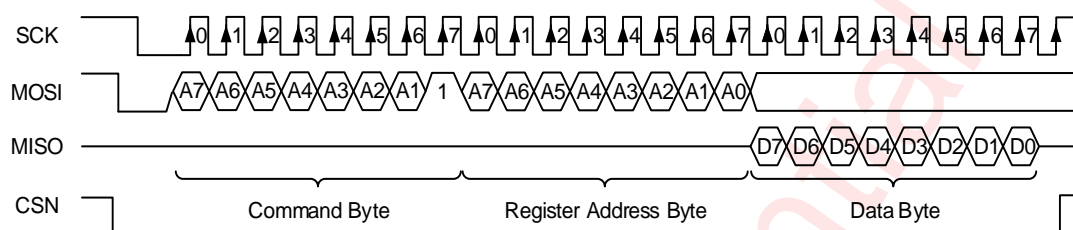


Figure 13 SPI Read from AW20216S (Typical)

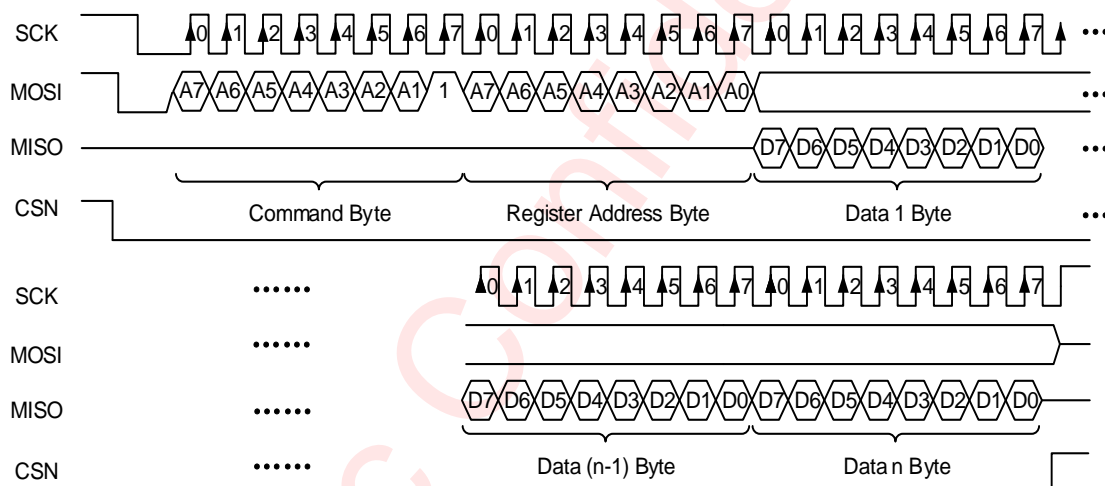


Figure 14 SPI Read from AW20216S (Automatic Address Increment)

UNDER VOLTAGE LOCK OUT (UVLO)

When bit UVDIS of the register UVCR (page0, address=0x2A) is set to "0", the device monitors the voltage of VCC. If the voltage drops below threshold (2.5V typically), the bit UVFLG of the register UVCR (page0, address=0x2A) will be set to "1". After read-out, the bit UVFLG will be clear.

If both bit UVDIS and bit UVPD of the register UVCR (page0, address=0x2A) are set to "0", UVLO protection function is enabled. Once the event of under voltage occurs, the bit CHIPEN of the register GCR (page0, address=0x00) will be cleared to "0", and then the device will enter into standby mode. If the voltage of VCC rises above the UVLO threshold and then write "1" to bit CHIPEN, the device will enter into active mode again. By default, control bits UVDIS, UVPD are all "0". Both UVLO monitor and protection are enabled.

OVER TEMPERATURE PROTECTION (OTP)

OVER TEMPERATURE ROLL OFF

The bits TRTH[1:0] and bits TROF[1:0] of register OTCR (page0, address=0x27) are thermal roll off threshold temperature and thermal roll off percentage of I_{OUT} respectively. The threshold temperature can be configured

as 140°C, 120°C, 100°C or 90°C. Thermal roll off percentage can be configured as 100%, 75%, 50% or 30%. When set the bits TRTH[1:0] to be “00” and set bits TROF[1:0] to be “10”, the thermal roll off threshold temperature is “140°C”. Once the temperature is over 140°C, the flag bit TRFLG of register OTCR (page0, address=0x27) is set to “1”, and I_{OUT} will be decreased to its 75%.

OVER TEMPERATURE ALL LED IS OFF

When bit OTDIS of the register OTCR (page0, address=0x27) is set to “0”, the over-temperature detection is enabled. Once the temperature of this device reaches 165°C, the over-temperature condition is detected, and the bit OTFLG of the register OTCR (page0, address=0x27) will be set to “1”. The OTFLG will be cleared to “0” after reading the register OTCR.

If both bit OTDIS and bit OTPD of the register OTCR (page0, address=0x27) are set to “0”, the Over-Temperature Protection (OTP) function is enabled. Once the temperature is over 165°C, the bit CHIPEN of the register GCR (page0, address=0x00) will be cleared to “0”, and then the device will enter into standby mode. When the temperature returns below 140°C, the device will enter into active mode again after writing “1” to bit CHIPEN.

By default, control bits OTDIS and OTPD are all “0”, both OT monitor and OT protection are enable.

LED OPEN/SHORT DETECTION

AW20216S supports LED open/short detection. When bits OSDE[1:0] of the register GCR (page0, address=0x00) are set to “11”, open detection is enabled, and the detection results can be read out via the registers OSR0~OSR35 (page0, address=0x03~0x26) when CHIPEN is “1”. Similarly, when set bits OSDE[1:0] of the register GCR (page0, address=0x00) to “10”, short detection is enabled, and the results also can be read out via the registers OSR0~OSR35 when CHIPEN is “1”. Each bit of OSR0~OSR35 store a LED's open/short status. Each OSR register stores 6 LEDs open/short status in bit5~bit0. For example, OSR0 stores the status of LED0~LED5, in which MSB is status of LED5, and LSB is status of LED0.

	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8	CS9	CS10	CS11	CS12	CS13	CS14	CS15	CS16	CS17	CS18
SW1	OSR0						OSR1						OSR2					
SW2	OSR3						OSR4						OSR5					
SW3	OSR6						OSR7						OSR8					
SW4	OSR9						OSR10						OSR11					
SW5	OSR12						OSR13						OSR14					
SW6	OSR15						OSR16						OSR17					
SW7	OSR18						OSR19						OSR20					
SW8	OSR21						OSR22						OSR23					
SW9	OSR24						OSR25						OSR26					
SW10	OSR27						OSR28						OSR29					
SW11	OSR30						OSR31						OSR32					
SW12	OSR33						OSR34						OSR35					

Figure 15 Open/Short Register

The valid detect result is determined by:

Short detection: $V_{CS} > PVCC - V_{TH_{SHORT}}$

Open detection: $V_{CS} < V_{TH_{OPEN}}$

$V_{TH_{SHORT}}$: Threshold of short detection ($V_{TH_{SHORT}} = 1.5V$, typical).

$V_{TH_{OPEN}}$: Threshold of open detection ($V_{TH_{OPEN}} = 0.1V$, typical).

The recommend configuration in $PVCC=4.2V$ is:

- $PSEL[1:0] = 2'b00$, (page0.PCCR[1:0]);
- $0x05 \leq GCC[7:0] \leq 0x80$, (page0.GCCR);
- $0x20 \leq PWM[7:0] \leq 0xFF$, (page1.PWMn, n=0~215);
- $SL=0xFF$, (page2.SLn, n=0~215);

LED DISPLAY AND CONTROL

LED DISPLAY CONTROL DESCRIPTION

The device supports up to 216 LEDs. The location of each LED is shown by the following figure. The parameter location in page1~page3 is the same as the LED.

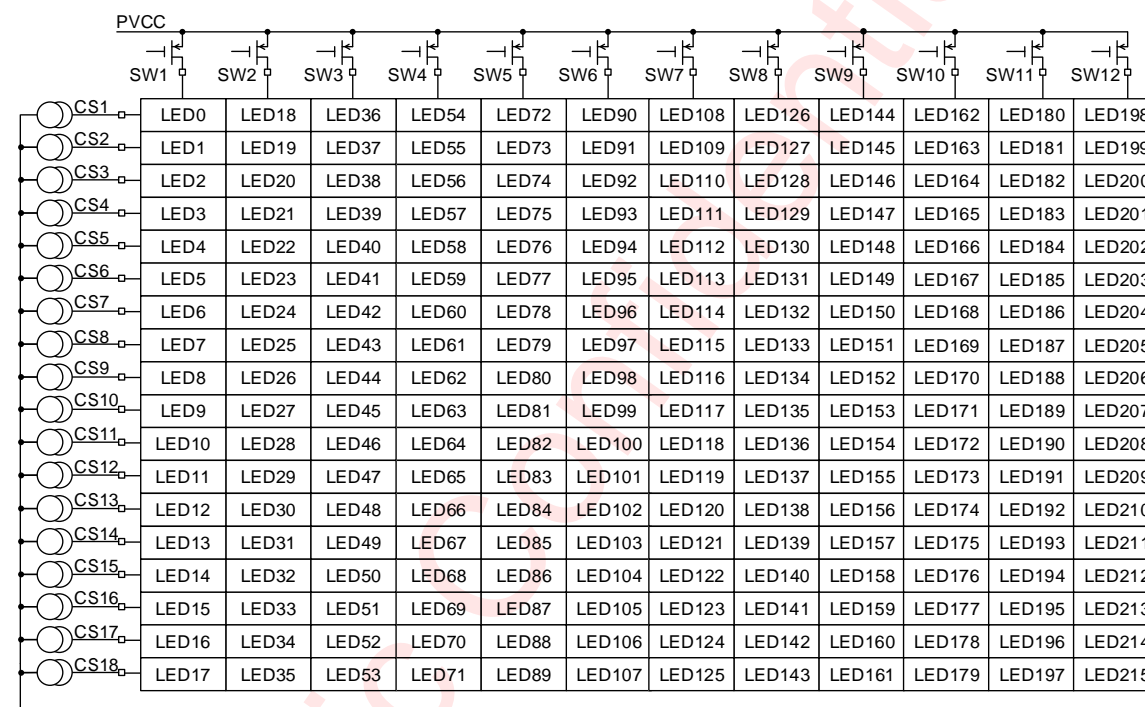


Figure 16 LED Location

In AW20216S, each LED is controlled by 4 independent parameters:

- $GCC[7:0]$ control, Global Current Control, register GCCR (page0, address=0x01);
- $PWM[7:0]$ control, register PWMn (page1, address=0x00~0xD7, n=0~215)
- $SL[7:0]$ control, register SLn (page2, address=0x00~0xD7, n=0~215)
- $PAT[1:0]$ selection, PAT choice, register PATn (page3, address= 0x00~0x47, n=0~215)

User can program above parameters to control each LED. Register PWM can control the brightness of LEDs, register SL can control the constant current and register GCCR can adjust the global current. Via configuring registers PATn (n=0~215), Each LED can be controlled by an internal pattern controller (PAT0, PAT1, PAT2) to dimming synchronously or output the same breathing lighting effect. A group PAT of LEDs controlled by register PATGn (n=0~71) which contains 3 adjacent LEDs. The figure below shows the LED current control model of AW20216S.

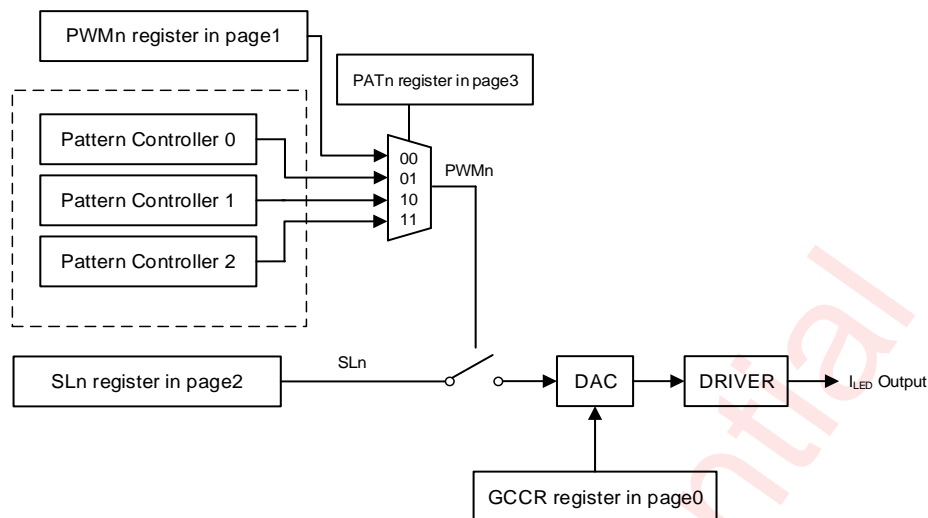


Figure 17 LED Current Control Model

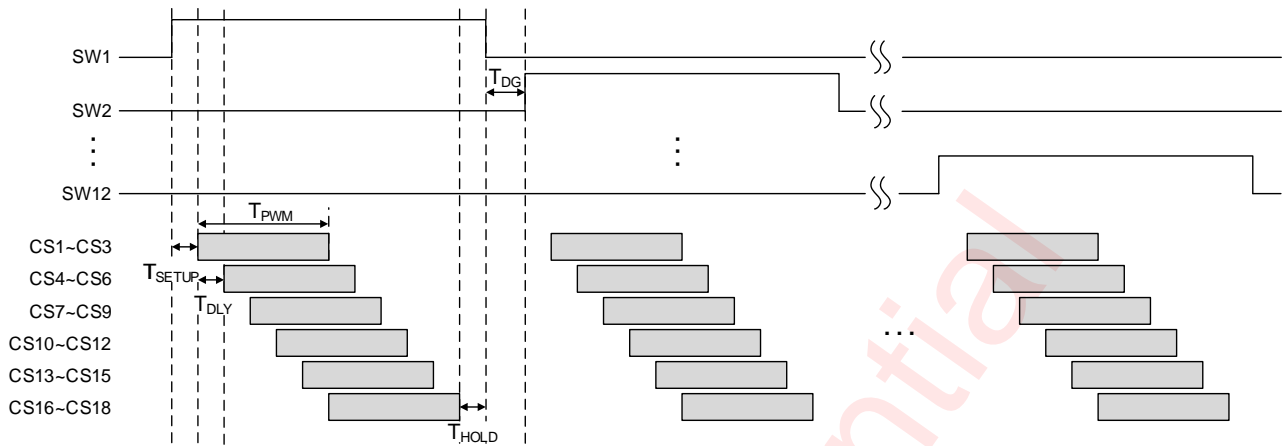
The device supports multiple parameters fast updating. The PWM, SL and PAT parameters of each LED are distributed in page1, page2 and page3 respectively. The page4 is virtual page. In page4, PWM and SL parameter of each LED are put together, so it is easy to update both PWM and SL in the order of LED in very short time via one continuous write operation of SPI. The following figure shows the distribution of display parameter in different page.

page1 (addr: 0x51)				page2 (addr: 0x52)			
0x00	PWM0			0x00	SL0		
0x01	PWM1			0x01	SL1		
0x02	PWM2			0x02	SL2		
		
0xD7	PWM215			0xD7	SL215		

page3 (addr: 0x53)				page4 (addr: 0x54)			
0x00	PAT2	PAT1	PAT0	PATG0	0x00	PWM0	SL0
0x01	PAT5	PAT4	PAT3	PATG1	0x01	PWM1	SL1
0x02	PAT8	PAT7	PAT6	PATG2	0x02	PWM2	SL2

0x47	PAT215	PAT214	PAT213	PATG71	0xD7	PWM215	SL215

Figure 18 Display Parameter Distribution in Page1~Page4

SCANNING TIMING**Figure 19 Scanning Timing**

As shown in scanning timing figure, the SW1~SW11 is turned on by serial, LED is driven by CS1~CS18 within the SW_x (x=1~12) active time. T_{DG} is the non-overlap between SW is De-Ghost time. T_{SETUP} is the delay time between the rising edge of SW_x and CS1. SW Control 18 channels current sink (CS1~CS18). CS are divided into 6 groups, and each group has a delay time, which is T_{DLY}. T_{PWM} is PWM active time when the register PWM_n=0xFF (n=0~215), and T_{HOLD} is the time between the falling edge of CS18 and SW_x. In addition, SW scanning number N (N=1~12) can be controlled by bits SWSEL[3:0] in register GCR. N is the sum of 1 and the value of SWSEL[3:0], when the value of SWSEL[3:0] is below 2'b1100. Otherwise N is 12.

When PCCR.PWMFRQ[2:0] = 000 (page0, address=0x29), the DUTY is:

$$DUTY = \frac{15.9375\mu s}{0.25\mu s + 5 \times 0.125\mu s + 16\mu s + 0.125\mu s + 1\mu s} \times \frac{1}{N}$$

Where T_{PWM} = 15.9375μs, T_{SETUP}=0.25μs, T_{DLY}=0.125μs, T_{HOLD}=0.125μs, and T_{DG}=1μs. The period of PWM is 16μs. N is the SW scanning number.

The average output current of LED_n (n=0~215) can be expressed by the following formula,

$$I_{LED} = \frac{K}{R_{EXT}} \times \frac{GCC}{255} \times \frac{SL_n}{255} \times \frac{PWM_n}{255} \times DUTY$$

Where K = 400V, and R_{EXT} is the value of external resistor.

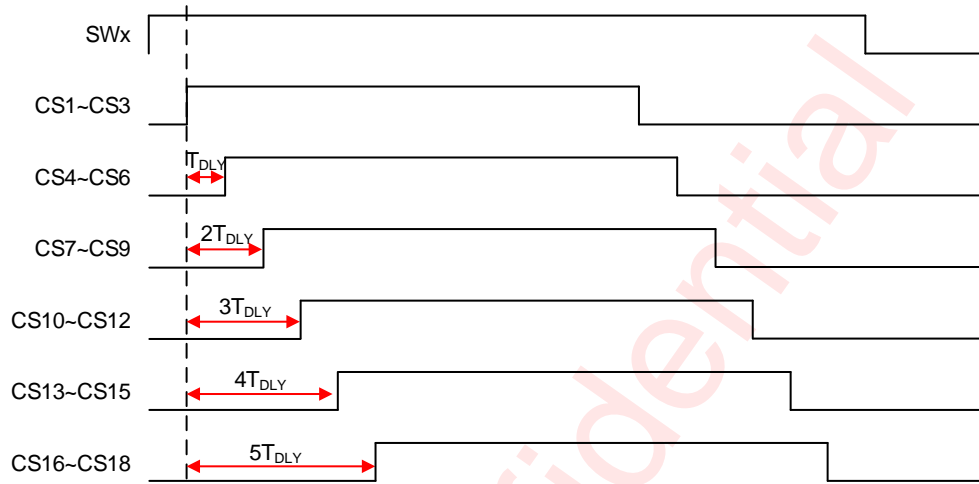
PWM MODULATION**PWM FREQUENCY**

The PWM frequency is decided by bits PWMFRQ[2:0] of register PCCR (page0, address=0x29). Following table shows the relationship of PWM frequency and the PWMFRQ[2:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency higher than 20 kHz.

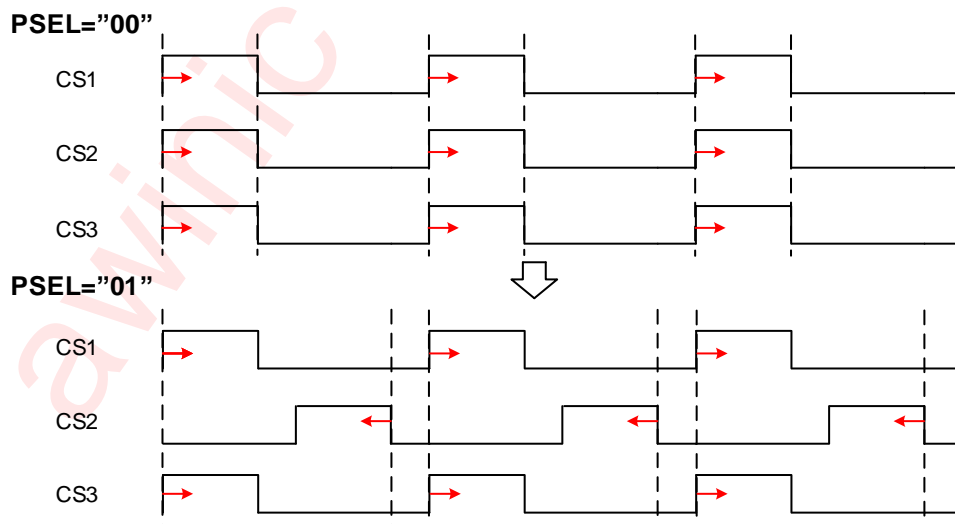
PWMFRQ[2:0]	000	001	010	011	100	101	110	111
PWM Freq.	62.5kHz	31.25kHz	15.6kHz	7.8kHz	3.9kHz	1.95kHz	975Hz	488Hz

PWM PHASE CONTROL

To reduce the peak load current and ceramic-capacitor audible ringing, AW20216S supports 6 groups phase delay, phase inverting and three-phase mode. When the bits PSEL[1:0] in register PCCR (page0, address=0x29) is "00", the 6 group PWM phase-delay scheme is enabled, which means only 3 of 18 LEDs could switch on in the same time. The following figure shows the timing of phase delay mode.

**Figure 20 Phase Delay Mode**

When setting the PSEL[1:0] to "01", the PWM phase of the even-numbered channels is inverted on the basis of phase-delay, as shown figure phase inverting mode. When setting the PSEL[1:0] to "10/11", three-phase mode is enabled, as shown figure three-phase mode. Phase delay, phase inverting and three-phase mode reduce the number of switch-on LEDs at the same time, which is good for reducing the input-current ripple.

**Figure 21 Phase Inverting Mode**

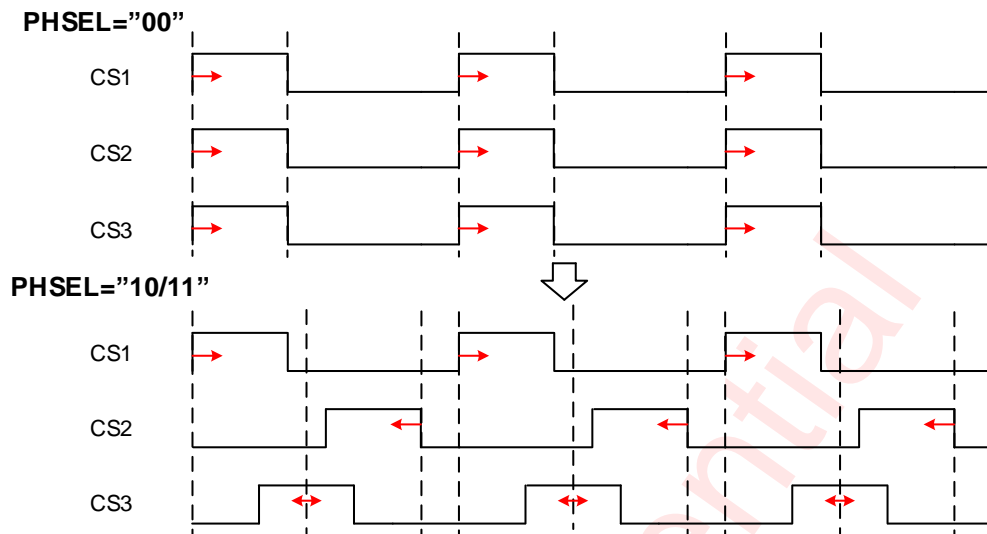


Figure 22 Three-Phase Mode

EMI REDUCTION

SLEW RATE

AW20216S supports programmed slew rate control, which can change the transition time of the LED current sink (CS1~CS18) on or off, so as to achieve the effect of reducing EMI. The slew rate control is configured by the bits SRR and SRF[1:0] of register SRCR(page0, address=0x2B).

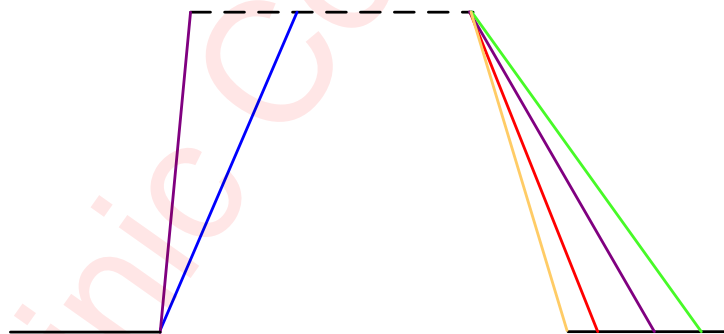


Figure 23 Slew Rate Control

SPREAD SPECTRUM

AW20216S has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (page0, address=0x28) is set to "1", spread spectrum function is enabled. By setting the bit SSR in register SSCR (page0, address=0x28), four spread spectrum range 5%, 15%, 25% and 35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

DE-GHOST FUNCTION

To prevent the LED ghost effect, AW20216S has integrated pull down resistors for each SWx (x=1~12) and pull up resistor for each CSx (x=1~18). The pull up 8kΩ resistor is disabled when bit PUDIS of register DGCR (page0, address=0x02) is set to "1", and the PUDIS is "0" in default. In addition, SWPDR[2:0] of register DGCR

(page0, address=0x02) can select the SWx pull down resistor. The PDMD of register DGCR (page0, address=0x02) can select the operating mode of de-ghost resistors. When the bit PDMD is "0", the SWx pull down resistor only work at CSx turning-off time. When the bit PDMD is "1", the SWx pull down resistor work all the time.

PATTERN CONTROLLERS

There is a breathing pattern controller (BPC) in the device, it has three patterns (PAT0~PAT2). Each LED can be configured different patterns by Page3 (PAT choice register), each register can control three LEDs, and each LED have three patterns (00: PWM, 01: PAT0, 10: PAT1, 11: PAT2). Page3 has 72 registers (72x3). PAT0CFG~PAT2CFG (page0, address=0x42~0x44) are PAT0~PAT2 configure registers. When bit PATEN in register PATxCFG (x=0~2) is set to "1", breathing pattern controller is enabled. Pattern controller can be configured as autonomous breathing mode or manual-controlled mode.

AUTONOMOUS BREATHING MODE

When PATEN is set to "1", the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off-time respectively. Register PWMxH (x=0~2, page0, address=0x30~0x32) and PWMxL (x=0~2, page0, address=0x33~0x35) control the maximum and minimum brightness of the breathing, respectively. When bit LOGEN in register PATxCFG (x=0~2) is set to "1", the lighting effects switch to logarithmic mode. In the logarithmic mode, the lighting effect is smoother than the linear mode during T0 and T2, and causes the change in intensity to appear more linear to the human eye.

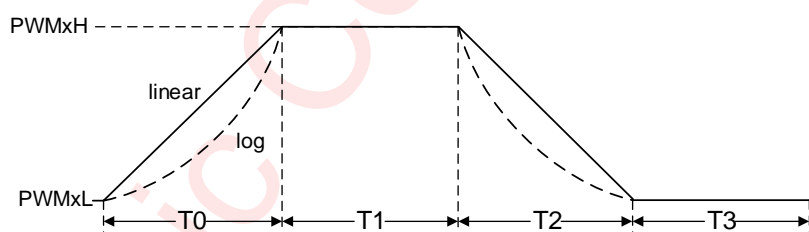


Figure 24 LED Breath Timing in Pattern Mode

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0~T3, which is set by bits LB[1:0] in register PATxT2 (x=0~2, page0, address=0x38, 0x3C, 0x40). The end point of the loop can only be selected between the end of T0 and the end of T2, which is determined by bits LE[1:0] in register PATxT2 (x=0~2). The repeat times are determined by the end point defined. If bits LE[1:0] are not "00", the end point of breathing loop is the end of T0, and the loop counter increment by 1 at the end of T0. If bits LE[1:0] are "00", the loop end point is the end of T2, and the loop counter increment by 1 at the end of T2.

The repeat times are decided by bits LT[11:8] in register PATxT2x (x=0~2) and register PATxT3.LT[7:0] (x=0~2, page0, address=0x39, 0x3D, 0x41). When setting LT[11:0] to "0", the breathing pattern will run unlimited times. After the breathing pattern is over, the status bit PATFLG in register PATxCFG (x=0~2) will be set to "1", and PATFLG will be cleared to "1" after reading out through SPI bus. Once breathing loop start again or pattern controller switches to manual mode by setting PATMD bit to "0", the PATFLG will also be cleared.

When bit RUNx in register PATGO (x=0~2, page0, address=0x45) is set to "1", breathing pattern x is started. The full process of the autonomous breathing is as follows:

- a) Set GCC, SL and PWMxH/L parameter.

- b) Set Page 3 (PAT choice registers) to select the pattern of LEDs.
- c) Configure PATxT0, PATxT1, PATxT2, PATxT3 (x=0~2) to control the breath time, start/stop point, and repeat times.
- d) Set PATEN=1 to enable breathing pattern mode.
- e) Set PATMD=1 and RAMPE=1 to select auto breathing mode and enable breathing ramp (x=0~2).
- f) Set LOGEN to select the breathing in log curve mode or linear mode (x=0~2).
- g) Set RUNx=1 to start the breath pattern x (x=0~2).

MANUAL CONTROL MODE

If bit PATMD is set to "0", manual control mode is selected. In manual control mode, user could set the bit SWITCH of register PATxCFG (x=0~2) to control the output of pattern controller. When SWITCH is "1", the output of pattern controller is decided by register PWMxH (x=0~2). When bit SWITCH is set to "0", the output is the decided by register PWMxL (x=0~2).

If bit RAMPE in register PATxCFG (x=0~2) is set to "1", the smooth ramp up/down will be enabled. At the same time, if SWITCH changes from "0" to "1", the output will be ramp up to PWMxH (x=0~2) smoothly. Similarly, if SWITCH changes from "1" to "0", the output of the pattern controller will ramp down to PWMxL (x=0~2) smoothly. It's also support the logarithmic mode ramp.

However, if RAMPE is set to "0", the output of the pattern controller will change to PWMxH or PWMxL(x=0~2) directly with no ramp as the SWITCH changes.

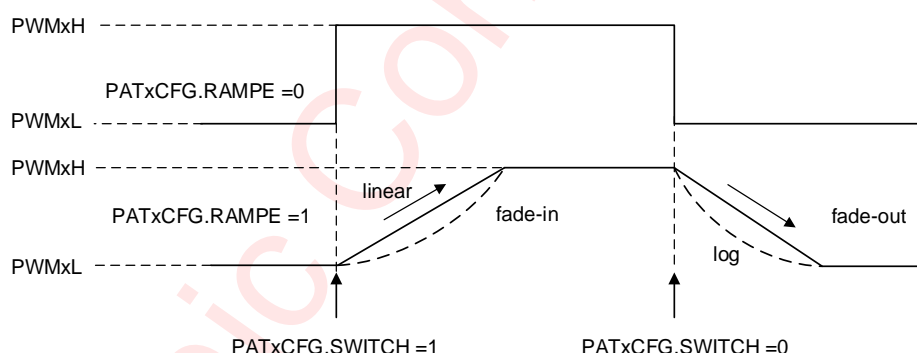


Figure 25 Manual Control Mode

MULTIPLE DEVICE SYNCHRONIZATION

AW20216S supports multiple device synchronization to drive more than 216 LEDs by cascade of multiple devices. In this application, all devices share a common clock, one device works as a master to output common clock on pin SYNC, and other devices work as slave to use external input clock from pin SYNC. Bit CLKOE and CLKSEL in Register SSCR (page0, address=0x28) select the clock input or output on pin SYNC.

CLKOE	CLKSEL	Device Clock Selection
0	0	Use Internal clock and pin SYNC is high-Z
1	0	Master, use internal clock and output it on pin SYNC
0	1	Slave, use external clock from pin SYNC
1	1	Forbidden

REGISTER CONFIGURATION

REGISTER CONTROL

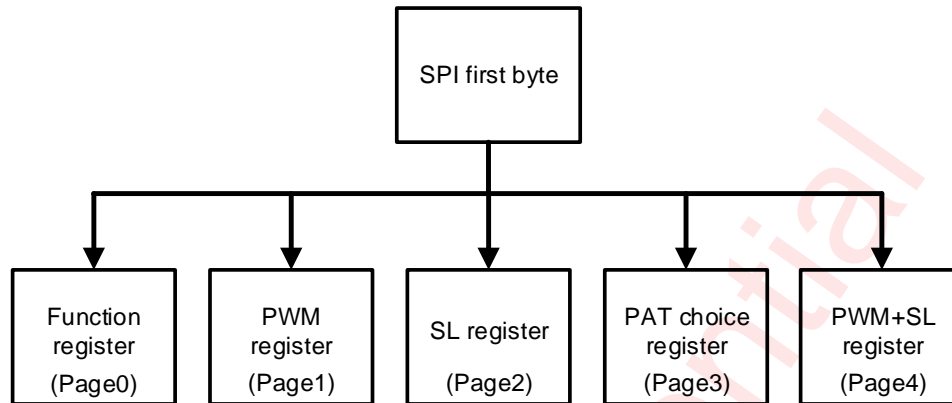


Figure 26 Register Control

AW20216S have five pages, and user can choose page0~page4 by changing first byte of SPI. The page0 is activated by default. The page4 is a virtual page that can configure PWM and SL in the same time, and the address auto-increases by one after the PWM and SL data are written. The page4 only supports writing, and is available when register MIXCR.PAGE4EN (page0, address=0x46) is set to “1”.

REGISTER LIST

Page0: Function Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
s0x00	GCR	R/W	SWSEL				-	OSDE		CHIPEN	0xB0
0x01	GCCR	R/W	GCC								0x00
0x02	DGCR	R/W	PUDIS	-			PDMD	SWPDR			0x44
0x03 ~ 0x26	OSR0 ~ OSR35	R	-		LED0~LED215 Open/Short status register					0x00	
0x27	OTCR	R/W	OTFLG	OTPD	OTDIS	TRFLG	TRTH		TROF		0x00
0x28	SSCR	R/W	CLKOE	CLKSEL	-	SSE	SRR		CLT		0x00
0x29	PCCR	R/W	PWMFRQ			-			PSEL		0x00
0x2A	UVCR	R/W	REXT_ST		OCPH	OCPD	PUST	UVFLG	UVPD	UVDIS	0x00
0x2B	SRCR	R/W	-		OTH	-		SRR	SRF		0x02
0x2F	RSTN	R/W	RSTN/ID								0x70
0x30	PWMH0	R/W	PWMH0								0x00
0x31	PWMH1	R/W	PWMH1								0x00
0x32	PWMH2	R/W	PWMH2								0x00
0x33	PWML0	R/W	PWML0								0x00
0x34	PWML1	R/W	PWML1								0x00
0x35	PWML2	R/W	PWML2								0x00
0x36	PAT0T0	R/W	T0				T1				0x00

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x37	PAT0T1	R/W	T2				T3				0x00
0x38	PAT0T2	R/W	LE		LB		LT[11:8]				0x00
0x39	PAT0T3	R/W	LT[7:0]								0x00
0x3A	PAT1T0	R/W	T0				T1				0x00
0x3B	PAT1T1	R/W	T2				T3				0x00
0x3C	PAT1T2	R/W	LE		LB		LT[11:8]				0x00
0x3D	PAT1T3	R/W	LT[7:0]								0x00
0x3E	PAT2T0	R/W	T0				T1				0x00
0x3F	PAT2T1	R/W	T2				T3				0x00
0x40	PAT2T2	R/W	LE		LB		LT[11:8]				0x00
0x41	PAT2T3	R/W	LT[7:0]								0x00
0x42	PAT0CFG	R/W	-		PATFLG	LOGEN	SWITH	RAMPE	PATMD	PATEN	0x00
0x43	PAT1CFG	R/W	-		PATFLG	LOGEN	SWITH	RAMPE	PATMD	PATEN	0x00
0x44	PAT2CFG	R/W	-		PATFLG	LOGEN	SWITH	RAMPE	PATMD	PATEN	0x00
0x45	PATGO	R/W	-	PAT2ST	PAT1ST	PAT0ST	-	RUN2	RUN1	RUN0	0x00
0x46	MIXCR	R/W	-					PAGE4EN	LPEN	-	0x02
0x4D	SDCR	R/W	-					SDCR			0x00

Page1: PWM Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	PWM0	R/W	PWM0								0x00
0x01	PWM1	R/W	PWM1								0x00
...	...	R/W	...								0x00
0xD7	PWM215	R/W	PWM215								0x00

Page2: SL Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	SL0	R/W	SL0								0x00
0x01	SL1	R/W	SL1								0x00
...	...	R/W	...								0x00
0xD7	SL215	R/W	SL215								0x00

Page3: PAT Choice Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	PATG0	R/W	-		PAT2		PAT1		PAT0		0x00
0x01	PATG1	R/W	-		PAT5		PAT4		PAT3		0x00
...	...	R/W	-			0x00
0x47	PATG71	R/W	-		PAT215		PAT214		PAT213		0x00

Page4: PWMx+SLx Register List

ADDR	NAME	R/W	Bit15	Bit14	...	Bit8	Bit7	Bit6	...	Bit0	Default
0x00	PWM0+ SL0	W	PWM0				SL0				0x00
0x01	PWM1+ SL1	W	PWM1				SL1				0x00
...	...	W				0x00
0xD7	PWM215+ SL215	W	PWM215				SL215				0x00

REGISTER DETAILED DESCRIPTION

GCR: Global Control Register (Page 0: Address 0x00)

Bit	Symbol	R/W	Description	Default
7:4	SWSEL	R/W	Active the SW number select 0000: SW1 active SW2~SW12 not active 0001: SW1~SW2 active SW3~SW12 not active 0010: SW1~SW3 active SW4~SW12 not active 0011: SW1~SW4 active SW5~SW12 not active 0100: SW1~SW5 active SW6~SW12 not active 0101: SW1~SW6 active SW7~SW12 not active 0110: SW1~SW7 active SW8~SW12 not active 0111: SW1~SW8 active SW9~SW12 not active 1000: SW1~SW9 active SW10~SW12 not active 1001: SW1~SW10 active SW11~SW12 not active 1010: SW1~SW11 active SW12 not active 1011~1111: SW1~SW12 active	1011
3	RESERVED	R	Reserved	0
2:1	OSDE	R/W	Open/short detect enable 0x: Detect disable 10: Short detect 11: Open detect	00
0	CHIPEN	R/W	Chip enable 0: Disable 1: Enable	0

GCCR: Global Current Control Register (Page 0: Address 0x01)

Bit	Symbol	R/W	Description	Default
7:0	GCC	R/W	Global current control	0x00

DGCR: De-ghost Control Register (Page 0: Address 0x02)

Bit	Symbol	R/W	Description	Default
7	PUDIS	R/W	8kΩ CSx pull up resistance disable (x=1~18): 0: Enable all the time 1: Disable	0
6:4	RESERVED	R	Reserved	100
3	PDMD	R/W	Pull down mode select 0: Only in SWx off time (x=1~12) 1: All the time	0
2:0	SWPDR	R/W	SW pull down resistance select 000: Disable pull down resistance 001: 0.25kΩ 010: 0.5kΩ 011: 1 kΩ 100: 2 kΩ 101: 4 kΩ 110: 8 kΩ 111: 16 kΩ	100

OSR0~OSR35: Open/Short Status Register (Page 0: Address 0x03~0x26)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	R	Reserved	00
5:0	OSR	R	Open/short status of LED0~LED215 0: Open/short not happen 1: Open/short happen	000000

OTCR: Over Temperature Control Register (Page 0: Address 0x27)

Bit	Symbol	R/W	Description	Default
7	OTFLG	R	Over temperature flag 0: Over-temperature not happen 1: Over-temperature happen	0
6	OTPD	R/W	Over-temperature(OT) protect disable 0: OT protect enable, when OT event occurs, device will clear GCR.CHIPEN to 0. 1: OT protect disable	0
5	OTDIS	R/W	Over-temperature detect disable 0: OT detect enable, when OT event occurs, OTCR.OTFLAG will be set. 1: OT detect disable	0

Bit	Symbol	R/W	Description	Default
4	TRFLG	R	Thermal roll off status 0: Roll off not happen 1: Roll off happen	0
3:2	TRTH	R/W	Thermal roll threshold 00: 140°C 01: 120°C 10: 100°C 11: 90°C	00
1:0	TROF	R/W	Thermal roll off percentage of I _{OUT} 00: 100% 01: 75% 10: 55% 11: 30%	00

SSCR: Spread Spectrum Control Register (Page 0: Address 0x28)

Bit	Symbol	R/W	Description	Default
7	CLKOE	R/W	Clock output enable 0: Disable 1: Enable	0
6	CLKSEL	R/W	0: Use internal 16MHz OSC clock 1: Use clock input from pin SYNC	0
5	RESERVED	R	Reserved	0
4	SSE	R/W	Spread spectrum enable 0: Disable 1: Enable	0
3:2	SSR	R/W	Spread spectrum range 00: ±5% 01: ±15% 10: ±25% 11: ±35%	00
1:0	CLT	R/W	Spread spectrum cycle time 00: 1980μs 01: 1200μs 10: 820μs 11: 660μs	00

PCCR: PWM Clock Control Register (Page 0: Address 0x29)

Bit	Symbol	R/W	Description	Default
7:5	PWMFRQ	R/W	PWM frequency selection 000: 62.5kHz 001: 32.25kHz 010: 15.6kHz 011: 7.8kHz 100: 3.9kHz 101: 1.95kHz 110: 977Hz 111: 488Hz	000
4:2	RESERVED	R	Reserved	000
1:0	PSEL	R/W	PWM phase selection 00: Phase delay mode 01: Phase inverting mode 1x: Three-phase mode	00

UVCR: UVLO Control Register (Page 0: Address 0x2A)

Bit	Symbol	R/W	Description	Default
7:6	REXT_ST	R	REXT status 00: Normal 10: REXT is open 01: REXT is short or OCP 11: Not defined	00
5	OCPTH	R/W	OCP threshold 0: 75mA 1: 120mA	0
4	OCPD	R/W	OCP disable 0: Enable OCP 1: Disable OCP	0
3	PUST	R	Power-up reset status 0: Power-up reset not happen 1: Power-up reset happen	0
2	UVFLG	R	UVLO status 0: UVLO not happen 1: UVLO happen	0
1	UVPD	R/W	UVLO protect disable 0: UVLO protect enable, when under-voltage event occurs, device will clear GCR.CHIPEN to 0. 1: UVLO protect disable	0
0	UVDIS	R/W	UVLO detect disable 0: UVLO detect enable, when under-voltage event occurs, UVCR.UVFLG will be set. 1: UVLO detect disable	0

SRCR: Open/Short Control Register (Page 0: Address 0x2B)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	R	Reserved	00
5	OTH	R/W	Open threshold 0: 0.1V 1: 0.2V	0
4:3	RESERVED	R	Reserved	0
2	SRR	R/W	Slew rate control for LED output rising time 0: 1ns 1: 6ns	0
1:0	SRF	R/W	Slew rate control for LED output falling time 00: 1ns 01: 3ns 10: 6ns 11: 10ns	10

RSTN: Reset Register (Page 0: Address 0x2F)

Bit	Symbol	R/W	Description	Default
7:0	RSTN	R/W	Write 0xAE to the register will reset all registers to their default value. The chip ID will be read out from the register.	0x70

PWMH0~PWMH2: Maximum Brightness for Auto Breath (Page 0: Address 0x30~0x32)

Bit	Symbol	R/W	Description	Default
7:0	PWMH	R/W	Maximum brightness configure for auto breath.	0x00

PWML0~PWML2: Minimum Brightness for Auto Breath (Page 0: Address 0x33~0x35)

Bit	Symbol	R/W	Description	Default
7:0	PWML	R/W	Minimum brightness configure for auto breath.	0x00

PAT0T0~PAT2T0: Pattern Timer 0 (Page 0: Address 0x36 0x3A 0x3E)

Bit	Symbol	R/W	Description				Default
7:4	T0	R/W	Ramp rise time				0000
			T0	Time	T0	Time	
			0000	0s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	
3:0	T1	R/W	Hold on time				0000
			T1	Time	T1	Time	
			0000	0.04s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	

PAT0T1~PAT2T1: Pattern Timer 1 (Page 0: Address 0x37 0x3B 0x3F)

Bit	Symbol	R/W	Description				Default
7:4	T2	R/W	Ramp fall time				0000
			T2	Time	T2	Time	
			0000	0s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	

Bit	Symbol	R/W	Description	Default
3:0	T3	R/W	Hold off time	0000
			T3 Time T3 Time	
			0000 0.04s 1000 2.1s	
			0001 0.13s 1001 2.6s	
			0010 0.26s 1010 3.1s	
			0011 0.38s 1011 4.2s	
			0100 0.51s 1100 5.2s	
			0101 0.77s 1101 6.2s	
			0110 1.04s 1110 7.3s	
			0111 1.6s 1111 8.3s	

PAT0T2~PAT2T2: Pattern Control Register 1 (Page 0: Address 0x38 0x3C 0x40)

Bit	Symbol	R/W	Description	Default
7:6	LE	R/W	End point of the auto-breath loop pattern 00: Pattern finally stop at OFF state Other: Pattern finally stop at ON state	00
5:4	LB	R/W	Start point of the auto-breath loop pattern 00: Pattern start from RISE state 01: Pattern start from ON state 10: Pattern start from FALL state 11: Pattern start from OFF state	00
3:0	LT[11:8]	R/W	4 MSB of auto-breath loop times	0000

PAT0T3~PAT2T3: Pattern Control Register 2 (Page 0: Address 0x39 0x3D 0x41)

Bit	Symbol	R/W	Description	Default
7:0	LT[7:0]	R/W	8 LSB of auto-breath loop times Note: when LT[11:0]=0, the pattern will run forever. In this case, you can switch auto-breath mode to manual mode and then turn the pattern off.	0x00

PAT0CFG~PAT2CFG: Configure Register (Page 0: Address 0x42~0x44)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	R	Reserved	00
5	PATFLG	R	Auto breath pattern loop end flag 0: Loop is not over 1: Loop is over	0

Bit	Symbol	R/W	Description	Default
4	LOGEN	R/W	Log curve output enable 0: Disable 1: Enable	0
3	SWITCH	R/W	Switch on or off at manual mode. 0: LED off 1: LED on	0
2	RAMPE	R/W	PAT ramp enable 0: Ramp disable 1: Ramp enable	0
1	PATMD	R/W	Breath pattern control mode selection 0: Manual mode 1: Auto breath pattern mode	0
0	PATEN	R/W	Auto breath pattern controller enable 0: Disable 1: Enable	0

PATGO: Start Control Register (Page 0: Address 0x45)

Bit	Symbol	R/W	Description	Default
7	RESERVED	R	Reserved	0
6	PAT2ST	R	Auto breath pattern 2 status 0: Pattern is stop 1: Pattern is running	0
5	PAT1ST	R	Auto breath pattern 1 status 0: Pattern is stop 1: Pattern is running	0
4	PAT0ST	R	Auto breath pattern 0 status 0: Pattern is stop 1: Pattern is running	0
3	RESERVED	R	Reserved	0
2	RUN2	R/W	Auto breath pattern 2 run control Write "1" to run auto breath pattern Note: You shall write "0" and then write "1" to this bit to restart a new auto breath pattern.	0
1	RUN1	R/W	Auto breath pattern 1 run control Write "1" to run auto breath pattern Note: You shall write "0" and then write "1" to this bit to restart a new auto breath pattern.	0
0	RUN0	R/W	Auto breath pattern 0 run control Write "1" to run auto breath pattern Note: You shall write "0" and then write "1" to this bit to restart a new auto breath pattern.	0

MIXCR: Mix Function Control Register (Page 0: Address 0x46)

Bit	Symbol	R/W	Description	Default
7:3	RESERVED	R	Reserved	00000
2	PAGE4EN	R/W	Page 4 enable 0: Disable 1: Enable	0
1	LPEN	R/W	Low-power mode enable 0: Disable 1: Enable	1
0	RESERVED	R	Reserved	0

SDCR: SW Drive Capability Register (Page 0: Address 0x4D)

Bit	Symbol	R/W	Description	Default
7:3	RESERVED	R	Reserved	00000
2:0	SDCR	R/W	Select the SW drive capability 000: 0.99A 100: 1.61A 001: 1.08A 101: 1.72A 010: 1.19A 110: 1.85A 011: 1.32A 111: 2.00A	000

PWMx (x=0~215): PWM Configure Register (Page 1: Address 0x00~0xD7)

Bit	Symbol	R/W	Description	Default
7:0	PWMx	R/W	PWM modulated	0x00

SLx (x=0~215): SL Configure Register (Page 2: Address 0x00~0xD7)

Bit	Symbol	R/W	Description	Default
7:0	SLx	R/W	Control the constant current	0x00

PATGx (x=0~71): PAT Choice Register (Page 3: Address 0x00~0x47)

Bit	Symbol	R/W	Description	Default
7:6	RESERVED	R	Reserved	00

Bit	Symbol	R/W	Description	Default
5:4	PAT3x+2	R/W	Control the patterns of LED 3x+2: 00: PWM parameter comes from PWM register 01: PWM parameter comes from pattern controller 0 10: PWM parameter comes from pattern controller 1 11: PWM parameter comes from pattern controller 2	00
3:2	PAT3x+1	R/W	Control the patterns of LED 3x+1: 00: PWM parameter comes from PWM register 01: PWM parameter comes from pattern controller 0 10: PWM parameter comes from pattern controller 1 11: PWM parameter comes from pattern controller 2	00
1:0	PAT3x	R/W	Control the patterns of LED 3x: 00: PWM parameter comes from PWM register 01: PWM parameter comes from pattern controller 0 10: PWM parameter comes from pattern controller 1 11: PWM parameter comes from pattern controller 2	00

PWMx+SLx (x=0~215): PWM and SL Configure Register (Page 4: Address 0x00~0xD7)

Bit	Symbol	R/W	Description	Default
15:8	PWMx	W	PWM modulated	0x00
7:0	SLx	W	Control the constant current	0x00

APPLICATION INFORMATION

If the equipment has antenna, the IC should be far away from the antenna in order to avoid the EMI.

R_{EXT}

The selection of R_{EXT} determined the maximum LED0~LED215 current I_{max} as described in below formula (1).

$$I_{max} = \frac{K}{R_{EXT}} \quad (1)$$

When R_{EXT} = 10KΩ, I_{max} = 40mA, I_{switch} = 720mA, SDCR[2:0] = 000 (page0, address = 0x4D)

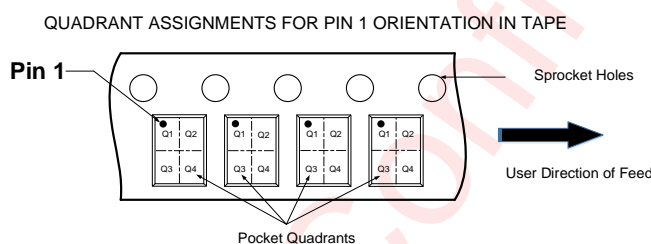
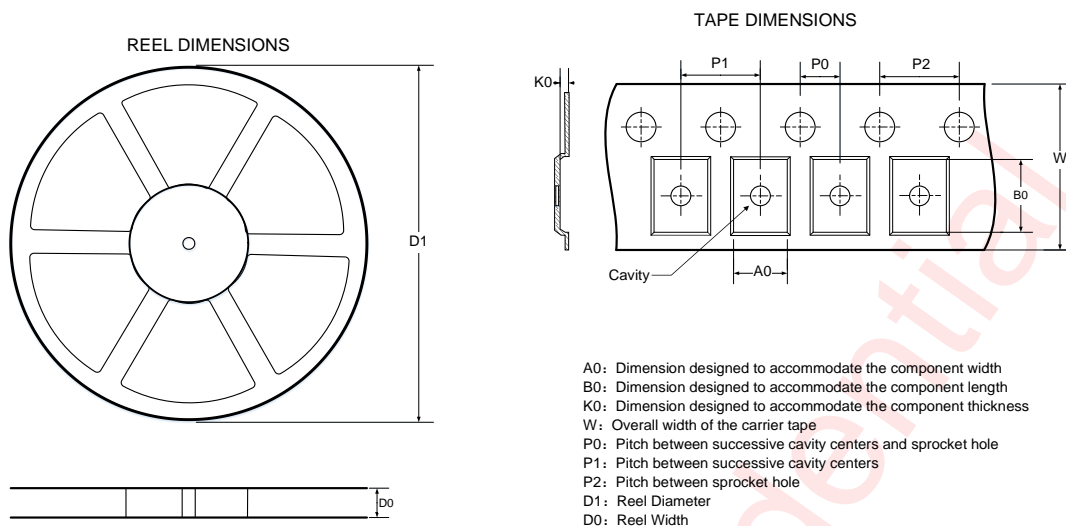
When R_{EXT} = 5KΩ, I_{max} = 80mA, I_{switch} = 1.44A, SDCR[2:0] = 111 (page0, address = 0x4D).

PCB LAYOUT CONSIDERATION

AW20216S is an 18x12 matrix LED driver programmed via an SPI compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C₁、C₂、C₃、C₄、C₅ should be placed as close to the chip as possible.
2. The R_{EXT} should be placed as close to the chip as possible.
3. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal via as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

TAPE AND REEL INFORMATION

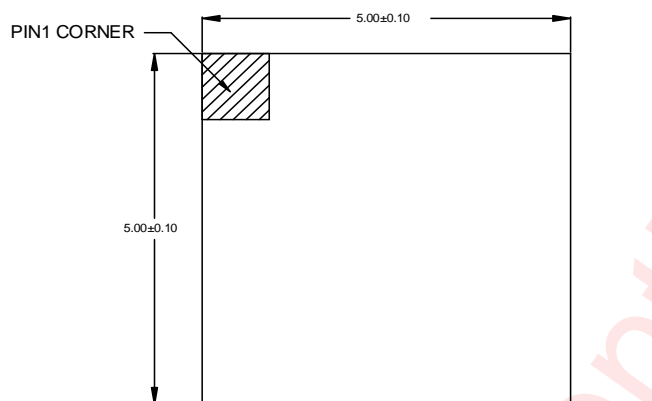


DIMENSIONS AND PIN1 ORIENTATION

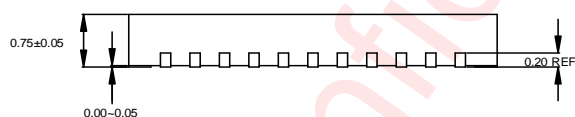
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	5.3	5.3	1.1	2	8	4	12	Q1

All dimensions are nominal

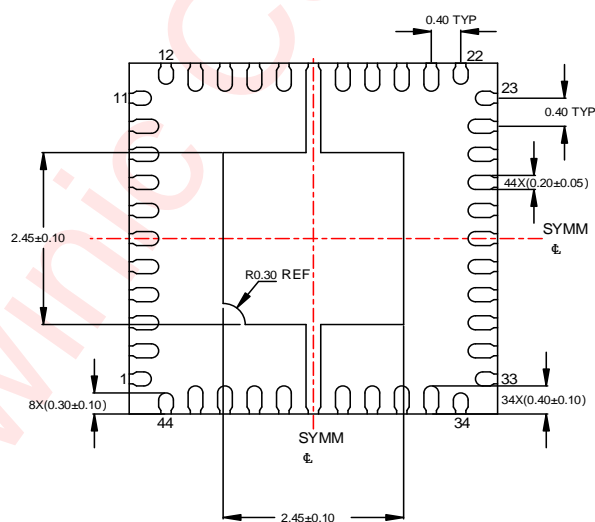
PACKAGE DESCRIPTION



Top View



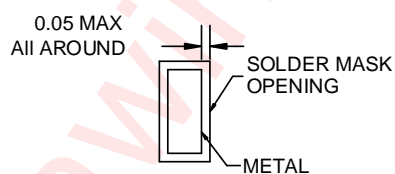
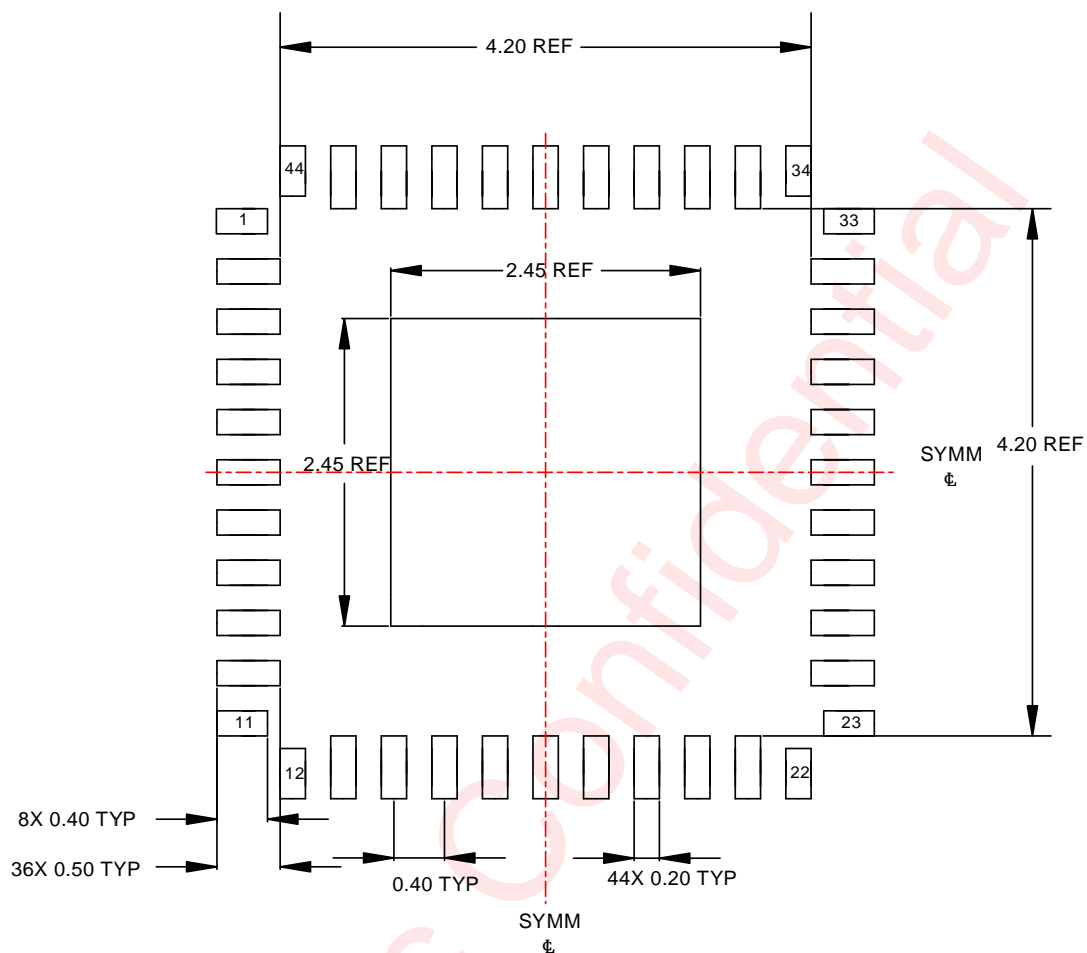
Side View



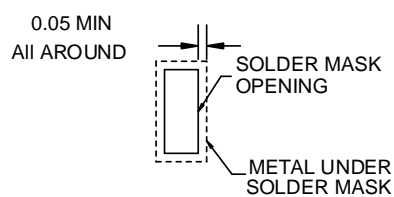
Bottom View

Unit: mm

LAND PATTERN DATA



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Apr. 2020	Officially released
V1.1	Jun. 2020	Add the EMI reduction description -- page20 Modify the register control description -- page23 Modify the CHIP ID -- page23 Add optional SW drive capability register description -- page33 Add application information description -- page35
V1.2	Oct. 2020	Add the Notes in application -- page35
V1.3	Mar. 2021	Update the description of typical application circuit -- page2 Update the description of De-Ghost Function -- page20
V1.4	Dec. 2021	Add the Max time of T_{DO} -- page10
V1.5	Feb. 2022	Modify the application circuit -- page2
V1.6	Nov. 2022	Corrected the formula of the DUTY --page18
V1.7	May. 2023	Corrected Typical Application Circuits --page2,4&5 Corrected Recommended Operating Conditions --page7 Corrected the default value of bit LPEN of register MIXCR(0x46) --page24&33 Corrected the description of bit OCPTH of register UVCR(0x2A) --page28 Corrected the formula of the DUTY --page18

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