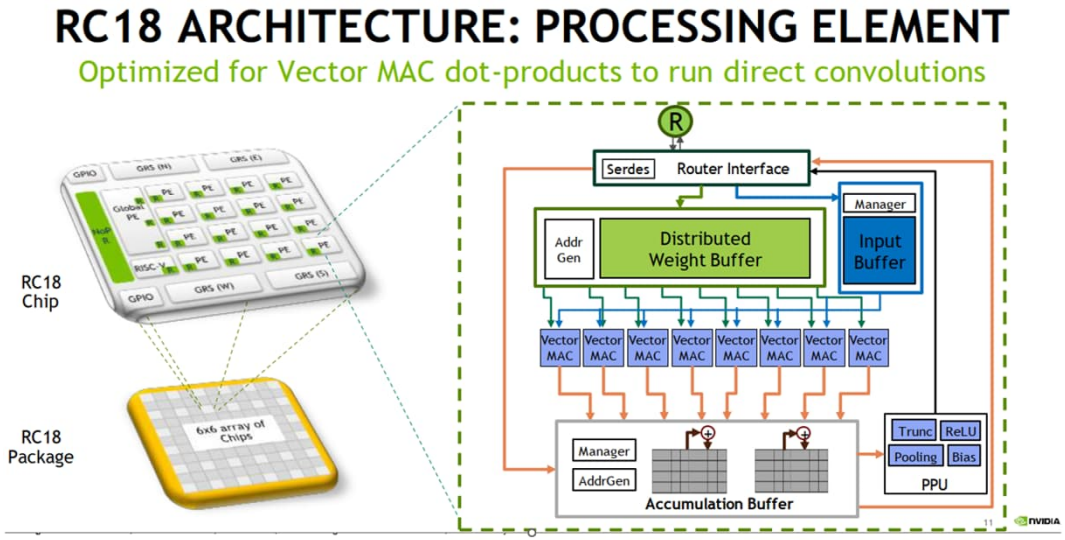
What is a “Throughput Accurate” Model?

Stuart Swan
Platform Architect
Siemens EDA
18 January 2024

SIEMENS

What is a “Throughput Accurate” Model?

- Consider an example SOC design shown here.
  - Entire chip is modeled in SystemC and implemented with HLS on a particular ASIC technology.
  - Blocks in the chip will have clocks, resets, transaction interfaces, signal interfaces, etc.
  - Clocks will have specific clock frequencies that account for target technology.
- In real chip, silicon will have gate delays.
  - HLS will implement pipelines and RTL synthesis will implement gate level logic to account for gate delays.
  - These delays will be accounted for in the RTL in a cycle accurate manner.



SIEMENS

Now, Assume Infinitely Fast Silicon…

- Consider the original SystemC model, but let's assume that the silicon is infinitely fast.
  - Keep exactly same clocks and clock frequencies as in RTL.
  - Keep exactly same transaction and signal interfaces as in RTL.
  - We do not model any latency in pipelines, since the silicon is infinitely fast.
  - Note that transactions will still stream through interfaces at the same rate as the real silicon.
  - This model is **throughput accurate** with respect to the real silicon.

Matchlib Enables Throughput Accurate Models

- Matchlib enables easy construction of throughput accurate models for pre-HLS simulation.
- This is very valuable because:
  - Performance-accurate model is available very early in design flow.
  - Much easier to debug than RTL.
  - Very high simulation performance (>30x RTL)
  - Pin level compatible with RTL.
  - Enables focus of verification and debug effort to move from RTL to pre-HLS model.
  - Post-HLS RTL model will closely match performance characteristics of pre-HLS model.

Is Matchlib Required for Throughput Accurate Models?

- Can you create a throughput accurate model in SystemC without using Matchlib?
  - Yes, but you need to code each process such that all the wait statements are manually merged.
  - Doing this is much harder, especially as designs becomes larger.
  - Model code will become complex and difficult to maintain.