CHIP DESIGN & IMPLEMENTATION

From RTL to GDSII

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This is an example slide.

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Clock Tree Synthesis (CTS)

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Layout versus Schematic (LVS)

List

- Point A

List

- Point A
- Point B

List

- Point A
- Point B
  - part 1

List

- Point A
- Point B
  - part 1
  - part 2

List

- Point A
- Point B
  - part 1
  - part 2
- Point C

List

- Point A
- Point B
  - part 1
  - part 2
- Point C
- Point D

Overlays

First Line of Text

Overlays

First Line of Text
Second Line of Text

Overlays

First Line of Text
Second Line of Text
Third Line of Text