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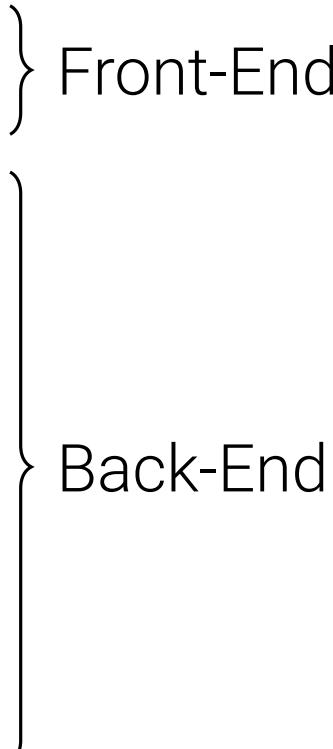
# CHIP DESIGN & IMPLEMENTATION

*From RTL to GDSII*

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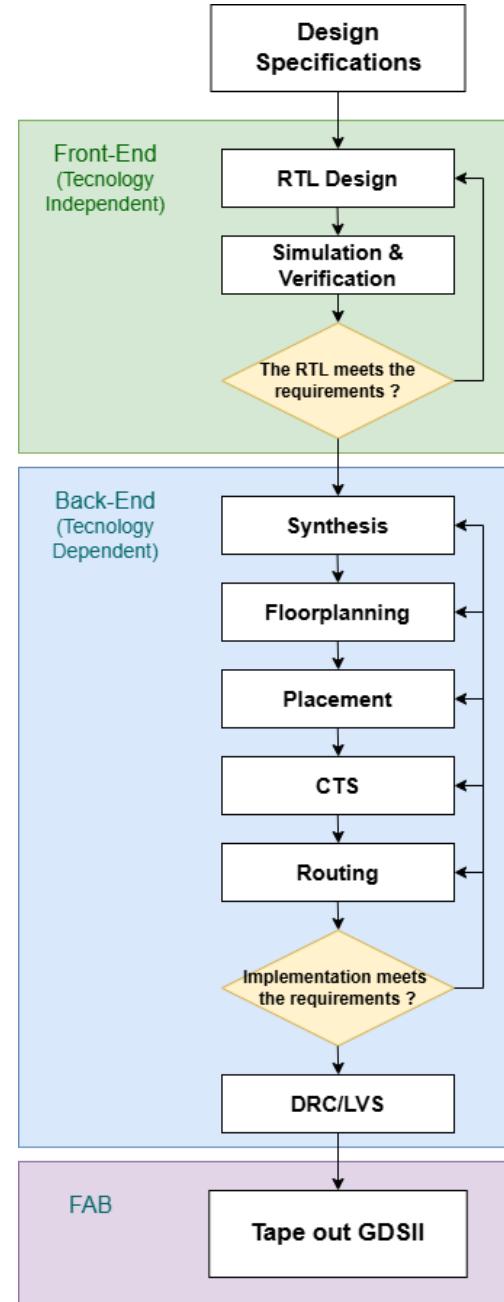
# Introduction

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## Chip Design & Implementation – From RTL to GDSII

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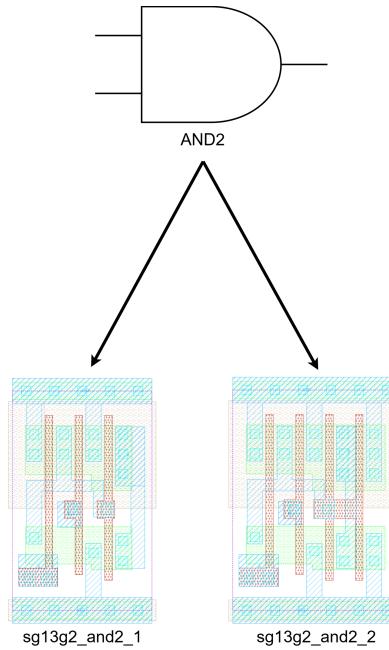
# RTL Design

# Simulation & Verification

# Physical Implementation

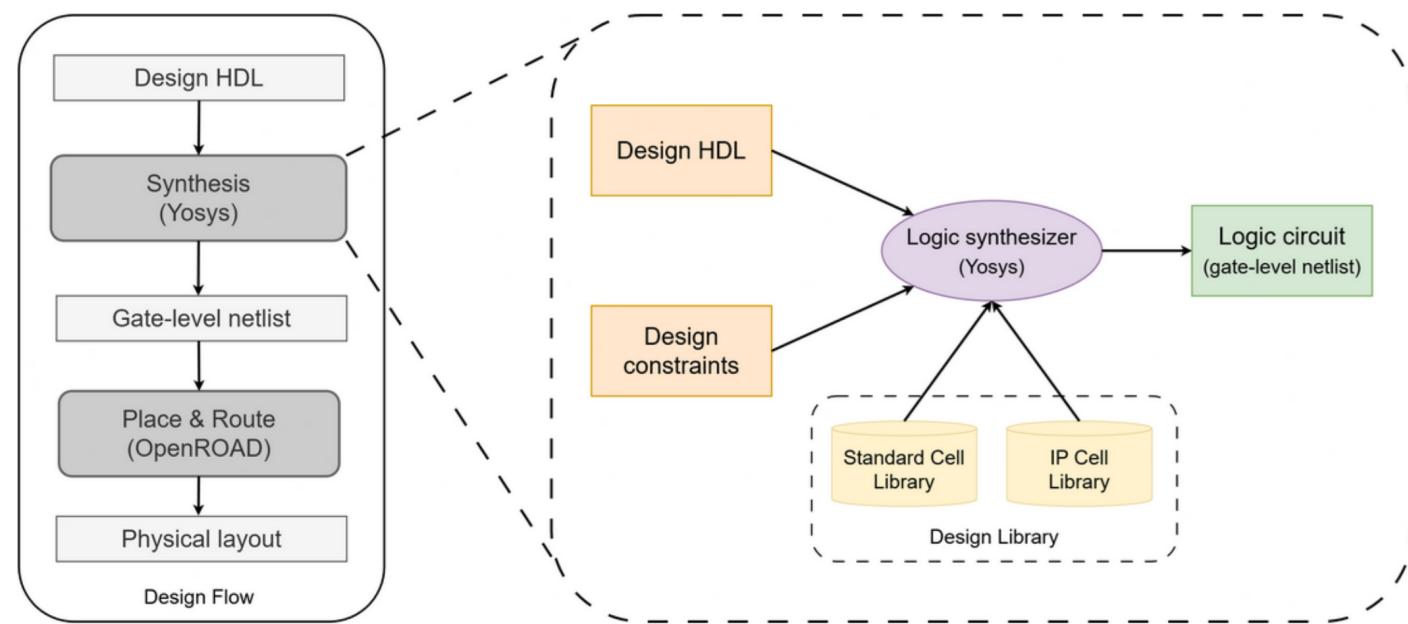
# Synthesis - Standard Cells

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



# Synthesis - Inputs & Outputs

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



# Synthesis - How it looks in the Practice?

```
module example (
    input wire clk,
    input wire rst,
    output wire y
);
    assign y = clk & ~rst;
endmodule
```

RTL code

```
module fulladd(a, b, c_in, c_out, sum);
    wire _00_;
    wire _01_;
    wire _02_;
    ...
    input [3:0] a;
    wire [3:0] a;
    ...
    assign _14_ = _07_ & ~(_13_);
    assign _15_ = _06_ & ~(_14_);
    assign c_out = _15_ | _04_;
    assign sum[0] = ~(_10_ ^ c_in);
    assign sum[1] = ~(_12_ ^ _08_);
    assign sum[2] = _14_ ^ _05_;
    assign _16_ = ~(_14_ | _05_);
    assign _17_ = _16_ | ~(_02_);
    assign sum[3] = _17_ ^ _01_;
endmodule
```

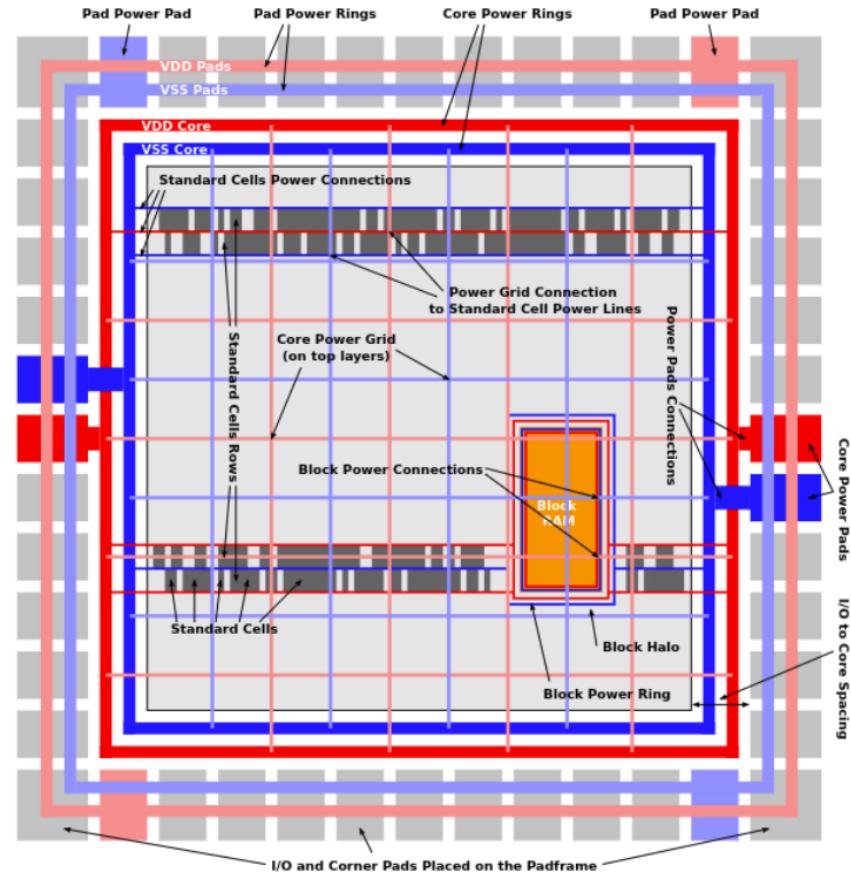
Netlist after synthesis

```
module fulladd(a, b, c_in, c_out, sum);
    wire _00_;
    wire _01_;
    wire _02_;
    ...
    output [3:0] sum;
    wire [3:0] sum;
    sg13g2_xor2_1 _61_ (
        .A(_25_), .B(_21_), .X(_42_)
    );
    sg13g2_o21ai_1 _62_ (
        .A1(_40_), .A2(_41_), .B1(_28_), .Y(_27_)
    );
    sg13g2_xnor2_1 _63_ (
        .A(_26_), .B(_35_), .Y(_43_)
    );
    sg13g2_xnor2_1 _64_ (
        .A(_36_), .B(_38_), .Y(_44_)
    );
    sg13g2_xnor2_1 _65_ (
        .A(_31_), .B(_39_), .Y(_45_)
    );
    ...
endmodule
```

Netlist after synthesis

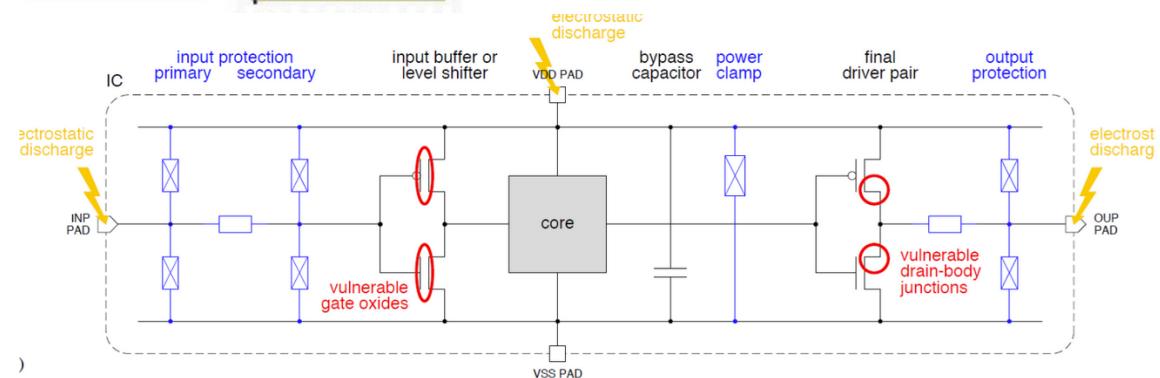
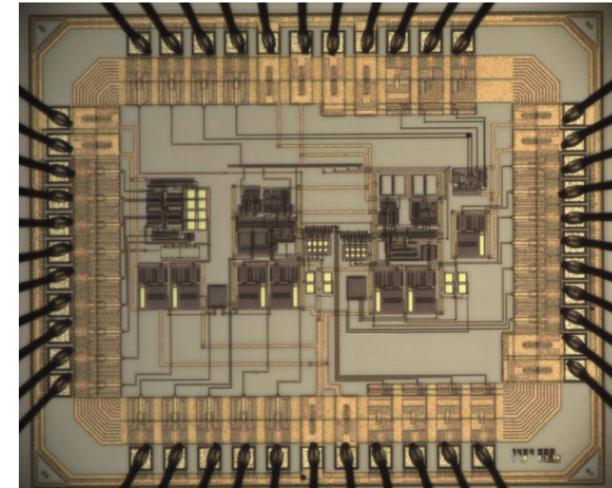
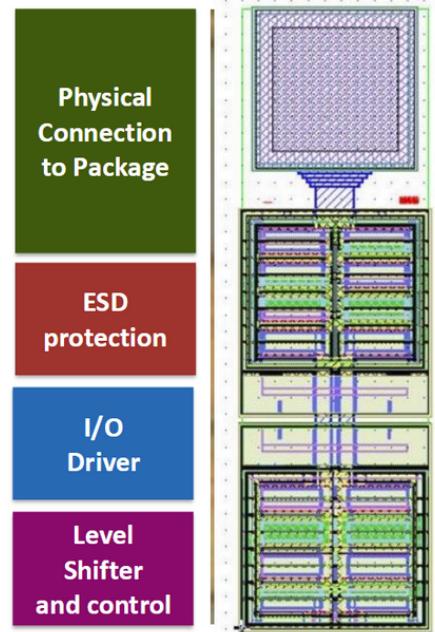
# Floorplanning

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



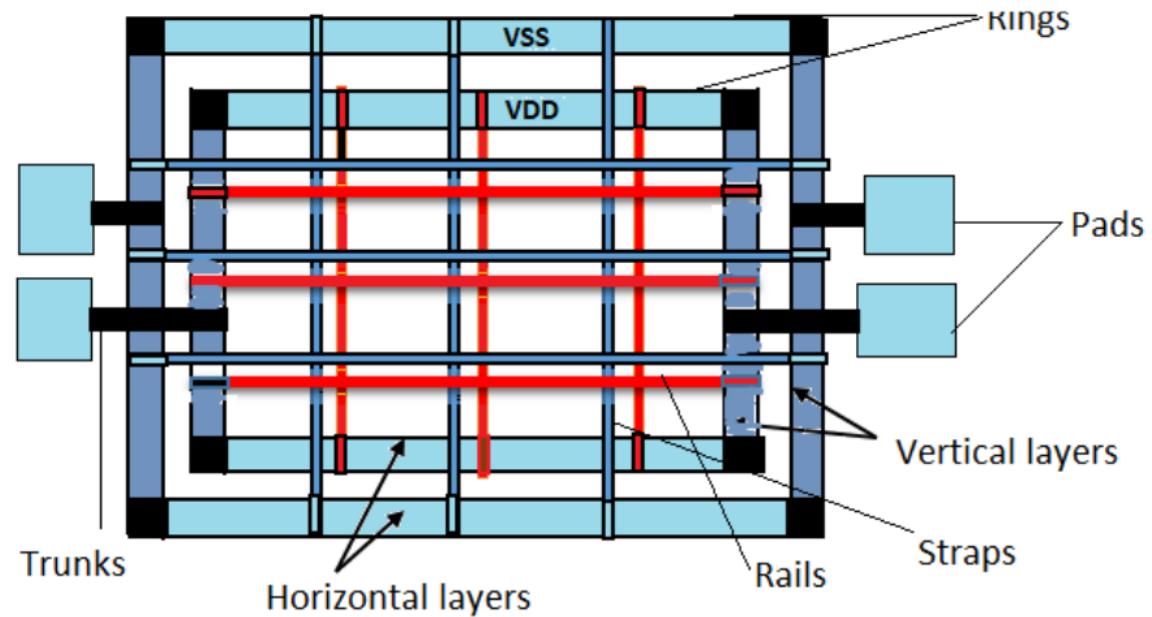
# Floorplanning - Padrino

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



# Floorplanning - Power Grid

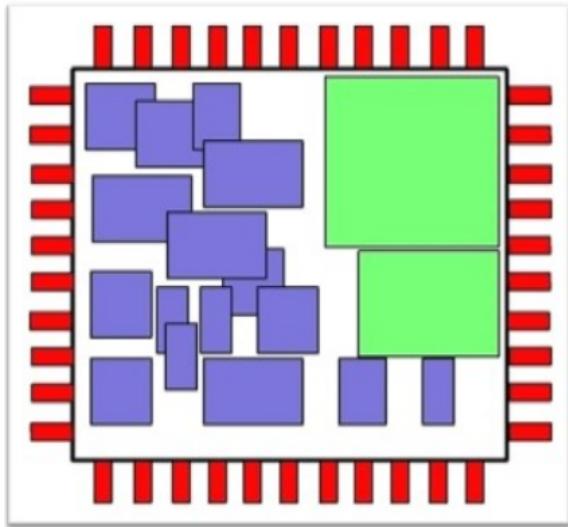
- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



# Placement

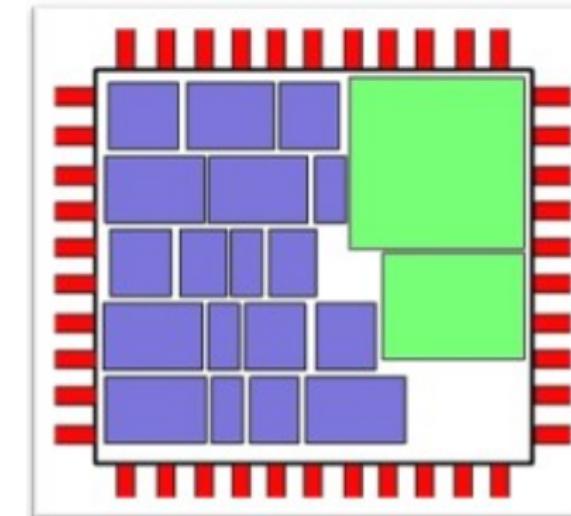
Global Placement

► qqasd



Detailed Placement

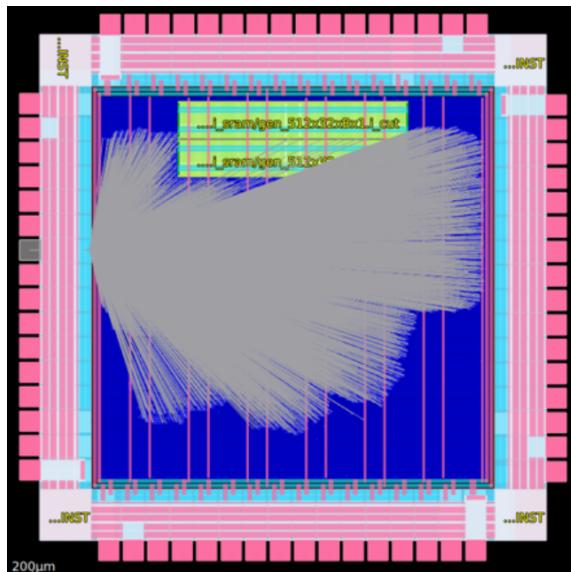
► asdasd



# Clock Tree Synthesis (CTS)

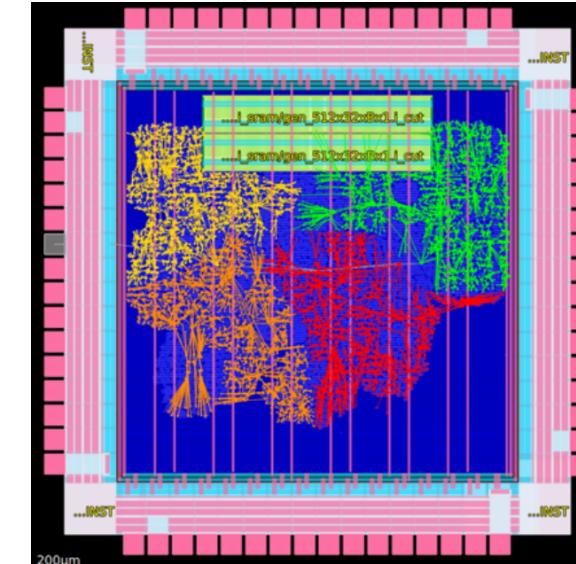
Before CTS

► qqasd

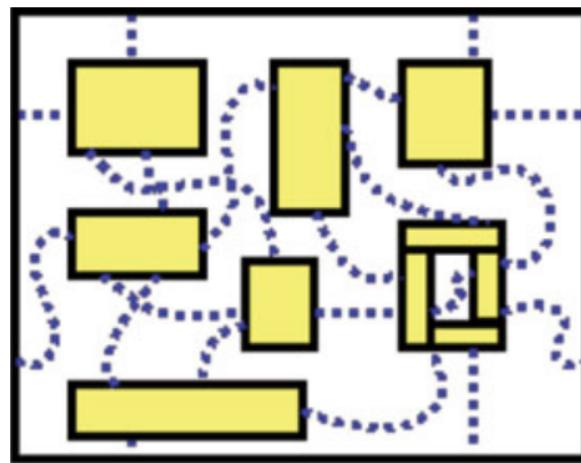


After CTS

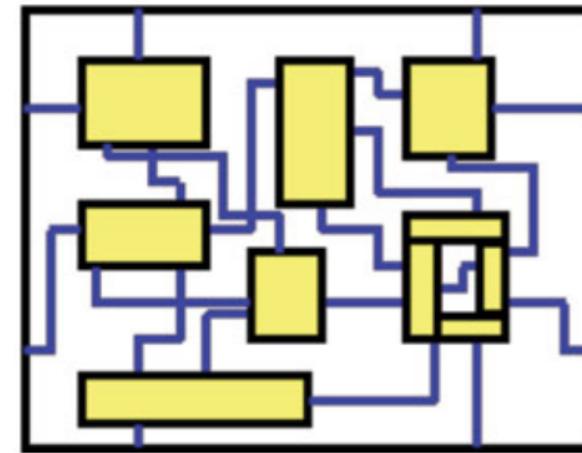
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# Routing



(a) Global routing



(b) Detailed routing

# Signoff & Tapeout

# Design Rule Check (DRC)

# Layout versus Schematic (LVS)