



Hochschule
München
University of
Applied Sciences

CHIP DESIGN & IMPLEMENTATION

From RTL to GDSII

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Front-End

Back-End

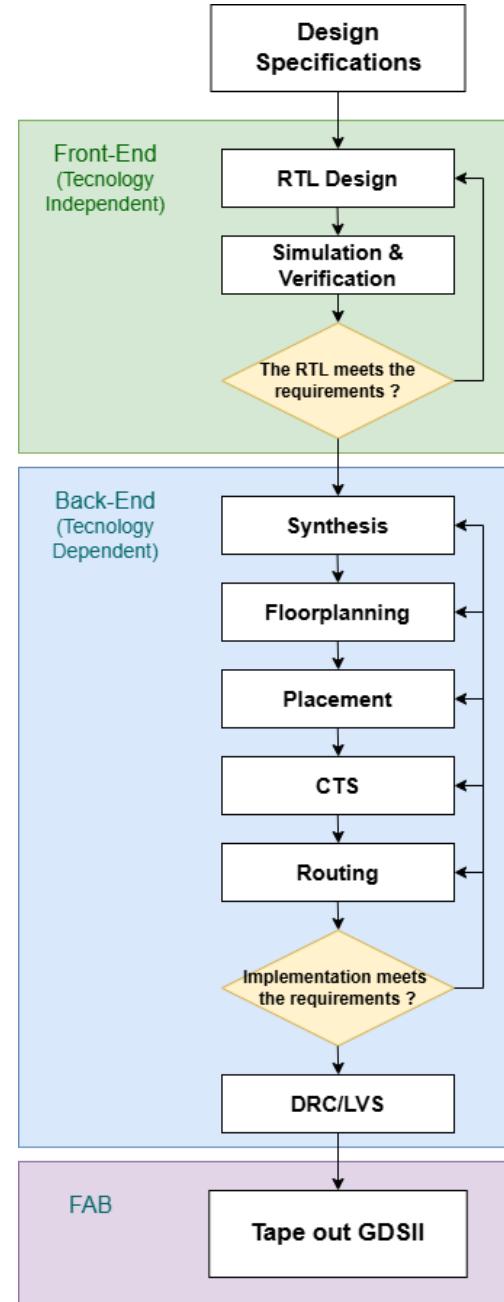
Introduction

- ▶ Bullet 1
- ▶ Bullet 2
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Chip Design & Implementation – From RTL to GDSII

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Front-End

RTL Design



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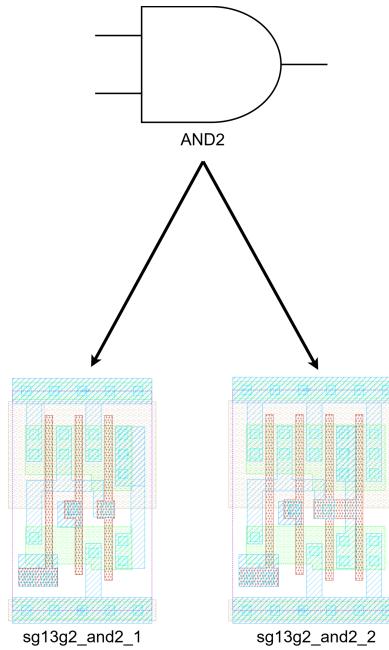
5

Simulation & Verification

Back-End

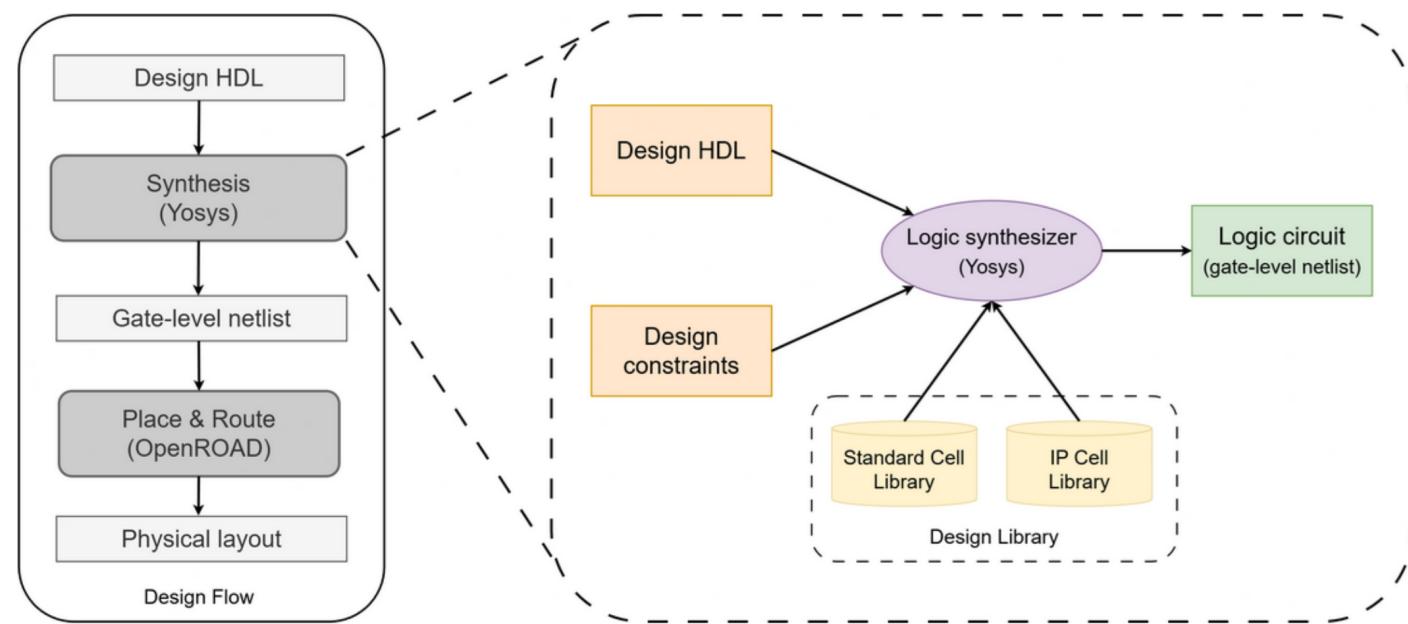
Synthesis - Standard Cells

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



Synthesis - Inputs & Outputs

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



Synthesis - How it looks in the Practice?

```
module example (
    input wire clk,
    input wire rst,
    output wire y
);
    assign y = clk & ~rst;
endmodule
```

RTL code

```
module fulladd(a, b, c_in, c_out, sum);
    wire _00_;
    wire _01_;
    wire _02_;
    ...
    input [3:0] a;
    wire [3:0] a;
    ...
    assign _14_ = _07_ & ~(_13_);
    assign _15_ = _06_ & ~(_14_);
    assign c_out = _15_ | _04_;
    assign sum[0] = ~(_10_ ^ c_in);
    assign sum[1] = ~(_12_ ^ _08_);
    assign sum[2] = _14_ ^ _05_;
    assign _16_ = ~(_14_ | _05_);
    assign _17_ = _16_ | ~(_02_);
    assign sum[3] = _17_ ^ _01_;
endmodule
```

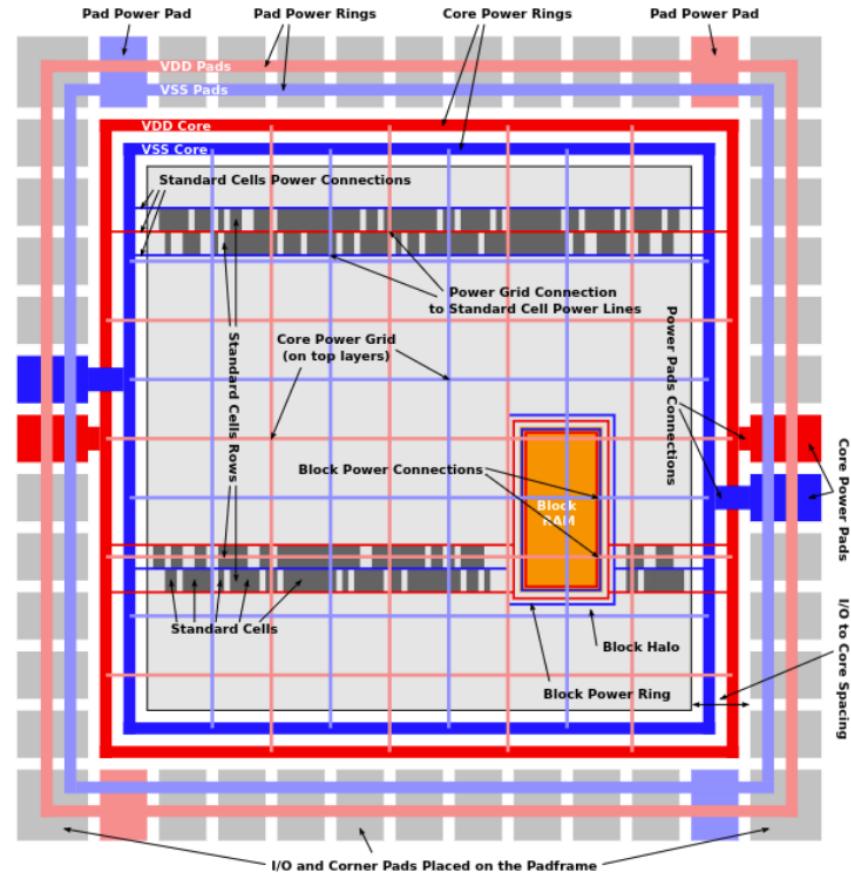
Netlist after synthesis

```
module fulladd(a, b, c_in, c_out, sum);
    wire _00_;
    wire _01_;
    wire _02_;
    ...
    output [3:0] sum;
    wire [3:0] sum;
    sg13g2_xor2_1 _61_ (
        .A(_25_), .B(_21_), .X(_42_)
    );
    sg13g2_o21ai_1 _62_ (
        .A1(_40_), .A2(_41_), .B1(_28_), .Y(_27_)
    );
    sg13g2_xnor2_1 _63_ (
        .A(_26_), .B(_35_), .Y(_43_)
    );
    sg13g2_xnor2_1 _64_ (
        .A(_36_), .B(_38_), .Y(_44_)
    );
    sg13g2_xnor2_1 _65_ (
        .A(_31_), .B(_39_), .Y(_45_)
    );
    ...
endmodule
```

Netlist after synthesis

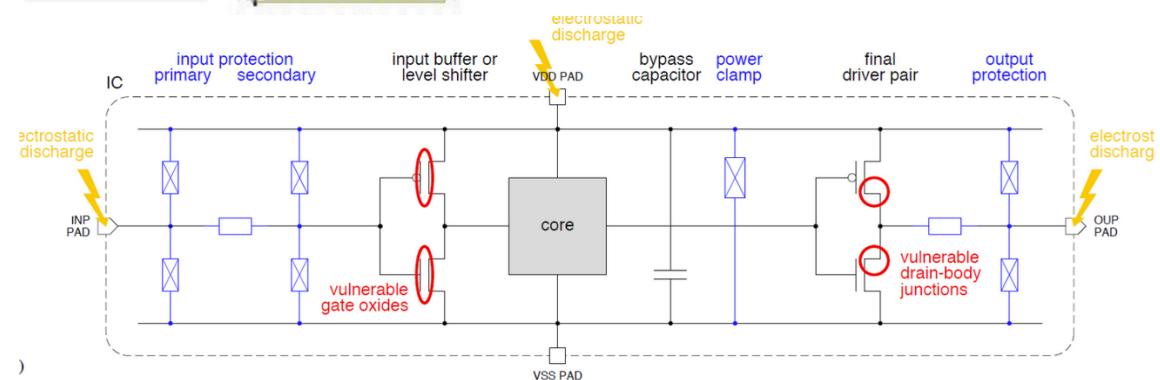
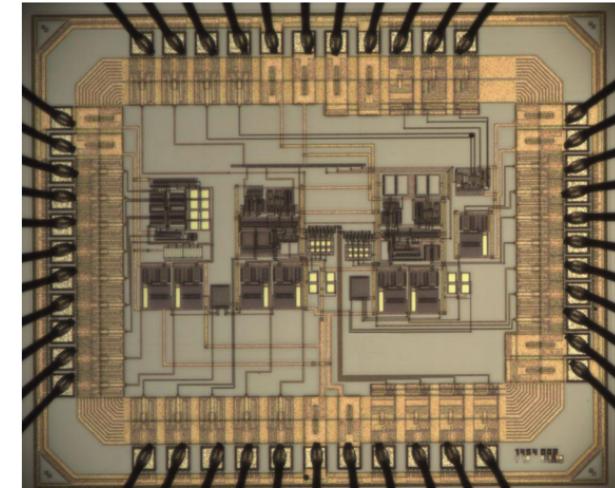
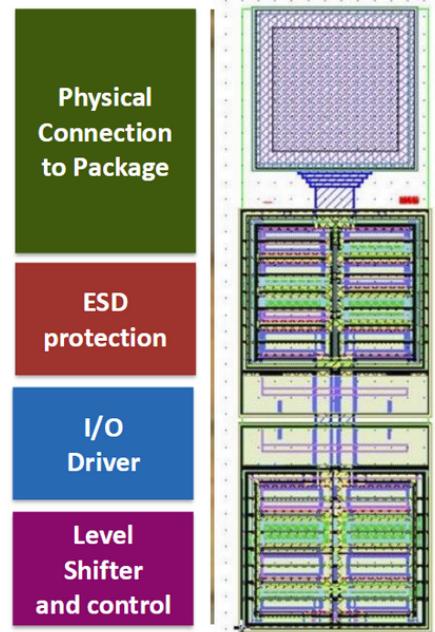
Floorplanning

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



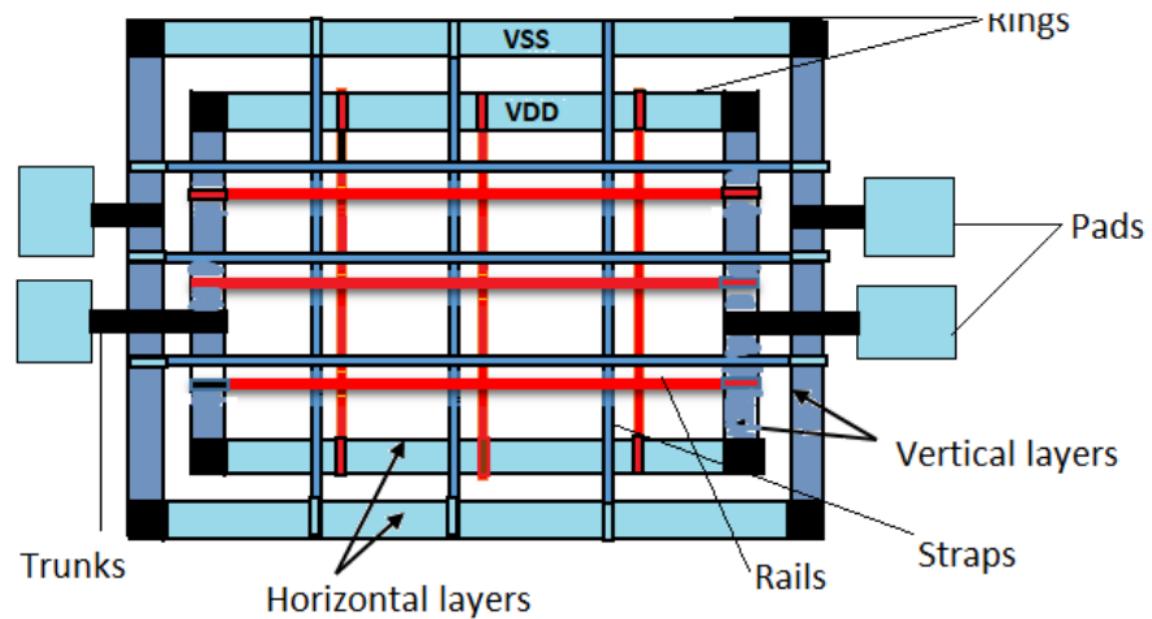
Floorplanning - Padrino

- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



Floorplanning - Power Grid

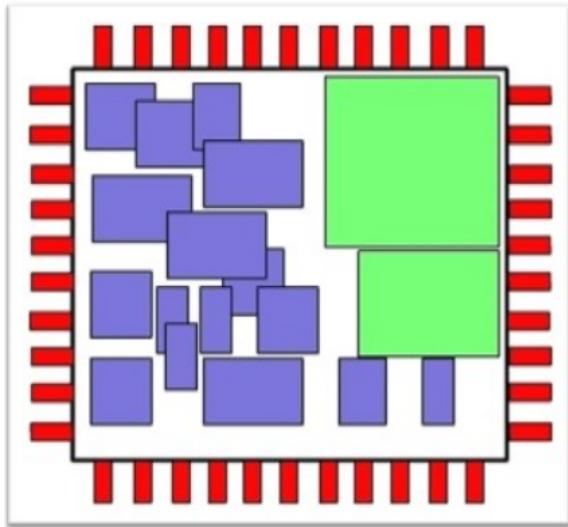
- ▶ Bullet 1
- ▶ Bullet 2
- ▶ Bullet 3



Placement

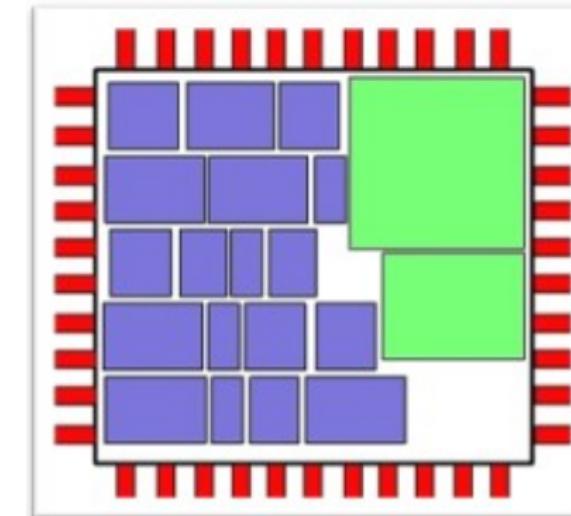
Global Placement

- ▶ qqasd



Detailed Placement

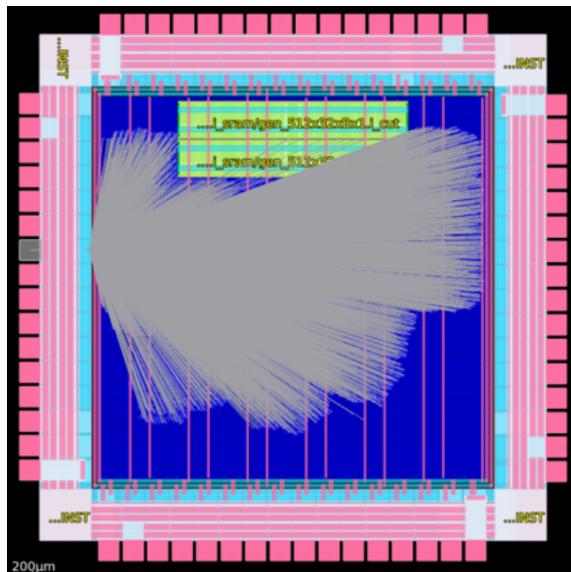
- ▶ asdasd



Clock Tree Synthesis (CTS)

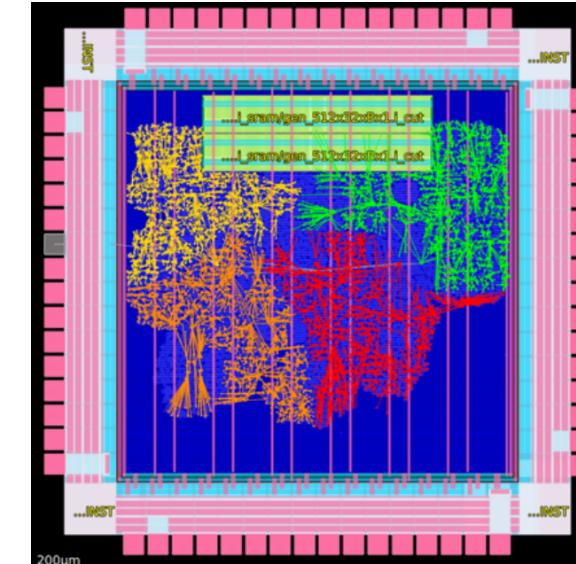
Before CTS

► qqasd

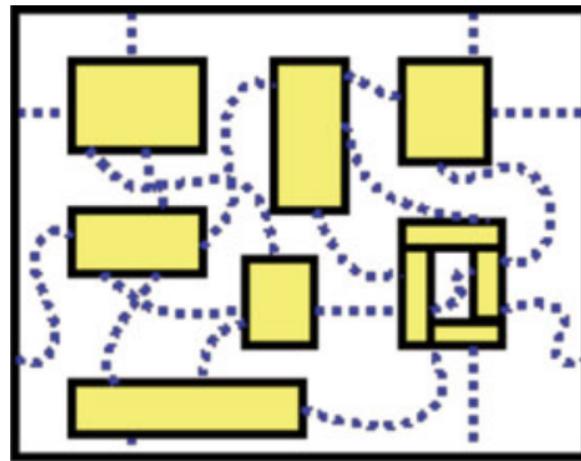


After CTS

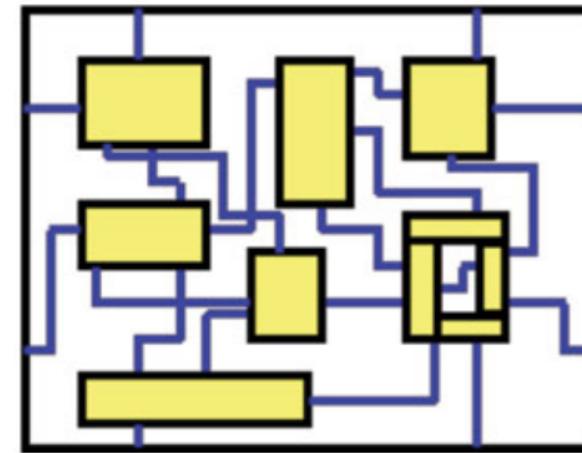
► asdasd



Routing



(a) Global routing



(b) Detailed routing

Signoff & Physical Verification

1. Timing Signoff
 - 1.1 Fill insertion
 - 1.2 RC Extraction
 - 1.3 STA post Physical Implementation
2. Physical Verification
 - 2.1 DRC
 - 2.2 LVS
3. Chip Finishing
 - 3.1 Sealring
 - 3.2 Metal Fill
 - 3.3 Others...

Timing Signoff

- ▶ Fill Insertion
 - ▶
- ▶ RC Extraction
- ▶ STA post Physical Implementation

Physical Verification - DRC

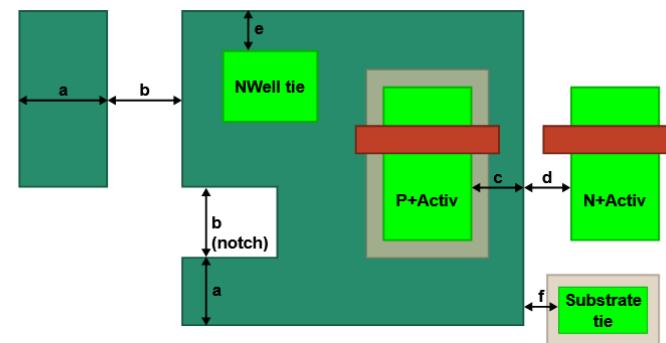
- ▶ DRC run at the fullchip level to ensure that the layout adheres to the foundry's physical rules (geometries, spacing, etc.)

5 Physical Layer Design Rules

5.1 NWell

Rule	Description	Value
NW.a	Min. NWell width	0.62
NW.b	Min. NWell space or notch (same net). NWell regions separated by less than this value will be merged.	0.62
NW.b1	Min. PWell width between NWell regions (different net) (Note 3)	1.80
NW.c	Min. NWell enclosure of P+Activ not inside ThickGateOx	0.31
NW.c1	Min. NWell enclosure of P+Activ inside ThickGateOx	0.62
NW.d	Min. NWell space to external N+Activ not inside ThickGateOx	0.31
NW.d1	Min. NWell space to external N+Activ inside ThickGateOx	0.62
NW.e	Min. NWell enclosure of NWell tie surrounded entirely by NWell in N+Activ not inside ThickGateOx	0.24
NW.e1	Min. NWell enclosure of NWell tie surrounded entirely by NWell in N+Activ inside ThickGateOx	0.62
NW.f	Min. NWell space to substrate tie in P+Activ not inside ThickGateOx	0.24
NW.f1	Min. NWell space to substrate tie in P+Activ inside ThickGateOx	0.62

Notes



Activ GatPoly NWell nBuLay pSD PWell:block

Figure 5.1: NWell dimensions (only rule variants without ThickGateOx are shown in this figure)

Physical Verification - LVS

- ▶ Extract layout (GDS) and build a SPICE netlist
 - ▶ Sometimes need to black-box sensitive layouts.
- ▶ Export RTL and synthesized netlist from earlier stages.
- ▶ Compare both netlists to ensure they match.

Chip Finishing

- ▶ Sealring
- ▶ Metal Fill

Tapeout & Fabrication