

CHIP DESIGN & IMPLEMENTATION

From RTL to GDSII

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Introduction

This is an example slide.

RTL Design

Simulation & Verification

Physical Implementation

Synthesis

Floorplanning

Placement

Clock Tree Synthesis (CTS)

Routing

Signoff & Tapeout

Design Rule Check (DRC)

Layout versus Schematic (LVS)

List

- ▶ Point A

List

- ▶ Point A
- ▶ Point B

List

- ▶ Point A
- ▶ Point B
 - ▶ part 1

List

- ▶ Point A
- ▶ Point B
 - ▶ part 1
 - ▶ part 2

List

- ▶ Point A
- ▶ Point B
 - ▶ part 1
 - ▶ part 2
- ▶ Point C

List

- ▶ Point A
- ▶ Point B
 - ▶ part 1
 - ▶ part 2
- ▶ Point C
- ▶ Point D

Overlays

First Line of Text

Overlays

First Line of Text
Second Line of Text

Overlays

First Line of Text
Second Line of Text
Third Line of Text