DDCO LAB SEM4

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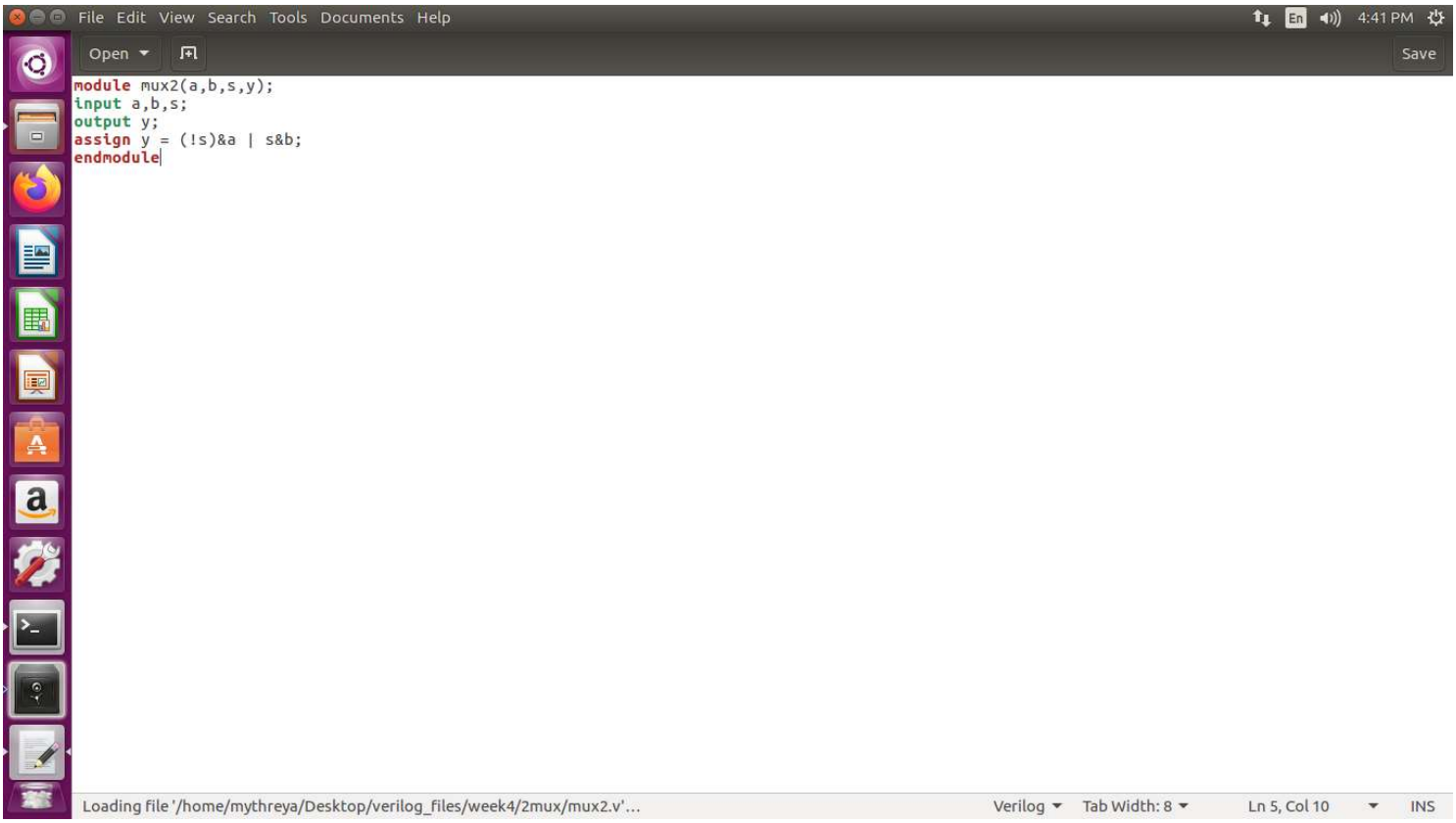
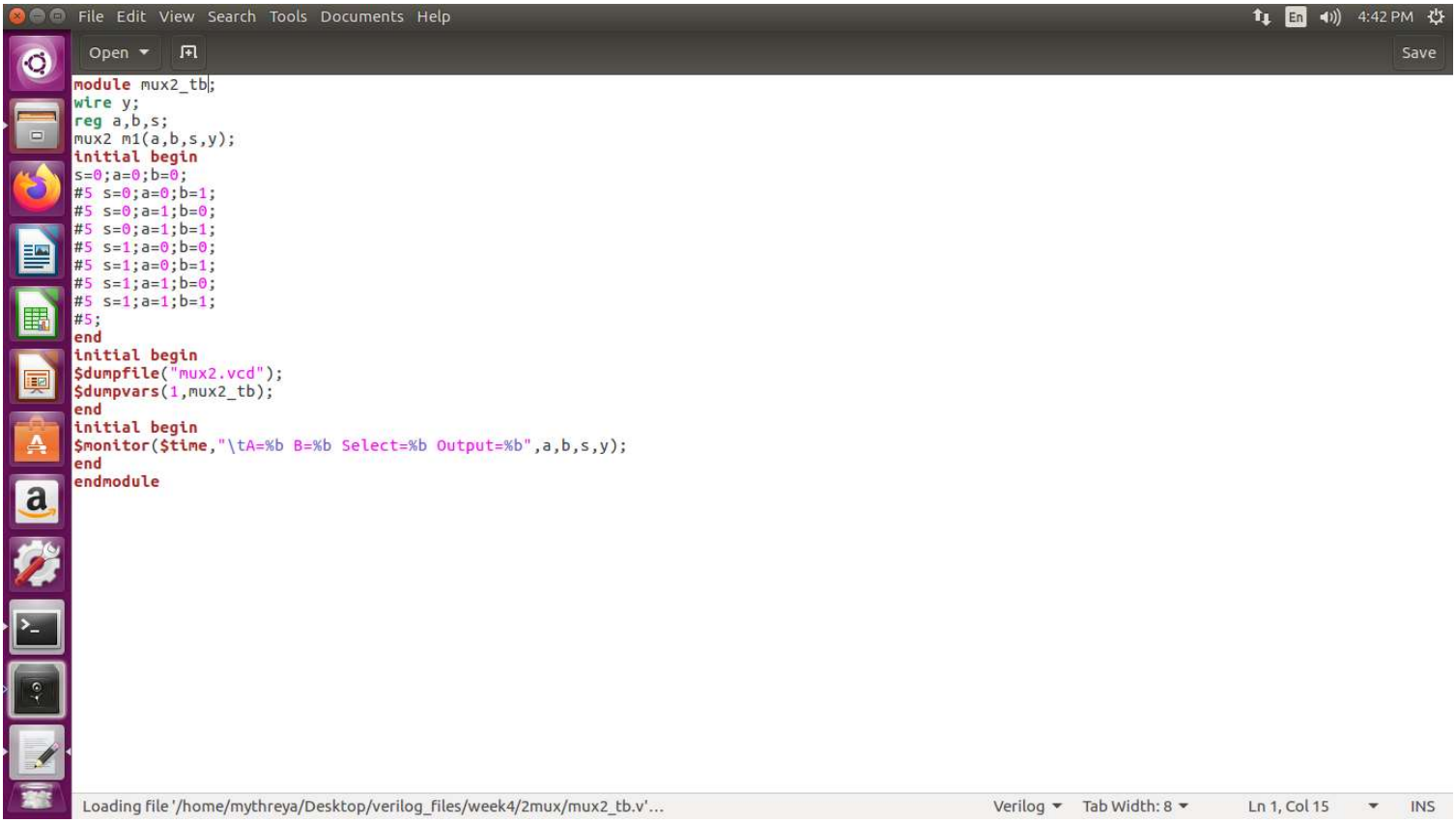
Section : C

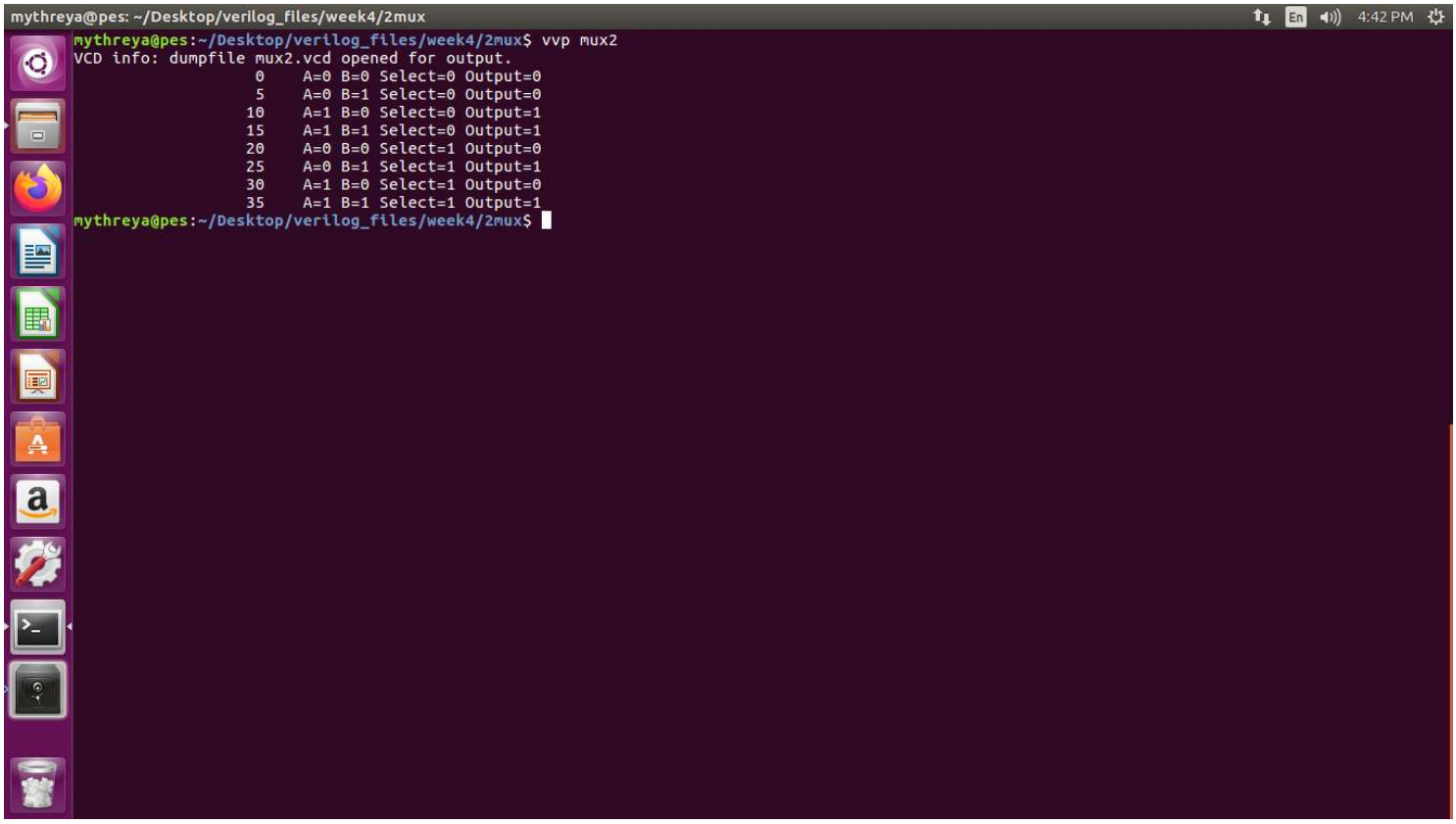
Week 4: MUX AND ALU

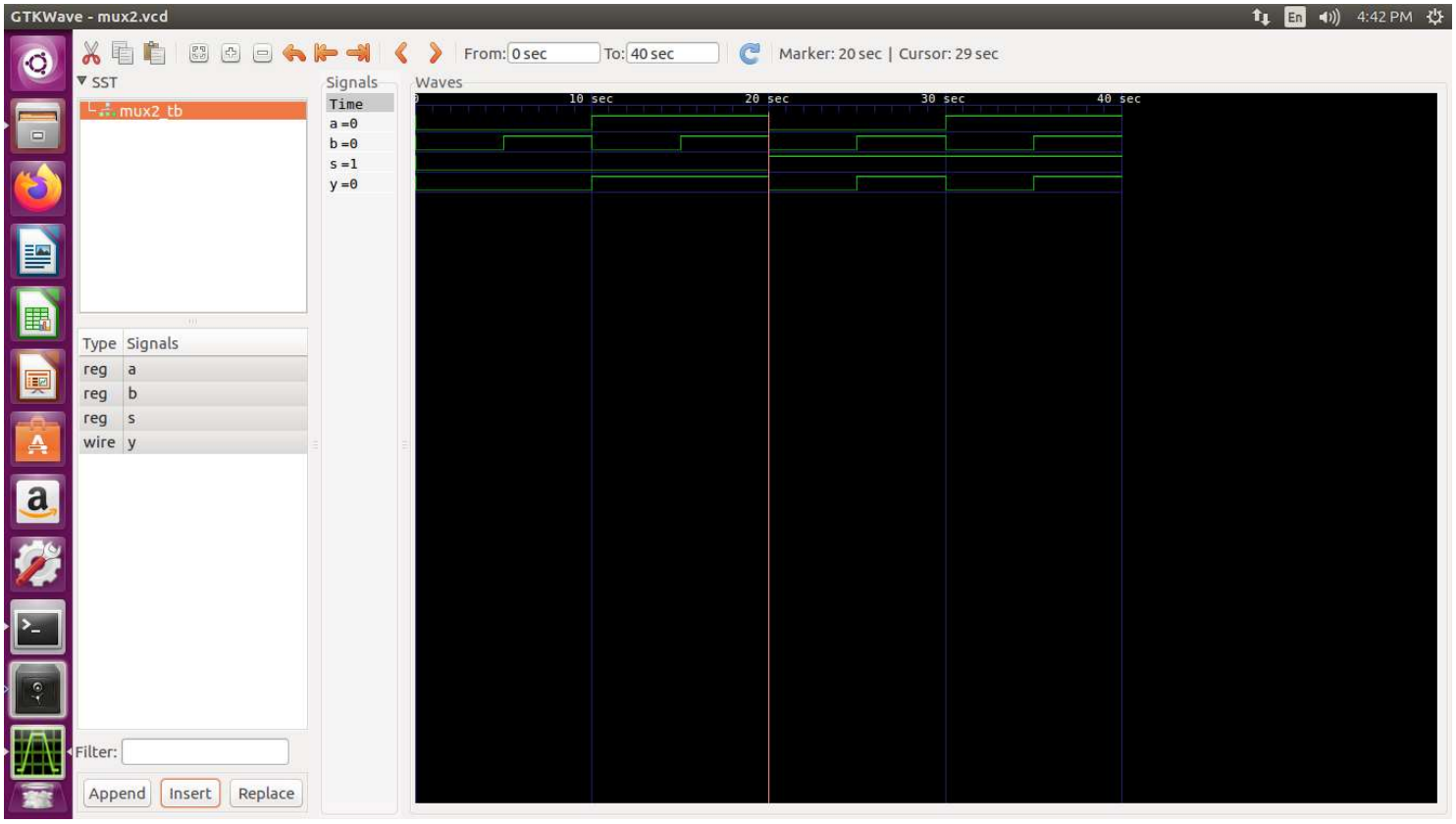
2X1 MUX





Output


mythreya@pes: ~/Desktop/verilog_files/week4/2mux
4:42 PM
mythreya@pes:~/Desktop/verilog_files/week4/2mux$ vvp mux2
VCD info: dumpfile mux2.vcd opened for output.
0 A=0 B=0 Select=0 Output=0
5 A=0 B=1 Select=0 Output=0
10 A=1 B=0 Select=0 Output=1
15 A=1 B=1 Select=0 Output=1
20 A=0 B=0 Select=1 Output=0
25 A=0 B=1 Select=1 Output=1
30 A=1 B=0 Select=1 Output=0
35 A=1 B=1 Select=1 Output=1
mythreya@pes:~/Desktop/verilog_files/week4/2mux$


GTKWave - mux2.vcd
4:42 PM
From: 0 sec
To: 40 sec
Marker: 20 sec | Cursor: 29 sec
SST
mux2_tb
Signals
Time
a =0
b =0
s =1
y =0
Waves
10 sec
20 sec
30 sec
40 sec
Type
Signals
reg a
reg b
reg s
wire y
Filter:
Append
Insert
Replace

4X1 MUX

mux4.v (~/Desktop/verilog_files/week4/4mux) - gedit

Open Save

mux4.v mux2.v

```
module mux4(a,b,c,d,s1,s2,y);
input a,b,c,d,s1,s2;
output y;
wire w1,w2;
mux2 m1(a,b,s1,w1);
mux2 m2(c,d,s1,w2);
mux2 m3(w1,w2,s2,y);
endmodule
```

Verilog Tab Width: 8 Ln 8, Col 10 INS

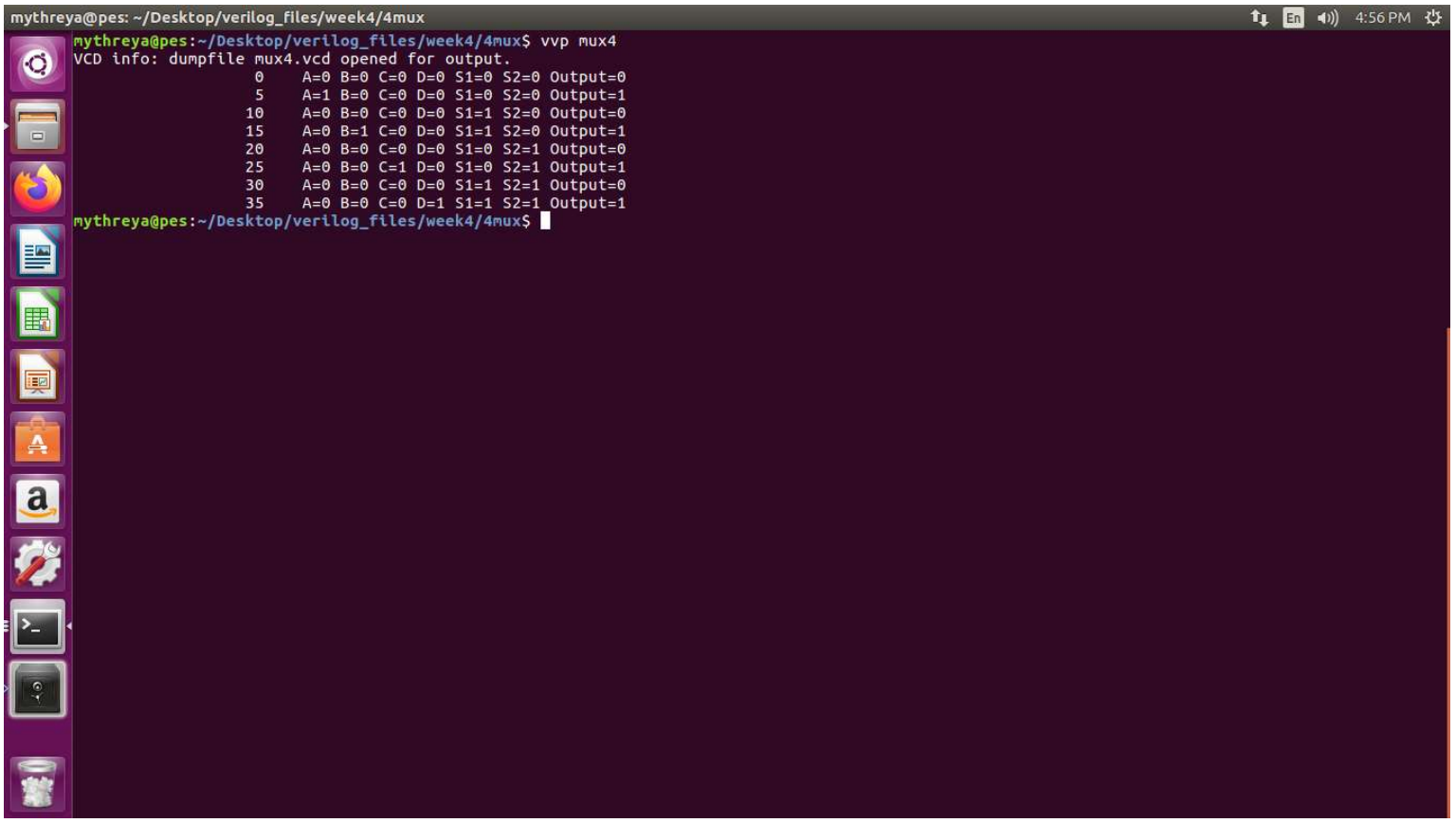
mux4_tb.v (~/Desktop/verilog_files/week4/4mux) - gedit

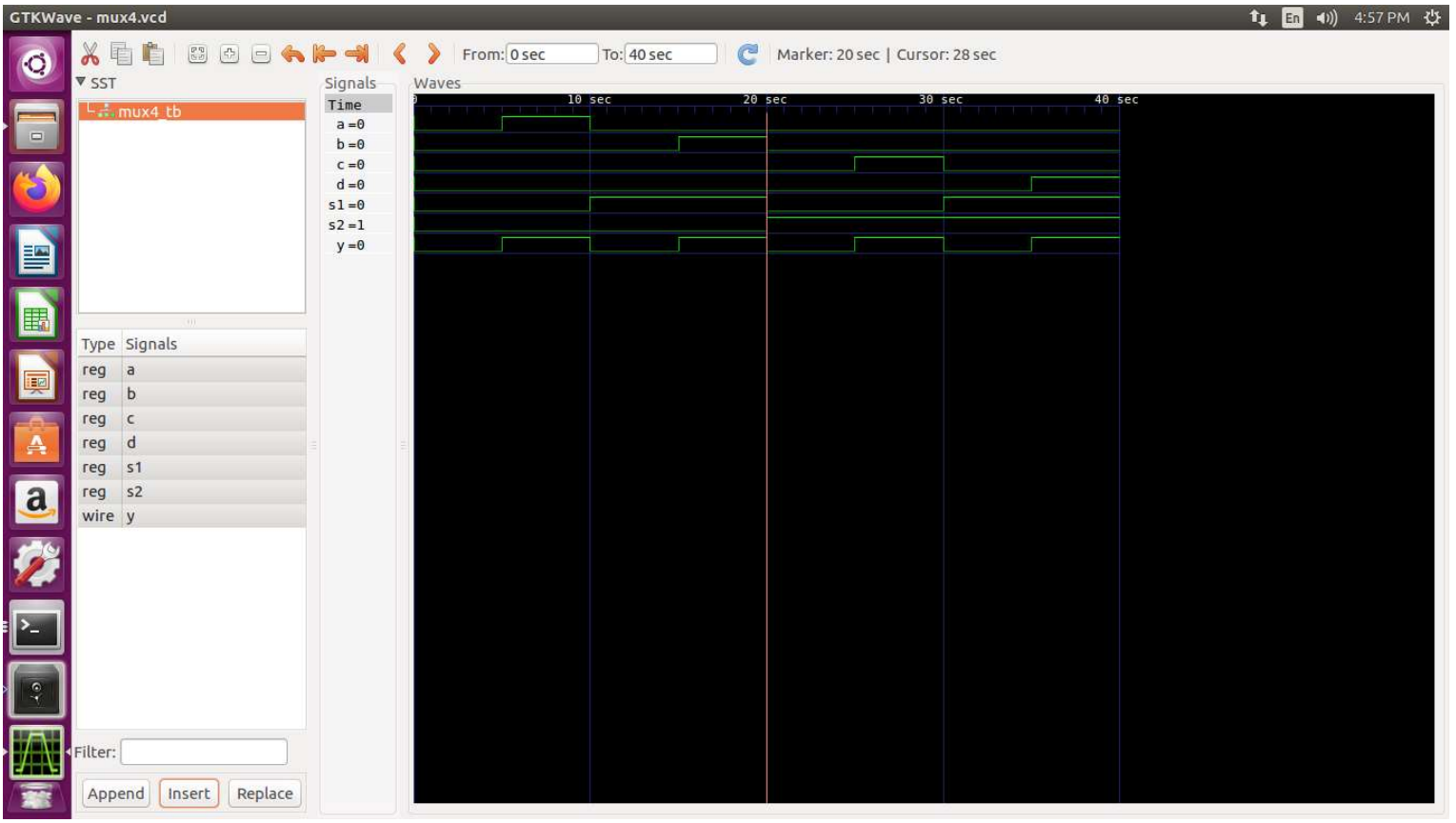
Open Save

```
module mux4_tb;
wire y;
reg a,b,c,d,s1,s2;
mux4 m1(a,b,c,d,s1,s2,y);
initial begin
s2=0;s1=0;a=0;b=0;c=0;d=0;
#5 s2=0;s1=0;a=1;b=0;c=0;d=0;
#5 s2=0;s1=1;a=0;b=0;c=0;d=0;
#5 s2=0;s1=1;a=0;b=1;c=0;d=0;
#5 s2=1;s1=0;a=0;b=0;c=0;d=0;
#5 s2=1;s1=0;a=0;b=0;c=1;d=0;
#5 s2=1;s1=1;a=0;b=0;c=0;d=0;
#5 s2=1;s1=1;a=0;b=0;c=0;d=1;
end
initial begin
$dumpfile("mux4.vcd");
$dumpvars(1,mux4_tb);
end
initial begin
$monitor($time,"\tA=%b B=%b C=%b D=%b S1=%b S2=%b Output=%b",a,b,c,d,s1,s2,y);
end
endmodule
```

Verilog Tab Width: 8 Ln 20, Col 78 INS

Output


mythreya@pes: ~/Desktop/verilog_files/week4/4mux
4:56 PM
mythreya@pes:~/Desktop/verilog_files/week4/4mux$ vvp mux4
VCD info: dumpfile mux4.vcd opened for output.
0 A=0 B=0 C=0 D=0 S1=0 S2=0 Output=0
5 A=1 B=0 C=0 D=0 S1=0 S2=0 Output=1
10 A=0 B=0 C=0 D=0 S1=1 S2=0 Output=0
15 A=0 B=1 C=0 D=0 S1=1 S2=0 Output=1
20 A=0 B=0 C=0 D=0 S1=0 S2=1 Output=0
25 A=0 B=0 C=1 D=0 S1=0 S2=1 Output=1
30 A=0 B=0 C=0 D=0 S1=1 S2=1 Output=0
35 A=0 B=0 C=0 D=1 S1=1 S2=1 Output=1
mythreya@pes:~/Desktop/verilog_files/week4/4mux$


GTKWave - mux4.vcd
4:57 PM
From: 0 sec
To: 40 sec
Marker: 20 sec | Cursor: 28 sec
SST
mux4_tb
Signals
Waves
Time
a =0
b =0
c =0
d =0
s1 =0
s2 =1
y =0
10 sec
20 sec
30 sec
40 sec
Type Signals
reg a
reg b
reg c
reg d
reg s1
reg s2
wire y
Filter:
Append
Insert
Replace

16-bit ALU

alu.v (~/Desktop/verilog_files/week5) - gedit

```
module alu(input wire[1:0] op,input wire[15:0] i0,i1,output wire[15:0] o,output wire cout);
wire[14:0] c;
alu_slice a1(op,i0[0],i1[0],op[0],c[0],o[0]);
alu_slice a2(op,i0[1],i1[1],op[1],c[1],o[1]);
alu_slice a3(op,i0[2],i1[2],op[2],c[2],o[2]);
alu_slice a4(op,i0[3],i1[3],op[3],c[3],o[3]);
alu_slice a5(op,i0[4],i1[4],op[4],c[4],o[4]);
alu_slice a6(op,i0[5],i1[5],op[5],c[5],o[5]);
alu_slice a7(op,i0[6],i1[6],op[6],c[6],o[6]);
alu_slice a8(op,i0[7],i1[7],op[7],c[7],o[7]);
alu_slice a9(op,i0[8],i1[8],op[8],c[8],o[8]);
alu_slice a10(op,i0[9],i1[9],op[9],c[9],o[9]);
alu_slice a11(op,i0[10],i1[10],op[10],c[10],o[10]);
alu_slice a12(op,i0[11],i1[11],op[11],c[11],o[11]);
alu_slice a13(op,i0[12],i1[12],op[12],c[12],o[12]);
alu_slice a14(op,i0[13],i1[13],op[13],c[13],o[13]);
alu_slice a15(op,i0[14],i1[14],op[14],c[14],o[14]);
alu_slice a16(op,i0[15],i1[15],op[15],cout,+o[15]);
endmodule
```

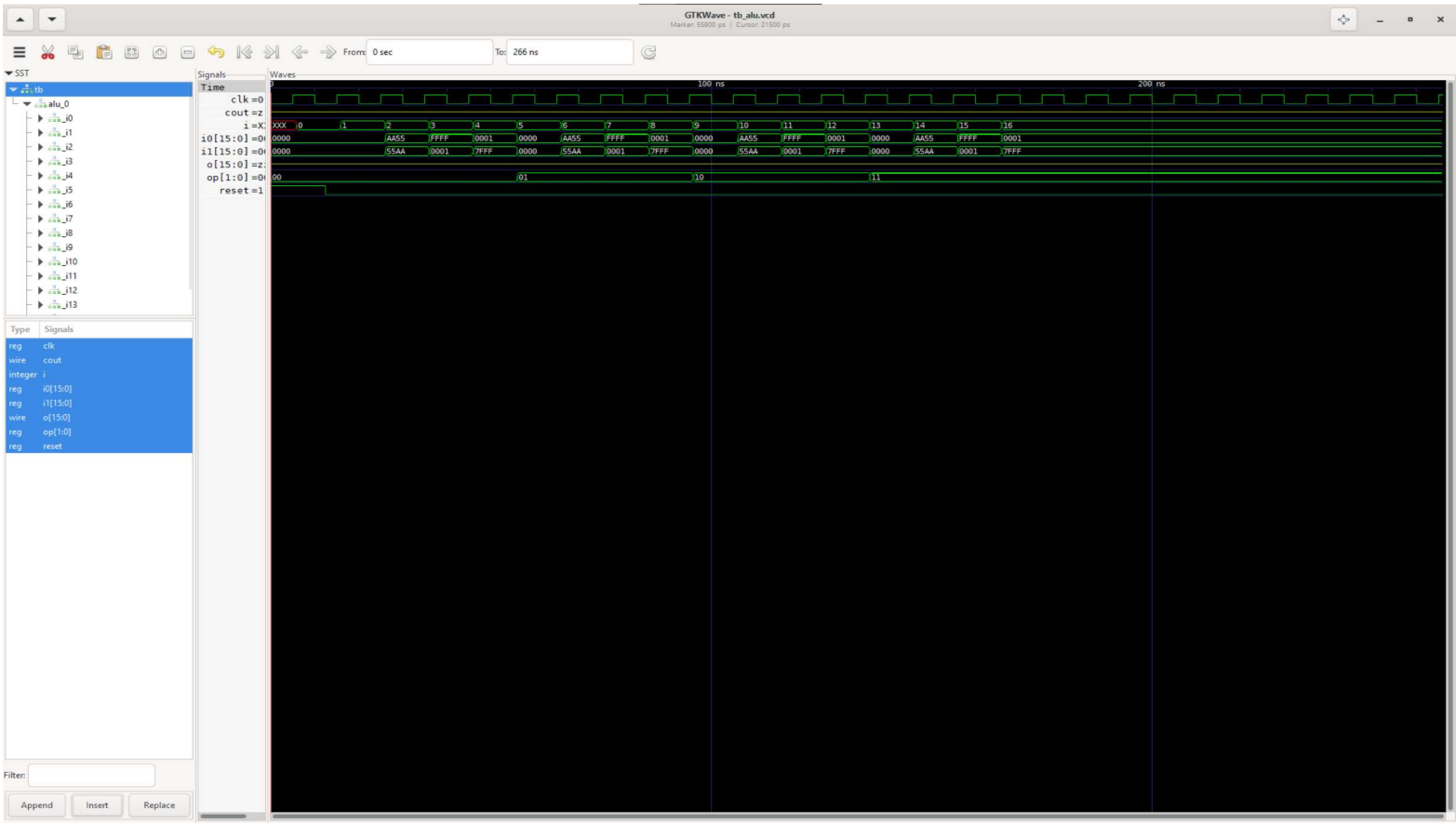
alu_slice.v (~/Desktop/verilog_files/week5) - gedit

```
module alu_slice(input wire[1:0] op,input wire i0,i1,cin,output wire cout,o);
wire t_addsub,t_andor;
addsub a1(op[0],i0,i1,cin,t_addsub,cout);
mux2 andor(i0&i1,i0|i1,op[0],t_andor);
mux2 out(t_andor,t_andsub,op[1],o);
endmodule
```

Output

```
C:\Windows\System32\cmd.exe

X:\sem3\sem3-lab\ddco_lab\week5\alu\try 2>vvp alu
VCD info: dumpfile tb_alu.vcd opened for output.
At time =                    0, Operator= 00,i0=0000, i1=0000,Sum = zzzz,Carry z
At time =                  260, Operator= 00,i0=aa55, i1=55aa,Sum = zzzz,Carry z
At time =                  360, Operator= 00,i0=ffff, i1=0001,Sum = zzzz,Carry z
At time =                  460, Operator= 00,i0=0001, i1=7fff,Sum = zzzz,Carry z
At time =                  560, Operator= 01,i0=0000, i1=0000,Sum = zzzz,Carry z
At time =                  660, Operator= 01,i0=aa55, i1=55aa,Sum = zzzz,Carry z
At time =                  760, Operator= 01,i0=ffff, i1=0001,Sum = zzzz,Carry z
At time =                  860, Operator= 01,i0=0001, i1=7fff,Sum = zzzz,Carry z
At time =                  960, Operator= 10,i0=0000, i1=0000,Sum = zzzz,Carry z
At time =                 1060, Operator= 10,i0=aa55, i1=55aa,Sum = zzzz,Carry z
At time =                 1160, Operator= 10,i0=ffff, i1=0001,Sum = zzzz,Carry z
At time =                 1260, Operator= 10,i0=0001, i1=7fff,Sum = zzzz,Carry z
At time =                 1360, Operator= 11,i0=0000, i1=0000,Sum = zzzz,Carry z
At time =                 1460, Operator= 11,i0=aa55, i1=55aa,Sum = zzzz,Carry z
At time =                 1560, Operator= 11,i0=ffff, i1=0001,Sum = zzzz,Carry z
At time =                 1660, Operator= 11,i0=0001, i1=7fff,Sum = zzzz,Carry z
tb_alu.v:45: $finish called at 2660 (100ps)
```



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· The programs and output submitted is duly written, verified and executed by me.

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· If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

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