

DDCO LAB SEM3

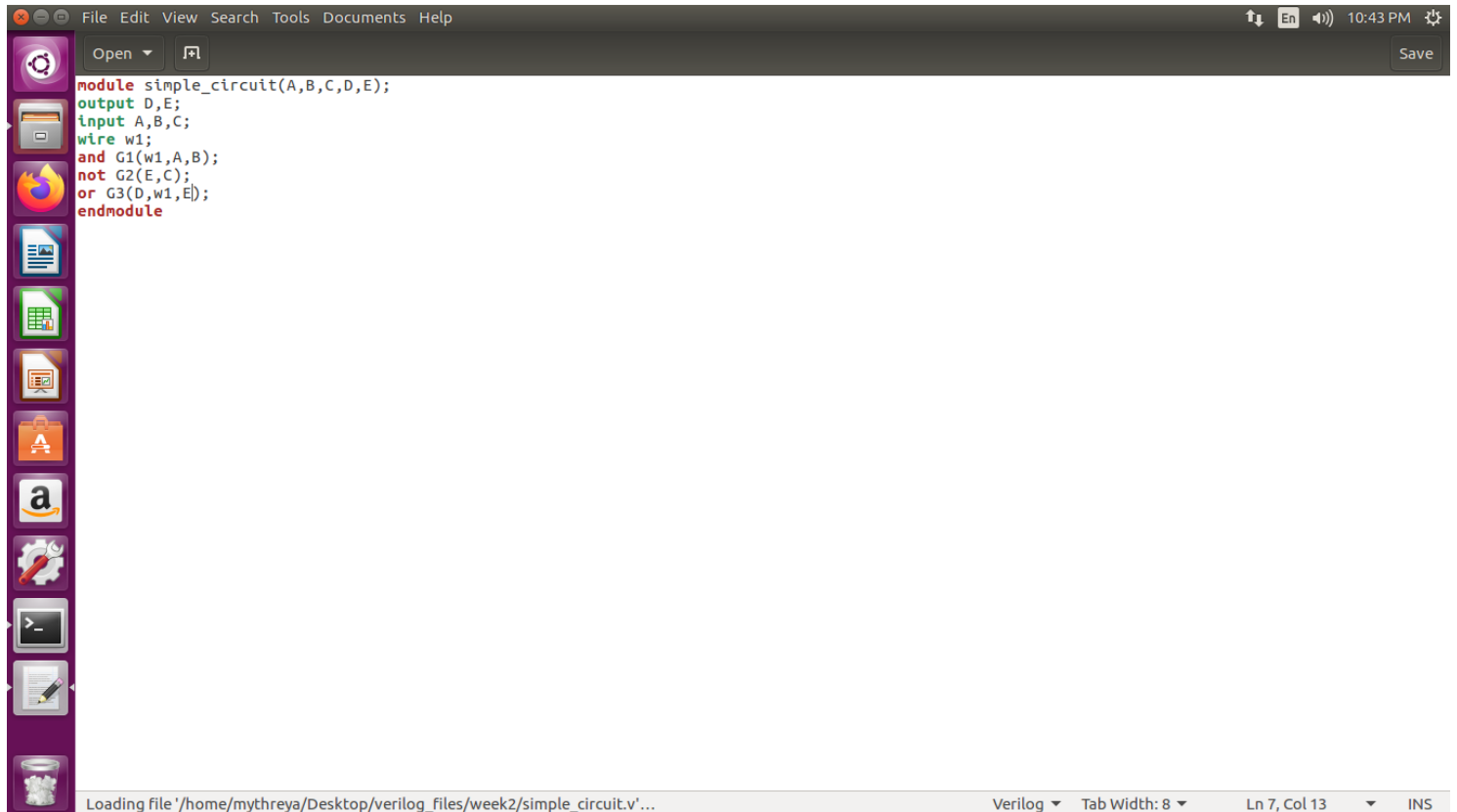
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SRN : PES2UG20CS130

Section : C

Week 2: Basic circuits

Circuit 1

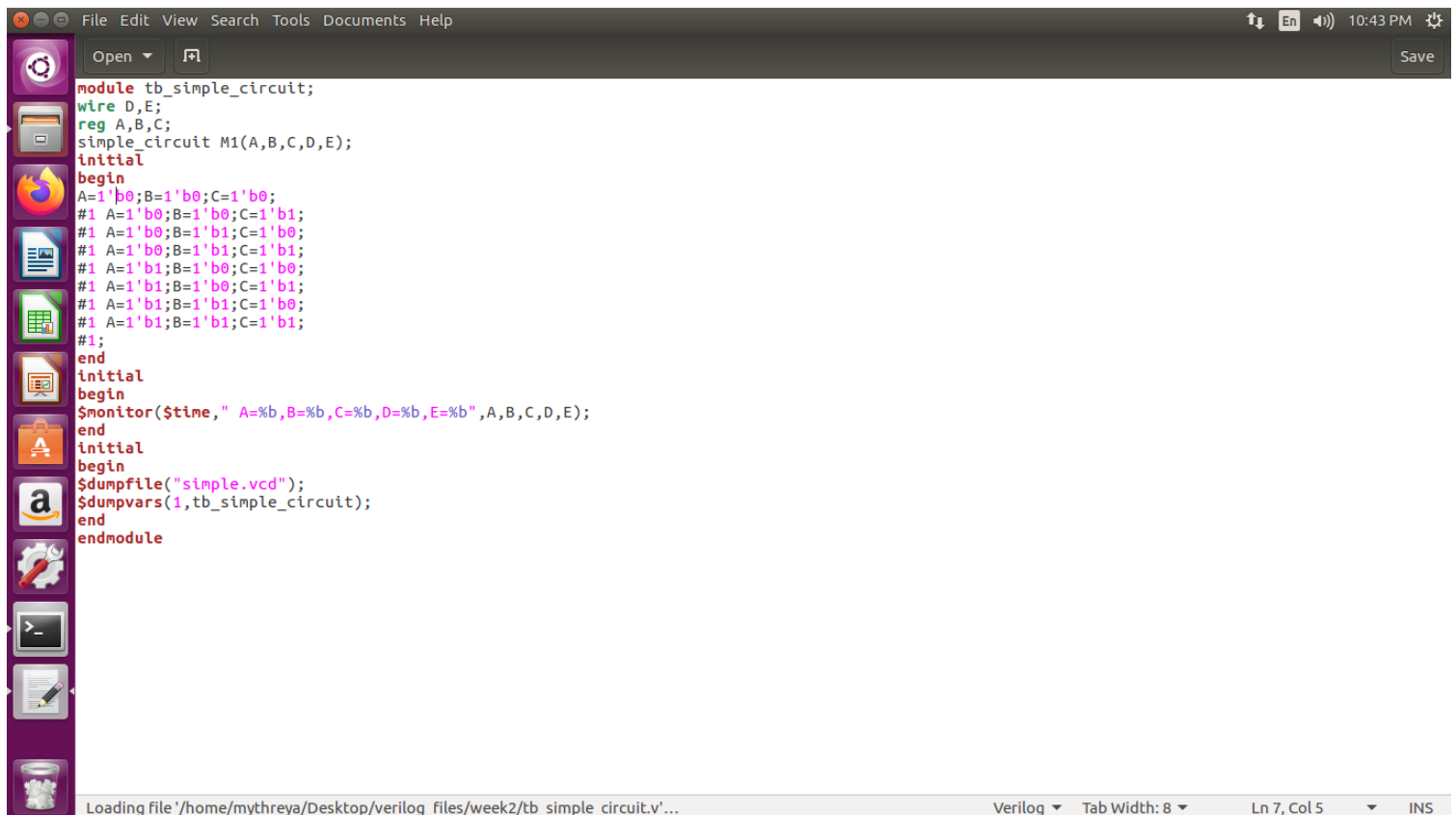


The screenshot shows a Verilog code editor window with a menu bar (File, Edit, View, Search, Tools, Documents, Help) and a toolbar with icons for Open, Save, and a cursor. The code defines a module named 'simple_circuit' with inputs A, B, C and outputs D, E. It uses a wire 'w1' and three gates: G1 (AND), G2 (NOT), and G3 (OR). The status bar at the bottom indicates the file path, language (Verilog), tab width (8), and current position (Ln 7, Col 13).

```
module simple_circuit(A,B,C,D,E);
output D,E;
input A,B,C;
wire w1;
and G1(w1,A,B);
not G2(E,C);
or G3(D,w1,E);
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/week2/simple_circuit.v'...

Verilog Tab Width: 8 Ln 7, Col 13 INS



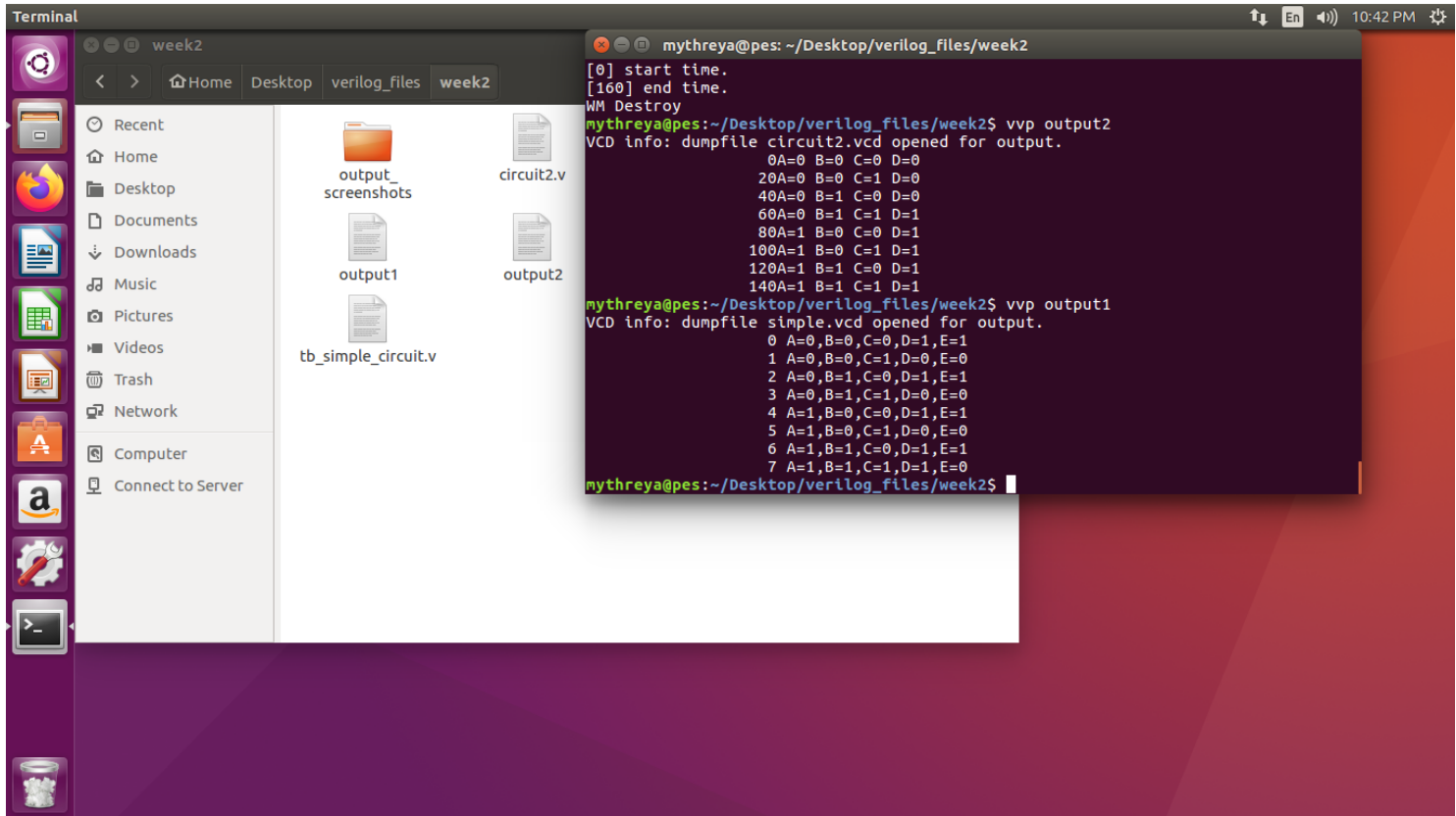
The screenshot shows a Verilog code editor window with a menu bar (File, Edit, View, Search, Tools, Documents, Help) and a toolbar with icons for Open, Save, and a cursor. The code defines a testbench module named 'tb_simple_circuit'. It instantiates the 'simple_circuit' module and applies a series of test vectors to inputs A, B, and C. It also includes a \$monitor statement to display the values of A, B, C, D, and E, and a \$dumpvars statement to save the waveforms to a file named 'simple.vcd'. The status bar at the bottom indicates the file path, language (Verilog), tab width (8), and current position (Ln 7, Col 5).

```
module tb_simple_circuit;
wire D,E;
reg A,B,C;
simple_circuit M1(A,B,C,D,E);
initial
begin
A=1'b0;B=1'b0;C=1'b0;
#1 A=1'b0;B=1'b0;C=1'b1;
#1 A=1'b0;B=1'b1;C=1'b0;
#1 A=1'b0;B=1'b1;C=1'b1;
#1 A=1'b1;B=1'b0;C=1'b0;
#1 A=1'b1;B=1'b0;C=1'b1;
#1 A=1'b1;B=1'b1;C=1'b0;
#1 A=1'b1;B=1'b1;C=1'b1;
#1;
end
initial
begin
$monitor($time," A=%b,B=%b,C=%b,D=%b,E=%b",A,B,C,D,E);
end
initial
begin
$dumpfile("simple.vcd");
$dumpvars(1,tb_simple_circuit);
end
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/week2/tb_simple_circuit.v'...

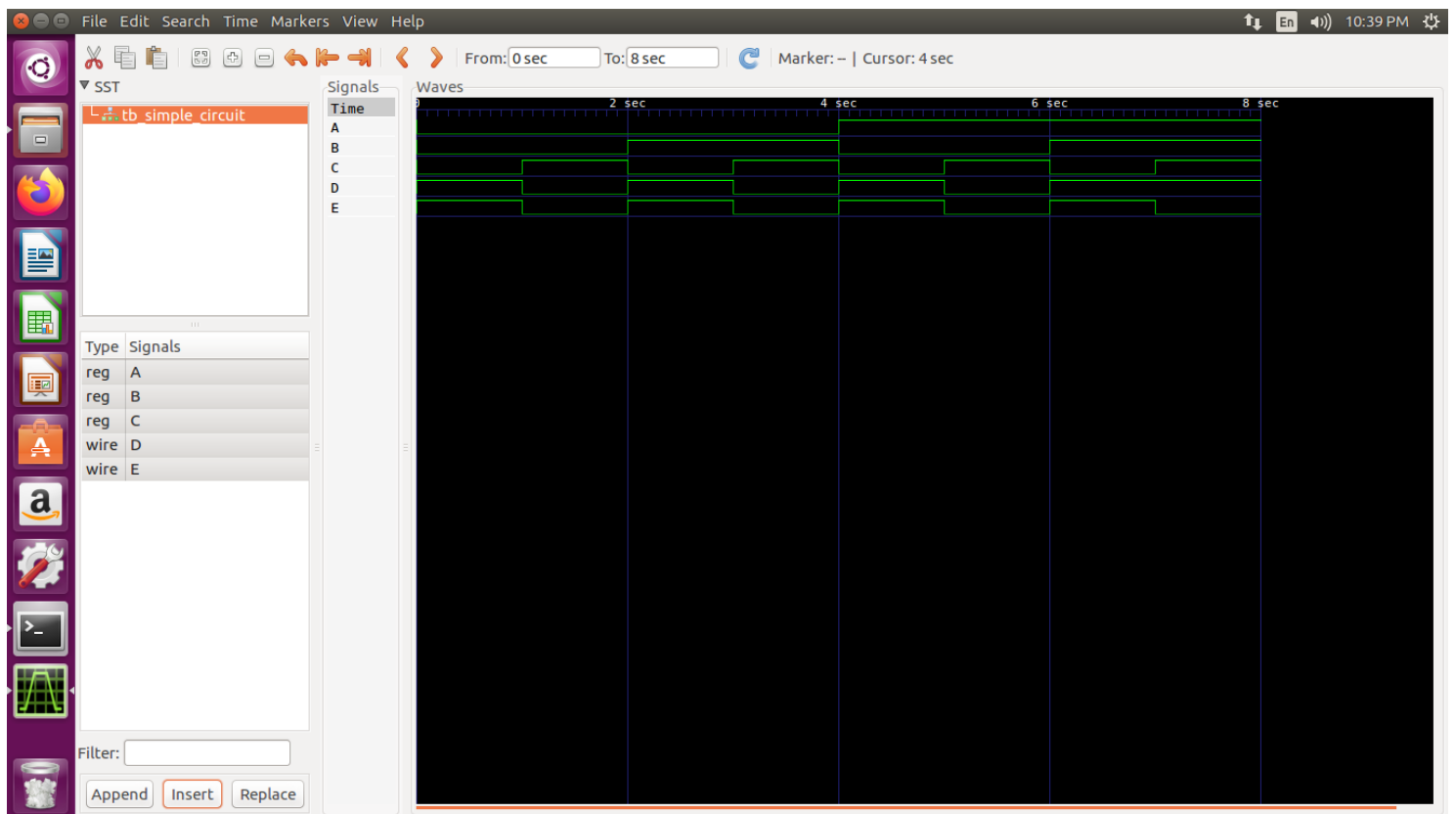
Verilog Tab Width: 8 Ln 7, Col 5 INS

Output

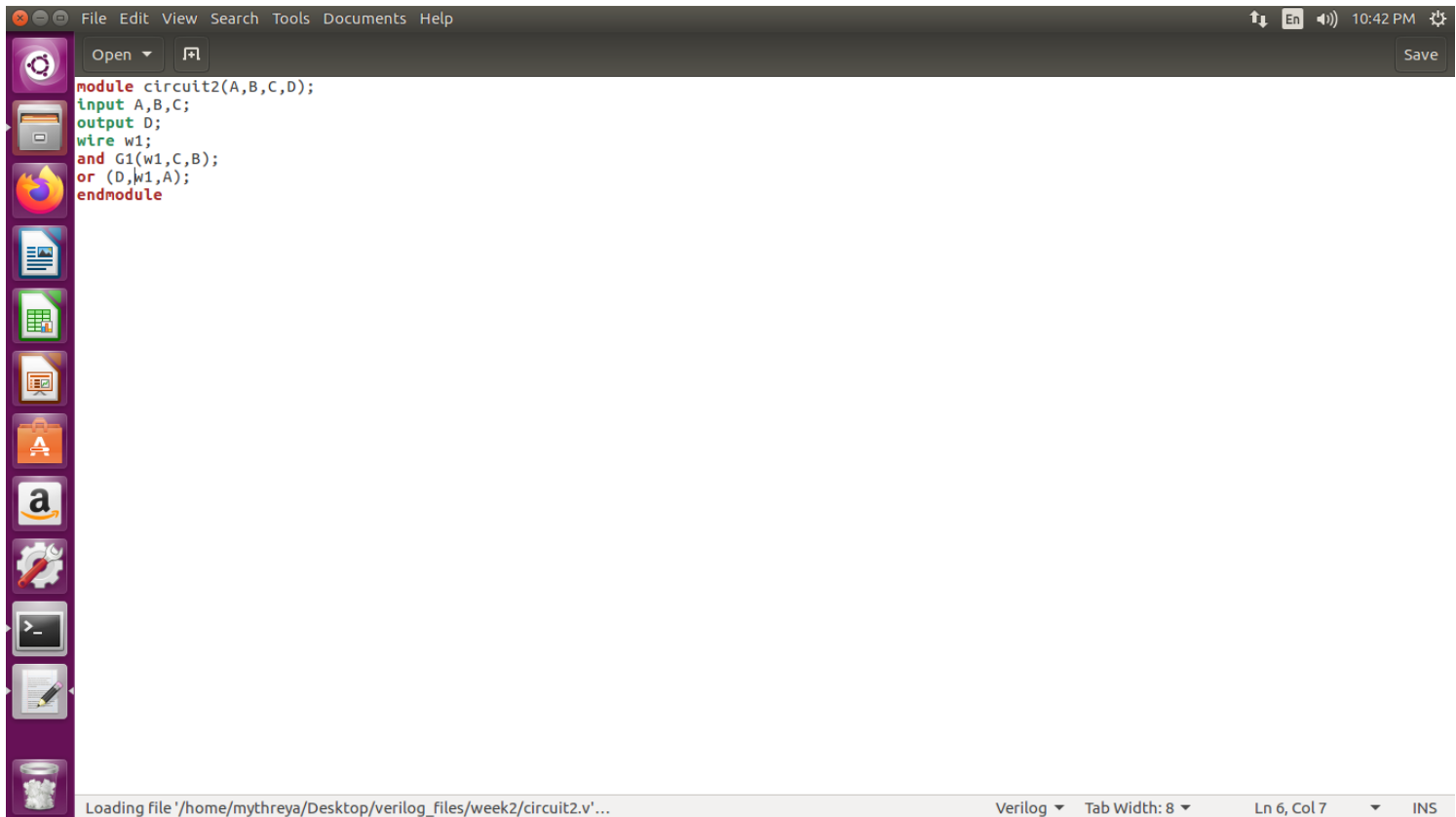


The image shows a Linux desktop environment with a file manager and a terminal window. The file manager displays the contents of the `~/Desktop/verilog_files/week2` directory, which includes folders `output_screenshots` and `output1`, and files `circuit2.v`, `output2`, and `tb_simple_circuit.v`. The terminal window shows the execution of Verilog simulation commands and the resulting output.

```
mythreya@pes: ~/Desktop/verilog_files/week2
[0] start time.
[160] end time.
WM Destroy
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output2
VCD info: dumpfile circuit2.vcd opened for output.
  0A=0 B=0 C=0 D=0
 20A=0 B=0 C=1 D=0
 40A=0 B=1 C=0 D=0
 60A=0 B=1 C=1 D=1
 80A=1 B=0 C=0 D=1
100A=1 B=0 C=1 D=1
120A=1 B=1 C=0 D=1
140A=1 B=1 C=1 D=1
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output1
VCD info: dumpfile simple.vcd opened for output.
  0 A=0,B=0,C=0,D=1,E=1
  1 A=0,B=0,C=1,D=0,E=0
  2 A=0,B=1,C=0,D=1,E=1
  3 A=0,B=1,C=1,D=0,E=0
  4 A=1,B=0,C=0,D=1,E=1
  5 A=1,B=0,C=1,D=0,E=0
  6 A=1,B=1,C=0,D=1,E=1
  7 A=1,B=1,C=1,D=1,E=0
mythreya@pes:~/Desktop/verilog_files/week2$
```



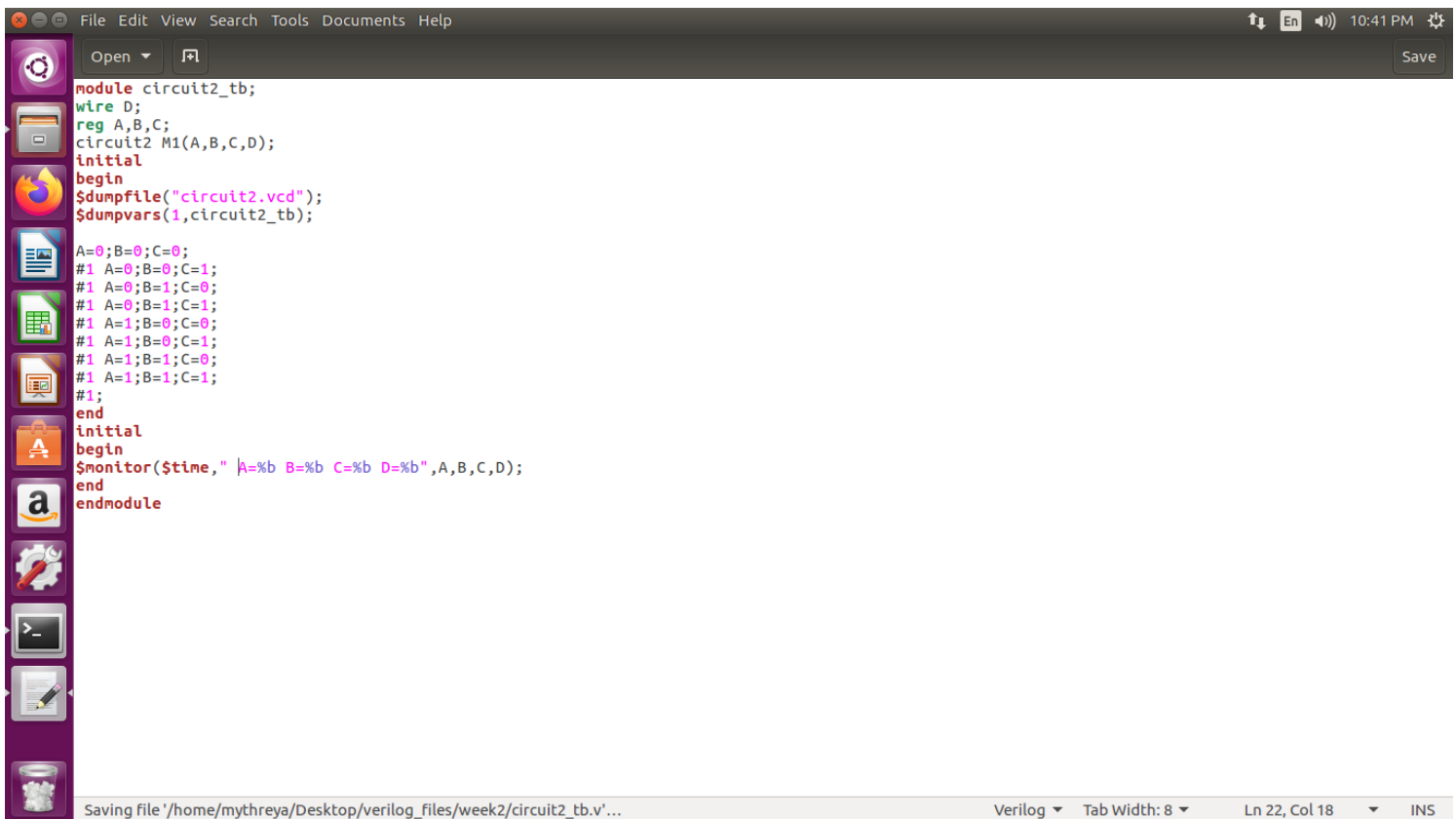
Circuit 2



A screenshot of a Verilog code editor window. The window has a menu bar with 'File', 'Edit', 'View', 'Search', 'Tools', 'Documents', and 'Help'. Below the menu bar is a toolbar with 'Open' and 'Save' buttons. The main text area contains the following Verilog code:

```
module circuit2(A,B,C,D);  
  input A,B,C;  
  output D;  
  wire w1;  
  and G1(w1,C,B);  
  or (D,w1,A);  
endmodule
```

The status bar at the bottom shows 'Loading file '/home/mythreya/Desktop/verilog_files/week2/circuit2.v'...', 'Verilog', 'Tab Width: 8', 'Ln 6, Col 7', and 'INS'.

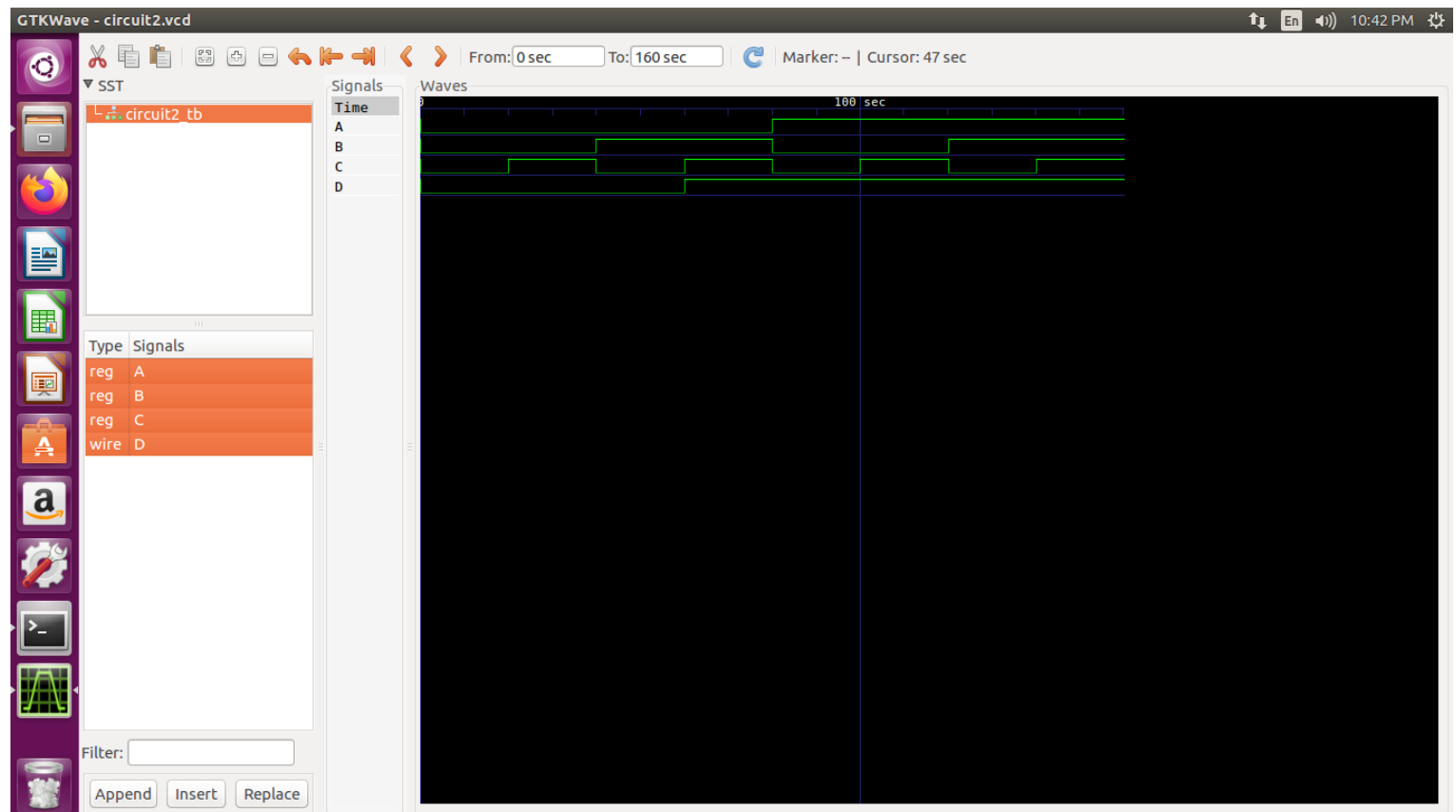
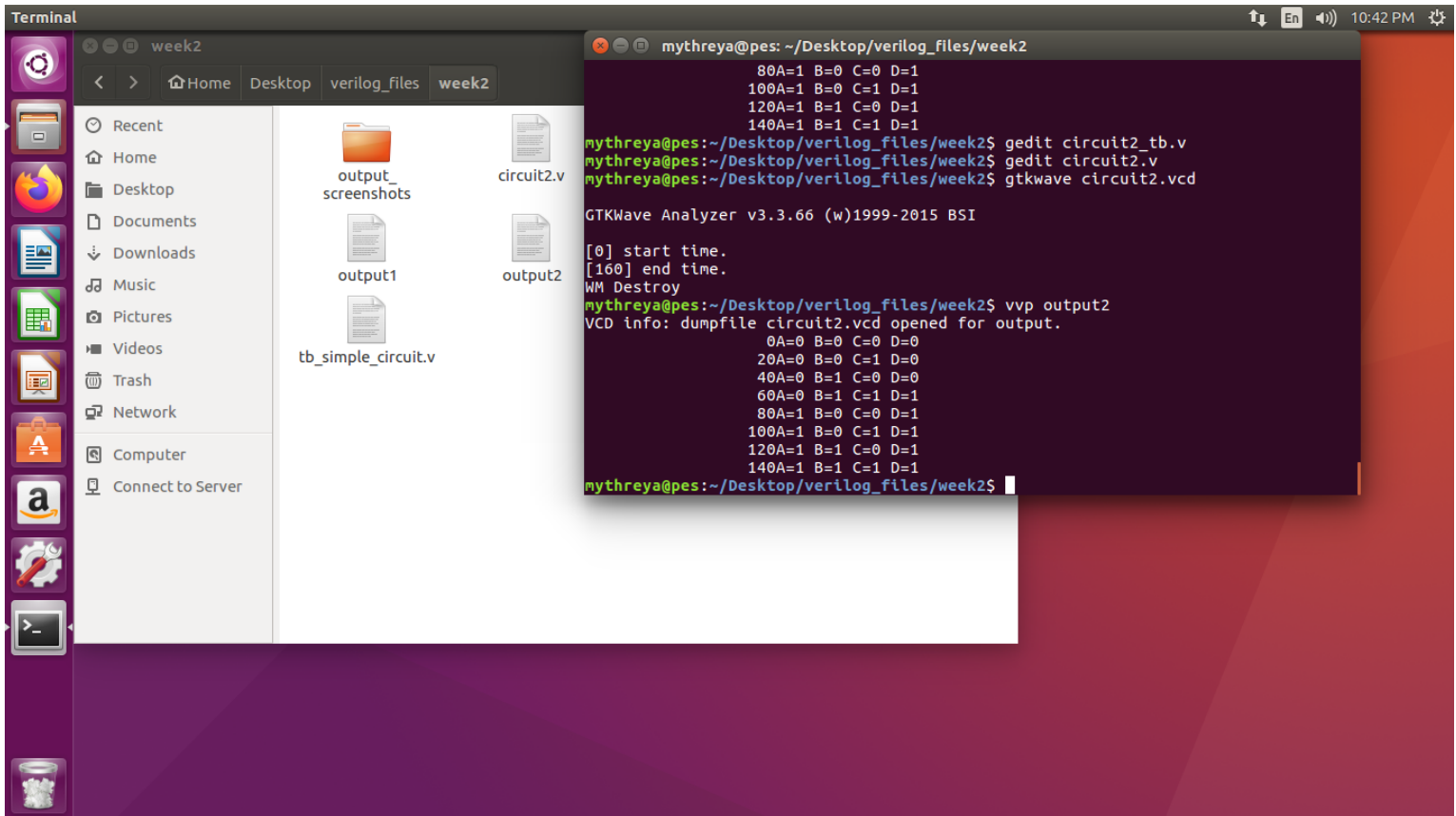


A screenshot of a Verilog code editor window. The window has a menu bar with 'File', 'Edit', 'View', 'Search', 'Tools', 'Documents', and 'Help'. Below the menu bar is a toolbar with 'Open' and 'Save' buttons. The main text area contains the following Verilog code:

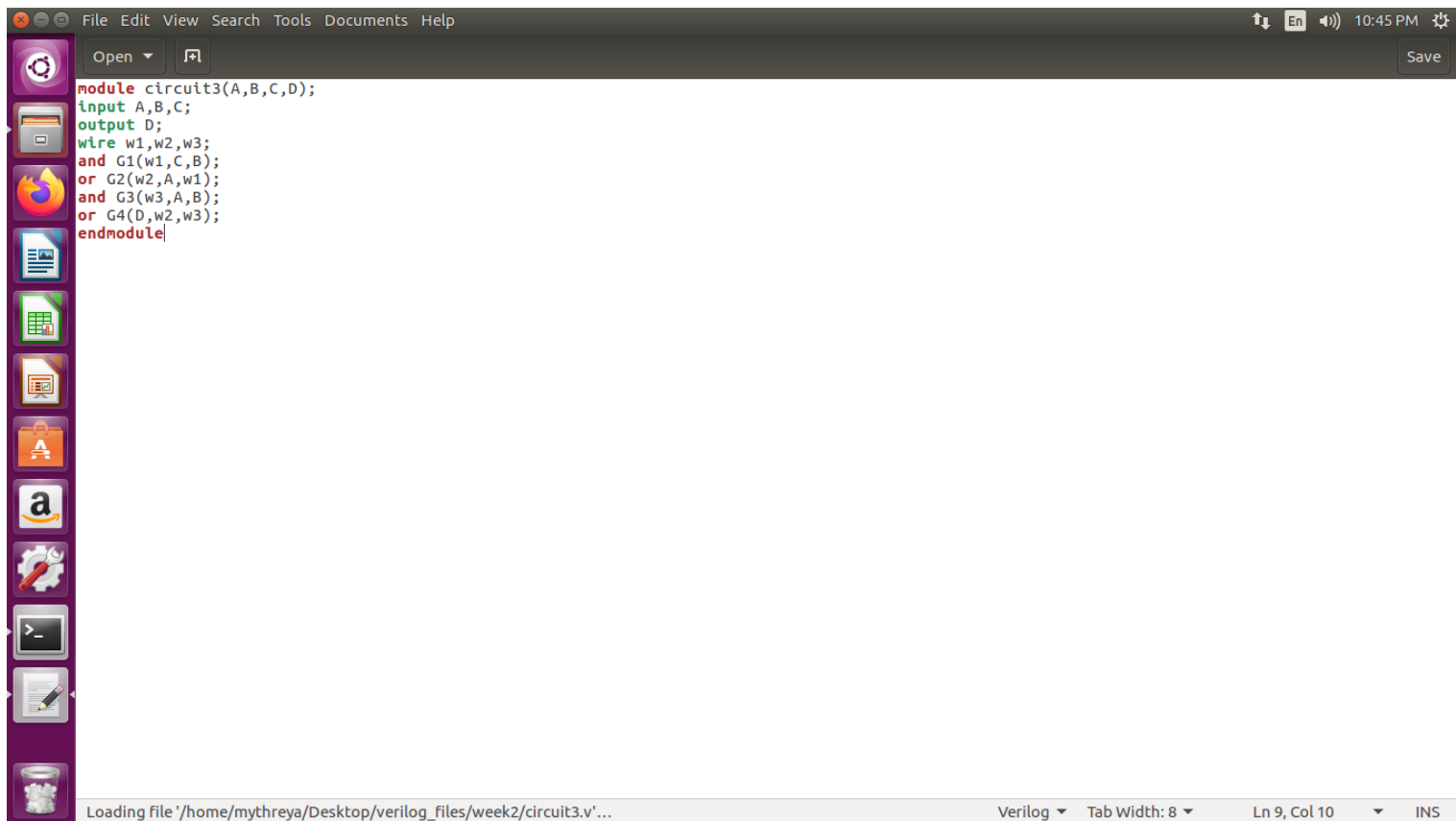
```
module circuit2_tb;  
  wire D;  
  reg A,B,C;  
  circuit2 M1(A,B,C,D);  
  initial  
  begin  
    $dumpfile("circuit2.vcd");  
    $dumpvars(1,circuit2_tb);  
  
    A=0;B=0;C=0;  
    #1 A=0;B=0;C=1;  
    #1 A=0;B=1;C=0;  
    #1 A=0;B=1;C=1;  
    #1 A=1;B=0;C=0;  
    #1 A=1;B=0;C=1;  
    #1 A=1;B=1;C=0;  
    #1 A=1;B=1;C=1;  
    #1;  
  end  
  initial  
  begin  
    $monitor($time," A=%b B=%b C=%b D=%b",A,B,C,D);  
  end  
endmodule
```

The status bar at the bottom shows 'Saving file '/home/mythreya/Desktop/verilog_files/week2/circuit2_tb.v'...', 'Verilog', 'Tab Width: 8', 'Ln 22, Col 18', and 'INS'.

Output



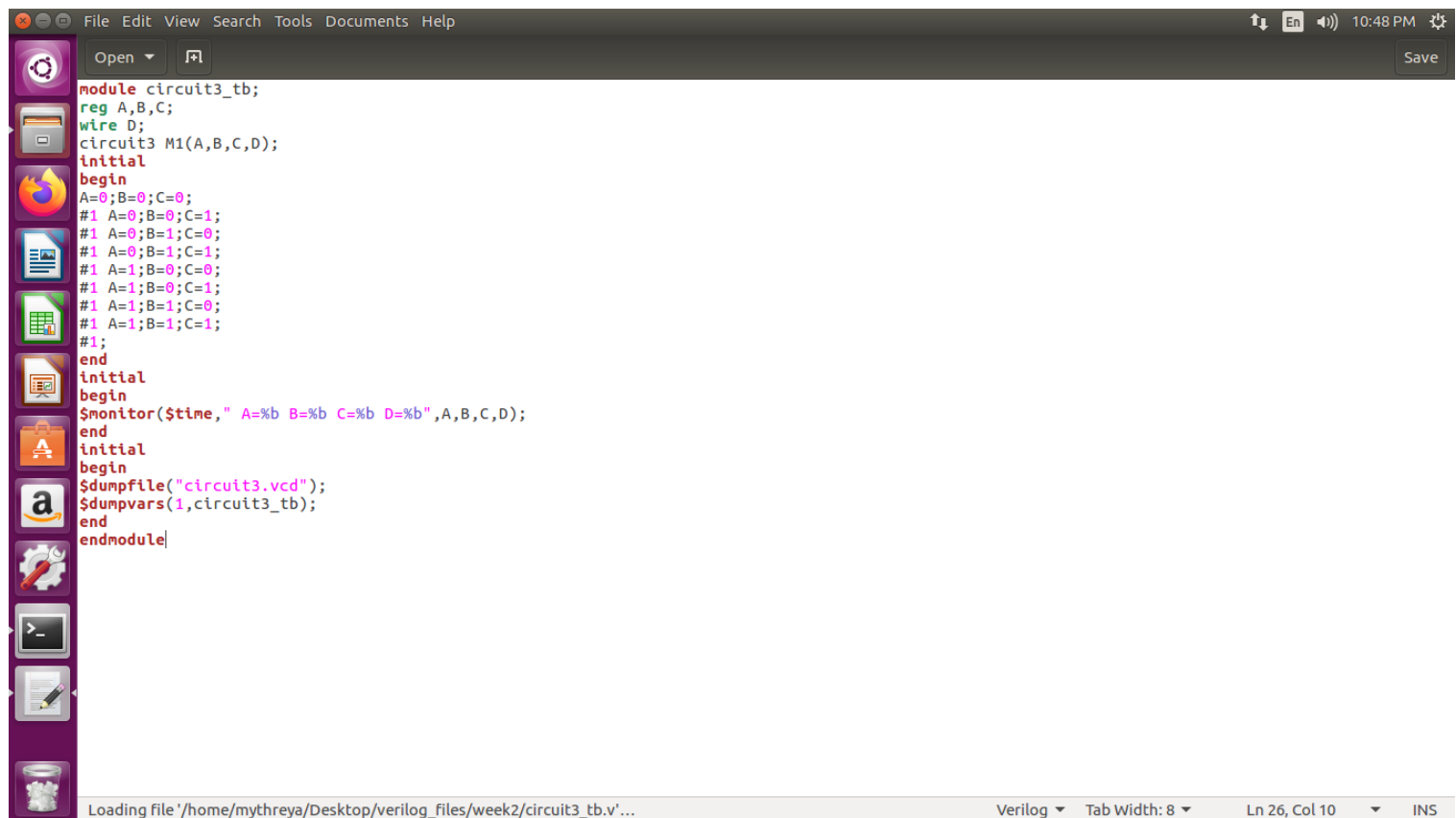
Circuit 3



A screenshot of a Verilog code editor window. The title bar shows 'File Edit View Search Tools Documents Help' and system icons on the right. The left sidebar contains icons for various applications. The main text area displays the following Verilog code:

```
module circuit3(A,B,C,D);  
input A,B,C;  
output D;  
wire w1,w2,w3;  
and G1(w1,C,B);  
or G2(w2,A,w1);  
and G3(w3,A,B);  
or G4(D,w2,w3);  
endmodule
```

The status bar at the bottom indicates 'Loading file "/home/mythreya/Desktop/verilog_files/week2/circuit3.v'...', 'Verilog', 'Tab Width: 8', 'Ln 9, Col 10', and 'INS'.

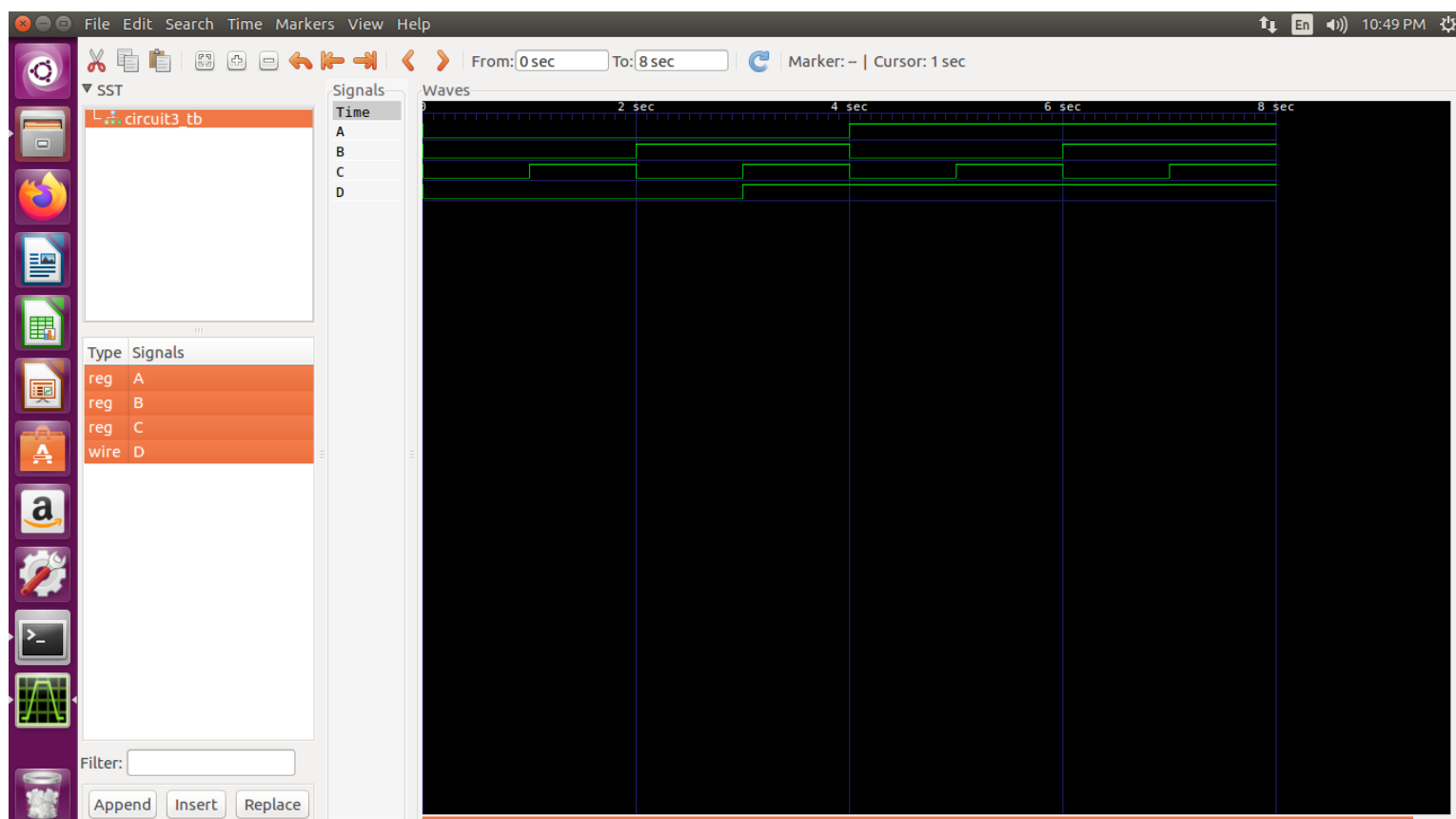
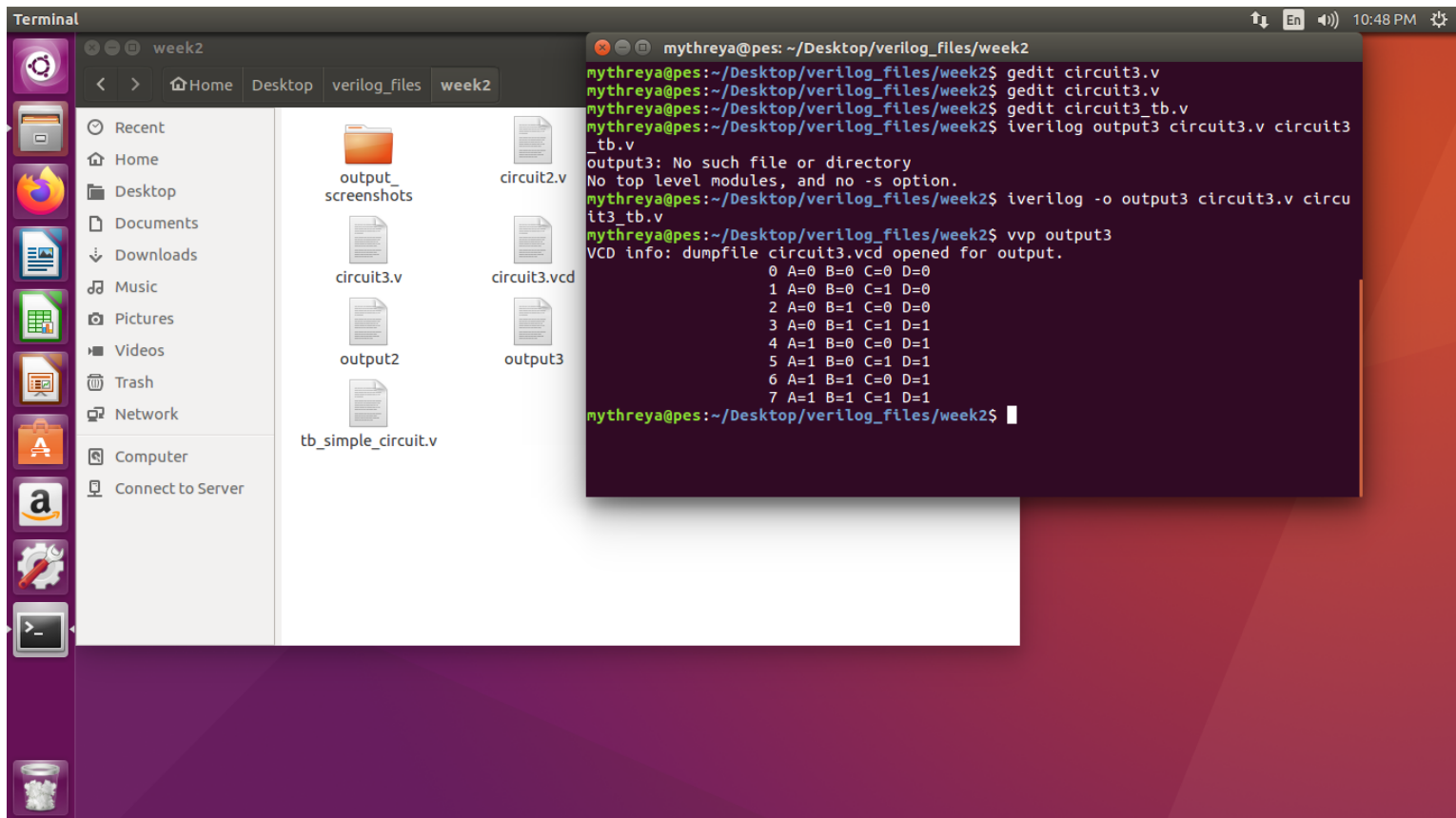


A screenshot of a Verilog code editor window showing a testbench module. The title bar and sidebar are the same as the previous image. The main text area displays the following Verilog code:

```
module circuit3_tb;  
reg A,B,C;  
wire D;  
circuit3 M1(A,B,C,D);  
initial  
begin  
A=0;B=0;C=0;  
#1 A=0;B=0;C=1;  
#1 A=0;B=1;C=0;  
#1 A=0;B=1;C=1;  
#1 A=1;B=0;C=0;  
#1 A=1;B=0;C=1;  
#1 A=1;B=1;C=0;  
#1 A=1;B=1;C=1;  
#1;  
end  
initial  
begin  
$monitor($time," A=%b B=%b C=%b D=%b",A,B,C,D);  
end  
initial  
begin  
$dumpfile("circuit3.vcd");  
$dumpvars(1,circuit3_tb);  
end  
endmodule
```

The status bar at the bottom indicates 'Loading file "/home/mythreya/Desktop/verilog_files/week2/circuit3_tb.v'...', 'Verilog', 'Tab Width: 8', 'Ln 26, Col 10', and 'INS'.

Output



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name:

SRN:

Section:

Date: