DDCO LAB SEM3

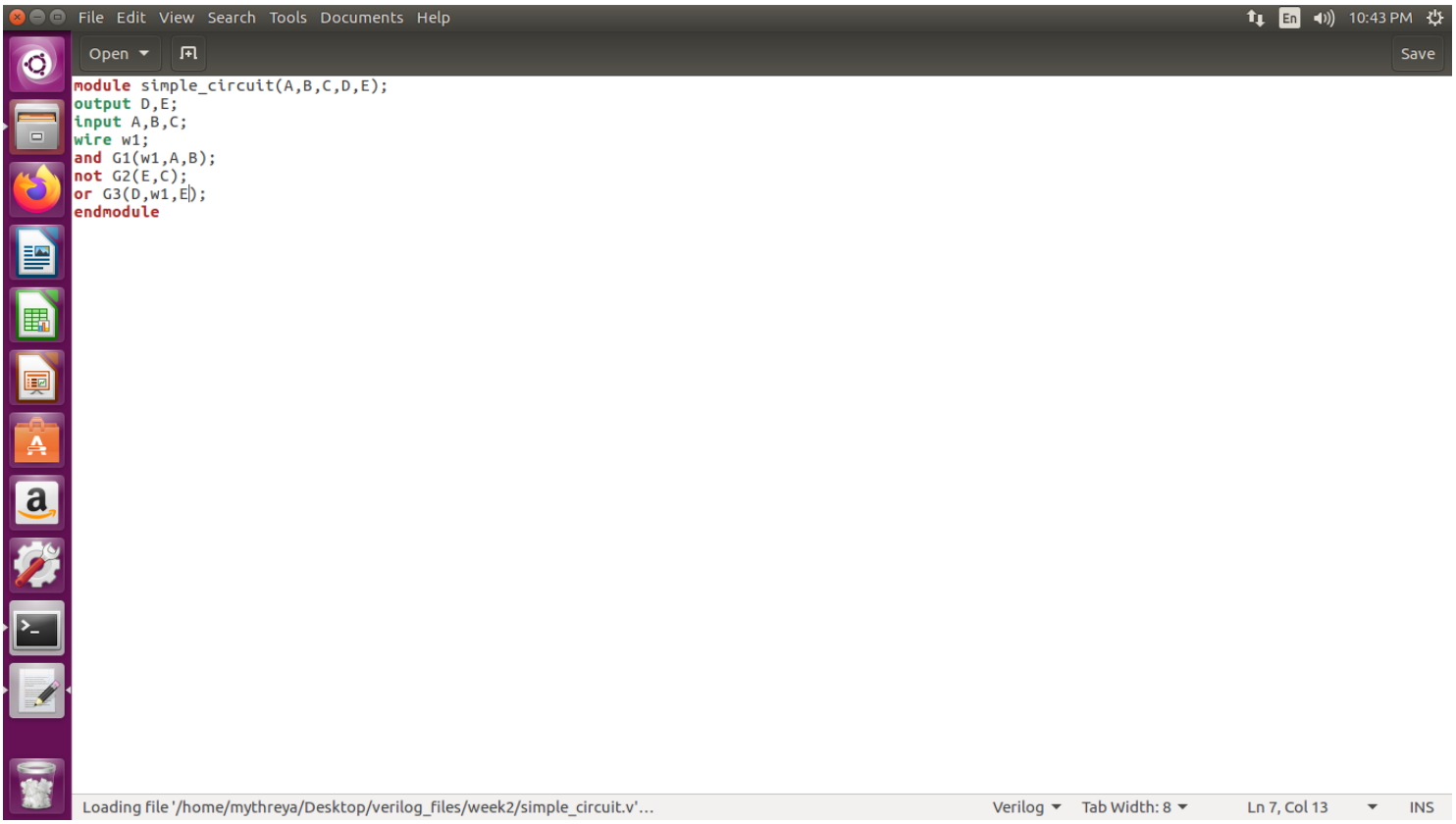
Name : H M Mythreya

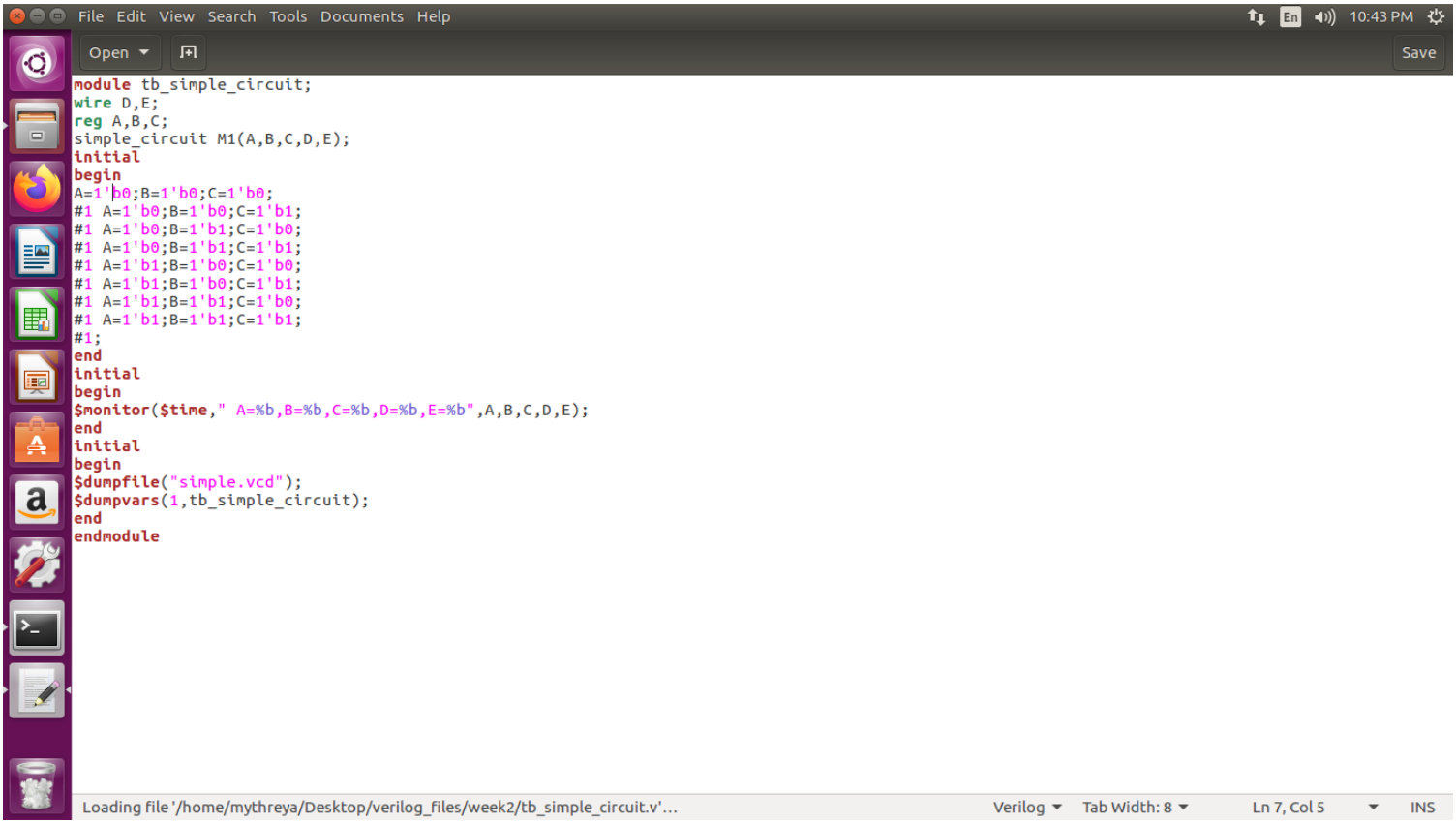
SRN : PES2UG20CS130

Section : C

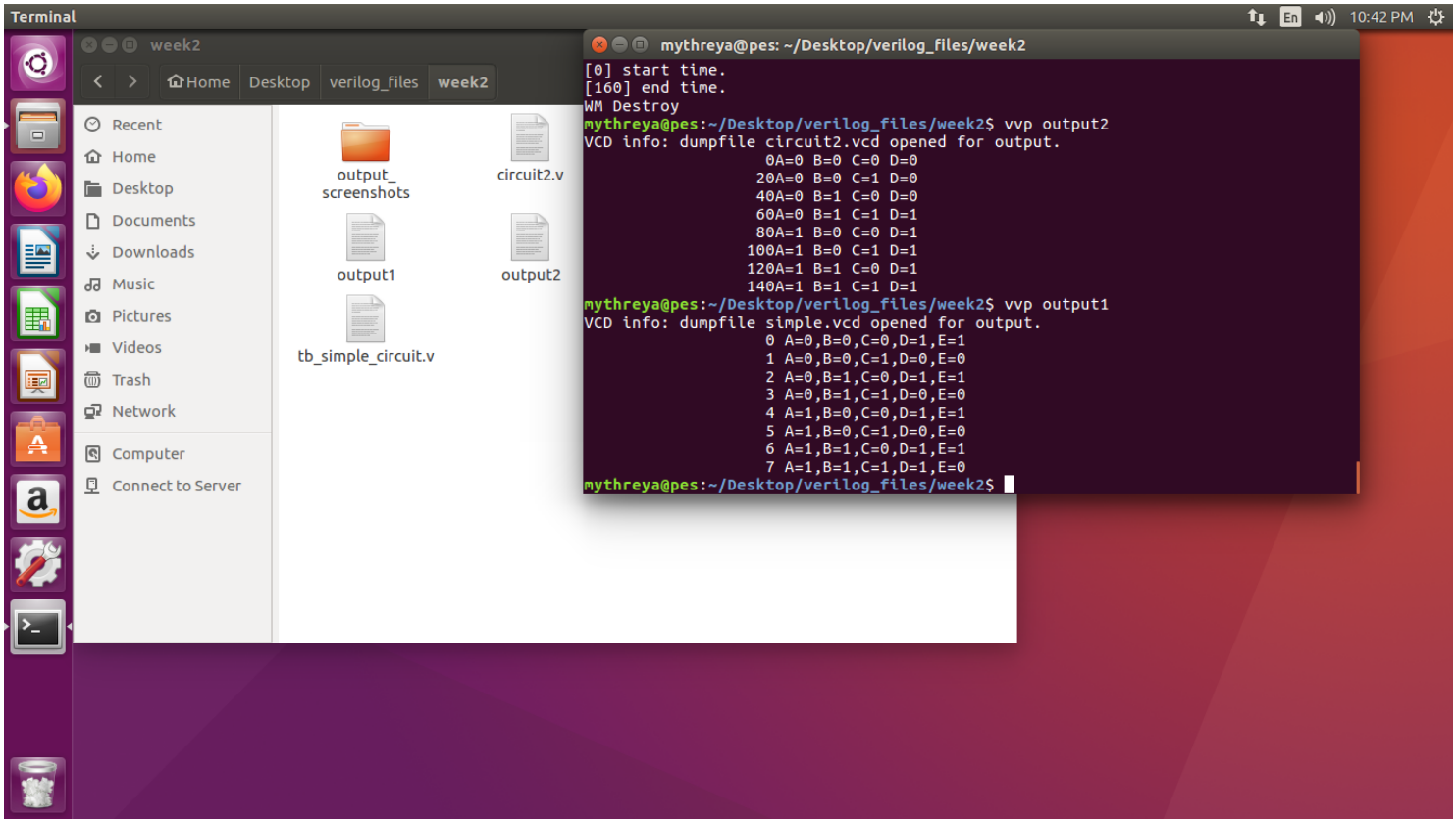
Week 2: Basic circuits

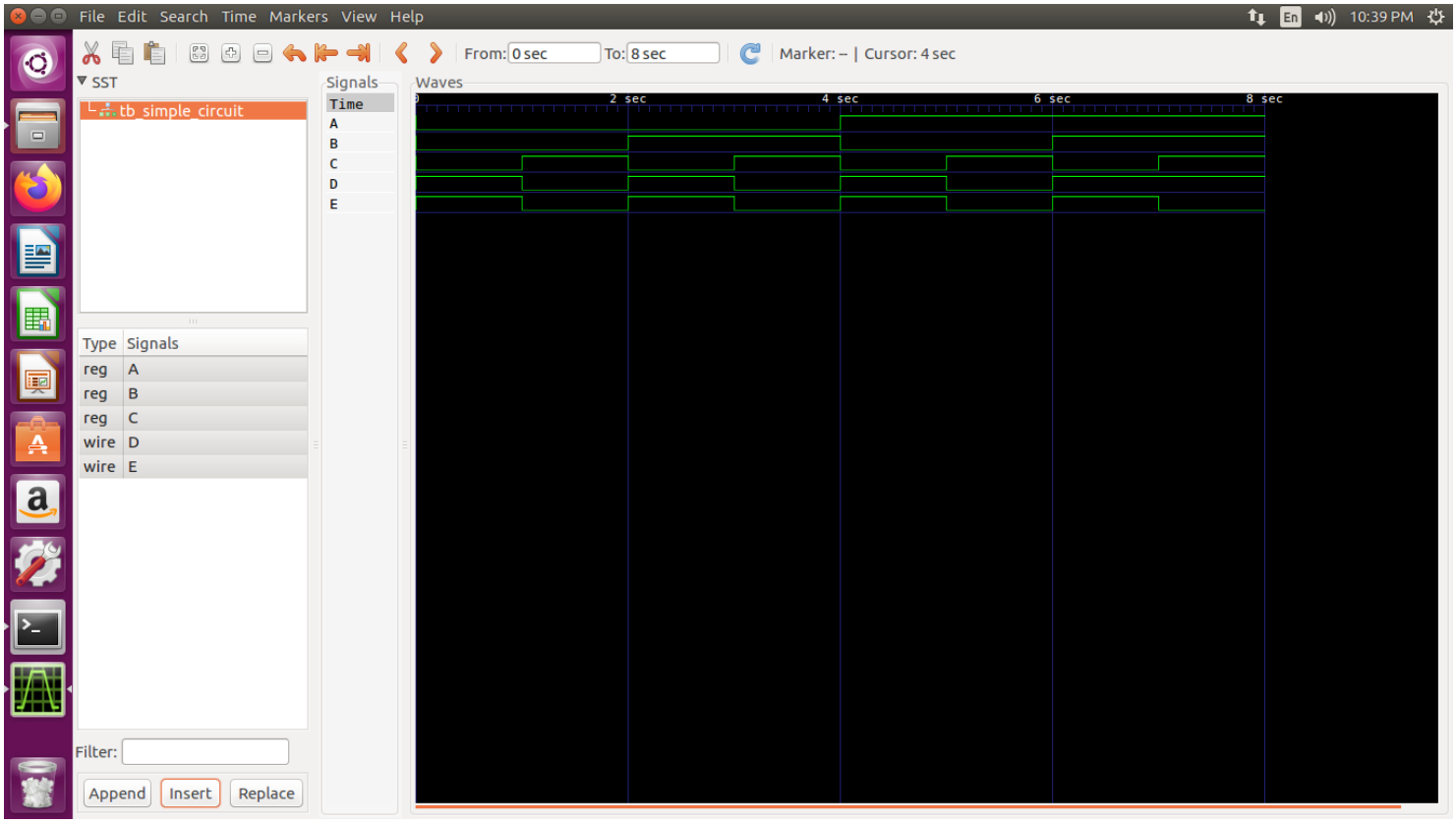
Circuit 1





Output


Terminal
10:42 PM
week2
Home
Desktop
verilog_files
week2
Recent
Home
Desktop
Documents
Downloads
Music
Pictures
Videos
Trash
Network
Computer
Connect to Server
output_ screenshots
circuit2.v
output1
output2
tb_simple_circuit.v
mythreya@pes: ~/Desktop/verilog_files/week2
[0] start time.
[160] end time.
WM Destroy
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output2
VCD info: dumpfile circuit2.vcd opened for output.
0A=0 B=0 C=0 D=0
20A=0 B=0 C=1 D=0
40A=0 B=1 C=0 D=0
60A=0 B=1 C=1 D=1
80A=1 B=0 C=0 D=1
100A=1 B=0 C=1 D=1
120A=1 B=1 C=0 D=1
140A=1 B=1 C=1 D=1
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output1
VCD info: dumpfile simple.vcd opened for output.
0 A=0,B=0,C=0,D=1,E=1
1 A=0,B=0,C=1,D=0,E=0
2 A=0,B=1,C=0,D=1,E=1
3 A=0,B=1,C=1,D=0,E=0
4 A=1,B=0,C=0,D=1,E=1
5 A=1,B=0,C=1,D=0,E=0
6 A=1,B=1,C=0,D=1,E=1
7 A=1,B=1,C=1,D=1,E=0
mythreya@pes:~/Desktop/verilog_files/week2$


File Edit Search Time Markers View Help
10:39 PM
From: 0 sec
To: 8 sec
Marker: – | Cursor: 4 sec
SST
tb_simple_circuit
Signals
Time
A
B
C
D
E
Waves
2 sec
4 sec
6 sec
8 sec
Type Signals
reg A
reg B
reg C
wire D
wire E
Filter:
Append
Insert
Replace

Circuit 2

File Edit View Search Tools Documents Help — 10:42 PM

Open — Save

```
module circuit2(A,B,C,D);
input A,B,C;
output D;
wire w1;
and G1(w1,C,B);
or (D,w1,A);
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/week2/circuit2.v'... Verilog Tab Width: 8 Ln 6, Col 7 INS

File Edit View Search Tools Documents Help — 10:41 PM

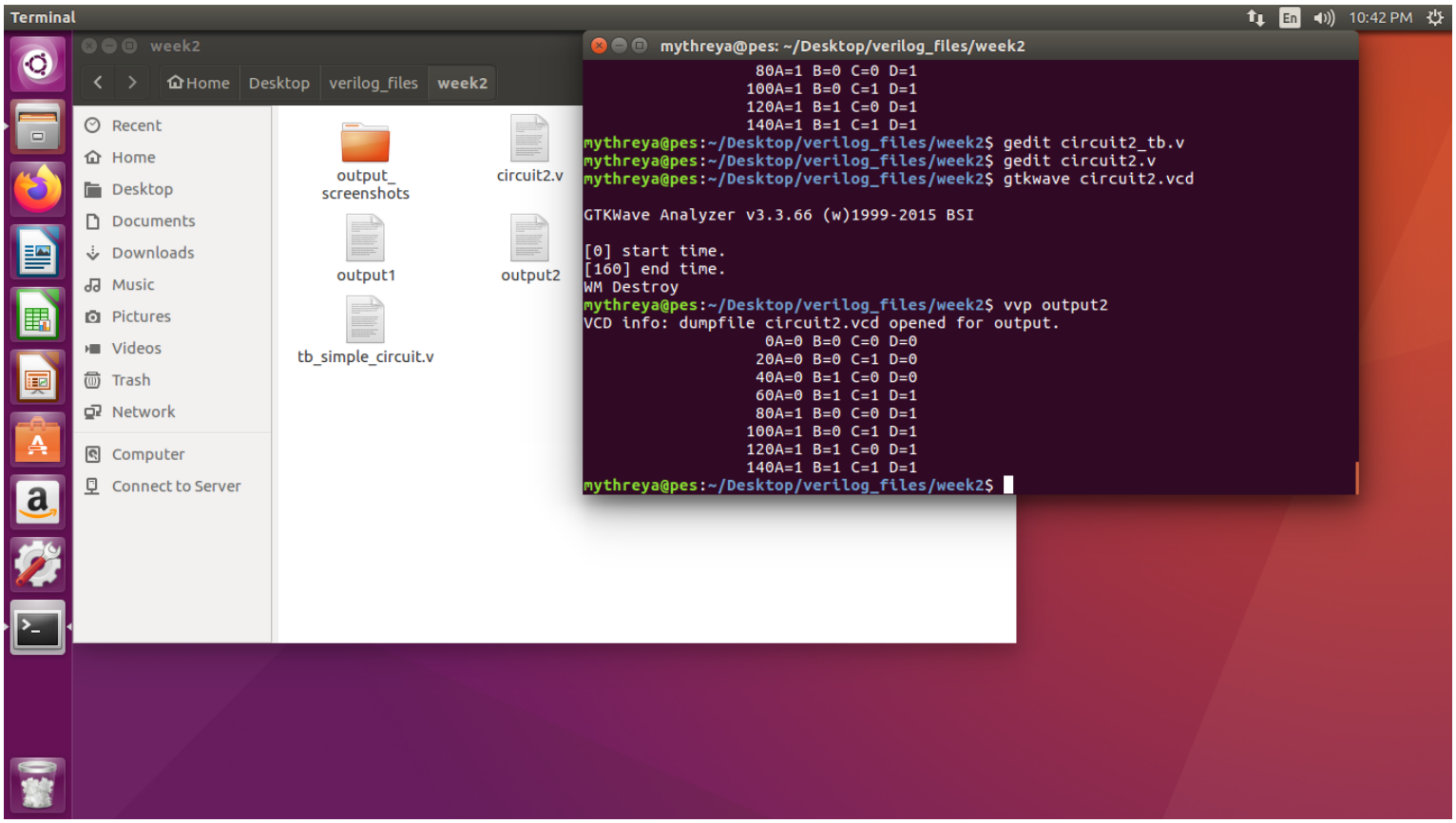
Open — Save

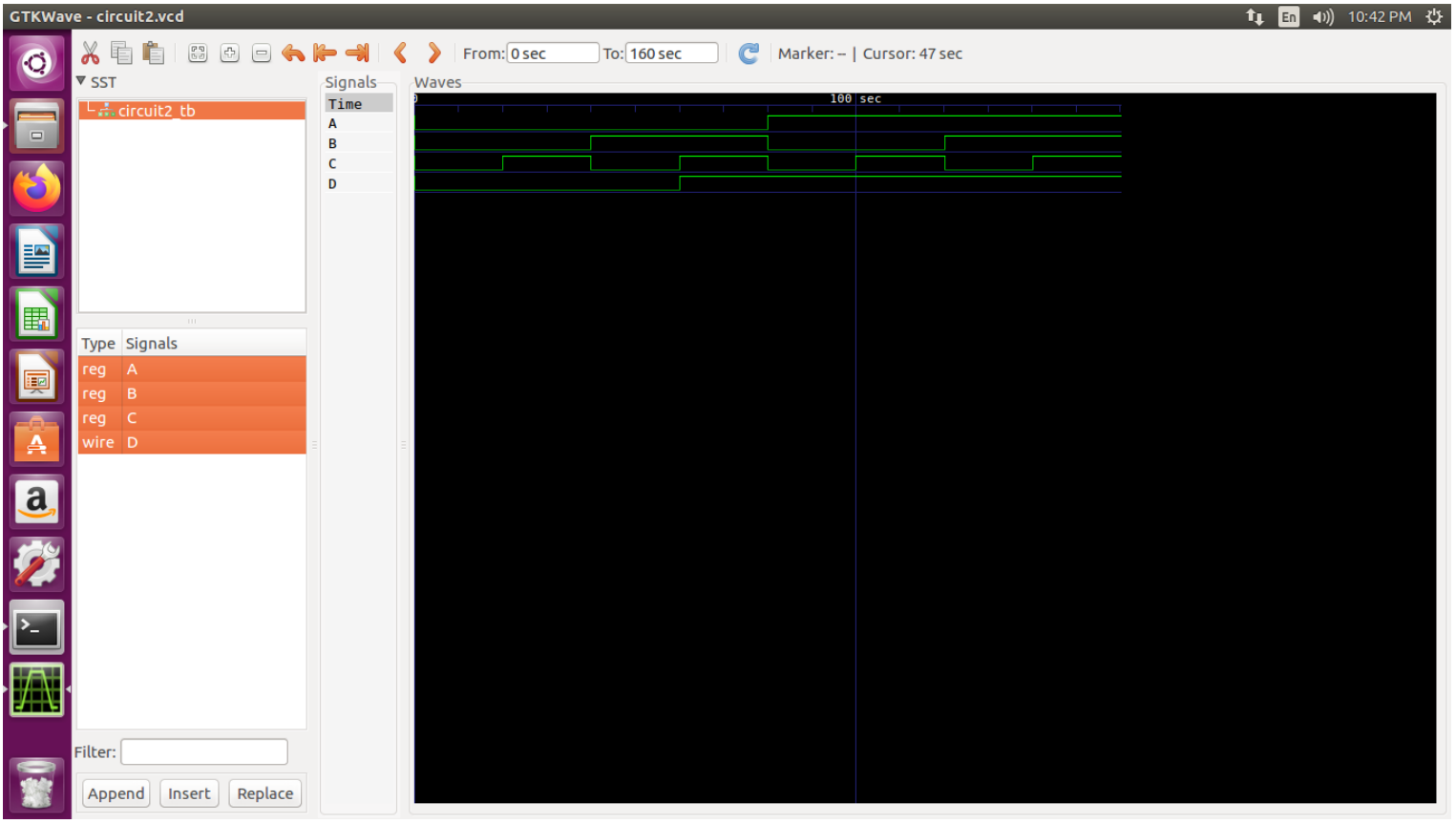
```
module circuit2_tb;
wire D;
reg A,B,C;
circuit2 M1(A,B,C,D);
initial
begin
$dumpfile("circuit2.vcd");
$dumpvars(1,circuit2_tb);

A=0;B=0;C=0;
#1 A=0;B=0;C=1;
#1 A=0;B=1;C=0;
#1 A=0;B=1;C=1;
#1 A=1;B=0;C=0;
#1 A=1;B=0;C=1;
#1 A=1;B=1;C=0;
#1 A=1;B=1;C=1;
#1;
end
initial
begin
$monitor($time," A=%b B=%b C=%b D=%b",A,B,C,D);
end
endmodule
```

Saving file '/home/mythreya/Desktop/verilog_files/week2/circuit2_tb.v'... Verilog Tab Width: 8 Ln 22, Col 18 INS

Output


Terminal
10:42 PM
week2
Home
Desktop
verilog_files
week2
Recent
Home
Desktop
Documents
Downloads
Music
Pictures
Videos
Trash
Network
Computer
Connect to Server
output_ screenshots
circuit2.v
output1
output2
tb_simple_circuit.v
mythreya@pes: ~/Desktop/verilog_files/week2
80A=1 B=0 C=0 D=1
100A=1 B=0 C=1 D=1
120A=1 B=1 C=0 D=1
140A=1 B=1 C=1 D=1
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit2_tb.v
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit2.v
mythreya@pes:~/Desktop/verilog_files/week2$ gtkwave circuit2.vcd
GTKWave Analyzer v3.3.66 (w)1999-2015 BSI
[0] start time.
[160] end time.
WM Destroy
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output2
VCD info: dumpfile circuit2.vcd opened for output.
0A=0 B=0 C=0 D=0
20A=0 B=0 C=1 D=0
40A=0 B=1 C=0 D=0
60A=0 B=1 C=1 D=1
80A=1 B=0 C=0 D=1
100A=1 B=0 C=1 D=1
120A=1 B=1 C=0 D=1
140A=1 B=1 C=1 D=1
mythreya@pes:~/Desktop/verilog_files/week2$


GTKWave - circuit2.vcd
10:42 PM
From: 0 sec
To: 160 sec
Marker: -- | Cursor: 47 sec
SST
circuit2_tb
Type
Signals
reg A
reg B
reg C
wire D
Filter:
Append
Insert
Replace
Signals
Time
A
B
C
D
Waves
100 sec

Circuit 3

File Edit View Search Tools Documents Help — 10:45 PM

Open — Save

```
module circuit3(A,B,C,D);
input A,B,C;
output D;
wire w1,w2,w3;
and G1(w1,C,B);
or G2(w2,A,w1);
and G3(w3,A,B);
or G4(D,w2,w3);
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/week2/circuit3.v'... Verilog Tab Width: 8 Ln 9, Col 10 INS

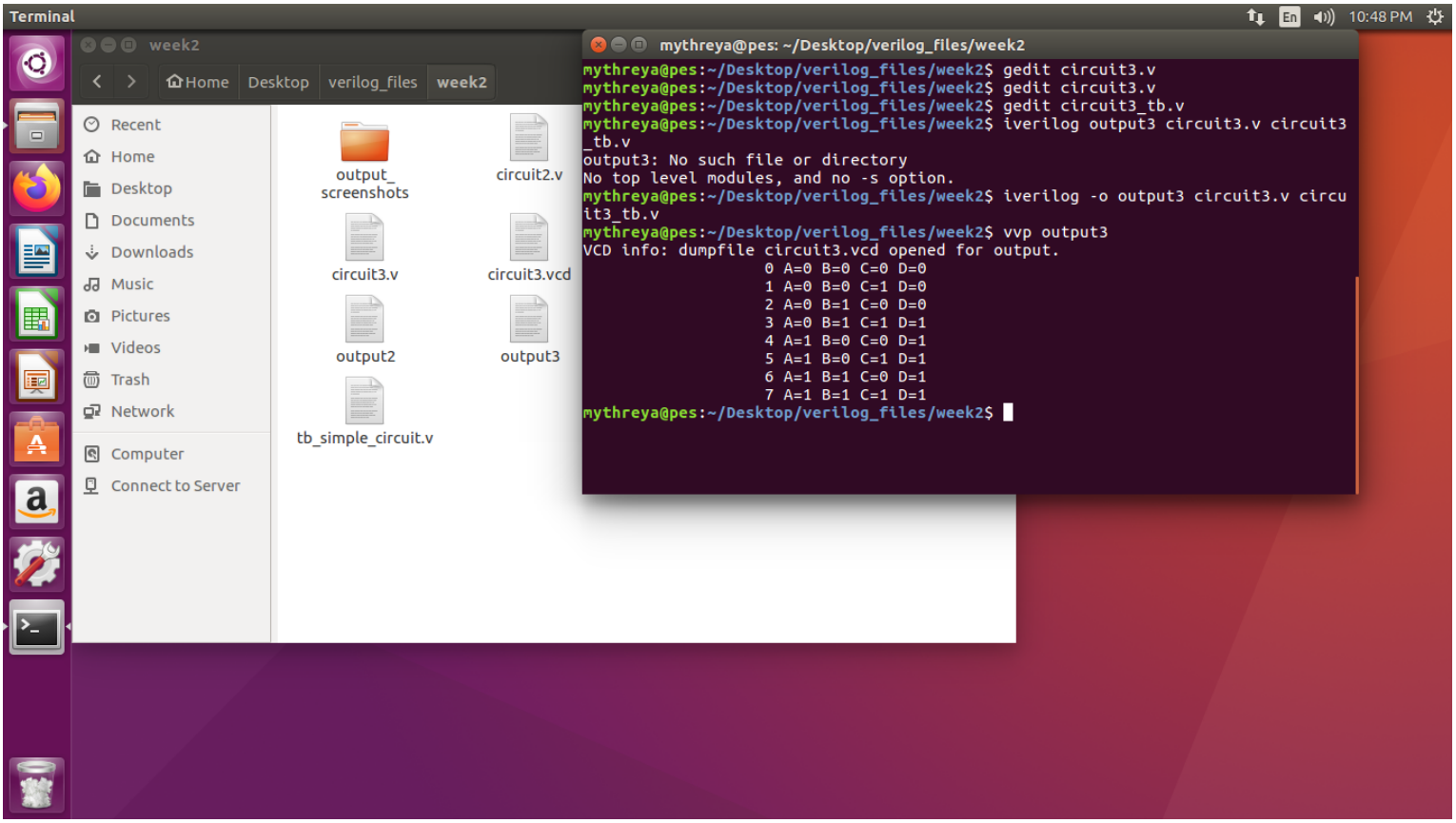
File Edit View Search Tools Documents Help — 10:48 PM

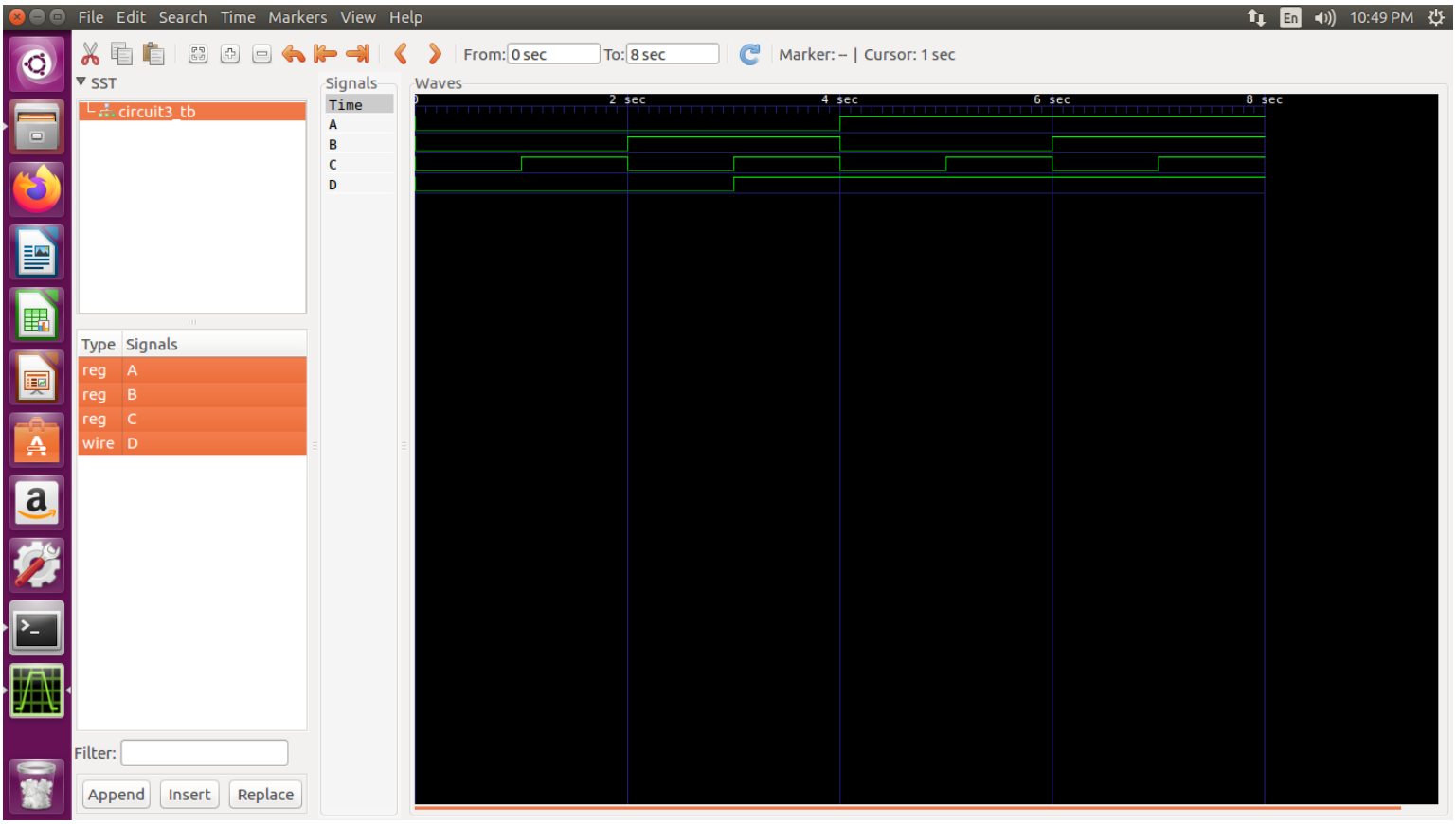
Open — Save

```
module circuit3_tb;
reg A,B,C;
wire D;
circuit3 M1(A,B,C,D);
initial
begin
A=0;B=0;C=0;
#1 A=0;B=0;C=1;
#1 A=0;B=1;C=0;
#1 A=0;B=1;C=1;
#1 A=1;B=0;C=0;
#1 A=1;B=0;C=1;
#1 A=1;B=1;C=0;
#1 A=1;B=1;C=1;
#1;
end
initial
begin
$monitor($time," A=%b B=%b C=%b D=%b",A,B,C,D);
end
initial
begin
$dumpfile("circuit3.vcd");
$dumpvars(1,circuit3_tb);
end
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/week2/circuit3_tb.v'... Verilog Tab Width: 8 Ln 26, Col 10 INS

Output


Terminal
10:48 PM
week2
Home
Desktop
verilog_files
week2
Recent
Home
Desktop
Documents
Downloads
Music
Pictures
Videos
Trash
Network
Computer
Connect to Server
output_ screenshots
circuit2.v
circuit3.v
circuit3.vcd
output2
output3
tb_simple_circuit.v
mythreya@pes: ~/Desktop/verilog_files/week2
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit3.v
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit3.v
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit3_tb.v
mythreya@pes:~/Desktop/verilog_files/week2$ iverilog output3 circuit3.v circuit3_tb.v
output3: No such file or directory
No top level modules, and no -s option.
mythreya@pes:~/Desktop/verilog_files/week2$ iverilog -o output3 circuit3.v circuit3_tb.v
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output3
VCD info: dumpfile circuit3.vcd opened for output.
0 A=0 B=0 C=0 D=0
1 A=0 B=0 C=1 D=0
2 A=0 B=1 C=0 D=0
3 A=0 B=1 C=1 D=1
4 A=1 B=0 C=0 D=1
5 A=1 B=0 C=1 D=1
6 A=1 B=1 C=0 D=1
7 A=1 B=1 C=1 D=1
mythreya@pes:~/Desktop/verilog_files/week2$


File Edit Search Time Markers View Help
10:49 PM
From: 0 sec
To: 8 sec
Marker: -- | Cursor: 1 sec
SST
circuit3_tb
Signals
Waves
Time
A
B
C
D
2 sec
4 sec
6 sec
8 sec
Type Signals
reg A
reg B
reg C
wire D
Filter:
Append
Insert
Replace

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Signature:

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SRN:

Section:

Date: