DDCO LAB SEM3

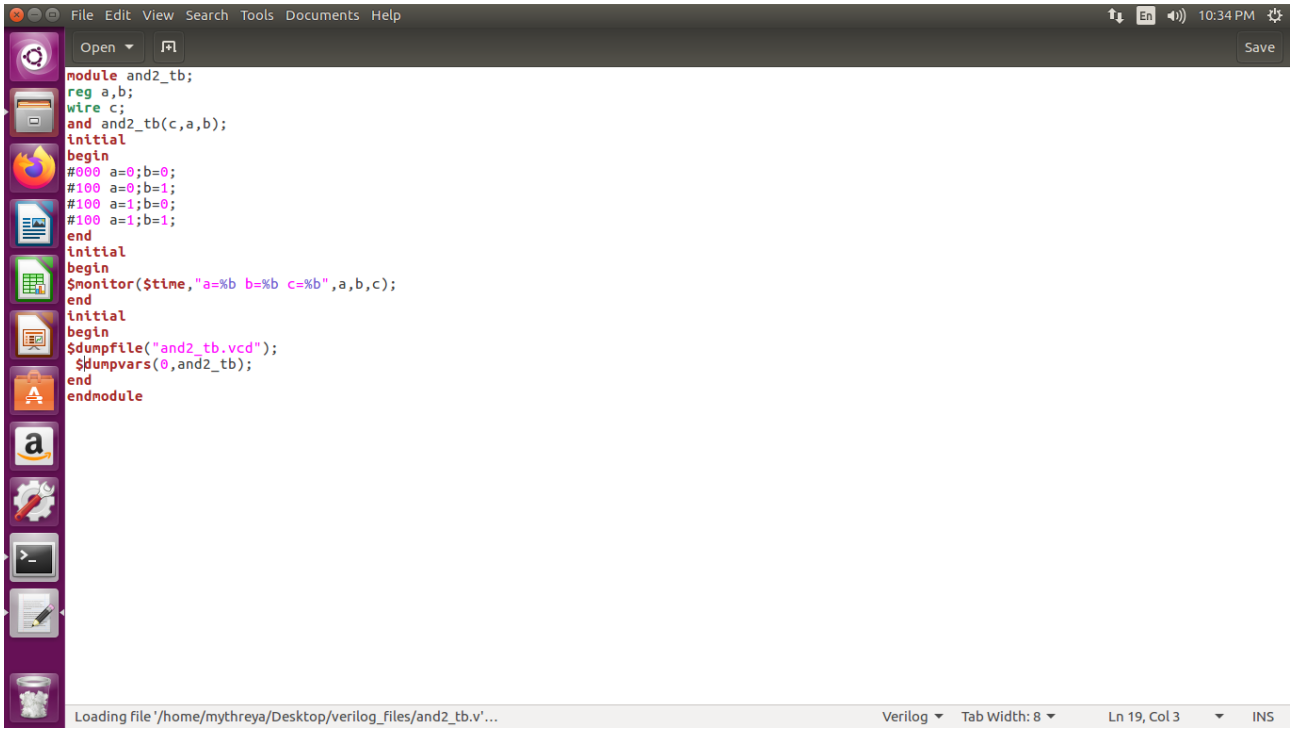
Name : H M Mythreya

SRN : PES2UG20CS130

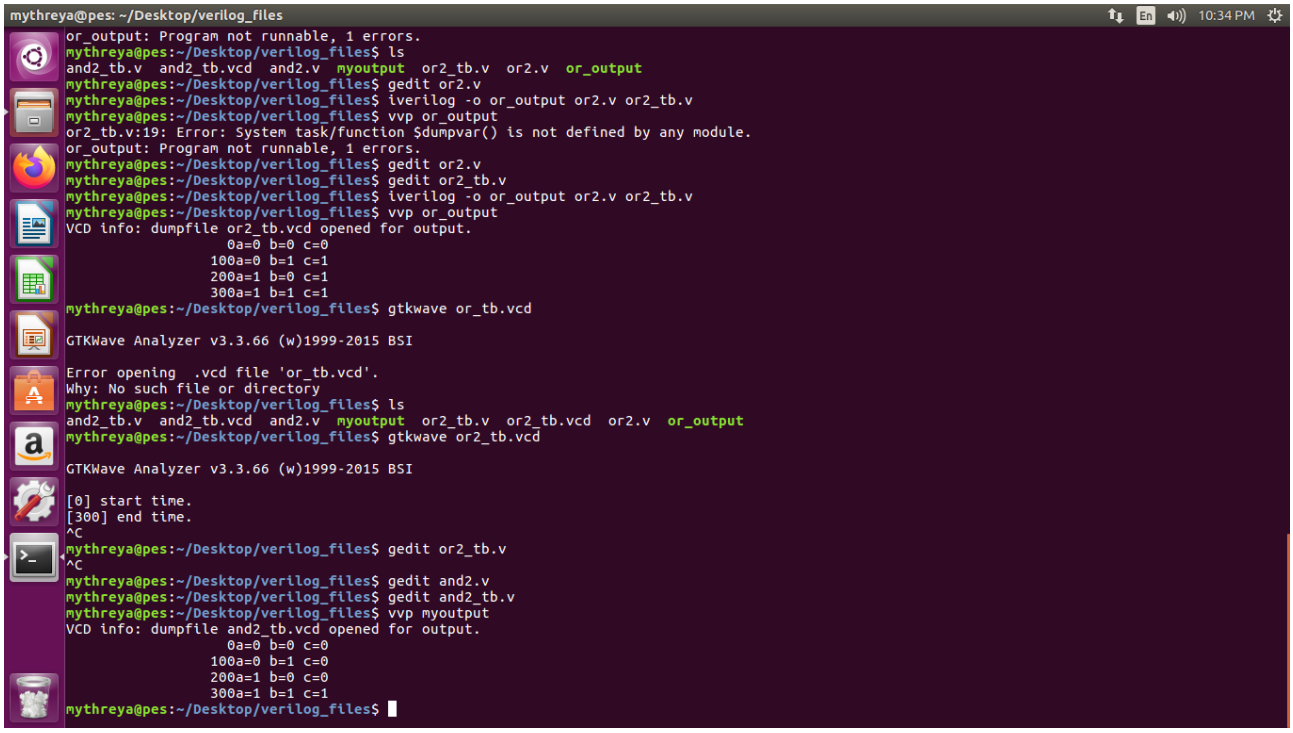
Section : C

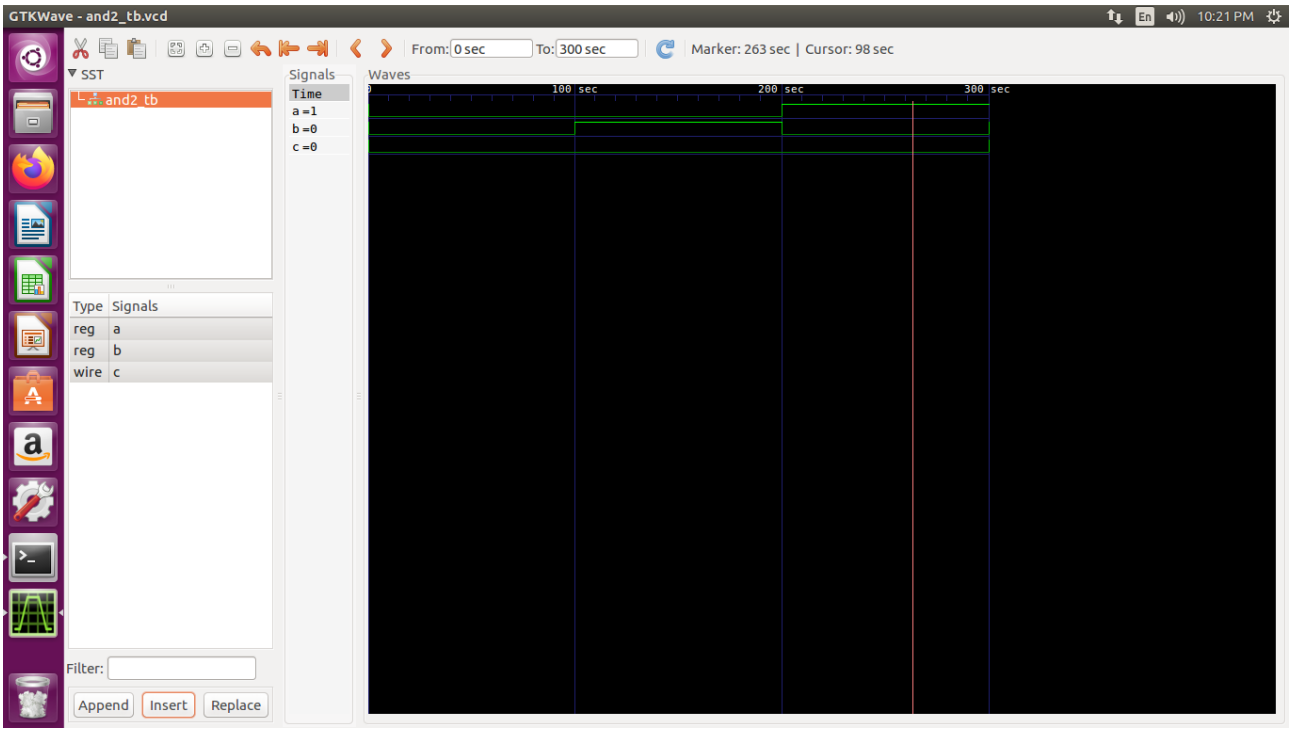
Week 1: Basic gates

And Gate



Output


mythreya@pes: ~/Desktop/verilog_files
10:34 PM
or_output: Program not runnable, 1 errors.
mythreya@pes:~/Desktop/verilog_files$ ls
and2_tb.v and2_tb.vcd and2.v myoutput or2_tb.v or2.v or_output
mythreya@pes:~/Desktop/verilog_files$ gedit or2.v
mythreya@pes:~/Desktop/verilog_files$ iverilog -o or_output or2.v or2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp or_output
or2_tb.v:19: Error: System task/function $dumpvar() is not defined by any module.
or_output: Program not runnable, 1 errors.
mythreya@pes:~/Desktop/verilog_files$ gedit or2.v
mythreya@pes:~/Desktop/verilog_files$ gedit or2_tb.v
mythreya@pes:~/Desktop/verilog_files$ iverilog -o or_output or2.v or2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp or_output
VCD info: dumpfile or2_tb.vcd opened for output.
0a=0 b=0 c=0
100a=0 b=1 c=1
200a=1 b=0 c=1
300a=1 b=1 c=1
mythreya@pes:~/Desktop/verilog_files$ gtkwave or_tb.vcd
GTKWave Analyzer v3.3.66 (w)1999-2015 BSI
Error opening .vcd file 'or_tb.vcd'.
Why: No such file or directory
mythreya@pes:~/Desktop/verilog_files$ ls
and2_tb.v and2_tb.vcd and2.v myoutput or2_tb.v or2_tb.vcd or2.v or_output
mythreya@pes:~/Desktop/verilog_files$ gtkwave or2_tb.vcd
GTKWave Analyzer v3.3.66 (w)1999-2015 BSI
[0] start time.
[300] end time.
^C
mythreya@pes:~/Desktop/verilog_files$ gedit or2_tb.v
^C
mythreya@pes:~/Desktop/verilog_files$ gedit and2.v
mythreya@pes:~/Desktop/verilog_files$ gedit and2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp myoutput
VCD info: dumpfile and2_tb.vcd opened for output.
0a=0 b=0 c=0
100a=0 b=1 c=0
200a=1 b=0 c=0
300a=1 b=1 c=1
mythreya@pes:~/Desktop/verilog_files$


GTKWave - and2_tb.vcd
10:21 PM
From: 0 sec
To: 300 sec
Marker: 263 sec | Cursor: 98 sec
SST
and2_tb
Signals
Time
a =1
b =0
c =0
Waves
100 sec
200 sec
300 sec
Type Signals
reg a
reg b
wire c
Filter:
Append
Insert
Replace

Or Gate

File Edit View Search Tools Documents Help — 10:34 PM

Open — Save

```
module or2(c,a,b);
input a,b;
output c;
assign c = a|b;
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/or2.v'... Verilog Tab Width: 8 Ln 4, Col 14 INS

File Edit View Search Tools Documents Help — 10:34 PM

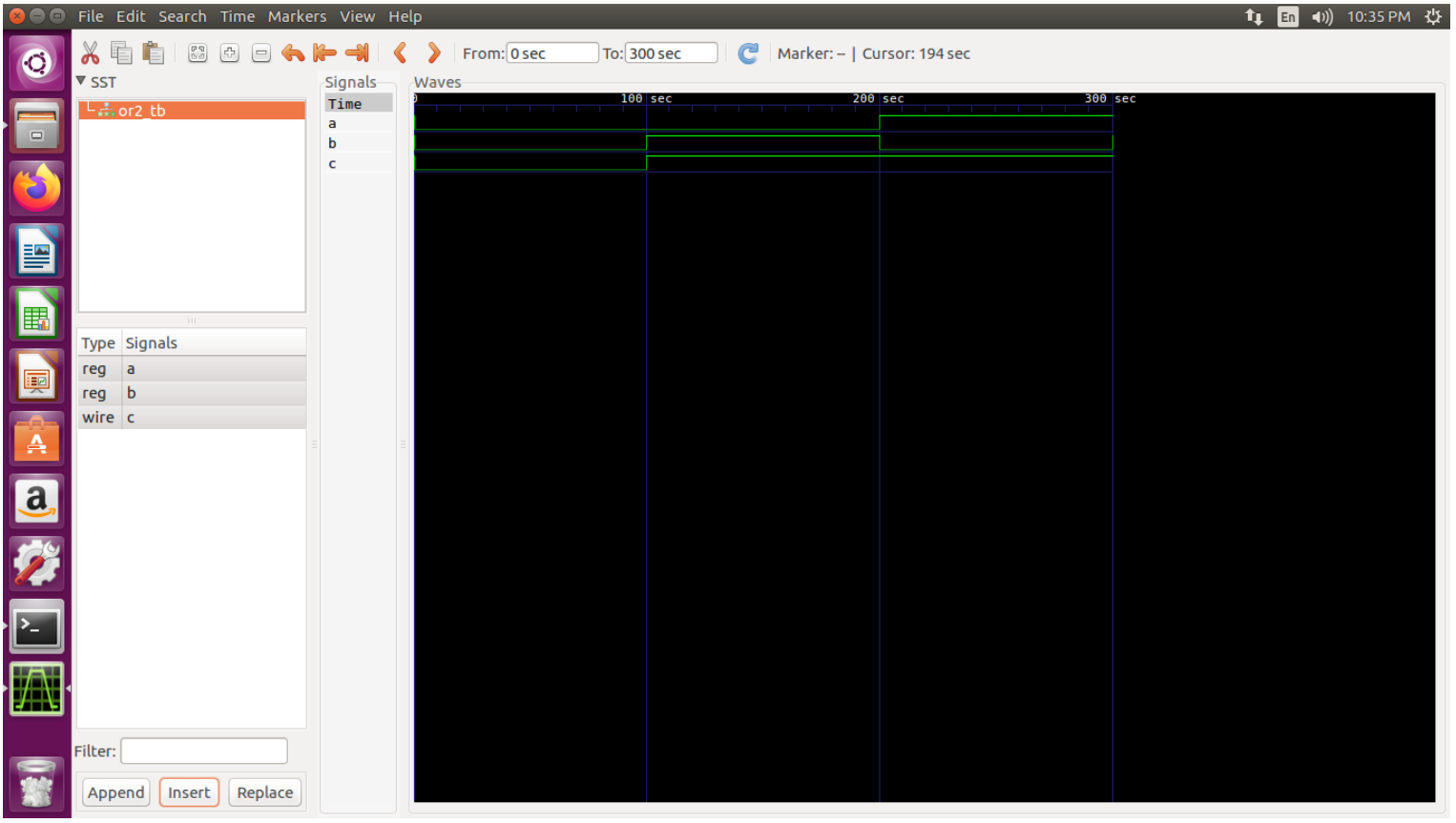
Open — Save

```
module or2_tb;
reg a,b;
wire c;
or or2_tb(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
end
initial
begin
$monitor($time,"a=%b b=%b c=%b",a,b,c);
end
initial
begin
$dumpfile("or2_tb.vcd");
 $dumpvars(0,or2_tb);
end
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/or2_tb.v'... Verilog Tab Width: 8 Ln 19, Col 11 INS

Output

```
mythreya@pes: ~/Desktop/verilog_files
mythreya@pes:~/Desktop/verilog_files$ gedit or2.v
mythreya@pes:~/Desktop/verilog_files$ gedit or2_tb.v
mythreya@pes:~/Desktop/verilog_files$ iverilog -o or_output or2.v or2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp or_output
VCD info: dumpfile or2_tb.vcd opened for output.
                  0a=0 b=0 c=0
                100a=0 b=1 c=1
                200a=1 b=0 c=1
                300a=1 b=1 c=1
mythreya@pes:~/Desktop/verilog_files$ gtkwave or_tb.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

Error opening  .vcd file 'or_tb.vcd'.
Why: No such file or directory
mythreya@pes:~/Desktop/verilog_files$ ls
and2_tb.v  and2_tb.vcd  and2.v  myoutput  or2_tb.v  or2_tb.vcd  or2.v  or_output
mythreya@pes:~/Desktop/verilog_files$ gtkwave or2_tb.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[300] end time.
^C
mythreya@pes:~/Desktop/verilog_files$ gedit or2_tb.v
^C
mythreya@pes:~/Desktop/verilog_files$ gedit and2.v
mythreya@pes:~/Desktop/verilog_files$ gedit and2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp myoutput
VCD info: dumpfile and2_tb.vcd opened for output.
                  0a=0 b=0 c=0
                100a=0 b=1 c=0
                200a=1 b=0 c=0
                300a=1 b=1 c=1
mythreya@pes:~/Desktop/verilog_files$ gedit or2.v
mythreya@pes:~/Desktop/verilog_files$ gedit or2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp or_output
VCD info: dumpfile or2_tb.vcd opened for output.
                  0a=0 b=0 c=0
                100a=0 b=1 c=1
                200a=1 b=0 c=1
                300a=1 b=1 c=1
mythreya@pes:~/Desktop/verilog_files$
```



Xor Gate

File Edit View Search Tools Documents Help — 10:45 PM

Open — Save

```
module xor2(c,a,b);
input a,b;
output c;
assign c = a^b;
endmodule
```

Loading file '/home/mythreya/Desktop/verilog_files/xor2.v'... Verilog Tab Width: 8 Ln 5, Col 10 INS

File Edit View Search Tools Documents Help — 10:45 PM

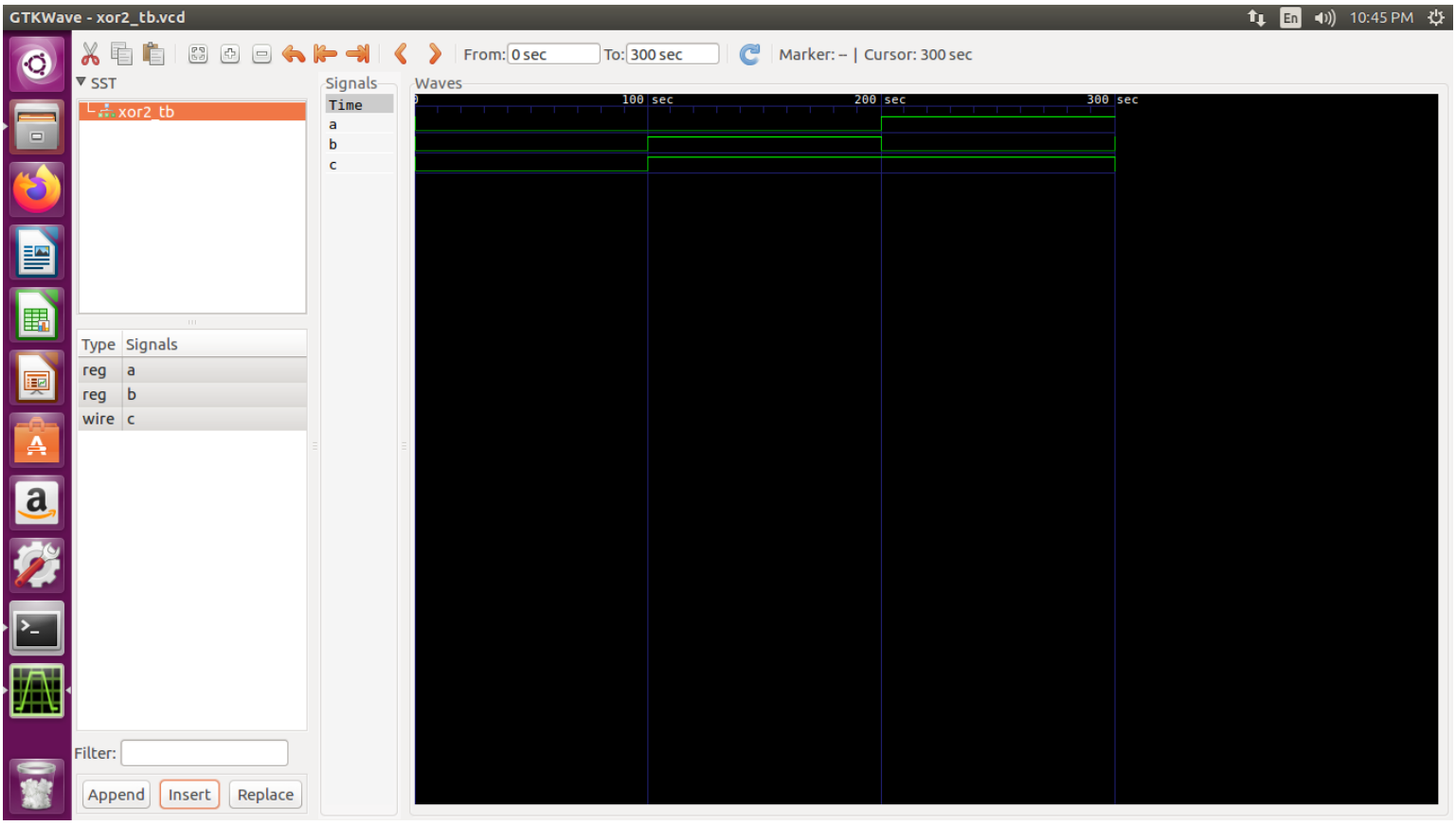
Open — Save

```
module xor2_tb;
reg a,b;
wire c;
xor xor2_tb(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("xor2_tb.vcd");
 $dumpvars(0,xor2_tb);
end
endmodule
```

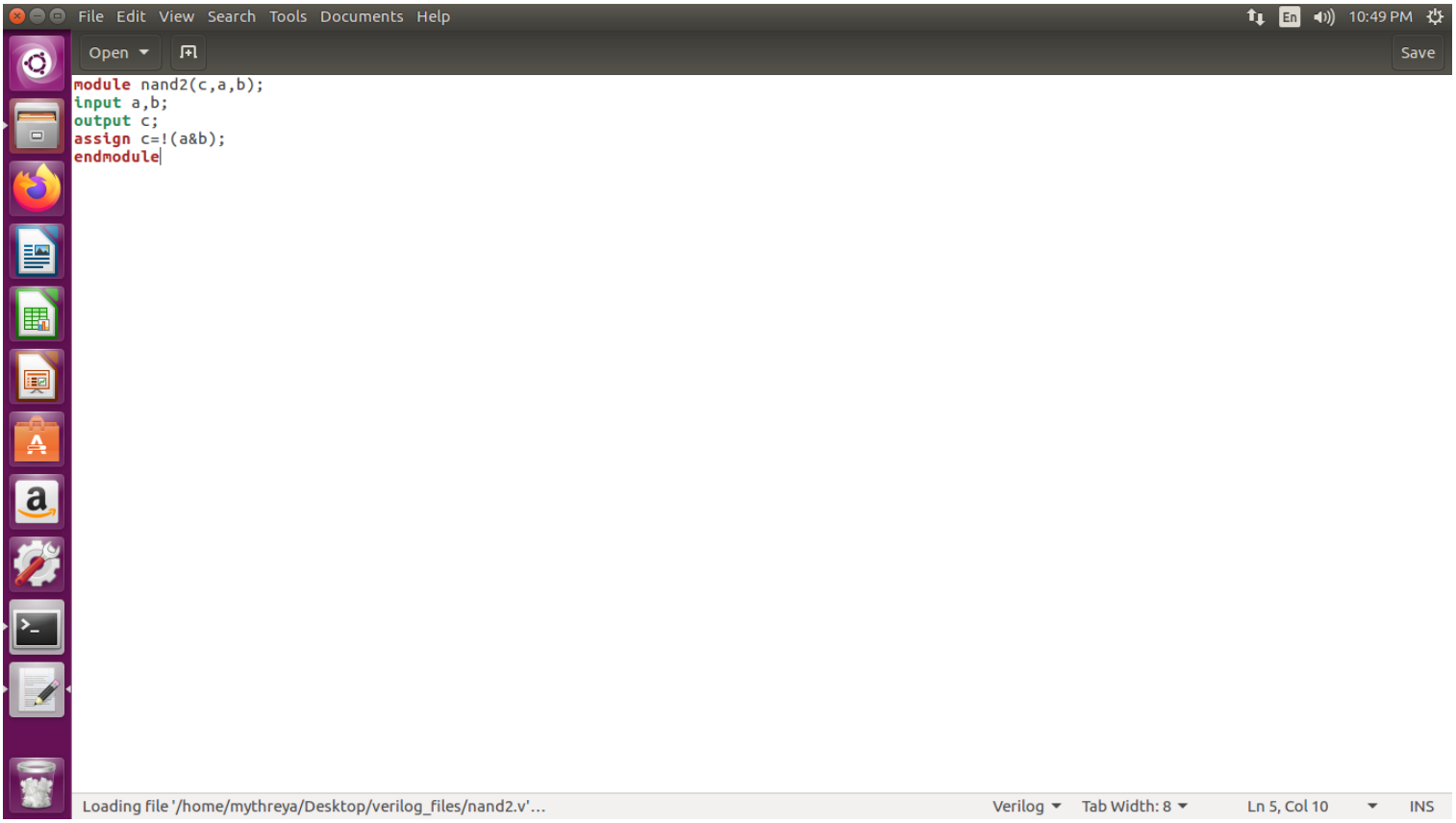
Loading file '/home/mythreya/Desktop/verilog_files/xor2_tb.v'... Verilog Tab Width: 8 Ln 21, Col 10 INS

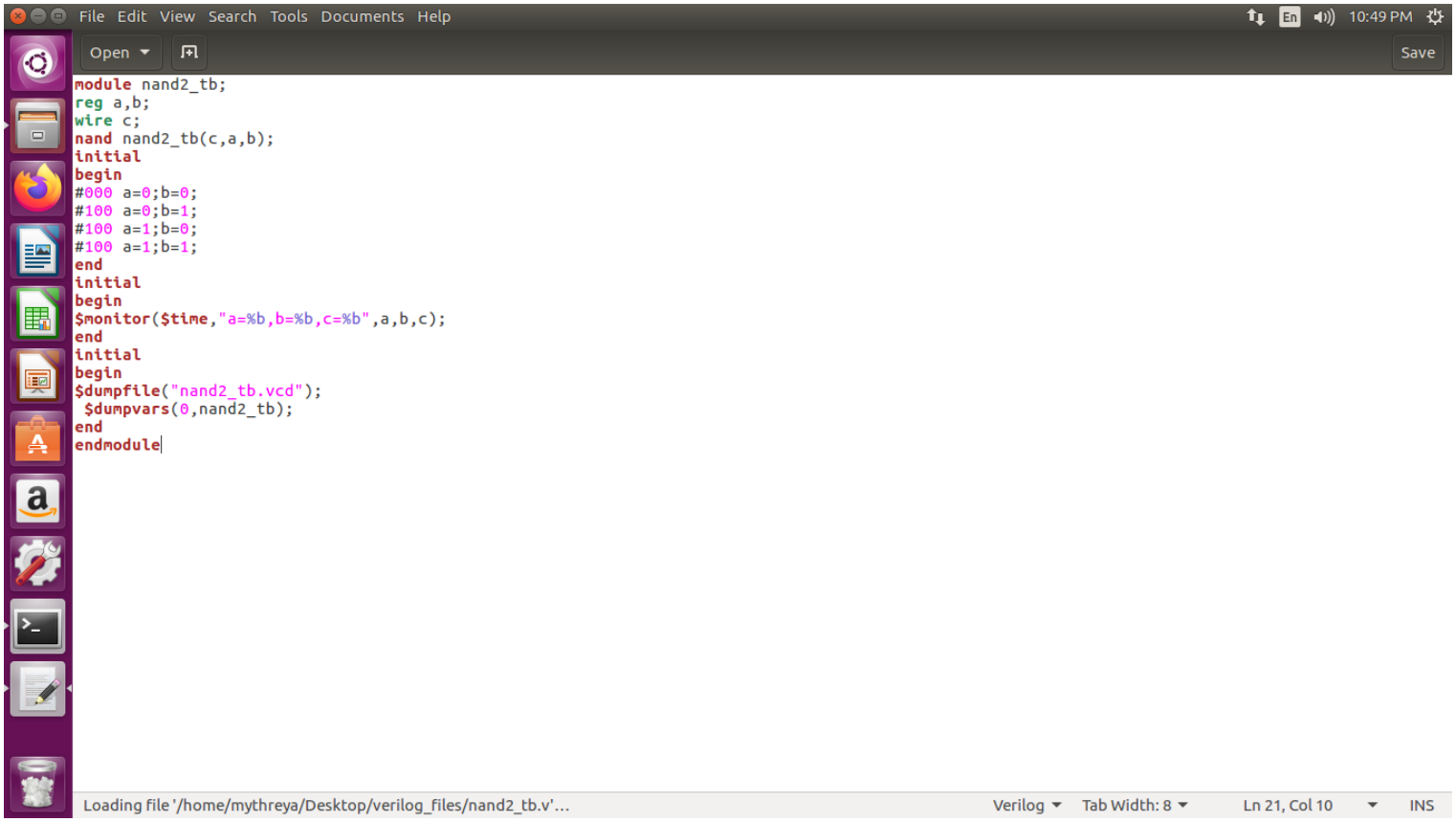
Output

```
mythreya@pes: ~/Desktop/verilog_files
mythreya@pes:~/Desktop/verilog_files$ gedit xor2.v
mythreya@pes:~/Desktop/verilog_files$ gedit xor2_tb.v
mythreya@pes:~/Desktop/verilog_files$ iverilog -o xor_output xor2.v xor2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp xor_output
VCD info: dumpfile xor2_tb.vcd opened for output.
                  0a=0,b=0,c=0
                100a=0,b=1,c=1
                200a=1,b=0,c=1
                300a=1,b=1,c=0
mythreya@pes:~/Desktop/verilog_files$ gtkwave xor2_tb.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[300] end time.
WM Destroy
mythreya@pes:~/Desktop/verilog_files$ gedit xor2.v
mythreya@pes:~/Desktop/verilog_files$ gedit xor2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp xor_output
VCD info: dumpfile xor2_tb.vcd opened for output.
                  0a=0,b=0,c=0
                100a=0,b=1,c=1
                200a=1,b=0,c=1
                300a=1,b=1,c=0
mythreya@pes:~/Desktop/verilog_files$
```



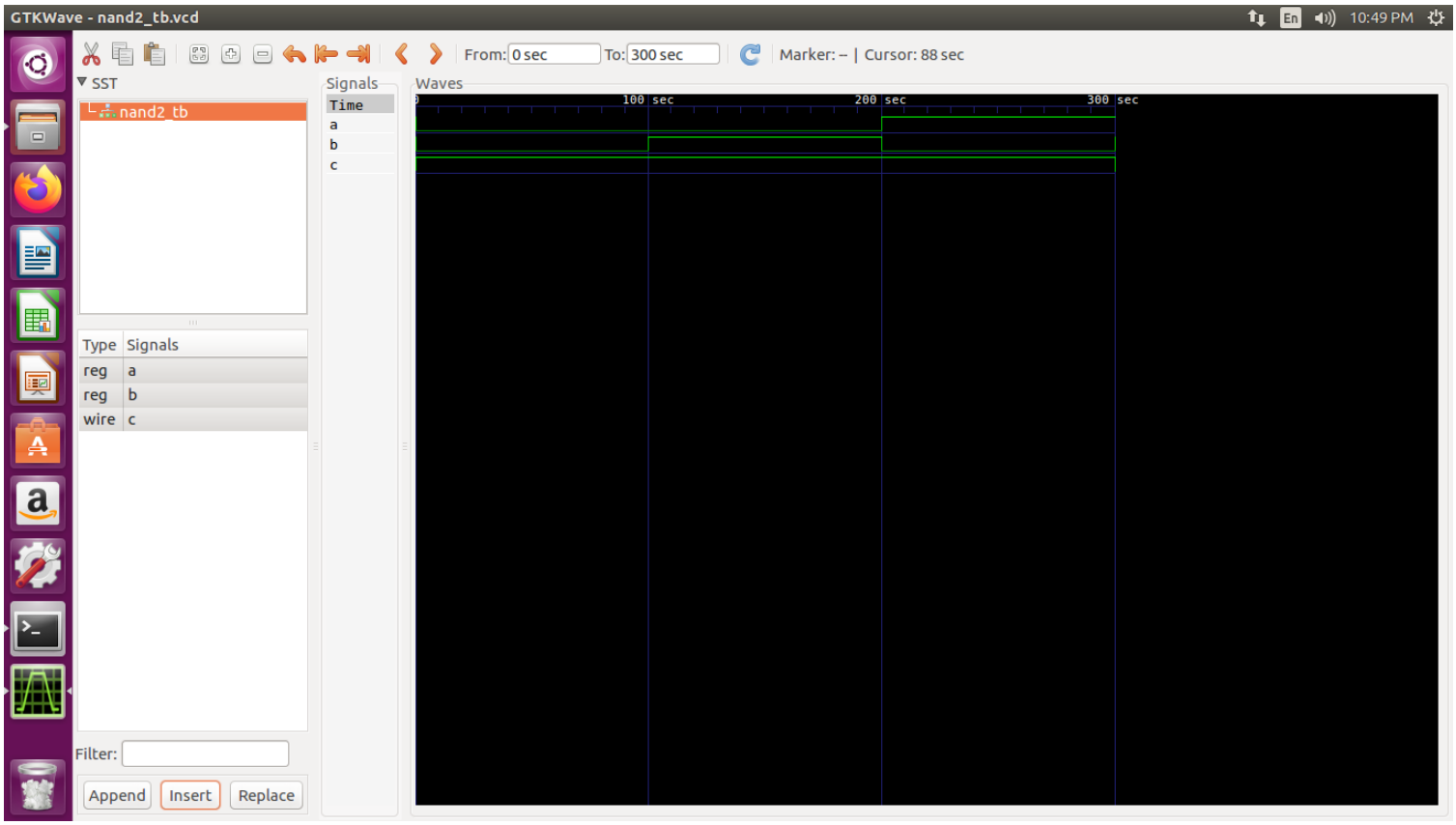
Nand Gate


File Edit View Search Tools Documents Help
10:49 PM
Open
Save
module nand2(c,a,b);
input a,b;
output c;
assign c=!(a&b);
endmodule
Loading file '/home/mythreya/Desktop/verilog_files/nand2.v'...
Verilog
Tab Width: 8
Ln 5, Col 10
INS


File Edit View Search Tools Documents Help
10:49 PM
Open
Save
module nand2_tb;
reg a,b;
wire c;
nand nand2_tb(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("nand2_tb.vcd");
$dumpvars(0,nand2_tb);
end
endmodule
Loading file '/home/mythreya/Desktop/verilog_files/nand2_tb.v'...
Verilog
Tab Width: 8
Ln 21, Col 10
INS

Output

```
mythreya@pes: ~/Desktop/verilog_files
mythreya@pes:~/Desktop/verilog_files$ gedit nand2.v
mythreya@pes:~/Desktop/verilog_files$ gedit nand2_tb.v
mythreya@pes:~/Desktop/verilog_files$ iverilog -o nand_output nand2.v nand2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp nand_output
VCD info: dumpfile nand2_tb.vcd opened for output.
                    0a=0,b=0,c=1
                  100a=0,b=1,c=1
                  200a=1,b=0,c=1
                  300a=1,b=1,c=0
mythreya@pes:~/Desktop/verilog_files$ gtkwave nand2_tb.vcd

GTKWave Analyzer v3.3.66 (w)1999-2015 BSI

[0] start time.
[300] end time.
WM Destroy
mythreya@pes:~/Desktop/verilog_files$ gedit nand2.v
mythreya@pes:~/Desktop/verilog_files$ gedit nand2_tb.v
mythreya@pes:~/Desktop/verilog_files$ vvp nand_output
VCD info: dumpfile nand2_tb.vcd opened for output.
                    0a=0,b=0,c=1
                  100a=0,b=1,c=1
                  200a=1,b=0,c=1
                  300a=1,b=1,c=0
mythreya@pes:~/Desktop/verilog_files$
```



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· The programs and output submitted is duly written, verified and executed by me.

· I have not copied from any of my peers nor from the external resource such as internet.

· If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name:

SRN:

Section:

Date: