DDCO LAB SEM3

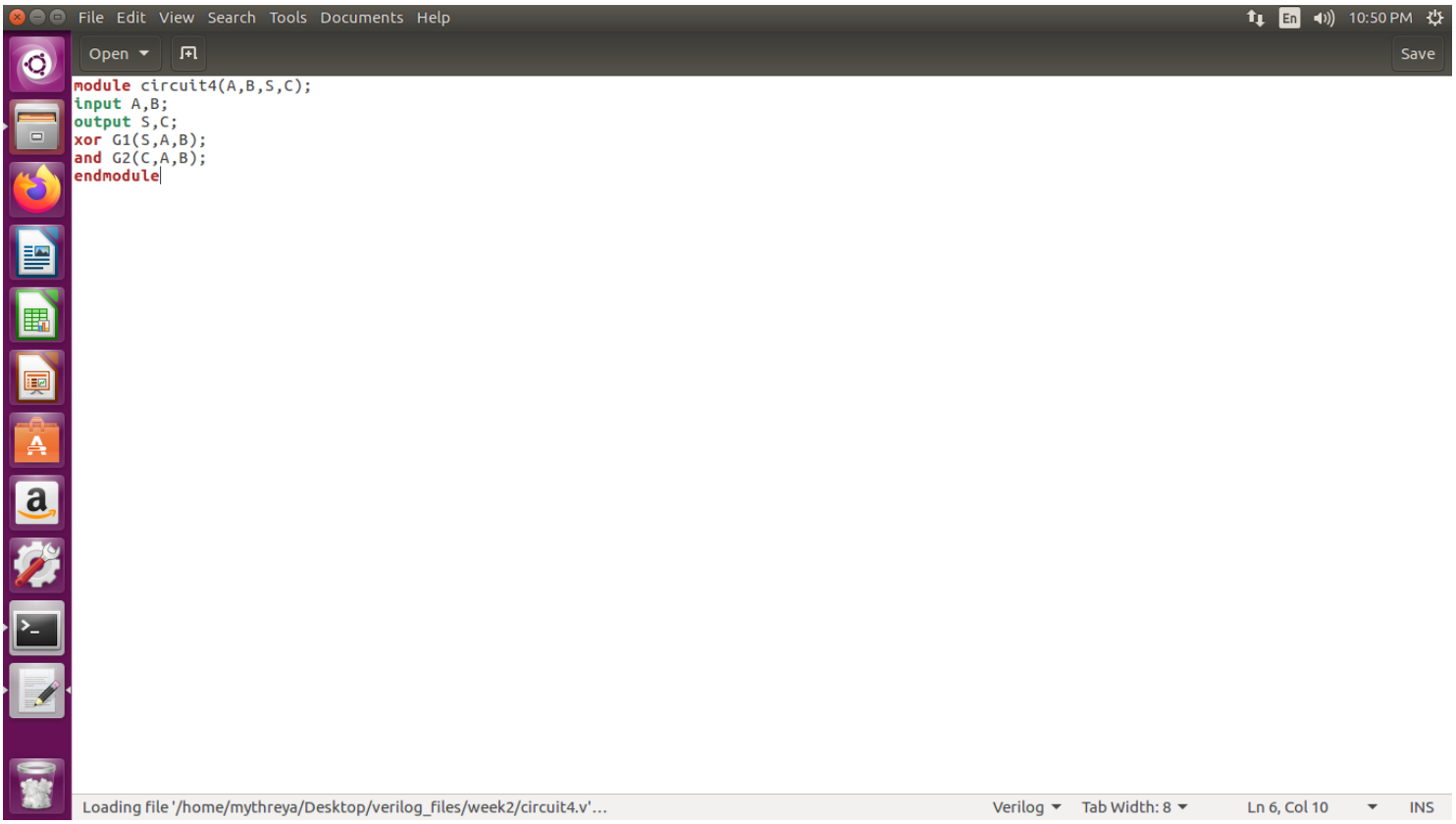
Name : H M Mythreya

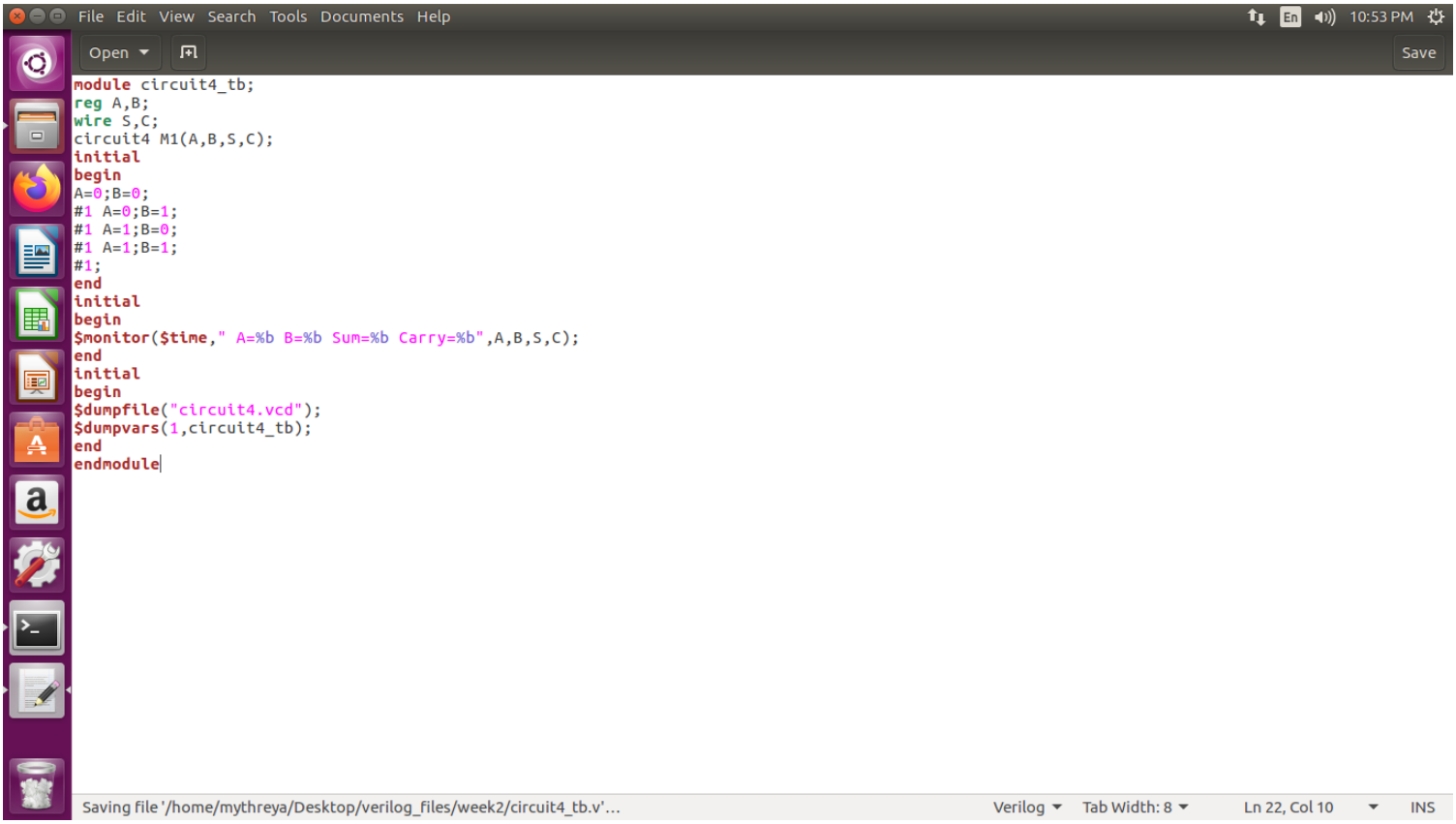
SRN : PES2UG20CS130

Section : C

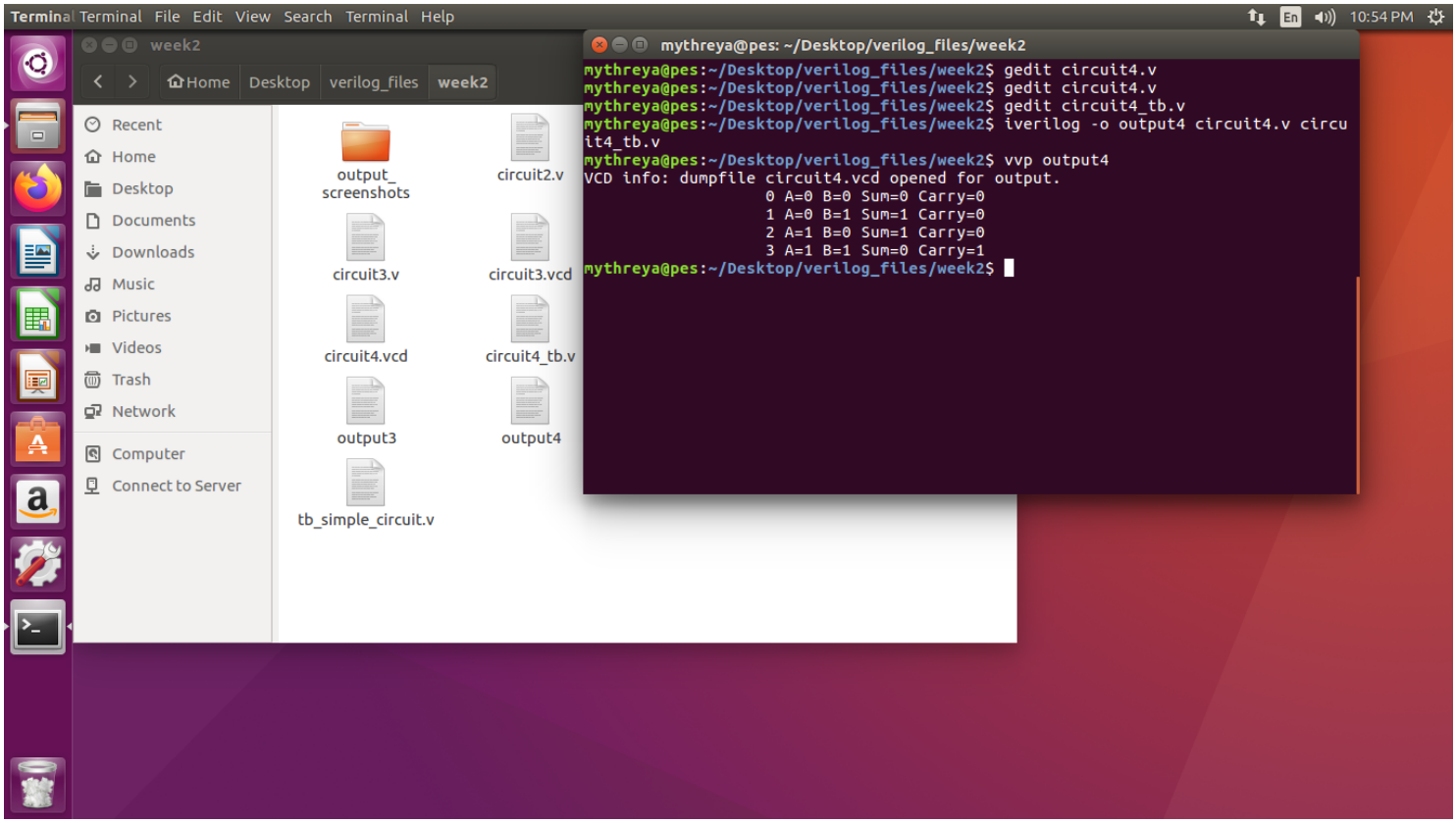
Week 3: Adders

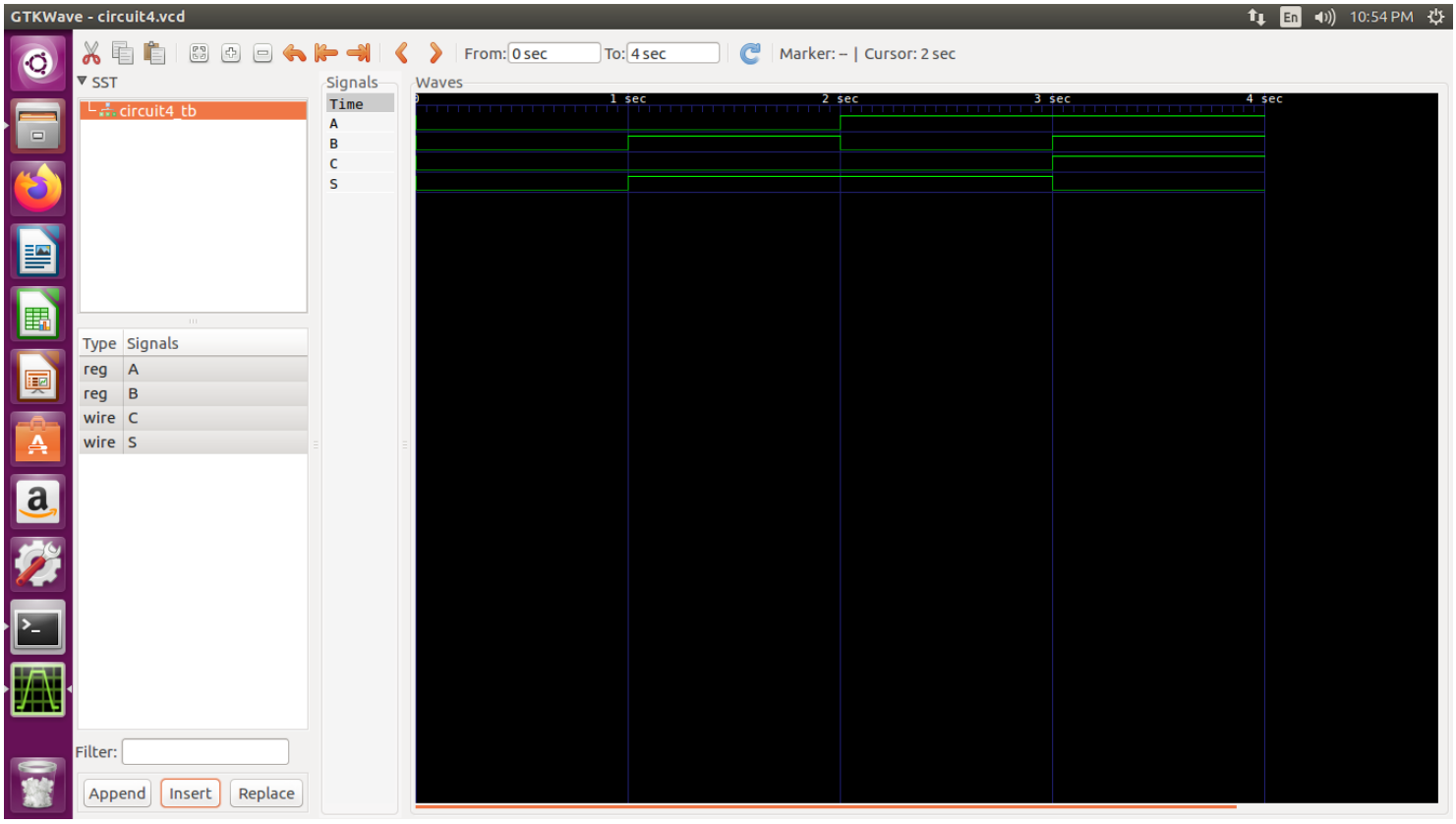
Half Adder





Output


Terminal Terminal File Edit View Search Terminal Help
10:54 PM
week2
Home Desktop verilog_files week2
Recent
Home
Desktop
Documents
Downloads
Music
Pictures
Videos
Trash
Network
Computer
Connect to Server
output_ screenshots
circuit2.v
circuit3.v
circuit3.vcd
circuit4.vcd
circuit4_tb.v
output3
output4
tb_simple_circuit.v
mythreya@pes: ~/Desktop/verilog_files/week2
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit4.v
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit4.v
mythreya@pes:~/Desktop/verilog_files/week2$ gedit circuit4_tb.v
mythreya@pes:~/Desktop/verilog_files/week2$ iverilog -o output4 circuit4.v circuit4_tb.v
mythreya@pes:~/Desktop/verilog_files/week2$ vvp output4
VCD info: dumpfile circuit4.vcd opened for output.
0 A=0 B=0 Sum=0 Carry=0
1 A=0 B=1 Sum=1 Carry=0
2 A=1 B=0 Sum=1 Carry=0
3 A=1 B=1 Sum=0 Carry=1
mythreya@pes:~/Desktop/verilog_files/week2$


GTKWave - circuit4.vcd
10:54 PM
From: 0 sec
To: 4 sec
Marker: -- | Cursor: 2 sec
SST
circuit4_tb
Signals
Time
A
B
C
S
Waves
1 sec
2 sec
3 sec
4 sec
Type Signals
reg A
reg B
wire C
wire S
Filter:
Append
Insert
Replace

Full Adder

File Edit View Search Tools Documents Help — 11:11 PM

Open — Save

```
module fulladder(A,B,Ci,S,Co);
input A,B,Ci;
output S,Co;
wire w1,w2,w3,w4,w5,w6;
xor G1(w1,A,B);
xor G2(S,Ci,w1);
and G3(w2,A,B);
and G4(w3,B,C);
and G5(w4,C,A);
or G6(w5,w2,w3);
or G7(w6,w5,w4);
endmodule
```

Saving file '/home/mythreya/Pictures/fulladder.v'... Verilog Tab Width: 8 Ln 13, Col 1 INS

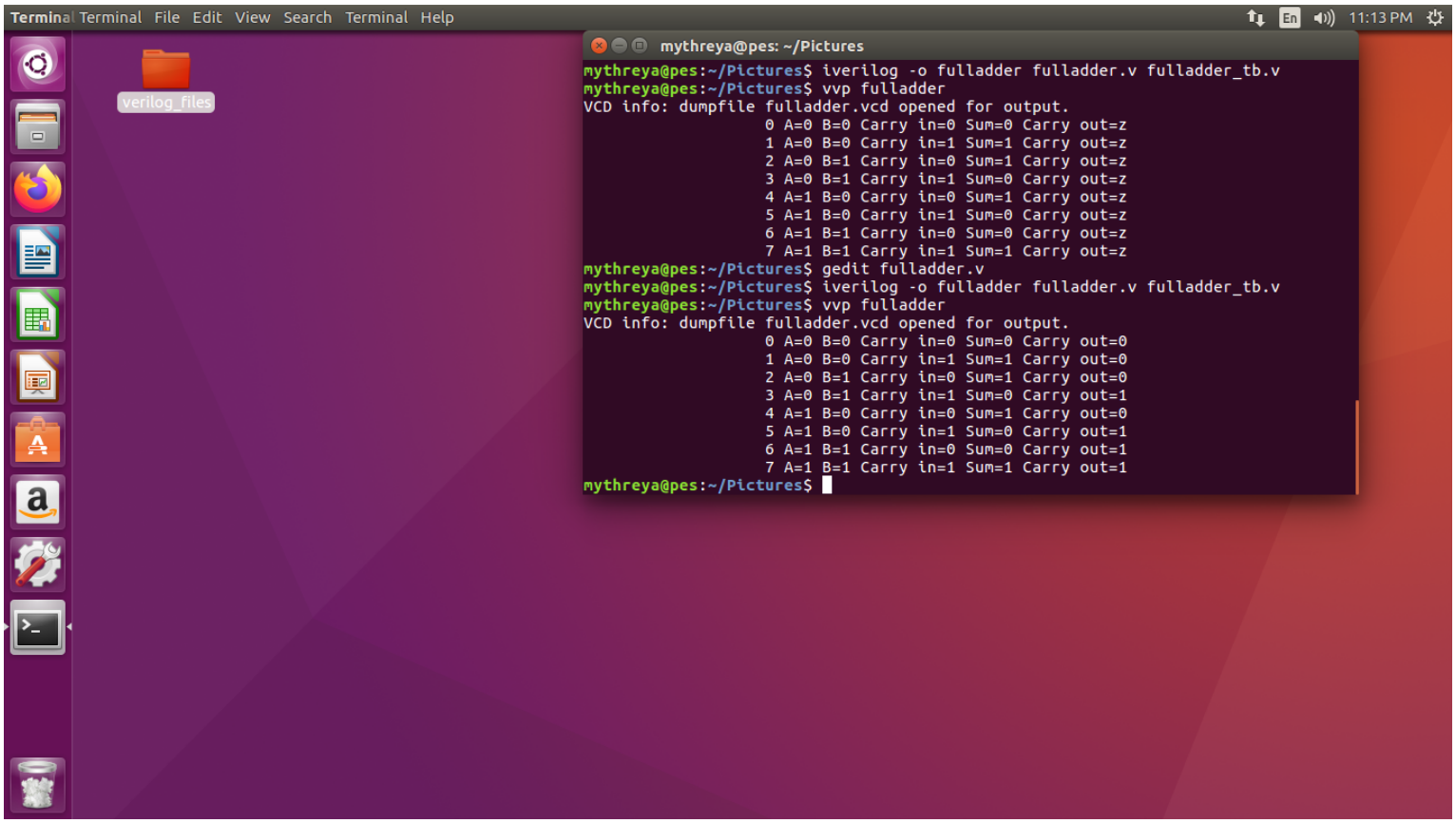
fulladder_tb.v (~/Pictures) - gedit — 11:04 PM

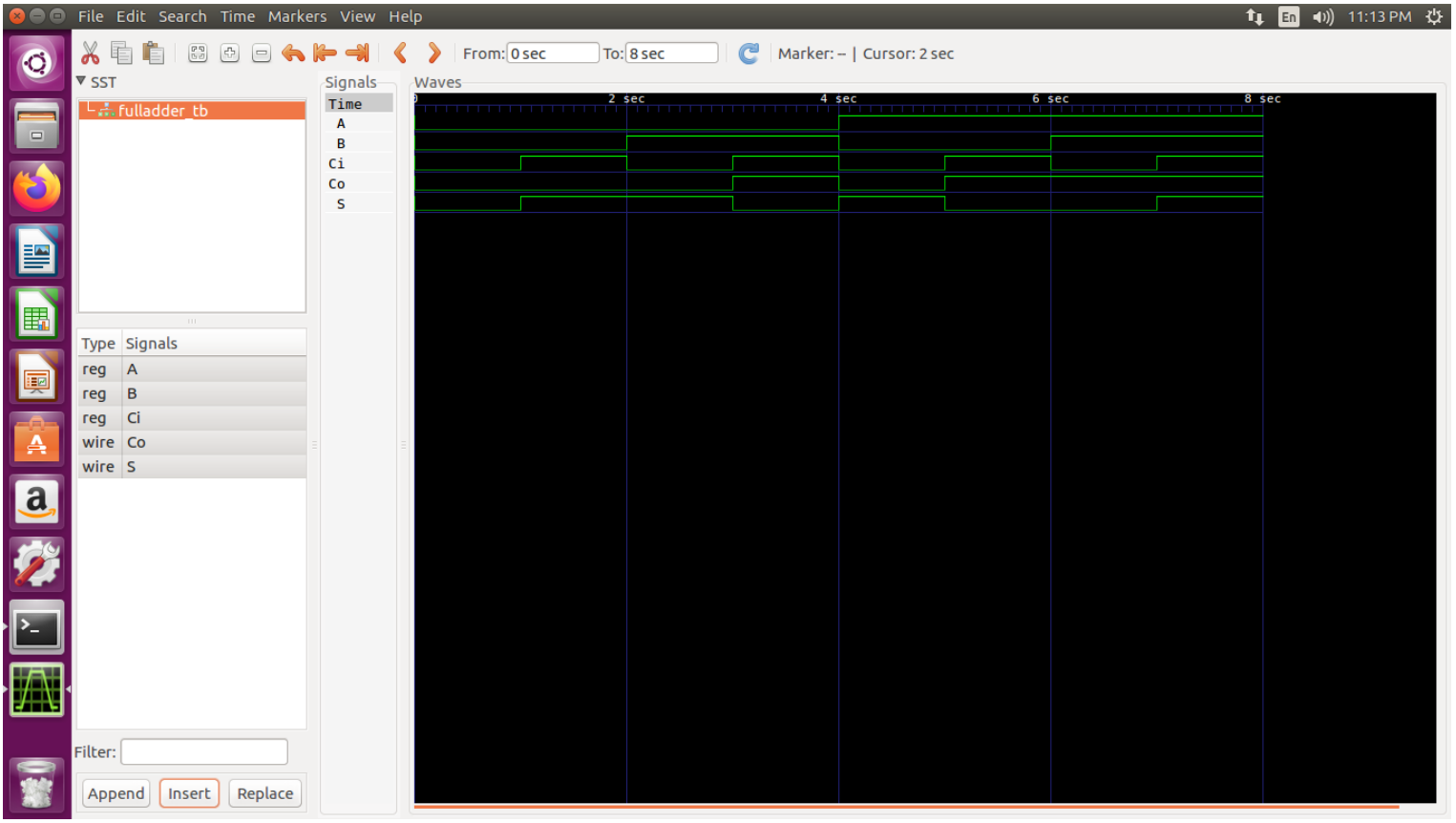
Open — Save

```
module fulladder_tb;
reg A,B,Ci;
wire S,Co;
fulladder M1(A,B,Ci,S,Co);
initial
begin
A=0;B=0;Ci=0;
#1 A=0;B=0;Ci=1;
#1 A=0;B=1;Ci=0;
#1 A=0;B=1;Ci=1;
#1 A=1;B=0;Ci=0;
#1 A=1;B=0;Ci=1;
#1 A=1;B=1;Ci=0;
#1 A=1;B=1;Ci=1;
#1;
end
initial
begin
$monitor($time," A=%b B=%b Carry in=%b Sum=%b Carry out=%b",A,B,Ci,S,Co);
end
initial
begin
$dumpfile("fulladder.vcd");
$dumpvars(1,fulladder_tb);
end
endmodule
```

Verilog Tab Width: 8 Ln 26, Col 10 INS

Output


Terminal Terminal File Edit View Search Terminal Help
11:13 PM
verilog_files
mythreya@pes: ~/Pictures
mythreya@pes:~/Pictures$ iverilog -o fulladder fulladder.v fulladder_tb.v
mythreya@pes:~/Pictures$ vvp fulladder
VCD info: dumpfile fulladder.vcd opened for output.
0 A=0 B=0 Carry in=0 Sum=0 Carry out=z
1 A=0 B=0 Carry in=1 Sum=1 Carry out=z
2 A=0 B=1 Carry in=0 Sum=1 Carry out=z
3 A=0 B=1 Carry in=1 Sum=0 Carry out=z
4 A=1 B=0 Carry in=0 Sum=1 Carry out=z
5 A=1 B=0 Carry in=1 Sum=0 Carry out=z
6 A=1 B=1 Carry in=0 Sum=0 Carry out=z
7 A=1 B=1 Carry in=1 Sum=1 Carry out=z
mythreya@pes:~/Pictures$ gedit fulladder.v
mythreya@pes:~/Pictures$ iverilog -o fulladder fulladder.v fulladder_tb.v
mythreya@pes:~/Pictures$ vvp fulladder
VCD info: dumpfile fulladder.vcd opened for output.
0 A=0 B=0 Carry in=0 Sum=0 Carry out=0
1 A=0 B=0 Carry in=1 Sum=1 Carry out=0
2 A=0 B=1 Carry in=0 Sum=1 Carry out=0
3 A=0 B=1 Carry in=1 Sum=0 Carry out=1
4 A=1 B=0 Carry in=0 Sum=1 Carry out=0
5 A=1 B=0 Carry in=1 Sum=0 Carry out=1
6 A=1 B=1 Carry in=0 Sum=0 Carry out=1
7 A=1 B=1 Carry in=1 Sum=1 Carry out=1
mythreya@pes:~/Pictures$


File Edit Search Time Markers View Help
11:13 PM
From: 0 sec
To: 8 sec
Marker: -- | Cursor: 2 sec
SST
fulladder_tb
Signals
Time
A
B
Ci
Co
S
Waves
2 sec
4 sec
6 sec
8 sec
Type Signals
reg A
reg B
reg Ci
wire Co
wire S
Filter:
Append
Insert
Replace

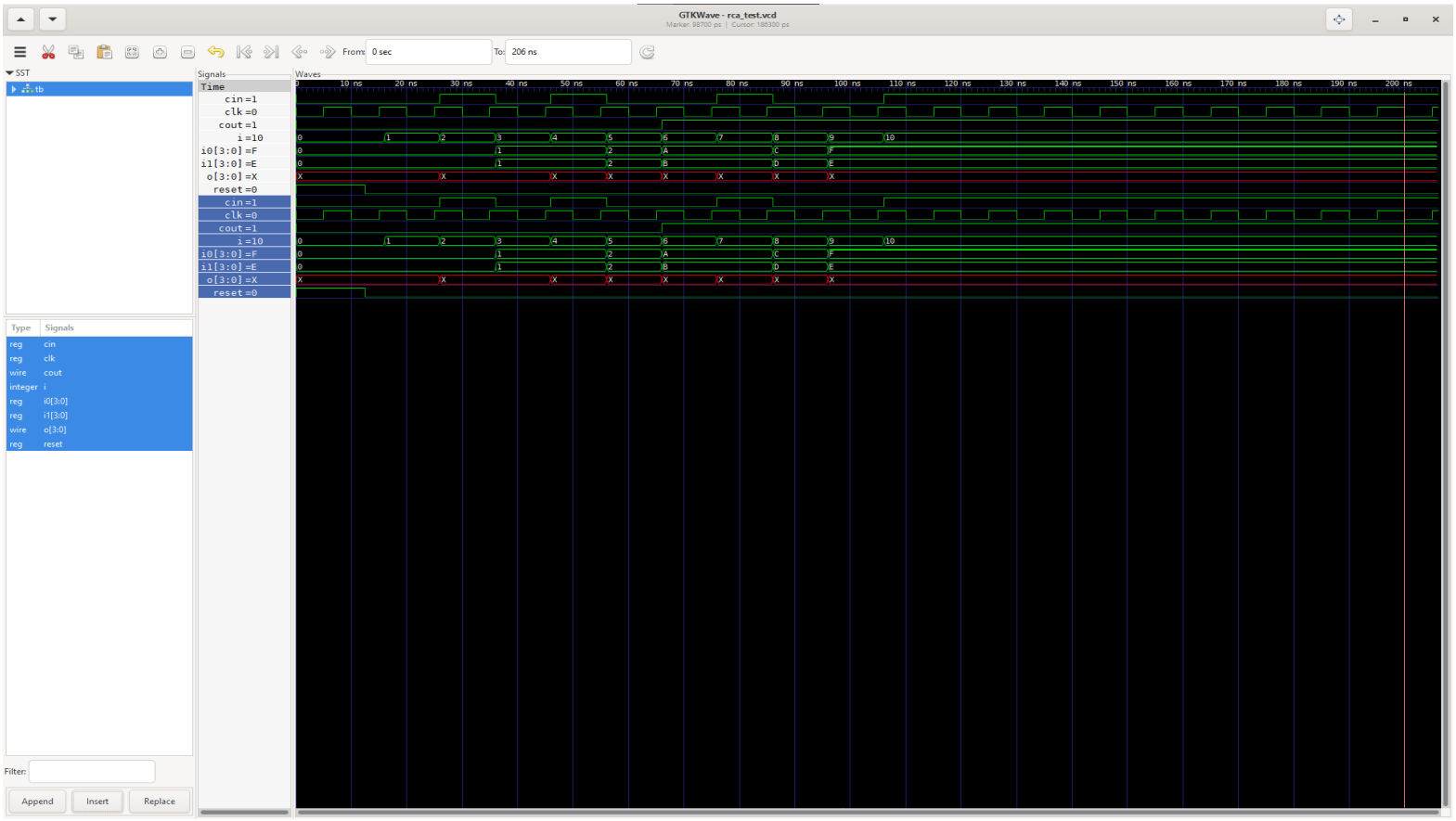
Ripple Carry Adder (rca)

```
module rca(input wire[3:0] a,b,input wire cin,output wire[3:0] sum,output wire cout);
output wire[2:0] c;
fulladder u0(a[0],b[0],cin,sum[0],c[0]);
fulladder u1(a[1],b[1],c[0],sum[1],c[1]);
fulladder u2(a[2],b[2],c[1],sum[2],c[2]);
fulladder u3(a[3],b[3],c[2],sum[3],cout);
endmodule
```

```
`timescale 1 ns / 100 ps
`define TESTVECS 10
module tb;
reg clk, reset;
reg [3:0] i0, i1;
reg cin;
wire [3:0] o;
wire cout;
reg [8:0] test_vecs [0:(`TESTVECS-1)];
integer i;
initial begin
$dumpfile("rca_test.vcd");
$dumpvars(0,tb);
end
initial begin
reset = 1'b1; #12.5 reset = 1'b0; end
initial clk = 1'b0; always #5 clk =~ clk;
initial begin
test_vecs[0] = 9'b000000000;
test_vecs[1] = 9'b000000001;
test_vecs[2] = 9'b000100010;
test_vecs[3] = 9'b000100011;
test_vecs[4] = 9'b001000100;
test_vecs[5] = 9'b101010110;
test_vecs[6] = 9'b101010111;
test_vecs[7] = 9'b110011010;
test_vecs[8] = 9'b111111100;
test_vecs[9] = 9'b111111101;
end
initial {i0, i1, cin, i} = 0;
rca u0 (i0, i1, cin, o, cout);
initial begin
#6 for(i=0;i<`TESTVECS;i=i+1)
    begin #10 {i0, i1, cin}=test_vecs[i]; end
#100 $finish;
end
always@(i0 or i1 or cin)
$monitor("At time = %t, i0=%b, i1=%b,cin=%b,Sum = %b,Carry %b", $time,i0,i1,cin,o,cout);
endmodule
```

Output

```
PS X:\sem3\sem3-lab\ddco_lab\week3\rippleCarryAdder> vvp rca
VCD info: dumpfile rca_test.vcd opened for output.
At time =                    0, i0=0000, i1=0000,cin=0,Sum = 00x0,Carry 0
At time =                  260, i0=0000, i1=0000,cin=1,Sum = 00xx,Carry 0
At time =                  360, i0=0001, i1=0001,cin=0,Sum = 00xx,Carry 0
At time =                  460, i0=0001, i1=0001,cin=1,Sum = 00x1,Carry 0
At time =                  560, i0=0010, i1=0010,cin=0,Sum = 01x0,Carry 0
At time =                  660, i0=1010, i1=1011,cin=0,Sum = 01x1,Carry 1
At time =                  760, i0=1010, i1=1011,cin=1,Sum = 01xx,Carry 1
At time =                  860, i0=1100, i1=1101,cin=0,Sum = 10xx,Carry 1
At time =                  960, i0=1111, i1=1110,cin=0,Sum = 11xx,Carry 1
At time =                 1060, i0=1111, i1=1110,cin=1,Sum = 11xx,Carry 1
rca_tb.v:60: $finish called at 2060 (100ps)
```



Disclaimer:

· The programs and output submitted is duly written, verified and executed by me.

· I have not copied from any of my peers nor from the external resource such as internet.

· If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name:

SRN:

Section:

Date: