

## DDCO LAB SEM3

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Section : C

Week 6: Program Counter

Source File: pc.v

```
module fa (input wire i0, i1, cin, output wire sum, cout);
    wire t0, t1, t2;
    xor3 _i0 (i0,i1,cin,sum);
    and2 _i1 (i0,i1,t0);
    and2 _i2 (i1,cin,t1);
    and2 _i3 (i0,cin,t2);
    or3 _i4 (t0,t1,t2,cout);
endmodule

module addsub (input wire addsub, i0, i1, cin, output wire sumdiff, cout);
    wire t;
    fa _i0 (i0,t,cin,sumdiff,cout);
    xor2 _i1 (i1,addsub,t);
endmodule

module pc_slice (input wire clk, reset, cin, load, inc, sub, offset,output wire cout, pc);
    wire in, inc_;
    invert invert_0 (inc,inc_);
    and2 and2_0 (inc_,offset,t);
    addsub addsub_0 (t,sub,pc,cin,in,cout);
    dfrl dfrl_0 (clk,reset,load,in,pc);
endmodule

module pc_slice0 (input wire clk, reset, cin, load, inc, sub, offset, output wire cout, pc);
    wire in;
    or2 or2_0 (inc,offset,t);
    addsub addsub_0 (sub,pc,t,cin,in,cout);
    dfrl dfrl_0 (clk,reset,load,in,pc);
endmodule

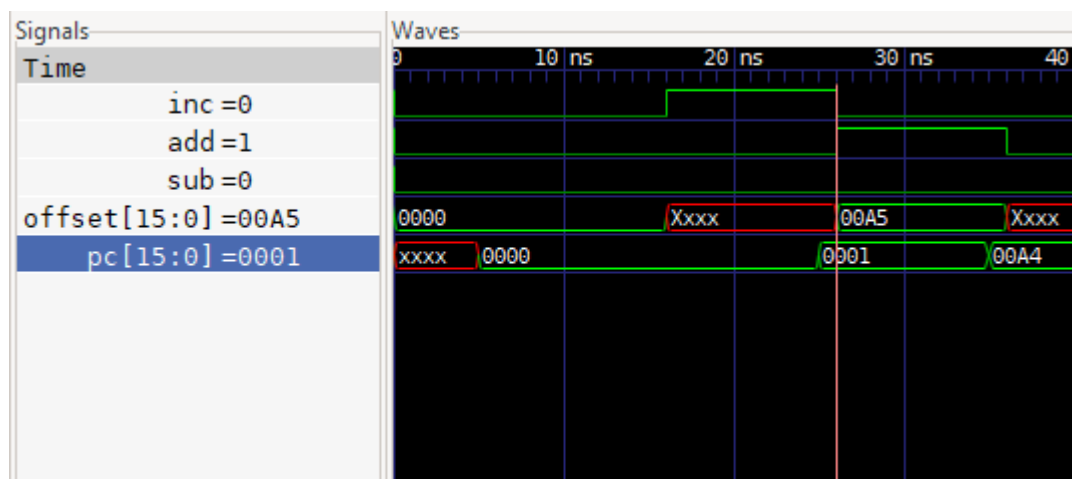
module pc (input wire clk, reset, inc, add, sub, input wire [15:0] offset, output wire [15:0] pc);
    input wire load;
    input wire [15:0] c;
    or3 or3_0 (add,sub,inc,load);
    pc_slice0 pc_slice_0 (clk, reset, sub, load, inc, sub, offset[0], c[0], pc[0]);
    pc_slice pc_slice_1 (clk, reset, sub, load, inc, sub, offset[1], c[1], pc[1]);
    pc_slice pc_slice_2 (clk, reset, sub, load, inc, sub, offset[2], c[2], pc[2]);
    pc_slice pc_slice_3 (clk, reset, sub, load, inc, sub, offset[3], c[3], pc[3]);
    pc_slice pc_slice_4 (clk, reset, sub, load, inc, sub, offset[4], c[4], pc[4]);
    pc_slice pc_slice_5 (clk, reset, sub, load, inc, sub, offset[5], c[5], pc[5]);
    pc_slice pc_slice_6 (clk, reset, sub, load, inc, sub, offset[6], c[6], pc[6]);
    pc_slice pc_slice_7 (clk, reset, sub, load, inc, sub, offset[7], c[7], pc[7]);
    pc_slice pc_slice_8 (clk, reset, sub, load, inc, sub, offset[8], c[8], pc[8]);
    pc_slice pc_slice_9 (clk, reset, sub, load, inc, sub, offset[9], c[9], pc[9]);
    pc_slice pc_slice_10 (clk, reset, sub, load, inc, sub, offset[10], c[10], pc[10]);
    pc_slice pc_slice_11 (clk, reset, sub, load, inc, sub, offset[11], c[11], pc[11]);
    pc_slice pc_slice_12 (clk, reset, sub, load, inc, sub, offset[12], c[12], pc[12]);
    pc_slice pc_slice_13 (clk, reset, sub, load, inc, sub, offset[13], c[13], pc[13]);
    pc_slice pc_slice_14 (clk, reset, sub, load, inc, sub, offset[14], c[14], pc[14]);
    pc_slice pc_slice_15 (clk, reset, sub, load, inc, sub, offset[15], c[15], pc[15]);
endmodule
```

## Truth Table for all cases:

	inc	add	sub	offset [15:0]	output
	Bit 18	Bit 17	Bit 16	Bit 15 to Bit0	pc[15:0]
<b>CASE 1</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>XXXX</b>	<b>0001</b>
<b>CASE 2</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>00A5</b>	<b>00A6</b>
<b>CASE 3</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>XXXX</b>	<b>00A6</b>
<b>CASE 4</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>XXXX</b>	<b>00A7</b>
<b>CASE 5</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0014</b>	<b>00B3</b>

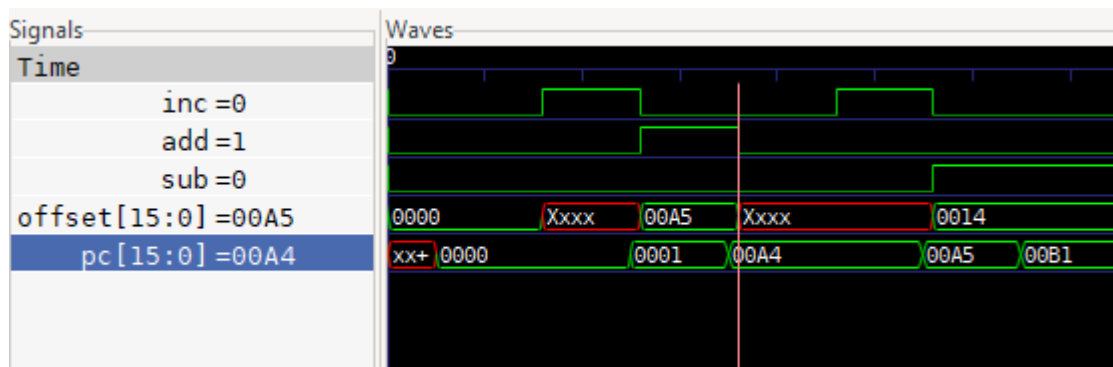
## Case 1: PC Increment operation with no offset

	inc	add	sub	offset [15:0]	output
	Bit 18	Bit 17	Bit 16	Bit 15 to Bit0	pc[15:0]
<b>CASE 1</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>XXXX</b>	<b>0001</b>



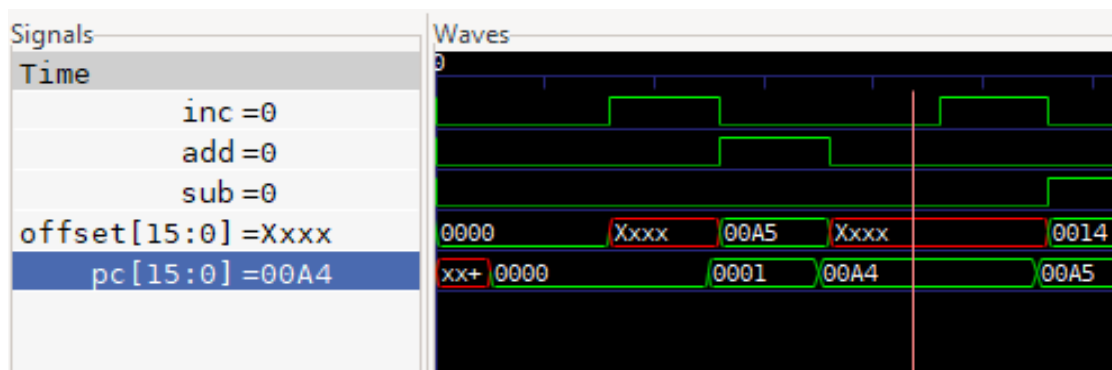
## Case 2: Add offset to PC

	inc	add	sub	offset [15:0]	output
	Bit 18	Bit 17	Bit 16	Bit 15 to Bit0	pc[15:0]
<b>CASE 2</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>00A5</b>	<b>00A6</b>



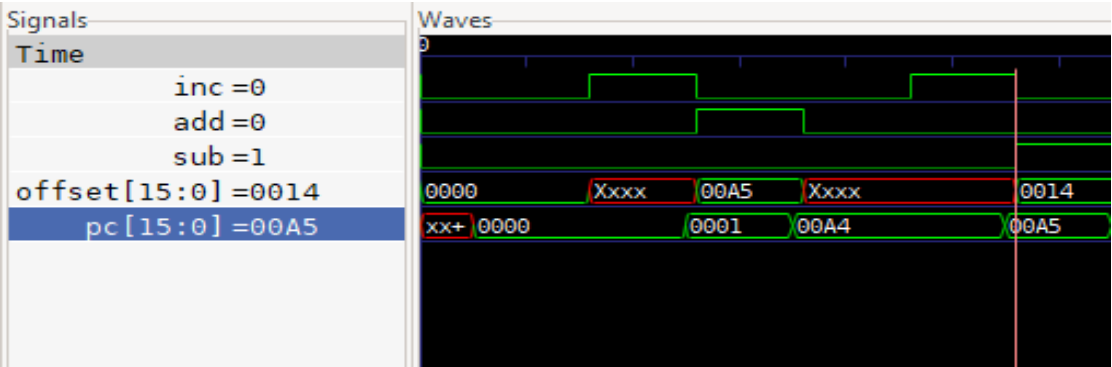
### Case 3: No change in PC

	inc	add	sub	offset [15:0]	output
	Bit 18	Bit 17	Bit 16	Bit 15 to Bit0	pc[15:0]
CASE 3	0	0	0	XXXX	00A6



Case 4: Auto Increment current value of PC

	inc	add	sub	offset [15:0]	output
	Bit 18	Bit 17	Bit 16	Bit 15 to Bit0	pc[15:0]
CASE 4	1	0	0	XXXX	00A7



Case 5: Subtract offset contents from PC

	inc	add	sub	offset [15:0]	output
	Bit 18	Bit 17	Bit 16	Bit 15 to Bit0	pc[15:0]
CASE 5	0	0	1	0014	00B3



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- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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