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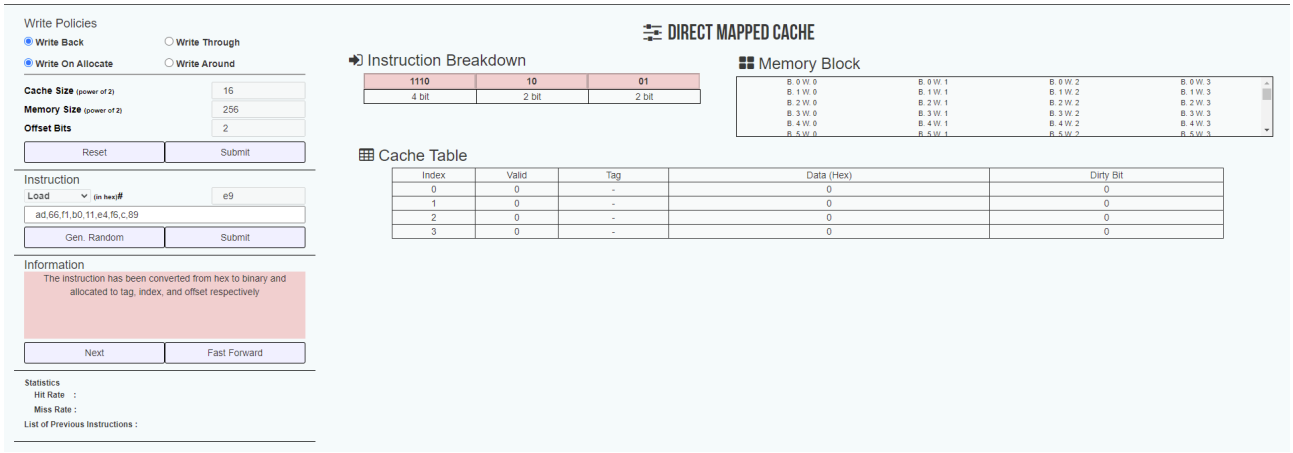
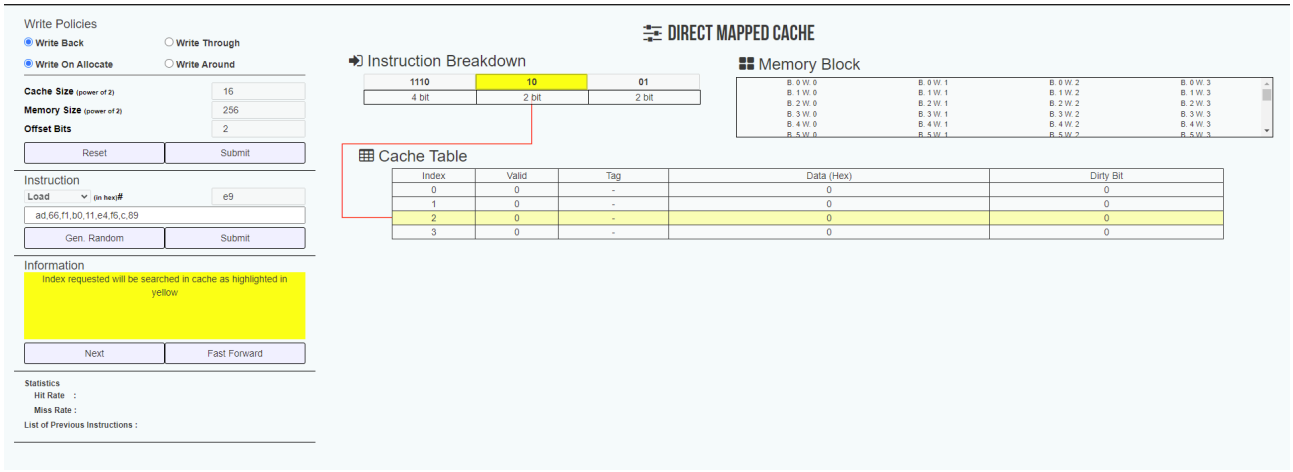
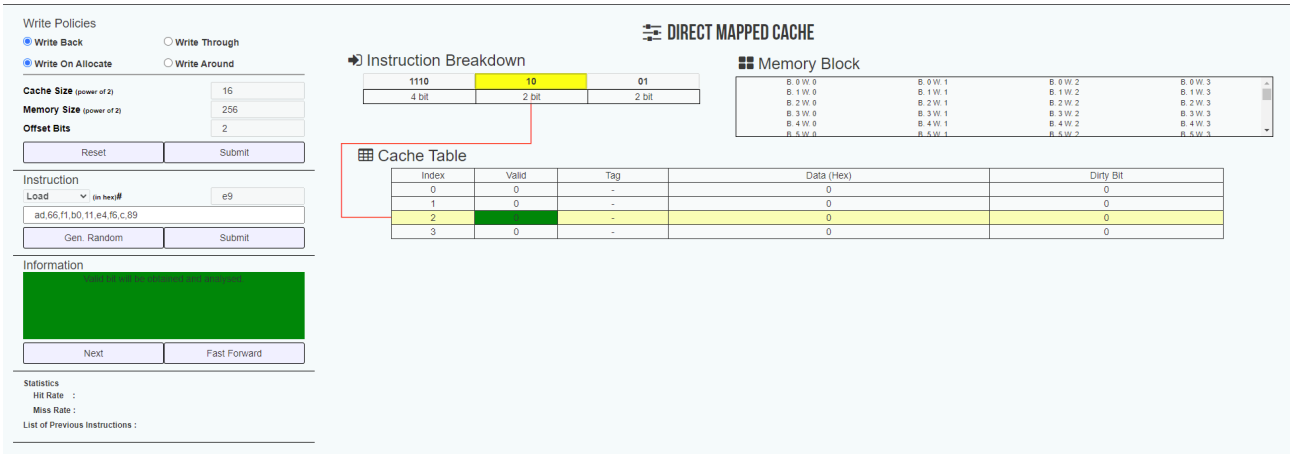
PES2UG20CS130

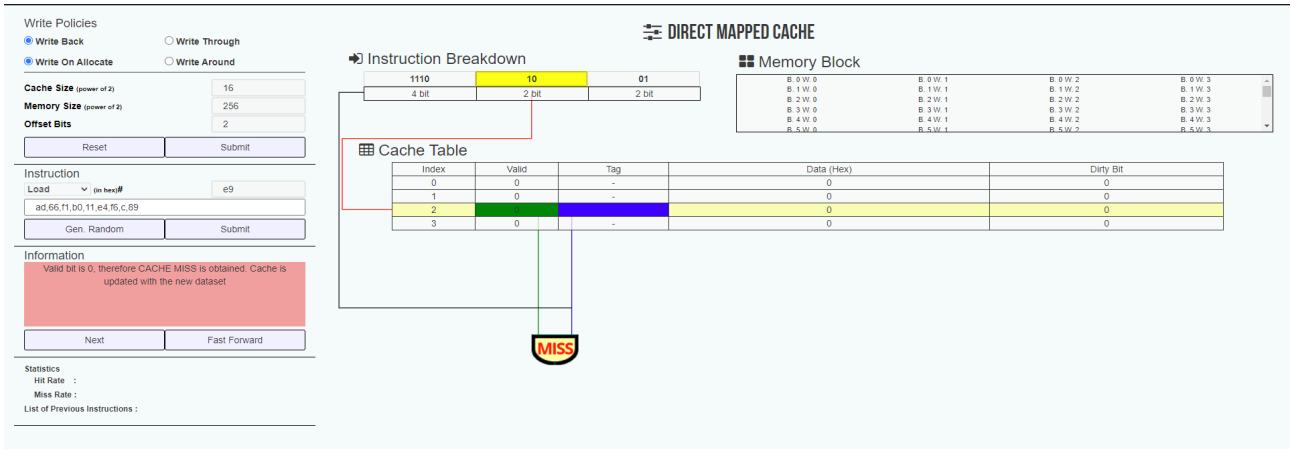
MPCA-Lab Week-8

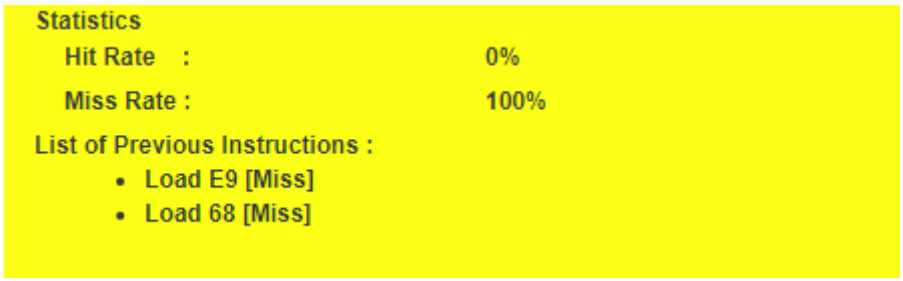
Task 1: Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset.The processor generates requests as follows 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11. Find hit rate and miss rate.

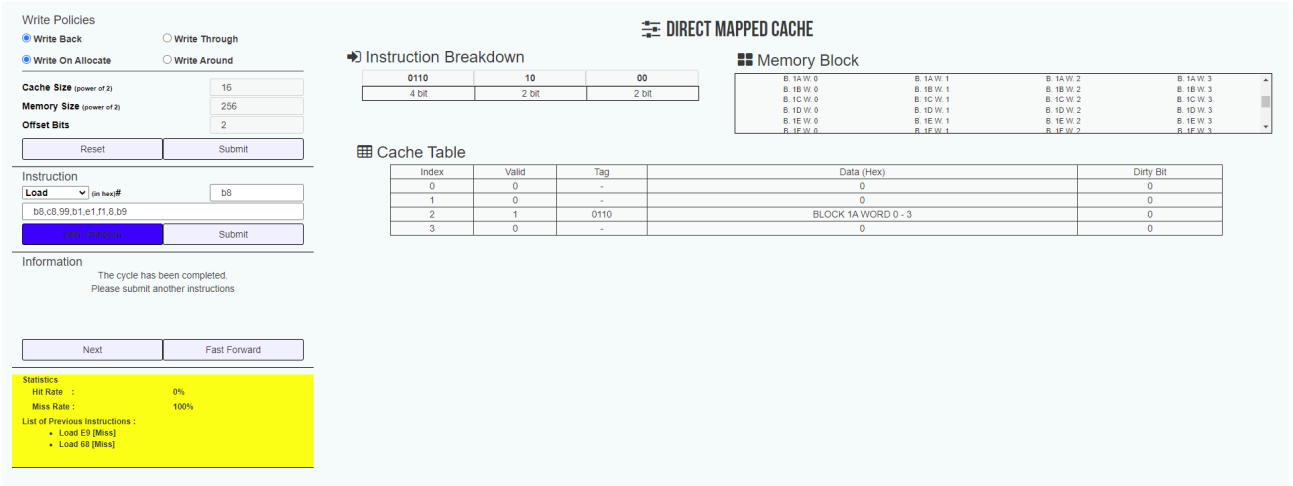




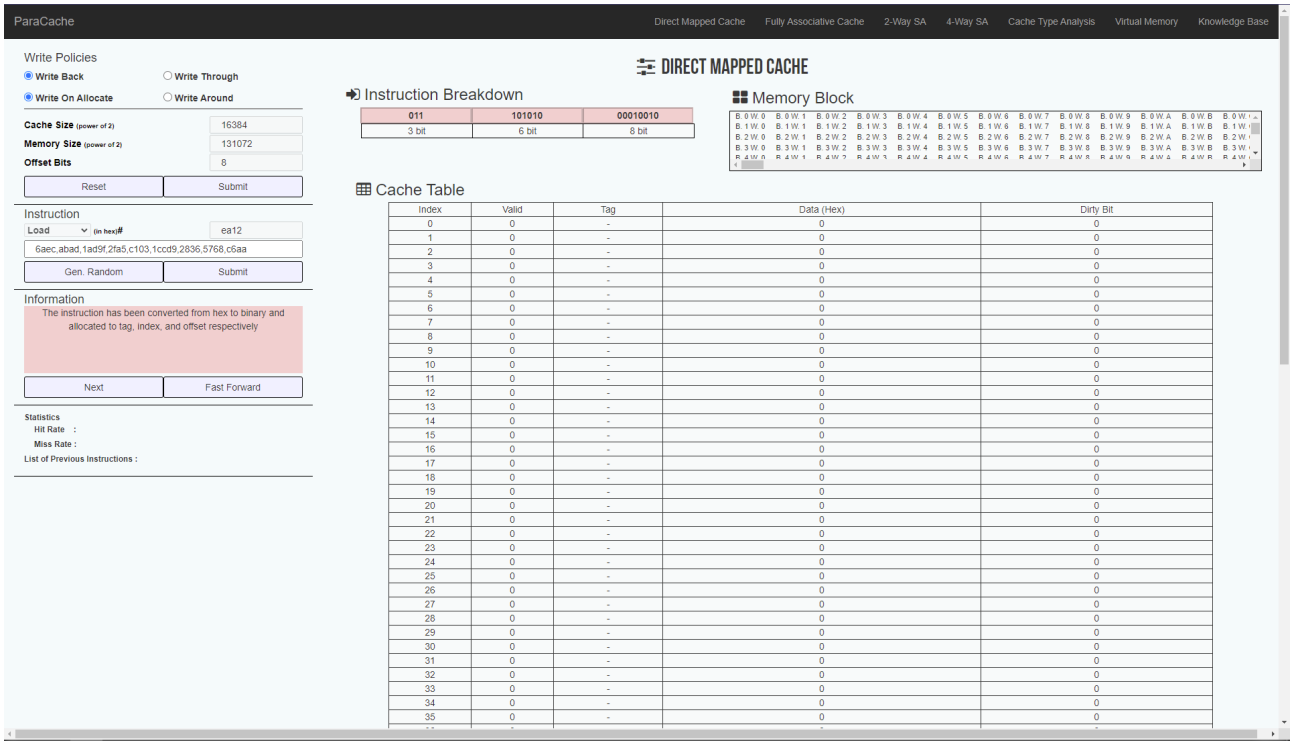


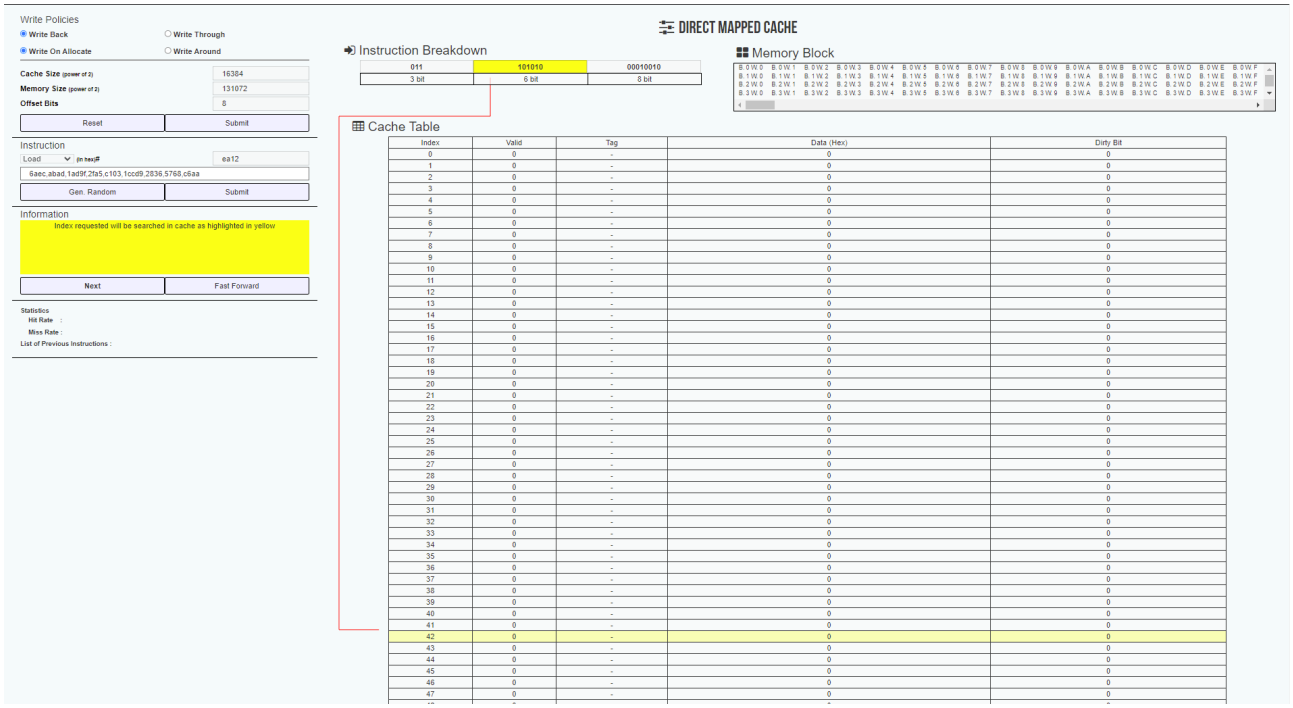

Write Policies
Write Back
Write Through
Write On Allocate
Write Around
Cache Size (power of 2) 16
Memory Size (power of 2) 256
Offset Bits 2
Reset
Submit
Instruction
Load (in hex)# e9
ad,66,f1,b0,11,e4,f6,c,89
Gen. Random
Submit
Information
Valid bit is 0, therefore CACHE MISS is obtained. Cache is updated with the new dataset
Next
Fast Forward
Statistics
Hit Rate :
Miss Rate :
List of Previous Instructions :
DIRECT MAPPED CACHE
Instruction Breakdown
1110 10 01
4 bit 2 bit 2 bit
Memory Block
Cache Table
Index Valid Tag Data (Hex) Dirty Bit
0 0 - 0 0
1 0 - 0 0
2 0 0 0
3 0 - 0 0
MISS

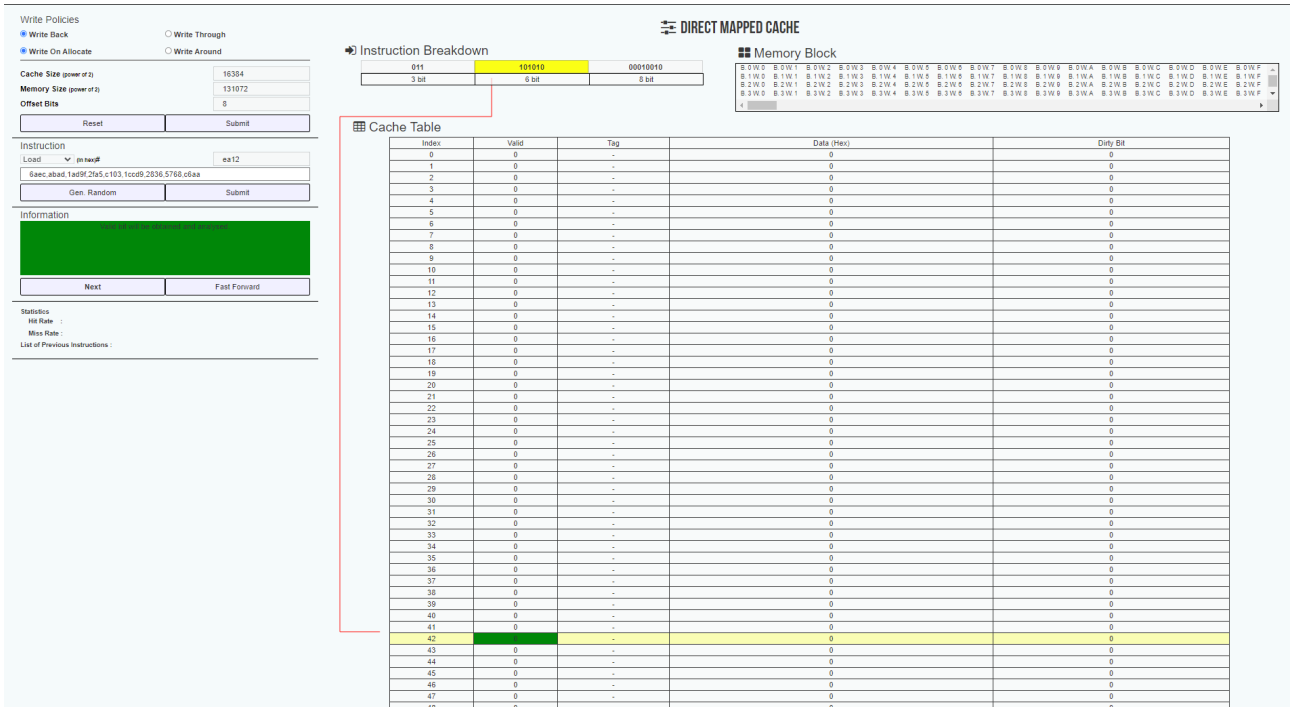

Statistics
Hit Rate : 0%
Miss Rate : 100%
List of Previous Instructions :
Load E9 [Miss]
Load 68 [Miss]

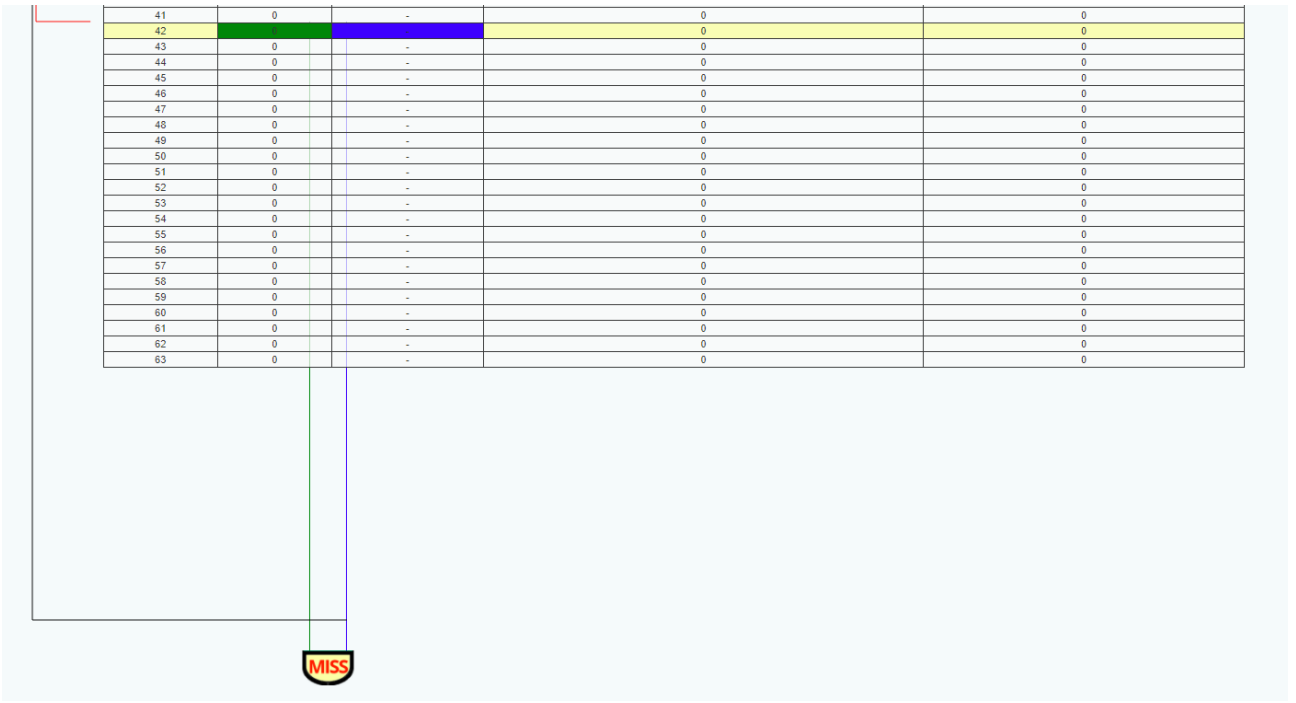

Write Policies
Write Back
Write Through
Write On Allocate
Write Around
Cache Size (power of 2) 16
Memory Size (power of 2) 256
Offset Bits 2
Reset
Submit
Instruction
Load (in hex)# b8
b8,c8,99,b1,e1,f1,8,b9
Gen. Random
Submit
Information
The cycle has been completed.
Please submit another instructions
Next
Fast Forward
Statistics
Hit Rate : 0%
Miss Rate : 100%
List of Previous Instructions :
Load E9 [Miss]
Load 68 [Miss]
DIRECT MAPPED CACHE
Instruction Breakdown
0110 10 00
4 bit 2 bit 2 bit
Memory Block
Cache Table
Index Valid Tag Data (Hex) Dirty Bit
0 0 - 0 0
1 0 - 0 0
2 1 0110 BLOCK 1A WORD 0 - 3 0
3 0 - 0 0

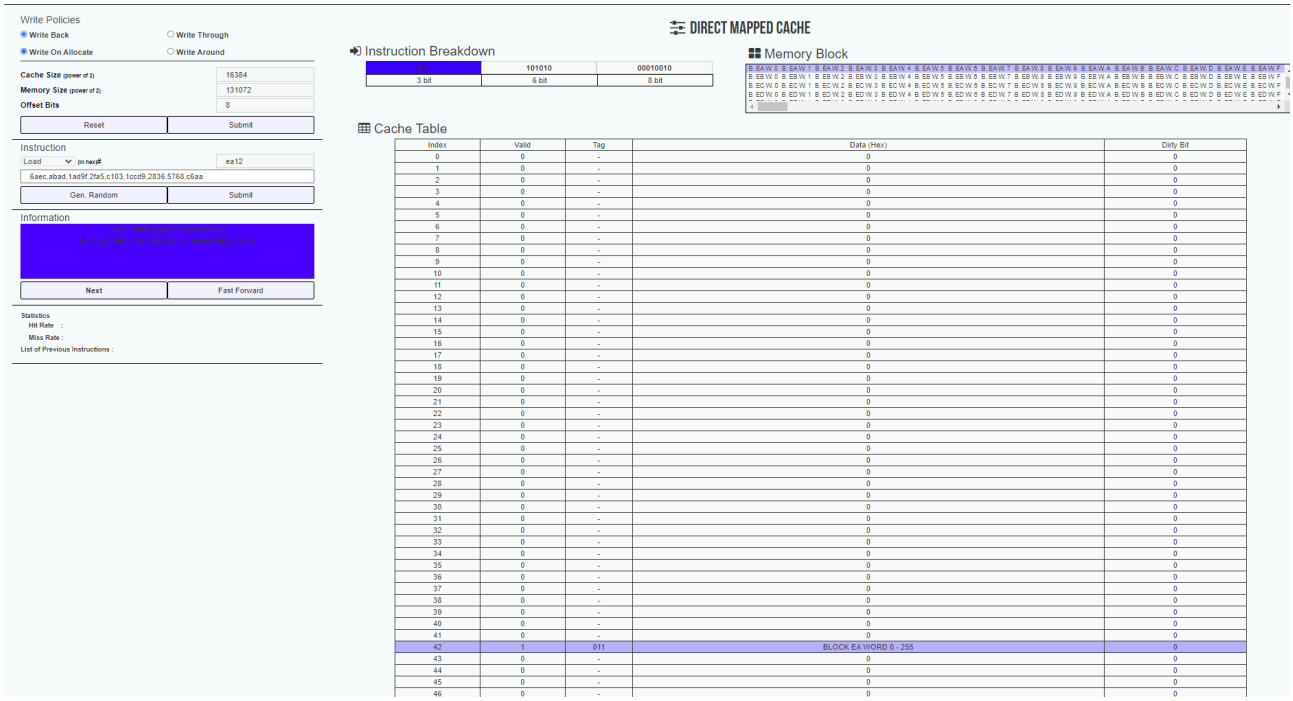
Task 2: Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate

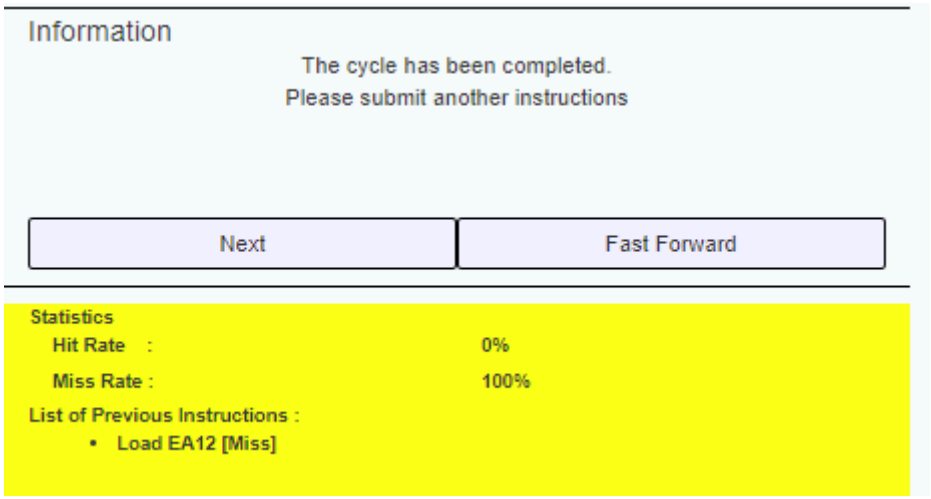





Write Policies
Write Back
Write Through
Write On Allocate
Write Around
Cache Size (power of 2)
16384
Memory Size (power of 2)
131072
Offset Bits
8
Reset
Submit
Instruction
Load
ea12
6aec,abad,1ad9f,2fa5,c103,1ccd9,2836,5768,c6aa
Gen. Random
Submit
Information
Next
Fast Forward
Statistics
Hit Rate :
Miss Rate :
List of Previous Instructions :
DIRECT MAPPED CACHE
Instruction Breakdown
011
101010
00010010
3 bit
6 bit
8 bit
Memory Block
Cache Table
Index
Valid
Tag
Data (Hex)
Dirty Bit


MISS

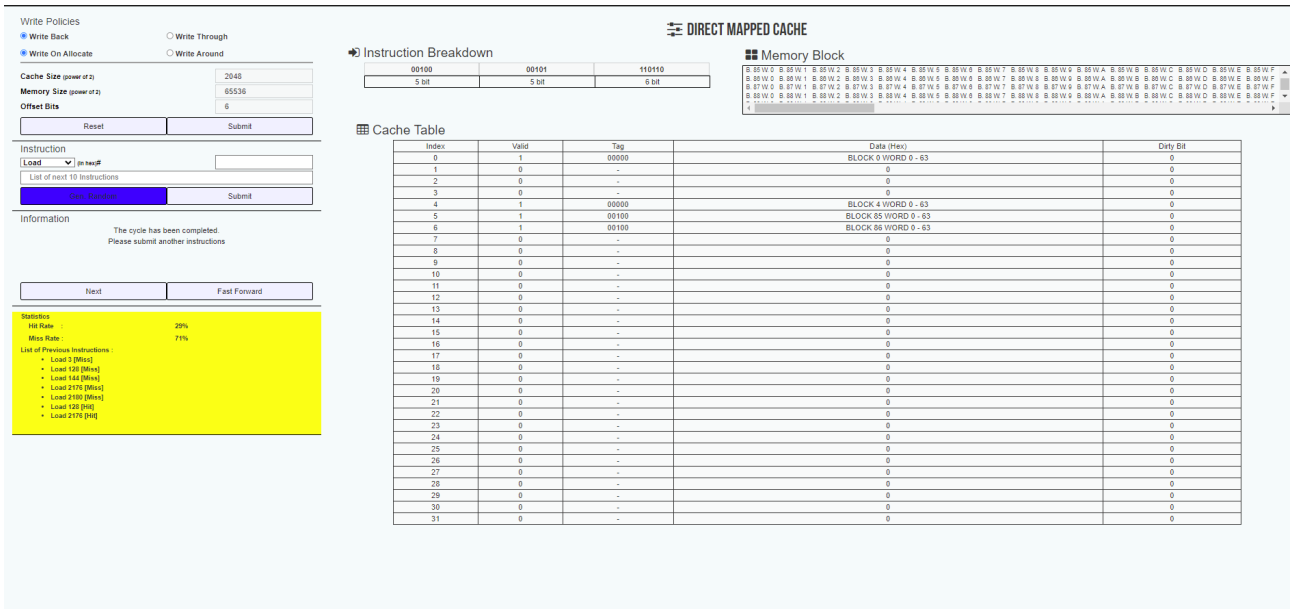

Write Policies
Write Back
Write Through
Write On Allocate
Write Around
Cache Size (power of 2)
16384
Memory Size (power of 2)
131072
Offset Bits
8
Reset
Submit
Instruction
Load
(in hex)#
ea12
6aec,abad,1ad9f,2fa5,c103,1ccd9,2836,5768,c6aa
Gen. Random
Submit
Information
The cycle has been completed.
Please submit another instructions
Next
Fast Forward
Statistics
Hit Rate :
Miss Rate :
List of Previous Instructions :
DIRECT MAPPED CACHE
Instruction Breakdown
011
101010
00010010
3 bit
6 bit
8 bit
Memory Block
Cache Table
Index
Valid
Tag
Data (Hex)
Dirty Bit
42
1
011
BLOCK EA WORD 0 - 255


Information
The cycle has been completed.
Please submit another instructions
Next
Fast Forward
Statistics
Hit Rate :
0%
Miss Rate :
100%
List of Previous Instructions :
Load EA12 [Miss]

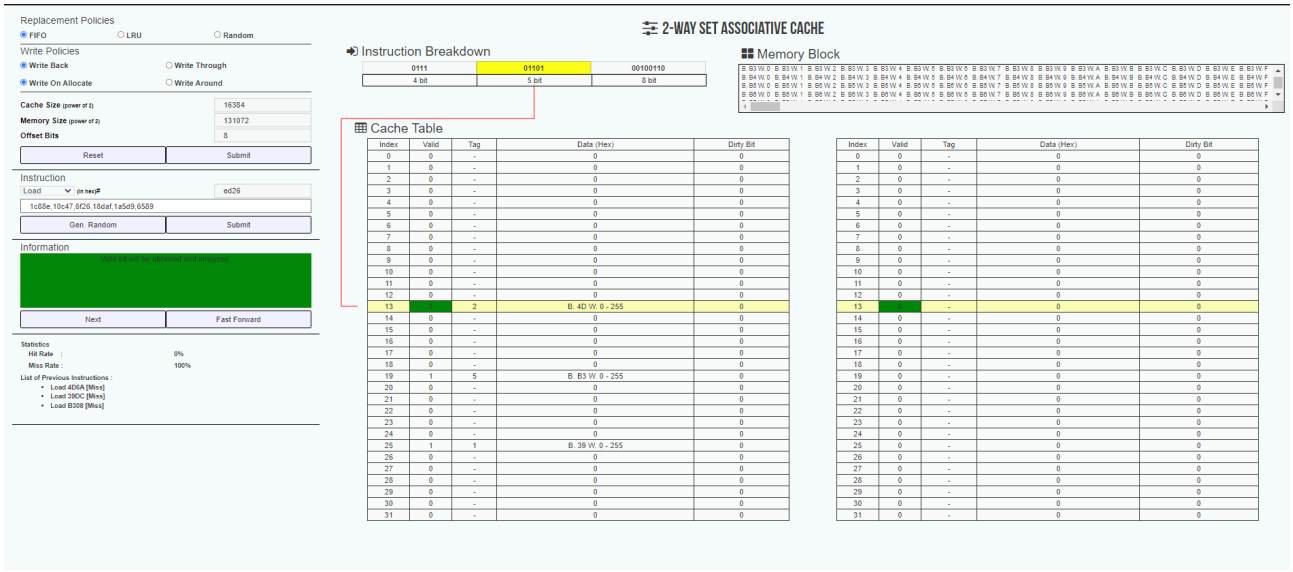
Task 3: A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

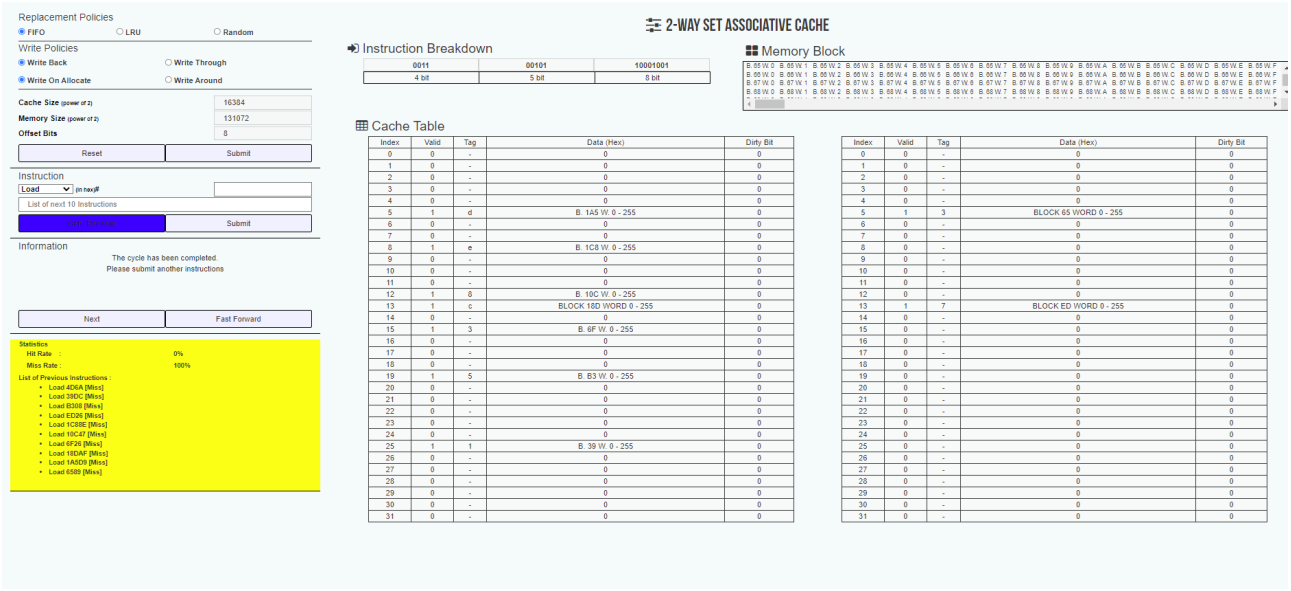
a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. 5,5,6 bits respectively

b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176 All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.



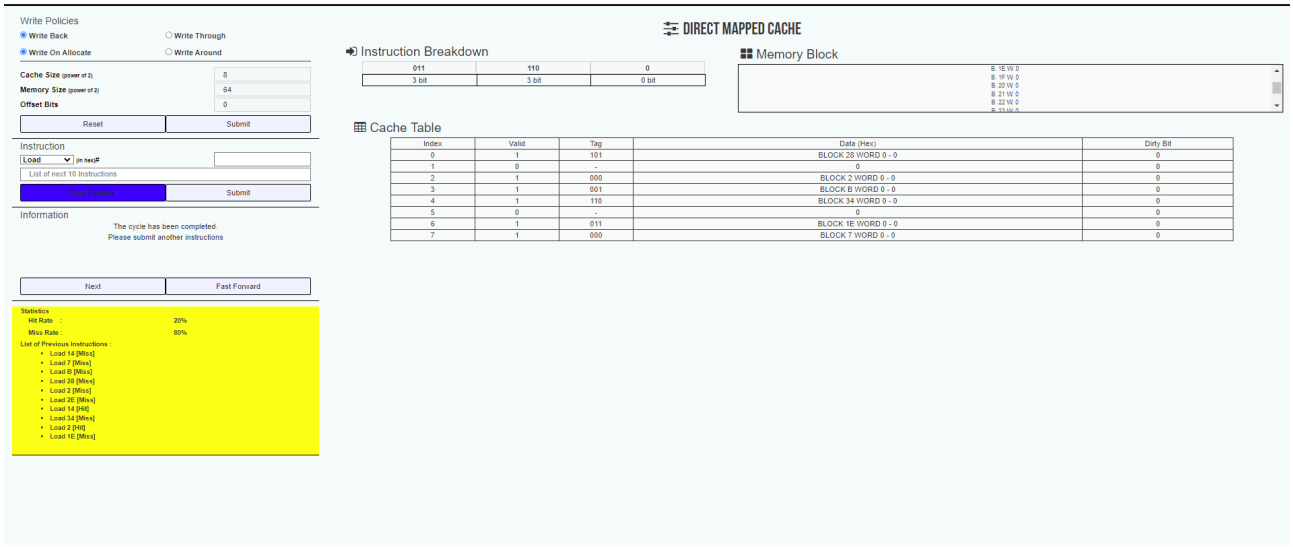
Task 4: Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.



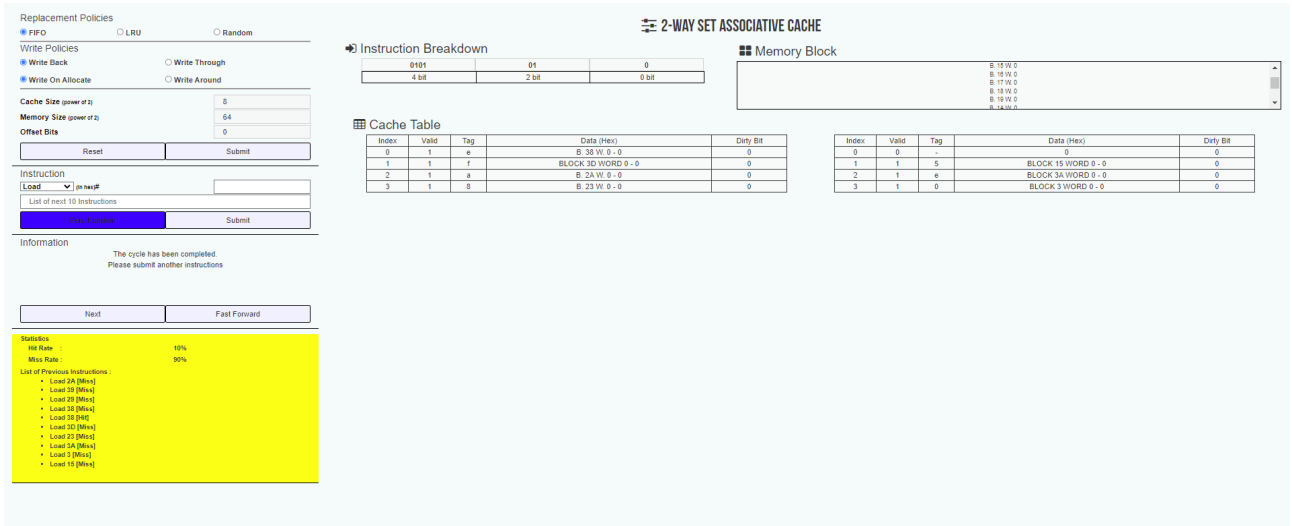


Task 5: Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used. The cache is mapped as:

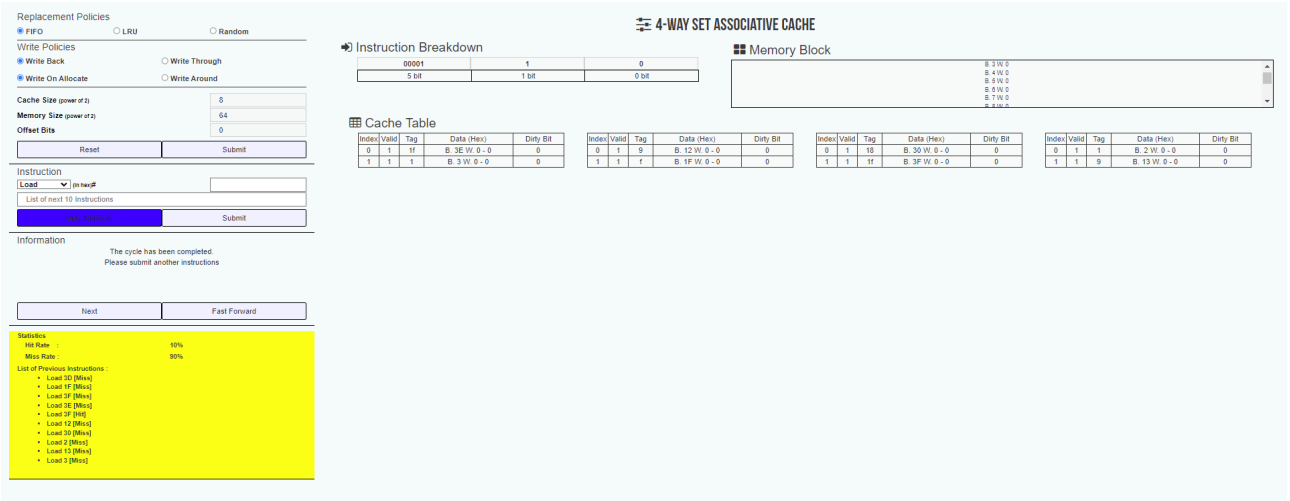
a) Direct mapped cache



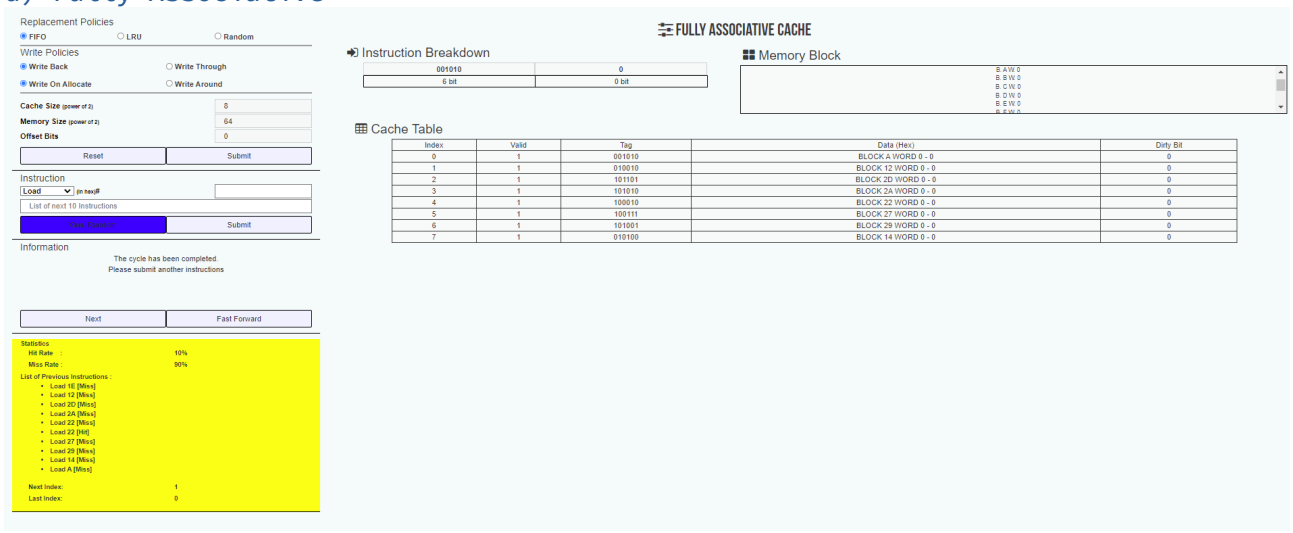
b) 2-Way Set Associative



c) 4-Way Set Associative



d) Fully Associative



Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	001010	BLOCK A WORD 0 - 0	0
1	1	010010	BLOCK 12 WORD 0 - 0	0
2	1	101101	BLOCK 2D WORD 0 - 0	0
3	1	101010	BLOCK 2A WORD 0 - 0	0
4	1	100010	BLOCK 22 WORD 0 - 0	0
5	1	100111	BLOCK 27 WORD 0 - 0	0
6	1	101001	BLOCK 29 WORD 0 - 0	0
7	1	010100	BLOCK 14 WORD 0 - 0	0