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MPCA-Lab Week-8

Task 1: Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset. The processor generates requests as follows 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11. Find hit rate and miss rate.

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

16

Memory Size (power of 2)

256

Offset Bits

2

Reset

Submit

Instruction

Load (in hex)

ad,66,f1,b0,11,e4,f5,c,89

Gen. Random

Submit

Information

The instruction has been converted from hex to binary and allocated to tag, index, and offset respectively

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :
List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

1110	10	01
4 bit	2 bit	2 bit

Memory Block

B:0 W:0	B:0 W:1	B:0 W:2	B:0 W:3
B:1 W:0	B:1 W:1	B:1 W:2	B:1 W:3
B:2 W:0	B:2 W:1	B:2 W:2	B:2 W:3
B:3 W:0	B:3 W:1	B:3 W:2	B:3 W:3
B:4 W:0	B:4 W:1	B:4 W:2	B:4 W:3
B:5 W:0	B:5 W:1	B:5 W:2	B:5 W:3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

16

Memory Size (power of 2)

256

Offset Bits

2

Reset

Submit

Instruction

Load (in hex)

ad,66,f1,b0,11,e4,f5,c,89

Gen. Random

Submit

Information

Index requested will be searched in cache as highlighted in yellow

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :
List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

1110	10	01
4 bit	2 bit	2 bit

Memory Block

B:0 W:0	B:0 W:1	B:0 W:2	B:0 W:3
B:1 W:0	B:1 W:1	B:1 W:2	B:1 W:3
B:2 W:0	B:2 W:1	B:2 W:2	B:2 W:3
B:3 W:0	B:3 W:1	B:3 W:2	B:3 W:3
B:4 W:0	B:4 W:1	B:4 W:2	B:4 W:3
B:5 W:0	B:5 W:1	B:5 W:2	B:5 W:3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

16

Memory Size (power of 2)

256

Offset Bits

2

Reset

Submit

Instruction

Load (in hex)

ad,66,f1,b0,11,e4,f5,c,89

Gen. Random

Submit

Information

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :
List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

1110	10	01
4 bit	2 bit	2 bit

Memory Block

B:0 W:0	B:0 W:1	B:0 W:2	B:0 W:3
B:1 W:0	B:1 W:1	B:1 W:2	B:1 W:3
B:2 W:0	B:2 W:1	B:2 W:2	B:2 W:3
B:3 W:0	B:3 W:1	B:3 W:2	B:3 W:3
B:4 W:0	B:4 W:1	B:4 W:2	B:4 W:3
B:5 W:0	B:5 W:1	B:5 W:2	B:5 W:3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Write Policies

Write Back

Write On Allocate

Write Through

Write Around

Cache Size (power of 2)

16

Memory Size (power of 2)

256

Offset Bits

2

Reset

Submit

Instruction

Load

(in hex)

e9

ad,66,f1,b0,11,e4,75,c,89

Gen. Random

Submit

Information

Valid bit is 0, therefore CACHE MISS is obtained. Cache is updated with the new dataset

Next

Fast Forward

Statistics

Hit Rate :

Miss Rate :

List of Previous Instructions :

Instruction Breakdown

1110

10

01

4 bit

2 bit

2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

MISS

Memory Block

B: 0 W: 0	B: 0 W: 1	B: 0 W: 2	B: 0 W: 3
B: 1 W: 0	B: 1 W: 1	B: 1 W: 2	B: 1 W: 3
B: 2 W: 0	B: 2 W: 1	B: 2 W: 2	B: 2 W: 3
B: 3 W: 0	B: 3 W: 1	B: 3 W: 2	B: 3 W: 3
B: 4 W: 0	B: 4 W: 1	B: 4 W: 2	B: 4 W: 3
B: 5 W: 0	B: 5 W: 1	B: 5 W: 2	B: 5 W: 3

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load E9 [Miss]
- Load 68 [Miss]

Write Policies

Write Back

Write On Allocate

Write Through

Write Around

Cache Size (power of 2)

16

Memory Size (power of 2)

256

Offset Bits

2

Reset

Submit

Instruction

Load

(in hex)

b8

b8,c8,99,b1,e1,f1,8,b,9

Gen. Random

Submit

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load E9 [Miss]
- Load 68 [Miss]

Instruction Breakdown

0110

10

00

4 bit

2 bit

2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	0110	BLOCK 1A WORD 0 - 3	0
3	0	-	0	0

Memory Block

B: 1A W: 0	B: 1A W: 1	B: 1A W: 2	B: 1A W: 3
B: 1B W: 0	B: 1B W: 1	B: 1B W: 2	B: 1B W: 3
B: 1C W: 0	B: 1C W: 1	B: 1C W: 2	B: 1C W: 3
B: 1D W: 0	B: 1D W: 1	B: 1D W: 2	B: 1D W: 3
B: 1E W: 0	B: 1E W: 1	B: 1E W: 2	B: 1E W: 3
B: 1F W: 0	B: 1F W: 1	B: 1F W: 2	B: 1F W: 3

Task 2: Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate

Write Policies

☒ Write Back
 ☐ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

Load

Information
 The instruction has been converted from hex to binary and allocated to tag, index, and offset respectively

Statistics
 Hit Rate :
 Miss Rate :
 List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

011	101010	00010010
3 bit	6 bit	8 bit

Memory Block

B 0W 0	B 0W 1	B 0W 2	B 0W 3	B 0W 4	B 0W 5	B 0W 6	B 0W 7	B 0W 8	B 0W 9	B 0W A	B 0W B	B 0W C	B 0W D	B 0W E	B 0W F
B 1W 0	B 1W 1	B 1W 2	B 1W 3	B 1W 4	B 1W 5	B 1W 6	B 1W 7	B 1W 8	B 1W 9	B 1W A	B 1W B	B 1W C	B 1W D	B 1W E	B 1W F
B 2W 0	B 2W 1	B 2W 2	B 2W 3	B 2W 4	B 2W 5	B 2W 6	B 2W 7	B 2W 8	B 2W 9	B 2W A	B 2W B	B 2W C	B 2W D	B 2W E	B 2W F
B 3W 0	B 3W 1	B 3W 2	B 3W 3	B 3W 4	B 3W 5	B 3W 6	B 3W 7	B 3W 8	B 3W 9	B 3W A	B 3W B	B 3W C	B 3W D	B 3W E	B 3W F
B 4W 0	B 4W 1	B 4W 2	B 4W 3	B 4W 4	B 4W 5	B 4W 6	B 4W 7	B 4W 8	B 4W 9	B 4W A	B 4W B	B 4W C	B 4W D	B 4W E	B 4W F

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
--	-	-	-	-

Write Policies

☒ Write Back
 ☐ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

Load

Information
 Index requested will be searched in cache as highlighted in yellow

Statistics
 Hit Rate :
 Miss Rate :
 List of Previous Instructions :

DIRECT MAPPED CACHE

Instruction Breakdown

011	101010	00010010
3 bit	6 bit	8 bit

Memory Block

B 0W 0	B 0W 1	B 0W 2	B 0W 3	B 0W 4	B 0W 5	B 0W 6	B 0W 7	B 0W 8	B 0W 9	B 0W A	B 0W B	B 0W C	B 0W D	B 0W E	B 0W F
B 1W 0	B 1W 1	B 1W 2	B 1W 3	B 1W 4	B 1W 5	B 1W 6	B 1W 7	B 1W 8	B 1W 9	B 1W A	B 1W B	B 1W C	B 1W D	B 1W E	B 1W F
B 2W 0	B 2W 1	B 2W 2	B 2W 3	B 2W 4	B 2W 5	B 2W 6	B 2W 7	B 2W 8	B 2W 9	B 2W A	B 2W B	B 2W C	B 2W D	B 2W E	B 2W F
B 3W 0	B 3W 1	B 3W 2	B 3W 3	B 3W 4	B 3W 5	B 3W 6	B 3W 7	B 3W 8	B 3W 9	B 3W A	B 3W B	B 3W C	B 3W D	B 3W E	B 3W F
B 4W 0	B 4W 1	B 4W 2	B 4W 3	B 4W 4	B 4W 5	B 4W 6	B 4W 7	B 4W 8	B 4W 9	B 4W A	B 4W B	B 4W C	B 4W D	B 4W E	B 4W F

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
36	0	-	0	0
37	0	-	0	0
38	0	-	0	0
39	0	-	0	0
40	0	-	0	0
41	0	-	0	0
42	0	-	0	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
--	-	-	-	-

Write Policies

Write Back

Write On Allocate

Write Through

Write Around

Cache Size (power of 2)
16384

Memory Size (power of 2)
131072

Offset Bits
8

Reset

Submit

Instruction

Load

jeq

ea12

6a6c.ab6d.1a09f.2fa5.c103.1cc09.2b36.5768.c6aa

Gen. Random

Submit

Information

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :
List of Previous Instructions :

Instruction Breakdown

011
3 bit

101010
6 bit

00010010
8 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
36	0	-	0	0
37	0	-	0	0
38	0	-	0	0
39	0	-	0	0
40	0	-	0	0
41	0	-	0	0
42	0	-	0	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
48	0	-	0	0

Memory Block

B0W0 B0W1 B0W2 B0W3 B0W4 B0W5 B0W6 B0W7 B0W8 B0W9 B0WA B0WB B0WC B0WD B0WE B0WF

B1W0 B1W1 B1W2 B1W3 B1W4 B1W5 B1W6 B1W7 B1W8 B1W9 B1WA B1WB B1WC B1WD B1WE B1WF

B2W0 B2W1 B2W2 B2W3 B2W4 B2W5 B2W6 B2W7 B2W8 B2W9 B2WA B2WB B2WC B2WD B2WE B2WF

B3W0 B3W1 B3W2 B3W3 B3W4 B3W5 B3W6 B3W7 B3W8 B3W9 B3WA B3WB B3WC B3WD B3WE B3WF

41	0	-	0	0
42	0	-	0	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
48	0	-	0	0
49	0	-	0	0
50	0	-	0	0
51	0	-	0	0
52	0	-	0	0
53	0	-	0	0
54	0	-	0	0
55	0	-	0	0
56	0	-	0	0
57	0	-	0	0
58	0	-	0	0
59	0	-	0	0
60	0	-	0	0
61	0	-	0	0
62	0	-	0	0
63	0	-	0	0

MISS

Write Policies

Write Back

Write On Allocate

Write Through

Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

16384

131072

8

Reset

Submit

Instruction

Load

6aecabb41ad9f2fa5c1031ccdd928365768c8aa

ea12

Gen: Random

Submit

Information

Cache table is updated successfully.
Block EA word 0-255 is assigned to cache

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :
List of Previous Instructions :

Instruction Breakdown

00000000

101010

00010010

3 bit

8 bit

5 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-		0
1	0	-		0
2	0	-		0
3	0	-		0
4	0	-		0
5	0	-		0
6	0	-		0
7	0	-		0
8	0	-		0
9	0	-		0
10	0	-		0
11	0	-		0
12	0	-		0
13	0	-		0
14	0	-		0
15	0	-		0
16	0	-		0
17	0	-		0
18	0	-		0
19	0	-		0
20	0	-		0
21	0	-		0
22	0	-		0
23	0	-		0
24	0	-		0
25	0	-		0
26	0	-		0
27	0	-		0
28	0	-		0
29	0	-		0
30	0	-		0
31	0	-		0
32	0	-		0
33	0	-		0
34	0	-		0
35	0	-		0
36	0	-		0
37	0	-		0
38	0	-		0
39	0	-		0
40	0	-		0
41	0	-		0
42	1	011	BLOCK EA WORD 0 - 255	0
43	0	-		0
44	0	-		0
45	0	-		0
46	0	-		0

Memory Block

EAWORD 0

EAWORD 1

EAWORD 2

EAWORD 3

EAWORD 4

EAWORD 5

EAWORD 6

EAWORD 7

EAWORD 8

EAWORD 9

EAWORD 10

EAWORD 11

EAWORD 12

EAWORD 13

EAWORD 14

EAWORD 15

EAWORD 16

EAWORD 17

EAWORD 18

EAWORD 19

EAWORD 20

EAWORD 21

EAWORD 22

EAWORD 23

EAWORD 24

EAWORD 25

EAWORD 26

EAWORD 27

EAWORD 28

EAWORD 29

EAWORD 30

EAWORD 31

EAWORD 32

EAWORD 33

EAWORD 34

EAWORD 35

EAWORD 36

EAWORD 37

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EAWORD 105

EAWORD 106

EAWORD 107

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EAWORD 110

EAWORD 111

EAWORD 112

EAWORD 113

EAWORD 114

EAWORD 115

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EAWORD 151

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EAWORD 165

EAWORD 166

EAWORD 167

EAWORD 168

EAWORD 169

EAWORD 170

EAWORD 171

EAWORD 172

EAWORD 173

EAWORD 174

EAWORD 175

EAWORD 176

EAWORD 177

EAWORD 178

EAWORD 179

EAWORD 180

EAWORD 181

EAWORD 182

EAWORD 183

EAWORD 184

EAWORD 185

EAWORD 186

EAWORD 187

EAWORD 188

EAWORD 189

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EAWORD 191

EAWORD 192

EAWORD 193

EAWORD 194

EAWORD 195

EAWORD 196

EAWORD 197

EAWORD 198

EAWORD 199

EAWORD 200

EAWORD 201

EAWORD 202

EAWORD 203

EAWORD 204

EAWORD 205

EAWORD 206

EAWORD 207

EAWORD 208

EAWORD 209

EAWORD 210

EAWORD 211

EAWORD 212

EAWORD 213

EAWORD 214

EAWORD 215

EAWORD 216

EAWORD 217

EAWORD 218

EAWORD 219

EAWORD 220

EAWORD 221

EAWORD 222

EAWORD 223

EAWORD 224

EAWORD 225

EAWORD 226

EAWORD 227

EAWORD 228

EAWORD 229

EAWORD 230

EAWORD 231

EAWORD 232

EAWORD 233

EAWORD 234

EAWORD 235

EAWORD 236

EAWORD 237

EAWORD 238

EAWORD 239

EAWORD 240

EAWORD 241

EAWORD 242

EAWORD 243

EAWORD 244

EAWORD 245

EAWORD 246

EAWORD 247

EAWORD 248

EAWORD 249

EAWORD 250

EAWORD 251

EAWORD 252

EAWORD 253

EAWORD 254

EAWORD 255

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate :
Miss Rate :

0%
100%

List of Previous Instructions :

Load EA12 [Miss]

b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176. All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

Write Policies

☒ Write Back
 ☐ Write Through

☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2)

2048

Memory Size (power of 2)

65536

Offset Bits

6

Reset

Submit

Instruction

Load

List of next 10 instructions

Local Processor

Submit

Information

The cycle has been completed.

Please submit another instructions

Next

Fast Forward

Statistics

100 Rate

20%

Miss Rate

77%

List of Previous Instructions :

- Load 3 [Miss]
- Load 120 [Miss]
- Load 144 [Miss]
- Load 2176 [Miss]
- Load 2180 [Miss]
- Load 180 [Hit]
- Load 2176 [Hit]

Instruction Breakdown

00100	00101	110110
5 bit	5 bit	6 bit

Memory Block

B 0010 0	B 0010 1	B 0010 2	B 0010 3	B 0010 4	B 0010 5	B 0010 6	B 0010 7	B 0010 8	B 0010 9	B 0010 A	B 0010 B	B 0010 C	B 0010 D	B 0010 E	B 0010 F
B 0010 0	B 0010 1	B 0010 2	B 0010 3	B 0010 4	B 0010 5	B 0010 6	B 0010 7	B 0010 8	B 0010 9	B 0010 A	B 0010 B	B 0010 C	B 0010 D	B 0010 E	B 0010 F
B 0010 0	B 0010 1	B 0010 2	B 0010 3	B 0010 4	B 0010 5	B 0010 6	B 0010 7	B 0010 8	B 0010 9	B 0010 A	B 0010 B	B 0010 C	B 0010 D	B 0010 E	B 0010 F
B 0010 0	B 0010 1	B 0010 2	B 0010 3	B 0010 4	B 0010 5	B 0010 6	B 0010 7	B 0010 8	B 0010 9	B 0010 A	B 0010 B	B 0010 C	B 0010 D	B 0010 E	B 0010 F

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00000	BLOCK 0 WORD 0 - 63	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	1	00000	BLOCK 4 WORD 0 - 63	0
5	1	00100	BLOCK 5 WORD 0 - 63	0
6	1	00100	BLOCK 66 WORD 0 - 63	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Task 4: Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

Replacement Policies
☒ FIFO ☐ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)
16384

Memory Size (power of 2)
131072

Offset Bits
8

Reset Submit

Instruction
Load ed26
1c8b6 10c47 826 18ca1 1a5d9 6589
Gen. Random Submit

Information
Next Fast Forward

Statistics
Hit Rate : 0%
Miss Rate : 100%
List of Previous Instructions :

- Load 4D0A [Miss]
- Load 380C [Miss]
- Load B308 [Miss]

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown
0111 01101 00100110
4 bit 5 bit 8 bit

Memory Block
B 85W 0 B 85W 1 B 85W 2 B 85W 3 B 85W 4 B 85W 5 B 85W 6 B 85W 7 B 85W 8 B 85W 9 B 85W A B 85W B B 85W C B 85W D B 85W E B 85W F
B 87W 0 B 87W 1 B 87W 2 B 87W 3 B 87W 4 B 87W 5 B 87W 6 B 87W 7 B 87W 8 B 87W 9 B 87W A B 87W B B 87W C B 87W D B 87W E B 87W F
B 89W 0 B 89W 1 B 89W 2 B 89W 3 B 89W 4 B 89W 5 B 89W 6 B 89W 7 B 89W 8 B 89W 9 B 89W A B 89W B B 89W C B 89W D B 89W E B 89W F

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	2	B 4D W 0 - 255	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	1	5	B B3 W 0 - 255	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	1	8	B 38 W 0 - 255	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Index Valid Tag Data (Hex) Dirty Bit
0 0 - 0 0
1 0 - 0 0
2 0 - 0 0
3 0 - 0 0
4 0 - 0 0
5 0 - 0 0
6 0 - 0 0
7 0 - 0 0
8 0 - 0 0
9 0 - 0 0
10 0 - 0 0
11 0 - 0 0
12 0 - 0 0
13 0 - 0 0
14 0 - 0 0
15 0 - 0 0
16 0 - 0 0
17 0 - 0 0
18 0 - 0 0
19 0 - 0 0
20 0 - 0 0
21 0 - 0 0
22 0 - 0 0
23 0 - 0 0
24 0 - 0 0
25 0 - 0 0
26 0 - 0 0
27 0 - 0 0
28 0 - 0 0
29 0 - 0 0
30 0 - 0 0
31 0 - 0 0

Replacement Policies
☒ FIFO ☐ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)
16384

Memory Size (power of 2)
131072

Offset Bits
8

Reset Submit

Instruction
Load
List of next 10 instructions
Next Instruction Submit

Information
The cycle has been completed.
Please submit another instructions
Next Fast Forward

Statistics
Hit Rate : 0%
Miss Rate : 100%
List of Previous Instructions :

- Load 4D0A [Miss]
- Load 380C [Miss]
- Load B308 [Miss]
- Load EC08 [Miss]
- Load 1C08 [Miss]
- Load 16C4F [Miss]
- Load 8F08 [Miss]
- Load 1A5D9 [Miss]
- Load 1A5D9 [Miss]
- Load 1A5D9 [Miss]

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown
0011 00101 10001001
4 bit 5 bit 8 bit

Memory Block
B 85W 0 B 85W 1 B 85W 2 B 85W 3 B 85W 4 B 85W 5 B 85W 6 B 85W 7 B 85W 8 B 85W 9 B 85W A B 85W B B 85W C B 85W D B 85W E B 85W F
B 87W 0 B 87W 1 B 87W 2 B 87W 3 B 87W 4 B 87W 5 B 87W 6 B 87W 7 B 87W 8 B 87W 9 B 87W A B 87W B B 87W C B 87W D B 87W E B 87W F
B 89W 0 B 89W 1 B 89W 2 B 89W 3 B 89W 4 B 89W 5 B 89W 6 B 89W 7 B 89W 8 B 89W 9 B 89W A B 89W B B 89W C B 89W D B 89W E B 89W F

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	1	d	B 1A5 W 0 - 255	0
6	0	-	0	0
7	0	-	0	0
8	1	e	B 1C8 W 0 - 255	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	1	8	B 18C W 0 - 255	0
13	1	c	BLOCK 18D WORD 0 - 255	0
14	0	-	0	0
15	1	3	B 8F W 0 - 255	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	1	5	B B3 W 0 - 255	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	1	1	B 39 W 0 - 255	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Index Valid Tag Data (Hex) Dirty Bit
0 0 - 0 0
1 0 - 0 0
2 0 - 0 0
3 0 - 0 0
4 0 - 0 0
5 1 3 BLOCK 65 WORD 0 - 255
6 0 - 0 0
7 0 - 0 0
8 0 - 0 0
9 0 - 0 0
10 0 - 0 0
11 0 - 0 0
12 0 - 0 0
13 1 7 BLOCK ED WORD 0 - 255
14 0 - 0 0
15 0 - 0 0
16 0 - 0 0
17 0 - 0 0
18 0 - 0 0
19 0 - 0 0
20 0 - 0 0
21 0 - 0 0
22 0 - 0 0
23 0 - 0 0
24 0 - 0 0
25 0 - 0 0
26 0 - 0 0
27 0 - 0 0
28 0 - 0 0
29 0 - 0 0
30 0 - 0 0
31 0 - 0 0

Task 5: Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used. The cache is mapped as:

a) Direct mapped cache

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

Load

List of next 10 Instructions

Information

The cycle has been completed
Please submit another instructions

Statistics

Hit Rate : 20%

Miss Rate : 80%

List of Previous Instructions :

- Load 14 (Miss)
- Load 7 (Miss)
- Load 8 (Miss)
- Load 28 (Miss)
- Load 2 (Miss)
- Load 25 (Miss)
- Load 14 (Hit)
- Load 14 (Miss)
- Load 3 (Miss)
- Load 15 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

011	110	0
3 bit	3 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	101	BLOCK 28 WORD 0 - 0	0
1	0	-	0	0
2	1	000	BLOCK 2 WORD 0 - 0	0
3	1	001	BLOCK 8 WORD 0 - 0	0
4	1	110	BLOCK 34 WORD 0 - 0	0
5	0	-	0	0
6	1	011	BLOCK 16 WORD 0 - 0	0
7	1	000	BLOCK 7 WORD 0 - 0	0

Memory Block

B 1E W 0
B 1F W 0
B 20 W 0
B 21 W 0
B 22 W 0
B 23 W 0

b) 2-Way Set Associative

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

Load

List of next 10 Instructions

Information

The cycle has been completed
Please submit another instructions

Statistics

Hit Rate : 50%

Miss Rate : 50%

List of Previous Instructions :

- Load 24 (Miss)
- Load 19 (Miss)
- Load 28 (Miss)
- Load 38 (Miss)
- Load 28 (Hit)
- Load 30 (Miss)
- Load 23 (Miss)
- Load 24 (Miss)
- Load 3 (Miss)
- Load 19 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0101	01	0
4 bit	2 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	e	B 38 W 0 - 0	0
1	1	f	BLOCK 3D WORD 0 - 0	0
2	1	a	B 2A W 0 - 0	0
3	1	8	B 23 W 0 - 0	0

Memory Block

B 10 W 0
B 15 W 0
B 16 W 0
B 17 W 0
B 18 W 0
B 19 W 0
B 20 W 0

c) 4-Way Set Associative

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

Load

List of next 10 Instructions

Information

The cycle has been completed
Please submit another instructions

Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load 30 (Miss)
- Load 1F (Miss)
- Load 2F (Miss)
- Load 1E (Miss)
- Load 3F (Hit)
- Load 12 (Miss)
- Load 30 (Miss)
- Load 2 (Miss)
- Load 13 (Miss)
- Load 2 (Miss)

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00001	1	0
5 bit	1 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	ff	B 3E W 0 - 0	0
1	1	1	B 3 W 0 - 0	0

Memory Block

B 3 W 0
B 4 W 0
B 5 W 0
B 6 W 0
B 7 W 0
B 8 W 0

d) Fully Associative

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

8

Memory Size (power of 2)

64

Offset Bits

0

Reset

Submit

Instruction

Load

001010

Submit

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 90%

Miss Rate : 10%

List of Previous Instructions :

- Load 16 (Miss)
- Load 12 (Miss)
- Load 20 (Miss)
- Load 24 (Miss)
- Load 22 (Miss)
- Load 28 (Hit)
- Load 27 (Miss)
- Load 29 (Miss)
- Load 14 (Miss)
- Load A (Miss)

Next Index: 1

Last Index: 0

FULLY ASSOCIATIVE CACHE

Instruction Breakdown

001010

0

6 bit

0 bit

Memory Block

B A W 0

B B W 0

B C W 0

B D W 0

B E W 0

B F W 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	001010	BLOCK A WORD 0 - 0	0
1	1	010010	BLOCK 12 WORD 0 - 0	0
2	1	101101	BLOCK 20 WORD 0 - 0	0
3	1	101010	BLOCK 24 WORD 0 - 0	0
4	1	100010	BLOCK 22 WORD 0 - 0	0
5	1	100111	BLOCK 27 WORD 0 - 0	0
6	1	101001	BLOCK 29 WORD 0 - 0	0
7	1	010100	BLOCK 14 WORD 0 - 0	0