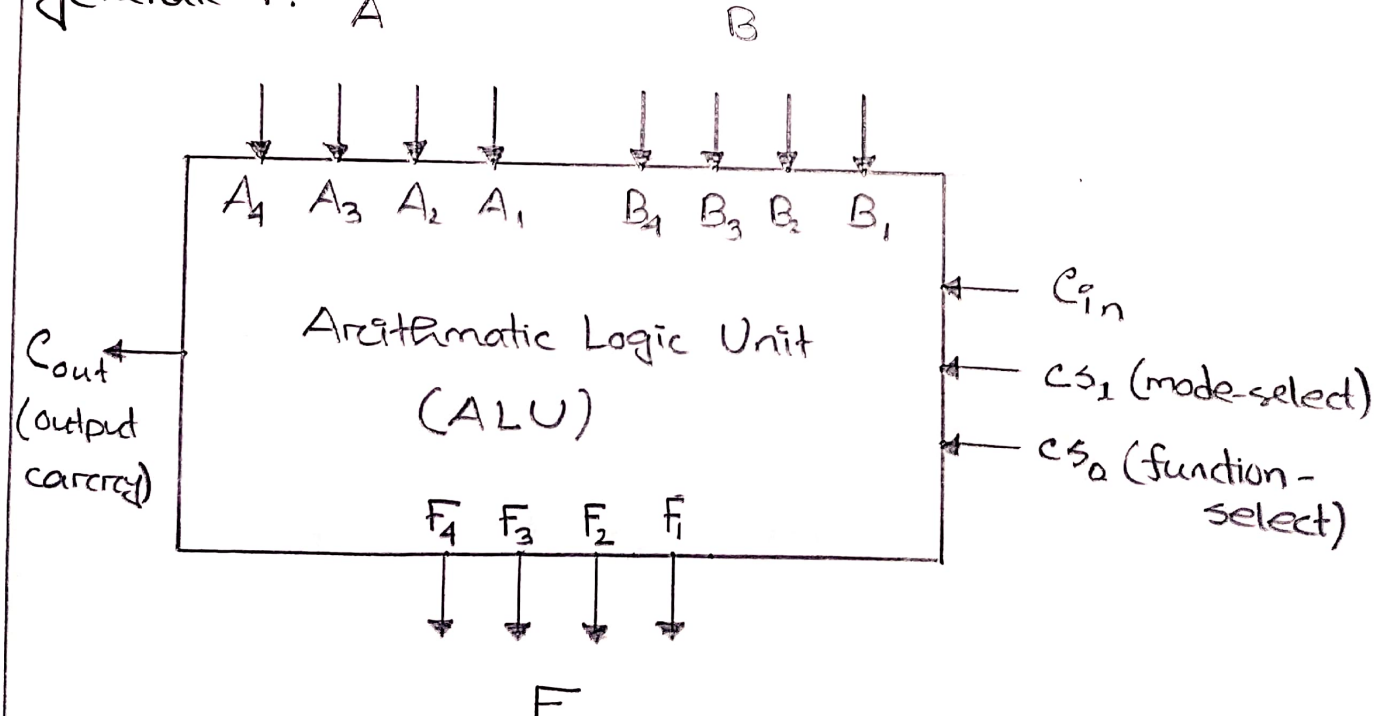
Introduction

An arithmatic-logic unit is the part of a central processing unit that carries out arithmatic and logic operations on the operands in a computer. It is basically a multi-operation, combinational logic digital function, that carries out the mentioned operations. The arithmatic-logic unit (ALU) has a number of selection lines to select a particular operation in the unit. The selection lines are controlled by selection variables and k selection variables can perform up to 2^k operations.

In our experiment, we have three selection variables (cs) that would enable us to perform $2^3 = 8$ operations. The four data inputs from A are combined with that of B to operate on and generate output at F. A combinational circuit is used to modify the data inputs of A and B to produce for the inputs for the parallel adders to generate F.



The selection variable cs_2 (we will name it s_2 from here) is used as the input carry, cs_1 (or s_1) is used for mode select and cs_0 (or s_0) is being used for function select in our ALU design.

A 4-bit status register is also being used to denote four different states, and they are C (carry), S (sign), V (overflow) and Z (zero). They change during arithmatic operations.

CF: C is set to 1 when output carry of the ALU is 1, else it is 0.

SF: S is set to 1 when the highest order bit of the output of the ALU is 1, else it is 0.

OF: V is set to 1 if the XOR of carries C_4 and C_5 (Fig. 2) is 1, else it is 0.

ZF: Z is set to 1 if the output of the ALU contains all 0's, else it is 1.

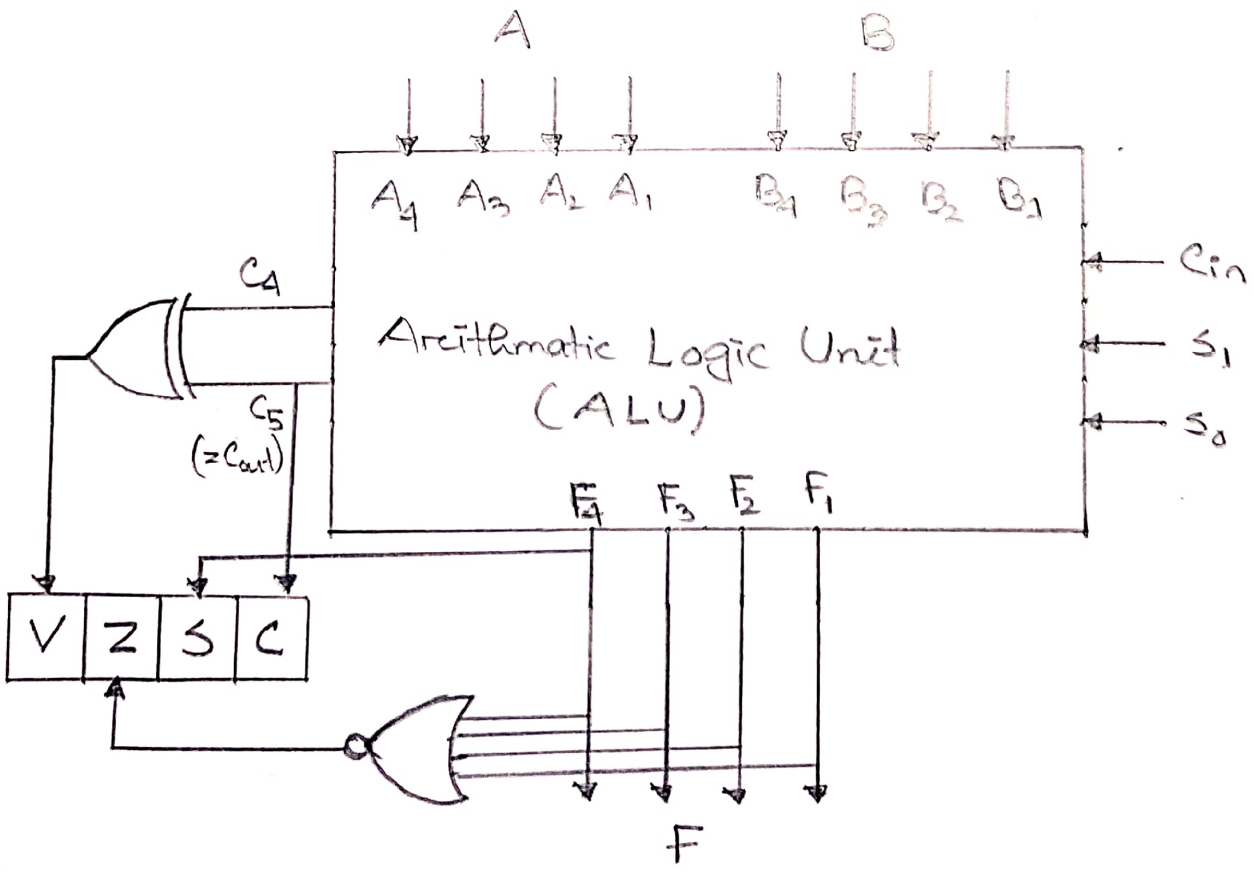


Fig. 2: A block diagram of an ALU with status registers

Problem Specification:

Design a 4-bit ALU with three selection bits cs_0, cs_1, cs_2 (or S_0, S_1, S_2) for performing the following operations

C_{in}			Function	Output
S_2	S_1	S_0		
0	0	0	Decrement A	F = A − 1
0	0	1	Subtract with borrow	F = A − B − 1
X	1	0	OR	F = A ∨ B
1	0	0	Transfer A	F = A
1	0	1	Subtract	F = A − B
X	1	1	AND	F = A ∧ B

Truth Table:

S_2	S_1	S_0	X_i	Y_i	Z_i	C_{in}	Output (F)
0	0	0	A_i	1	C_i	0	A-1
0	0	1	A_i	B_i'	C_i	0	A-B-1
1	0	0	A_i	1	C_i	1	A
1	0	1	A_i	B_i'	C_i	1	A-B
X	1	0	A_i+B_i	1	1	1	$A \vee B$
X	1	1	A_i+B_i'	B_i'	0	0	$A \wedge B$

Equations:

$$X_i = A_i + S_1 (B_i \oplus S_0)$$

$$Y_i = (S_0 \cdot B_i)'$$

$$Z_i = S_1' C_i + S_1 S_0'$$

$$C_{in} = S_1' S_2 + S_1 S_0'$$

Required ICs:

Name	Count
7400	
7408	
7432	
7483	
7486	

Simulator : Logisim