UNIVERSITI TEKNOLOGI MALAYSIA

RESEARCH UNIVERSITY

# MIDTERM TEST SEMESTER 2

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|---|---|---|
| **COURSE CODE** | **:** | **SECR1013** |
| **COURSE TITLE** | **:** | **DIGITAL LOGIC** |
| **TOTAL TIME** | **:** | **2 HOURs** |
| **DATE** | **:** | |
| **VENUE** | **:** | |

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**(GENERAL INSTRUCTION):**

**Write ALL your answers in the answer booklet. Show all your workings.**

**This test will contribute 20% towards the total marks of 100.**

**Warning!**

**Students who are caught cheating during the examination will be reported to the disciplinary board for possible suspension of the student for one or two semesters.**

| | |
|---|---|
| **Name** | |
| **Metric No** | |
| **Year / Course** | |
| **Section (Circle)** | |
| **Lecturer (Circle)** | |

**This question booklet consists of 7 pages excluding the front page.**

**QUESTION 1 [17 MARKS]**

a. State **TRUE or FALSE** for the following statements. **[4M]**

i. Analog systems can process, store, and transmit data more efficiently but can only assign discrete values (discontinuous) to each point.

ii. The process of converting an analog signal to a digital signal using an involves sampling, quantization, and digital conversion, and can result in errors and loss of information during sampling and quantization.

iii. The duty cycle of a signal refers to the proportion of time during which the signal is active or low, compared to the total period of the signal.

iv. A multiplexer (MUX) is a device that takes multiple input signals and routes them to multiple output signals simultaneously, while a demultiplexer (DEMUX) combines multiple input signals into a single output signal.

v. The unit nano (n) is represented by $10^9$.

b. Identify the correct **term** for the following descriptions **(i) to (iv)** from the answer options below. **[4M]**

| Descriptions | Term |
|---|---|
| An integrated circuit that is designed to perform a specific function and cannot be reprogrammed or altered after manufacturing. | (i) |
| A type of package for integrated circuits, with two parallel rows of pins. | (ii) |
| A method for producing electronic circuits where the components are mounted directly onto the surface of printed circuit boards (PCBs). | (iii) |
| An integrated circuit that can be reprogrammed or configured by the user after manufacturing to perform different functions. | (iv) |
| Which PLD is categorized at SPLD? | (v) |

Answer options:

| | | | |
|---|---|---|---|
| TTL | PAL | Wellon Programmer | SMT |
| Fine Grain | WinCUPL | CPLD | Coarse Grain |

c. Details are given as follows: **frequency(*f*)=10MHz** and **duty cycle=25%**. Draw duty cycle diagram to show on and off state and label the diagram clearly with pulse width ($t_w$) and period (T) in microsecond (μs). Show all your workings. **[7M]**

**QUESTION 2 [24 MARKS]**

a. Convert the base-5 number **$2431.23_5$** to its **decimal** equivalent. Show all your workings. **[4M]**

b. Convert the decimal number **$47.234_{10}$** to **octal**. Answer in **3 radix points**. Show all your workings. **[4M]**

c. Convert the binary number **$101110.11011_2$** to its **hexadecimal** equivalent. Show all your workings. **[4M]**

d. Convert the Gray code **$101101_{gray}$** to binary number. Show all your workings. **[4M]**

e. Perform the arithmetic operation using **8-bit 2's complement** system. Show all your workings, including the numbers in 2's complement form, the addition process, and the result. Finally, check the correctness of the result by converting 2's complement answer back to original decimal form. **[8M]**

**-14 – 4**

**QUESTION 3 [7 MARKS]**

a. **Figure 1** shows 3 inputs (A, B, C) and output (y) waveforms of a logic gate. Observe the waveforms and write a concise logic statement for the gate. **[5M]**

b. Determine the single logic gate that (a) represents. Draw the logic gate. **[2M]**

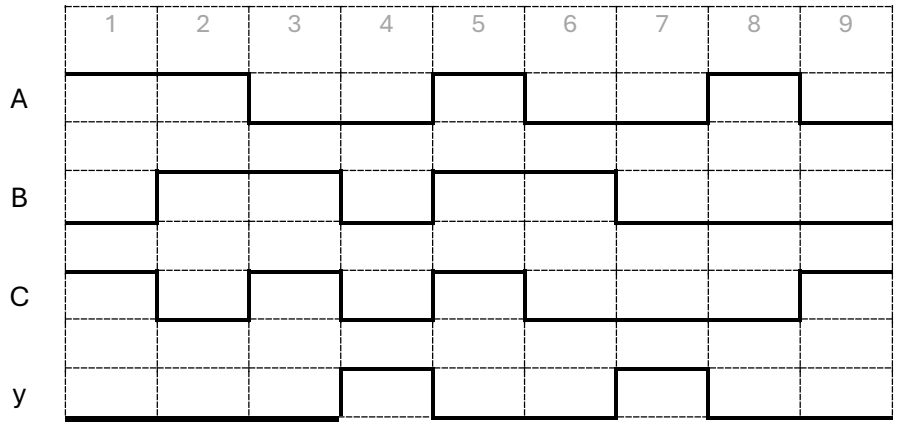


**Figure 1** waveform

**QUESTION 4 [19 MARKS]**

a. Determine the most simplified form of the following Boolean expression using Boolean rules & laws and applying DeMorgan theorem. **[8M]**

$$F = \overline{\bar{x} \bullet (x + y) \bullet [\overline{(x + y)} + (\overline{\bar{x} + \bar{y}})]}$$

b. Transform the following Boolean function into simplified POS function. **[11M]**

F (A, B, C, D) = $AB\bar{C} + \overline{(A\bar{C} + \bar{B}D)}$

**QUESTION 5 [23 MARKS]**

a. Convert the logic circuit below using 2 input NOR universal gates only. Show all your workings. **[6M]**

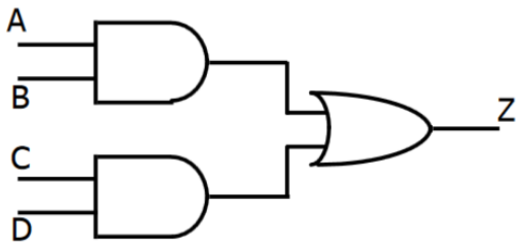


**Figure 2** Logic Circuit

b. Based on the truth table below, implement the active low output by applying the AND-OR-Invert logic. Draw the circuit. You must use Boolean algebra in your answer / solution. Show all your workings. **[14M]**

| Input | | | Output |
|---|---|---|---|
| A | B | C | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

c. Replace the odd or even level the circuit as shown in **Figure 3** below with dual symbol (alternate symbol). Show the final output of the circuit. **[3M]**

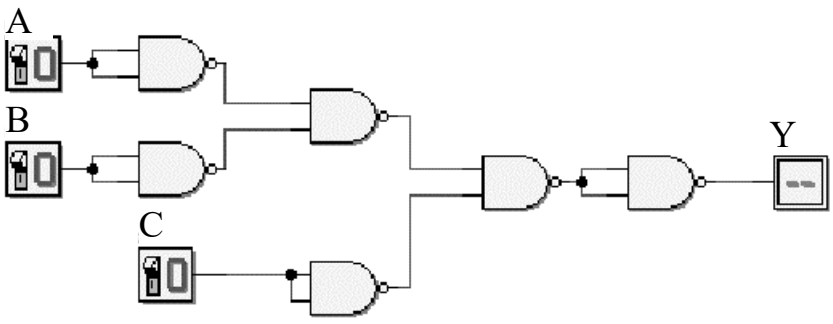


**Figure 3** Logic Circuit

| | |
|---|---|
| 1 | $A + 0 = A$ |
| 2 | $A + 1 = 1$ |
| 3 | $A \quad 0 = 0$ |
| 4 | $A \quad 1 = A$ |
| 5 | $A + A = A$ |
| 6 | $A + A = 1$ |
| 7 | $A \quad A = A$ |
| 8 | $A \quad A = 0$ |
| 9 | $A = A$ |
| 10 | $A + AB = A$ |
| 11 | $A + AB = A + B$ |
| 12 | $(A + B)(A + C) = A + BC$ |