



## COURSE INFORMATION

<b>School/Faculty:</b>	Faculty of Computing		
<b>Program name:</b>	BSc in Software Engineering with honours		
<b>Course code:</b>	SCSR1013	<b>Academic Session/Semester:</b>	20252026/1
<b>Course name:</b>	Digital Logic	<b>Pre/co requisite (course name and code, if applicable):</b>	
<b>Credit hours:</b>	3		

<b>Course synopsis</b>	This foundational course <b>introduces</b> students to the principles of digital electronics as the basis for microprocessor-based systems in computers, robots, automobiles, and industrial control applications. It covers key topics including number systems and codes, logic gates, Boolean algebra, combinational logic circuits, latches, flip-flops, counters, and shift registers, progressing from basic concepts to programmable logic devices. Teaching and learning are carried out through <b>lectures, tutorials, hands-on labs</b> with Deeds Software, and <b>project-based</b> activities, emphasizing <b>problem-solving, collaboration</b> , and practical application. By the end of the course, students will be able to <b>apply</b> digital logic fundamentals, <b>design</b> and construct circuits using simulation tools and real devices, and <b>suggest</b> improvements to enhance solutions for practical problems.			
<b>Course coordinator (If applicable)</b>	Ahmad Fariz Bin Ali			
<b>Course lecturer(s)</b>	<b>Name</b>	<b>Office</b>	<b>Contact no.</b>	<b>E-mail @utm.my</b>
	Ahmad Fariz Bin Ali			ahmadfariz
	Muhaim Bin Mohamed Amin, Dr.			muhaim
	Zuriahati Binti Mohd Yunus, Dr.			zuriahati

**Mapping of the Course Learning Outcomes (CLO) to the Programme Learning Outcomes (PLO), Teaching & Learning (T&L) methods and Assessment methods:**

No.	* CLO	PLO ** (MQF Cluster Code)	*** Taxonomies and **** Graduate Attributes	T&L methods	***** Assessment methods
CLO1	Apply the fundamentals of digital knowledge concepts and numbering systems to digital logic circuits by using <b>critical thinking</b> to evaluate accuracy and effectiveness.	PLO1 (C1)	C3 SC1	Lectures Tutorial	Tu, Q, T, F
CLO2	Demonstrating <b>normative</b> skills in managing and coordinating relevant information to design and construct a digital logic circuit using appropriate technologies, while adhering to shared standards and best practices to solve practical problems effectively.	PLO6 (C3D)	P4 A(IT2)	Lectures Hands-on Lab	L
CLO3	Suggest further improvement for the solution to the problem in digital logic by demonstrating <b>awareness</b> of system limitations and possible enhancements.	PLO9 (C4A)	A4 A(ES2)	Project-based Learning	D, PR

This is the basic mapping required for the CI. Any added information is allowed (extra columns for weight or other elements) provided this is made consistent for all CI at program/school/faculty level.

\* Up to 5 CLO

Refer \*\*\* Taxonomies of Learning and \*\*\*\* UTM's Graduate Attributes for UG and Generic Skills for PG, where applicable for measurement of outcomes achievement

\*\*\*\*\* Q – Quiz; T – Test; L – Lab; Tu – Tutorial; D – Demo; PR – Project; F – Final Exam.

### \*\* MQF Cluster Code

C1 = Knowledge & Understanding, C2 = Cognitive Skills, C3A = Practical Skills, C3B = Interpersonal Skills, C3C = Communication Skills, C3D = Digital Skills, C3E = Numeracy Skills, C3F = Leadership, Autonomy & Responsibility, C4A = Personal Skills, C4B = Entrepreneurial Skills, C5 = Ethics & Professionalism

### Details on Innovative T&L practices:

No.	Type	Implementation
1	Hands-on Lab	Hands-on sessions are conducted using Deeds Software and ETS-5000 Logic Kit, where students work in pairs simulate and test digital logic circuits. This provides an interactive platform to apply theoretical concepts, verify circuit functionality, and develop problem-solving skills through direct experimentation.
2	Project-based Learning	Conducted through a design project, where students work in group to develop digital logic solutions involving both design and verification using Deeds simulator. The project emphasizes compliance with given design specifications, and outcomes are documented through written reports and demonstrated in practical demos, reinforcing teamwork, technical proficiency, and communication skills.

This course helps students build transferable skills by applying digital logic concepts to practical circuit design and improvement. Through lab work with Deeds Software and real devices, they develop **normative skills** in managing information, coordinating tasks, and using technology effectively while adhering to shared standards. The design project further enhances **awareness** by encouraging students to suggest improvements, recognize system limitations, and propose enhancements. These experiences foster problem-solving, adaptability, collaboration, and communication, preparing students to apply their knowledge in diverse professional and academic contexts.

Week/ Meeting	Course Content Outline and Subtopics	CLO*	Learning and Teaching Activities										TOTAL SLT	
			Face-to-Face (F2F)								Non F2F Independent Learning			
			Physical				Online (Synchronous)				Online (Asynchronous)	Others		
			L	T	P	O	L	T	P	O				
Week 1	Introduction	CLO1	2	1									2	5
Week 2	Digital Logic Overview	CLO1	2	1								1	2	6
Week 3	Number Systems and Codes	CLO1	2	1									2	5
Week 4	Logic Gates <b>Quiz 1</b> (Chap 1 and 2)	CLO1 CLO2	2	1								1	2	6
Week 5	Boolean Algebra and Logic Simplification	CLO1	2	1									2	5
Week 6			2	1								1	2	6
Week 7	Combinational Logic Circuit	CLO1 CLO2	2	1									2	5
Week 8	SEM BREAK													
Week 9	Functions of Combinational Logic <b>Quiz 2</b> (Chap 4)	CLO1	2	1								1	2	6
Week 10	Latches and Flip-flops	CLO1	2	1									2	5
Week 11	<b>Midterm Test</b> Date: 16.12.2025 (Tuesday) Time: 8pm - 10:30pm Counters: Asynchronous	CLO1	2	1								1	2	6
Week 12			2	1									2	5
Week 13	Counters: Synchronous	CLO1 CLO2 CLO3	2	1								1	2	6
Week 14		2	1									2	5	
Week 15	Shift Registers <b>Quiz 3</b> (Chap 7 and 8)	CLO1	2	1								1	2	6
											SUB-TOTAL SLT :		77	

Final Assessment		%	Face-to-Face (F2F)		Non F2F Independent Learning for Assessment		TOTAL SLT
			Physical	Online (Synchronous)	Online (Asynchronous)	Others	
1	Final Exam	30	3			9	12
					SUB-TOTAL SLT :		12
					SLT for Assessment :		43
					GRAND TOTAL SLT :		120
A	% SLT for F2F Physical Component :				45.83		
B	% SLT for Online & Independent Learning Component :				54.17		
C	% SLT for Online Component :				9.17		
D	% SLT for All Practical Component :				0.00		
D1	% SLT for F2F Physical Practical Component :				0.00		
D2	% SLT for F2F Online Practical Component :				0.00		
Please tick (✓) if this course is Industrial Training/ Clinical Placement/ Practicum using 50% of Effective Learning Time (ELT)							

**Identify special requirement or resources to deliver the course** (e.g., software, nursery, computer lab, simulation room etc )

Digital Logic Lab and Lab Assistant (TA)

Software: Deeds Software, WinCUPL software, Wellon software, Universal Programmer Hardware: Burner device, ETS5000, Integrated Circuits (IC), IC Tester, Coloured wire.

**References** (include required and further readings, and should be the most current)

1. Floyd, T. L. (2015). Digital fundamentals (11th ed.). Prentice Hall.
2. Monkman, G. (2022). Digital electronics. Springer. <https://doi.org/10.1007/978-3-031-69726-5>
3. Roth, C. (2014). Fundamentals of logic design (7th ed.). Thomson Brooks.
4. School of Computing, Faculty of Engineering, UTMJB. (2020). Digital logic. UTMJB.
5. School of Computing, Faculty of Engineering, UTMJB. (2020). Digital logic lab manual. UTMJB.
6. Tocchi, R. J., Widmer, N. S., & Moss, G. L. (2014). Digital systems (11th ed.). Prentice Hall.
7. Universiti Teknologi Malaysia. (n.d.). UTM eLearning portal. <http://elearning.utm.my>
8. Ward, H. H. (2022). Mastering digital electronics. Springer. <https://doi.org/10.1007/978-1-4842-9878-7>

**Academic honesty and plagiarism:**

Assignments are individual tasks and NOT group activities (UNLESS EXPLICITLY INDICATED AS GROUP ACTIVITIES)

Copying of work (texts, simulation results etc.) from other students/groups or from other sources is not allowed. Brief quotations are allowed and then only if indicated as such. Existing texts should be reformulated with your own words used to explain what you have read. It is not acceptable to retype existing texts and just acknowledge the source as a reference. Be warned: students who submit copied work will obtain a mark of zero for the assignment and disciplinary steps may be taken by the Faculty. It is also unacceptable to do somebody else's work, to lend your work to them or to make your work available to them to copy.

**Other additional information** (if applicable)

All students must adhere to the following to pass a computing course:

- i. Pass both Continuous Assessment AND Final Assessment.
- ii. Get at least minimum pass marks following UTM regulation (40% or D+).

The passing mark for:

- Continuous Assessment is 30% of continuous marks.
- Final Assessment is 20% of the final marks.

If a student does not achieve the passing mark for Continuous Assessment OR the passing mark for the Final Assessment, then the student's overall final mark will be set below the UTM passing mark.

**Disclaimer:**

All teaching and learning materials associated with this course are for personal use only. The materials are intended for educational purposes only. Reproduction of the materials in any form for any purposes other than what it is intended for is prohibited.

While every effort has been made to ensure the accuracy of the information supplied herein, Universiti Teknologi Malaysia cannot be held responsible for any errors or omissions.

$ELT = (\text{Theory} + \text{Industrial Guidance} + \text{Assessment}) \times 50\%$

Total of credit for LI/Practical =  $ELT/40$  Notional Hours

Note: For ODL Programme : Courses with mandatory practical requirement imposed by programme standards or any related standards can be exempted from complying to the minimum 80% ODL delivery rule in the SLT.

**Prepared by :**

**Name :** Ahmad Fariz Bin Ali

**Signature :**

**Date :** 4-Oct-2025



**Certified by:**

**Name :** Md. Asri Bin Ngadi, Prof. Dr.

**Signature :**

**Date :** 4-Oct-2025

