UNIVERSITI TEKNOLOGI MALAYSIA

RESEARCH UNIVERSITY

MIDTERM TEST SEMESTER 1 20xx/20xx

COURSE CODE	**:**	**SECR1013**
COURSE TITLE	**:**	**DIGITAL LOGIC**
TOTAL TIME	**:**	**2 HOUR 30 MINUTES**
DATE	**:**	
VENUE	**:**	

(GENERAL INSTRUCTION):

Write ALL your answers in the answer booklet. Show all your workings.

This test will contribute 20% towards the total marks of 100.

Warning!

Students who are caught cheating during the examination will be reported to the disciplinary board for possible suspension of the student for one or two semesters.

Name	
Metric No	
Year / Course	
Section (Circle)	**01 / 02 / 03 / 04 / 05 / 06 / 07 / 08 / 09 / 10 / 11 / 12**
Lecturer (Circle)	

This question booklet consists of 6 pages excluding the front page.

QUESTION 1 [15 MARKS]

a. State **TRUE** or **FALSE** for the following statements. [4]

i. Digital quantities varies continuously according to time of the day.

ii. Digital to Analog Converter (DAC) converts digital data to analog signal which is amplified to produce the original analog sound.

iii. Non periodic square wave keeps on repeating after a fixed time period.

iv. The unit Kilo (K) is represented by 10^6.

b. Identify the correct **term** for the following descriptions **(i) to (iv)** from the answer options below. [4]

Descriptions	**Term**
It is a method for constructing electronic circuits in which the components are mounted directly onto the surface of printed circuit boards (PCBs).	**(i)**
Which PLD is categorized as SPLD?	**(ii)**
Hardware description language or HDL is any language from a class of computer languages and/or programming languages for formal description of digital logic and electronic circuits. It can describe the circuit's operation, its design and organization, and tests to verify its operation by means of simulation.	**(iii)**
Which of the following is fixed function integrated circuit technology?	**(iv)**

Answer options:

TTL	PAL	Wellon Programmer	SMT
Fine Grain	WinCUPL	CPLD	Coarse Grain

c. Details are given as follows: **frequency(*f*)=5MHz** and **duty cycle=75%**. Draw duty cycle diagram to show on and off state and label the diagram clearly with pulse width (t_w) and period (T) in microsecond (μs). Show all your workings. [7]

QUESTION 2 [24 MARKS]

a. Convert the base-7 number $\mathbf{2431_7}$ to its **decimal** equivalent. Show all your workings. [4]

b. Convert the decimal number $\mathbf{47.234_{10}}$ to **octal**. Answer in **4 radix points**. Show all your workings. [5]

c. Convert the binary number $\mathbf{11110.110011_2}$ to its **hexadecimal** equivalent. Show all your workings. [4]

d. Convert the binary number $\mathbf{101101_2}$ to Gray code. Show all your workings. [3]

e. Perform the arithmetic operation using **8-bit 2's complement** system. Show all your workings, including the numbers in 2's complement form, the addition process, and the result. Finally, check the correctness of the result by converting 2's complement answer back to original decimal form. [8]

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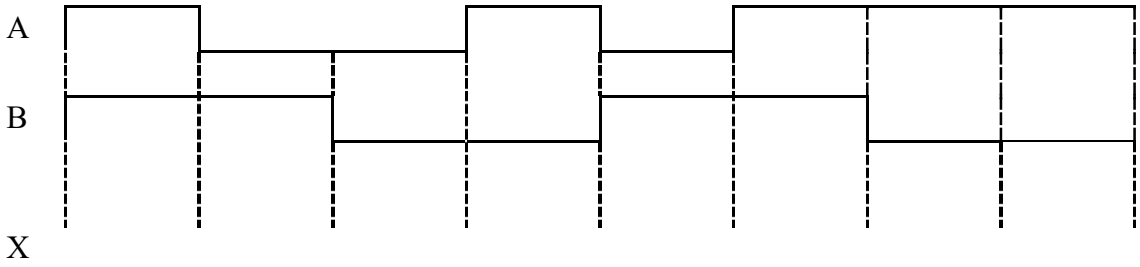
QUESTION 3 [7 MARKS]

a. Draw timing diagram for output $\boldsymbol{X} = \boldsymbol{A} \oplus \mathbf{B}$ in your answer booklet. Please copy and redraw the timing diagram exactly as shown below in your answer booklet. [4]



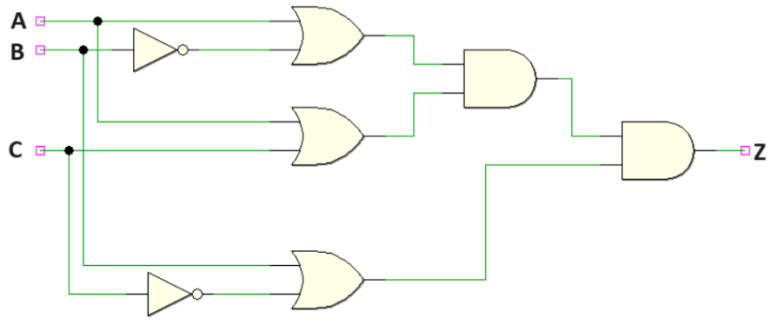
b. Draw a logic circuit using basic gates for the following Boolean expression below without expending the expression. [3]

$$(\boldsymbol{A} + \mathbf{B})\overline{\mathbf{C}}$$

QUESTION 4 [26 MARKS]

a. Simplify Boolean expression $\boldsymbol{Z = AB + \overline{C}(\overline{BC + AC})}$ using Boolean Algebra laws, rules, and De Morgan theorem. Show all your workings. [7]

b. Given the circuit below, [5]



i. Write the Boolean expression Z.

ii. Convert the Boolean expression Z to **standard POS** form. Show all your workings.

c. Given the truth table below, produce minimum **SOP** expression Z using K-Map. Show all your workings. [6]

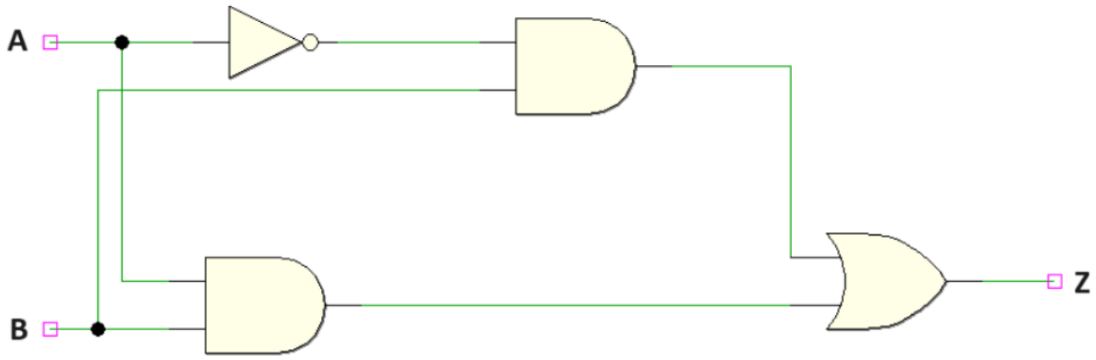
A	B	C	D	Z
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

d. Using K-Map minimization, find the minimum **POS** expression W for the following. Show all your workings. [8]

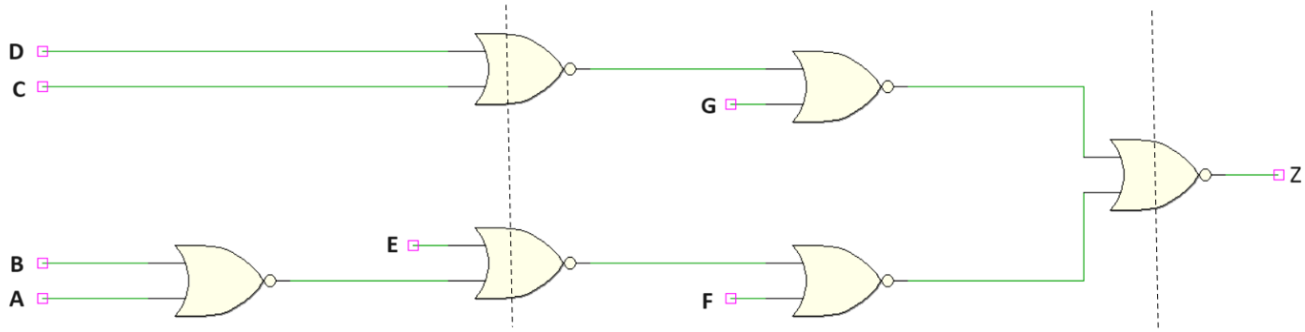
$$\mathbf{W} = \boldsymbol{\pi_{ABCD}}\ (\mathbf{2, 5, 6, 8, 11}) + \boldsymbol{d}(\mathbf{1, 3, 7, 10})$$

QUESTION 5 [28 MARKS]

a. Convert the following circuit below to **NAND** universal gate circuit using dual symbol. Show all your workings. [3]



b. Simplify schematic reading of Boolean expression Z using dual symbol for NOR universal gate at **ODD level** for the circuit shown below. Get Boolean expression Z and show all your workings in the answer booklet. [5]



c. A circuit processes **4 bit 2's complement number** with **binary inputs A, B, C, D** and **2 outputs X, Y.** Output X is to detect negative sign bit and output Y is to detect parity bit error. Design a circuit according to the following rules: [20]

RULE 1:

- **Binary inputs values A, B, C, D ABOVE than 1011 are INVALID.**

RULE 2:

- **Output X is HIGH when sign bit detected is NEGATIVE.**

RULE 3:

- **The circuit uses ODD parity with A as parity bit.**
- **Output Y is HIGH when parity bit error is detected.**

i. Construct complete **truth table** using the following header.

INPUT				**OUTPUT**	
A	**B**	**C**	**D**	**X**	**Y**

ii. Get minimum **SOP** Boolean expression for X and Y.

iii. Draw **circuit for X and Y** using **3 input** basic gates NOT, AND, OR.

1	$A + 0 = A$
2	$A + 1 = 1$
3	$A \bullet 0 = 0$
4	$A \bullet 1 = A$
5	$A + A = A$
6	$A + \overline{A} = 1$
7	$A \bullet A = A$
8	$A \bullet \overline{A} = 0$
9	$\overline{\overline{A}} = A$
10	$A + AB = A$
11	$A + \overline{A}B = A + B$
12	$(A + B)(A + C) = A + BC$