DESIGN PROJECT

Design, lay out, and simulate a CMOS four-input XOR gate in the standard 0.25 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use: you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 2.5 V! Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit.

The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.5 ns and occupy an area of no more than 500 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay.

The design will be graded on the magnitude of $A \times t_p^2$, the product of the area of your design and the square of the delay for the worst-case transition.

A. Design Reference Invertor

Design Data — Transistor Model for Manual Analysis

Table 3.2 tabulates the obtained parameter values for the minimum-sized NMOS and a similarly sized PMOS device in our generic 0.25 μm CMOS process. These values will be used as generic model-parameters in later chapters.

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

[3] A MATLAB implementation of the model is available on the web-site of the textbook.

From Eq. (5.2), we can derive the required ratio of PMOS versus NMOS transistor sizes such that the switching threshold is set to a desired value V_M. When using this expression, please make sure that the assumption that both devices are velocity-saturated still holds for the chosen operation point.

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)} \tag{5.5}$$

Design Technique — Maximizing the noise margins

When designing static CMOS circuits, it is advisable to balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section, if one wants to maximize the noise margins and obtain symmetrical characteristics. The required ratio is given by Eq. (5.5).

Example 5.1 Switching threshold of CMOS inverter

We derive the sizes of PMOS and NMOS transistors such that the switching threshold of a CMOS inverter, implemented in our generic 0.25 µm CMOS process, is located in the middle between the supply rails. We use the process parameters presented in Example 3.7, and assume a supply voltage of 2.5 V. The minimum size device has a width/length ratio of 1.5. With the aid of Eq. (5.5), we find

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{30 \times 10^{-6}} \times \frac{0.63}{1.0} \times \frac{(1.25 - 0.43 - 0.63/2)}{(1.25 - 0.4 - 1.0/2)} = 3.5$$

Figure 5.7 plots the values of switching threshold as a function of the PMOS/NMOS ratio, as obtained by circuit simulation. The simulated PMOS/NMOS ratio of 3.4 for a 1.25 V switching threshold confirms the value predicted by Eq. (5.5).

Because VDD= 2.5 V, and From the result in Example 5.1, We chose

$$\frac{(W/L)_p}{(\frac{W}{L})_n}=3$$

Design Data — MOS Transistor Capacitances

Table 3.5 summarizes the parameters needed to estimate the parasitic capacitances of the MOS transistors in our generic 0.25 µm CMOS process.

Table 3.5 Capacitance parameters of NMOS and PMOS transistors in 0.25 µm CMOS process.

	C_{ox} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (*V*)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (*V*)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

a considerable simplification of the actual situation, even in the case of a simple inverter.

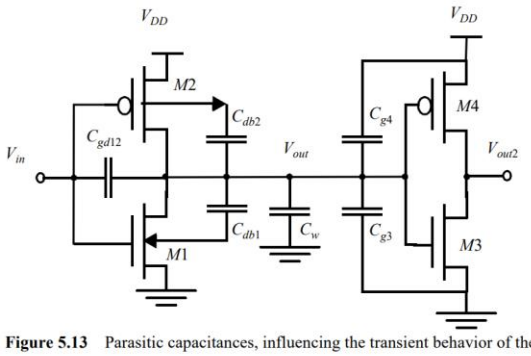


Figure 5.13 Parasitic capacitances, influencing the transient behavior of the cascaded inverter pair.

When the PMOS devices are made β times larger than the NMOS ones ($\beta = (W/L)_p / (W/L)_n$), all transistor capacitances will scale in approximately the same way, or $C_{dp1} \approx \beta C_{dn1}$, and $C_{gp2} \approx \beta C_{gn2}$. Eq. (5.23) can then be rewritten:

$$C_L = (1+\beta)(C_{dn1} + C_{gn2}) + C_W \tag{5.24}$$

An expression for the propagation delay can be derived, based on Eq. (5.20)

Cint = Cgd12+Cdb2+ Cb1 =

$$C_{int} = C_{gd1} + C_{gd2} + C_{db1} + C_{db1}$$

Table 5.1 Inverter transistor data.

	W/L	AD (μm^2)	PD (μm)	AS (μm^2)	PS (μm)
NMOS	0.375/0.25	0.3 (19 λ^2)	1.875 (15λ)	0.3 (19 λ^2)	1.875 (15λ)
PMOS	1.125/0.25	0.7 (45 λ^2)	2.375 (19λ)	0.7 (45 λ^2)	2.375 (19λ)

This physical information can be combined with the approximations derived above to come up with an estimation of C_L. The capacitor parameters for our generic process were summarized in Table 3.5, and repeated here for convenience:

Overlap capacitance: CGD0(NMOS) = 0.31 fF/μm; CGDO(PMOS) = 0.27 fF/μm
Bottom junction capacitance: CJ(NMOS) = 2 fF/μm^2; CJ(PMOS) = 1.9 fF/μm^2
Side-wall junction capacitance: CJSW(NMOS) = 0.28 fF/μm; CJSW(PMOS) = 0.22 fF/μm
Gate capacitance: C_{ox}(NMOS) = C_{ox}(PMOS) = 6 fF/μm^2

Table 5.2 Components of C_L (for high-to-low and low-to-high transitions).

Capacitor	Expression	Value (fF) (H→L)	Value (fF) (L→H)
C_{gd1}	$2\ CGD0_n\ W_n$	0.23	0.23
C_{gd2}	$2\ CGD0_p\ W_p$	0.61	0.61
C_{db1}	$K_{eqn}\ AD_n\ CJ + K_{eqswn}\ PD_n\ CJSW$	0.66	0.90
C_{db2}	$K_{eqp}\ AD_p\ CJ + K_{eqswp}\ PD_p\ CJSW)$	1.5	1.15
C_{g3}	$(CGD0_n+CGSO_n)\ W_n + C_{ox}\ W_n\ L_n$	0.76	0.76
C_{g4}	$(CGD0_p+CGSO_p)\ W_p + C_{ox}\ W_p\ L_p$	2.28	2.28
C_w	From Extraction	0.12	0.12
C_L	Σ	6.1	6.0

$$C_{int} = C_{gd1} + C_{gd2} + C_{db1} + C_{db1}$$

$$= 2CGD0_nW_n + 2CGD0_nW_n + C_{db1} + C_{db1}$$

$$= 2 * 0.31\left(\frac{fF}{um}\right) * W_n(um) + 2 * 0.27\left(\frac{fF}{um}\right) * W_p(um) + 0.66\ (fF) + 1.5\ (fF)$$

$$= 0.62\ W_n(fF) + 0.54 * W_p(fF) + 2.16(fF)$$

We have $C_L = C_{int} + C_{ext}$

From the requirement with external load = 20 fF, so

$$C_L = C_{int} + C_{ext} = 0.62\ W_n(fF) + 0.54 * W_p(fF) + 2.16(fF) + 20fF$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

Design Data — Equivalent Resistance Model

Table 3.3 enumerates the equivalent resistances obtained by simulation of our generic 0.25 µm CMOS process. These values will come in handy when analyzing the performance of CMOS gates in later chapters.

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 µm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

And with he generic 0.25 um CMOS process, we have the R_{eq} for NMOS and PMOS at VDD=2.5 V is:

$$R_{eqn} = 13\ K\Omega\ and\ R_{eqp} = 31\ K\Omega$$

And with the requirement for propagation delay is <0.5ns.

$$t_p = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right) < 0.5ns$$

$$t_p = 0.69\left(0.62\ W_n(fF) + 0.54 * W_p(fF) + 2.16(fF) + 20fF\right)\left(\frac{R_{eqn} + R_{eqp}}{2} \right) < 0.5ns$$

So we must choose W_n, W_p to obtain tp<0.5 ns

$$0.69\left(0.62\ W_n(fF) + 0.54 * W_p(fF) + 2.16(fF) + 20fF\right)\left(\frac{R_{eqn} + R_{eqp}}{2} \right) = 0.5ns$$

So we have equation:

0.6 Wn(fF)+0.54Wp (fF) $= \frac{0.5ns}{\left(\frac{R_{eqn}+R_{eqp}}{2}\right)*0.69} - 20\ fF = \frac{0.5*10^{-9}}{\left(\frac{13*10^3+31*10^3}{2}\right)*0.69} - 20 * 10^{-15}$ = 12.9(fF)

0.6 Wn(fF)+0.54Wp (fF)=12.9(fF);

And Wp=3Fn

To have propagate delay <5ns, the size of invertor must be:

Wp <14.32 um and Wn < 4.48 um

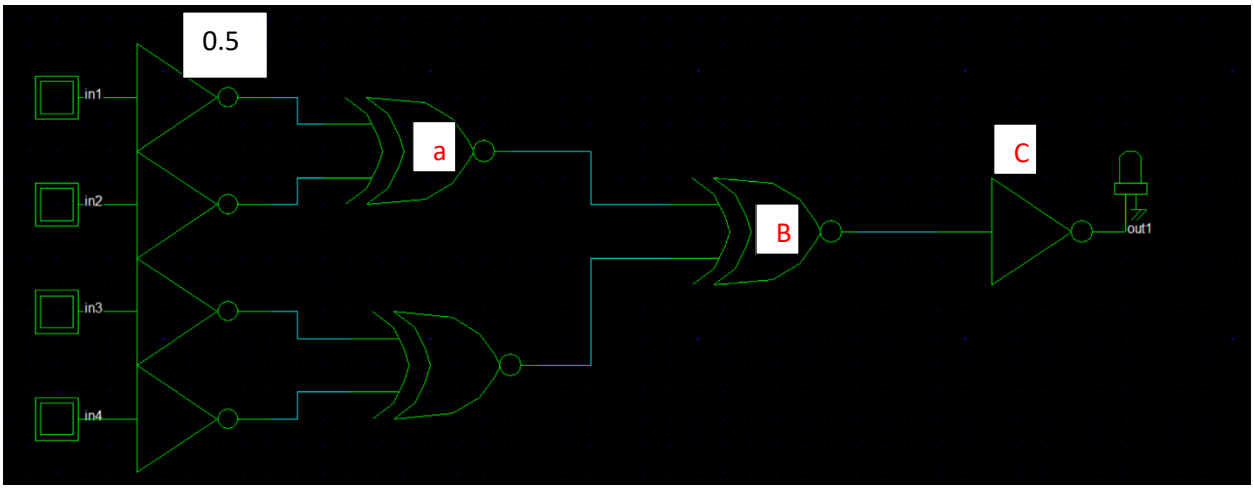
Let choose the size of reference invertor is:

$$W_n = 0.5\ um\ and\ Wp = 1.5\ um$$

So, Cint of of reference invertor is: $0.62\ W_n(fF) + 0.54 * W_p(fF) + 2.16(fF)$

$$= 0.62\ W_n(fF) + 0.54 * W_p(fF) + 2.16(fF) = 0.62 * 0.5 + 0.54 * 1.5 + 2.16 = 3.28\ (fF)$$

Design the 4input XOR gate :



Chọn Wp/Wn = 3,

Choose Wc

Chọn W,Wn

Tìm Cint

Tìm CL

Tìm Delay

+ Tính cái cổng Xor ; s