THE UNIVERSITY OF DANANG
UNIVERSITY OF SCIENCE AND TECHNOLOGY
Faculty of Advanced Science and Technology

LABORATORY REPORT

INTRODUCTION TO VERY LARGE SCALE INTERGRATION IC DESIGN

Instructor **:** Nguyen Van Cuong

Class **:** 21ECE

Student **:** Tran Hoang Minh

Da Nang, October 21st 2024

Introduction:

DESIGN PROJECT

Design, lay out, and simulate a CMOS four-input XOR gate in the standard 0.25 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use: you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 2.5 V! Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit.

The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.5 ns and occupy an area of no more than 500 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay.

The design will be graded on the magnitude of $A \times t_p^2$, the product of the area of your design and the square of the delay for the worst-case transition.

Overview of Microwind and DSCH:

Microwind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator.

DSCH is software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation.

Silicon is for 3D display of the atomic structure of silicon, with emphasis on the silicon lattice, the dopants, and the silicon dioxide

The Microwind software works is based on a lambda grid, not on a micro grid. Consequently, the same layout may be simulated in any CMOS technology. The value of lambda is half the minimum polysilicon gate length. Table A-xxx gives the correspondence between lambda and micron for all CMOS technologies available in the companion CD-ROM.

Technology file available in the CD-Rom	Minimum gate length	Value of lambda
Cmos12.rul	1.2µm	0.6µm
Cmos08.rul	0.7µm	0.35µm
Cmos06.rul	0.5µm	0.25µm
Cmos035.rul	0.4µm	0.2µm
Cmos025.rul	0.25µm	0.125µm
Cmos018.rul	0.2µm	0.1µm
Cmos012.rul	0.12µm	0.06µm
Cmos90n.rul	0.1µm	0.05µm
Cmos70n.rul	0.07µm	0.035µm
Cmos50n.rul	0.05µm	0.025µm

Table 1-xxx: correspondence between technology and the value of lambda in µm

Technical design

Design Reference Invertor

Design Data — Transistor Model for Manual Analysis

Table 3.2 tabulates the obtained parameter values for the minimum-sized NMOS and a similarly sized PMOS device in our generic 0.25 µm CMOS process. These values will be used as generic model-parameters in later chapters.

Table 3.2 Parameters for manual model of generic 0.25 µm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	-0.4	-1	-30×10^{-6}	-0.1

From Eq. (5.2), we can derive the required ratio of PMOS versus NMOS transistor sizes such that the switching threshold is set to a desired value V_M. When using this expression, please make sure that the assumption that both devices are velocity-saturated still holds for the chosen operation point.

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)} \tag{5.5}$$

So we have $\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{115\times10^{-6}}{-30\times10^{-6}} \times \frac{0.63}{-1} \times \frac{2.50-0.43-\frac{0.63}{2}}{2.50-0.4-\frac{1.0}{2}} \approx 3$

Design Data — MOS Transistor Capacitances

Table 3.5 summarizes the parameters needed to estimate the parasitic capacitances of the MOS transistors in our generic 0.25 µm CMOS process.

Table 3.5 Capacitance parameters of NMOS and PMOS transistors in 0.25 µm CMOS process.

	C_{ox} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Table 5.2 Components of C_L (for high-to-low and low-to-high transitions).

Capacitor	Expression	Value (fF) (H→L)	Value (fF) (L→H)
C_{gd1}	2 $CGD0_n$ W_n	0.23	0.23
C_{gd2}	2 $CGD0_p$ W_p	0.61	0.61
C_{db1}	K_{eqn} AD_n CJ + K_{eqswn} PD_n CJSW	0.66	0.90
C_{db2}	K_{eqp} AD_p CJ + K_{eqswp} PD_p CJSW)	1.5	1.15
C_{g3}	($CGD0_n$+$CGSO_n$) W_n + C_{ox} W_n L_n	0.76	0.76
C_{g4}	($CGD0_p$+$CGSO_p$) W_p + C_{ox} W_p L_p	2.28	2.28
C_w	From Extraction	0.12	0.12
C_L	Σ	6.1	6.0

$C_{int} = C_{gd1} + C_{gd2} + C_{db1} + C_{db1}$

$C_{int} = 2CGD0_n W_n + 2CGD0_n W_n + C_{db1} + C_{db1}$

$C_{int} = 2 \times 0.31 \left(\frac{fF}{\mu m}\right) \times W_n(\mu m) + 2 \times 0.27 \left(\frac{fF}{\mu m}\right) \times W_p(\mu m) + 0.66\ (fF) + 1.5\ (fF)$

$C_{int} = 0.62\ \times W_n(fF) + 0.54 \times W_p(fF) + 2.16(fF)$

We have $C_L = C_{int} + C_{ext}$

From the requirement with external load is equal 20 fF, so

$$C_L = C_{int} + C_{ext} = [\,0.62 \times W_n(fF) + 0.54 \times W_p(fF) + 2.16(fF)\,] + 20fF$$

Design Data — Equivalent Resistance Model

Table 3.3 enumerates the equivalent resistances obtained by simulation of our generic 0.25 μm CMOS process. These values will come in handy when analyzing the performance of CMOS gates in later chapters.

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

And with he generic 0.25 um CMOS process, we have the R_{eq} for NMOS and PMOS at VDD=2.5 V is:

$R_{eqn} = 13\ k\Omega\ and\ R_{eqp} = 31\ k\Omega$

And with the requirement for propagation delay is $< 0.5ns$.

$t_p = 0.69C_L \left(\frac{R_{eqn} + R_{eqp}}{2}\right) < 0.5ns$

$t_p = 0.69[0.62\ W_n(fF) + 0.54W_p(fF) + 2.16(fF) + 20(fF)] \left(\frac{R_{eqn} + R_{eqp}}{2}\right) < 0.5ns$

$=> 0.69[0.62 \times W_n(fF) + 0.54 \times W_p(fF) + 2.16(fF) + 20(fF)] \left(\frac{13\ k\Omega + 31\ k\Omega}{2}\right) < 0.5ns$

$=> 0.62 \times W_n(fF) + 0.54 \times W_p(fF) < 10.8\ (fF)$

And we have $\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} \approx 3$ *or* $W_p = 3W_n$

$=> W_p < 17.277\,\mu m$ *and* $W_n < 5.750\,\mu m$

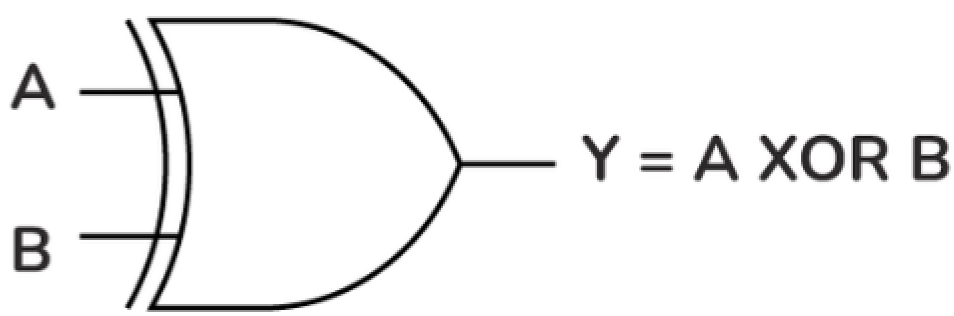
choose $W_p = 2.250\,\mu m$ *and* $W_n = 0.750\,\mu m$

Physical design

The XOR (Exclusive OR) gate is a digital logic gate that outputs true or high only when the two binary bit inputs to it are unequal. In other words, it outputs a 1 when the number of 1's inputs is odd, making it essential for arithmetic functions in computers and other digital systems.

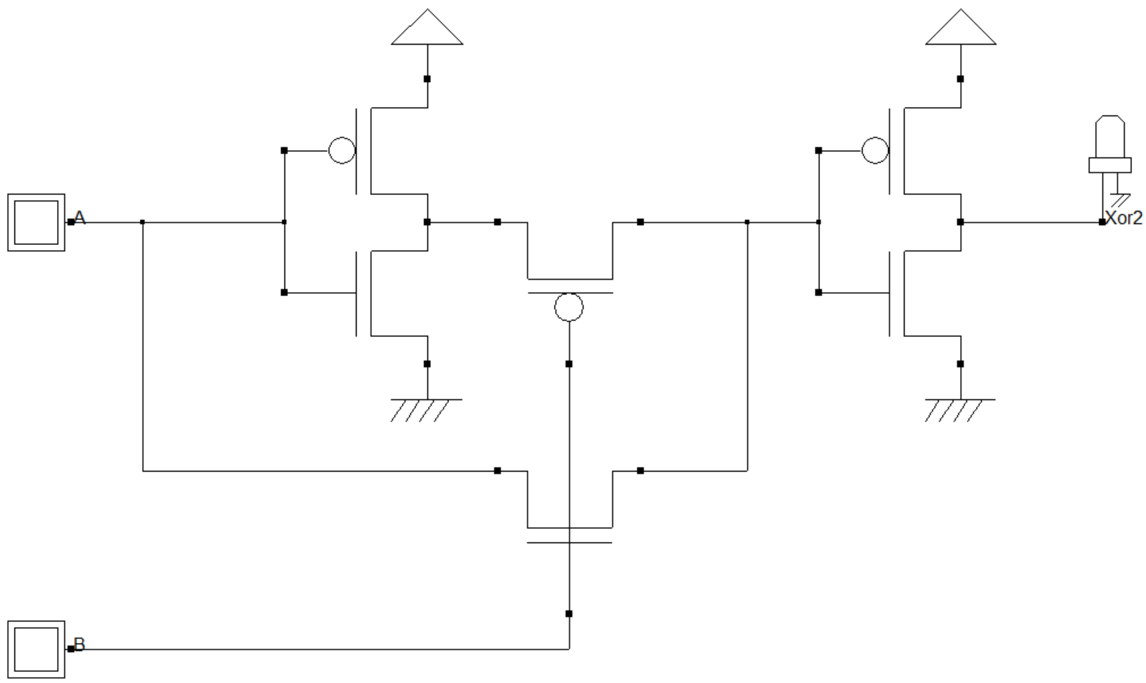
The CMOS layout for an XOR gate using six transistors involves two NMOS transistors in series and two PMOS transistors in parallel for each input combination that results in a high output. The gate uses complementary pairs to ensure that when one path turns off, the other turns on, thereby creating the desired XOR functionality.

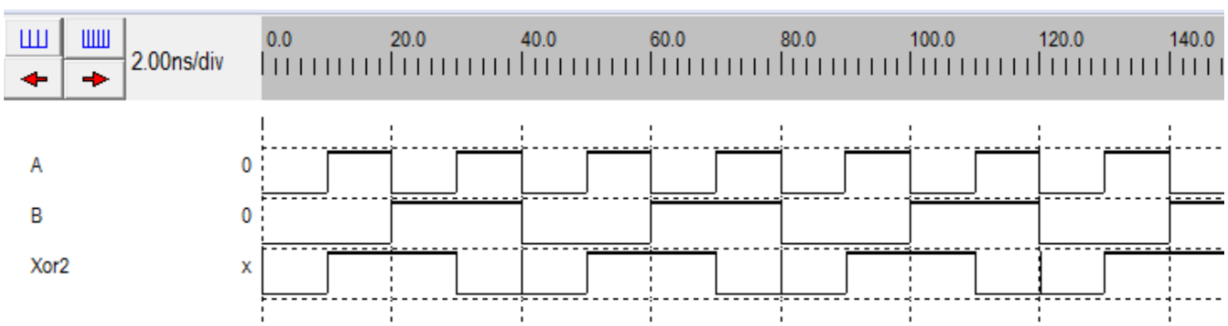
Input A	Input B	Output (A XOR B)
0	0	0
0	1	1
1	0	1
1	1	0



The Boolean expression of two-input XOR gate is Y = = A ⊕ B = AB' + A'B = A'B' + AB

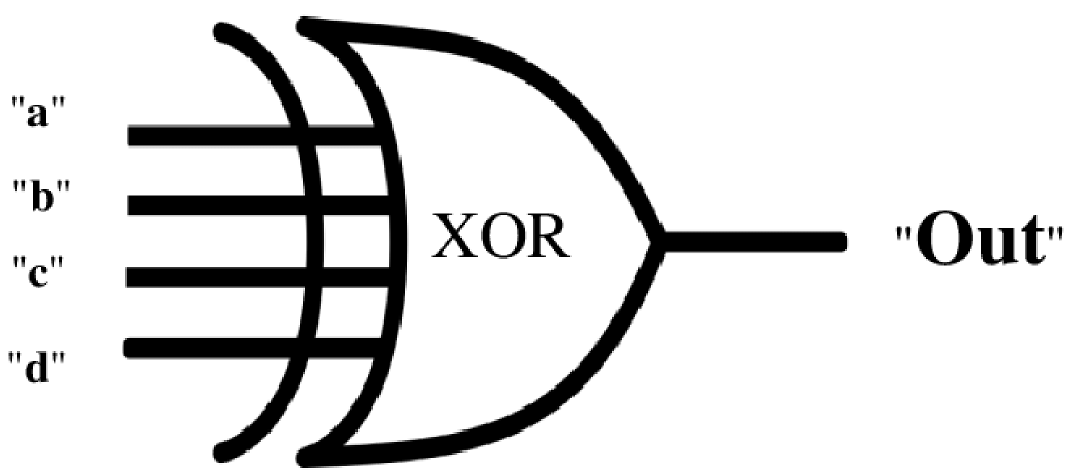
The 6-transistor XOR gate design is a very compact solution for implementing the XOR function. The main drawback is the use of pass transistors which may create non-ideal logic levels due to threshold voltage degradation. In short, n-channel transistors cannot transfer the level 1 correctly, the p-channel transistors cannot transfer the level 0 correctly. Other values are correctly executed. Using DSCH, the observed simulation is always correct, as DSCH do not take into account “weak-1” and “weak-0” levels.



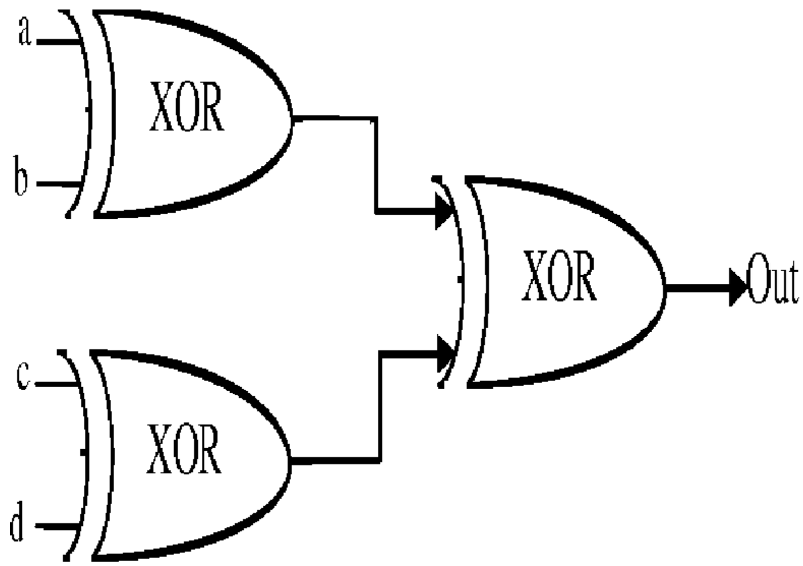


Logic design

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

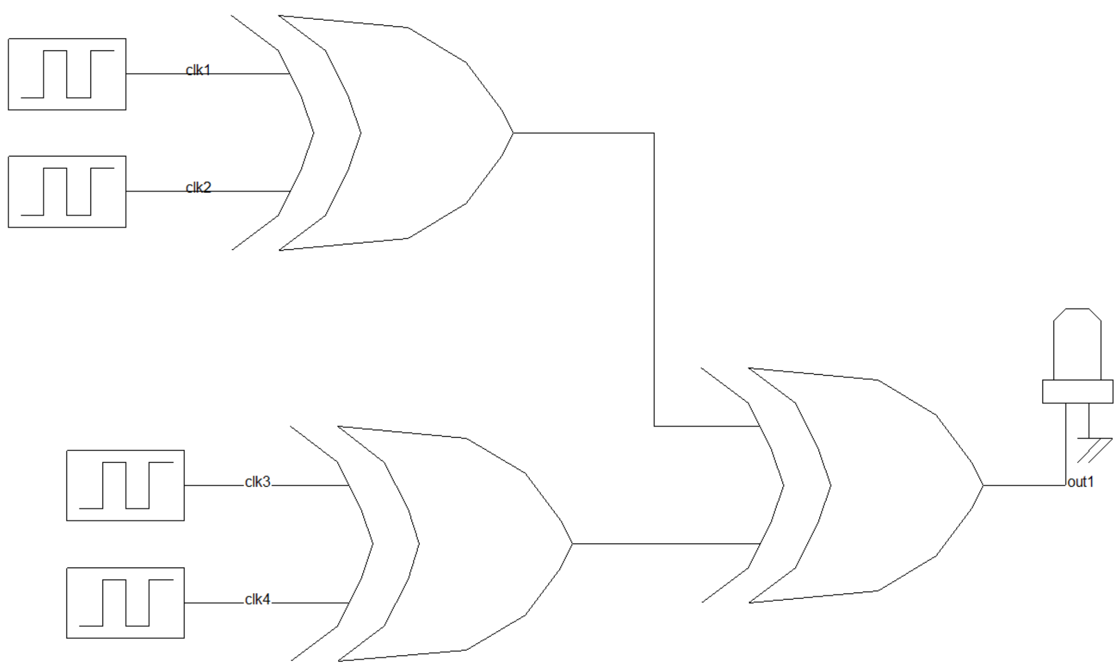


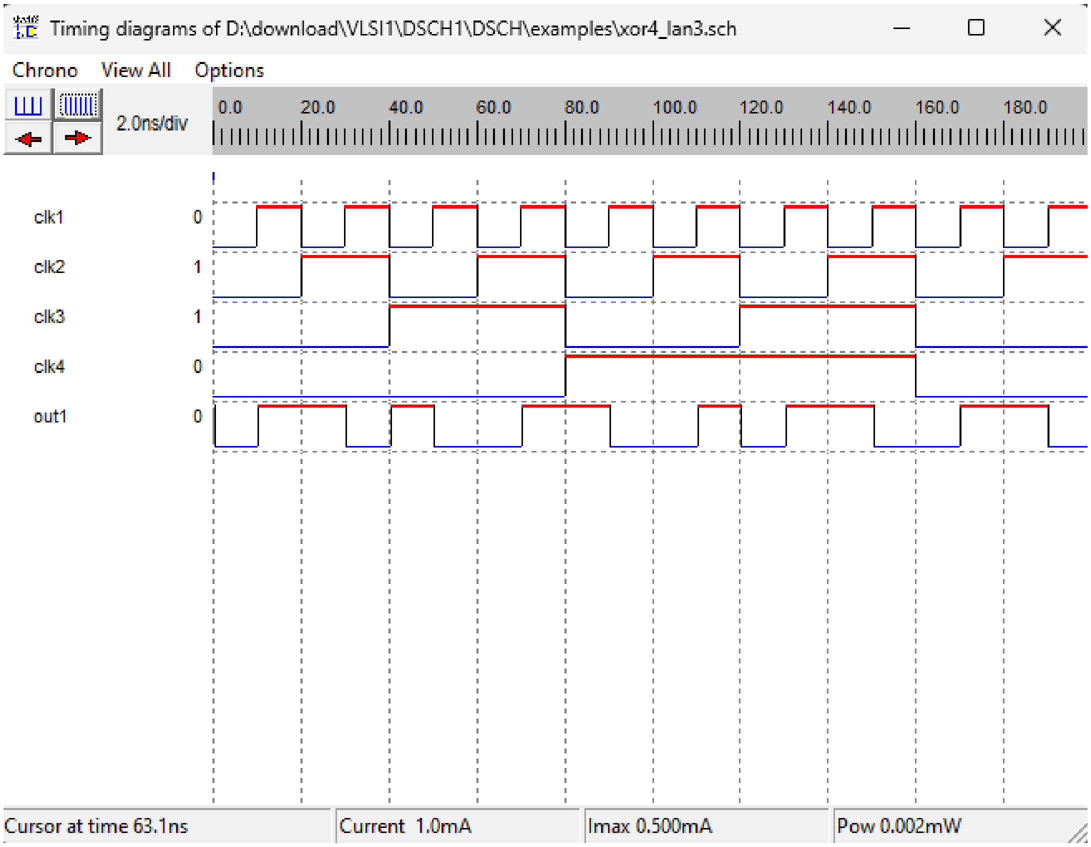
OUT = $A \oplus B \oplus C \oplus D = (A \oplus B) \oplus (C \oplus D)$

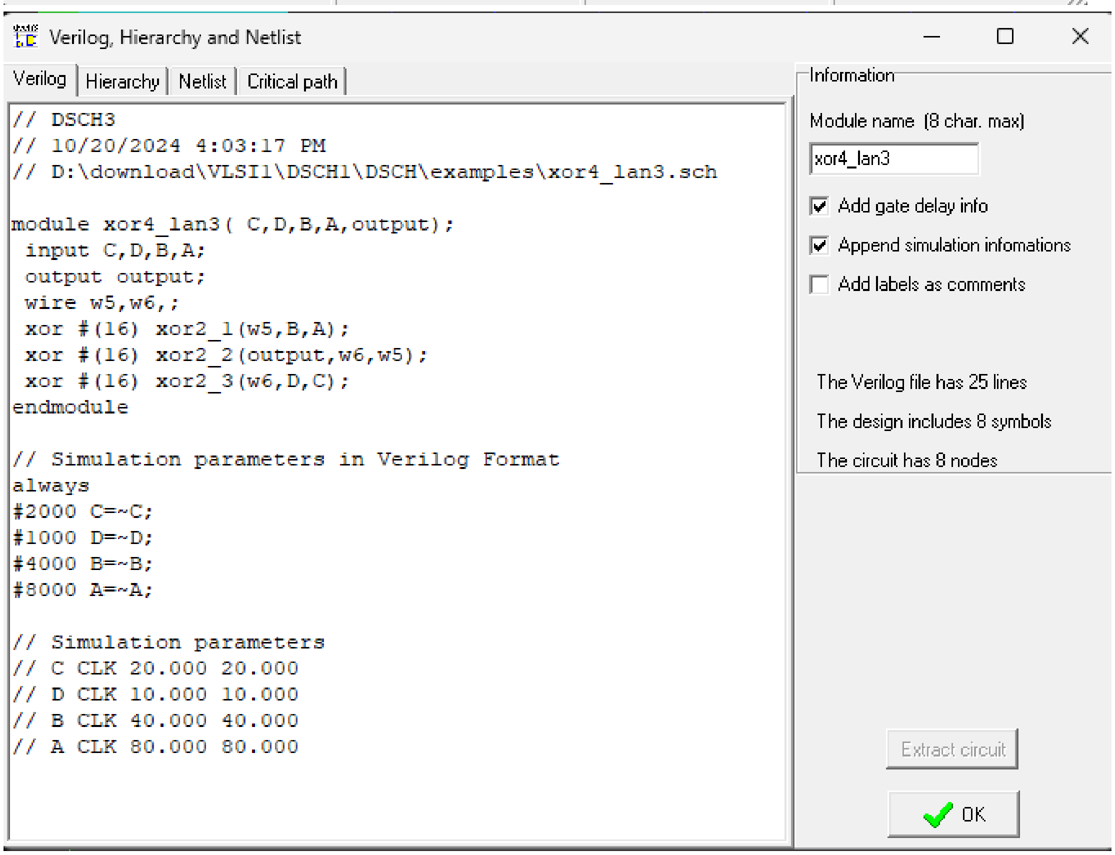


SS

XOR Gate Schematic

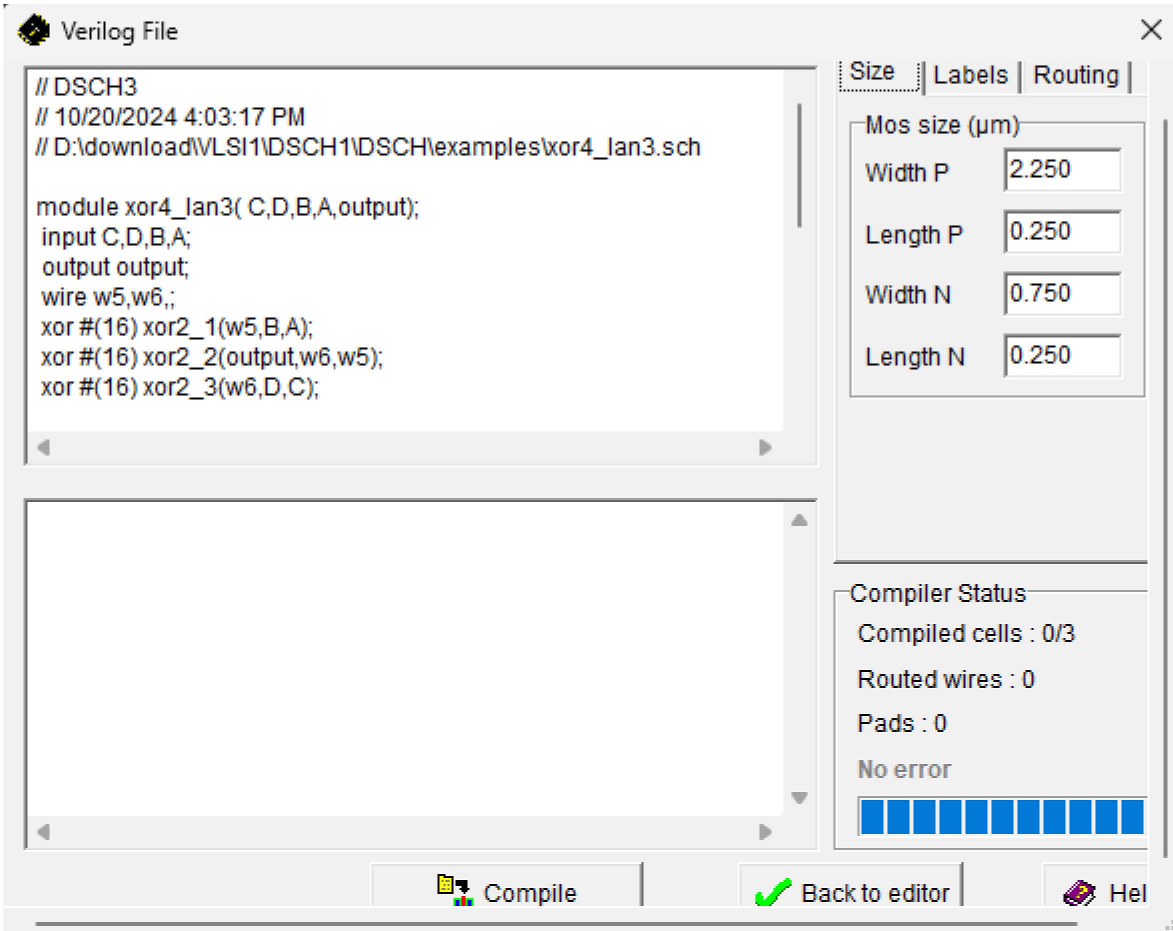


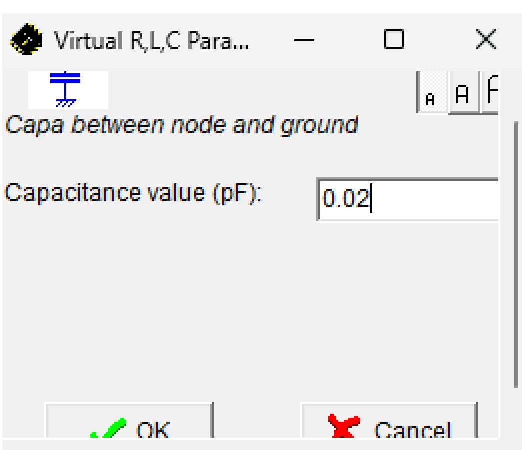


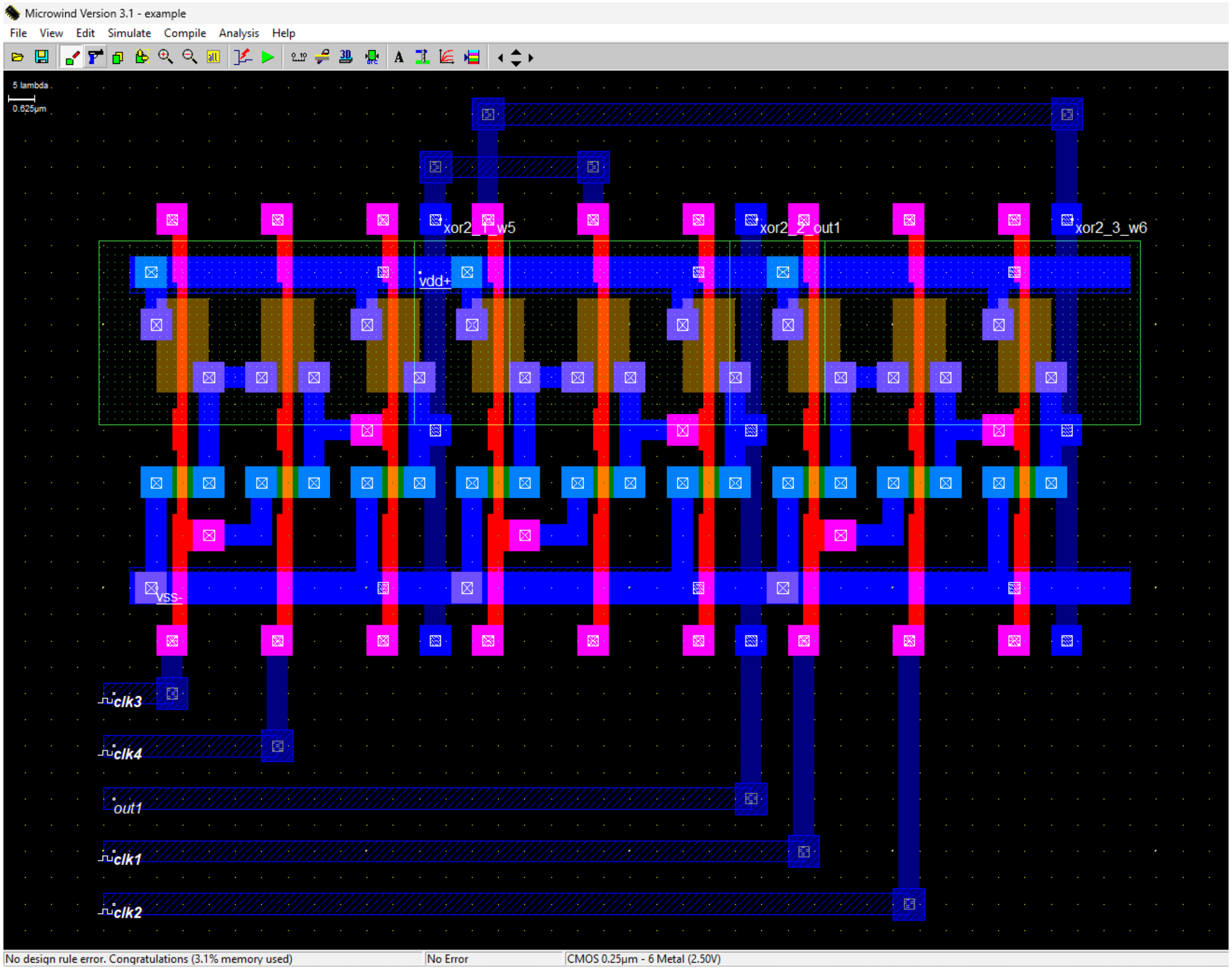



```
// DSCH3
// 10/20/2024 4:03:17 PM
// D:\download\VLSI1\DSCH1\DSCH\examples\xor4_lan3.sch

module xor4_lan3( C,D,B,A,output);
 input C,D,B,A;
 output output;
 wire w5,w6,;
 xor #(16) xor2_1(w5,B,A);
 xor #(16) xor2_2(output,w6,w5);
 xor #(16) xor2_3(w6,D,C);
endmodule

// Simulation parameters in Verilog Format
always
#2000 C=~C;
#1000 D=~D;
#4000 B=~B;
#8000 A=~A;

// Simulation parameters
// C CLK 20.000 20.000
// D CLK 10.000 10.000
// B CLK 40.000 40.000
// A CLK 80.000 80.000
```

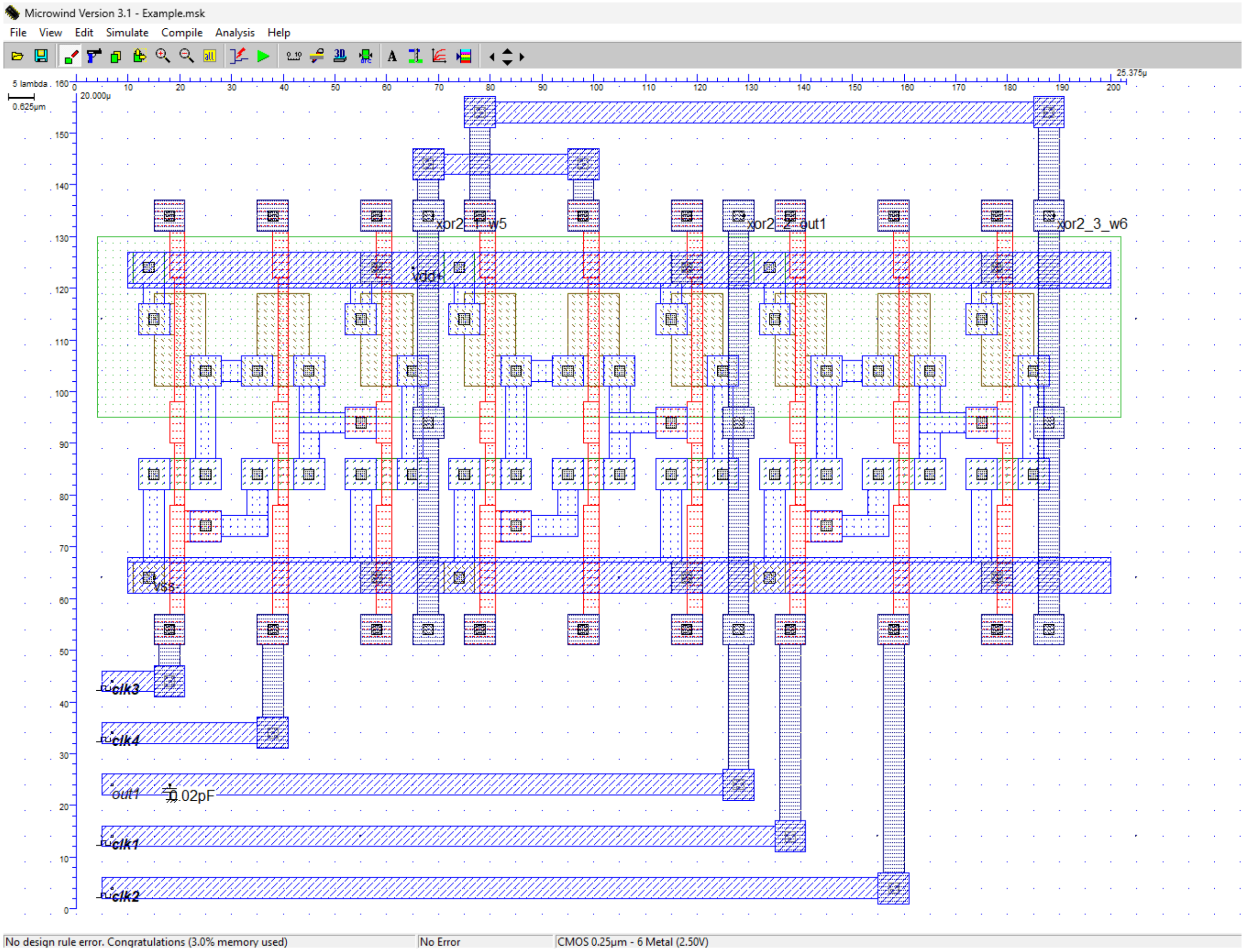
Layout design

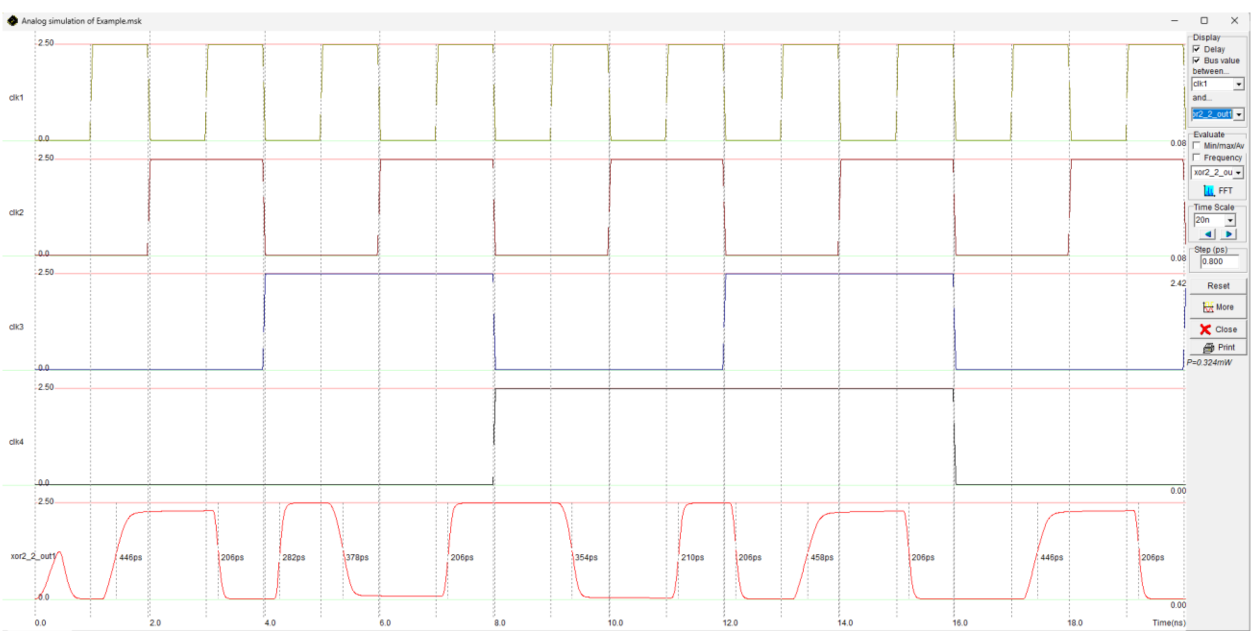


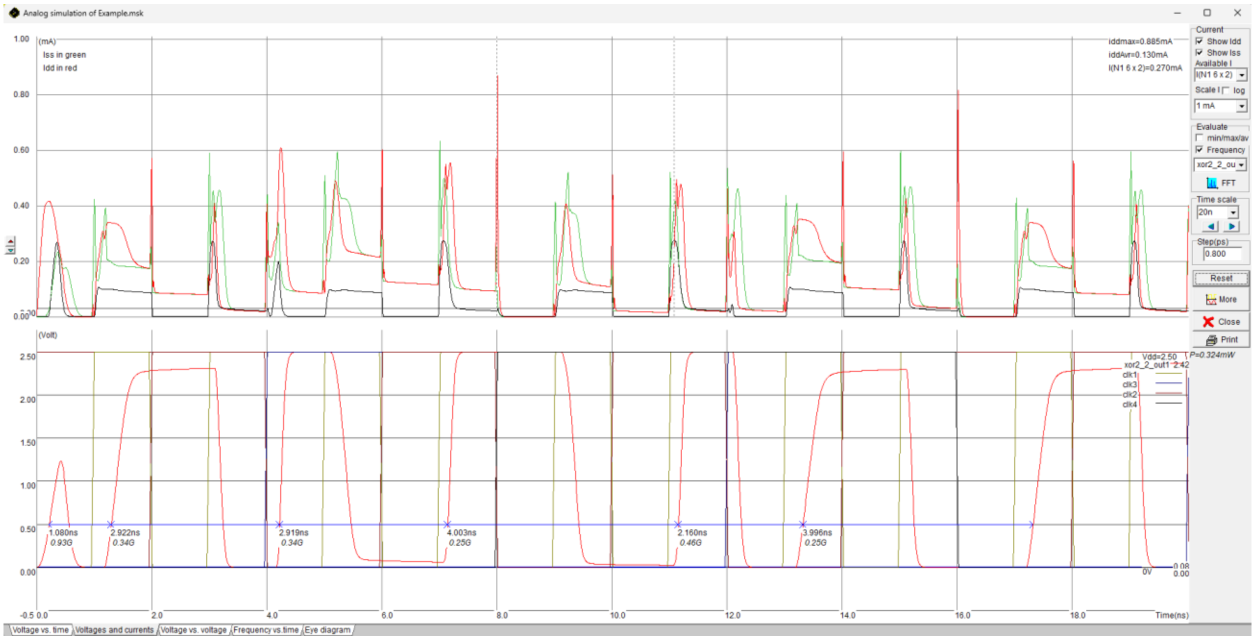


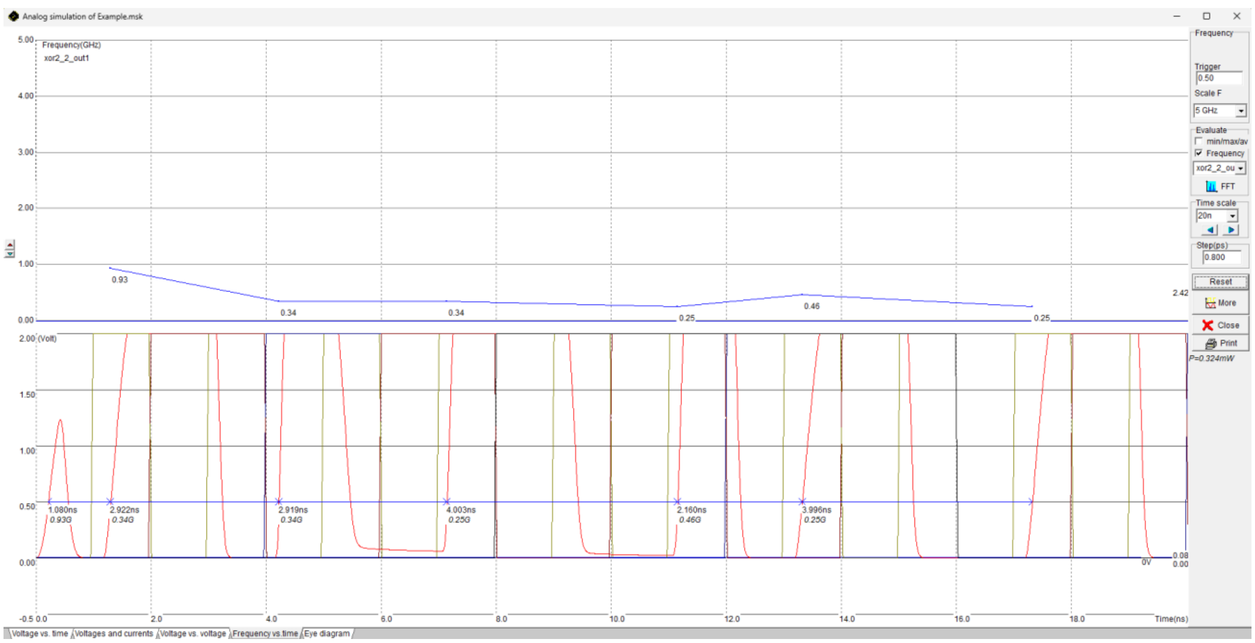


Microwind Version 3.1 - example
File View Edit Simulate Compile Analysis Help
5 lambda
0.625µm
xor2_1_w5
xor2_2_out1
xor2_3_w6
vdd+
vss-
clk3
clk4
out1
clk1
clk2
No design rule error. Congratulations (3.1% memory used)
No Error
CMOS 0.25µm - 6 Metal (2.50V)


Microwind Version 3.1 - Example.msk
File View Edit Simulate Compile Analysis Help
xor2_1_w5
xor2_2_out1
xor2_3_w6
vdd+
vss-
clk3
clk4
out1
0.02pF
clk1
clk2
No design rule error. Congratulations (3.0% memory used)
No Error
CMOS 0.25µm - 6 Metal (2.50V)


Analog simulation of Example.msk
clk1
clk2
clk3
clk4
xor2_2_out1
446ps
206ps
282ps
378ps
206ps
354ps
210ps
206ps
458ps
206ps
446ps
206ps
Time(ns)
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram





Reference

[jntuh vlsi lab - Research is Fun]

[Microsoft PowerPoint - MohantyVLSI5Microwind]