

**THE UNIVERSITY OF DANANG  
UNIVERSITY OF SCIENCE AND TECHNOLOGY  
Faculty of Advanced Science and Technology**



## **LABORATORY REPORT**

# **INTRODUCTION TO VERY LARGE SCALE INTEGRATION IC DESIGN**

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**Class** : 21ECE

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## Overview of Microwind and DSCH:

Microwind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator.

DSCH is software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation.

Silicon is for 3D display of the atomic structure of silicon, with emphasis on the silicon lattice, the dopants, and the silicon dioxide.

The Microwind software works is based on a lambda grid, not on a micro grid. Consequently, the same layout may be simulated in any CMOS technology. The value of lambda is half the minimum polysilicon gate length. Table A-xxx gives the correspondence between lambda and micron for all CMOS technologies available in the companion CD-ROM.

Technology file available in the CD-Rom	Minimum gate length	Value of lambda
Cmos12.rul	1.2 $\mu\text{m}$	0.6 $\mu\text{m}$
Cmos08.rul	0.7 $\mu\text{m}$	0.35 $\mu\text{m}$
Cmos06.rul	0.5 $\mu\text{m}$	0.25 $\mu\text{m}$
Cmos035.rul	0.4 $\mu\text{m}$	0.2 $\mu\text{m}$
Cmos025.rul	0.25 $\mu\text{m}$	0.125 $\mu\text{m}$
Cmos018.rul	0.2 $\mu\text{m}$	0.1 $\mu\text{m}$
Cmos012.rul	0.12 $\mu\text{m}$	0.06 $\mu\text{m}$
Cmos90n.rul	0.1 $\mu\text{m}$	0.05 $\mu\text{m}$
Cmos70n.rul	0.07 $\mu\text{m}$	0.035 $\mu\text{m}$
Cmos50n.rul	0.05 $\mu\text{m}$	0.025 $\mu\text{m}$

*Table 1-xxx: correspondence between technology and the value of lambda in  $\mu\text{m}$*

# Technical design

## DESIGN PROJECT

Design, lay out, and simulate a CMOS four-input XOR gate in the standard 0.25 micron CMOS process. You can choose any logic circuit style, and you are free to choose how many stages of logic to use: you could use one large logic gate or a combination of smaller logic gates. The supply voltage is set at 2.5 V! Your circuit must drive an external 20 fF load in addition to whatever internal parasitics are present in your circuit.

The primary design objective is to minimize the propagation delay of the worst-case transition for your circuit. The secondary objective is to minimize the area of the layout. At the very worst, your design must have a propagation delay of no more than 0.5 ns and occupy an area of no more than 500 square microns, but the faster and smaller your circuit, the better. Be aware that, when using dynamic logic, the precharge time should be made part of the delay.

The design will be graded on the magnitude of  $A \times t_p^2$ , the product of the area of your design and the square of the delay for the worst-case transition.

Name	4-input XOR gate
Process	0.25-micron
Supply voltage	2.5V
Propagation delay	< 0.5 ns
Area	< 500 square microns
External load	20 fF

# Physical design

## Design Reference Invertor

### Design Data — Transistor Model for Manual Analysis

Table 3.2 tabulates the obtained parameter values for the minimum-sized NMOS and a similarly sized PMOS device in our generic 0.25  $\mu\text{m}$  CMOS process. These values will be used as generic model-parameters in later chapters.

**Table 3.2** Parameters for manual model of generic 0.25  $\mu\text{m}$  CMOS process (minimum length device).

	$V_{T0}$ (V)	$\gamma$ ( $\text{V}^{0.5}$ )	$V_{DSAT}$ (V)	$k'$ ( $\text{A/V}^2$ )	$\lambda$ ( $\text{V}^{-1}$ )
NMOS	0.43	0.4	0.63	$115 \times 10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30 \times 10^{-6}$	-0.1

From Eq. (5.2), we can derive the required ratio of PMOS versus NMOS transistor sizes such that the switching threshold is set to a desired value  $V_M$ . When using this expression, please make sure that the assumption that both devices are velocity-saturated still holds for the chosen operation point.

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn} (V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp} (V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)} \quad (5.5)$$

So we have  $\frac{(W/L)_p}{(W/L)_n} = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1} \times \frac{2.50 - 0.43 - \frac{0.63}{2}}{2.50 - 0.4 - \frac{1.0}{2}} = 3.5 \approx 3$

### Design Data — MOS Transistor Capacitances

Table 3.5 summarizes the parameters needed to estimate the parasitic capacitances of the MOS transistors in our generic 0.25  $\mu\text{m}$  CMOS process.

**Table 3.5** Capacitance parameters of NMOS and PMOS transistors in 0.25  $\mu\text{m}$  CMOS process.

	$C_{ox}$ (fF/ $\mu\text{m}^2$ )	$C_O$ (fF/ $\mu\text{m}$ )	$C_j$ (fF/ $\mu\text{m}^2$ )	$m_j$	$\phi_b$ (V)	$C_{jsw}$ (fF/ $\mu\text{m}$ )	$m_{jsw}$	$\phi_{bsw}$ (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

**Table 5.2** Components of  $C_L$  (for high-to-low and low-to-high transitions).

Capacitor	Expression	Value (fF) (H→L)	Value (fF) (L→H)
$C_{gd1}$	$2\ CGD0_n\ W_n$	0.23	0.23
$C_{gd2}$	$2\ CGD0_p\ W_p$	0.61	0.61
$C_{db1}$	$K_{eqn}\ AD_n\ CJ + K_{eqsw_n}\ PD_n\ CJSW$	0.66	0.90
$C_{db2}$	$K_{eqp}\ AD_p\ CJ + K_{eqsw_p}\ PD_p\ CJSW$	1.5	1.15
$C_{g3}$	$(CGD0_n + CGSO_n)\ W_n + C_{ox}\ W_n\ L_n$	0.76	0.76
$C_{g4}$	$(CGD0_p + CGSO_p)\ W_p + C_{ox}\ W_p\ L_p$	2.28	2.28
$C_w$	From Extraction	0.12	0.12
$C_L$	$\Sigma$	6.1	6.0

$$C_{int} = C_{gd1} + C_{gd2} + C_{db1} + C_{db2}$$

$$C_{int} = 2CGD0_n W_n + 2CGD0_p W_p + C_{db1} + C_{db2}$$

$$C_{int} = 2 \times 0.31 \times W_n + 2 \times 0.27 \times W_p + 0.66 + 1.5$$

$$C_{int} = 0.62 \times W_n + 0.54 \times W_p + 2.16$$

$$\text{We have } C_L = C_{int} + C_{ext}$$

From the requirement with external load is equal 20 fF, so

$$C_L = C_{int} + C_{ext} = (0.62 \times W_n + 0.54 \times W_p + 2.16) + 20$$

### Design Data — Equivalent Resistance Model

Table 3.3 enumerates the equivalent resistances obtained by simulation of our generic 0.25  $\mu\text{m}$  CMOS process. These values will come in handy when analyzing the performance of CMOS gates in later chapters.

**Table 3.3** Equivalent resistance  $R_{eq}$  ( $W/L=1$ ) of NMOS and PMOS transistors in 0.25  $\mu\text{m}$  CMOS process (with  $L = L_{min}$ ). For larger devices, divide  $R_{eq}$  by  $W/L$ .

$V_{DD}$ (V)	1	1.5	2	2.5
NMOS (k $\Omega$ )	35	19	15	13
PMOS (k $\Omega$ )	115	55	38	31

And with the generic 0.25  $\mu\text{m}$  CMOS process, we have the  $R_{eq}$  for NMOS and PMOS at  $V_{DD}=2.5\text{ V}$  is:

$$R_{eqn} = 13\text{ k}\Omega \text{ and } R_{eqp} = 31\text{ k}\Omega$$

And with the requirement for propagation delay is  $< 0.5\text{ ns}$ .

$$t_p = 0.69C_L \left( \frac{R_{eqn} + R_{eqp}}{2} \right) < 0.5\text{ ns}$$

$$t_p = 0.69[0.62 W_n + 0.54 W_p + 2.16 + 20] \left( \frac{R_{eqn} + R_{eqp}}{2} \right) < 0.5\text{ ns}$$

$$\Rightarrow 0.69[0.62 \times W_n + 0.54 \times W_p + 2.16 + 20] \left( \frac{13\text{ k}\Omega + 31\text{ k}\Omega}{2} \right) < 0.5\text{ ns}$$

$$\Rightarrow 0.62 \times W_n (fF) + 0.54 \times W_p (fF) < 10.8 (fF)$$

$$\text{And we have } \frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} \approx 3 \text{ or } W_p = 3W_n$$

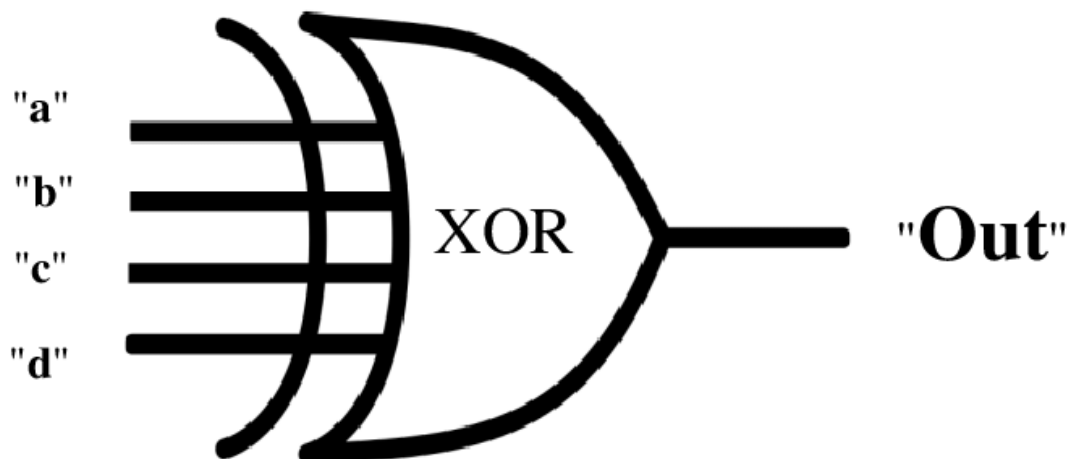
$$\Rightarrow W_p < 17.277\text{ }\mu\text{m} \text{ and } W_n < 5.750\text{ }\mu\text{m} \text{ and } W_p = 3W_n$$

$$\text{Choose } W_p = 2.500\text{ }\mu\text{m} \text{ and } W_n = 0.750\text{ }\mu\text{m}$$

## Logic design

The XOR (Exclusive OR) gate is a digital logic gate that outputs true or high only when the two binary bit inputs to it are unequal. In other words, it outputs a 1 when the number of 1's inputs is odd, making it essential for arithmetic functions in computers and other digital systems.

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0





$$A \oplus B \oplus C \oplus D$$

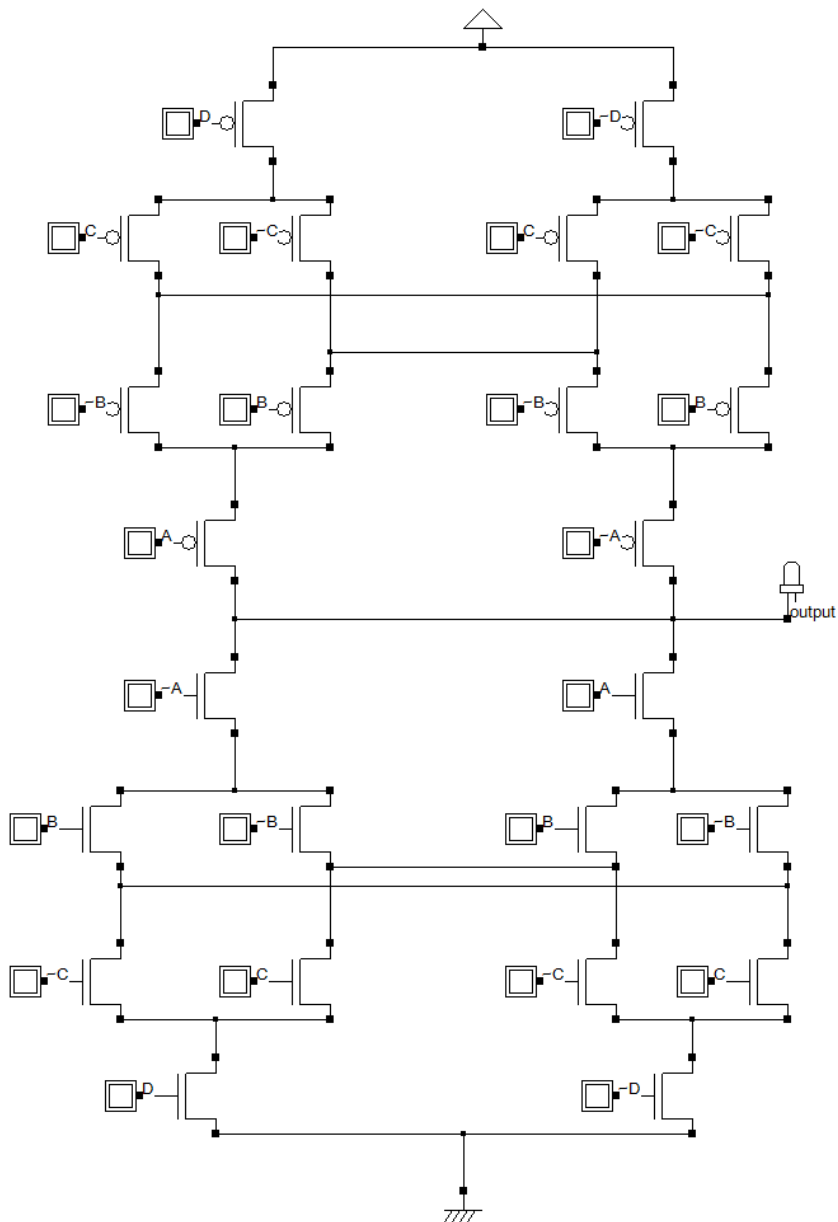
$$= (A \oplus (B \oplus C \oplus D))$$

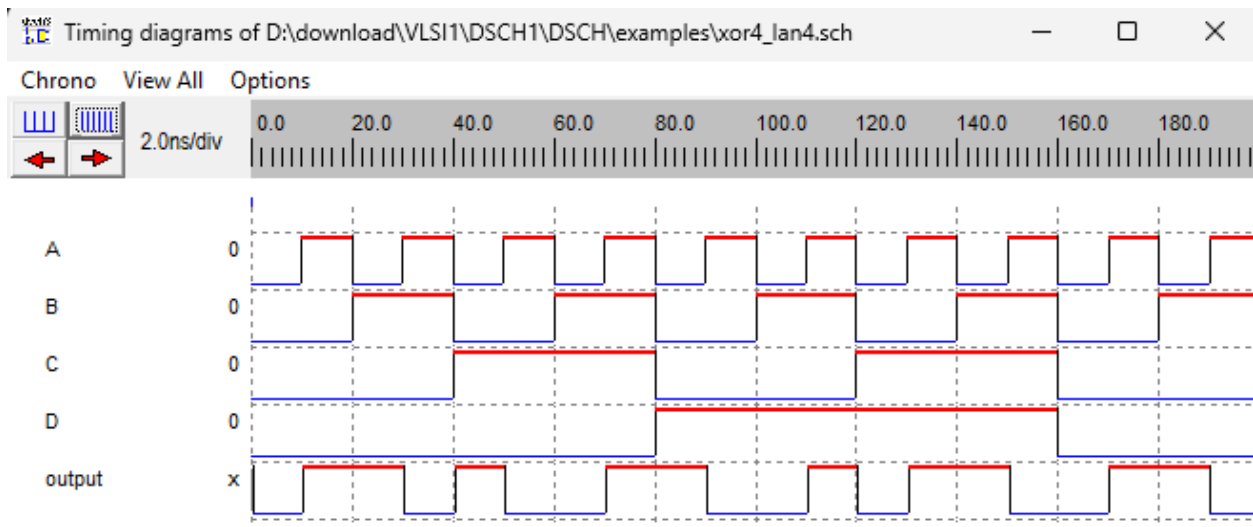
$$= A \cdot (B \oplus C \oplus D)' + A' \cdot (B \oplus C \oplus D)$$

$$= A \cdot (((B \cdot C') + (B' \cdot C)) \cdot D') + (((B \cdot C') + (B' \cdot C))' \cdot D) + A' \cdot (((B \cdot C') + (B' \cdot C)) \cdot D') + (((B \cdot C') + (B' \cdot C))' \cdot D)$$

$$= A \cdot [(B' + C) \cdot (B + C') + D] \cdot [(B' + C) \cdot (B + C') + D'] + A' \cdot (((B \cdot C') + (B' \cdot C)) \cdot D') + (((B \cdot C') + (B' \cdot C))' \cdot D)$$

#### Four-input XOR Gate Schematic





## Layout design

Size | Labels | Routing

Mos size ( $\mu\text{m}$ )

Width P 2.500

Length P 0.250

Width N 0.750

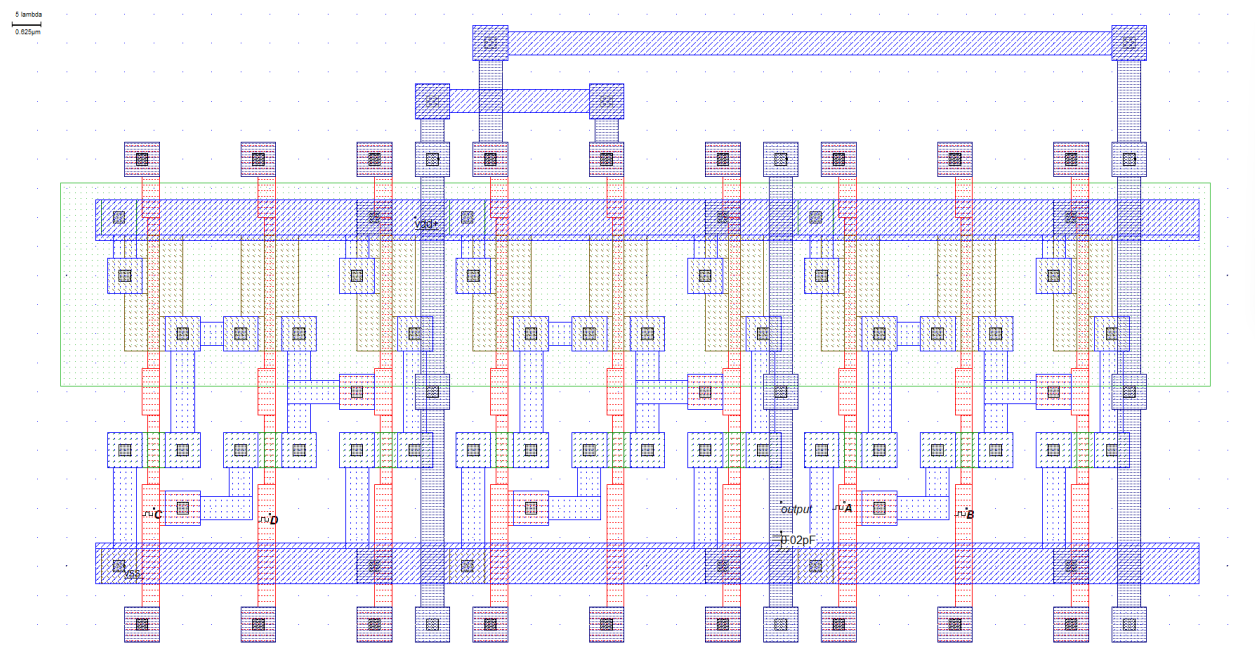
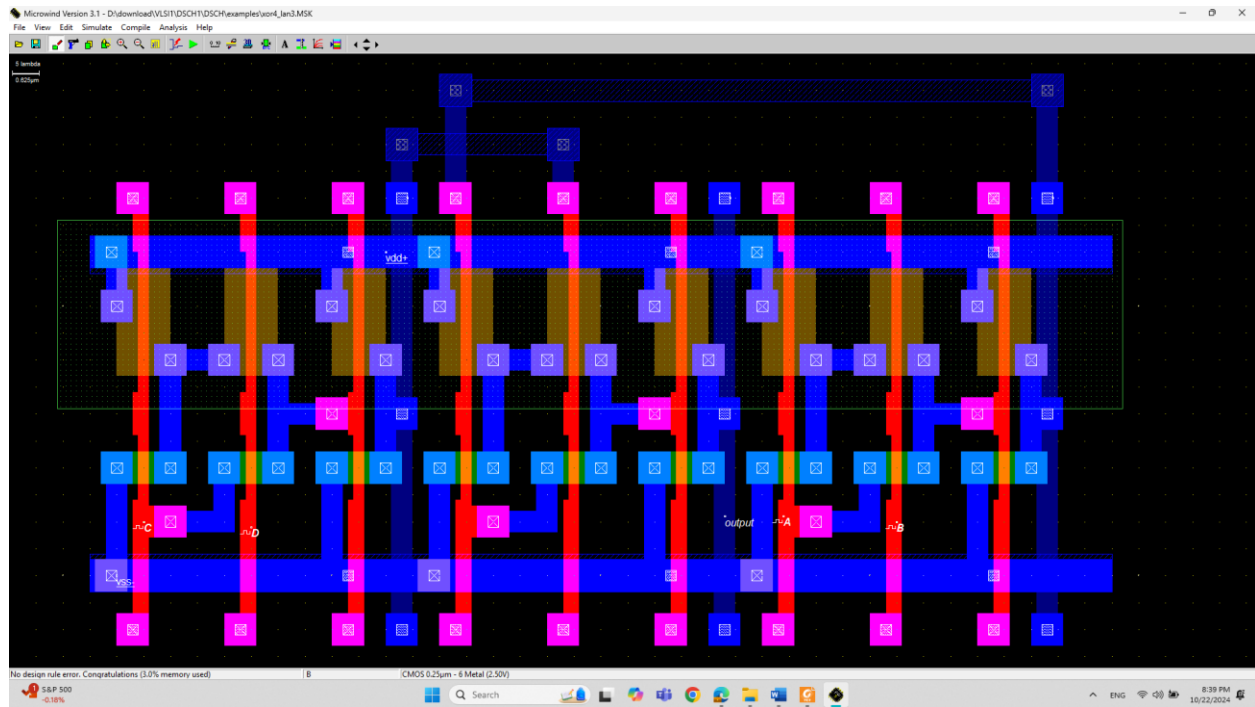
Length N 0.250

Virtual R,L,C Para...

Capa between node and ground

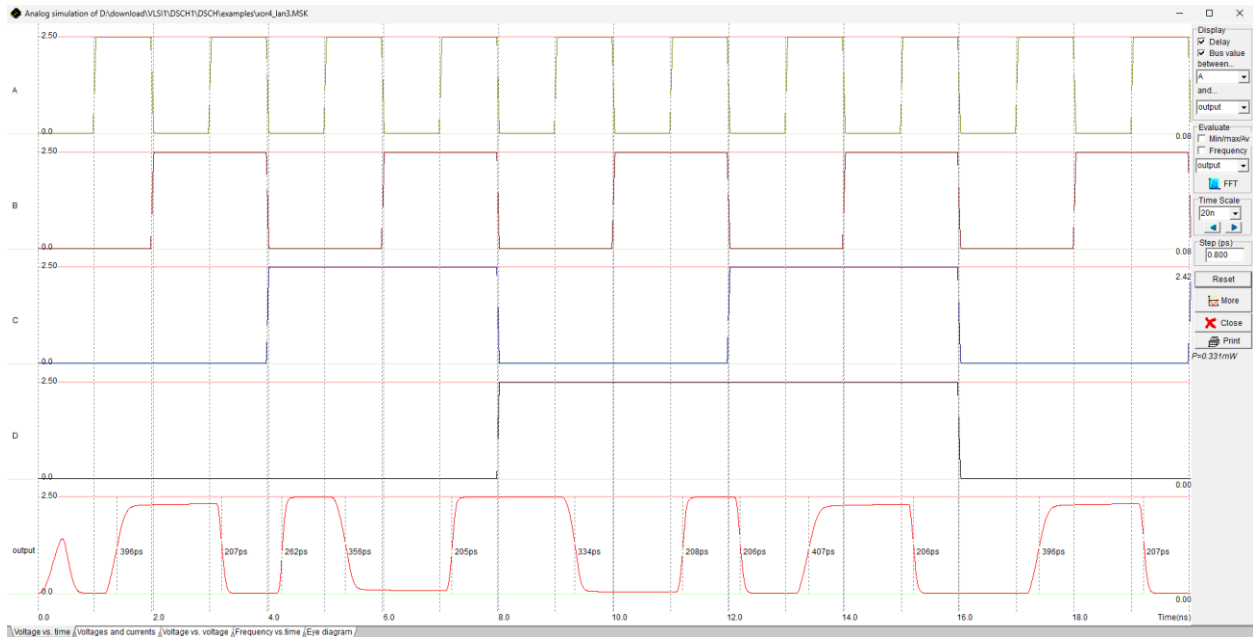
Capacitance value (pF): 0.02

OK Cancel



# Result

**Timing:** Confirm that the propagation delay meets the 0.5 ns specification.



**Area:** Validate that the area is within acceptable limits ( $24.8 \times 13.3 = 330$  square microns)

Properties of D:\download\VLSI1\DSCH1\DSCH\examples\xor4\_1an3...

General | Miscellaneous

Technology and Design rules  
CMOS 0.25 $\mu$ m - 6 Metal(D:\download\cmos025.rul)

Set as default technology | Detail of design rules

Structure

boxes :	428/300000		0.1% full
text :	10/2000		0.5% full
main array:	152 x 44		3.0% full

Layout Size

Width: 24.8 $\mu$ m (198 lambda)  
Height: 13.3 $\mu$ m (106 lambda)  
Surf: 327.9 $\mu$ m<sup>2</sup> (0.0 mm<sup>2</sup>)

Electrical Properties

electrical nodes :	16/3000
nMOS devices :	9/2000
pMOS devices :	9/2000

OK | Extract

# Reference

[Microsoft Word - Book appendixA e.doc](#)

[jntuh vlsi lab - Research is Fun](#)

[Microsoft PowerPoint - MohantyVLSI5Microwind](#)