
EE476

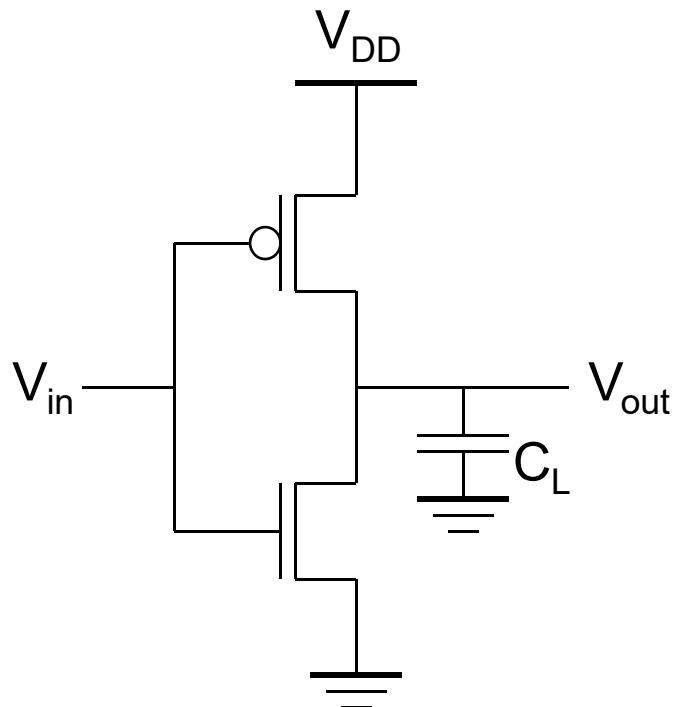
VLSI Digital Circuits

Lecture 02: IC Manufacturing

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: CMOS Inverter

Advantages:



- Full rail-to-rail swing \Rightarrow high noise margins
- Low output impedance
- High input impedance
- No direct path steady-state between power and ground \Rightarrow no static power dissipation
- Propagation delay is a function of load capacitance and on resistance of transistors

Growing the Silicon Ingot

- ✓ Base material: a single-crystalline, lightly doped wafer between 4 and 12 inches and a thickness of, at most, 1 mm
 - ✓ obtained from cutting a single-crystal ingot into thin slices.
 - ✓ Starting wafer of p- type around 2×10^{21} impurities/m³.
- Lightly doped

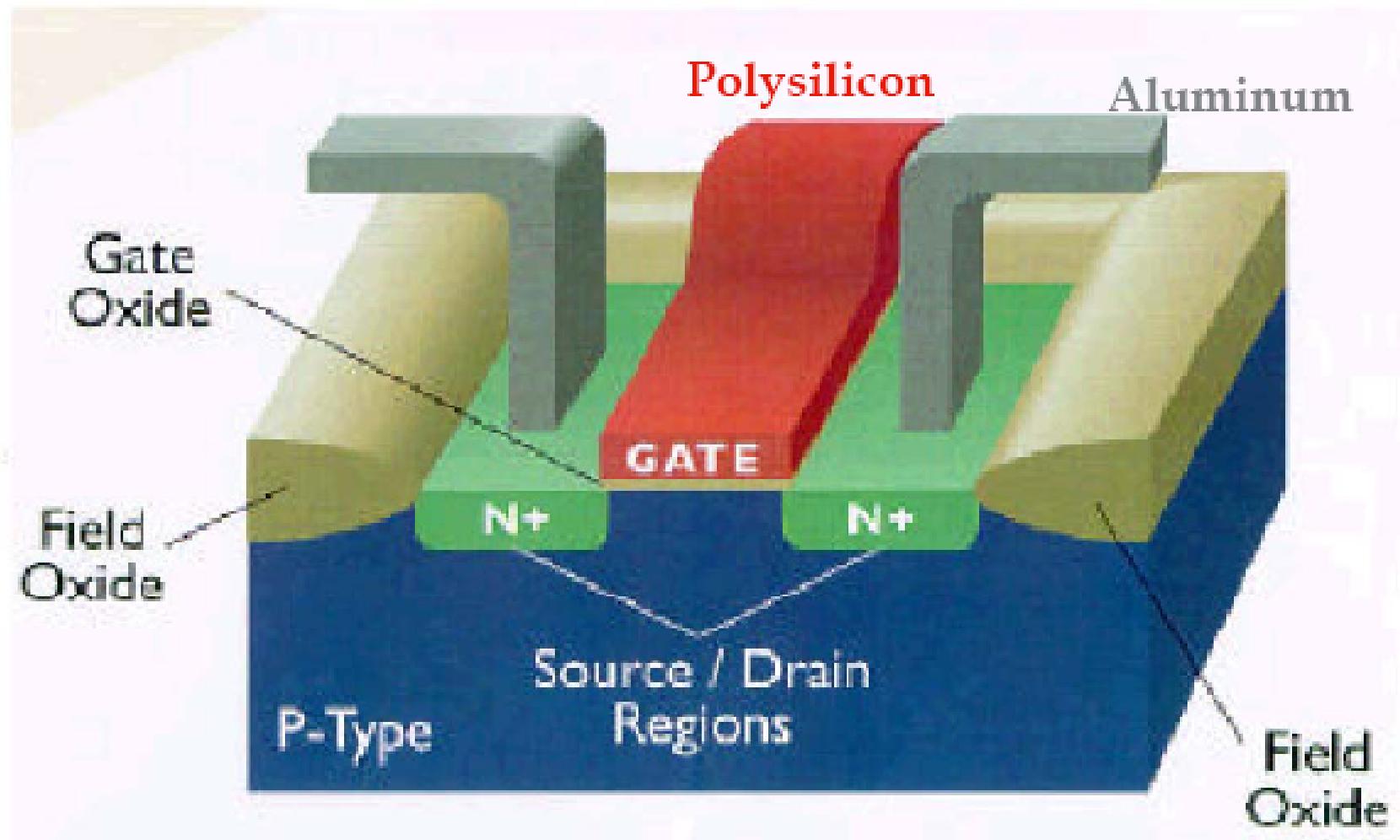


The substrate serves both as the physical medium and as part of the electrical circuit itself

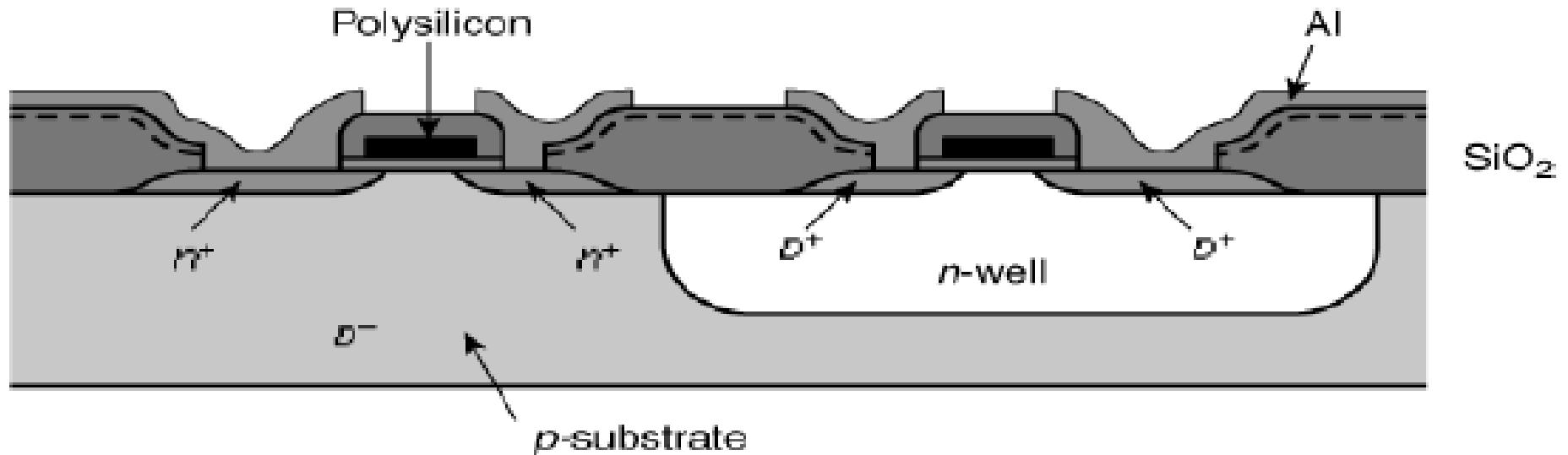
From Smithsonian, 2000

Irwin&Vijay, PSU, 2002

The MOS Transistor



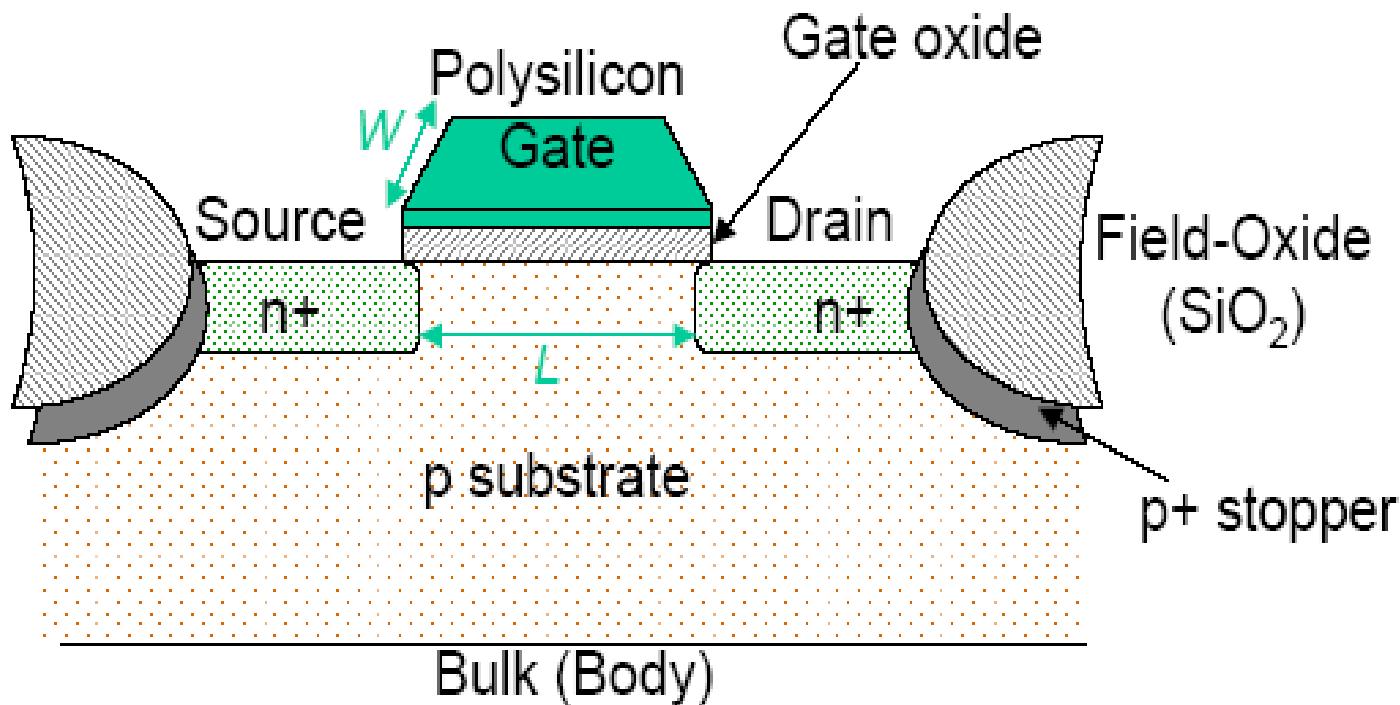
Cross section of an *n*-well CMOS process.



The CMOS process requires that both *n-channel (NMOS)* and *p-channel (PMOS)* transistors be built in the same silicon material

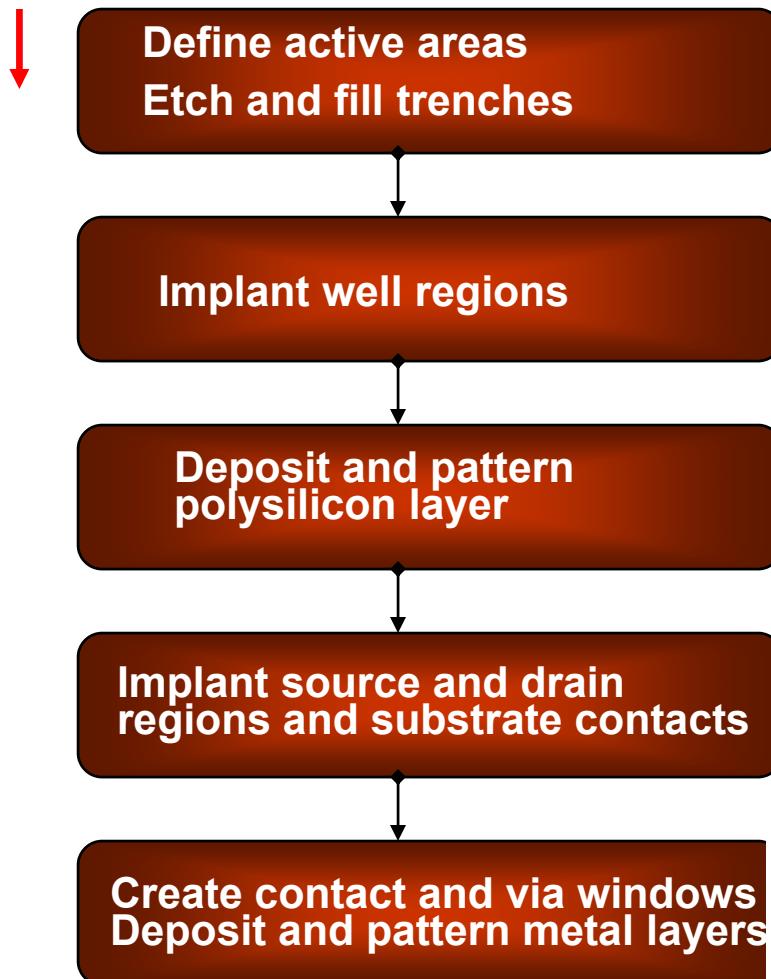
The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration N_D - electrons are the majority carriers



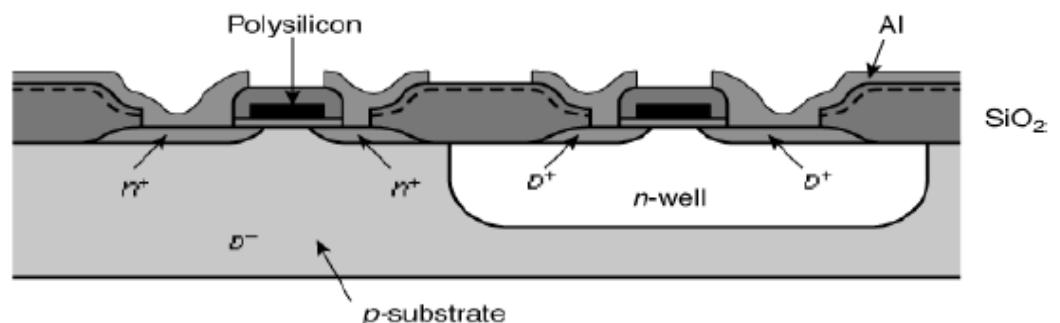
p areas have been doped with acceptor ions (boron) of concentration N_A - holes are the majority carriers

CMOS Process at a Glance

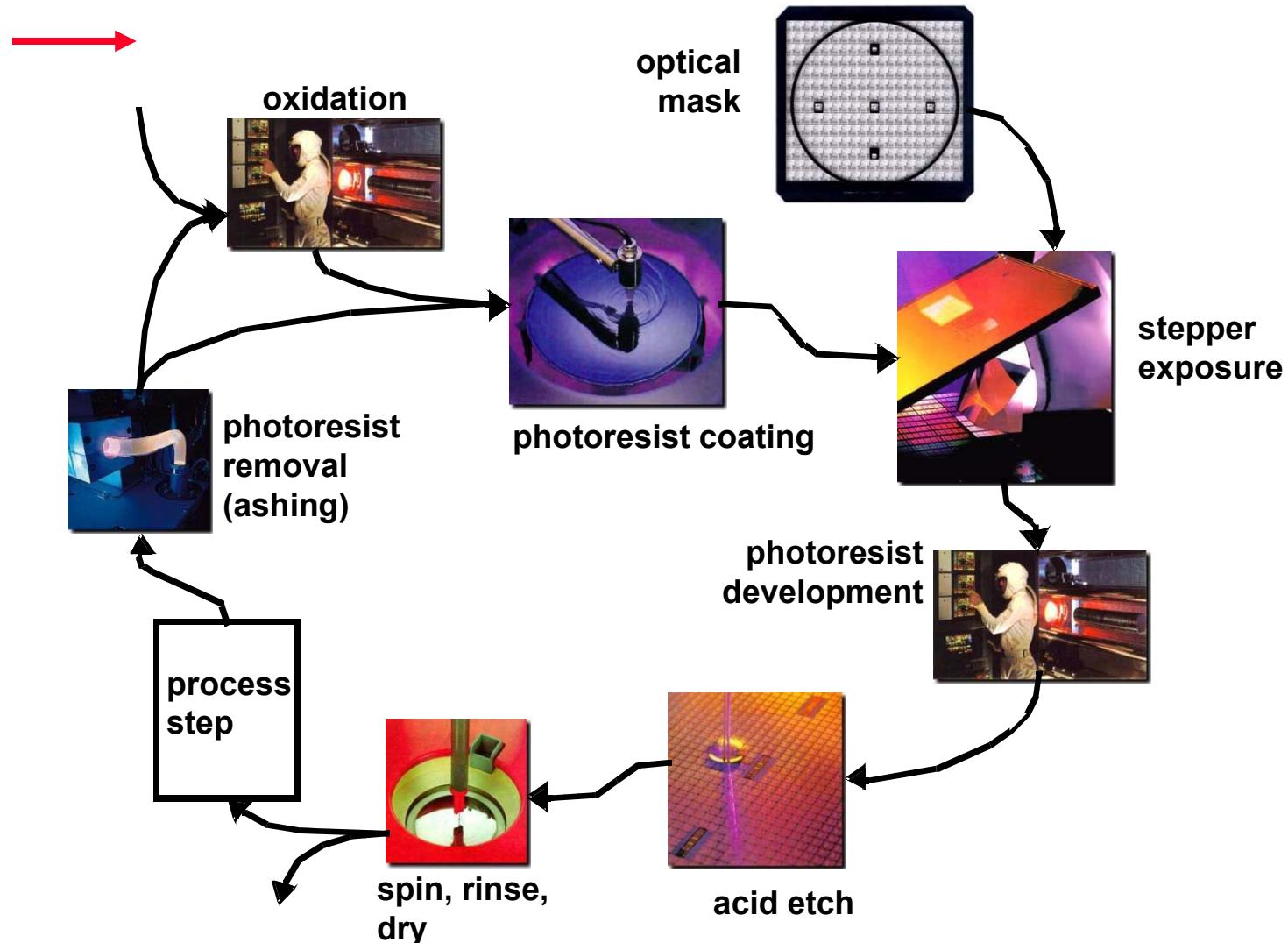


- ❑ One full **photolithography** sequence per layer (mask)
- ❑ Built (roughly) from the bottom up
 - 5 metal 2
 - 4 metal 1
 - 3 **polysilicon**
 - 2 **source and drain diffusions**
 - 1 **tubs (aka wells, active areas)**

The processing step can be any of a wide range of tasks including *oxidation, etching, metal and polysilicon deposition, and ion implantation*. The technique to accomplish this selective masking, called **photolithography**

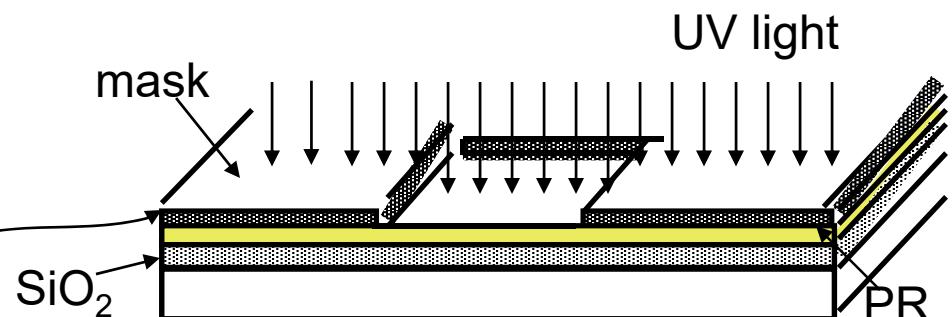


Photolithographic Process

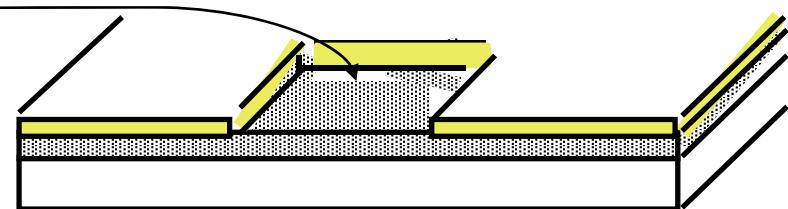


Patterning - Photolithography

1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure

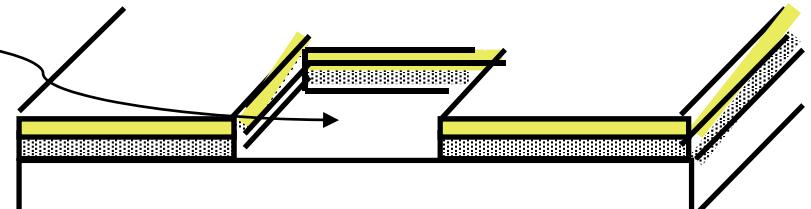


4. Photoresist development and bake

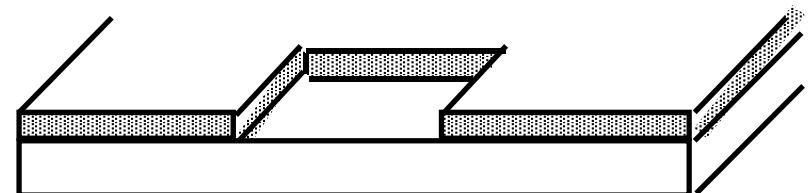


5. Acid etching
- Unexposed (negative PR)
- Exposed (positive PR)

6. Spin, rinse, and dry



7. Processing step
- Ion implantation
- Plasma etching
- Metal deposition

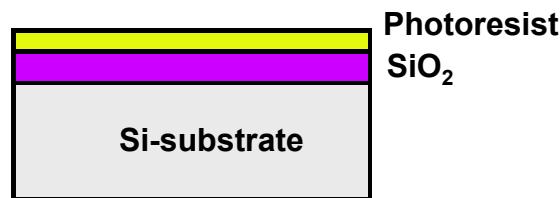


8. Photoresist removal (ashing)

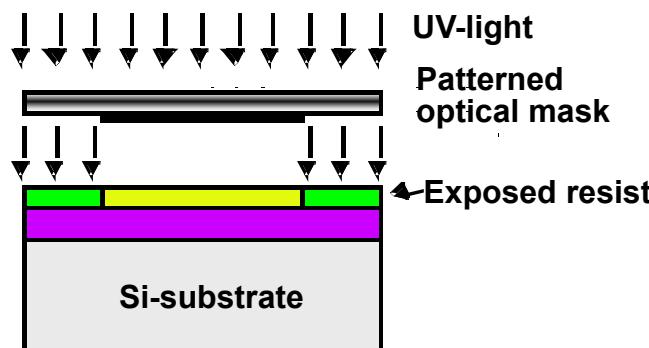
Example of Patterning of SiO₂



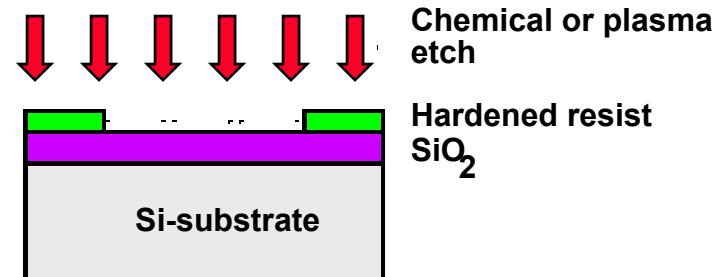
Silicon base material



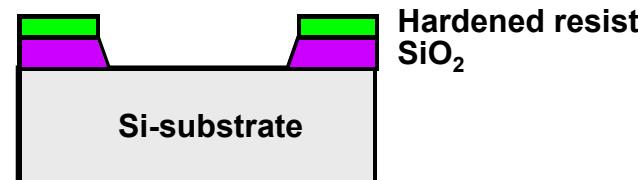
1&2. After oxidation and deposition of negative photoresist



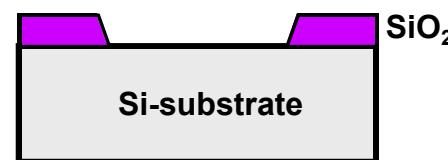
3. Stepper exposure



4. After development and etching of resist, chemical or plasma etch of SiO₂



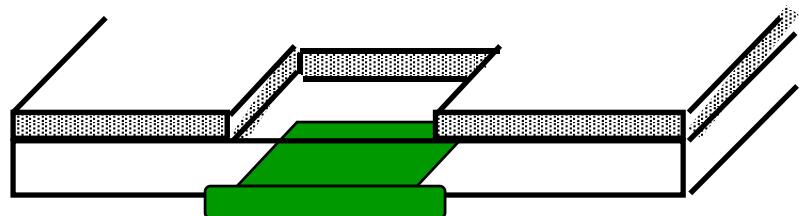
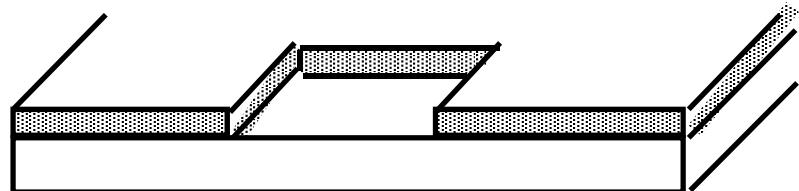
5. After etching



8. Final result after removal of resist

Diffusion and Ion Implantation

1. Area to be doped is exposed
(photolithography)
2. Diffusion or Ion implantation



Needed for well, source and drain regions, doping of polysilicon, adjustment of thresholds

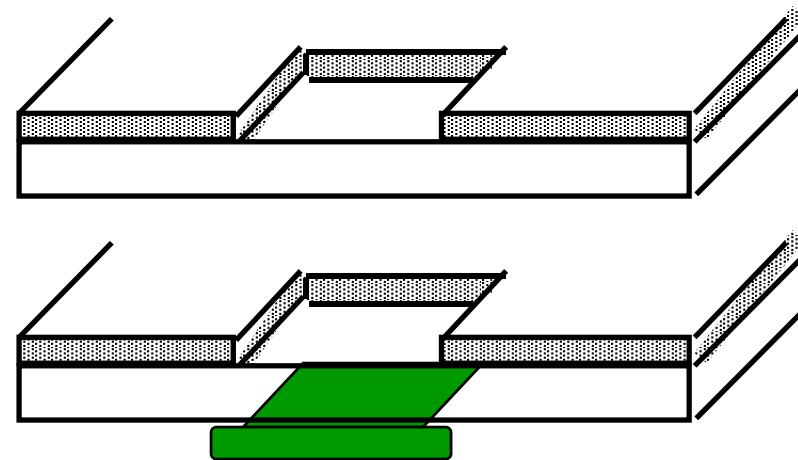
Diffusion – wafer placed in quartz tube embedded in a furnace (900 to 1100 °C).

- Gas containing dopant is introduced in the tub. Dopants diffused into the exposed surface both vertically and horizontally.
- Final dopant concentration is highest at surface and decreases in a gaussian profile deeper in the material

Diffusion and Ion Implantation

Ion implantation

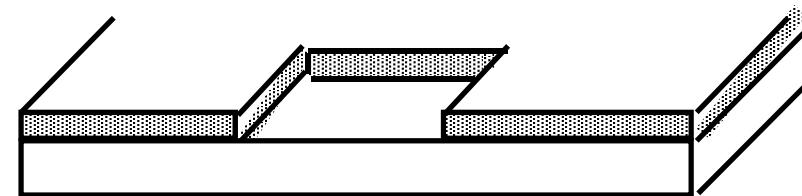
- sweeping a beam of purified ions over the surface
- acceleration determines how deep ions will penetrate



- the **beam current** and **exposure time** determine **dosage**.
- ion implantation has largely **displaced diffusion**.
- a **side effect** of causing **lattice damage** to substrate
- so usually follow with an **annealing step** (wafer heated to 1000C for 15 to 30 minutes and allowed to cool slowly). Heating vibrates atoms and allows the bonds to reform.

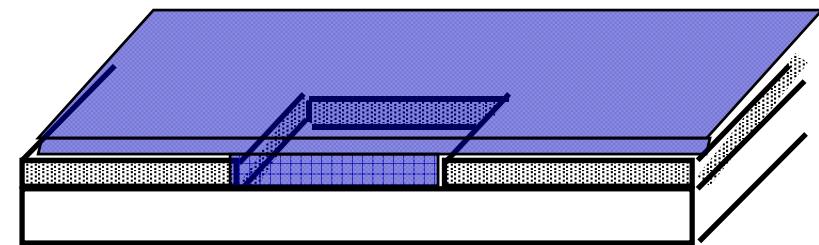
Deposition and Etching

1. Pattern masking
(photolithography)



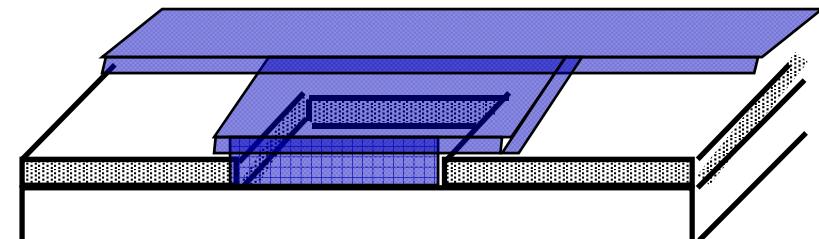
2. Deposit material over entire wafer

CVD (Si_3N_4)
chemical deposition
(polysilicon)
sputtering (Al)



3. Etch away unwanted material

wet etching
dry (plasma) etching



Needed for insulating SiO_2 , silicon nitride (sacrificial buffer), polysilicon, metal interconnect

Planarization: Polishing the Wafers

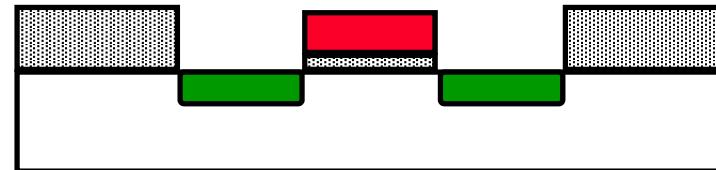
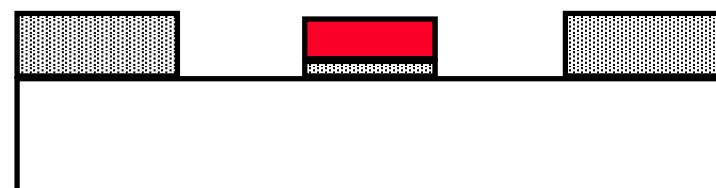
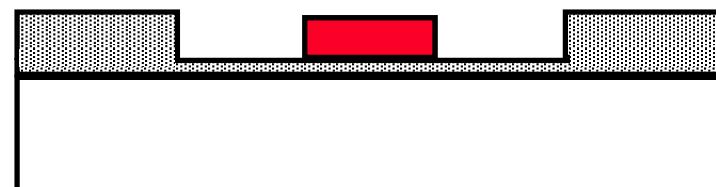
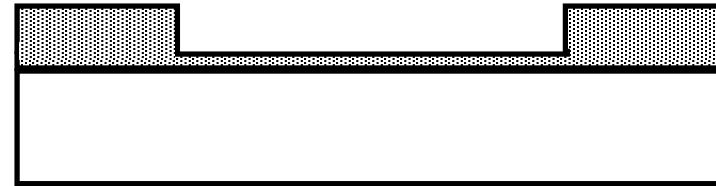


- + Essential to keep the surface of the wafer approximately flat between processing steps.
- uses a slurry compound – a liquid carrier with a suspended abrasive component such as aluminum oxide or silica – to microscopically plane a device layer and to **reduce step heights**.

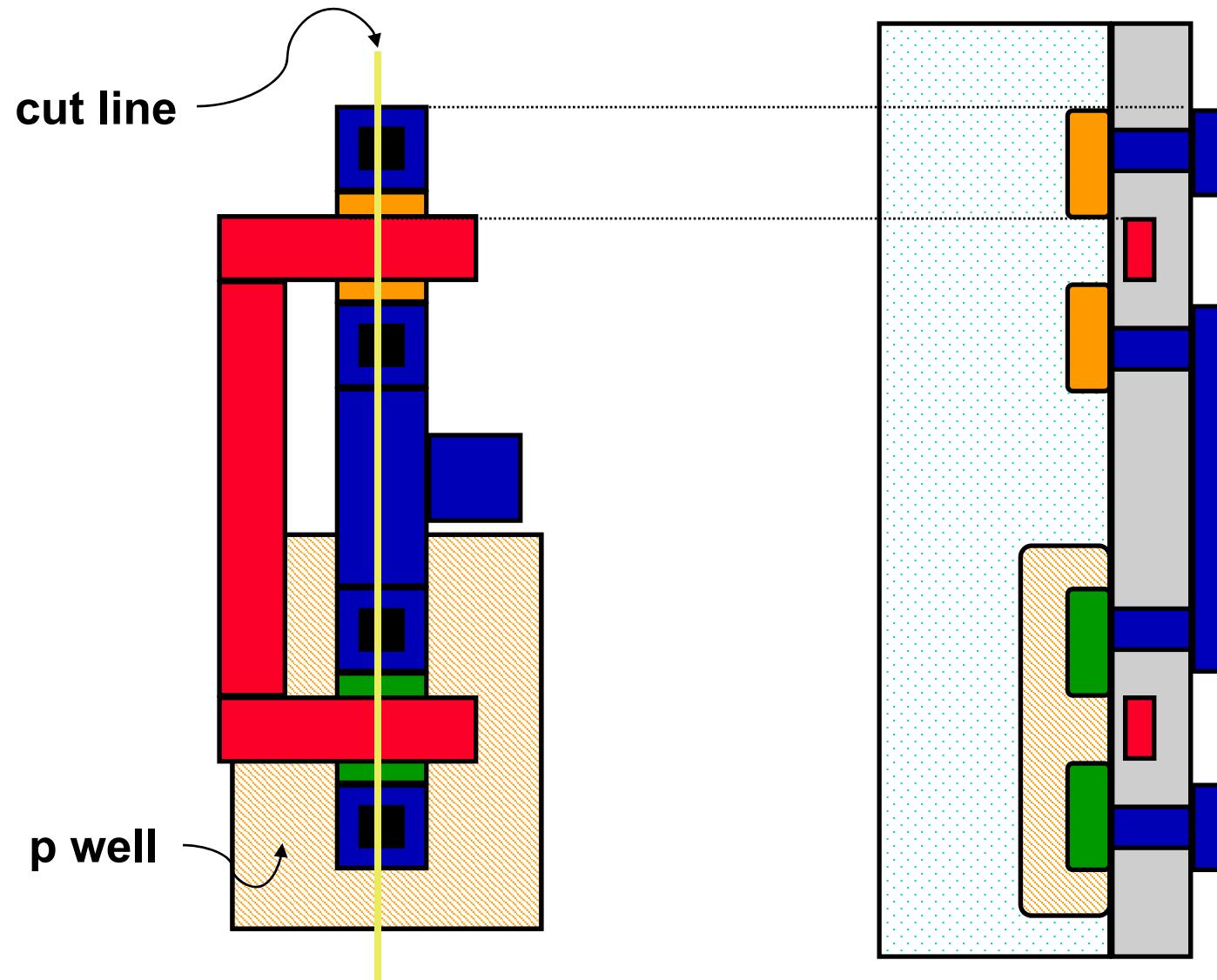
Self-Aligned Gates

1. Create thin oxide in the “active” regions, thick elsewhere
2. Deposit polysilicon
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)
4. Implant dopant

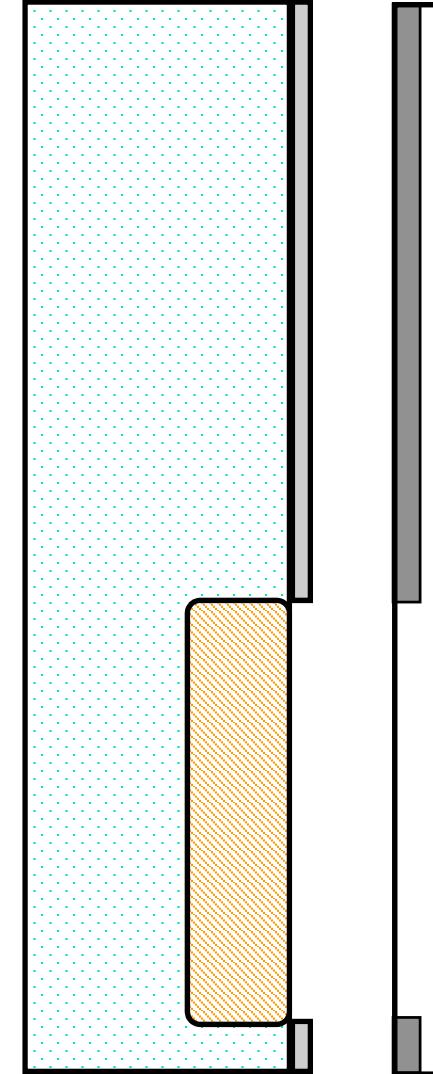
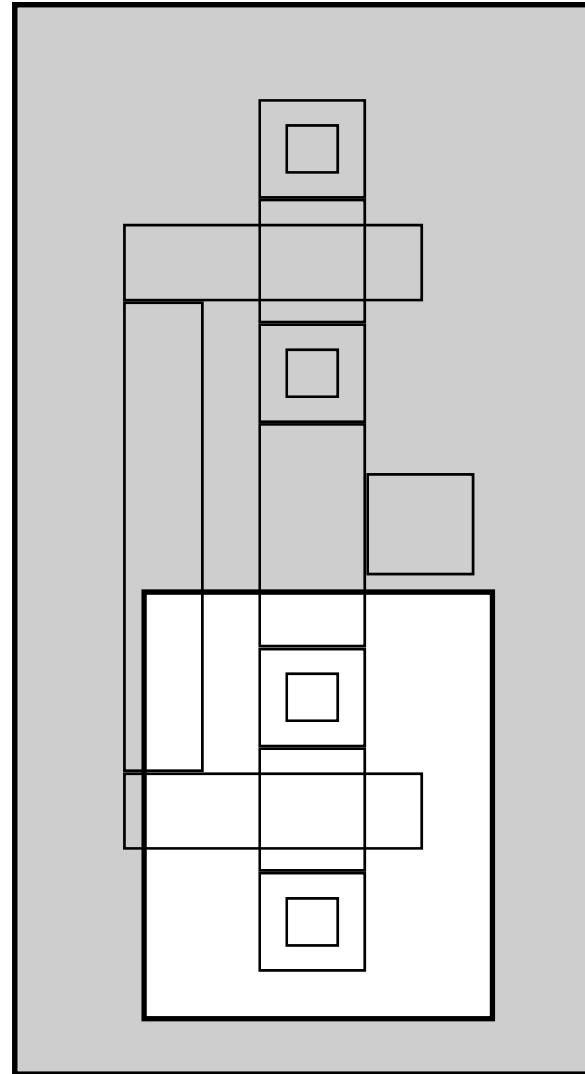
defining the precise location of the channel region and the locations of the source and drain regions



Simplified CMOS Inverter Process

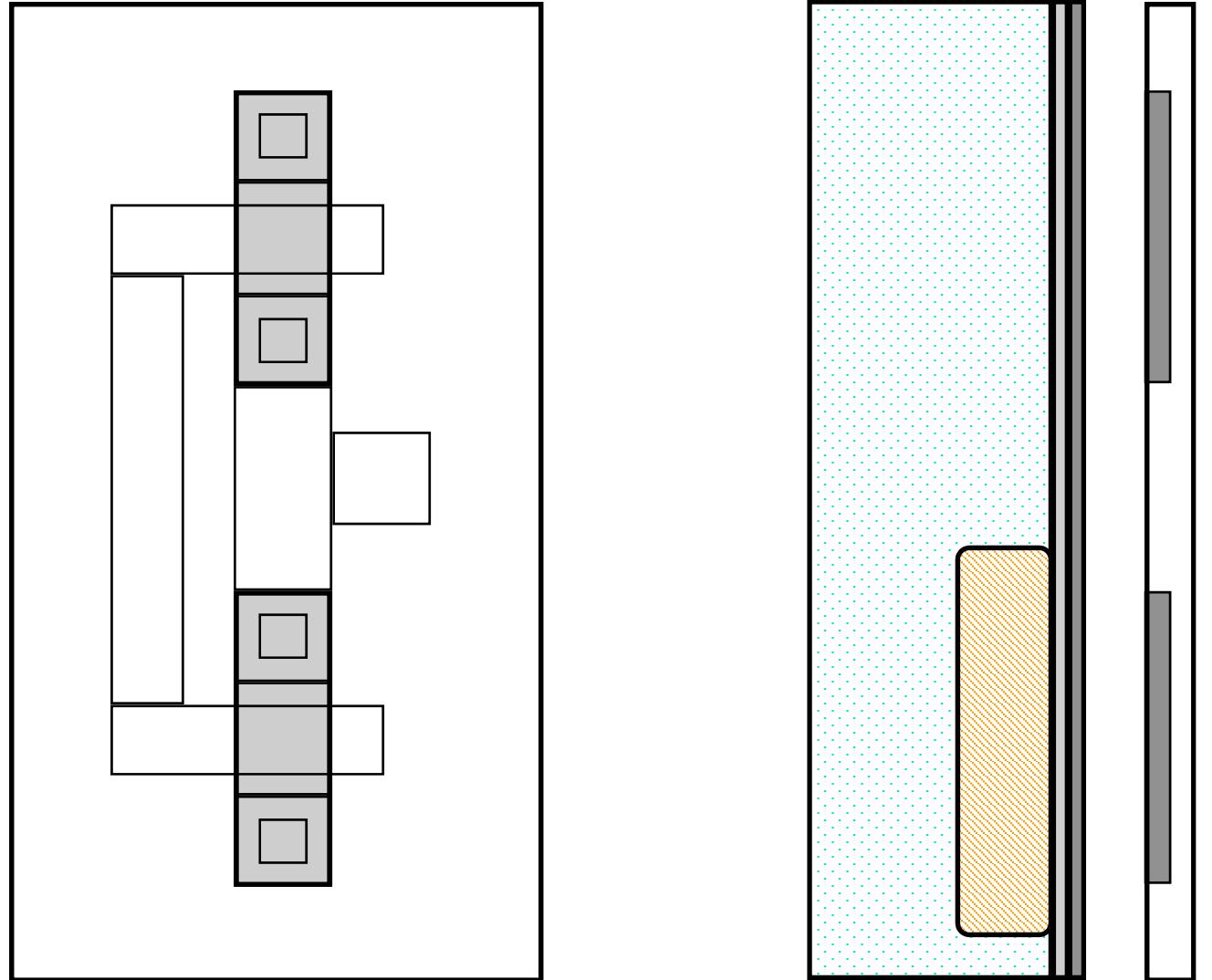


P-Well Mask



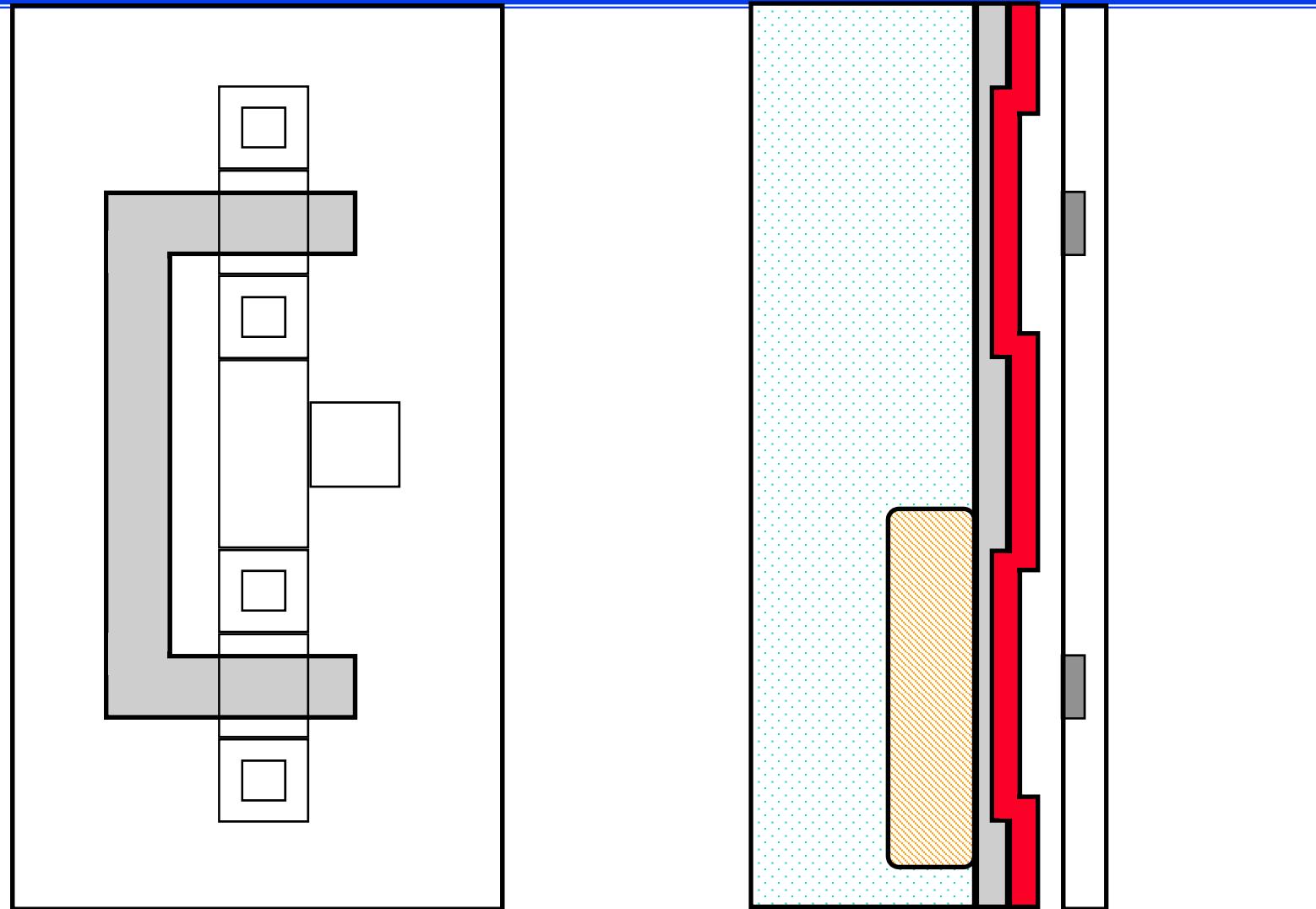
After p-well use implants to adjust VTn

Active Mask



Grown thick oxide. Then use active mask to create thin oxide layers over the active areas – where we are going to place the transistors (**source, gate, and drain areas**)

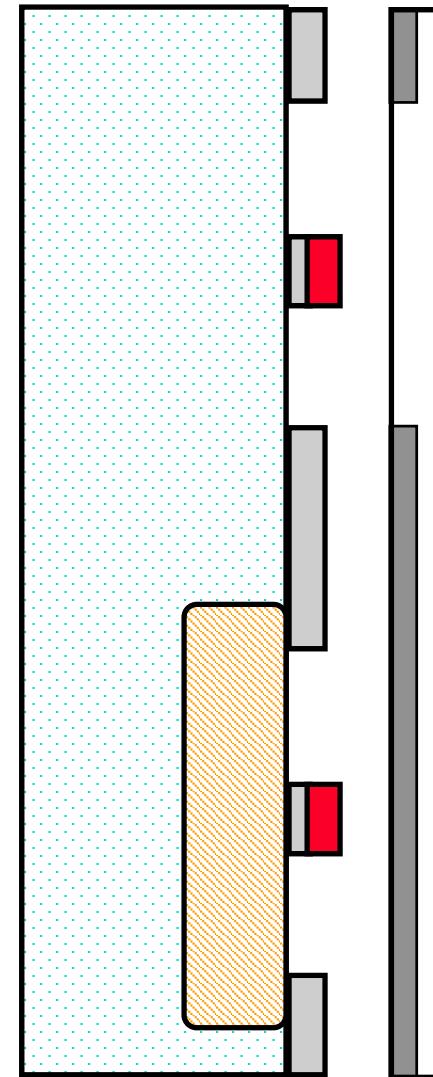
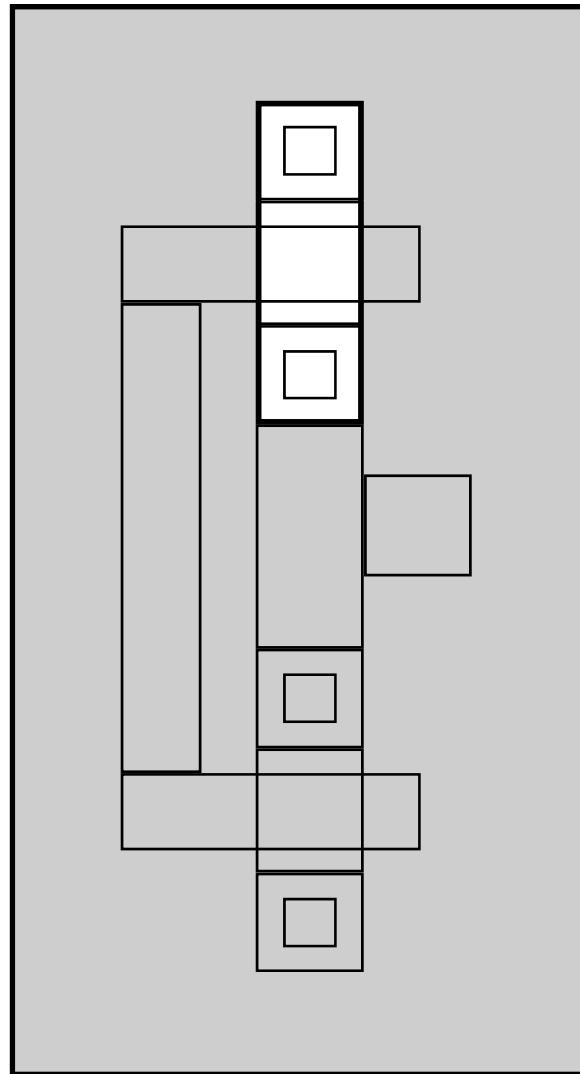
Poly Mask



First used chemical deposition to deposit polysilicon on wafer.

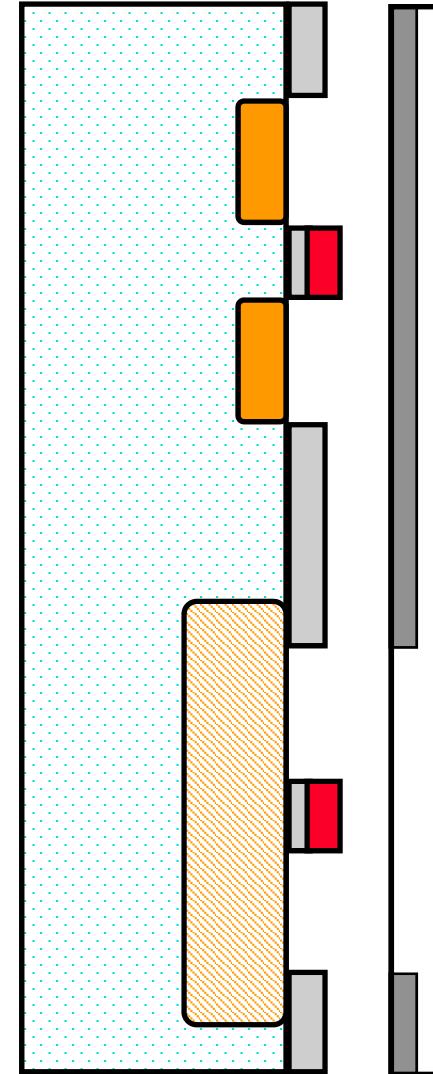
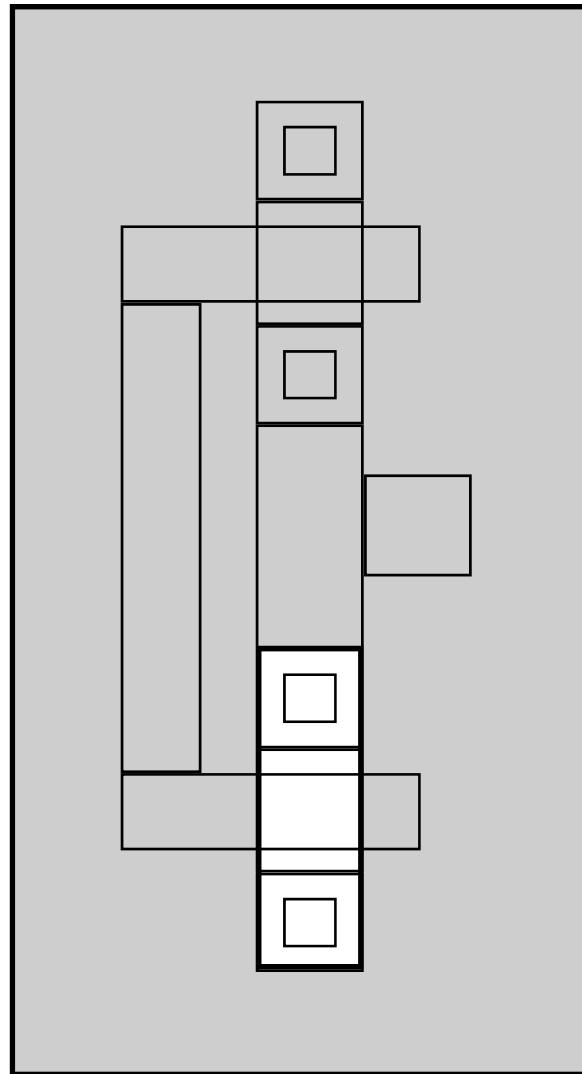
0.25 micron technology -> 6.5 to 5.5 microns thick

P+ Select Mask



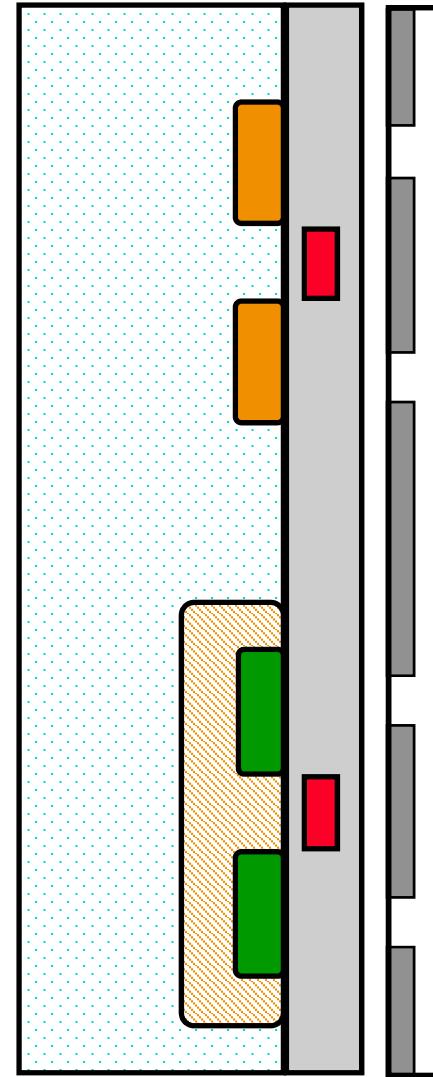
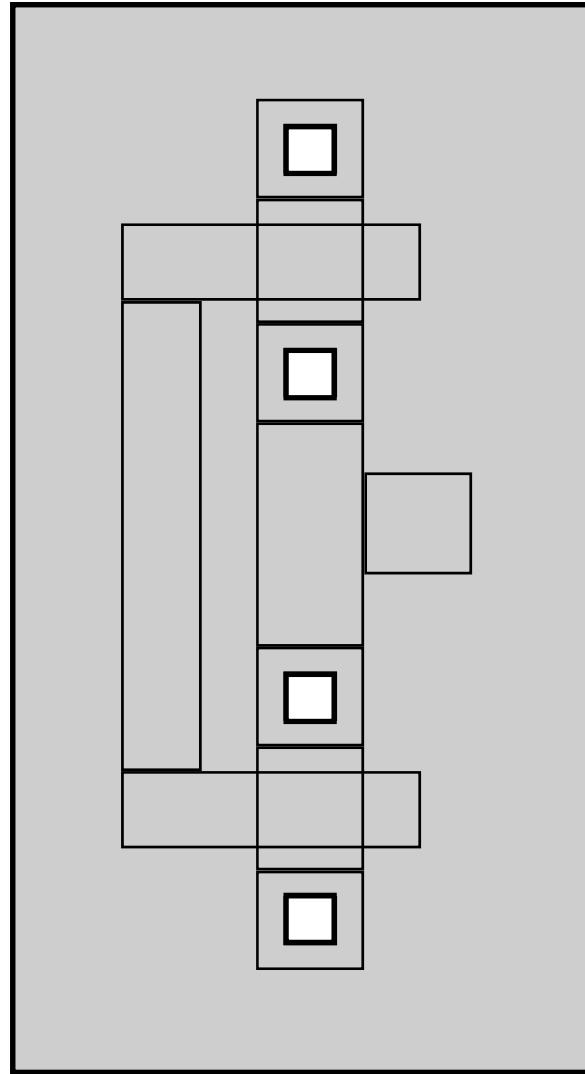
Followed by diffusion (ion implant) to build pfets source and drain areas

N+ Select Mask



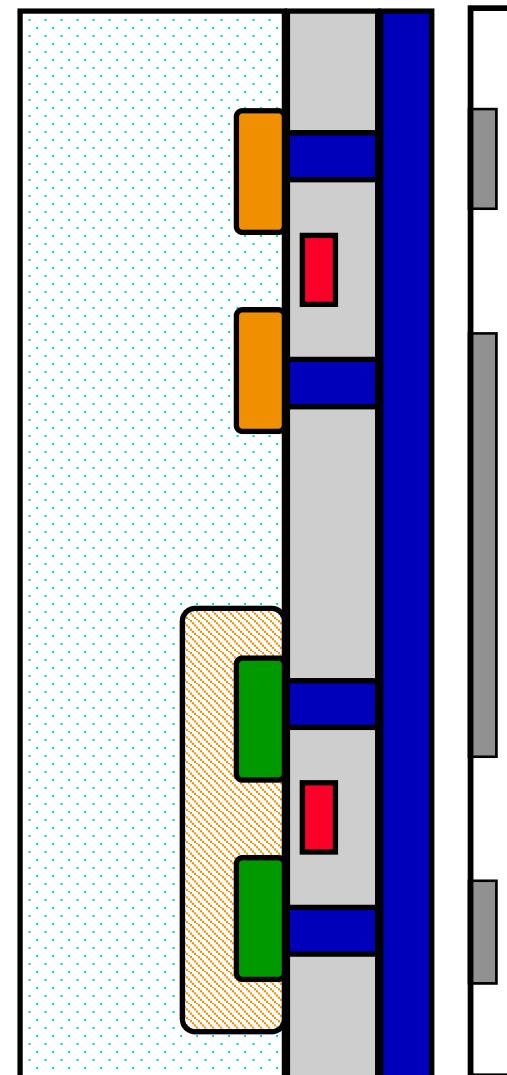
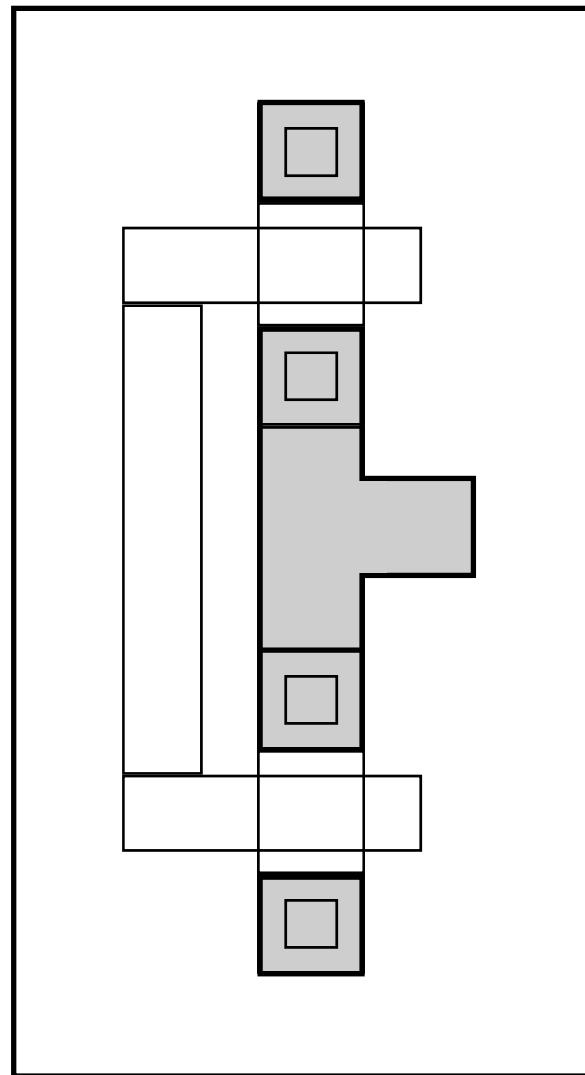
Followed by diffusion (ion implant) to build nfets source and drain areas

Contact Mask



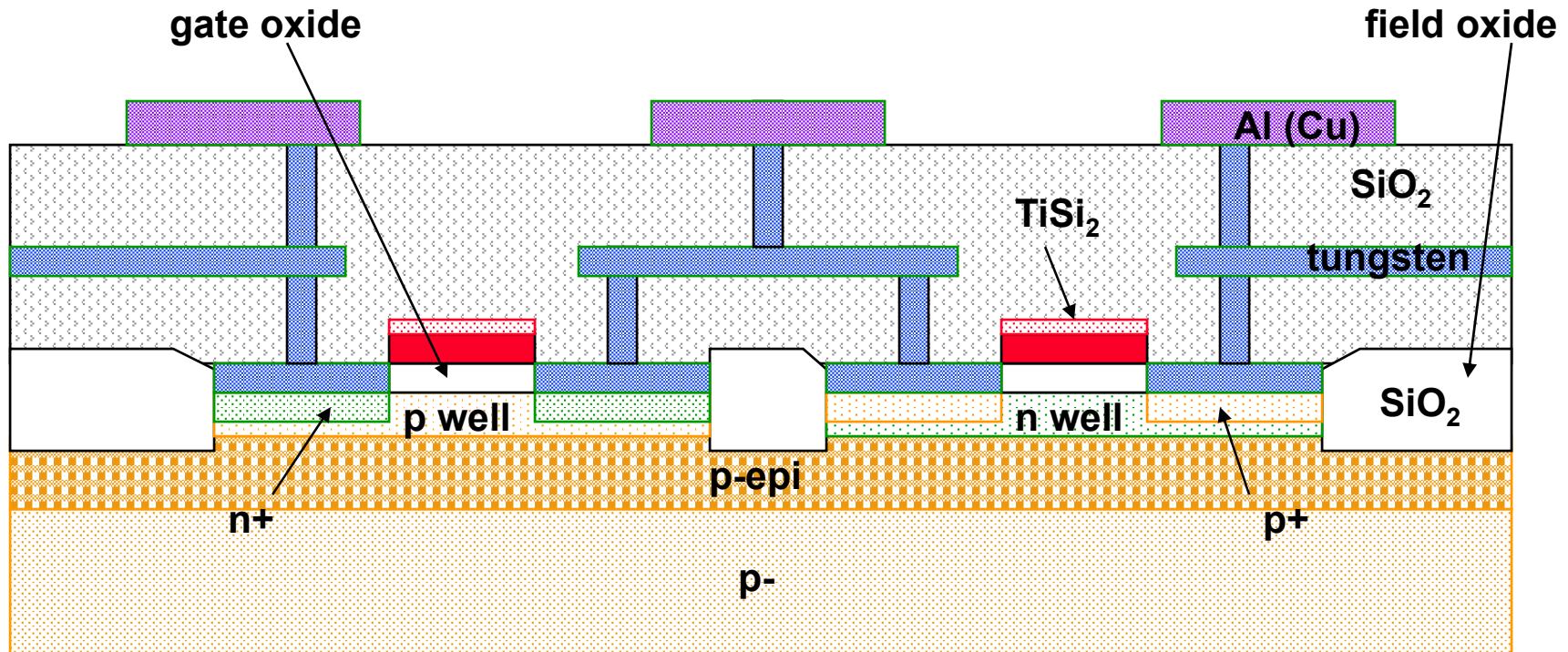
After deposition of SiO_2 insulator, then contact holes are etched (in this case to make contacts to source and drain regions)

Metal Mask



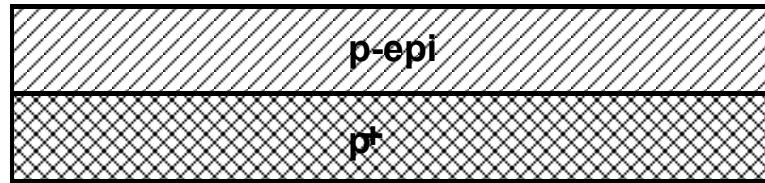
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS

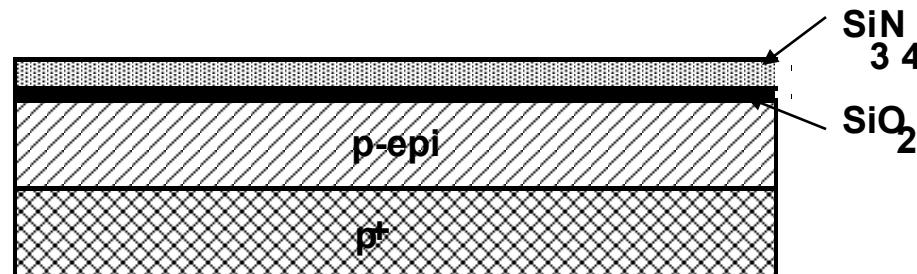


dual-well approach uses both n- and p- wells grown on top of a epitaxial layer(using trench isolation areas of SiO₂)

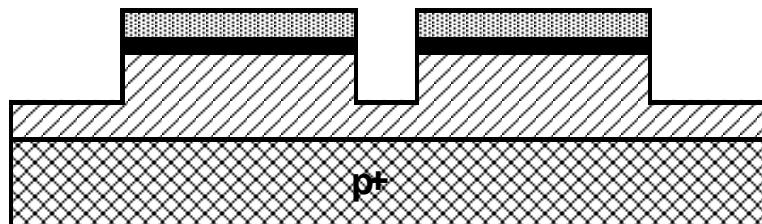
Modern CMOS Process Walk-Through



Base material: p⁺ substrate
with p-epi layer

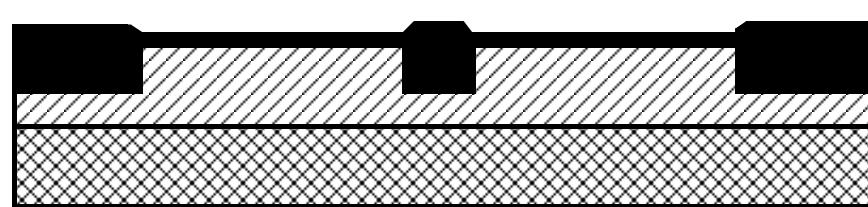


After **deposition** of gate-oxide and sacrificial nitride (acts as a buffer layer)

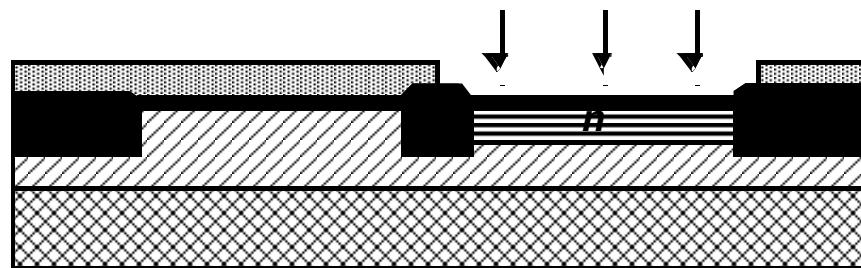


After **plasma etch** of **insulating trenches** using the **inverse of the active area mask**

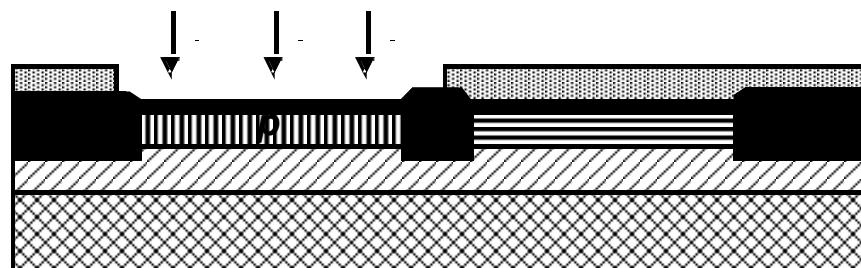
CMOS Process Walk-Through, con't



After trench filling,
CMP planarization,
and removal of
sacrificial nitride



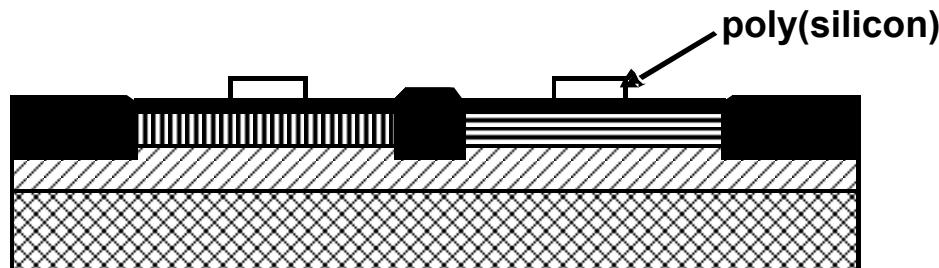
After n-well and V_{Tp}
adjust implants



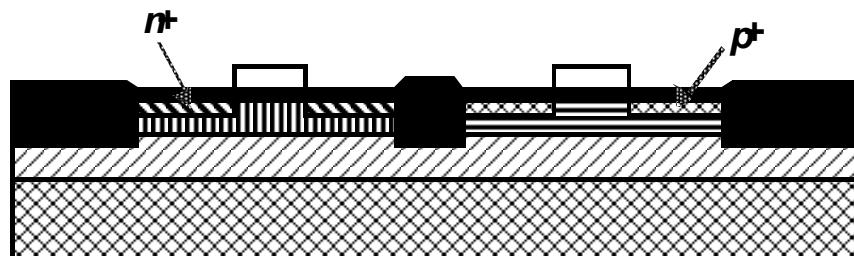
After p-well and V_{Tn}
adjust implants

CMP: chemical-mechanical planarization

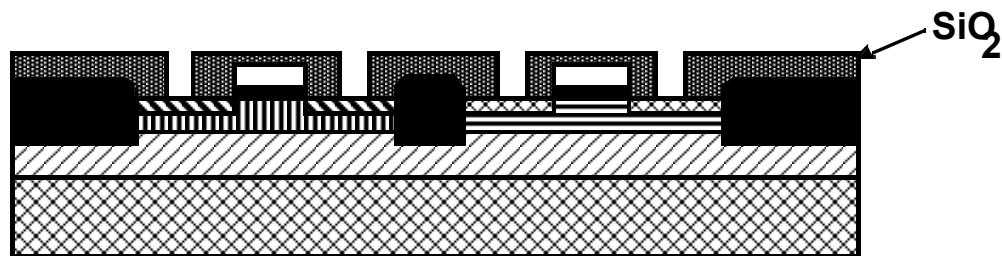
CMOS Process Walk-Through, con't



After **polysilicon deposition** and etch

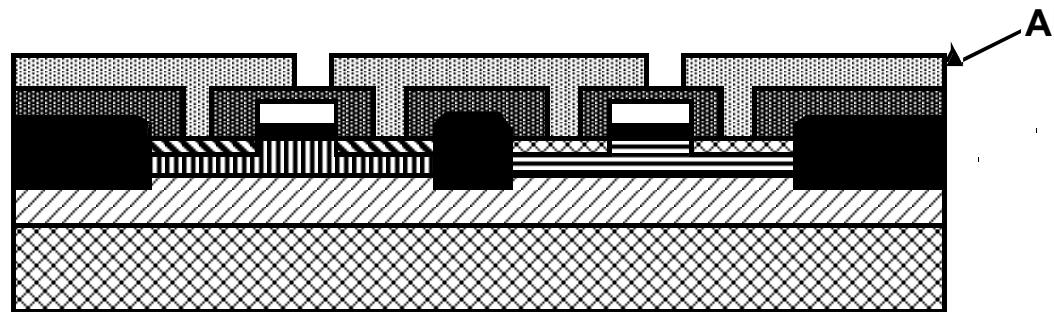


After n^+ source/drain and p^+ source/drain implants. These steps also dope the polysilicon.

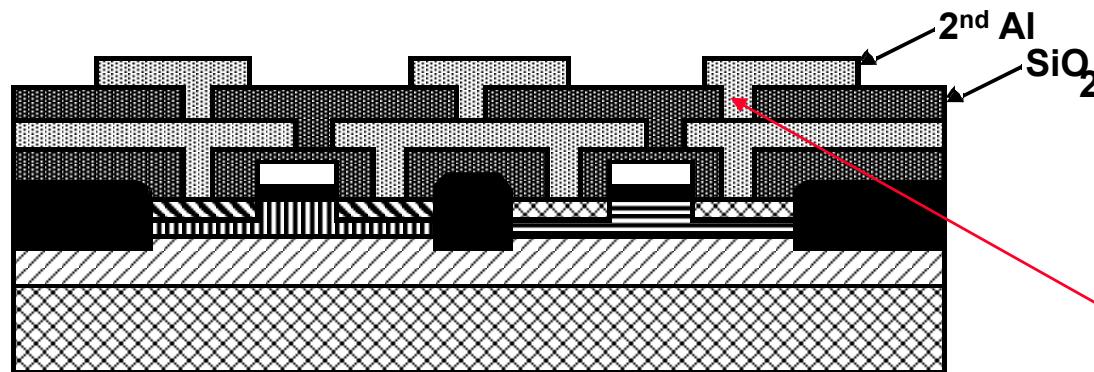


After deposition of SiO_2 insulator and **contact hole etch**

CMOS Process Walk-Through, con't

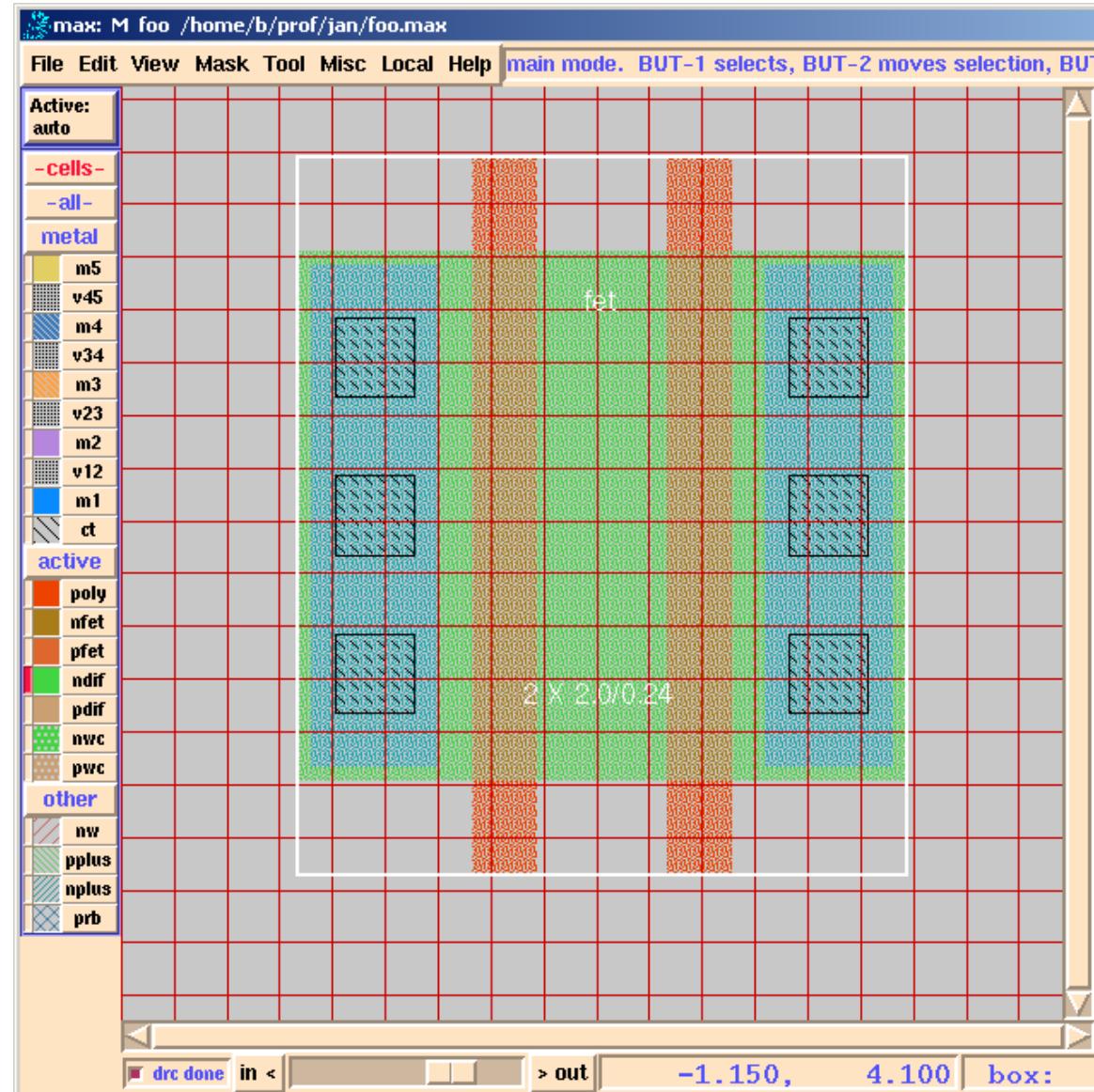


After deposition and patterning of first Al layer.

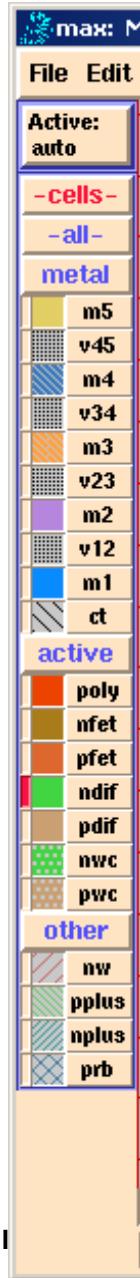


After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Layout Editor: max Design Frame



max Layer Representation



- ❑ Metals (five) and vias/contacts between the interconnect levels
 - Note that **m5** connects only to **m4**, **m4** only to **m3**, etc., and **m1** only to poly, ndif, and pdif
 - Some technologies support “stacked vias”
- ❑ Active – active areas on/in substrate (**poly** gates, transistor channels (**nfet**, **pfet**), source and drain diffusions (**ndif**, **pdif**), and well contacts (**nwc**, **pwc**))
- ❑ Wells (**nw**) and other select areas (**pplus**, **nplus**, **prb**)

Physical Resource Block PRB

Layout with Cadence Tools

- Layer Map

CMOS Features

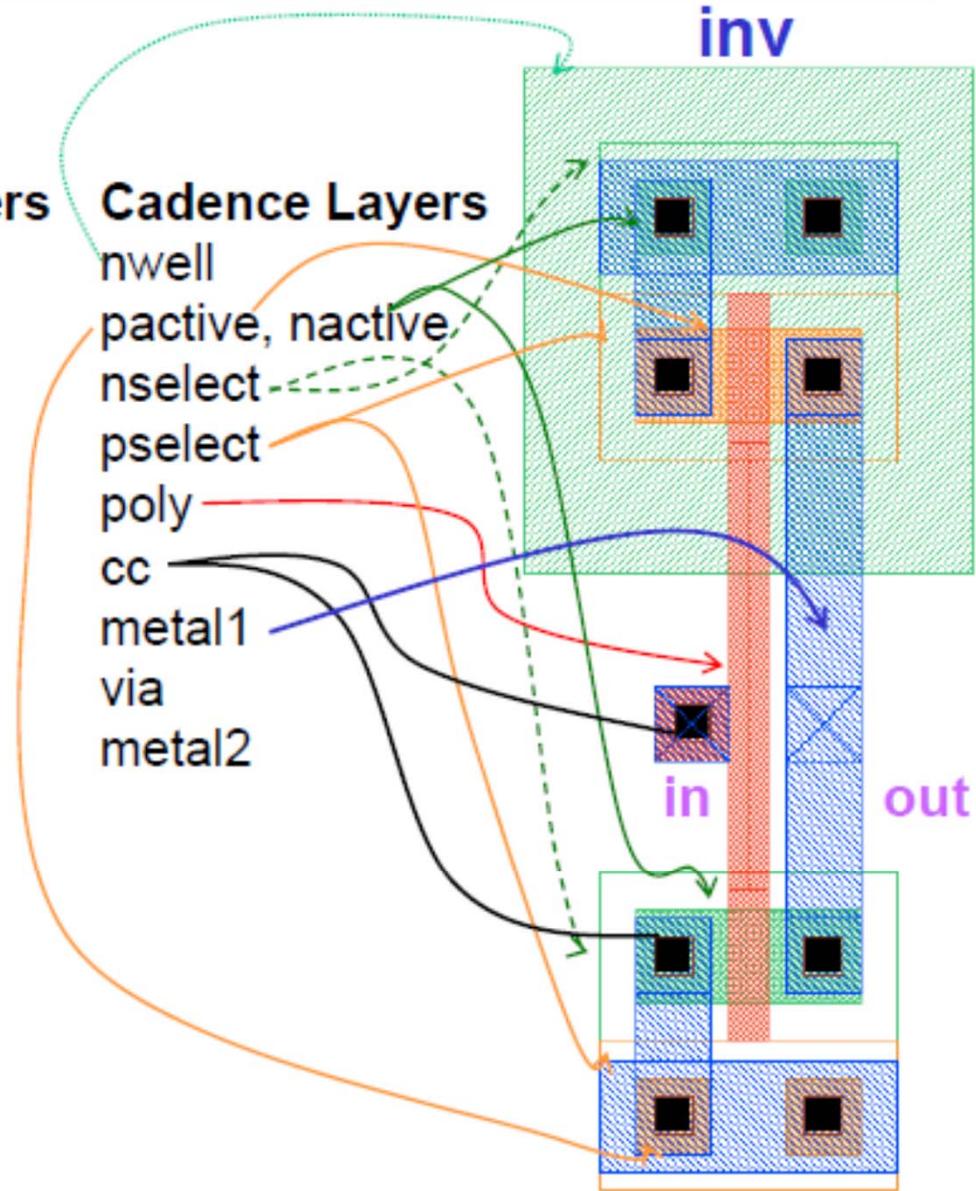
n-well
FOX
n+ S/D regions
p+ S/D regions
Gate
Active/Poly contact
Metal 1
Via
Metal 2

CMOS Mask Layers

n-well
active
n+ doping
p+ doping
poly
Contact
Metal 1
VIA
Metal 2

Cadence Layers

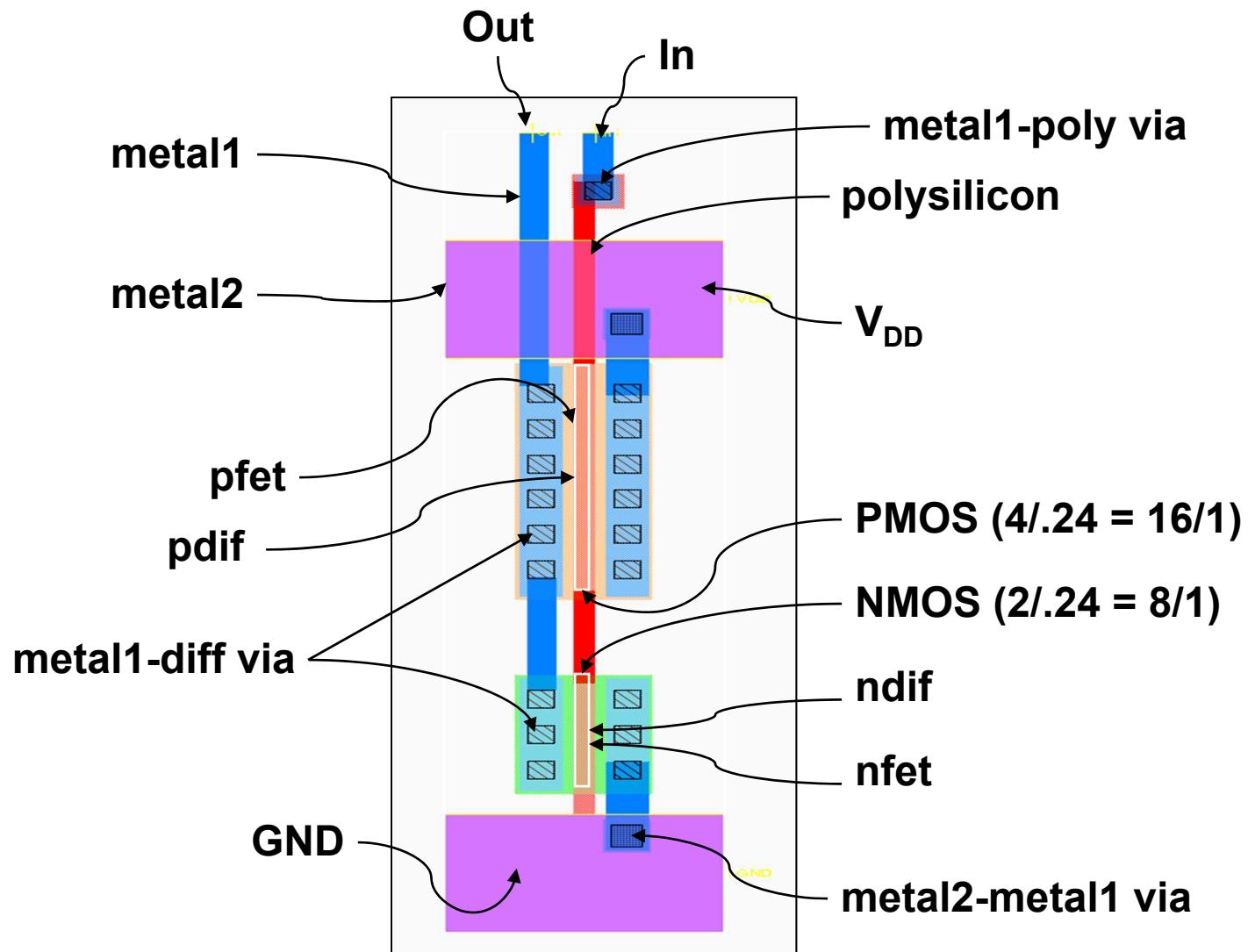
nwell
pactive, nactive
nselect
pselect
poly
cc
metal1
via
metal2



- Inverter Example



What's that?



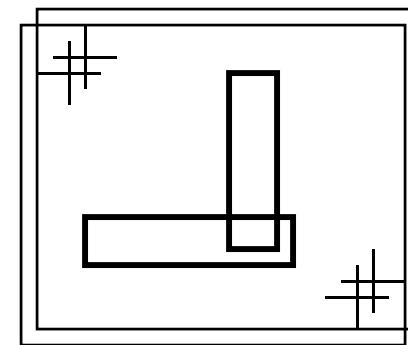
Design Rules

- ❑ Interface between the circuit designer and process engineer
- ❑ Guidelines for constructing process masks
- ❑ Unit dimension: minimum line width
 - *scalable design rules: lambda parameter*
 - *absolute dimensions: micron rules*
- ❑ Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- ❑ A complete set includes
 - *set of layers*
 - *intra-layer: relations between objects in the same layer*
 - *inter-layer: relations between objects on different layers*

Why Have Design Rules?

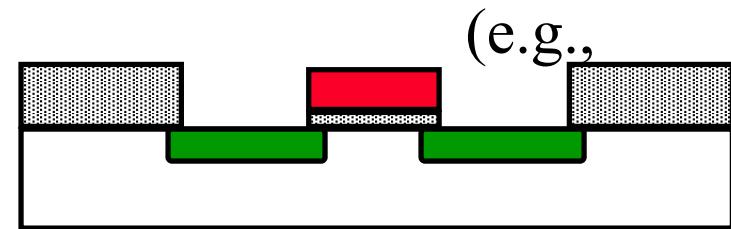
- ❑ To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

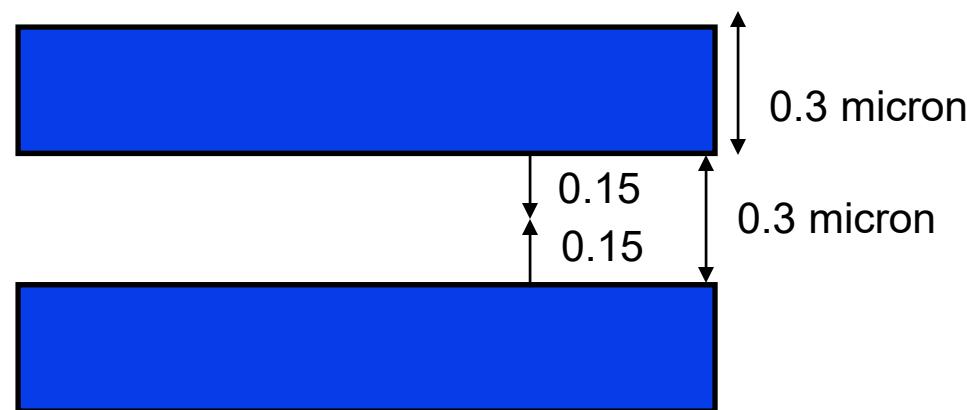
3. Process parameters
(lateral diffusion)



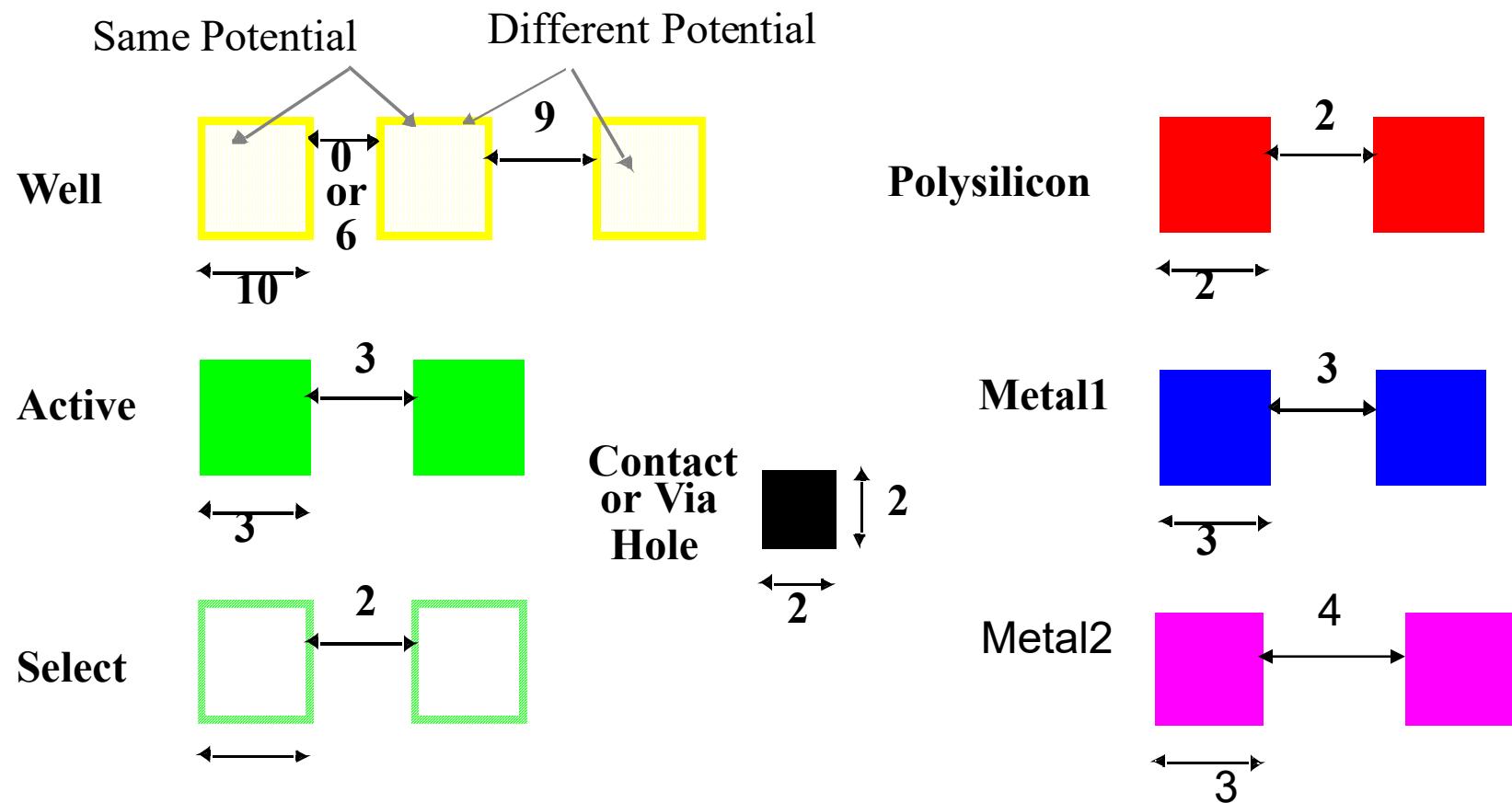
4. Rough surfaces

Intra-Layer Design Rule Origins

- ❑ Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
 - *minimum line width is set by the resolution of the patterning process (photolithography)*
- ❑ Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



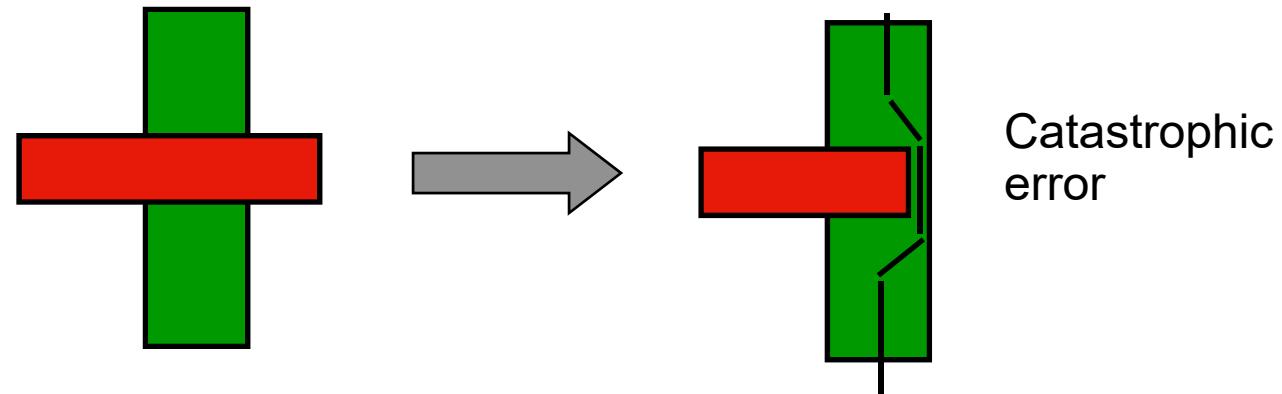
Intra-Layer Design Rules



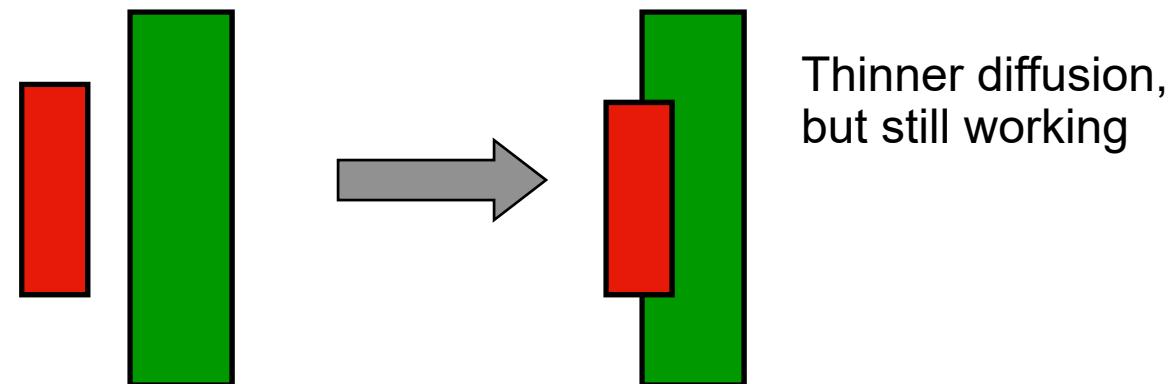
Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers

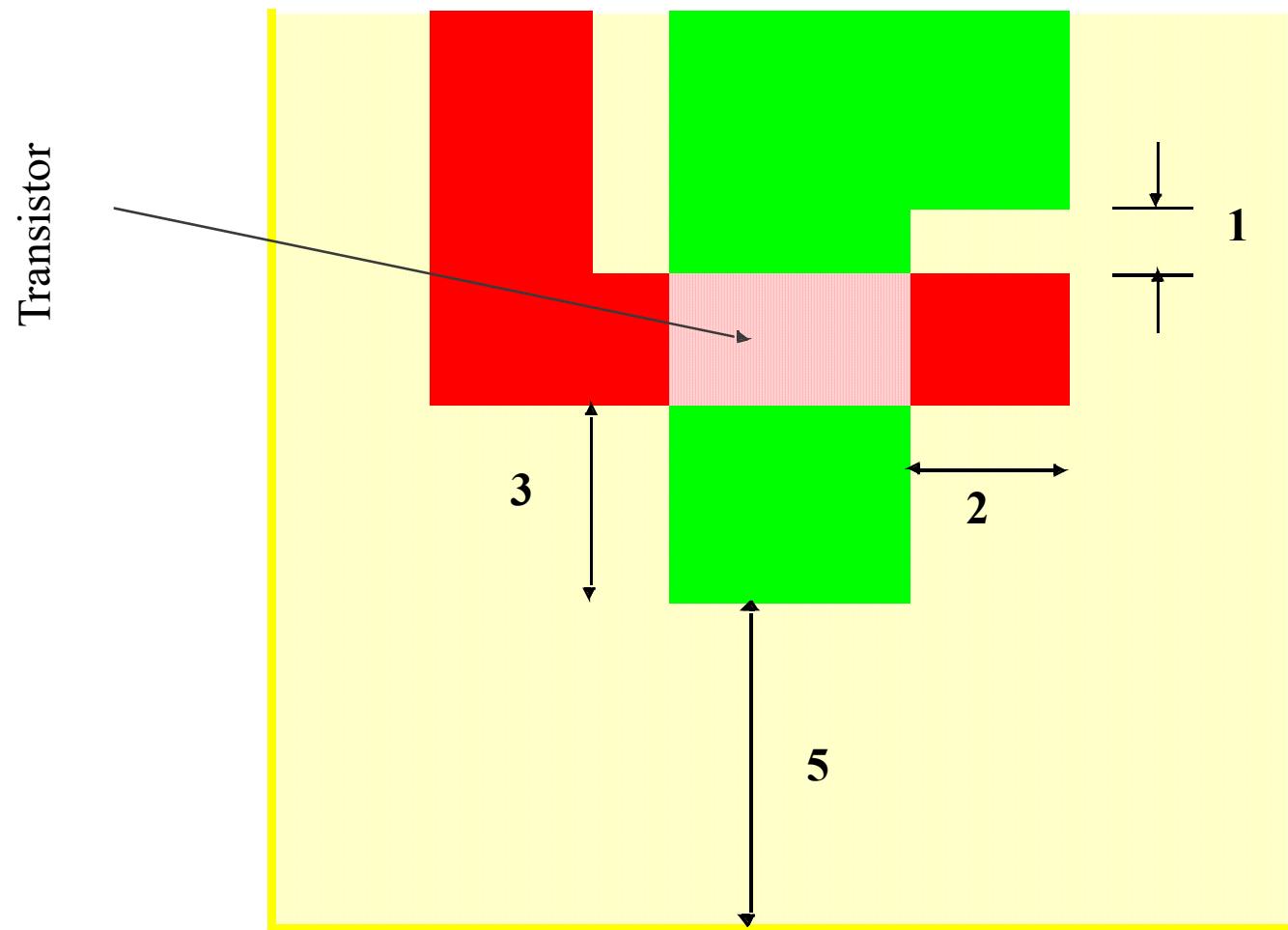
Transistors



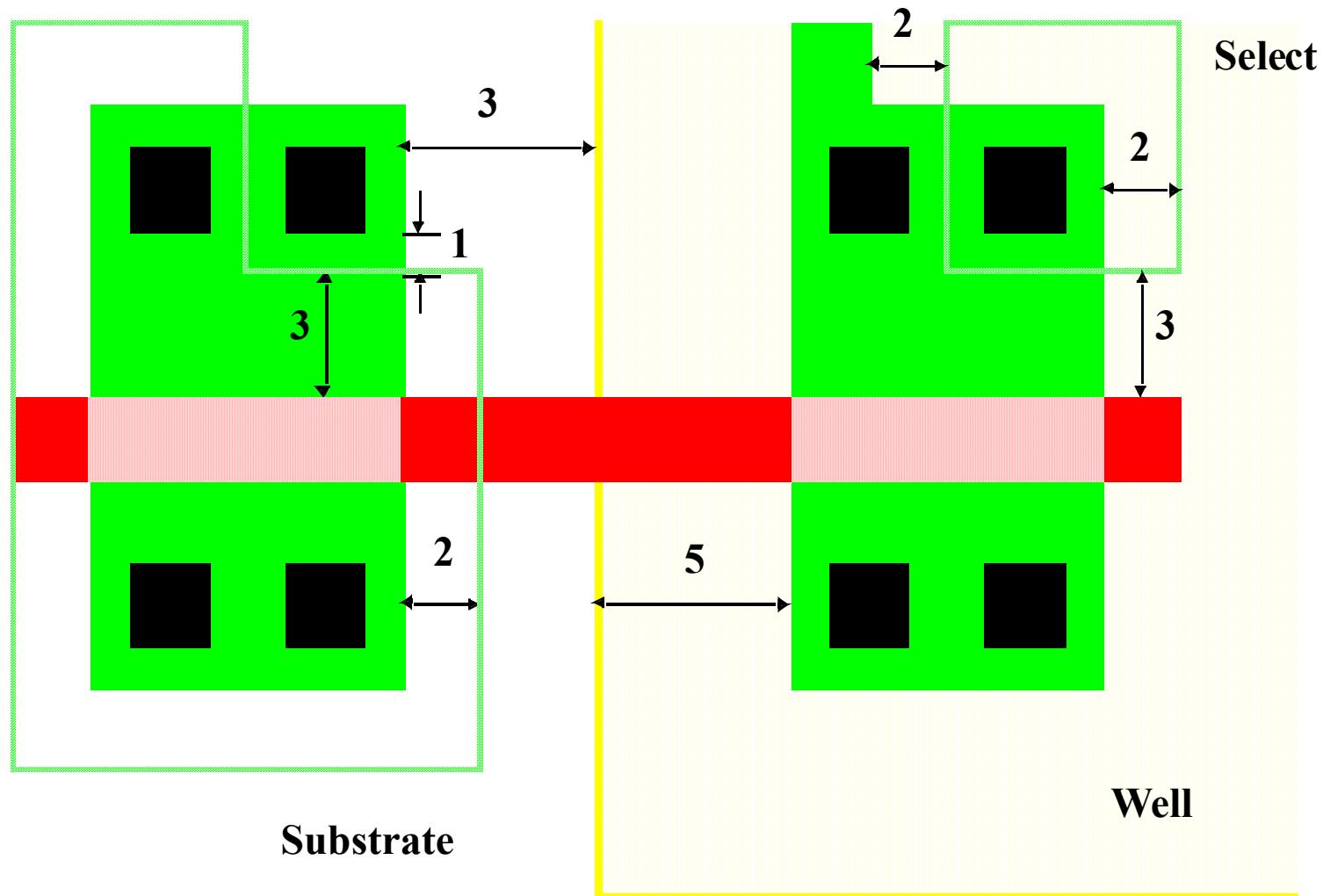
Unrelated Poly & Diffusion



Transistor Layout

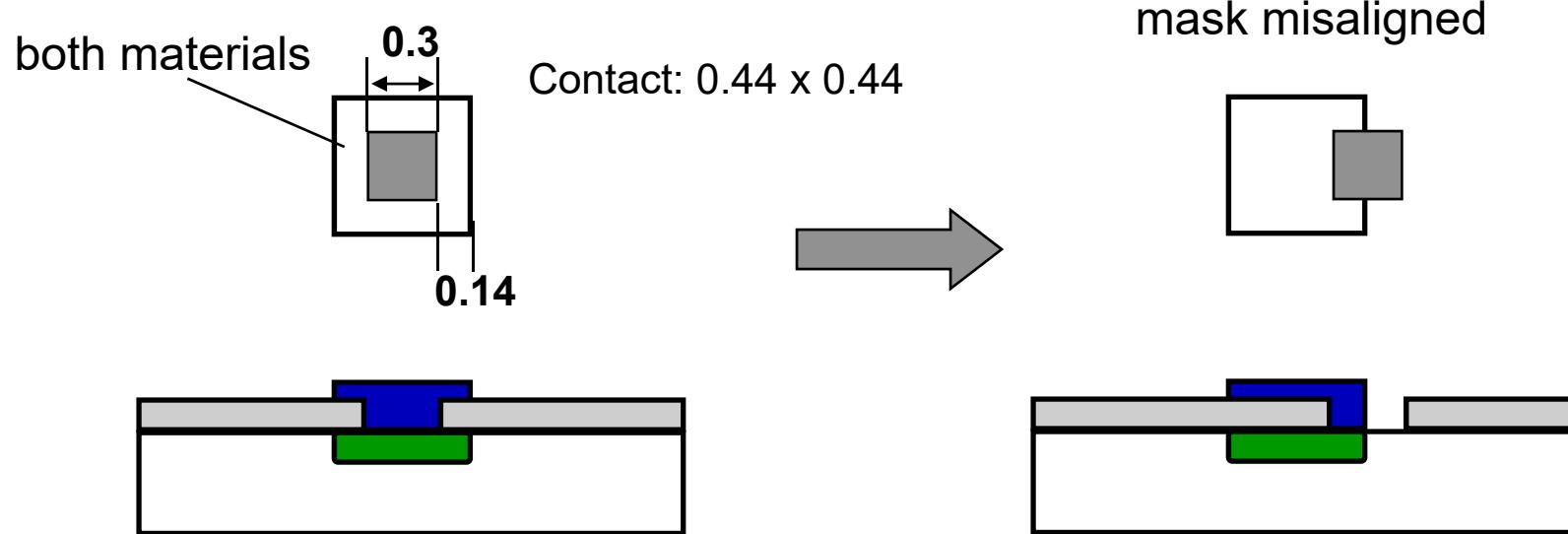
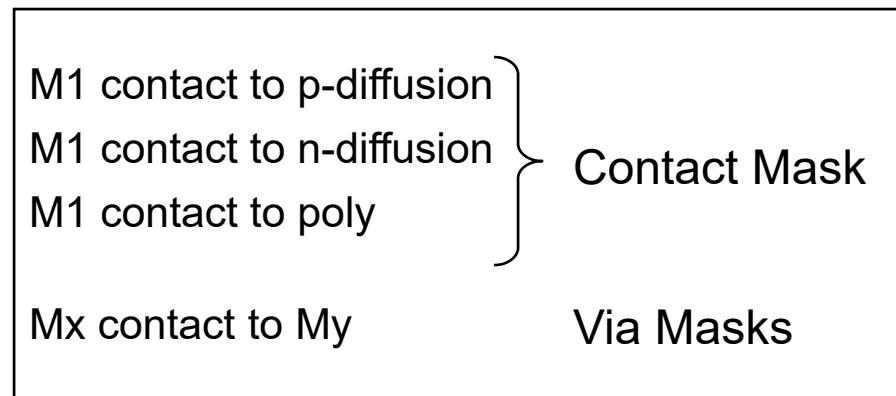


Select Layer

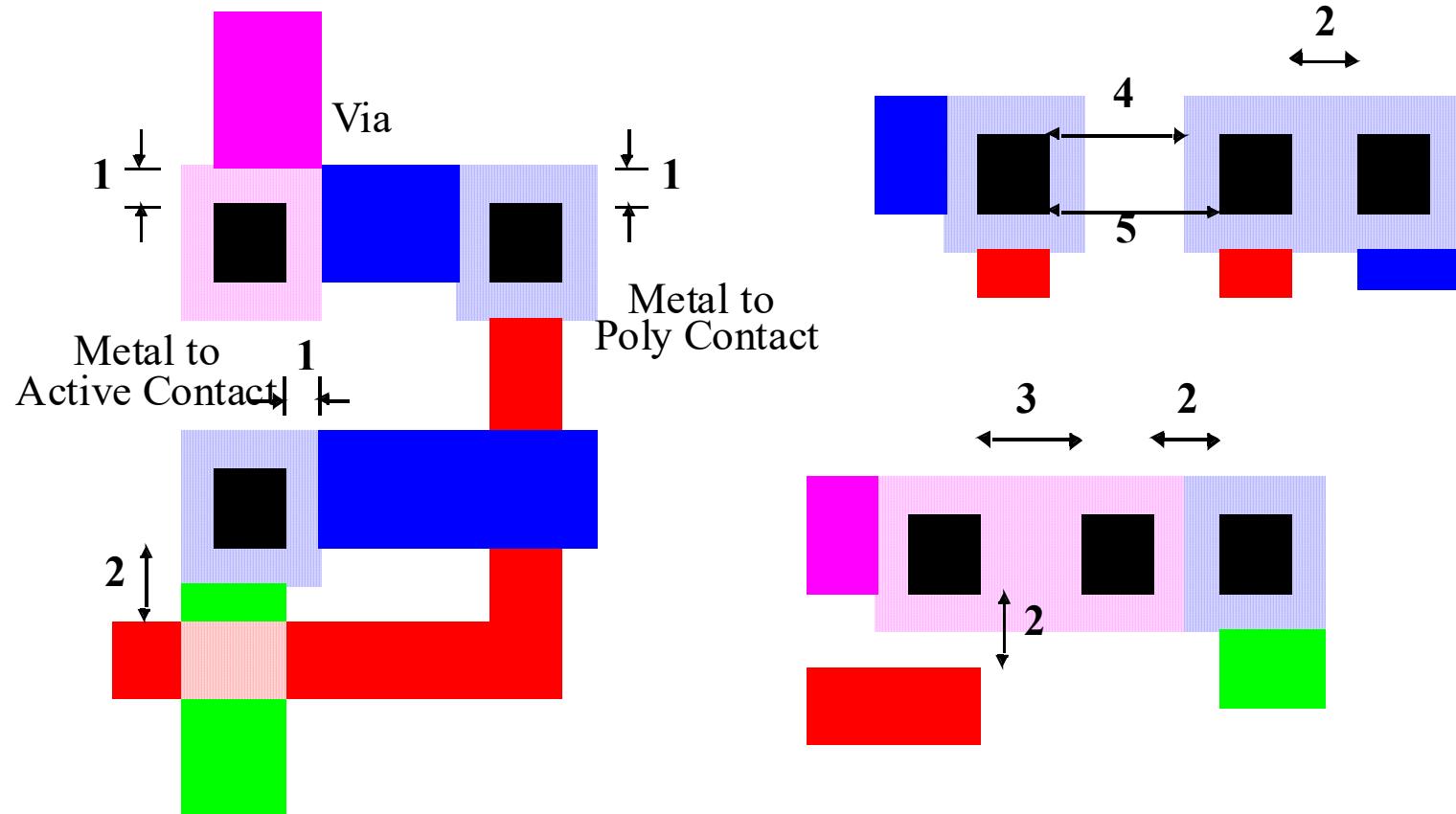


Inter-Layer Design Rule Origins, Con't

2. Contact and via rules



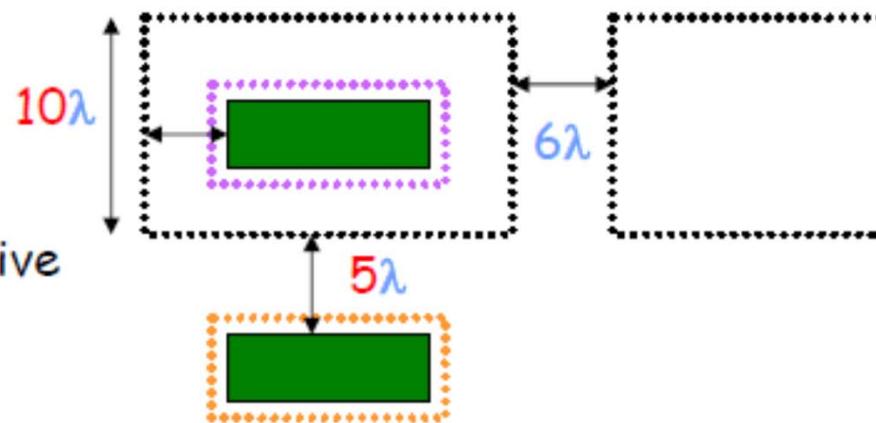
Vias and Contacts



Design Rules: 1

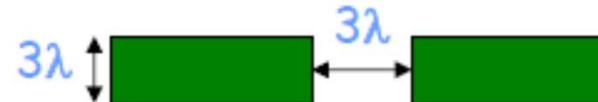
- n-well MOSIS SCMSOS rules; $\lambda = 0.3\mu m$ for AMI C5N

- required everywhere pMOS is needed
- rules
 - minimum width
 - minimum separation to self
 - minimum separation to nMOS Active
 - minimum overlap of pMOS Active



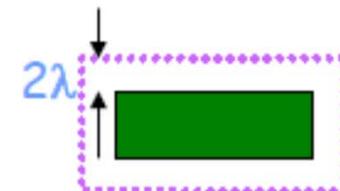
- Active

- required everywhere a transistor is needed
- any non-Active region is FOX
- rules
 - minimum width
 - minimum separation to other Active

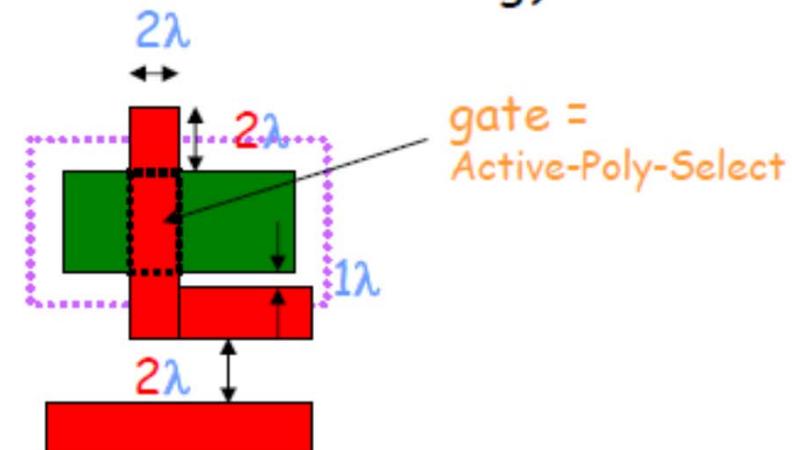


Design Rules: 2

- n/p Select
 - defines regions to be doped n+ and p+
 - tx S/D = Active AND Select NOT Poly
 - tx gate = Active AND Select AND Poly
 - rules
 - minimum overlap of Active
 - same for pMOS and nMOS
 - several more complex rules available



- Poly
 - high resistance conductor (can be used for short routing)
 - primarily used for tx gates
 - rules
 - minimum size
 - minimum space to self
 - minimum overlap of gate
 - minimum space to Active

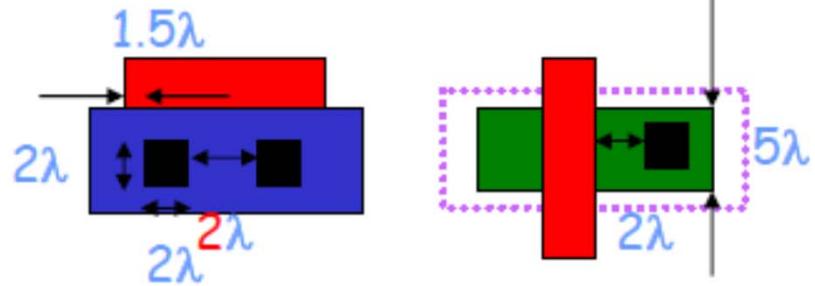


Design Rules: 3

- Contacts

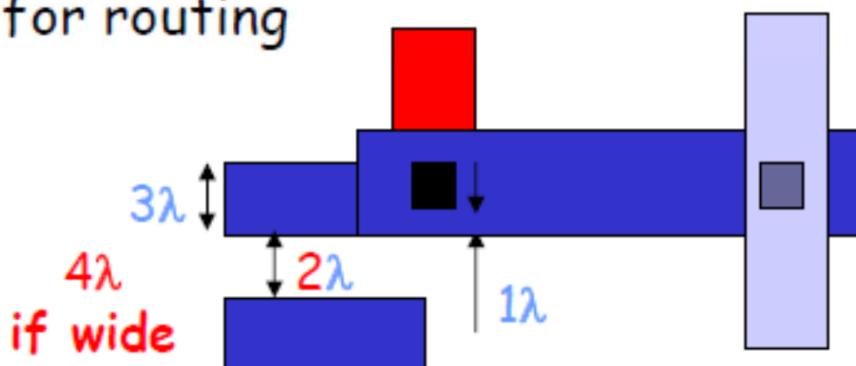
- Contacts to Metal1, from Active or Poly
 - use same layer and rules for both
- must be **SQUARE** and **MINIMUM SIZED**
- rules
 - exact size
 - minimum overlap by Active/Poly
 - minimum space to Contact
 - minimum space to gate

note: due to contact size and overlap rules, min. active size at contact will be $2+1.5+1.5=5\lambda$



- Metal1

- low resistance conductor used for routing
- rules
 - minimum size
 - minimum space to self
 - minimum overlap of Contact

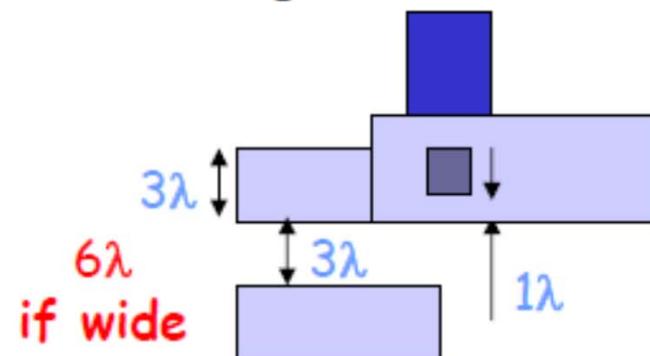


Design Rules: 4

- Vias
 - Connects Metal1 to Metal2
 - must be **SQUARE** and **MINIMUM SIZED**
 - rules
 - exact size 2λ
 - space to self 3λ
 - minimum overlap by Metal1/Metal2 1λ
 - minimum space to Contact 2λ
 - minimum space to Poly/Active edge 2λ

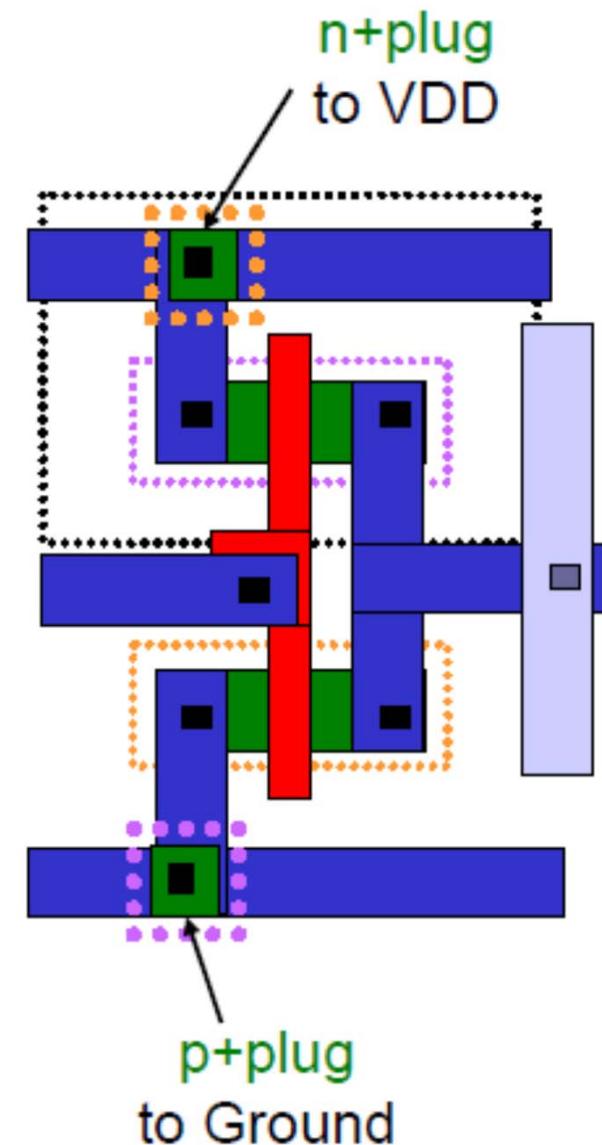
see MOSIS site
for illustrations

- Metal2
 - low resistance conductor used for routing
 - rules
 - minimum size
 - minimum space to self
 - minimum overlap of Via



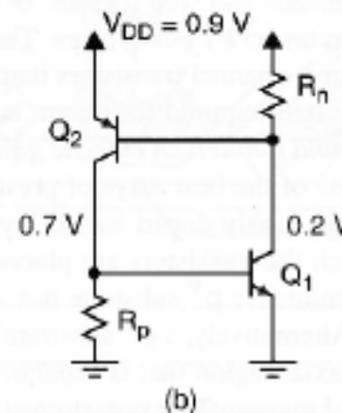
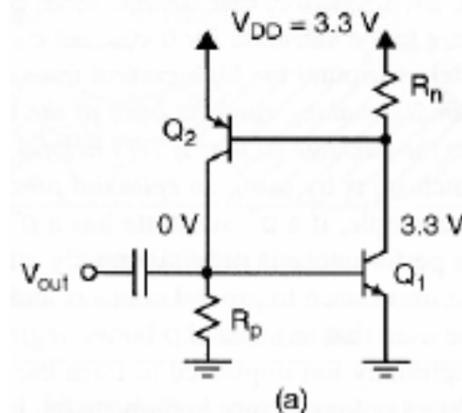
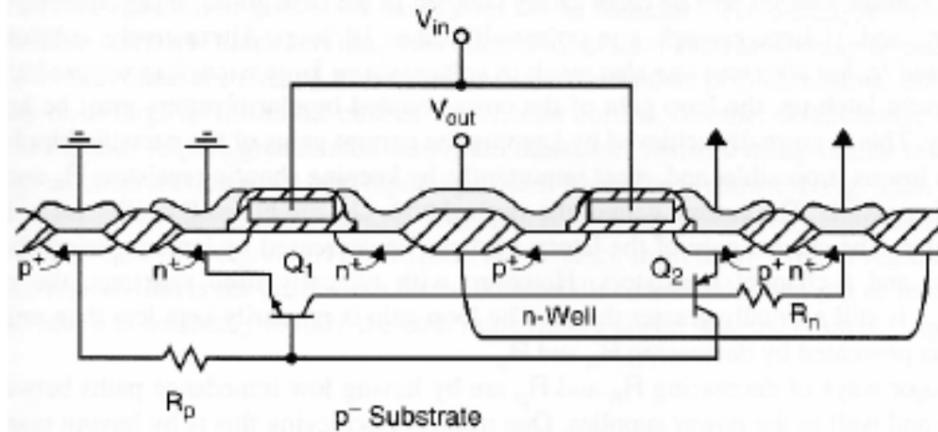
Substrate/well Contacts

- Substrate and nWells must be connected to the power supply within each cell
 - use many connections to reduce resistance
 - generally place
 - ~ 1 substrate contact per nMOS tx
 - ~ 1 nWell contact per pMOS tx
 - this connection is called a tap, or plug
 - often done on top of VDD/Ground rails
 - need p+ plug to Ground at substrate
 - need n+ plug to VDD in nWell



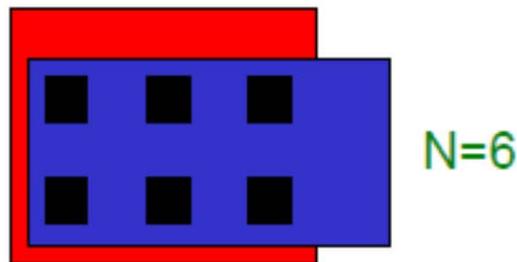
Latch-Up

- Latch-up is a very real, very important factor in circuit design that must be accounted for
- Due to (relatively) large current in substrate or n-well
 - create voltage drops across the resistive substrate/well
 - most common during large power/ground current spikes
 - turns on parasitic BJT devices, **effectively shorting power & ground**
 - often results in device failure with fused-open wire bonds or interconnects
 - **hot carrier effects** can also result in latch-up
 - latch-up very important for short channel devices
- **Avoid latch-up by**
 - including as many substrate/well contacts as possible
 - rule of thumb: one "plug" each time a tx connects to the power rail
 - limiting the maximum supply current on the chip

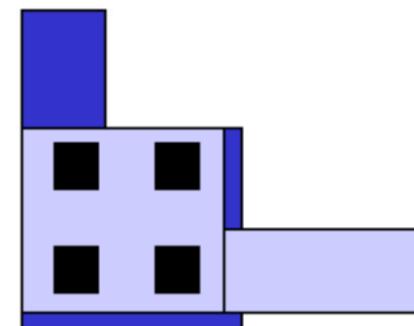
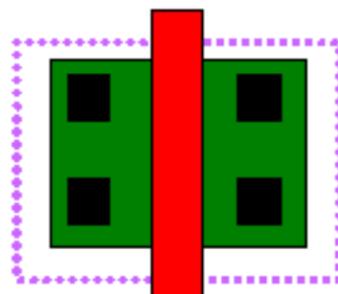


Multiple Contacts

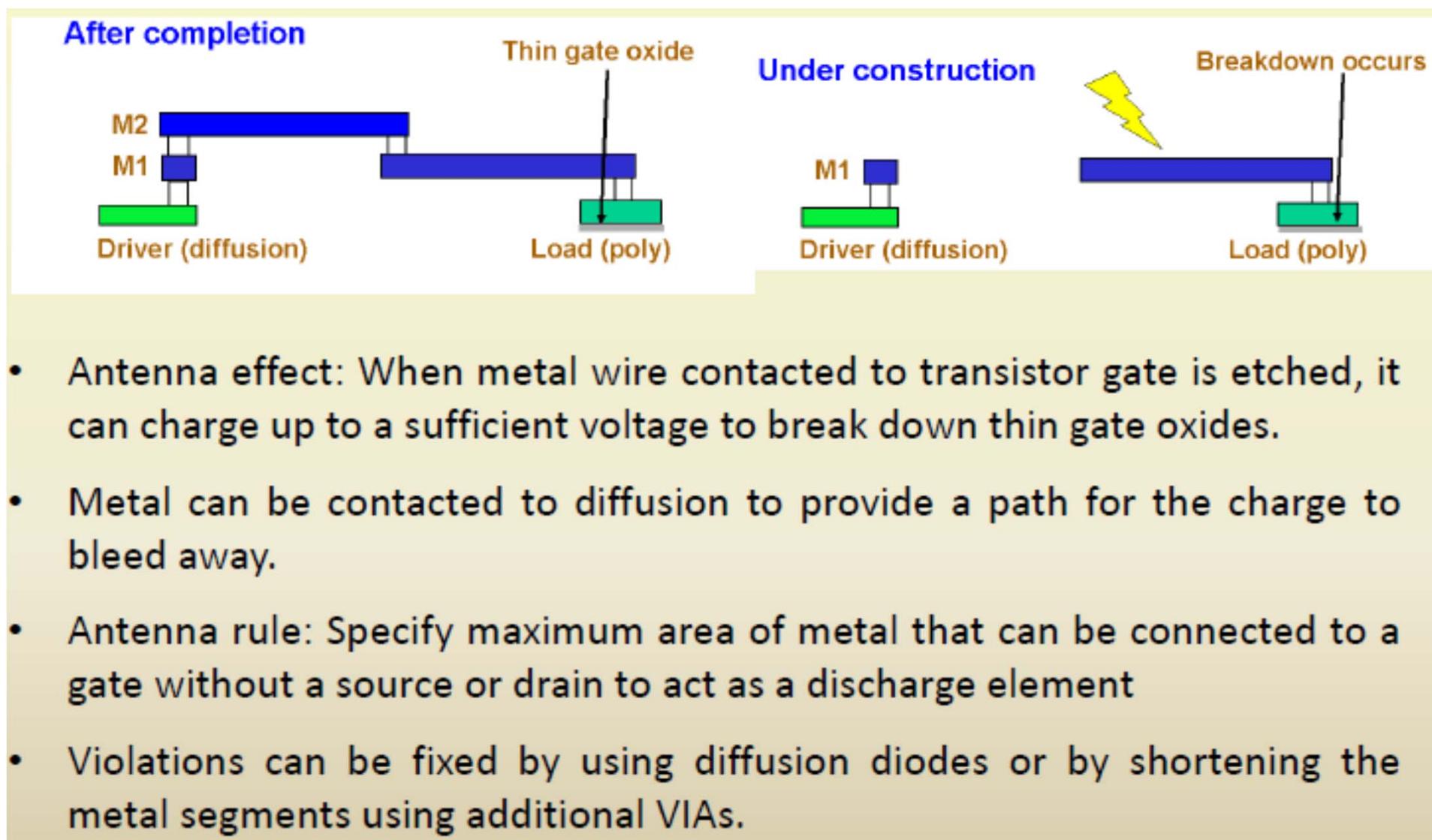
- Each contact has a characteristic resistance, R_c
- Contact resistances are much higher than the resistance of most interconnect layers
- Multiple contacts can be used to reduce resistance
 - $R_{c,eff} = R_c / N$, N =number of contacts



- Generally use as many contacts as space allows

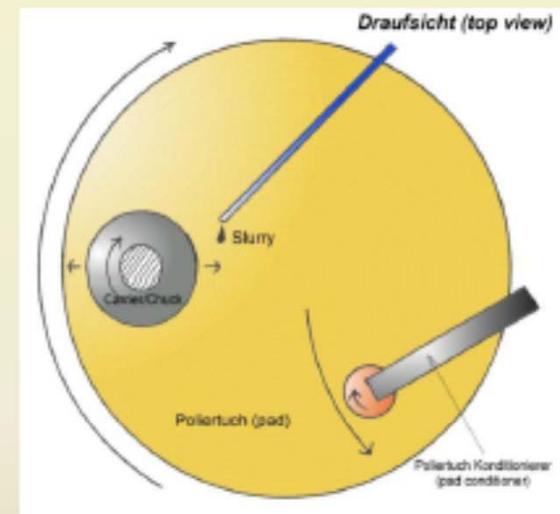


Specific rules: 1) Antenna rules



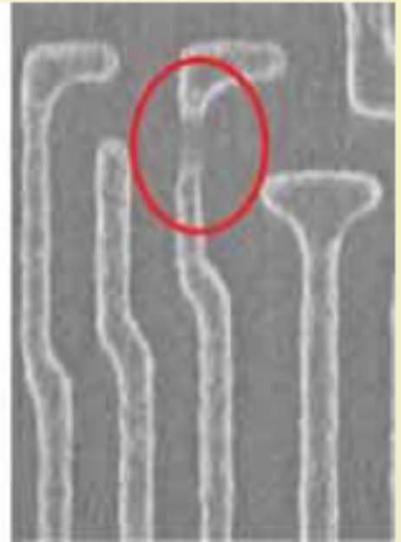
Specific rules: 2) Layer density rules

- For advanced processes, a minimum and maximum density of a particular layer within a specific area should be specified.
- Required to achieve uniform etch rates when using the CMP (Chemical-mechanical planarization) process
- CMP is a process of smoothing surfaces with the combination of chemical and mechanical forces
- As an example a metal layer might have a 30% minimum and 70% maximum fill with a 1mm by 1mm area.
- Poly and metal fillers should be added when a design is completed.



Litho-friendly layout design

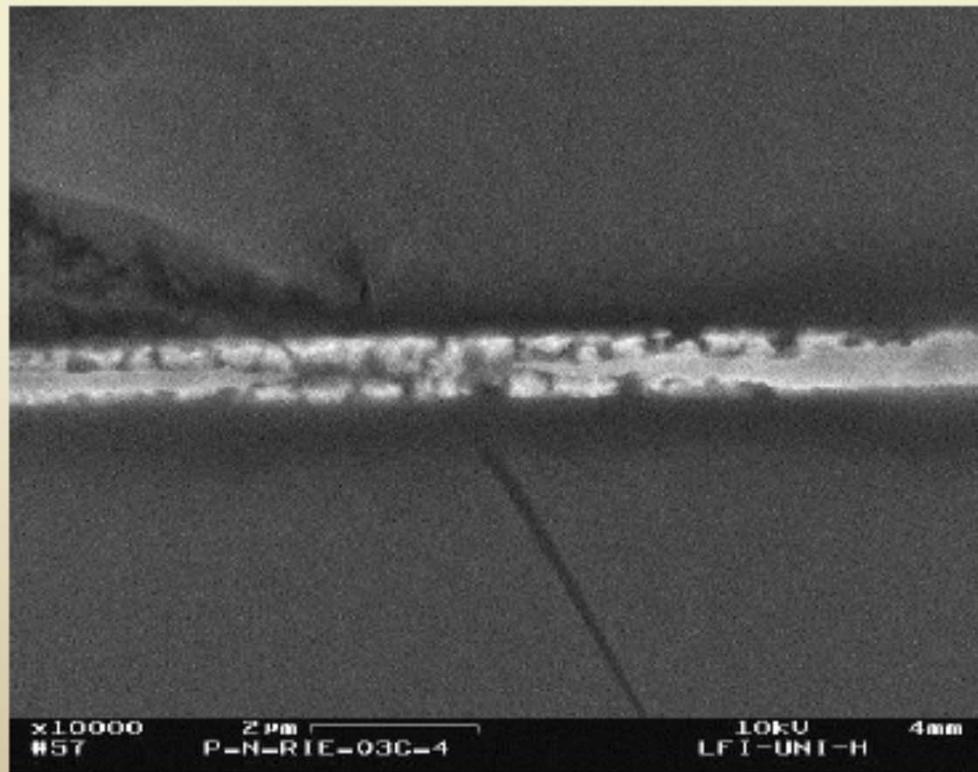
- Electrical short and open were caused by lithography process variation



- The foundry provides the designer with a “Litho-Friendly Design” (LFD) kit for the process in the same manner as a DRC kit.
- The lithography simulation tool identifies layout hotspots (structures with a higher probability of failing due to lithography process variations).
- The designer uses the feedback from the lithography simulation tool to improve the layout.

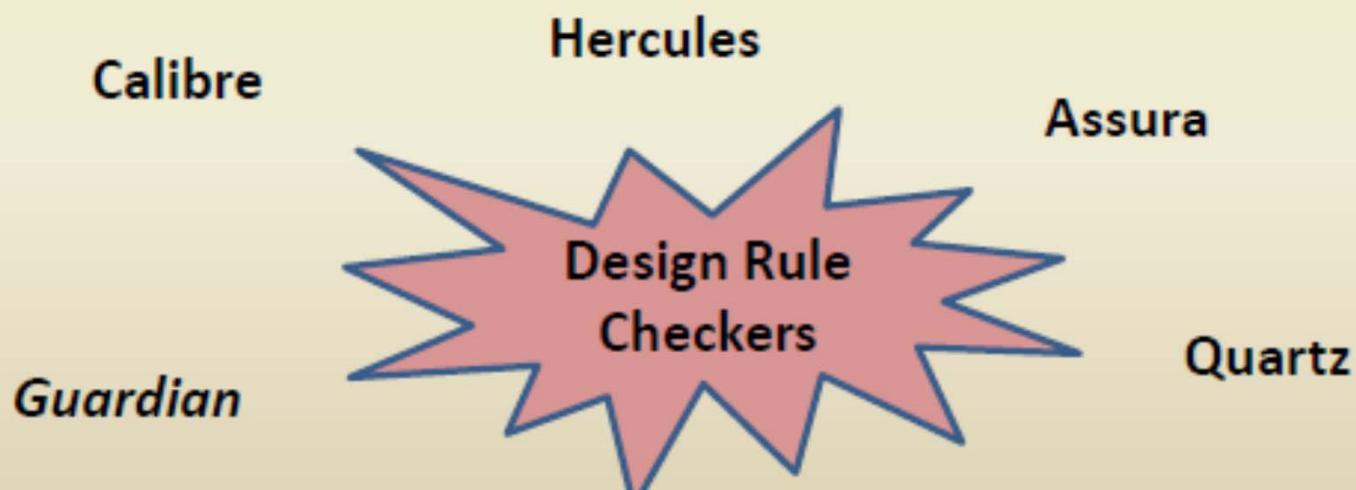
Electromigration

- Electromigration is the movement of the lattice ions of the interconnect material as the result of the momentum transfer from electrons.
- High current density or irregular shapes for the interconnects may cause the electromigration to happen in a short time.



Verifying the layout

- Ensure that none of the design rules are not violated.
- Computer-Aided Design Rule Checker (DRC)
- Online DRC for complicated designs
- Some of the products in the DRC area of the EDA are:



Next Lecture and Reminders

❑ Next lecture

- Static complementary CMOS gate design
 - Reading assignment – Rabaey, et al, 6.1-6.2.1

❑ Reminders

- Project Title due September 12th (next class!)
- HW2 due September 24th
- Evening midterm exam scheduled
 - Wednesday, October 10th from 8:15 to 10:15pm in 260 Willard
 - Only one midterm conflict filed for so far