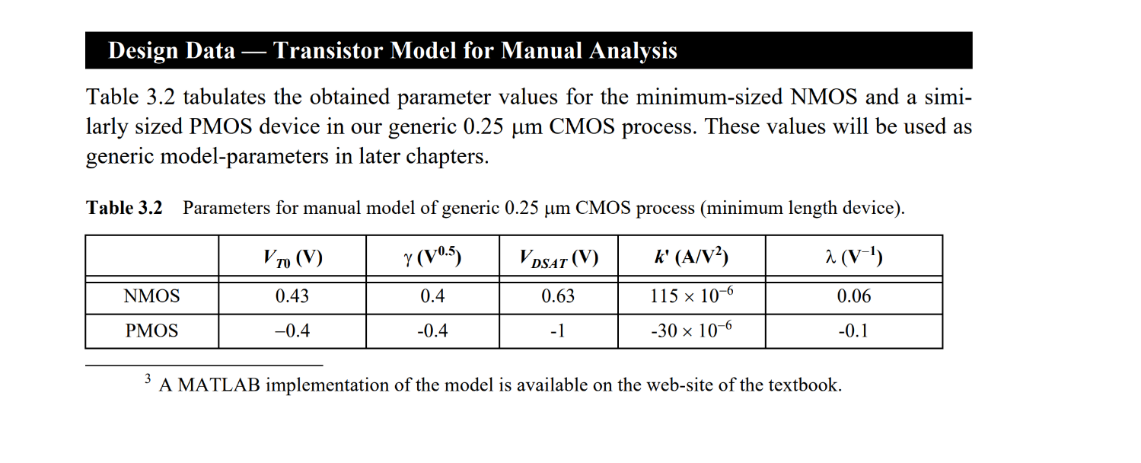
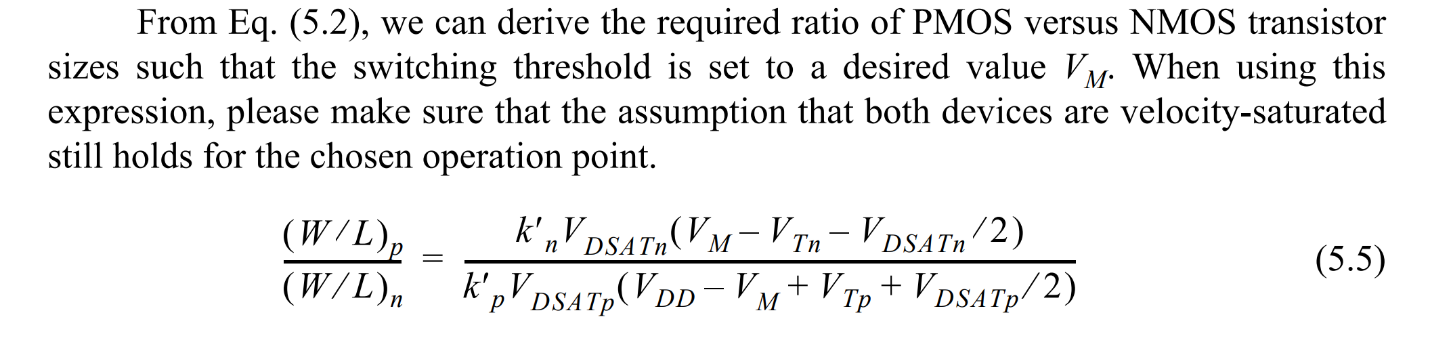
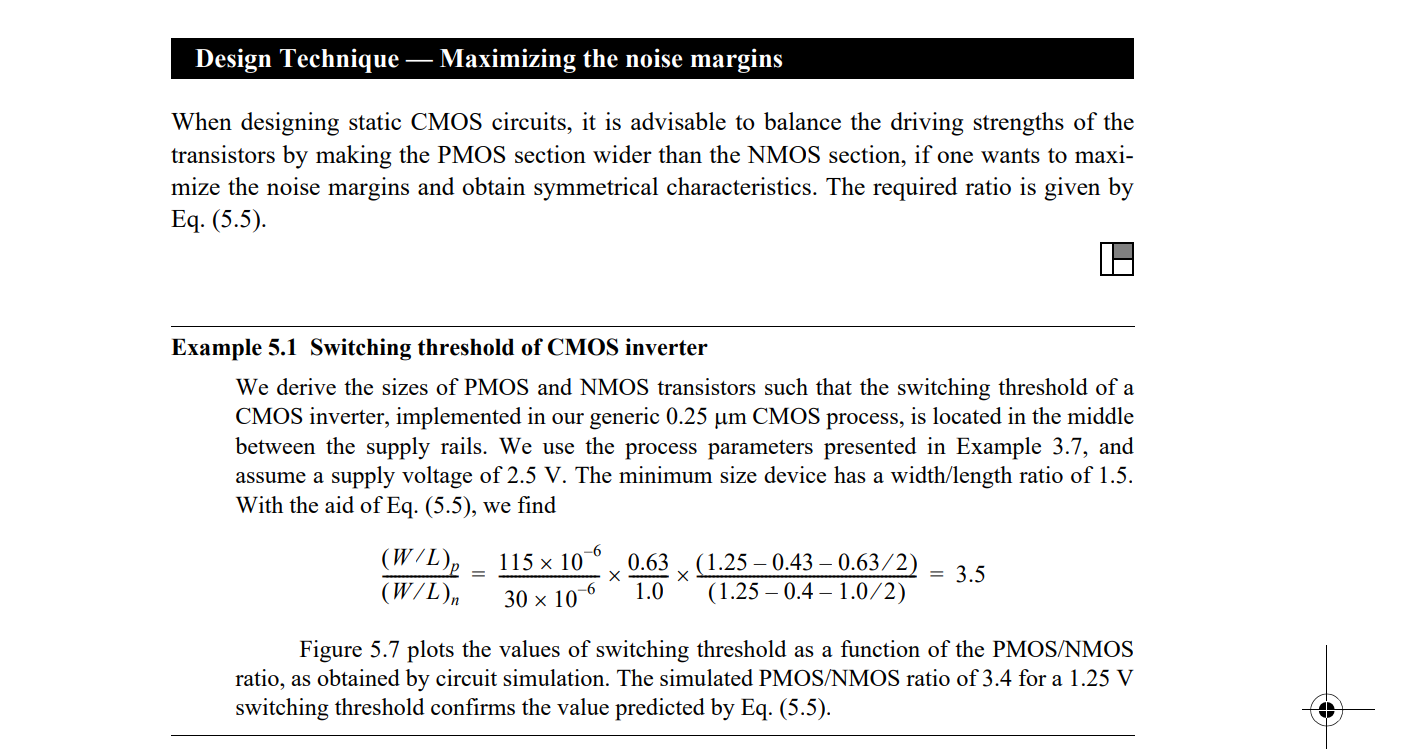


1. Design Reference Invertor

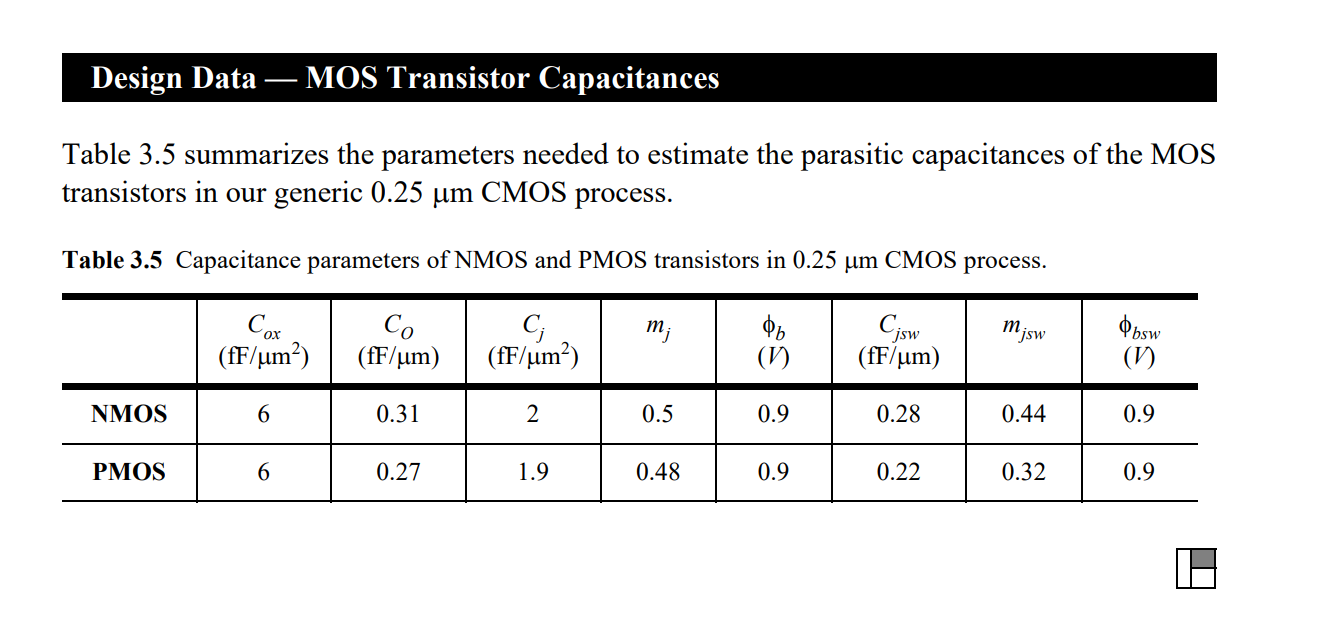


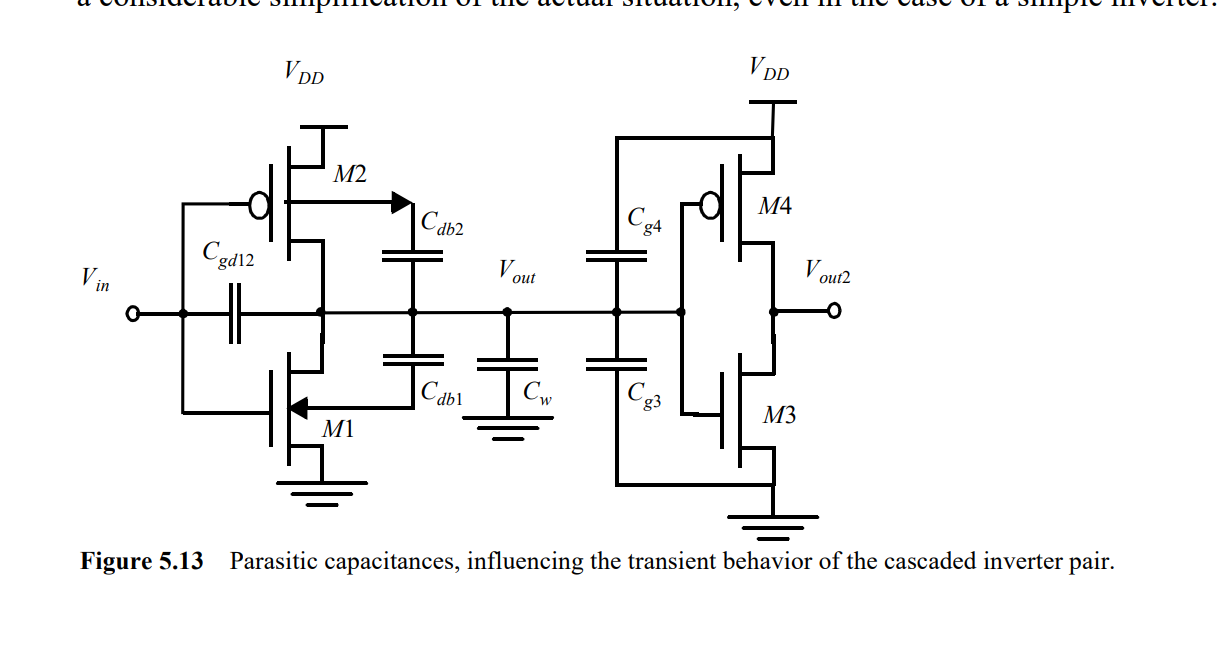


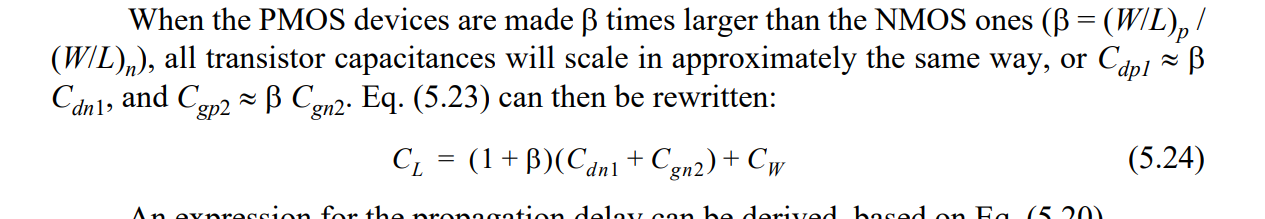


Because VDD= 2.5 V, and From the result in Example 5.1, We chose

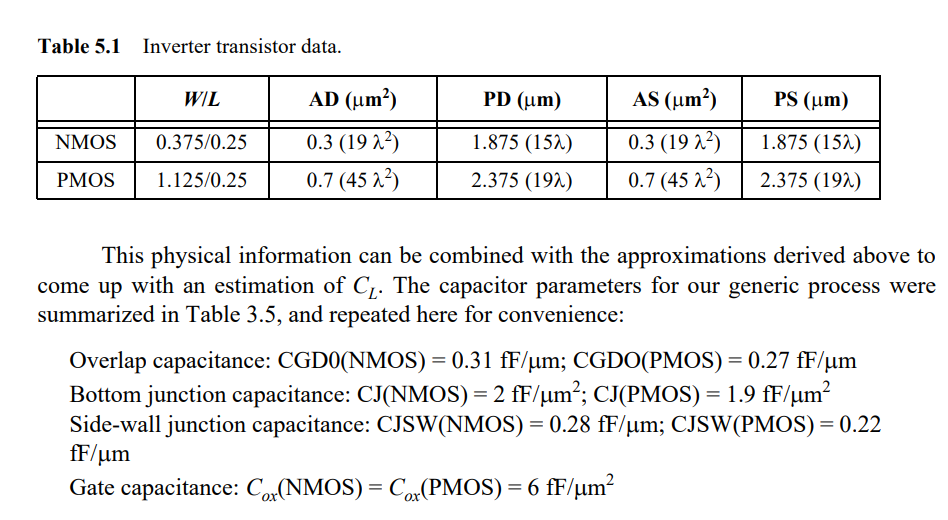
=3

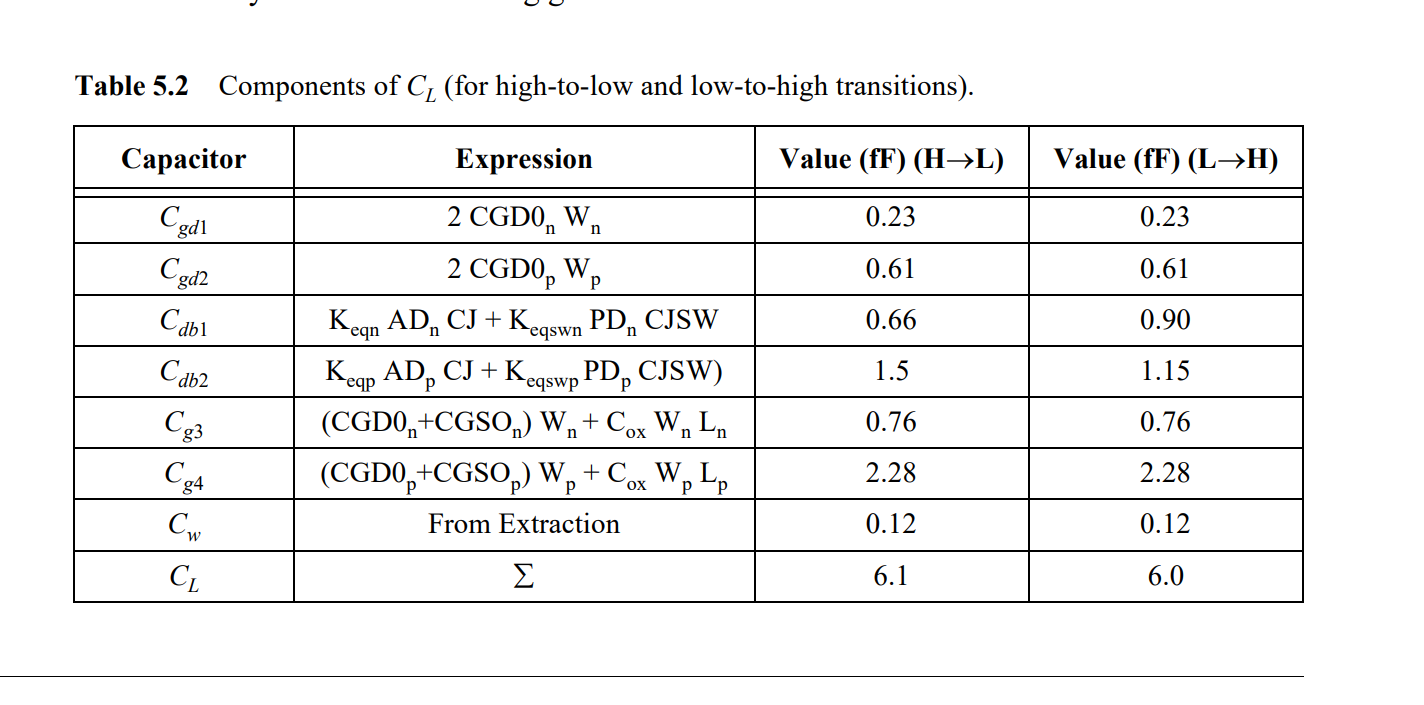






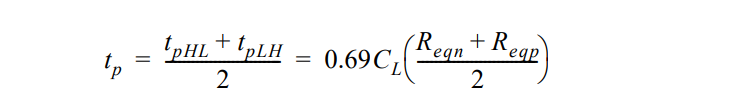
Cint = Cgd12+Cdb2+ Cb1 =

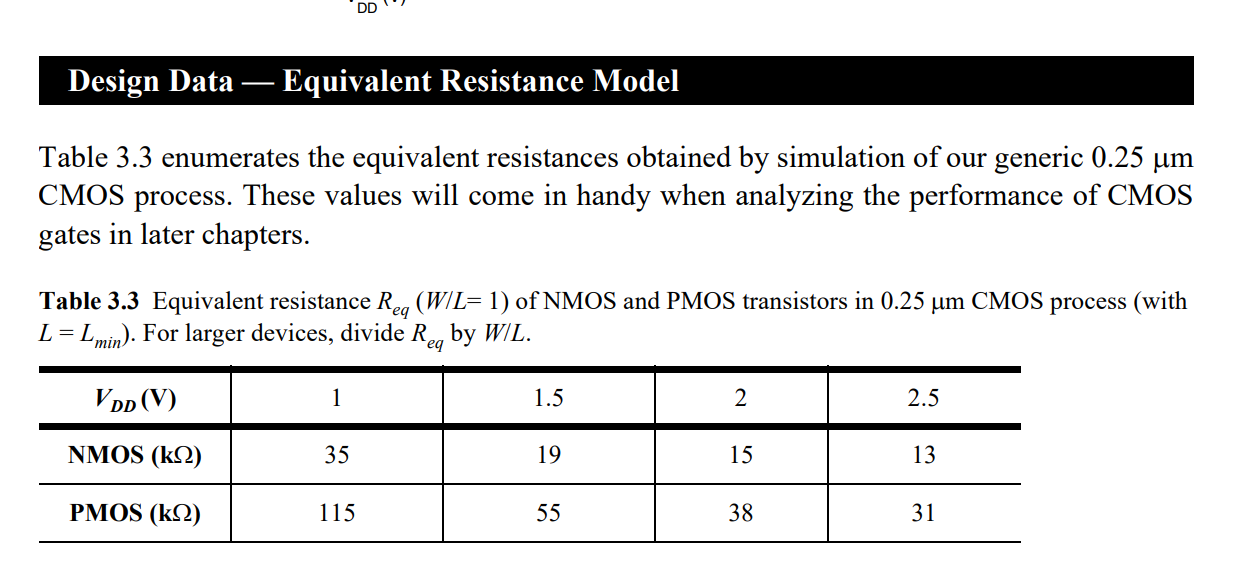




We have

From the requirement with external load = 20 fF, so





And with he generic 0.25 um CMOS process, we have the for NMOS and PMOS at VDD=2.5 V is:

And with the requirement for propagation delay is <0.5.

So we must choose to obtain tp<0.5 ns

So we have equation:

0.6Wn(fF)+0.54Wp (fF) = = 12.9(fF)

0.6Wn(fF)+0.54Wp (fF)=12.9(fF);

And Wp=3Fn

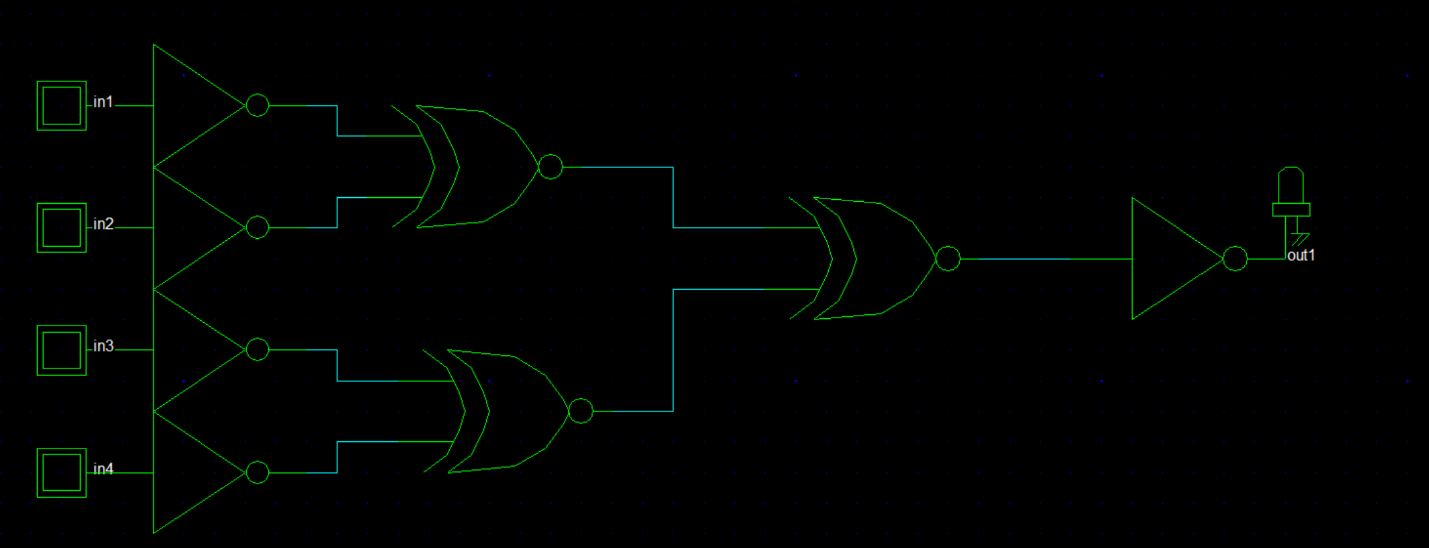
To have propagate delay <5ns, the size of invertor must be:

Wp <14.32 um and Wn < 4.48 um

Let choose the size of reference invertor is:

So, Cint of of reference invertor is:

Design the 4input XOR gate :



0.5

C

B

a

Chọn Wp/Wn = 3,

Choose Wc

Chọn W,Wn

Tìm Cint

Tìm CL

Tìm Delay

+ Tính cái cổng Xor ; s

