CSE477
VLSI Digital Circuits
Fall 2002

Lecture 07: Pass Transistor Logic

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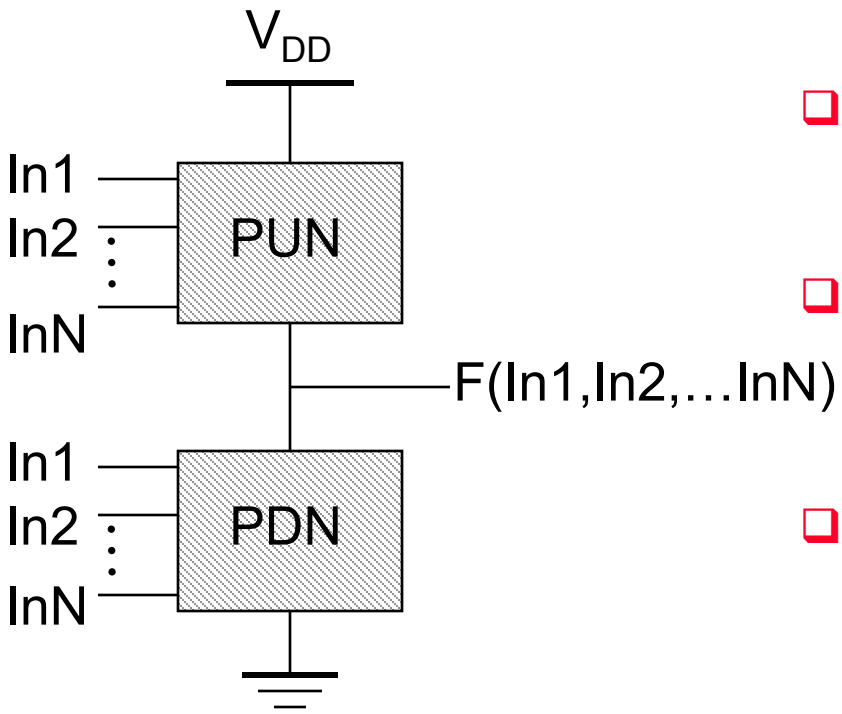
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: Static Complementary CMOS



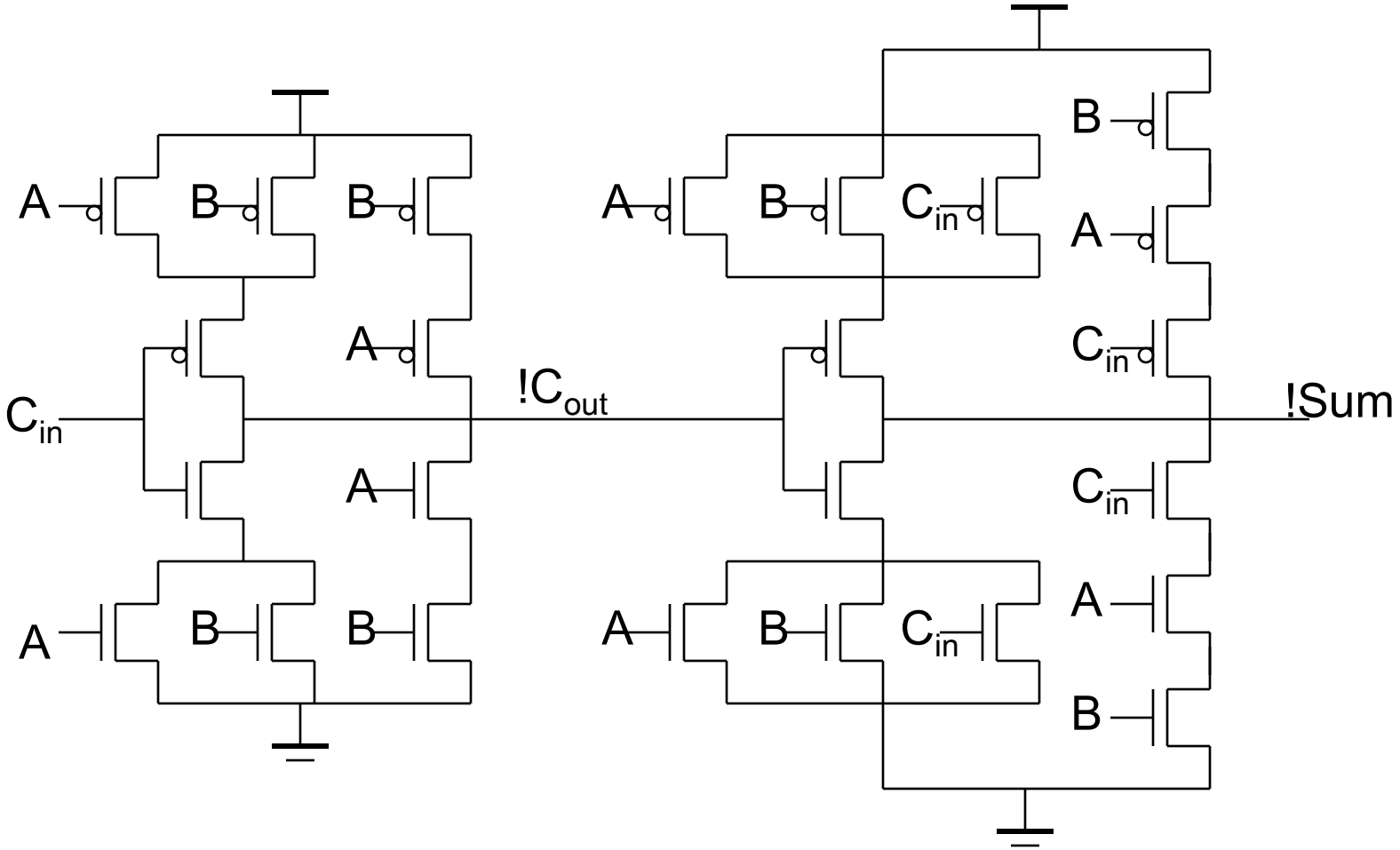
PUN and PDN are dual logic networks

- High noise margins
  - V_{OH} and V_{OL} are at V_{DD} and GND, respectively
- Low output impedance, high input impedance
- No static power consumption
  - Never a direct path between V_{DD} and GND in steady state
- Delay a function of load capacitance and transistor on resistance
- Comparable rise and fall times (under the appropriate relative transistor sizing conditions)

Review: Static CMOS Full Adder Circuit

$!C_{out} = !C_{in}\ (!A \vee !B) \vee !A\ !B$

$!Sum = C_{out}\ (!A \vee !B \vee !C_{in}) \vee !A\ !B\ !C_{in}$

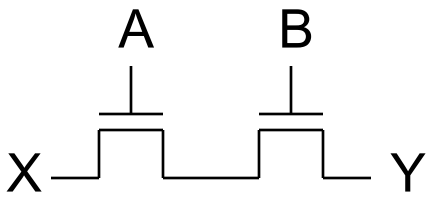


$C_{out} = C_{in}\ (A \vee B) \vee A\ B$

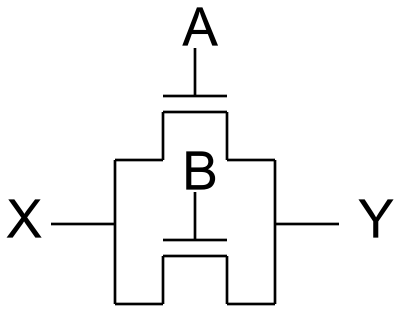
$Sum = !C_{out}\ (A \vee B \vee C_{in}) \vee A\ B\ C_{in}$

NMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



X = Y if A and B

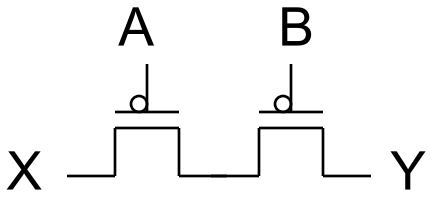


X = Y if A or B

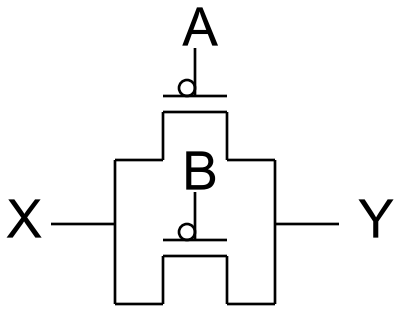
- Remember - NMOS transistors pass a strong 0 but a weak 1

PMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low



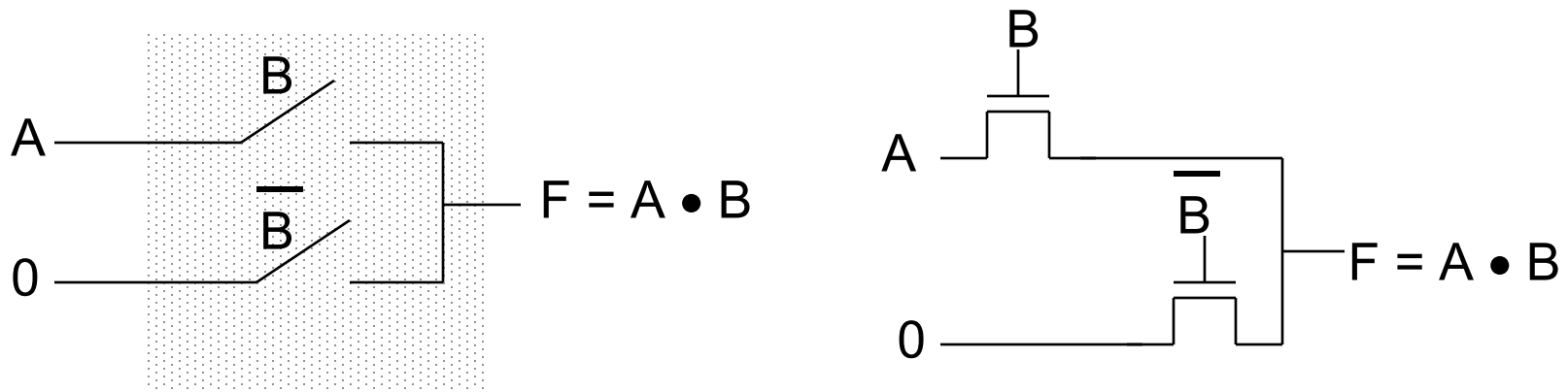
$X = Y$ if $\overline{A}$ and $\overline{B} = \overline{A + B}$



$X = Y$ if $\overline{A}$ or $\overline{B} = \overline{A \bullet B}$

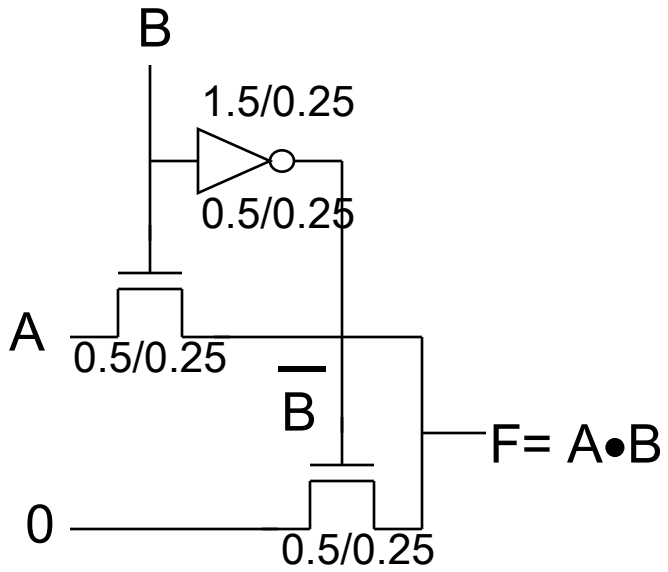
- Remember - PMOS transistors pass a strong 1 but a weak 0

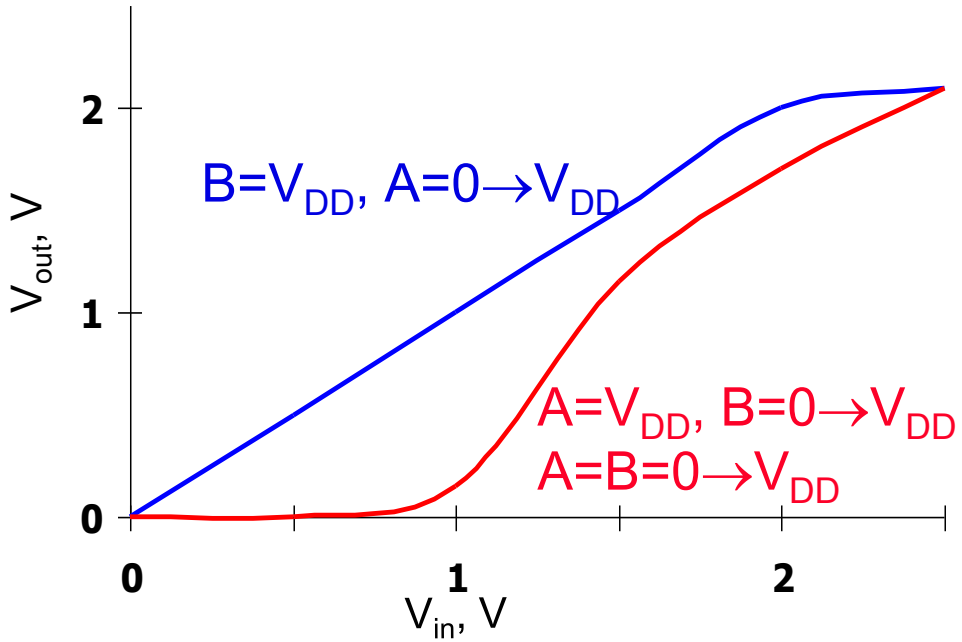
Pass Transistor (PT) Logic



- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)

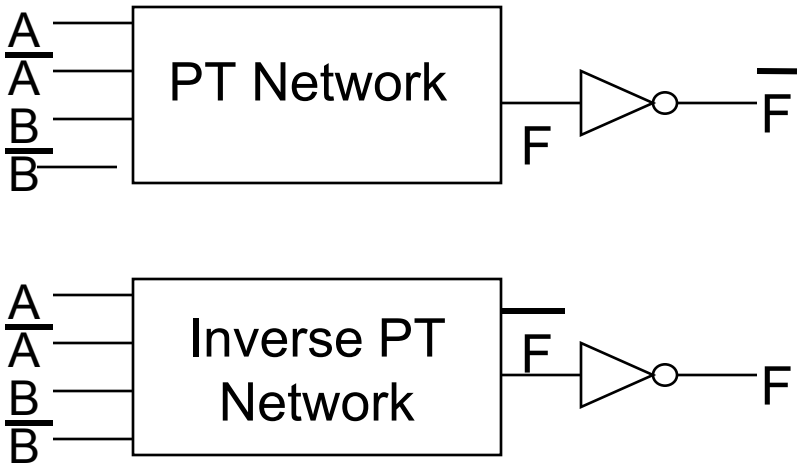
VTC of PT AND Gate

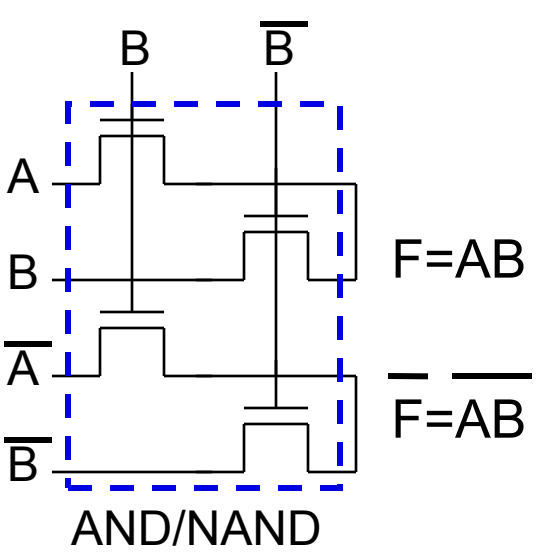


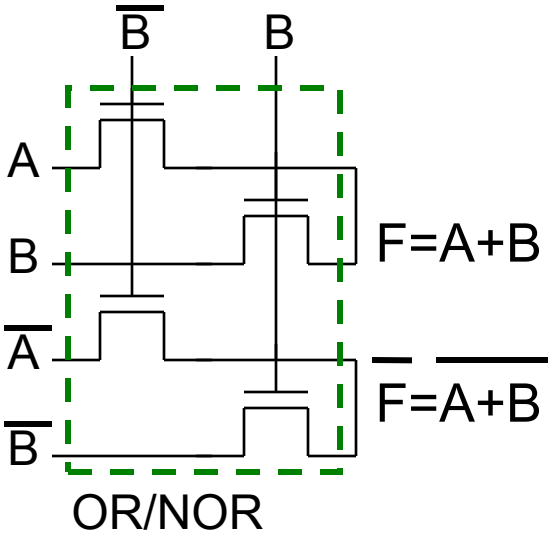


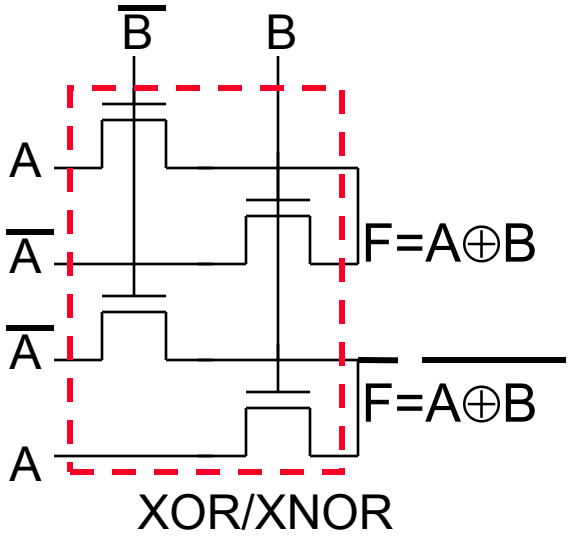
- Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

Differential PT Logic (CPL)





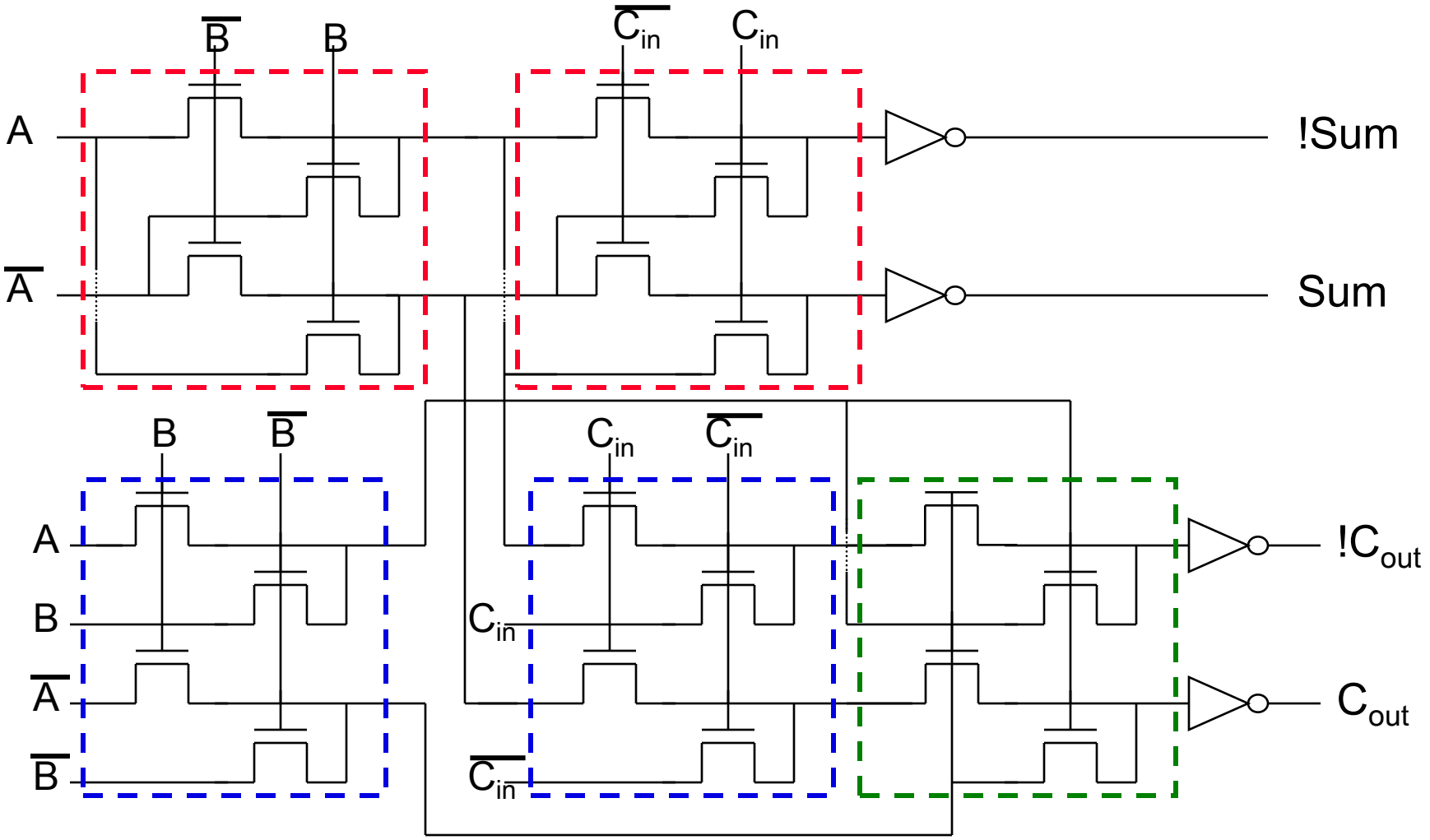




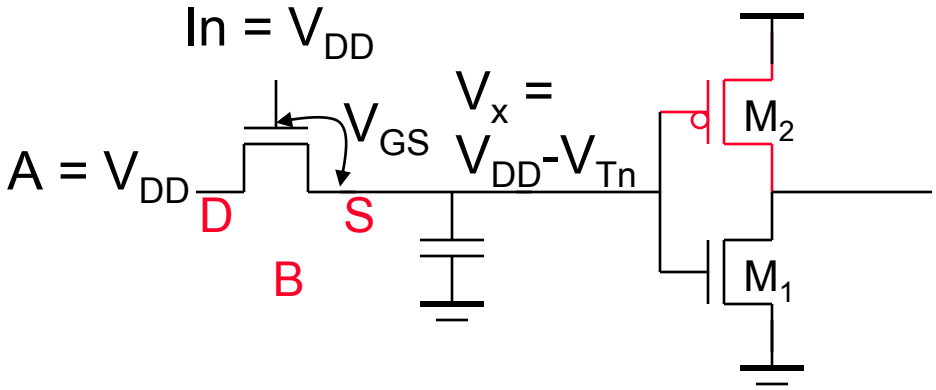
CPL Properties

- Differential so complementary data inputs and outputs are always available (so don't need extra inverters)
- Still static, since the output defining nodes are always tied to V_{DD} or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

CPL Full Adder

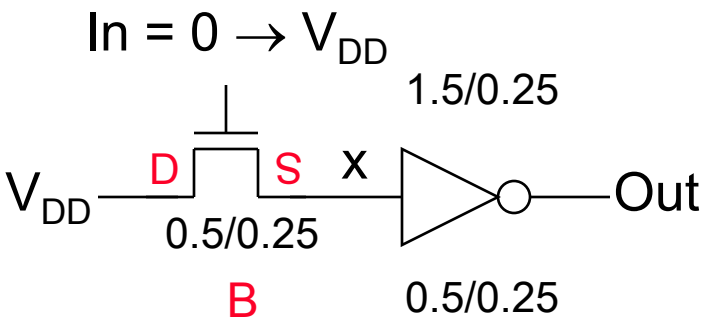


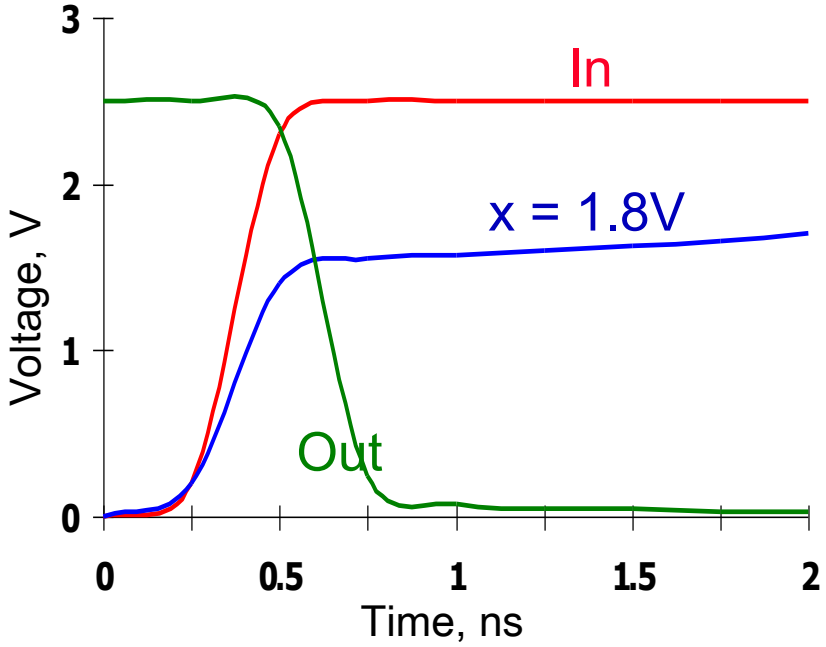
NMOS Only PT Driving an Inverter



- V_x does not pull up to V_{DD}, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power consumption (M_2 may be weakly conducting forming a path from V_{DD} to GND)
- Notice V_{Tn} increases of pass transistor due to body effect (V_{SB})

Voltage Swing of PT Driving an Inverter

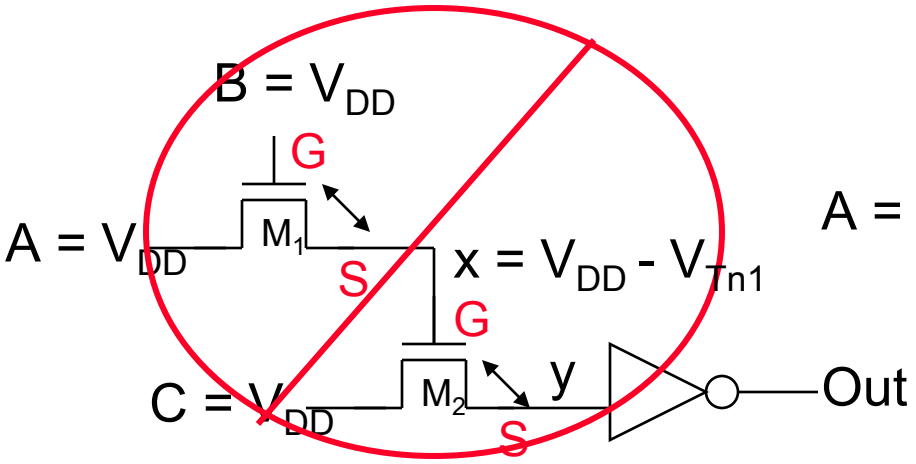


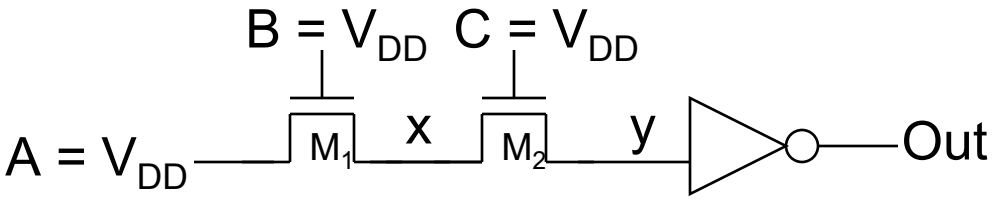


- Body effect – large V_{SB} at x - when pulling high (B is tied to GND and S charged up close to V_{DD})
- So the voltage drop is even worse

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{(|2\phi_f| + V_x)} - \sqrt{|2\phi_f|}))$$

Cascaded NMOS Only PTs



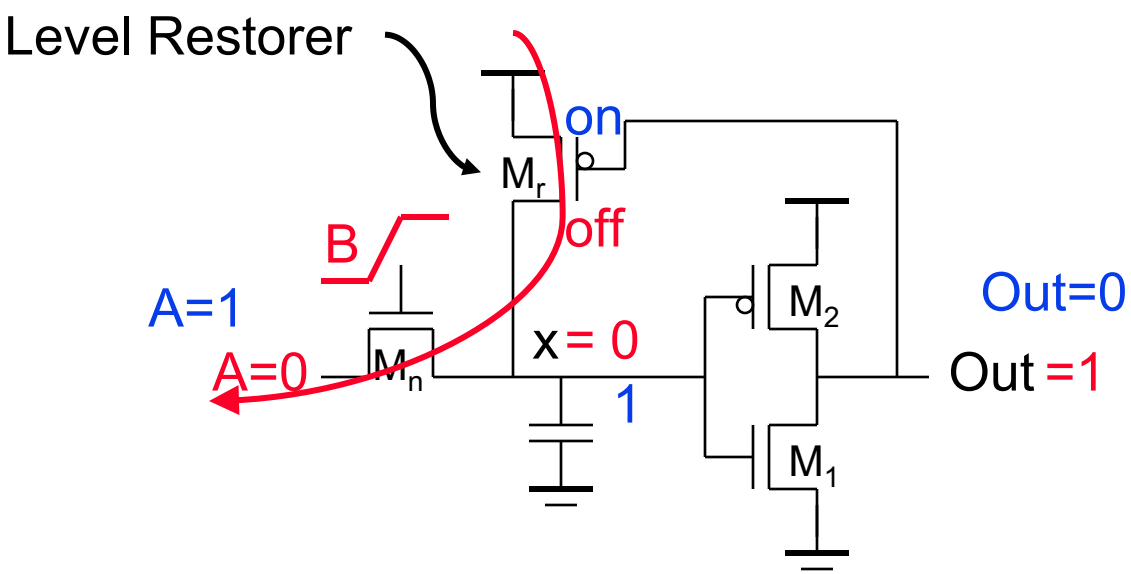


Swing on y = $V_{DD} - V_{Tn1} - V_{Tn2}$

Swing on y = $V_{DD} - V_{Tn1}$

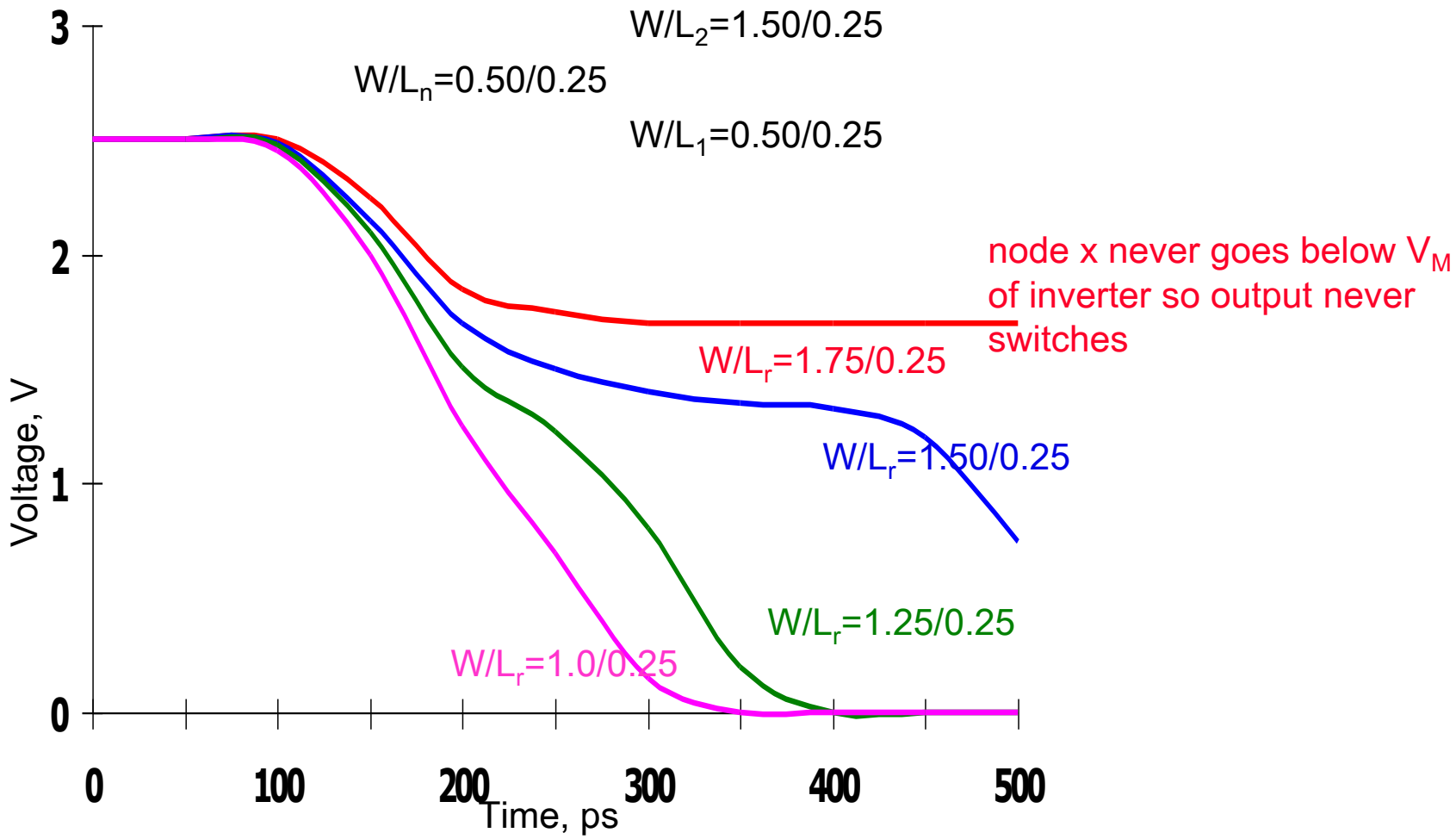
- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

Solution 1: Level Restorer



- Full swing on x (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when A is high
- For correct operation M_r must be sized correctly (ratioed)

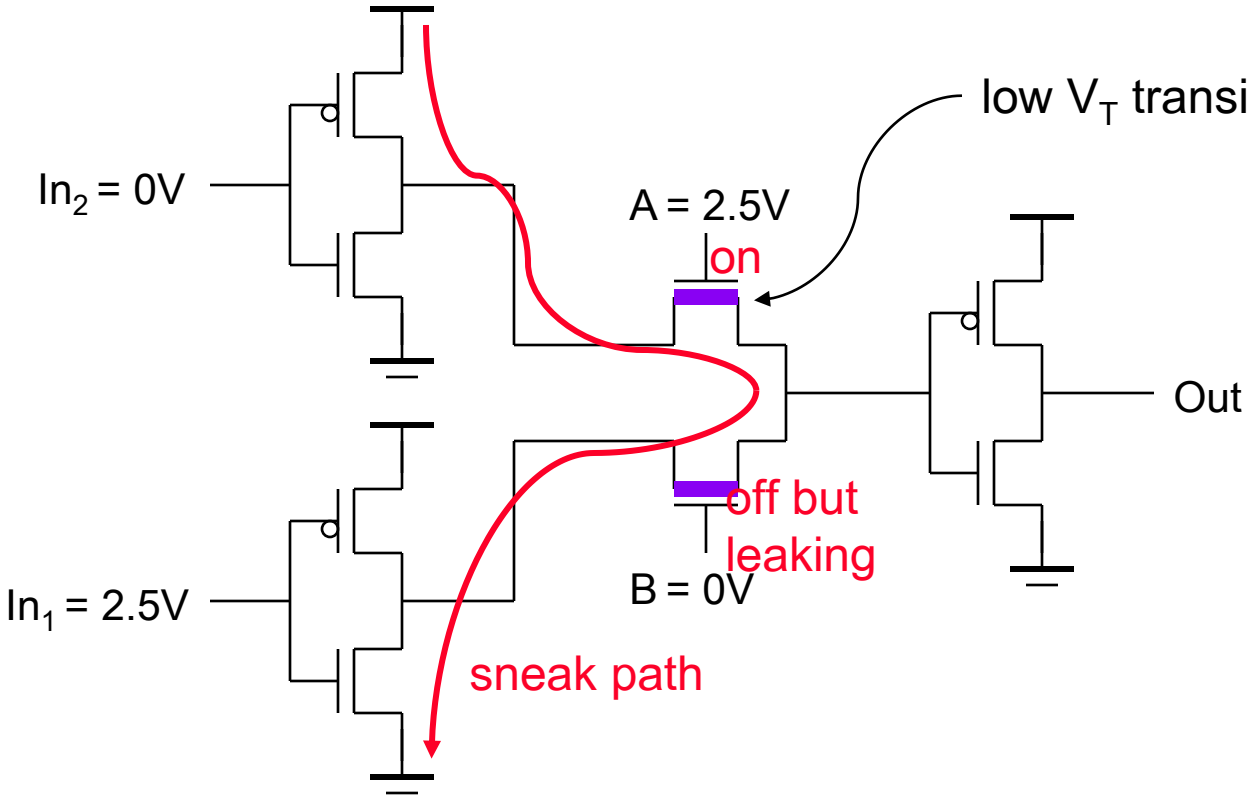
Transient Level Restorer Circuit Response



- Restorer has speed and power impacts: increases the capacitance at x, slowing down the gate; increases t_r (but decreases t_f)

Solution 2: Multiple V_T Transistors

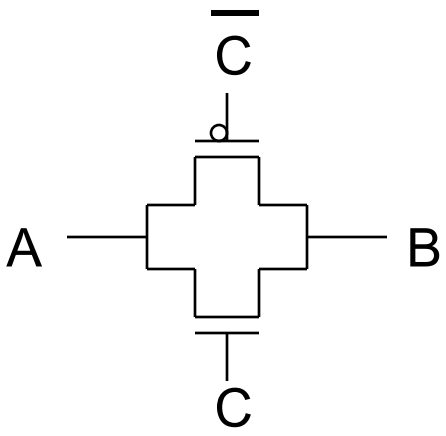
- Technology solution: Use (near) zero V_T devices for the NMOS PTs to eliminate *most* of the threshold drop (body effect still in force preventing full swing to V_{DD})

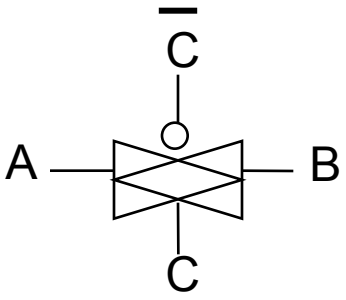


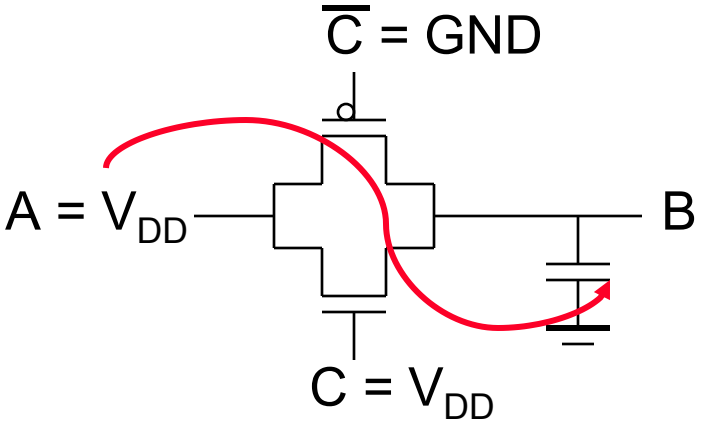
- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if V_{GS} is below V_T)

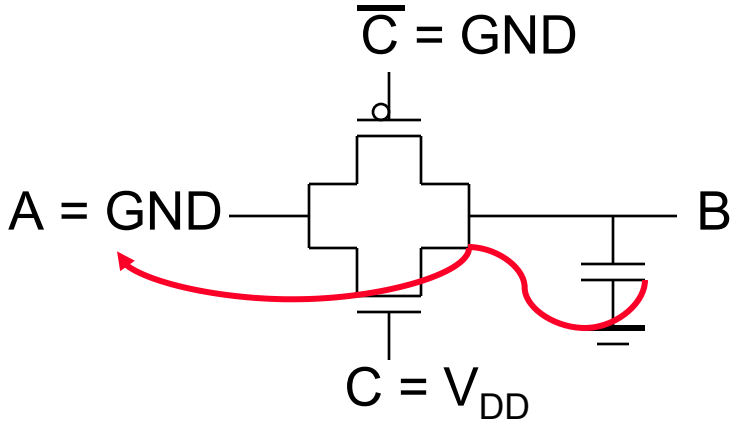
Solution 3: Transmission Gates (TGs)

- Most widely used solution



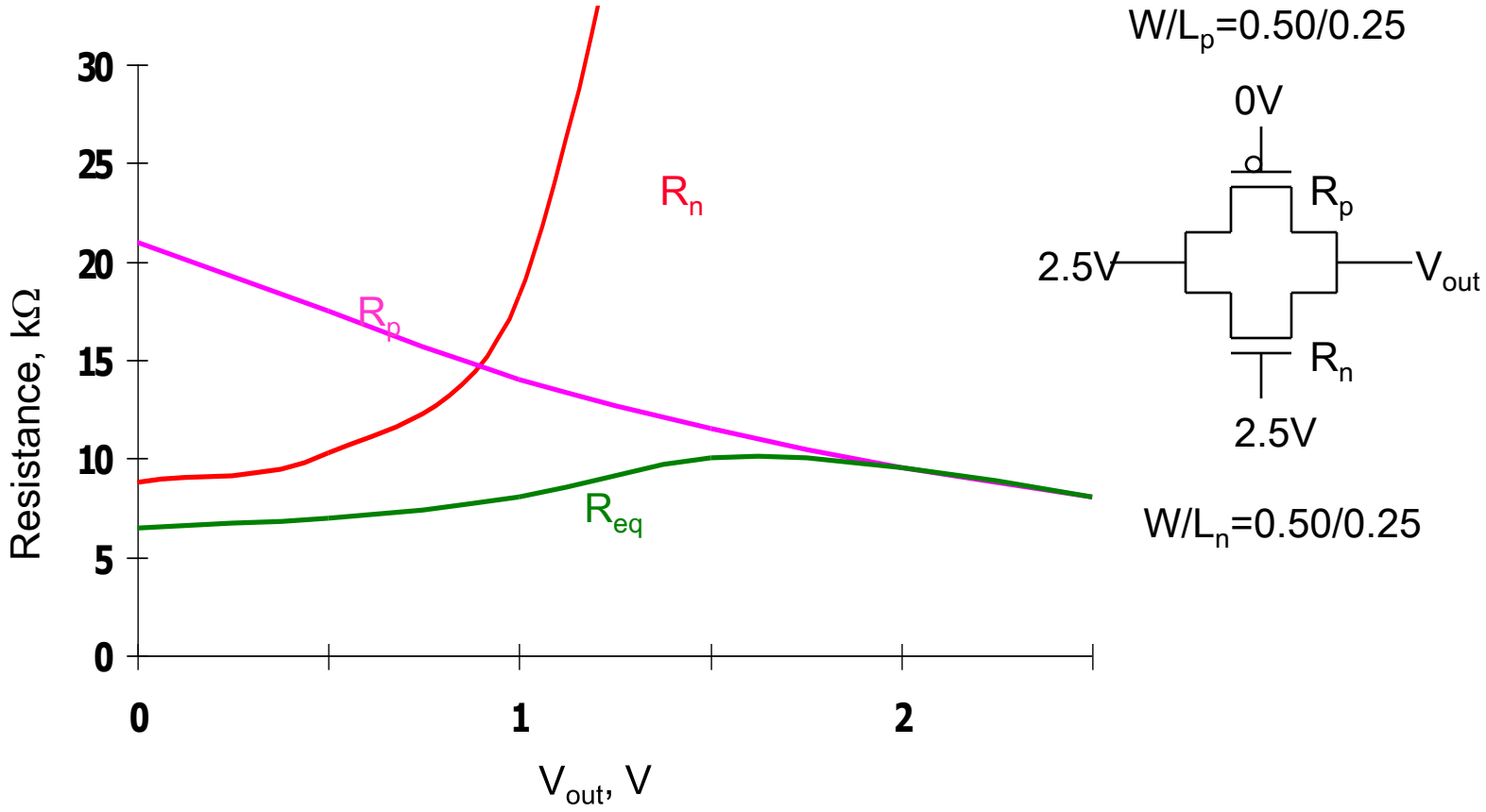




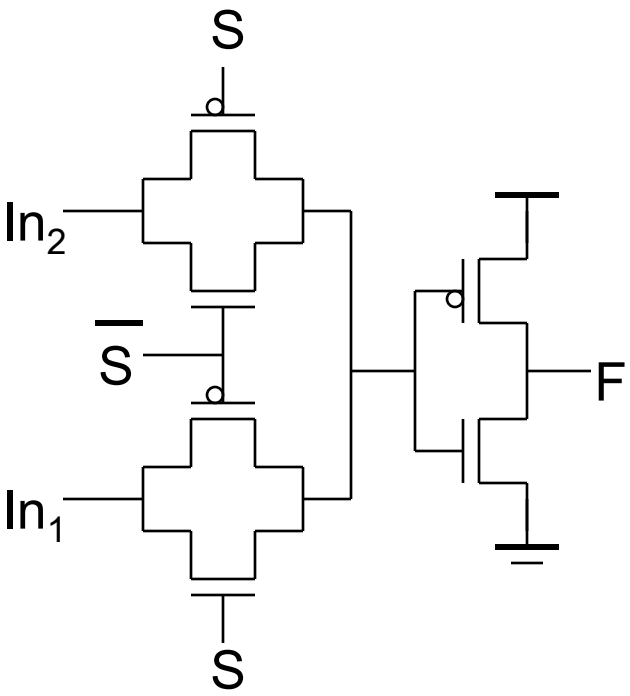


- Full swing *bidirectional* switch controlled by the gate signal C, A = B if C = 1

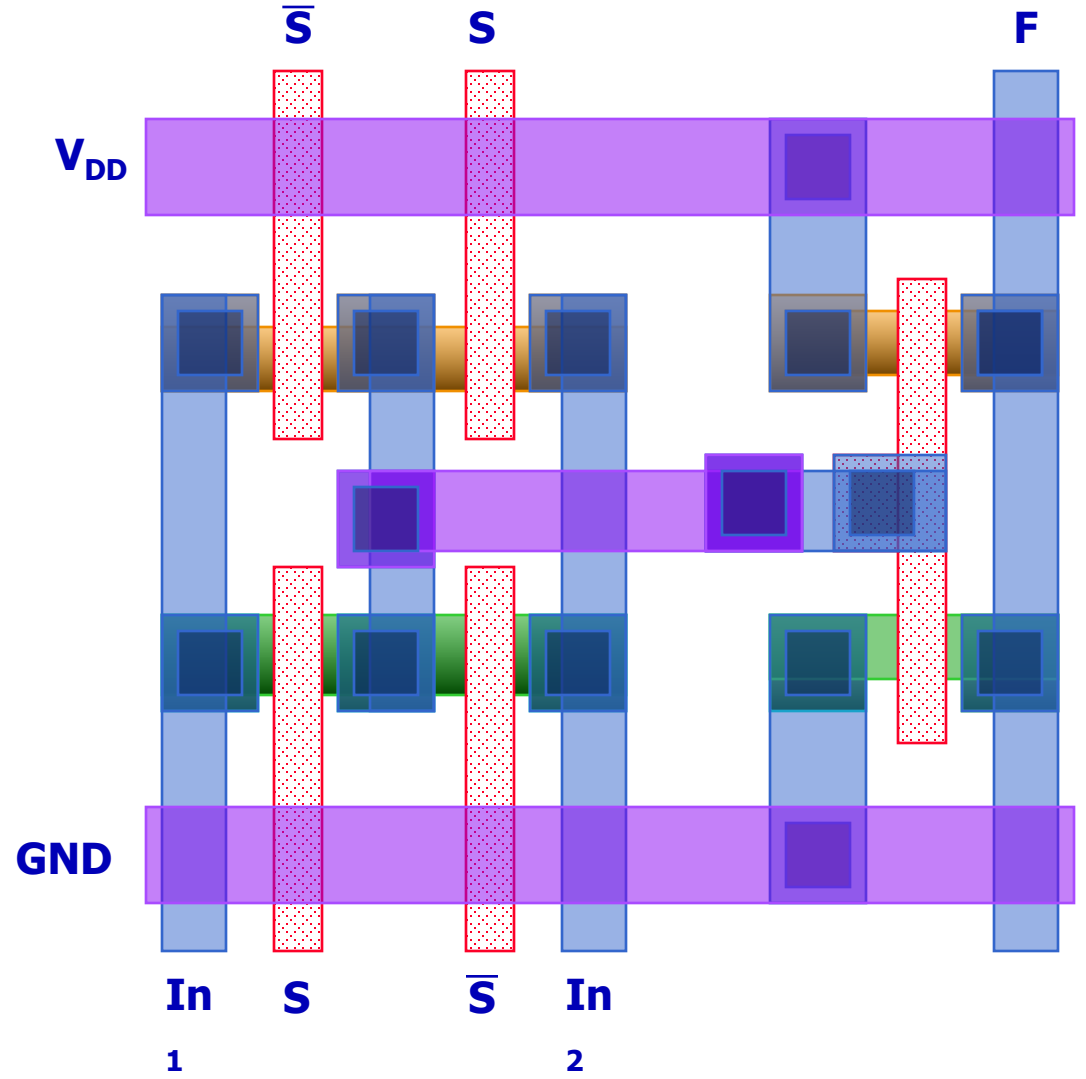
Resistance of TG



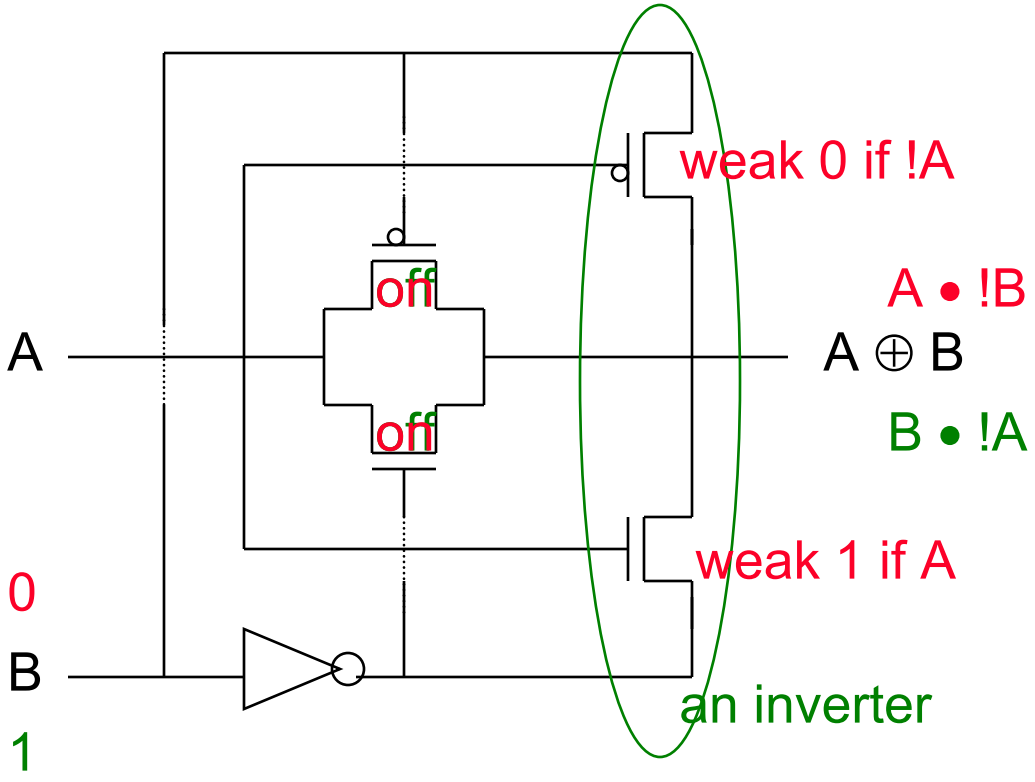
TG Multiplexer



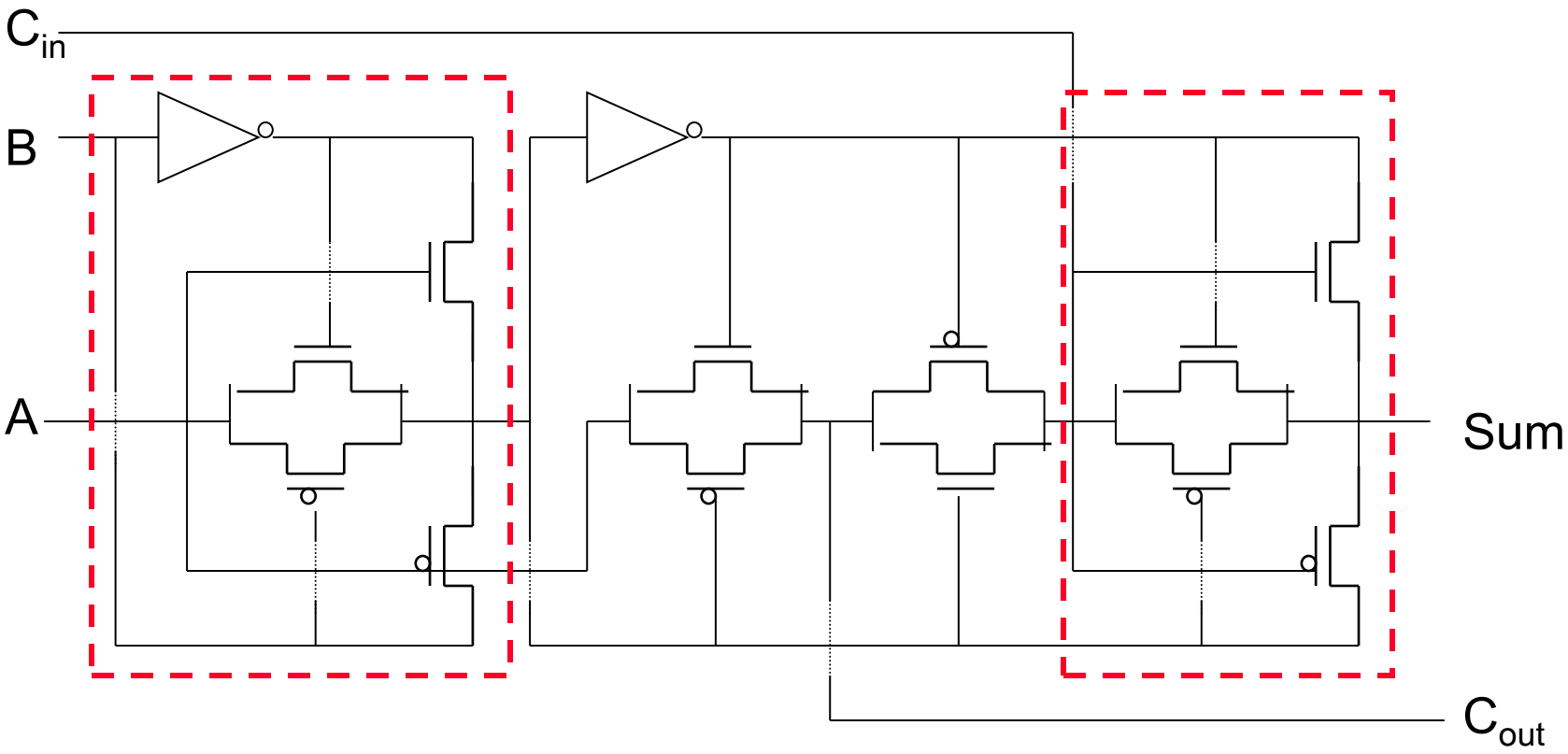
$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$



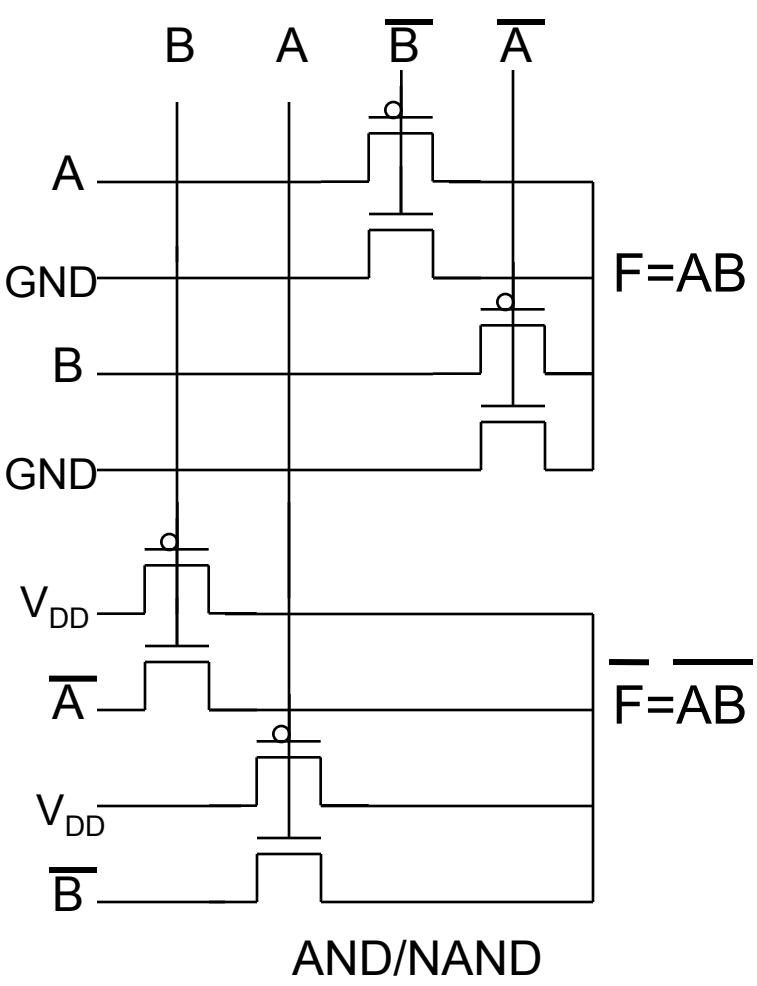
Transmission Gate XOR



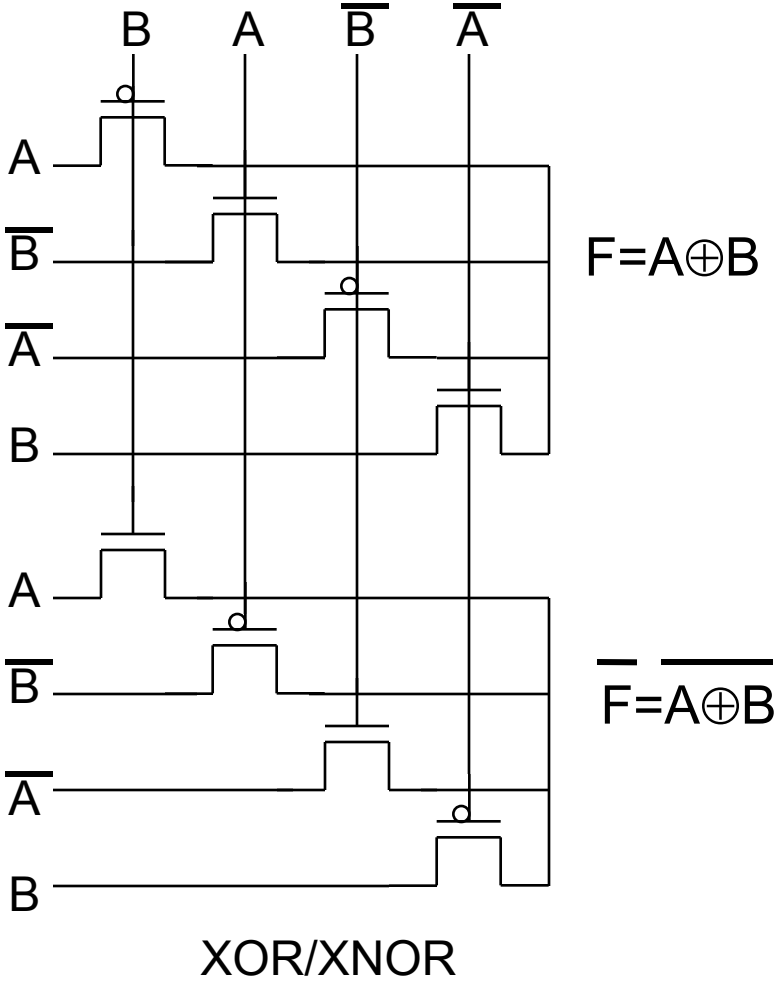
TG Full Adder



Differential TG Logic (DPL)



AND/NAND



XOR/XNOR

Next Time: The MOS Transistor

- MOS transistor dynamic behavior (R and C)
- Wire capacitance

Next Lecture and Reminders

- Next lecture
  - MOS transistor dynamic behavior
    - Reading assignment – Rabaey, et al, 3.2.3 & 3.3.3-3.3.5
  - Wiring capacitance
    - Reading assignment – Rabaey, et al, 4.1-4.3.1
- Reminders
  - Lecture 5! will be Thursday (guest lecturer)
  - Lecture 8 will be on the 24th and lectures 9+10 will be on the 26th
  - HW2 due September 24th; HW3 handed out then (due Oct 10th)
  - Evening midterm exam scheduled
    - Wednesday, October 16th from 8:15 to 10:15pm in 260 Willard
    - Only one midterm conflict filed for so far