CSE477
VLSI Digital Circuits
Fall 2002

Lecture 27: System Level Interconnect

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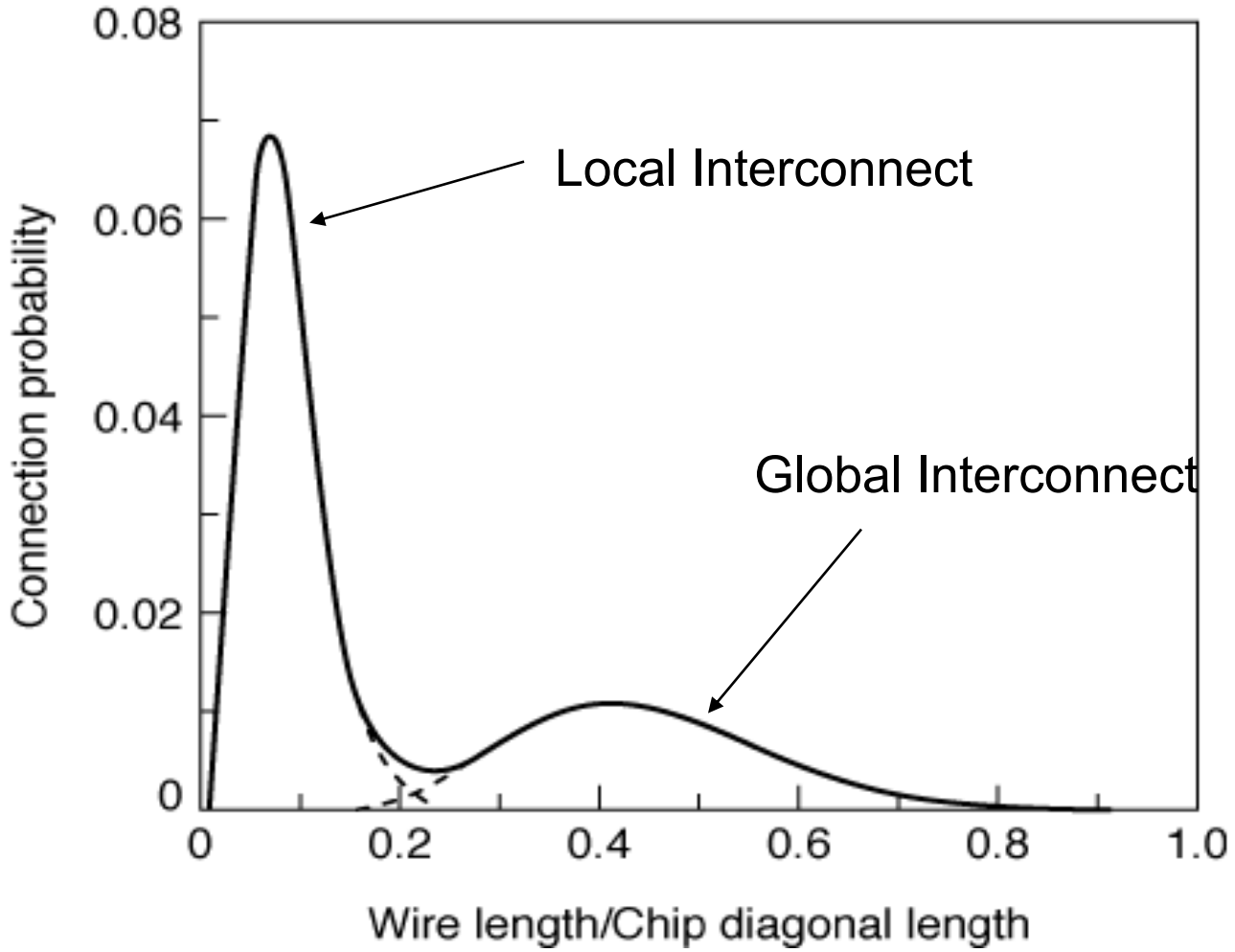
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Nature of Interconnect



Global Interconnect

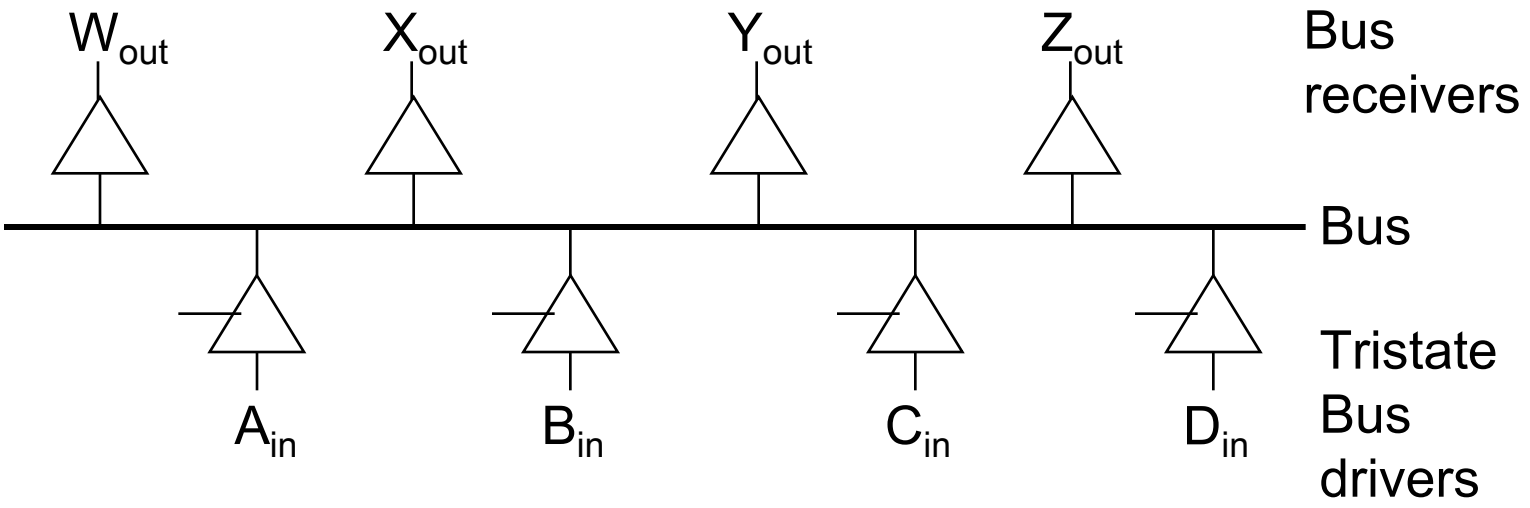
- System level signal interconnect - buses
- Vdd and Gnd planes
- System clock

Impact of Interconnect Parasitics

- Reduced reliability
- Reduced performance

- Classes of parasitics
  - capacitive
  - resistive
  - inductive

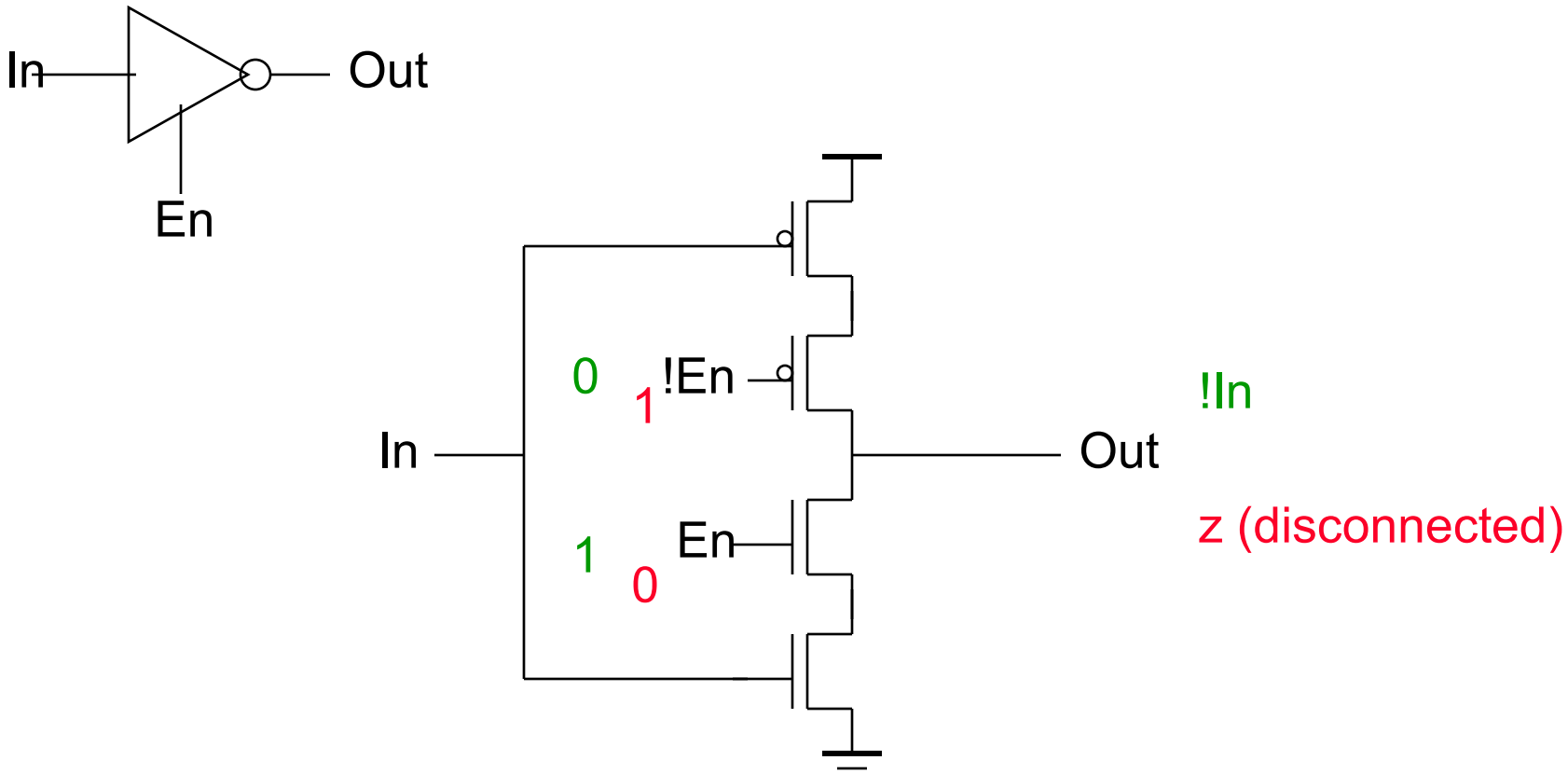
System Level Signal Interconnect



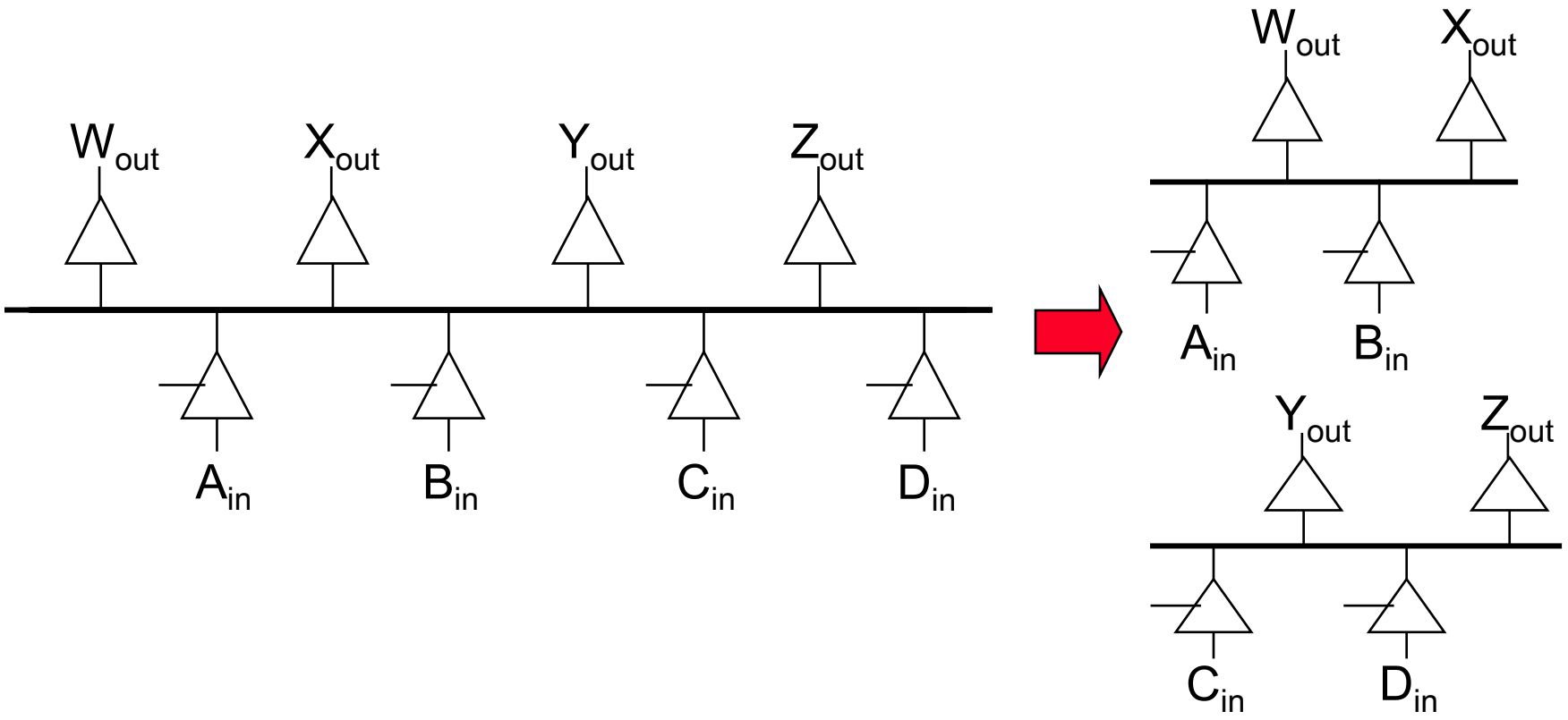
- Many drivers - only one active at a time
- Many receivers - many may be active at a time

Tristate Buffers

Three states - 0, 1, and z (high impedance)

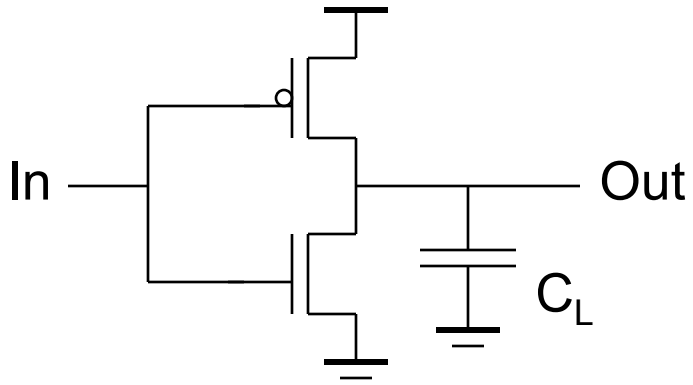


Reducing Effective Capacitance



- Shared resources may also incur extra switching activity

Driving Large Capacitances

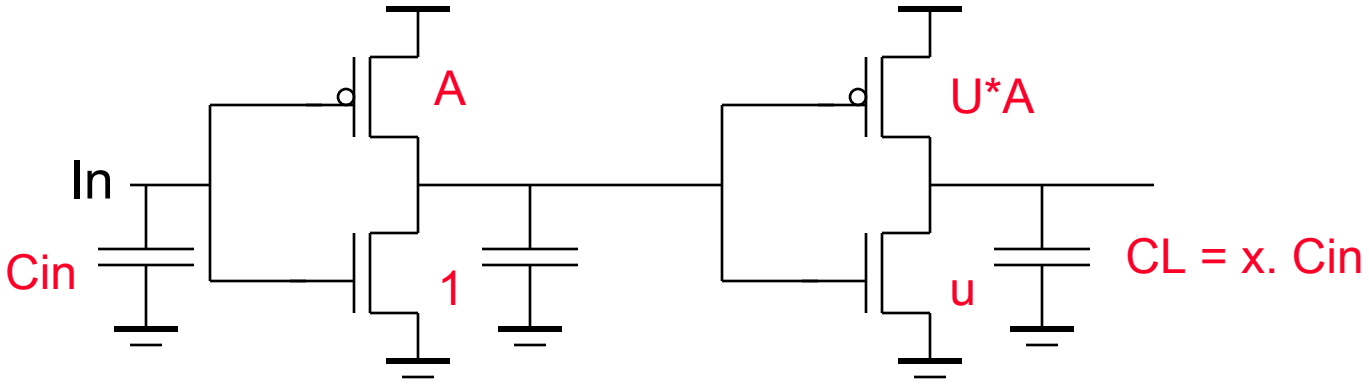


$$t_{pHL} = \frac{C_L \, V_{swing/2}}{I_{av}}$$

Increase with transistor sizing

$I_D = k'/2 \; W/L \; (\ldots)$

Single Inverter as buffer



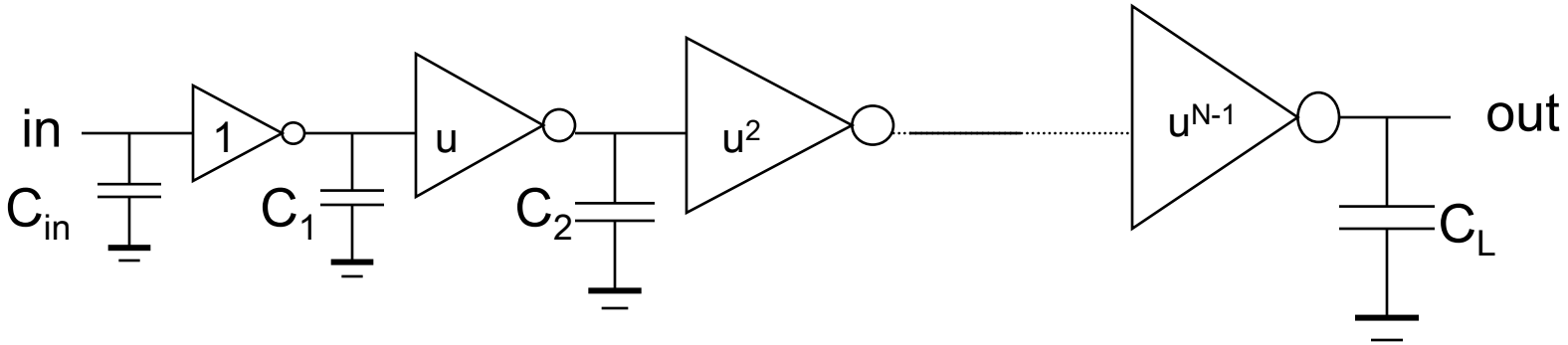
Total propogation delay = tp(inv) + tp(buffer)

tp0 - delay of minimum sized inverter with single minimum sized inverter for fanout

tp = u. tp0 + x/u tp0

uopt = sqrt(x); tp,opt = 2 tp0. Sqrt(x)

Use Cascaded Buffers



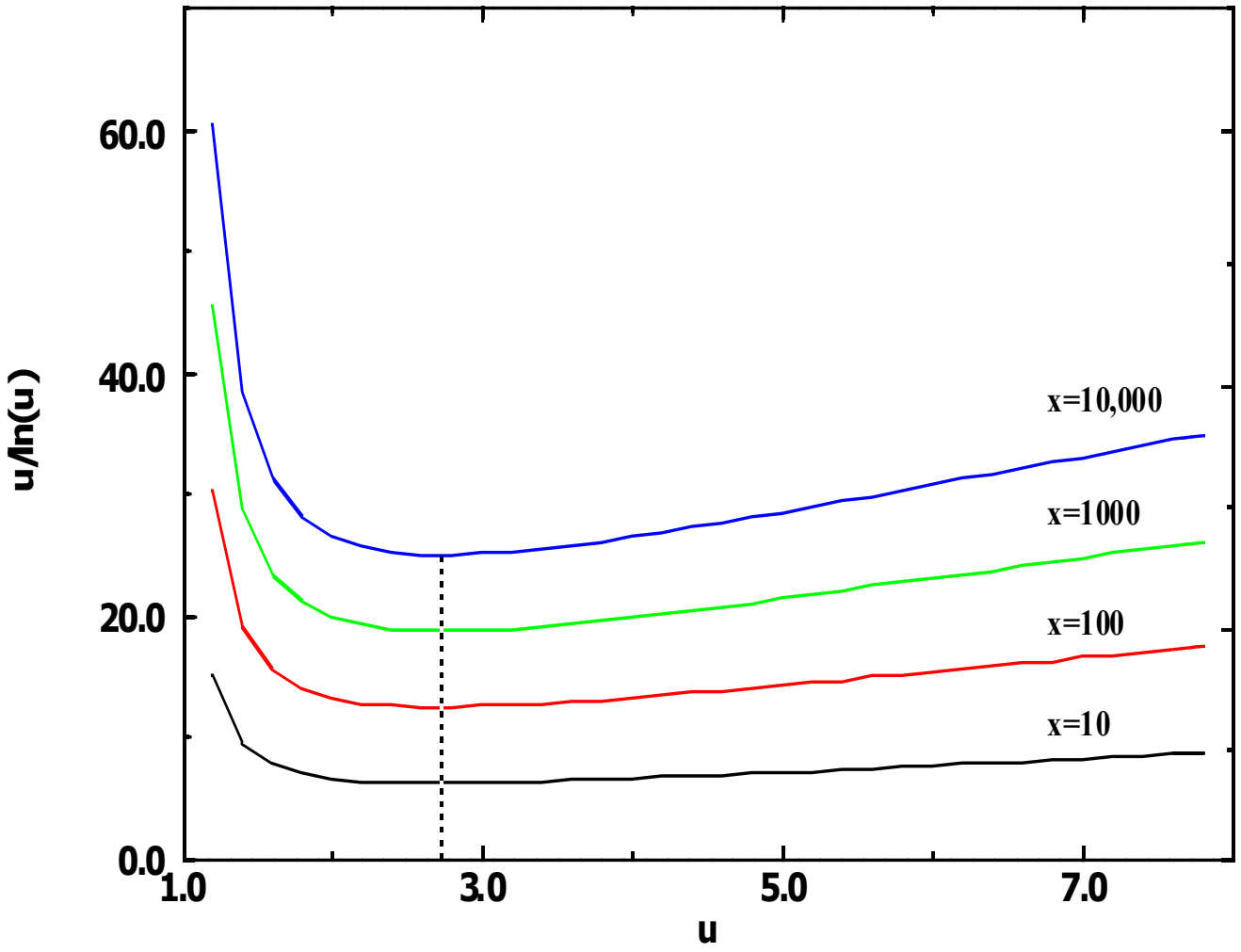
3 9 27 81

1 3 9 27

$C_L = xC_{in} = u^N C_{in}$

$u_{opt} = e$

t_p as a Function of u and x



Impact of Cascading Buffers

x	Unbuffered	Single Buffer	Cascaded Buffers
10	10	6.3	6.3
100	100	20	12.5
1,000	1,000	63	18.8
10,000	10,000	200	25

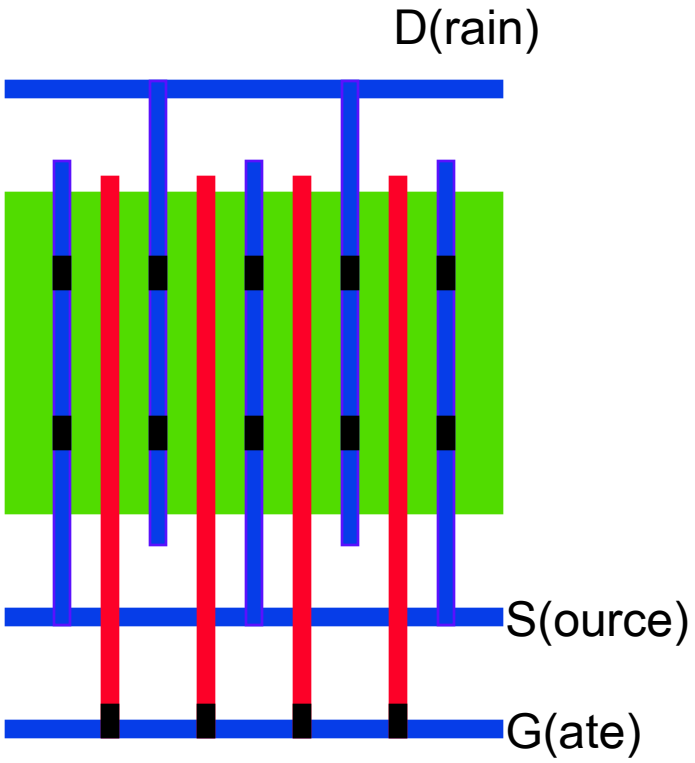
chip bus

I/O pads

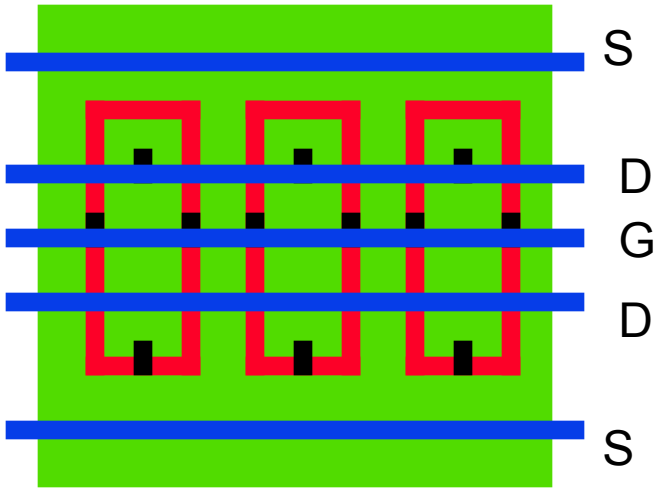
t_{opt}/t_{p0} versus x for various driver configurations

C_{in} = 10 fF in 1 micron CMOS

Designing Large Transistors



Small transistors in parallel

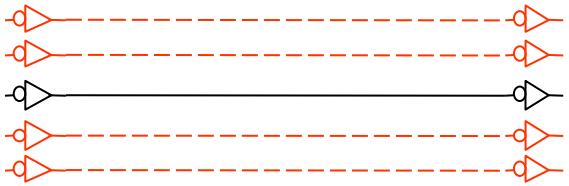


Circular transistors

Capacitive Coupling (Crosstalk)

- Signal wire glitches as large as 80% of the supply voltage will be common due to crosstalk between neighboring wires as feature sizes continue to scale

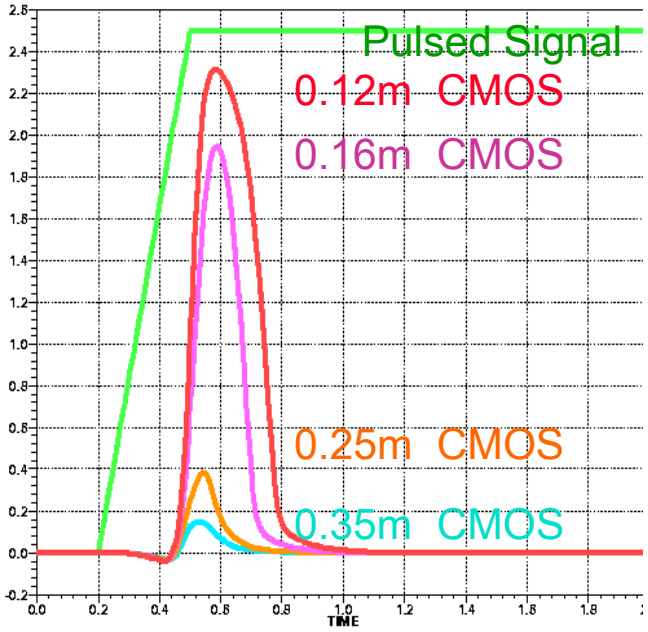
Crosstalk vs. Technology



Black line quiet

Red lines pulsed

Glitches strength vs technology

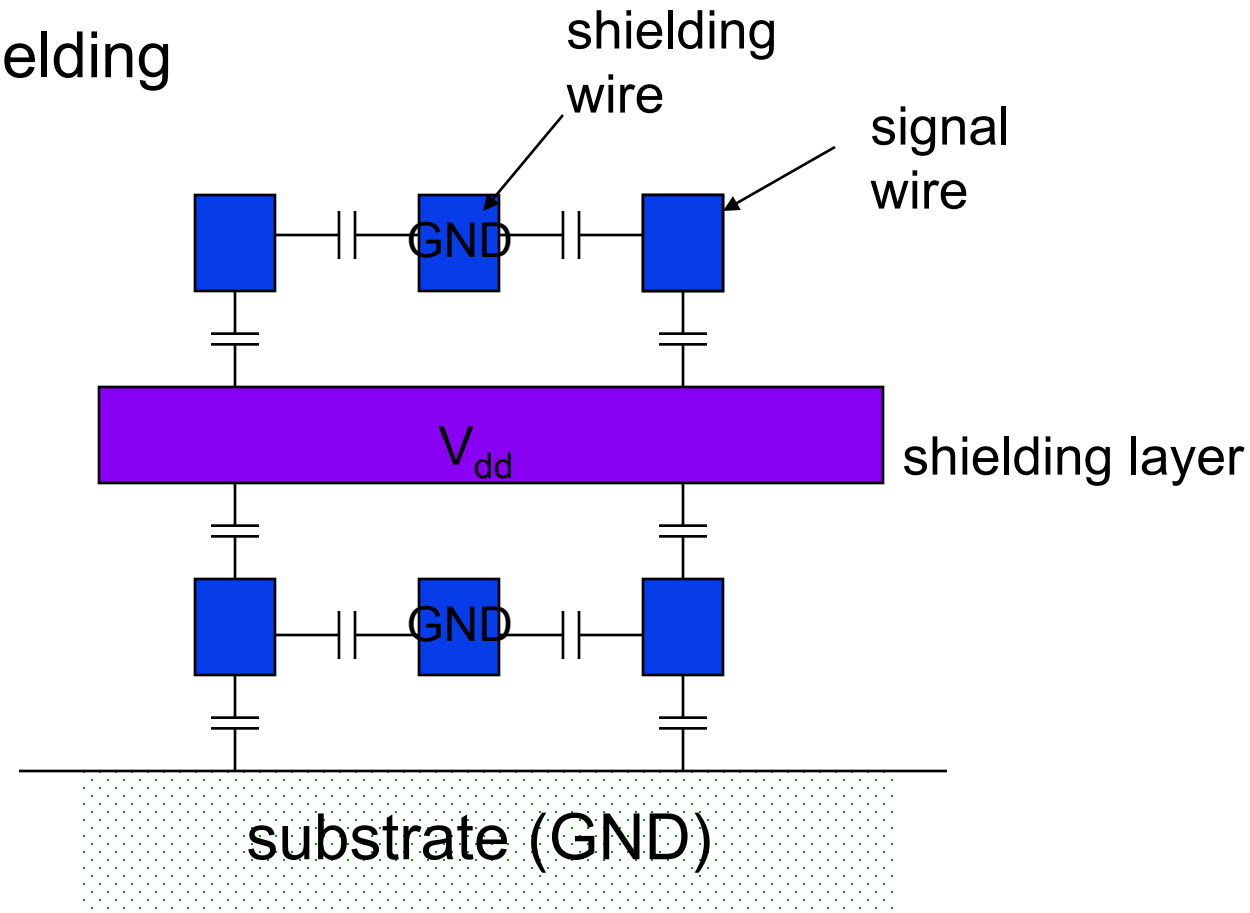


From Dunlop, Lucent, 2000

Battling Capacitive Crosstalk

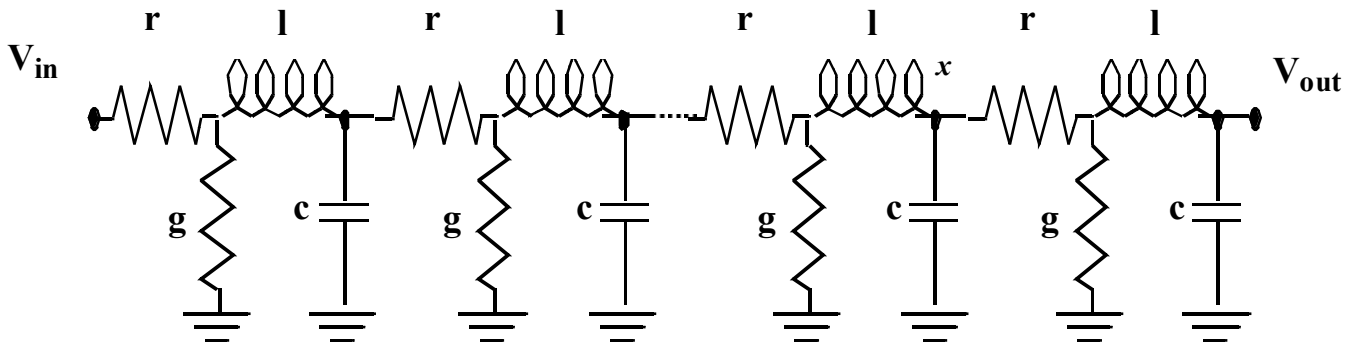
- Avoid parallel lines

- Use shielding



Inductive Effects

- When wires are sufficiently long or circuits are sufficiently fast, inductance of the wire starts to dominate the delay behavior



- Must consider wire transmission line effects
  - Wave mode instead of diffusion equations used so far
  - Signal alternately transfers energy from capacitive to inductive modes

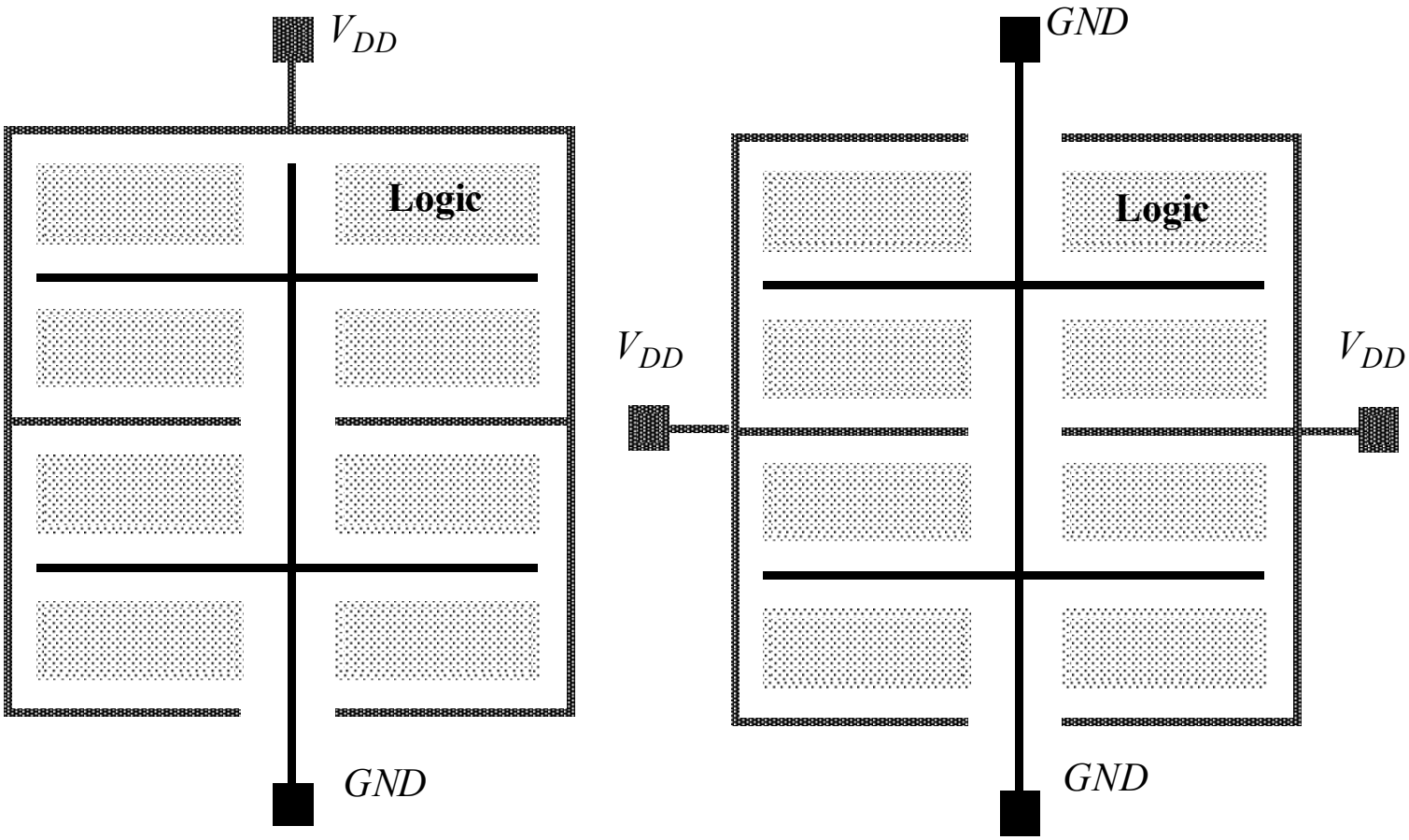
Transmission Line Considerations

- Transmission line effects should be considered when the rise or fall time of the input signal is smaller than the time-of-flight of the transmission line

Rule of Thumb

$$t_r \ (t_f) < 2.5\, t_{flight} = 2.5\, L/v$$

Power and Ground Distribution



(a) Finger-shaped network

(b) Network with multiple supply pins

Next Lecture and Reminders

- Next lecture
  - Design for test
    - Reading assignment – Rabaey, et al, xx
- Reminders
  - Project final reports due today
  - Final grading negotiations/correction (except for the final exam) must be concluded by December 10th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in 118 and 121 Thomas