
CSE477

VLSI Digital Circuits

Fall 2002

Read Me

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

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- ❑ Vijay Narayanan and Mary Jane Irwin also ask that you acknowledge our (considerable) efforts in some way. One way is to acknowledge that your slides are adapted from ours on the first slide of each set of slides - or to retain our copyright.

Course Details

- ❑ The slides are for a 15 week (full semester) senior and early graduate level course in computer science and engineering. It is taken by undergraduate computer engineering majors, graduate computer science and engineering majors, and both undergraduate and graduate electrical engineering majors.
- ❑ The course, CSE 477, covers topics in VLSI digital circuits (Digital integrated circuit design, layout, simulation, and fabrications; VLSI design techniques and system architecture; computer-aided design tools and techniques).
- ❑ The course prerequisites are a senior undergraduate level switching theory and logic design of digital circuits course and a junior level electronic circuit design course (properties of fundamental electronic devices, analysis of DC, C, small-signal and nonlinear behavior, analog and digital circuit design applications).

Course Structure

- ❑ The course at Penn State differs in style and structure from that taught at UCB. The course at PSU is a design intensive course - students get their first design project the first week of class. Thus, we cover the material somewhat out of order at the beginning of the semester to give the students the information they need to get started designing circuits. The (rough) outline we use is on the next slide.
- ❑ Tools used currently are *max* and *sue* (from MMI, bought by Juniper Networks). These tools are, unfortunately, no longer being distributed by Juniper. They are a modern day version of the old magic tool set. We also use HSPICE from Synopsys for circuit level simulation. All designs are done in 0.25 micron (with a nominal supply voltage of 2.5V).
- ❑ A significant design project (in teams of two) is assigned during the semester.

Course Outline

Wk	Topic	D/C Reading	HW
1	Introduction, design metrics	1	HW1
2	MOS transistors, CMOS inverters – the static view	3.1-3.3.2 & 5.1-5.3	
3	Manufacturing process, Static CMOS logic	2.1-2.3 & 6.1-6.2.1	HW2
4	Pass transistor logic, MOS transistor C and R	6.2.3 & 3.3.3-3.3.5	
5	The wire	4	HW3
6	CMOS inverter – the dynamic view	5.4-5.7	
7	Catch-up, review and midterm examination	Midterm exam week	HW4
8	Dynamic CMOS logic, Timing metrics	6.3-6.5 & 7.1	
9	Static and dynamic sequential circuits	7.2-7.3 & 7.5	
10	Coping with interconnect	9	HW5
11	Timing issues, Datapaths	10.1-10.3.3 & 11.1-11.2	
12	Adders, Multipliers, Shifters	11.3-11.9	
13	Other arith. op's, Memory classes and ROM cores	11.7-11.9 & 12.1-12.2.1	
14	SRAM, DRAM, CAM cores, Memory peripheral circuitry	12.2.2-12.5	
15	Design for test, Tech. trends and scaling issues	H & 2.5, 3.5, 4.6, 5.6	

Keeping Your Students Awake and Involved

- ❑ Throughout the set of slides, you will often see two slides that are almost identical. One is for the class handout and is missing some key points (it is marked in the notes section as “for class handout”). The other is for lecture (marked “for lecture”) where the key points are included and are animated to appear as students respond to questions posed to them in class.
 - Put the “for lecture” slide in hide mode when preparing class handouts and the “for class handouts” in hide mode when preparing lectures
 - A sample pair of slides follows
- ❑ Note that the graphs from *D/C* have been converted into powerpoint graphs so that they could be animated effectively. The data used to construct the graph is only *approximate*; it was constructed to make the graphs as similar to the graphs in *D/C* as possible (given the considerable limitations of ppt).
- ❑ The notes section contains backup for each slide from *D/C*.

CMOS Inverter VTC

