CSE477
VLSI Digital Circuits
Fall 2002

Lecture 18: Dynamic Sequential Circuits

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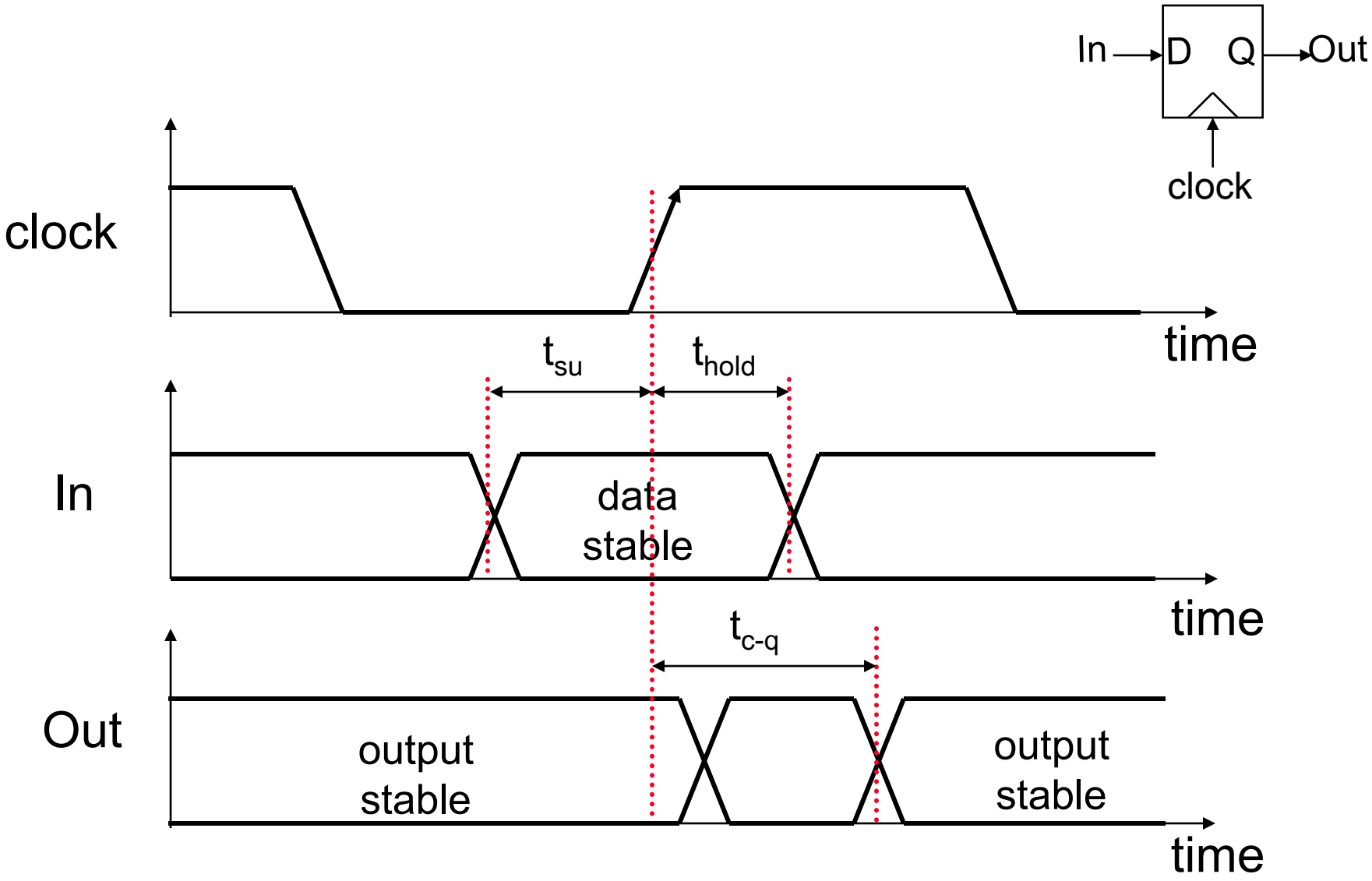
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

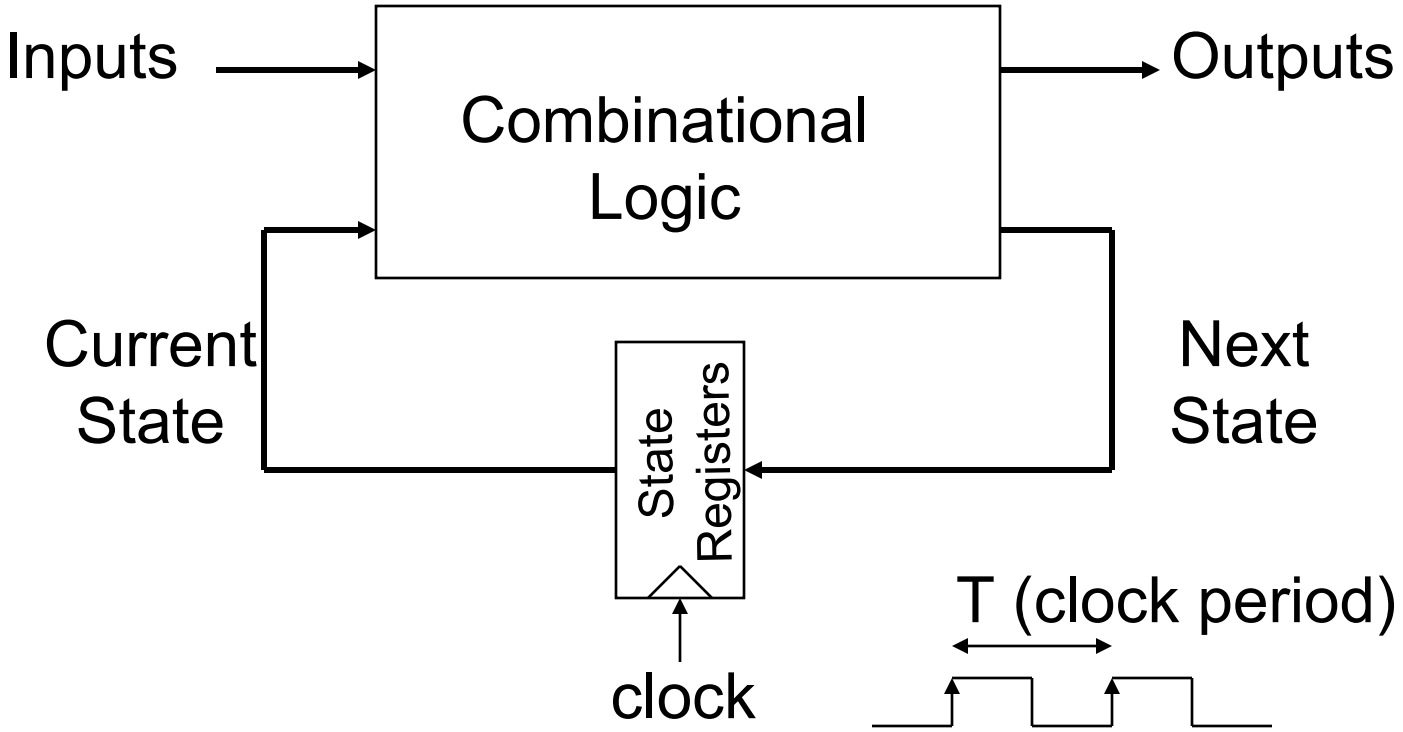
Review: Sequential Definitions

- Static versus dynamic storage
  - static uses a bistable element with feedback (regeneration) and thus preserves its state as long as the power is on
  - static is preferred when updates are infrequent (clock gating)
  - dynamic stores state on parasitic capacitors so only holds the state for a period of time (milliseconds) and requires periodic refresh
  - dynamic is usually simpler (fewer transistors), higher speed, lower power
- Latch versus flipflop
  - latches are level sensitive with two modes: transparent - inputs are passed to Q and hold - output stable
  - fliplflops are edge sensitive that only sample the inputs on a clock transition

Review: Timing Metrics



Review: System Timing Constraints



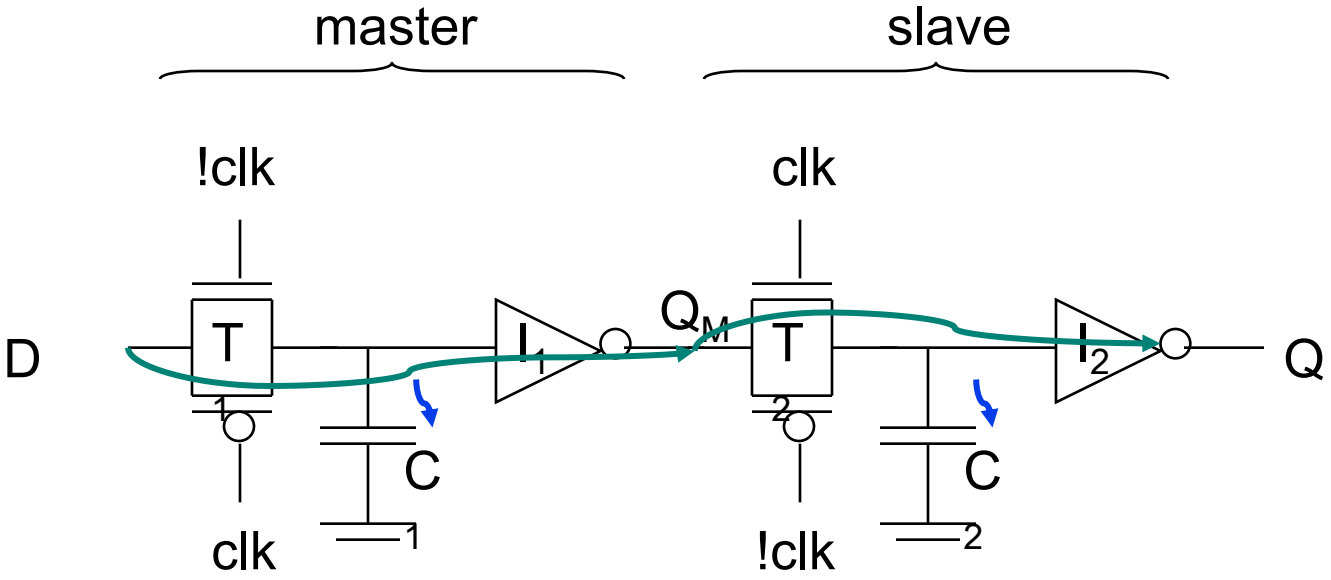
$$t_{cdreg} + t_{cdlogic} \geq t_{hold}$$

$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

You spend all this time designing one machine and it's only a hot box for two years, and it has all the useful life of a washing machine.

The Soul of a New Machine, Kidder, pg. 239

Dynamic ET Flipflop

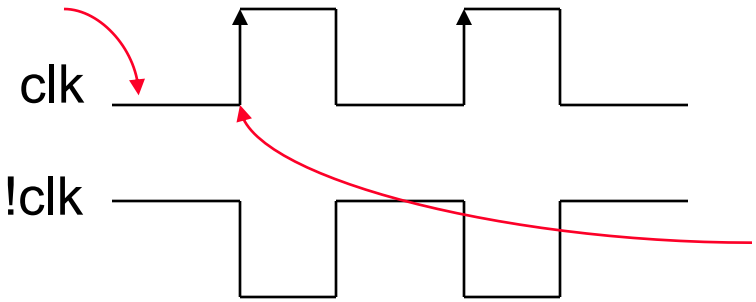


$t_{su} = t_{pd\_tx}$

$t_{hold} =$ zero

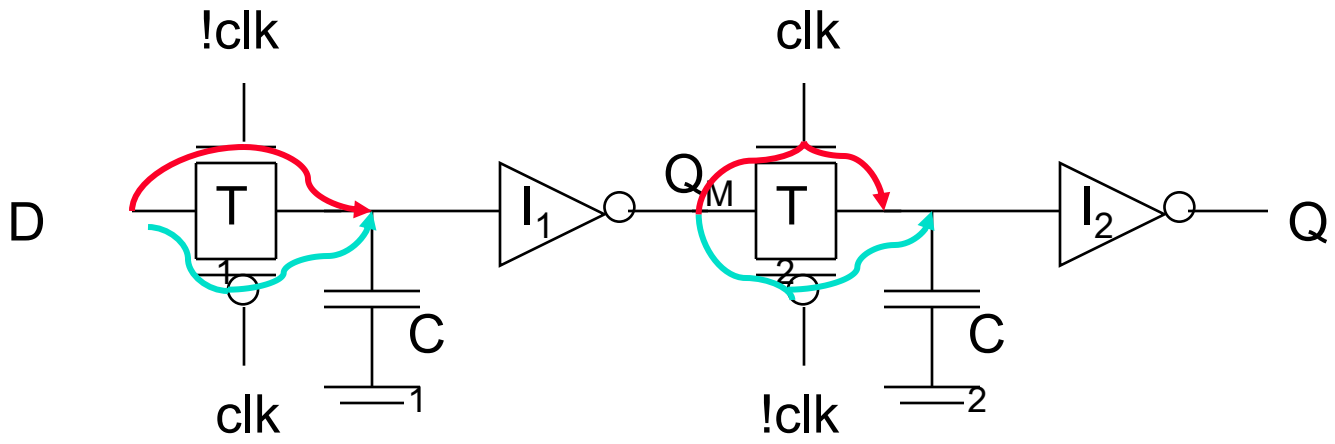
$t_{c\text{-}q} = 2\,t_{pd\_inv} + t_{pd\_tx}$

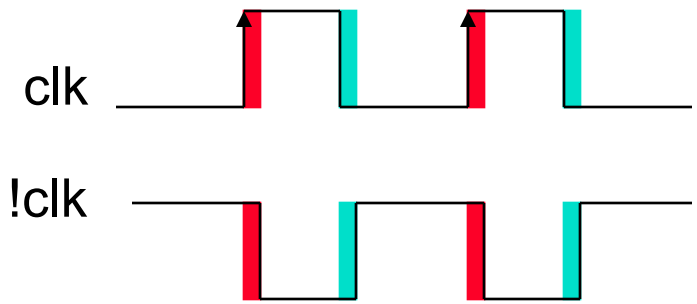
master transparent
slave hold



master hold
slave transparent

Dynamic ET FF Race Conditions





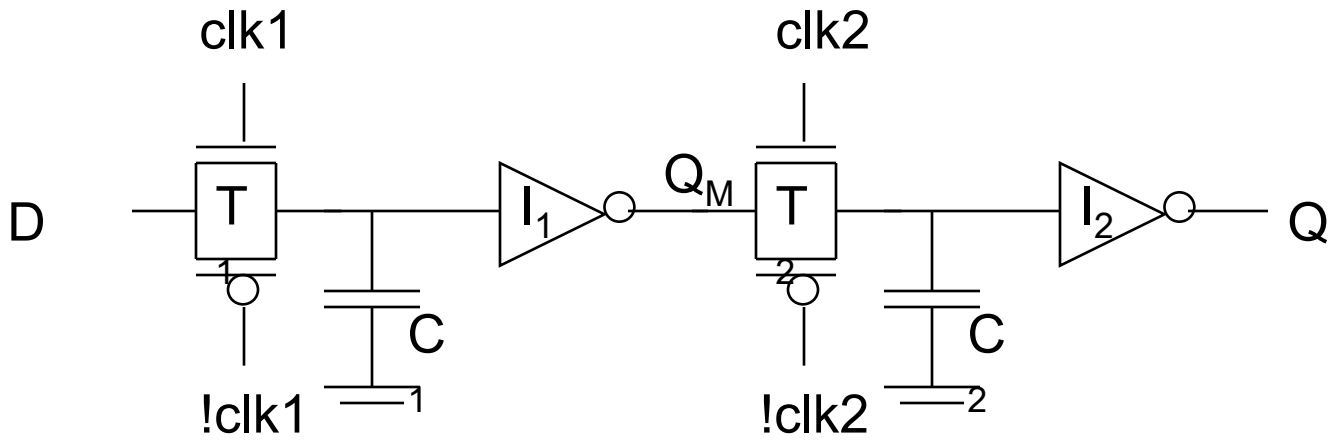
0-0 overlap race condition

$t_{overlap0\text{-}0} < t_{T1} + t_{I1} + t_{T2}$

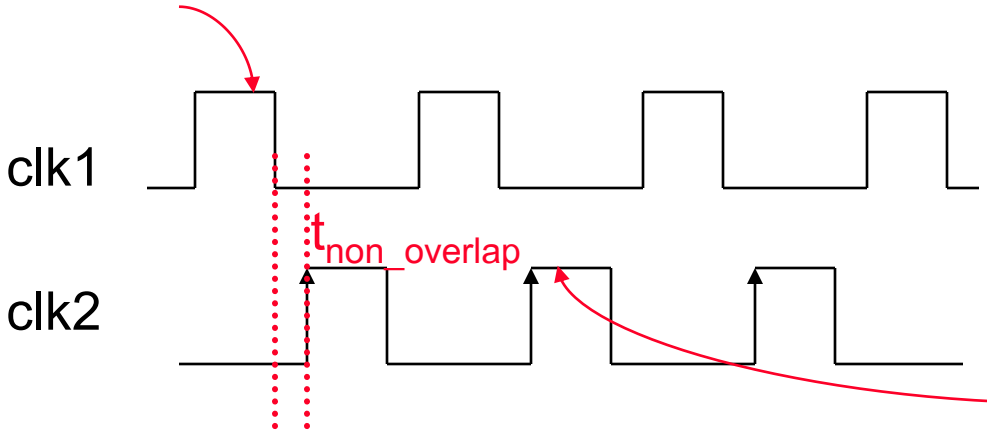
1-1 overlap race condition

$t_{overlap1\text{-}1} < t_{hold}$

Dynamic Two-Phase ET FF



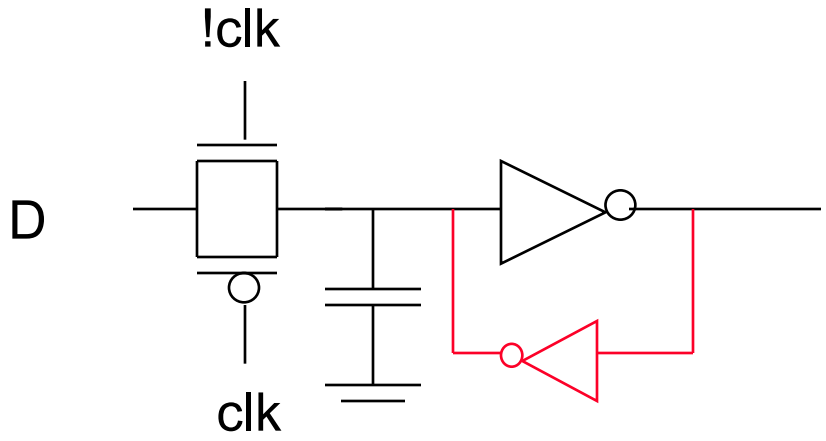
master transparent
slave hold



master hold
slave transparent

Pseudostatic Dynamic Latch

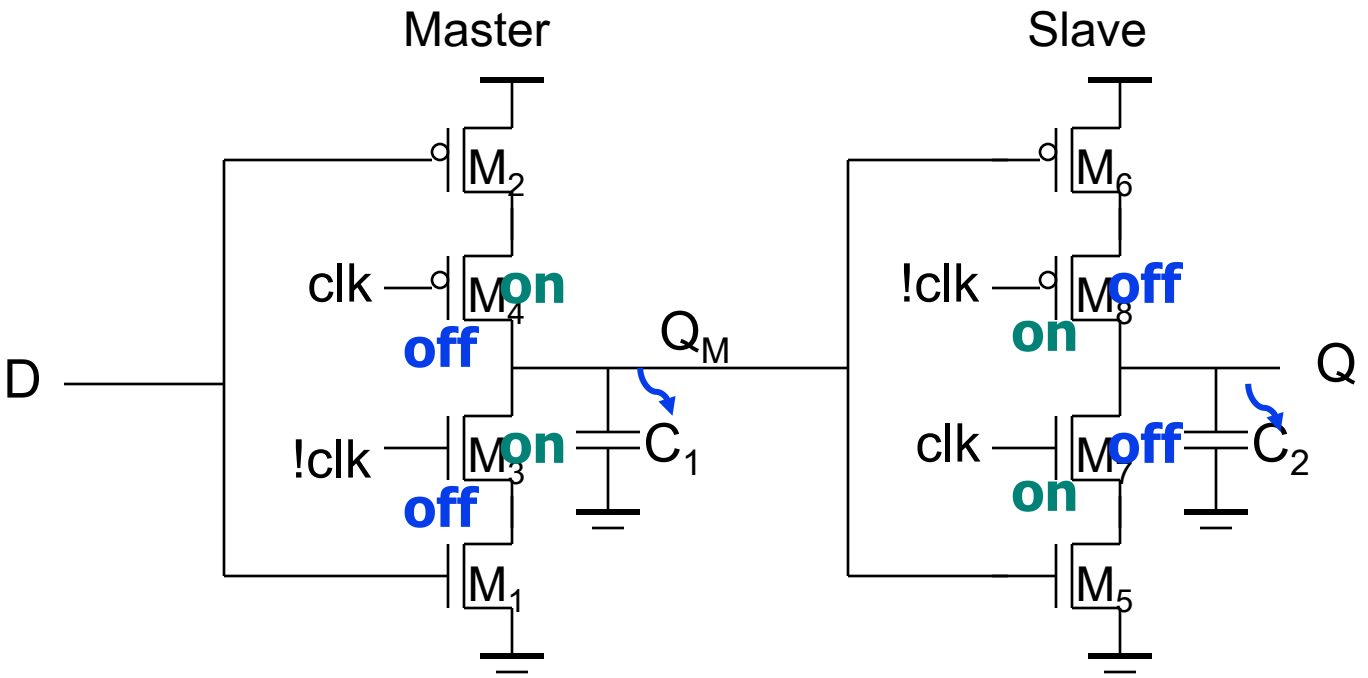
- Robustness considerations limit the use of dynamic FF's
  - coupling between signal nets and internal storage nodes can inject significant noise and destroy the FF state
  - leakage currents cause state to leak away with time
  - internal dynamic nodes don't track fluctuations in V_{DD} that reduces noise margins
- A simple fix is to make the circuit pseudostatic



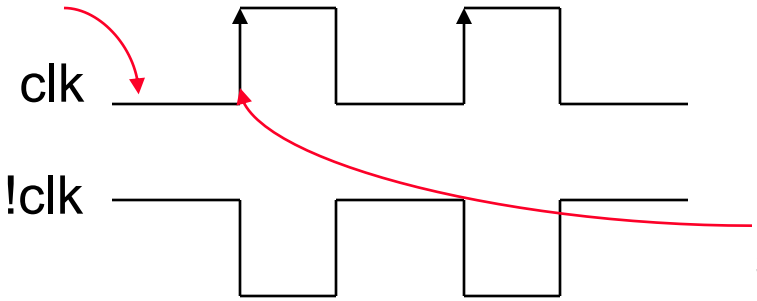
- Add above logic added to all dynamic latches

C²MOS (Clocked CMOS) ET Flipflop

- A clock-skew insensitive FF



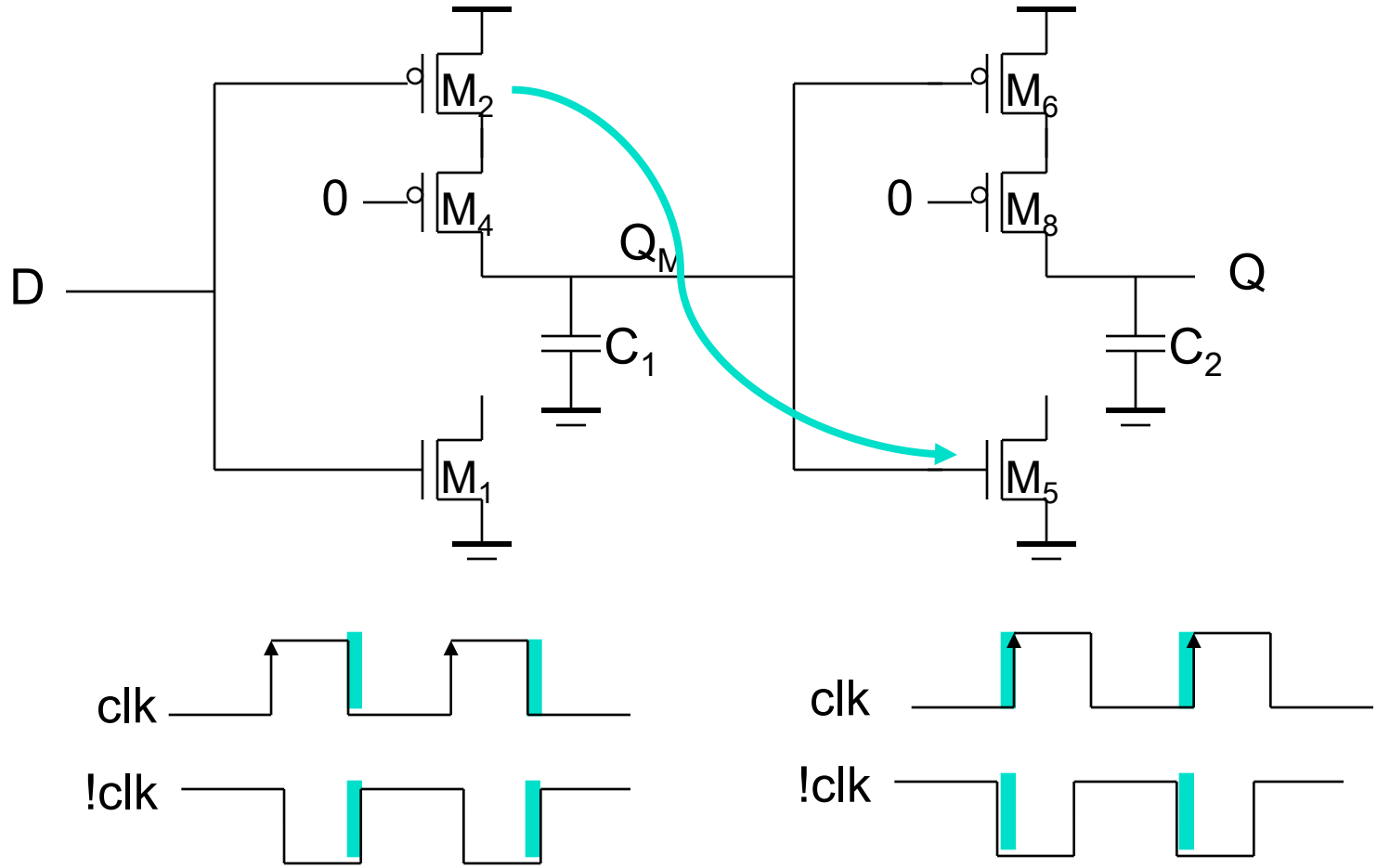
master transparent
slave hold



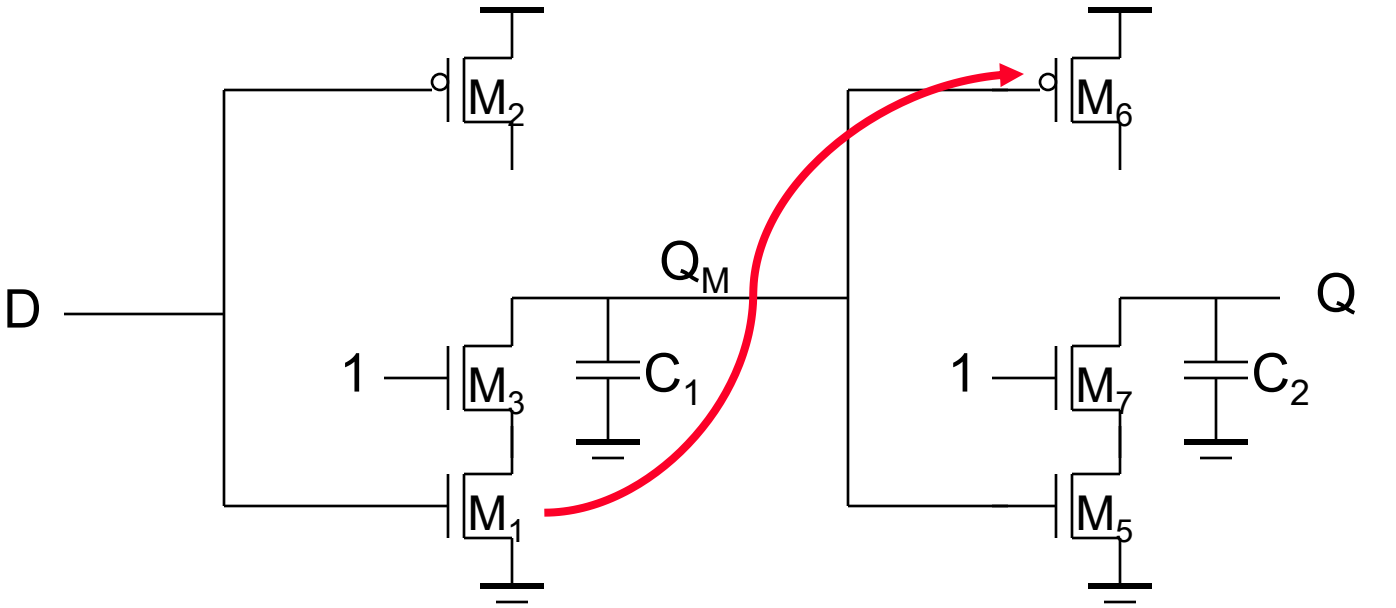
master hold
slave transparent

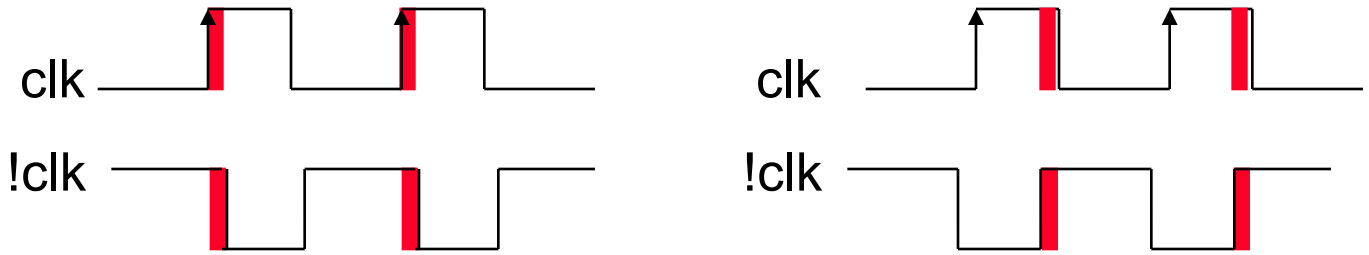
C²MOS FF 0-0 Overlap Case

- Clock-skew insensitive as long as the rise and fall times of the clock edges are sufficiently small



C²MOS FF 1-1 Overlap Case

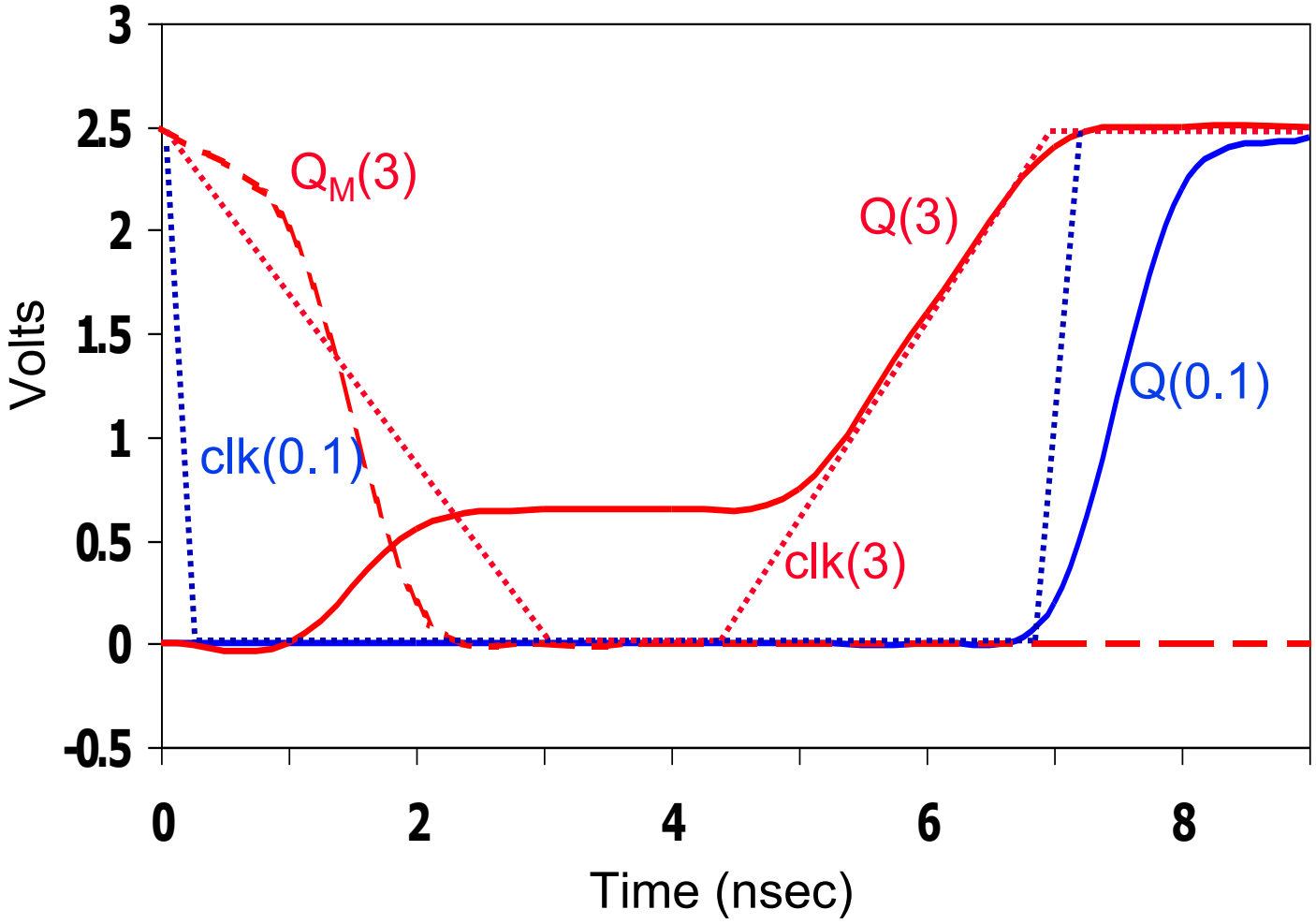




1-1 overlap constraint

$t_{overlap1\text{-}1} < t_{hold}$

C²MOS Transient Response

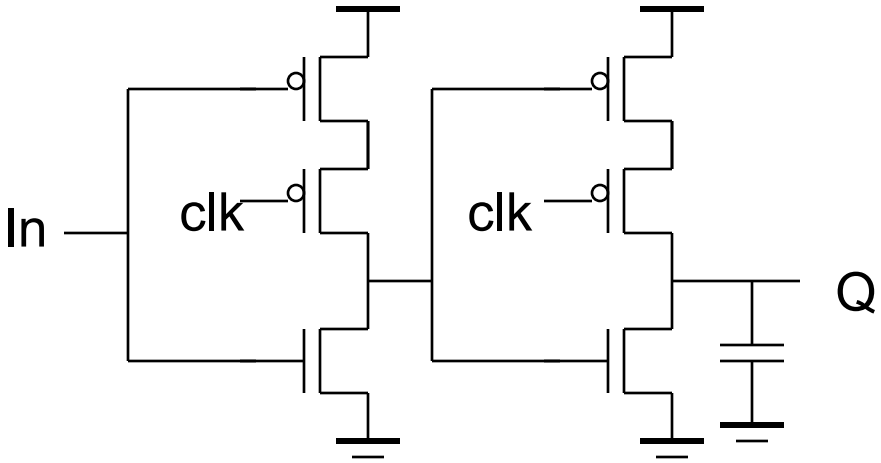


For a
0.1 ns clock

For a
3 ns clock
(race condition
exists)

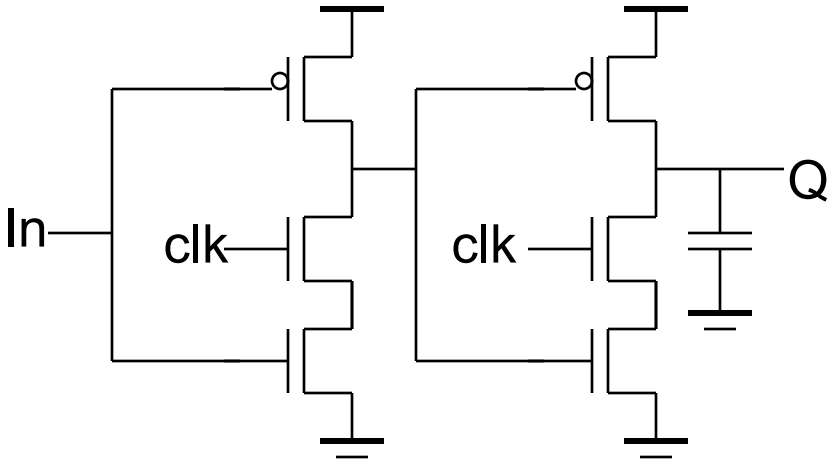
True Single Phase Clocked (TSPC) Latches

Negative Latch



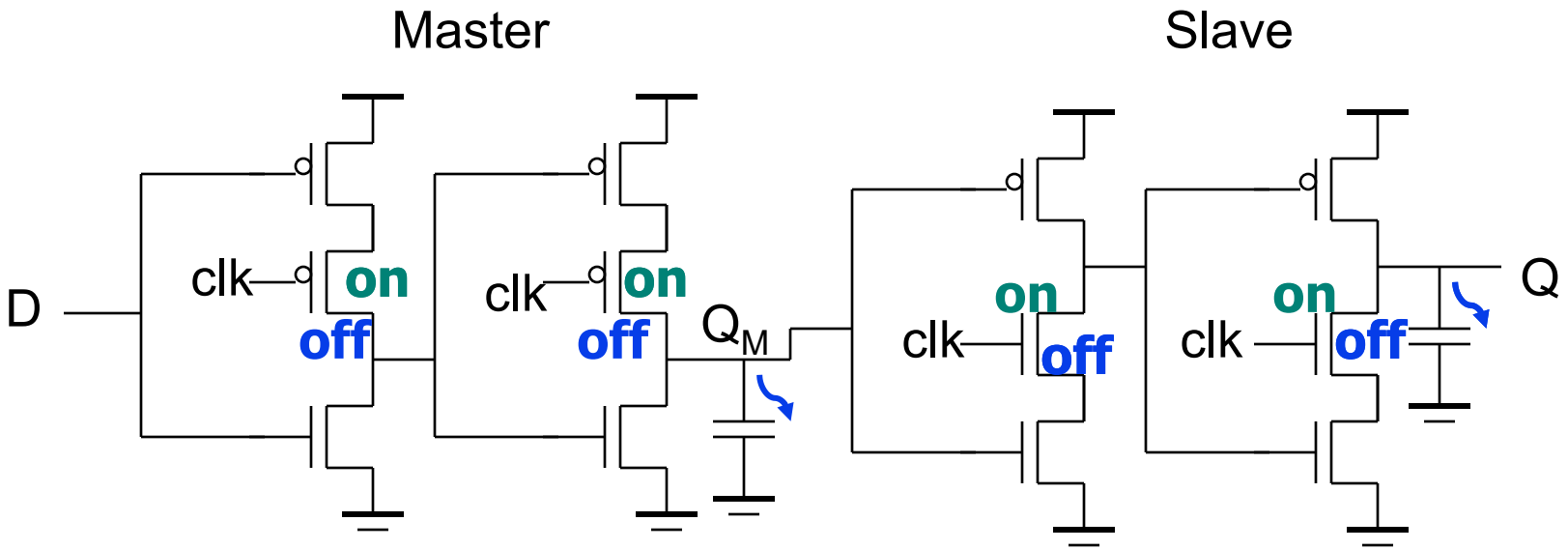
hold when clk = 1
transparent when clk = 0

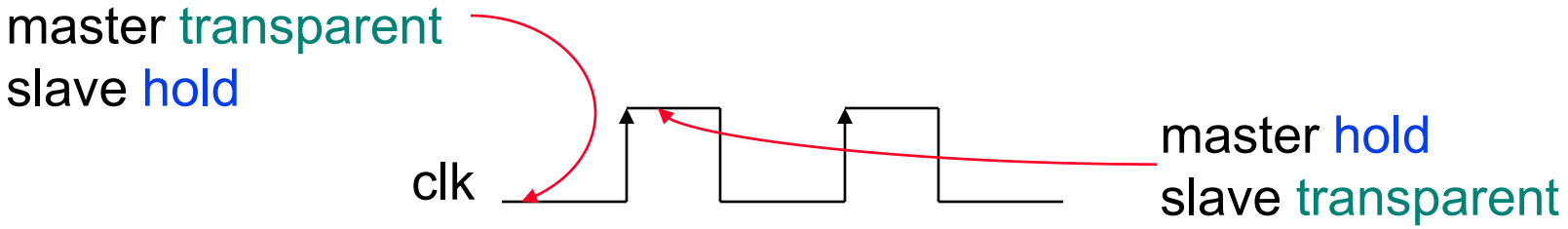
Positive Latch



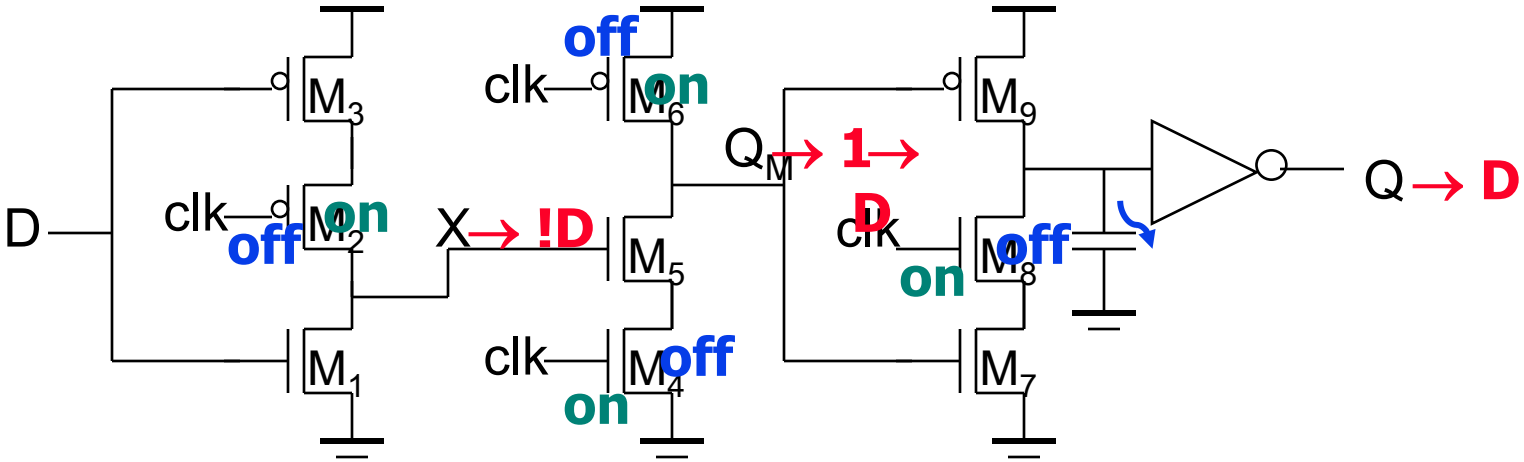
transparent when clk = 1
hold when clk = 0

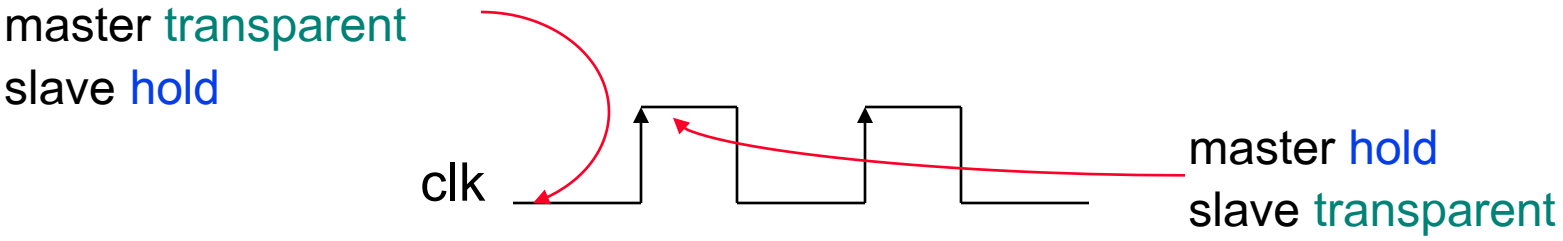
TSPC ET FF


Master
Slave
D
clk
on
off
clk
on
off
Q_M
on
clk
off
clk
on
off
Q

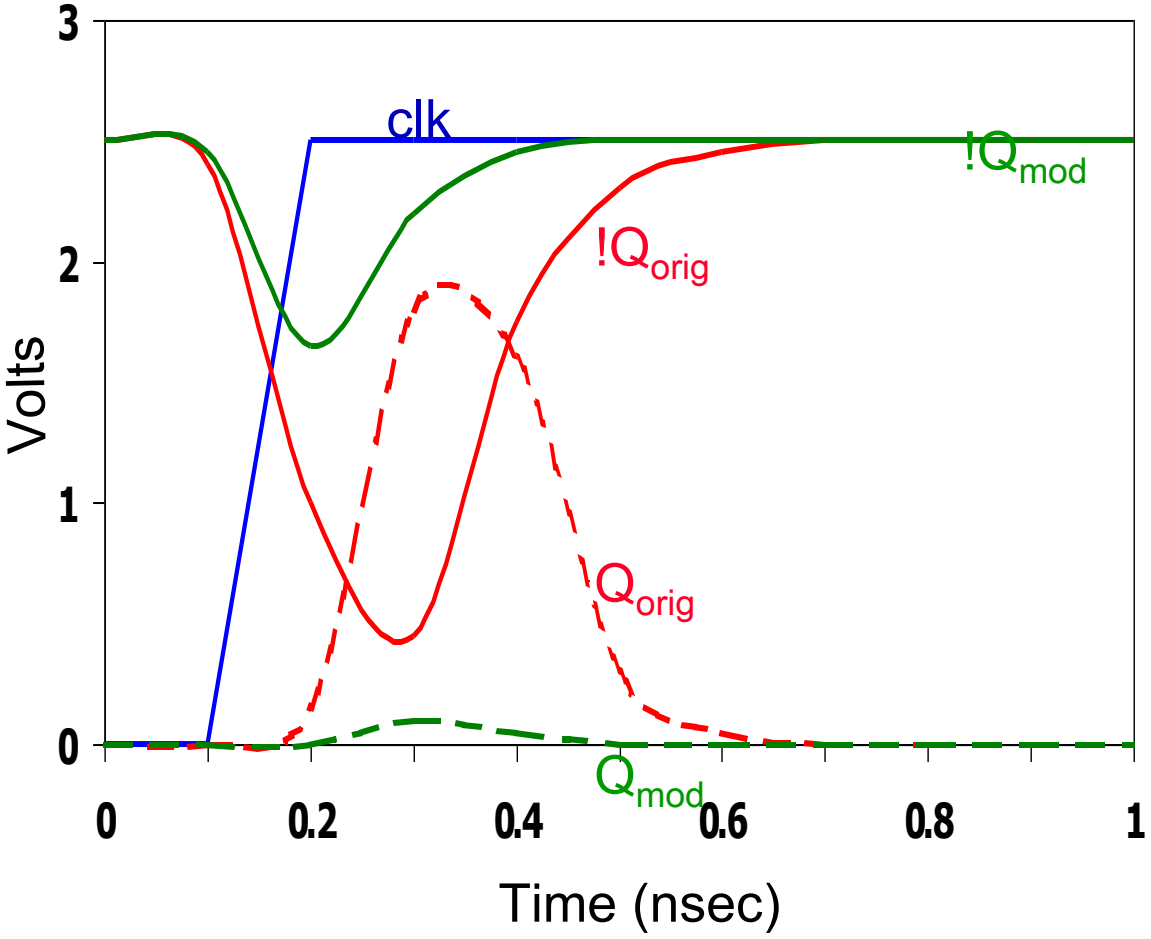

master transparent
slave hold
clk
master hold
slave transparent

Simplified TSPC ET FF





Sizing Issues in Simplified TSPC ET FF



Transistor sizing

Original width

M_4, M_5 = 0.5μm

M_7, M_8 = 2μm

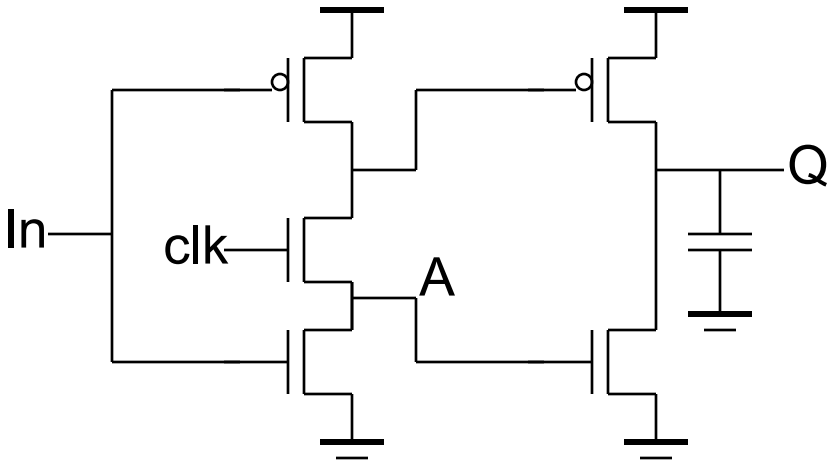
Modified width

M_4, M_5 = 1μm

M_7, M_8 = 1μm

Split-Output TSPC Latches

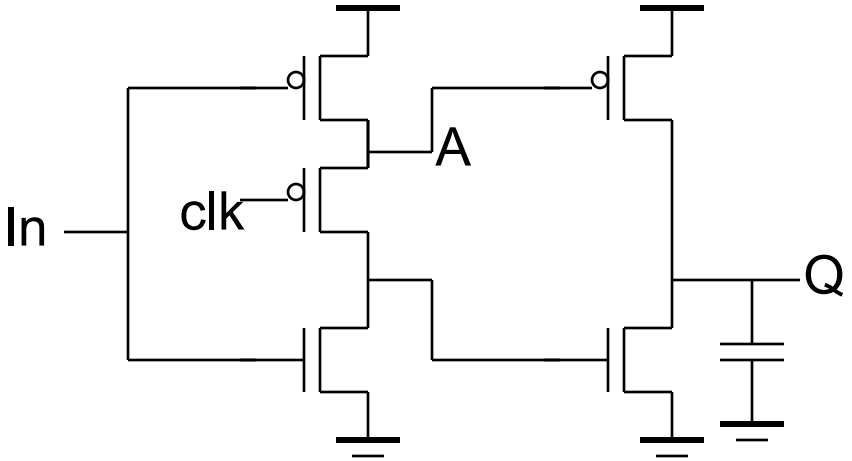
Positive Latch



transparent when clk = 1
hold when clk = 0

When In = 0, A = $V_{DD} - V_{Tn}$

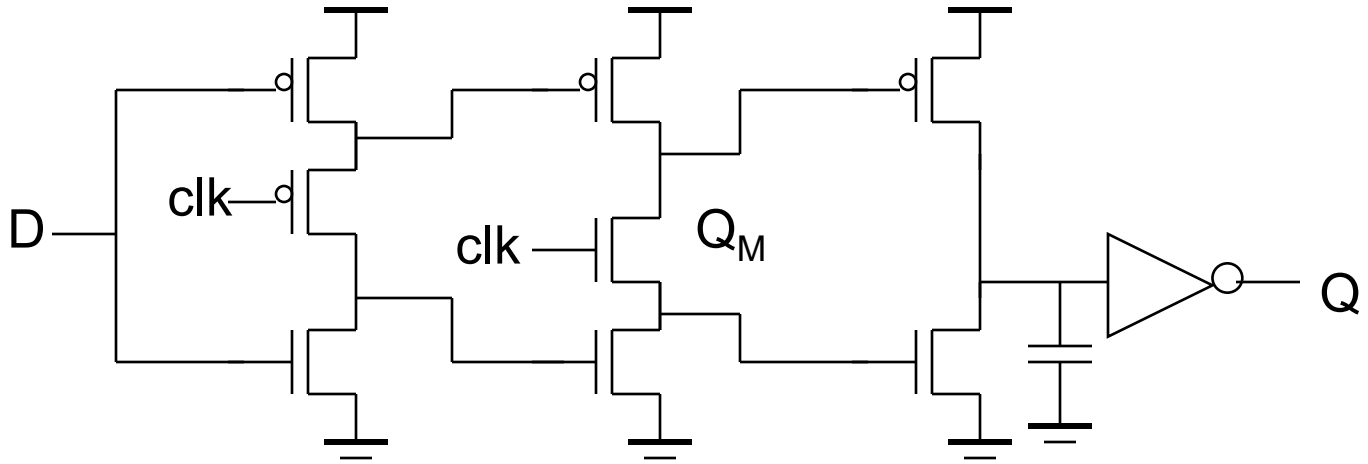
Negative Latch

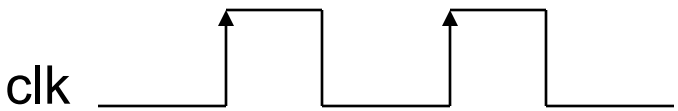


hold when clk = 1
transparent when clk = 0

When In = 1, A = $| V_{Tp} |$

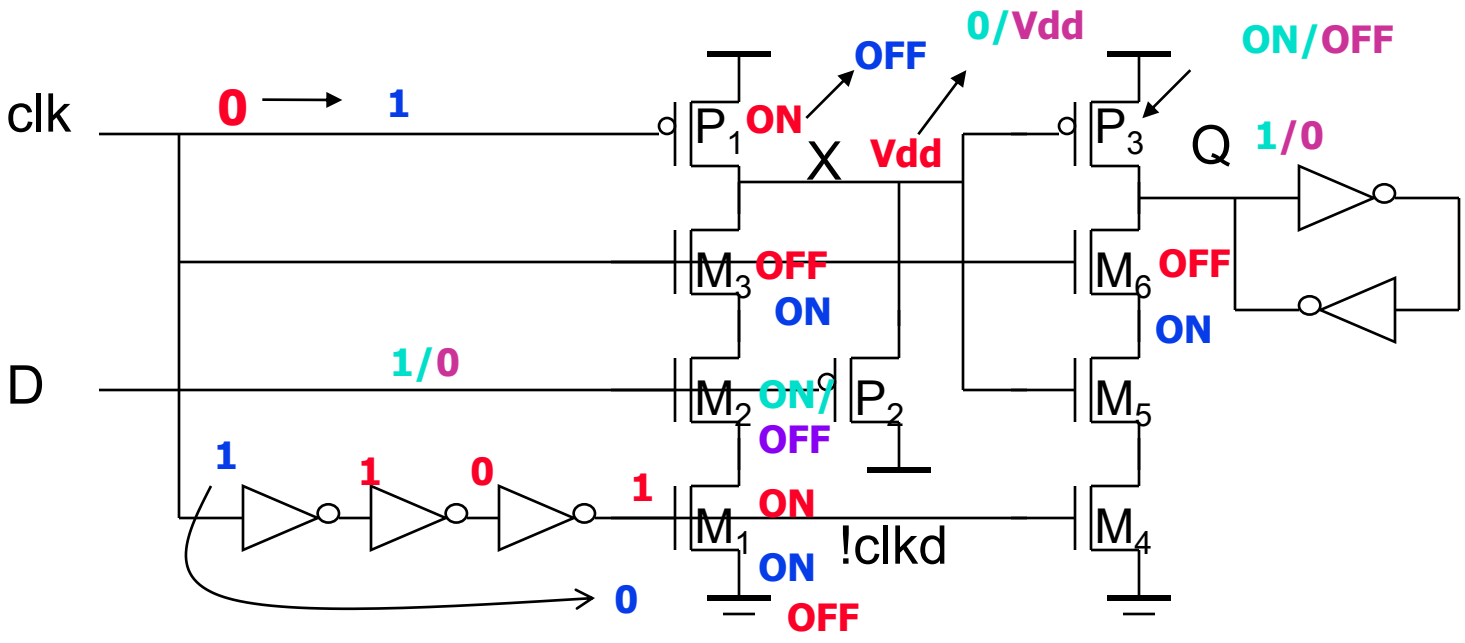
Split-Output TSPC ET FF





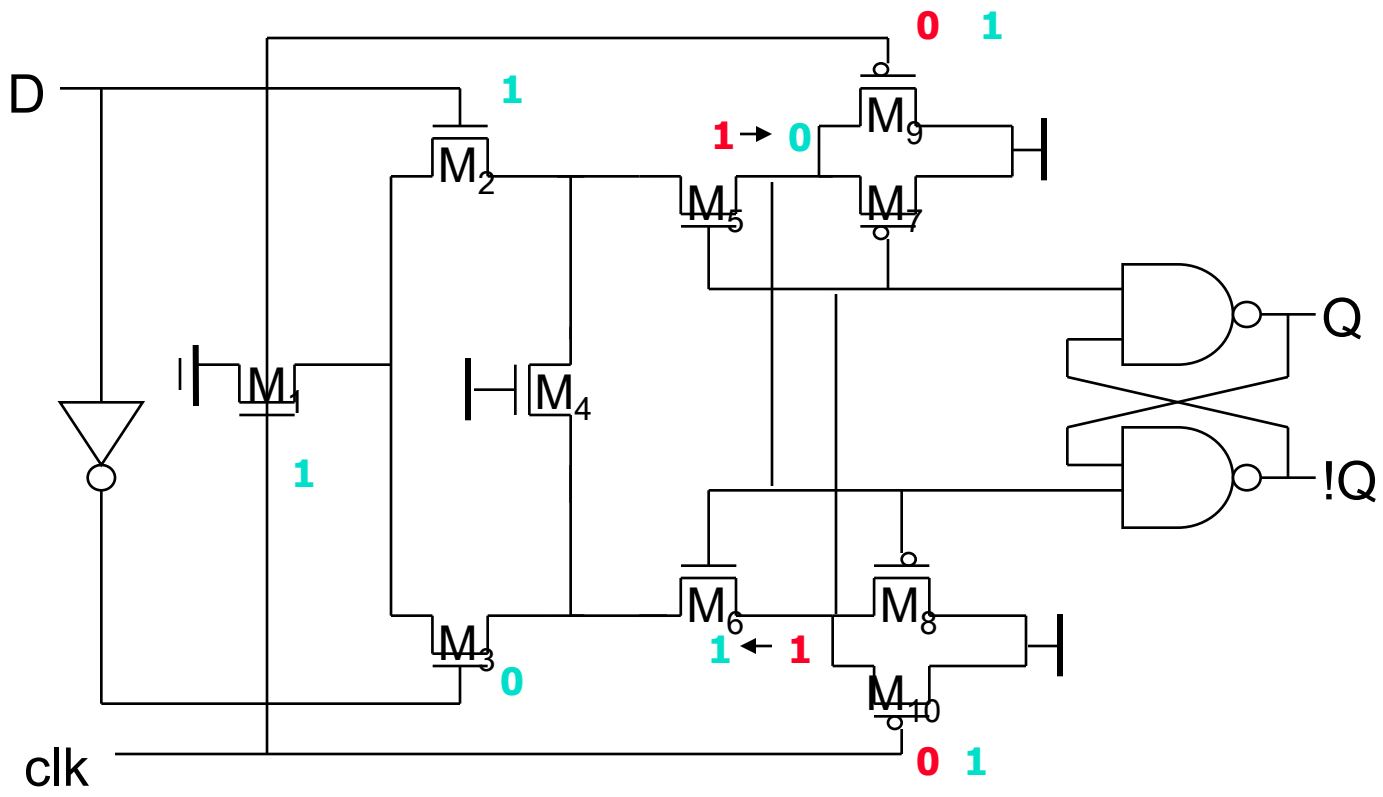
Pulsed FF (AMD-K6)

- Pulse registers - a short pulse (glitch clock) is generated locally from the rising (or falling) edge of the system clock and is used as the clock input to the flipflop
  - race conditions are avoided by keeping the transparent mode time very short (during the pulse only)
  - advantage is reduced clock load; disadvantage is substantial increase in verification complexity



Sense Amp FF (StrongArm SA100)

- Sense amplifier (circuits that accept small swing input signals and amplify them to full rail-to-rail signals) flipflops
  - advantages are reduced clock load and that it can be used as a receiver for reduced swing differential buses



Flipflop Comparison Chart

Name	Type	#clk ld	#tr	t_{set-up}	t_{hold}	t_{pFF}
Mux	Static	8 (clk-!clk)	20	$3t_{pinv}+t_{ptx}$	0	$t_{pinv}+t_{ptx}$
PowerPC	Static	8 (clk-!clk)	16			
2-phase	Ps-Static	8 (clk1-clk2)	16			
T-gate	Dynamic	4 (clk-!clk)	8	t_{ptx}	t_{o1-1}	$2t_{pinv}+t_{ptx}$
C^2MOS	Dynamic	4 (clk-!clk)	8			
TSPC	Dynamic	4 (clk)	11	t_{pinv}	t_{pinv}	$3t_{pinv}$
S-O TSPC	Dynamic	2 (clk)	10			
AMD K6	Dynamic	5 (clk)	19			
SA 100	SenseAmp	3 (clk)	20			

Choosing a Clocking Strategy

- Choosing the right clocking scheme affects the functionality, speed, and power of a circuit
- Two-phase designs
  - + robust and conceptually simple
  - - need to generate and route two clock signals
  - - have to design to accommodate possible skew between the two clock signals
- Single phase designs
  - + only need to generate and route one clock signal
  - + supported by most automated design methodologies
  - + don't have to worry about skew between the two clocks
  - - have to have guaranteed slopes on the clock edges

Next Lecture and Reminders

- Next lecture
  - Timing issues, Intro to datapath design
    - Reading assignment – Rabaey, et al, 10.1-10.3.3; 11.1-11.2
- Reminders
  - Pick up second half of the new edition of the book from Sue in 202 Pond Lab
  - Project final reports due December 5th
  - HW4 due November 5th
  - HW5 out November 5th and due November 19th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in TBD