CSE477
VLSI Digital Circuits
Fall 2002

Lecture 05: IC Manufacturing

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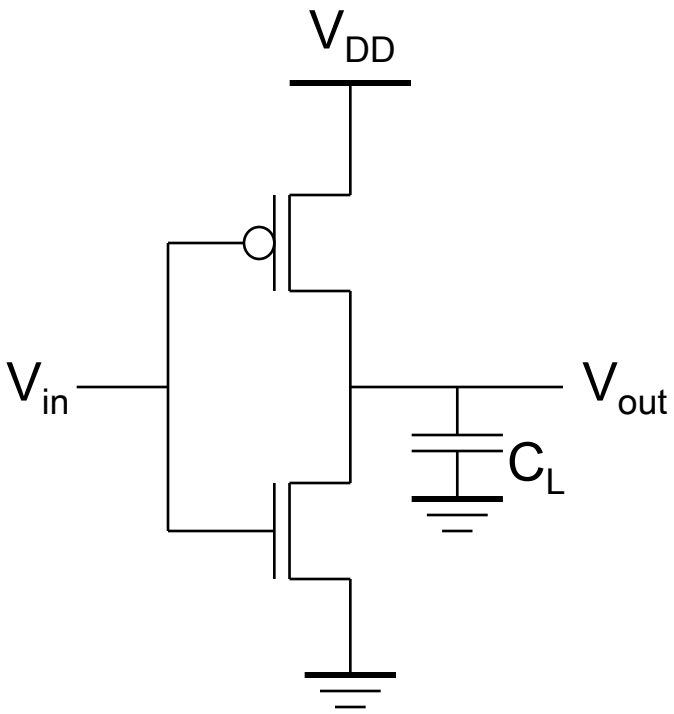
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: CMOS Inverter

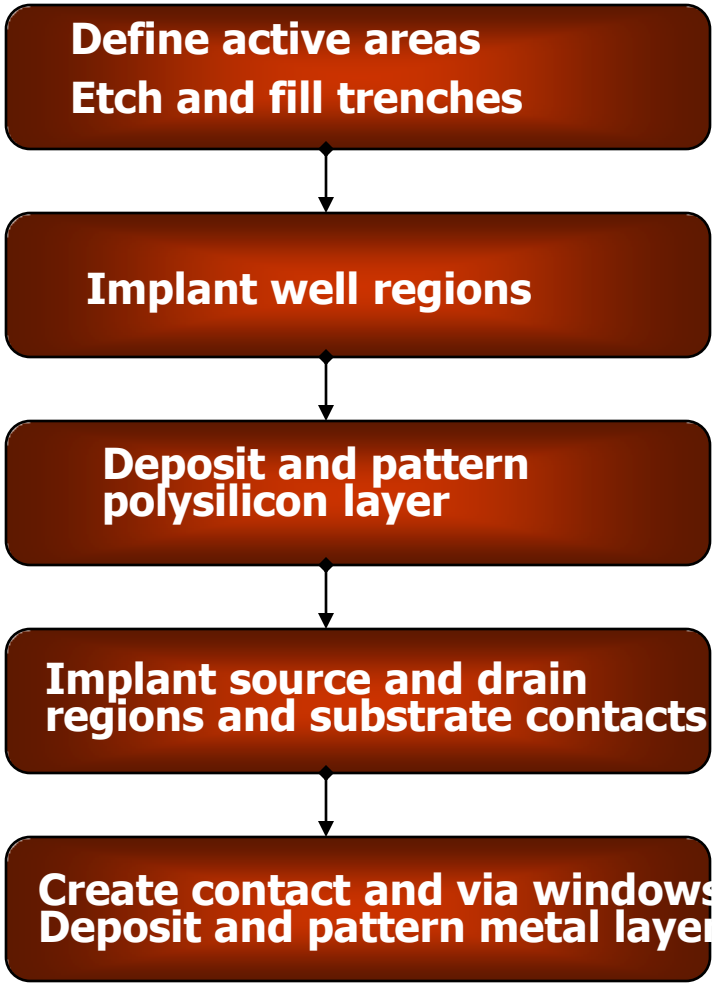


- Full rail-to-rail swing ⇒ high noise margins
- Low output impedance
- High input impedance
- No direct path steady-state between power and ground ⇒ no static power dissipation
- Propagation delay a function of load capacitance and on resistance of transistors

Growing the Silicon Ingot

From *Smithsonian*, 2000

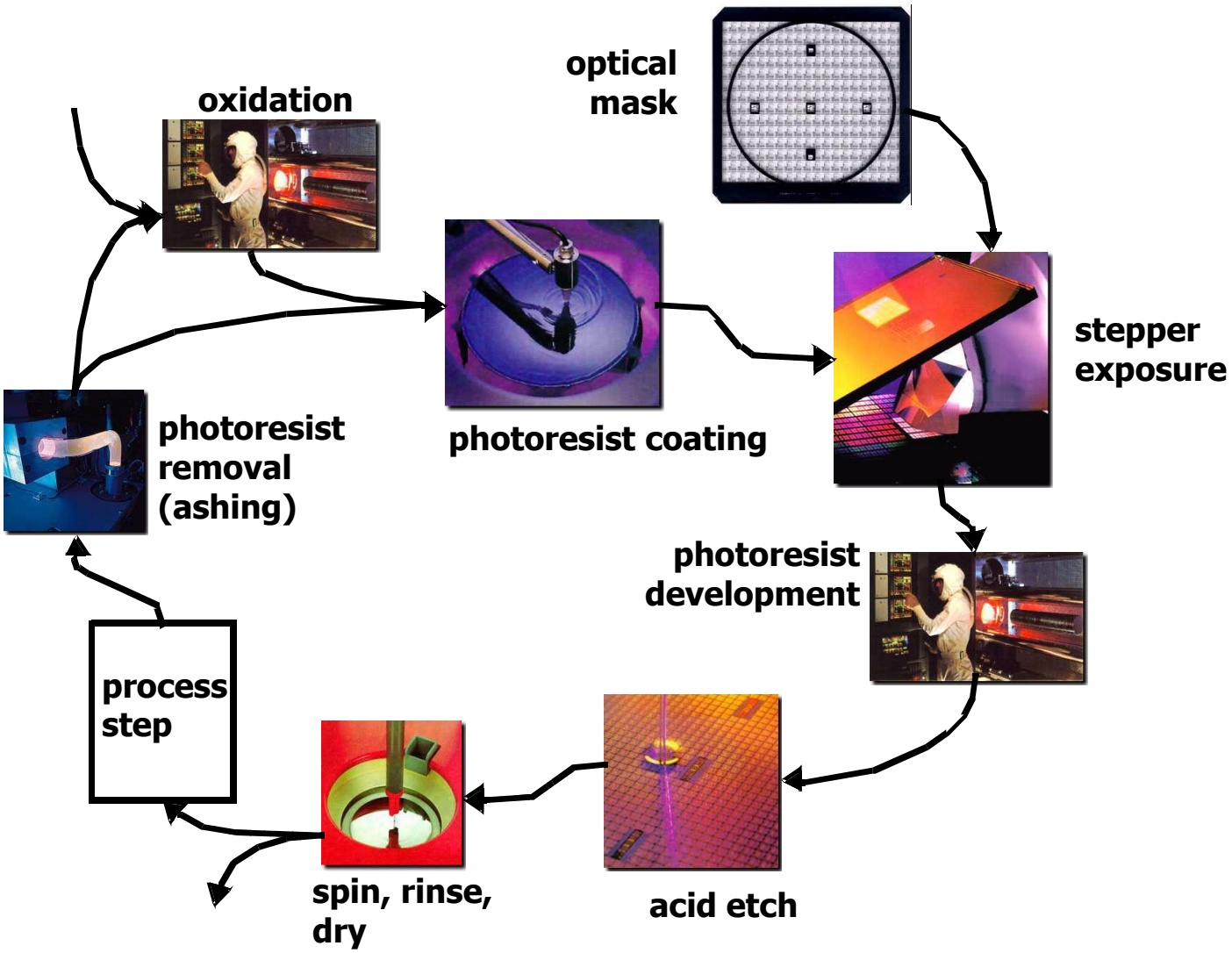
CMOS Process at a Glance



- One full photolithography sequence per layer (mask)
- Built (roughly) from the bottom up
  - 5 metal 2
  - 4 metal 1
  - 2 polysilicon
  - 3 source and drain diffusions
  - 1 tubs (aka wells, active areas)

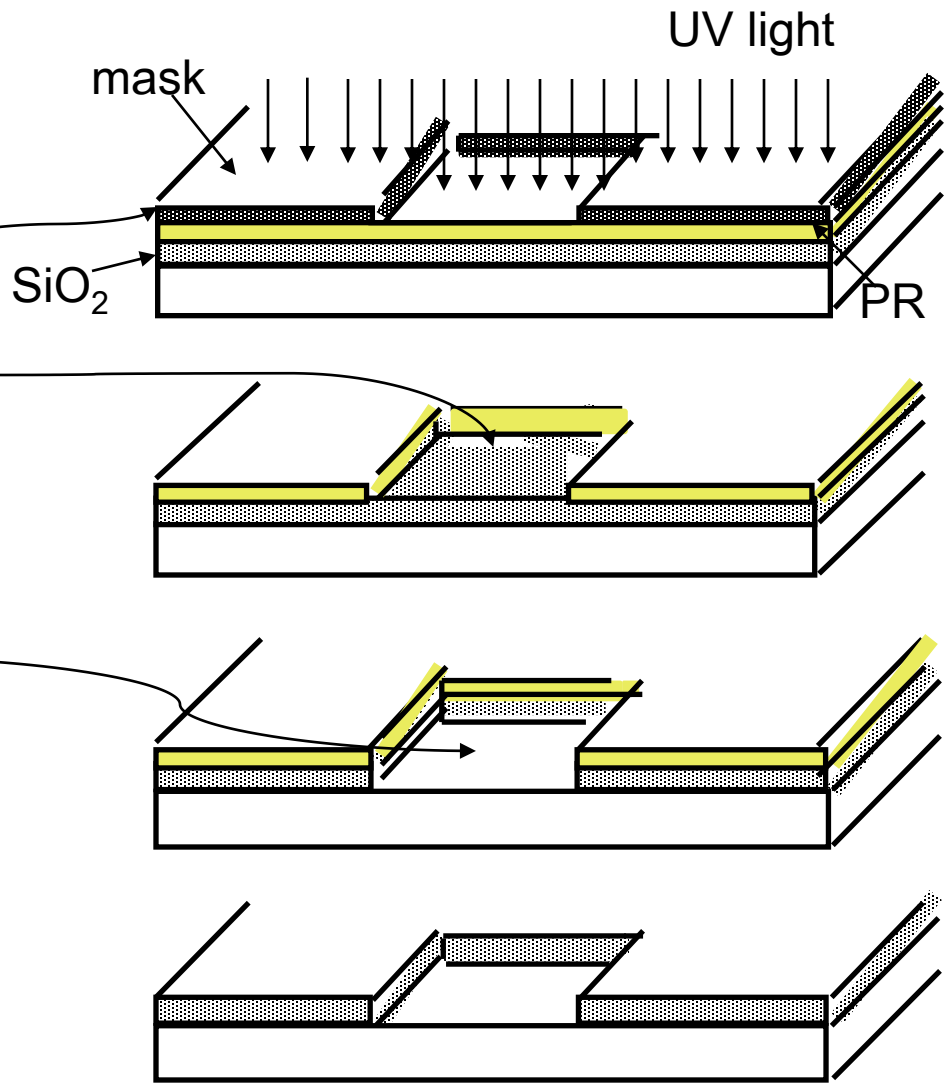
exception!

Photolithographic Process

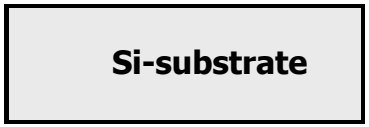


Patterning - Photolithography

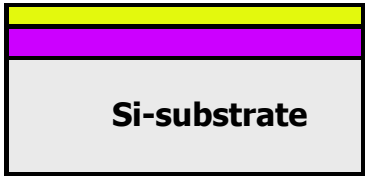
1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
   - Unexposed (negative PR)
   - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
   - Ion implantation
   - Plasma etching
   - Metal deposition
8. Photoresist removal (ashing)



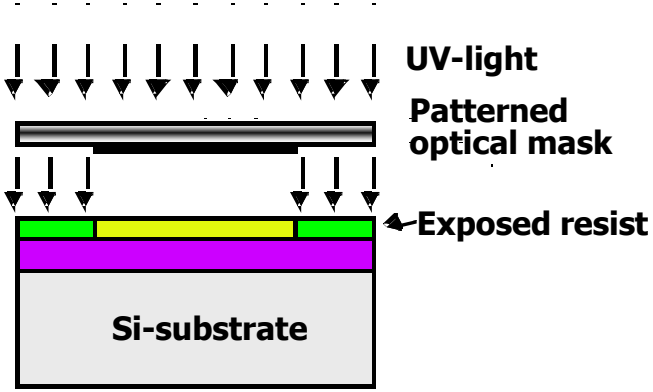
Example of Patterning of SiO2



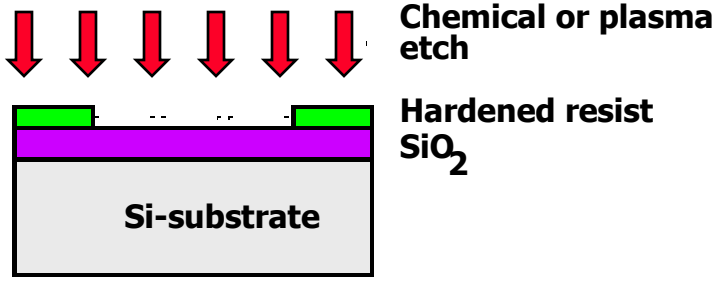
Silicon base material



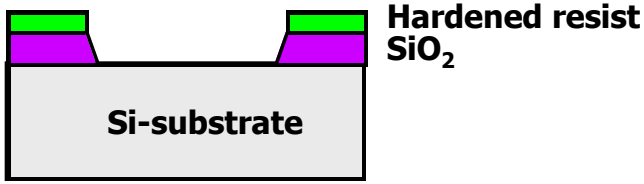
1&2. After oxidation and deposition of negative photoresist



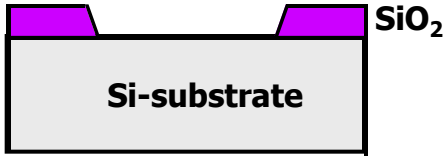
3. Stepper exposure



4. After development and etching of resist, chemical or plasma etch of SiO_2



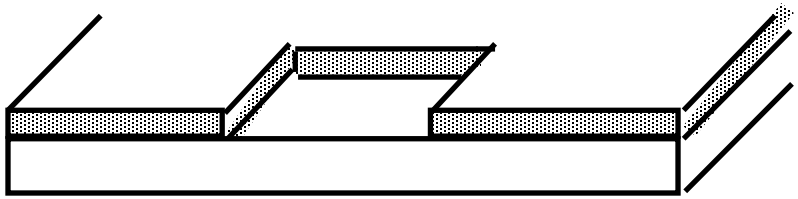
5. After etching



8. Final result after removal of resist

Diffusion and Ion Implantation

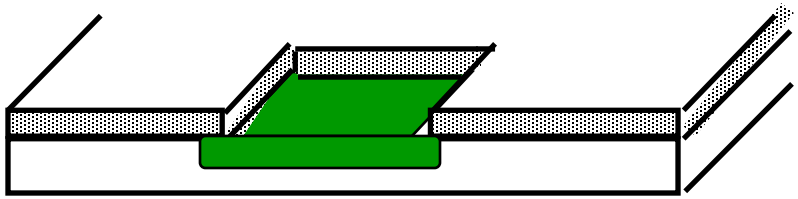
1. Area to be doped is exposed (photolithography)



2. Diffusion

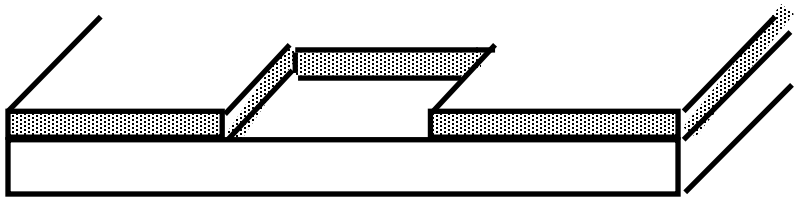
   or

   Ion implantation

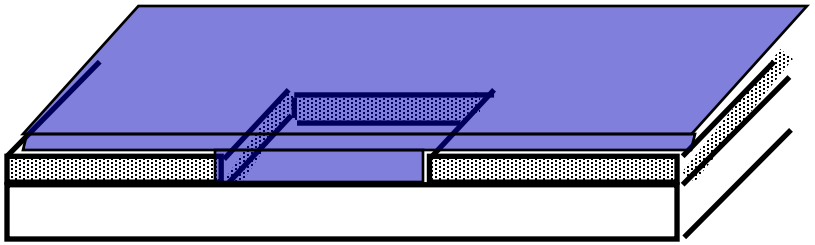


Deposition and Etching

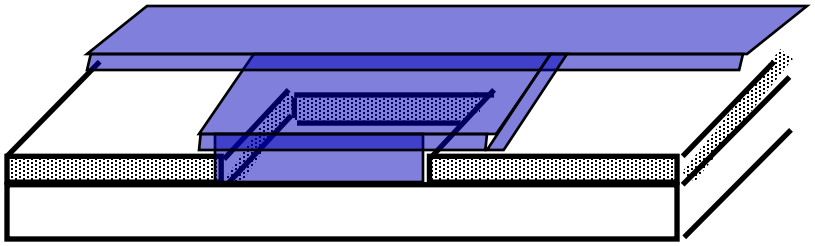
1. Pattern masking (photolithography)



2. Deposit material over entire wafer
   - CVD (Si_3N_4)
   - chemical deposition (polysilicon)
   - sputtering (Al)



3. Etch away unwanted material
   - wet etching
   - dry (plasma) etching

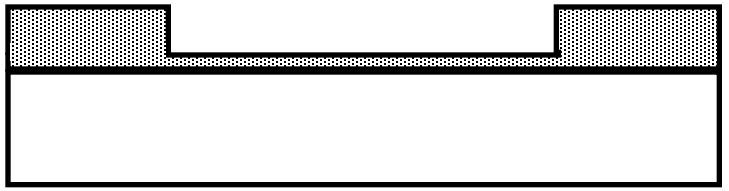


Planarization: Polishing the Wafers

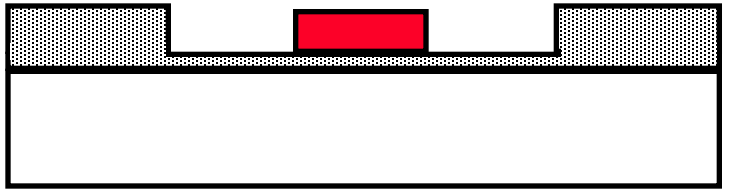
From *Smithsonian*, 2000

Self-Aligned Gates

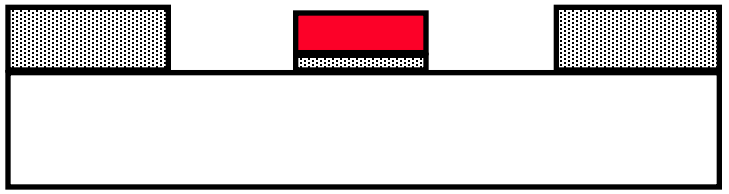
1. Create thin oxide in the “active” regions, thick elsewhere



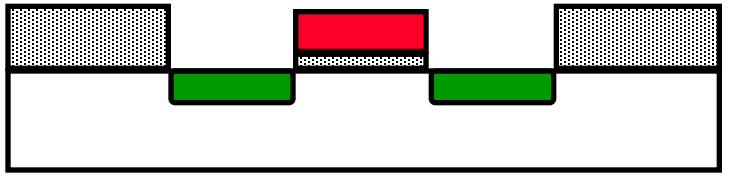
2. Deposit polysilicon



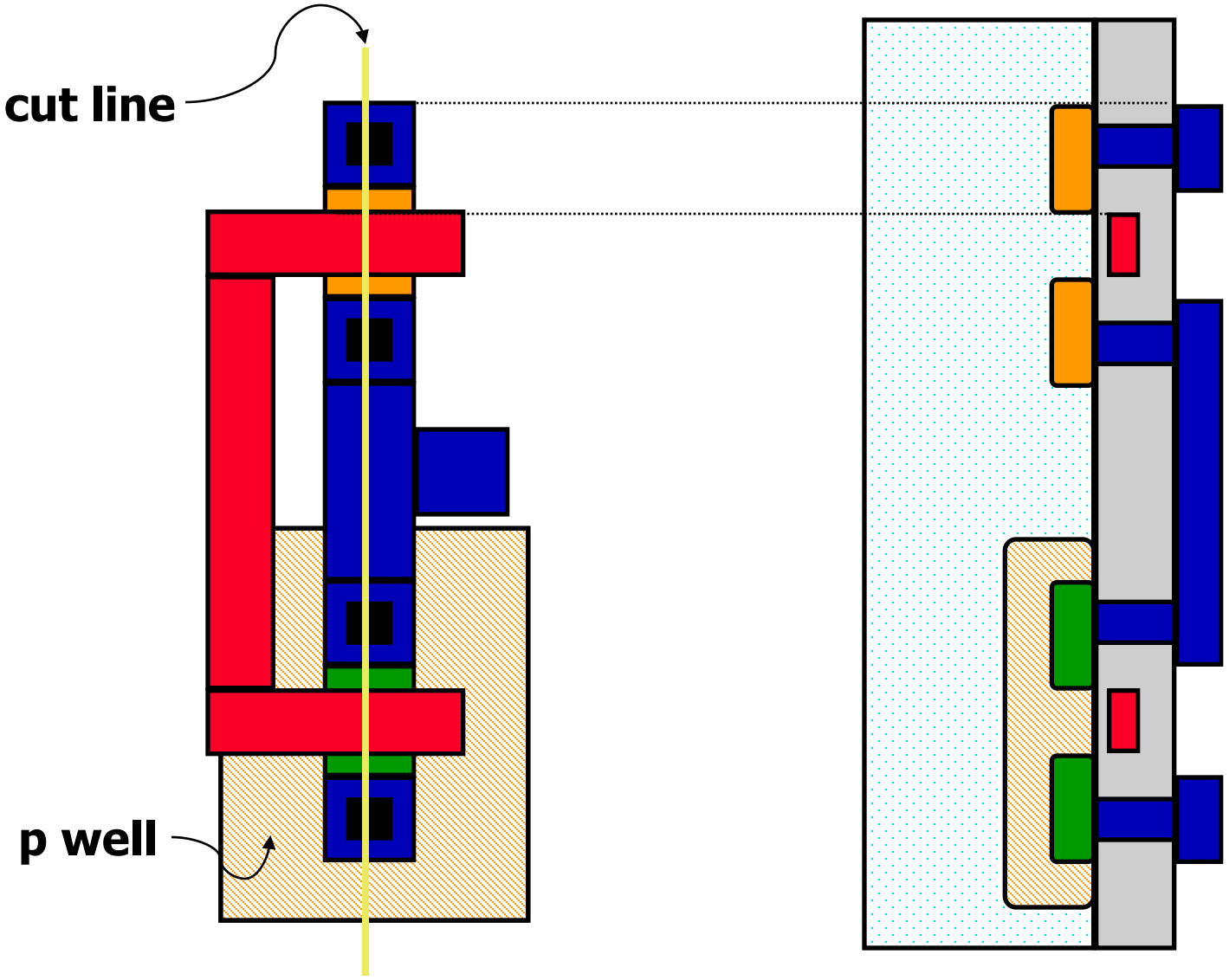
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)



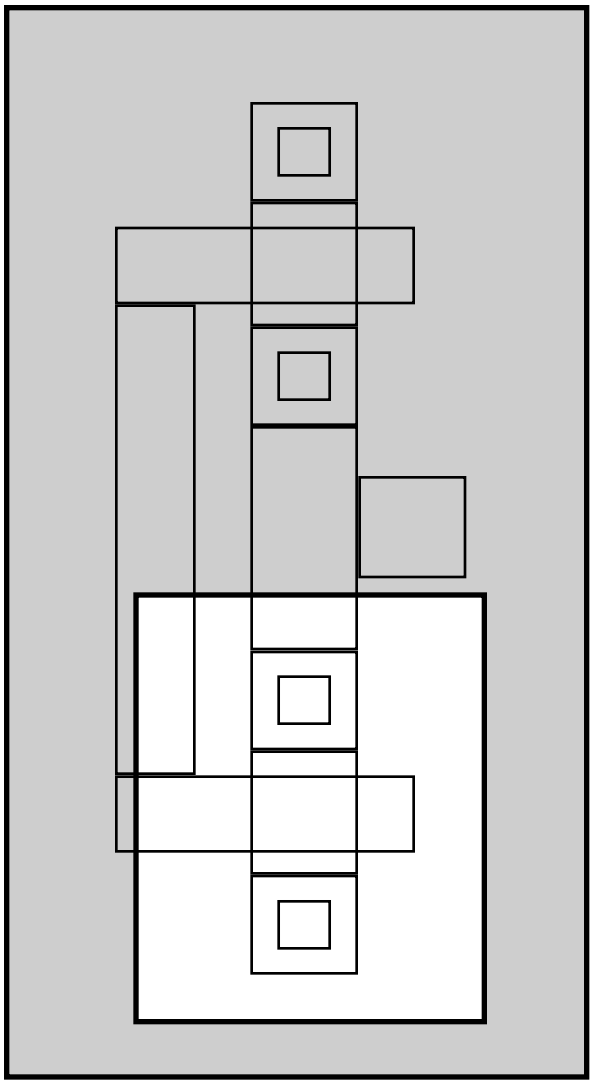
4. Implant dopant

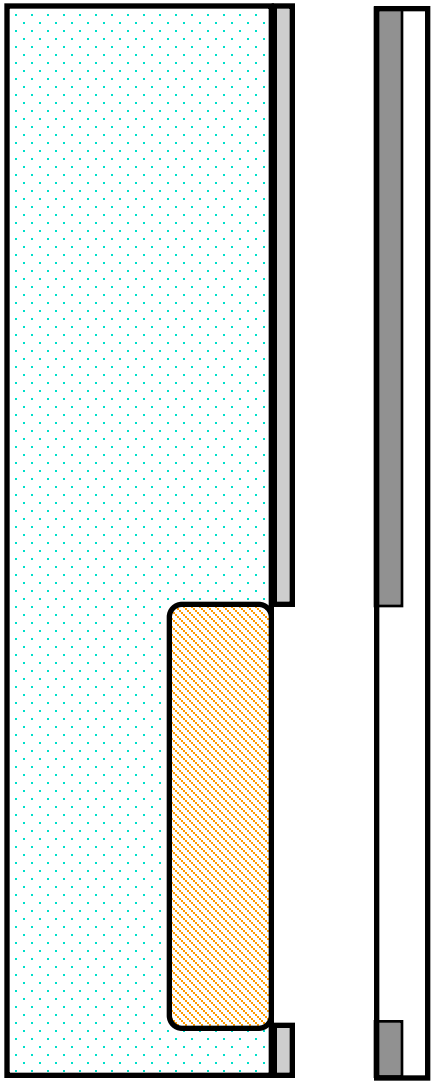


Simplified CMOS Inverter Process

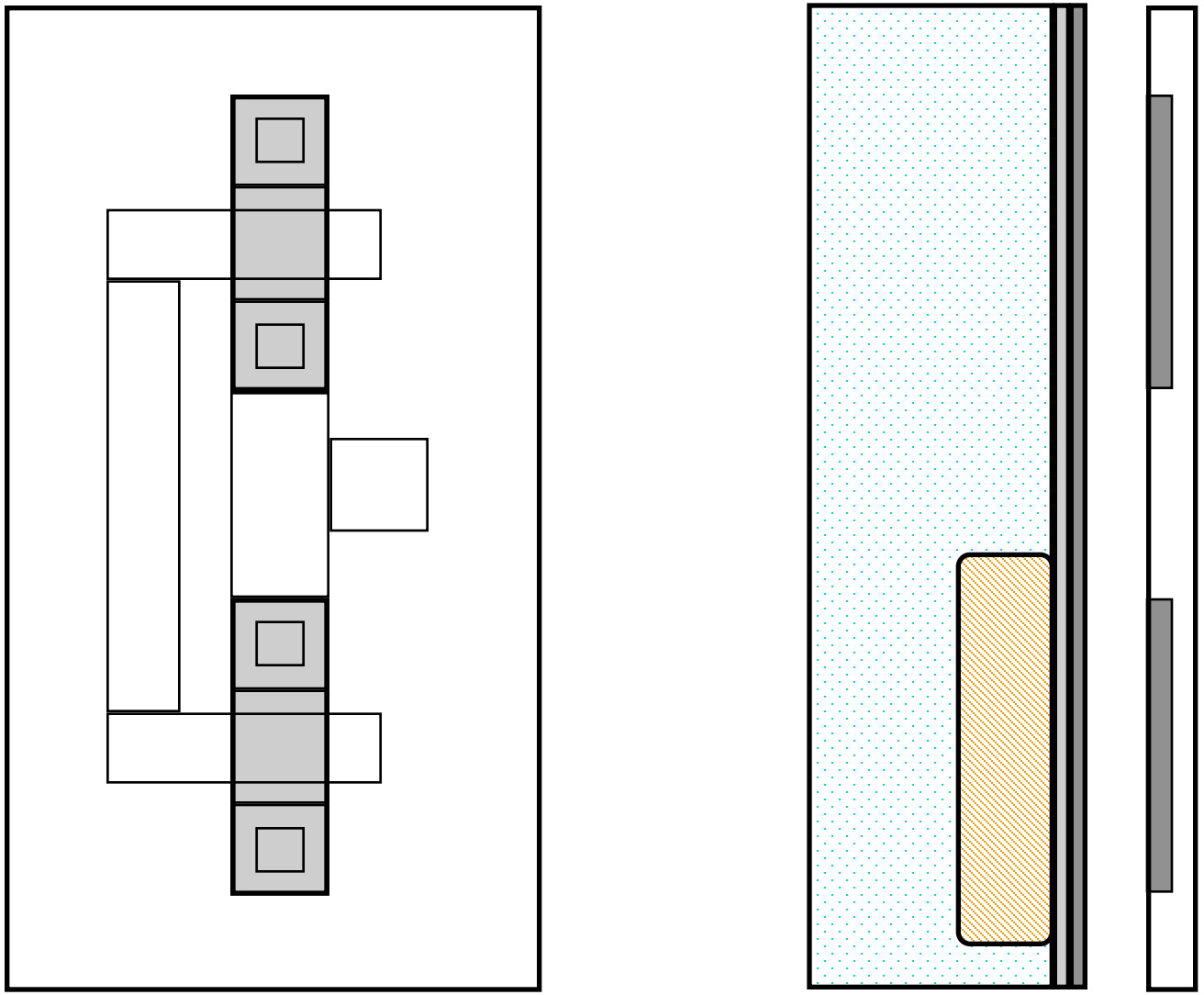


P-Well Mask

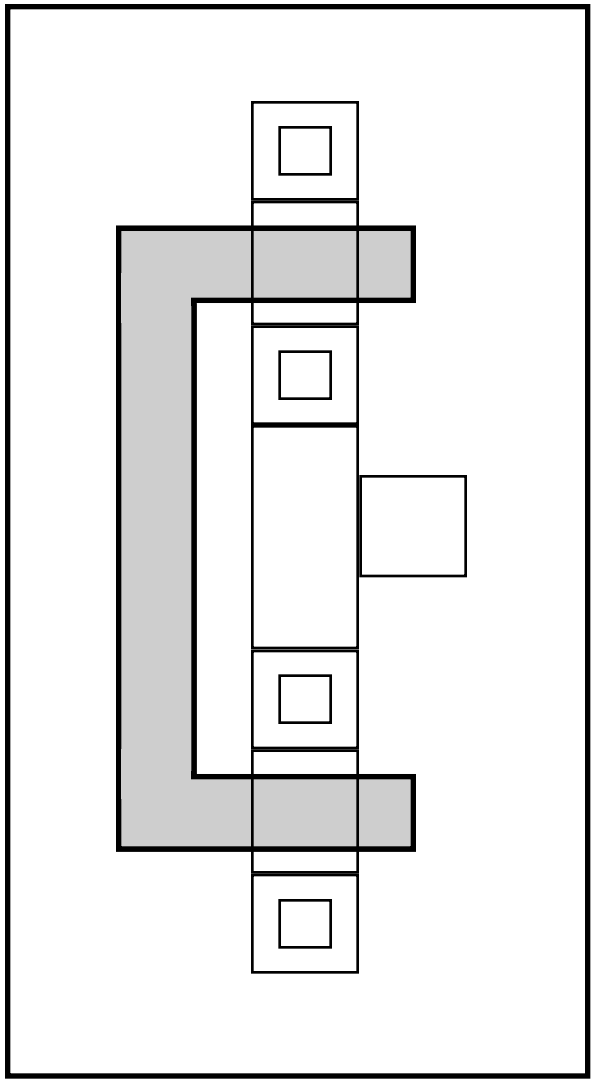


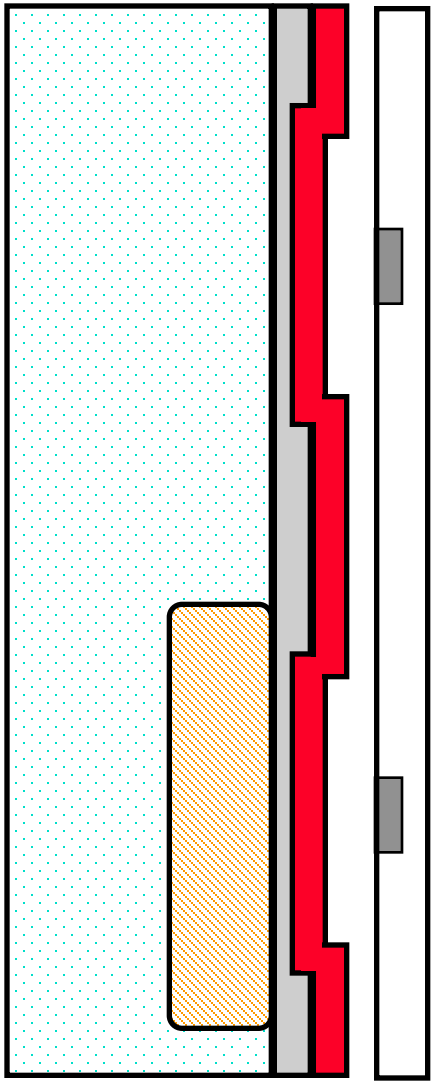


Active Mask

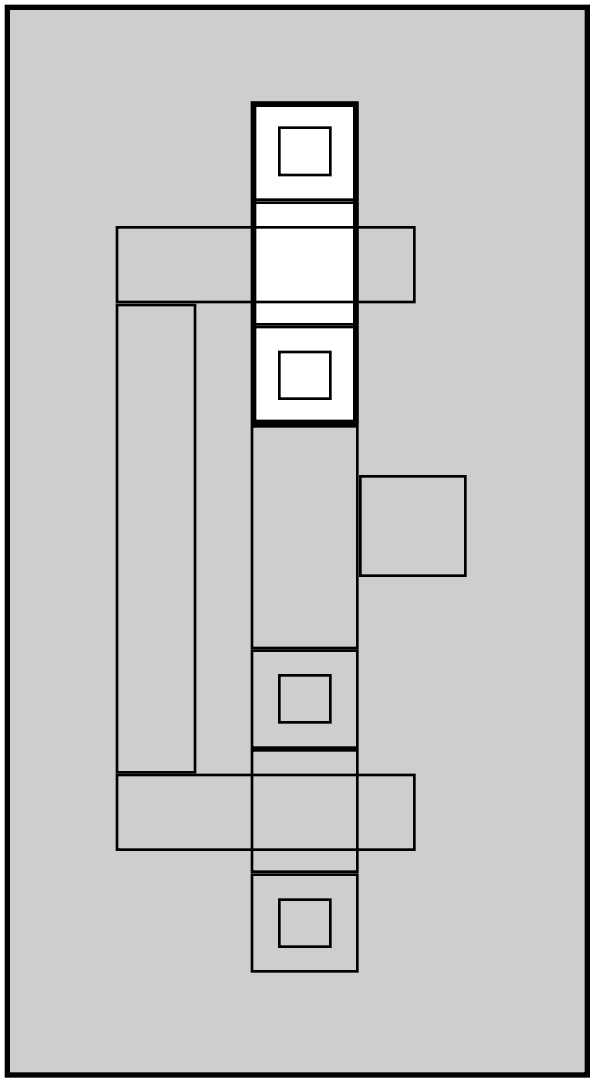


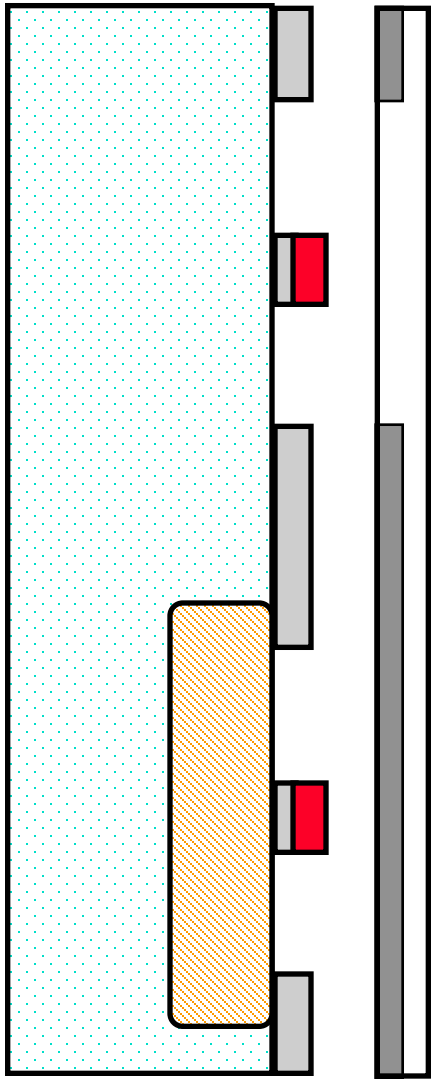
Poly Mask



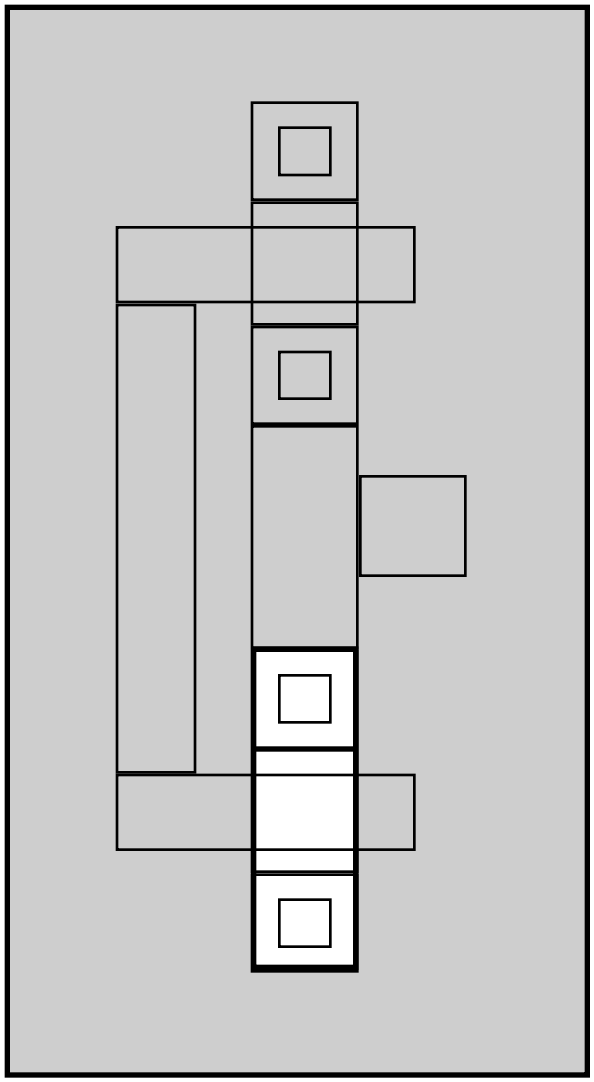


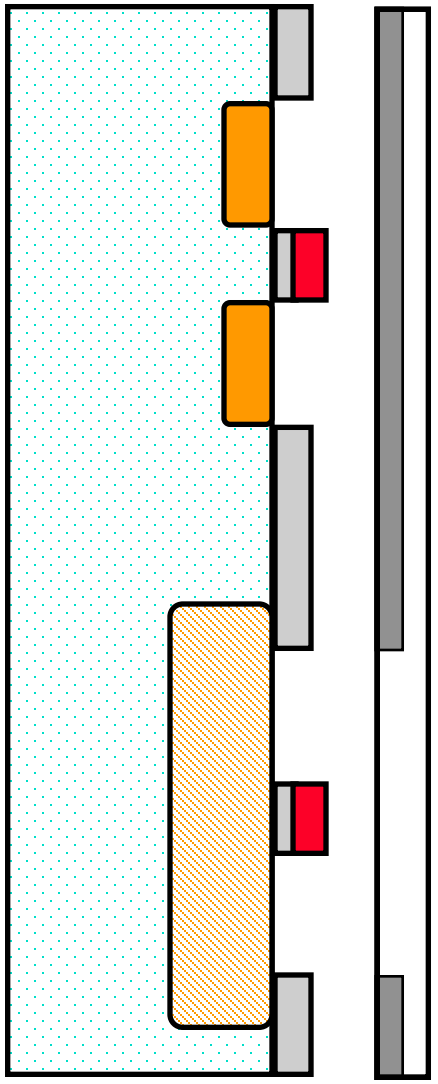
P+ Select Mask



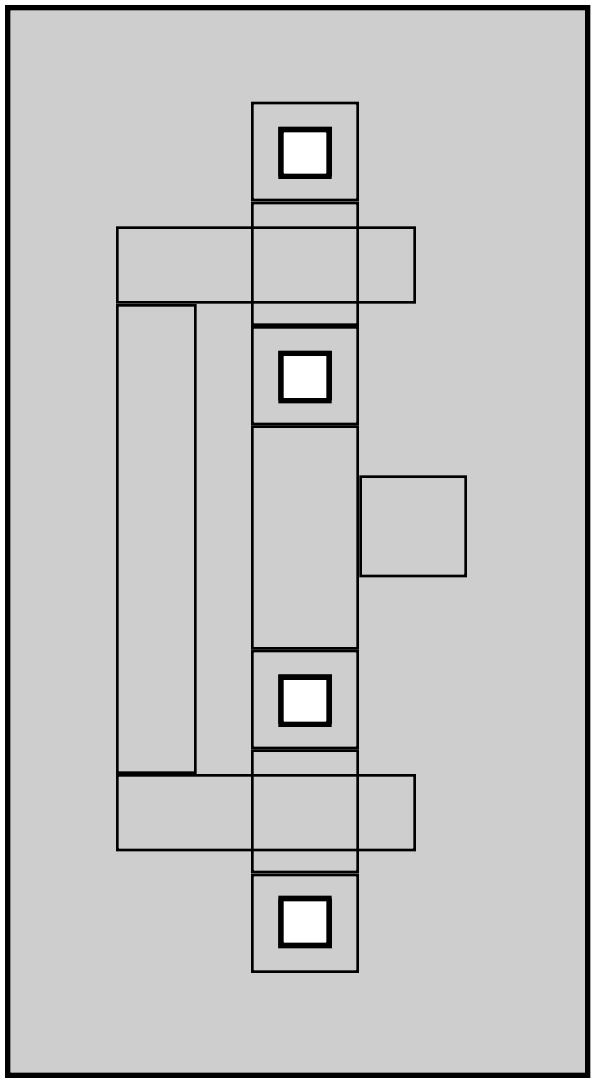


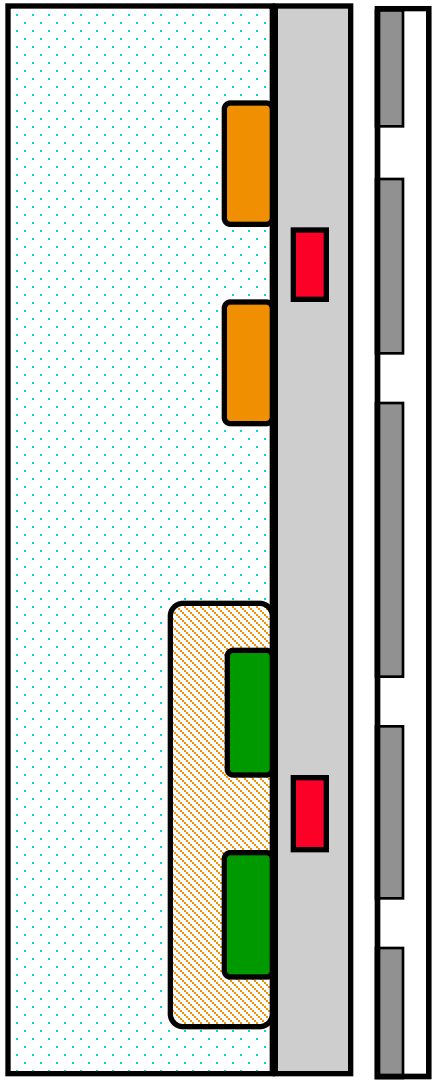
N+ Select Mask



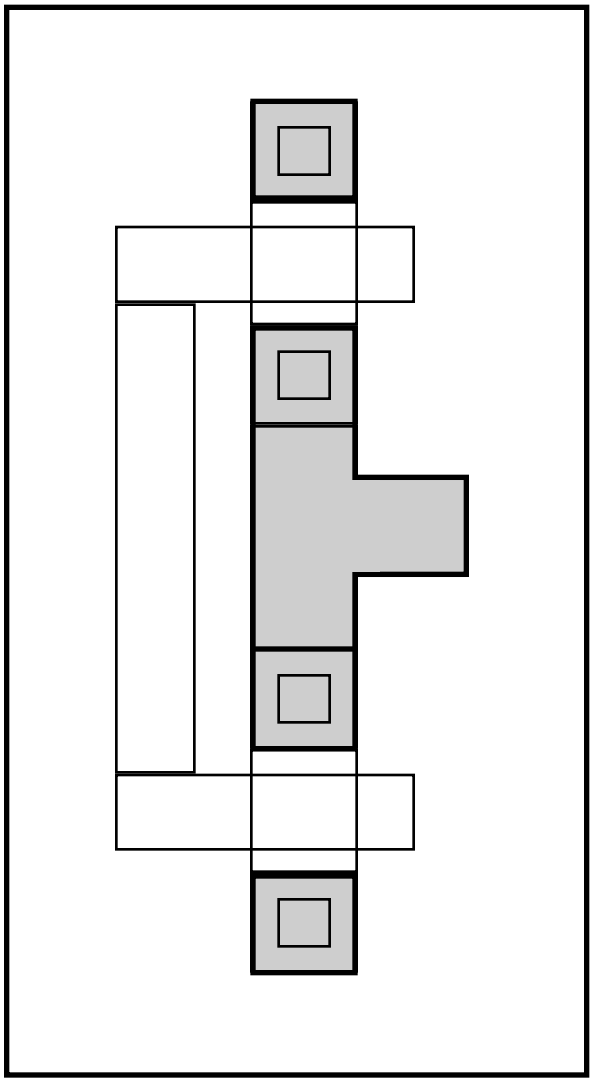


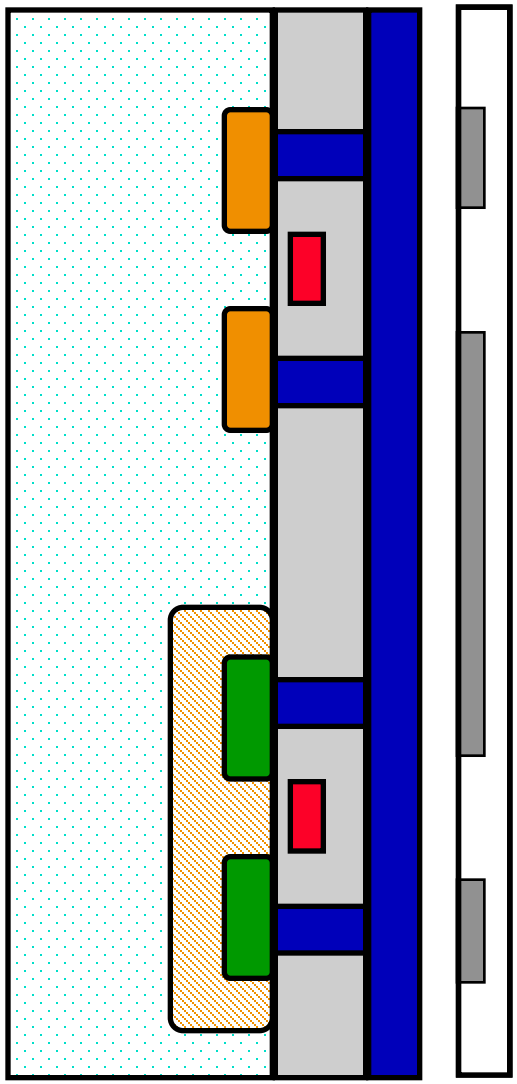
Contact Mask





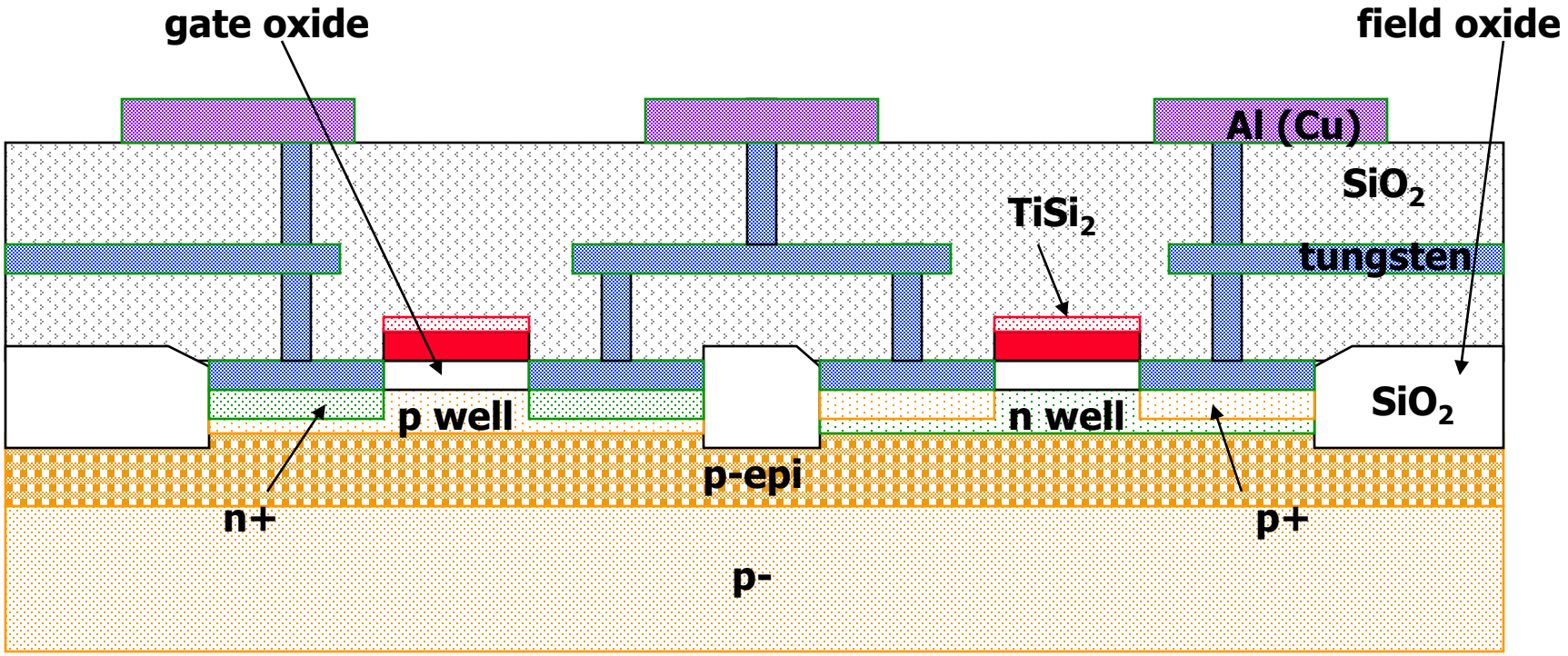
Metal Mask



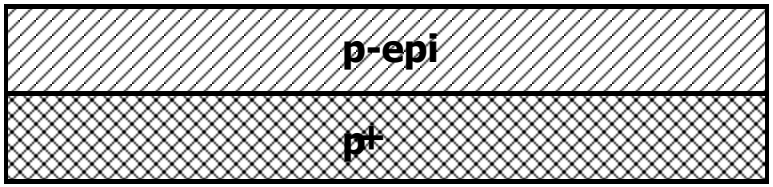


A Modern CMOS Process

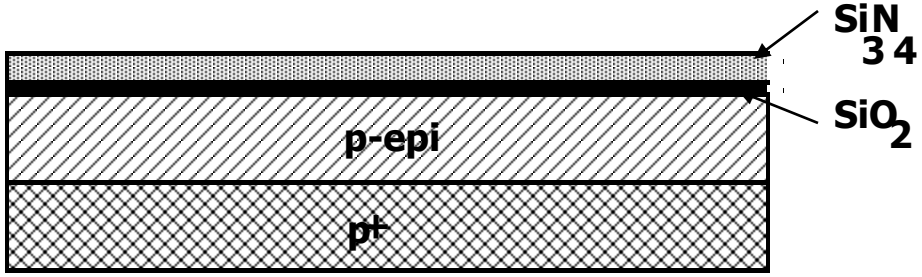
Dual-Well Trench-Isolated CMOS



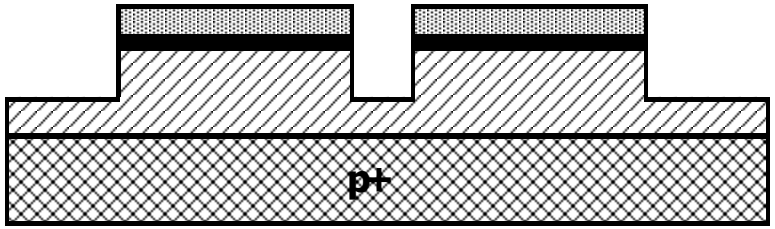
Modern CMOS Process Walk-Through



Base material: p+ substrate with p-epi layer

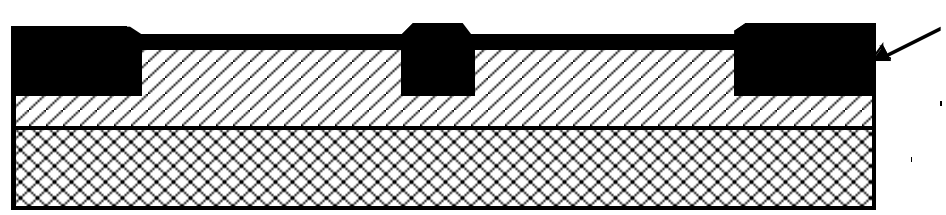


After deposition of gate-oxide and sacrifical nitride (acts as a buffer layer)

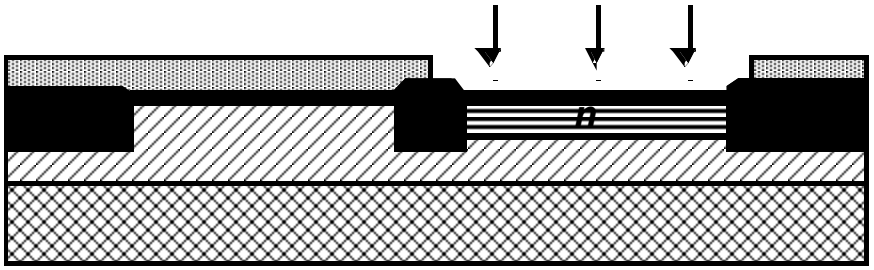


After plasma etch of insulating trenches using the inverse of the active area mask

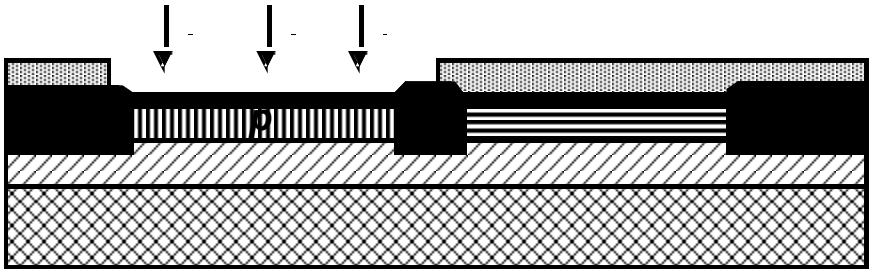
CMOS Process Walk-Through, con't



After trench filling, CMP planarization, and removal of sacrificial nitride

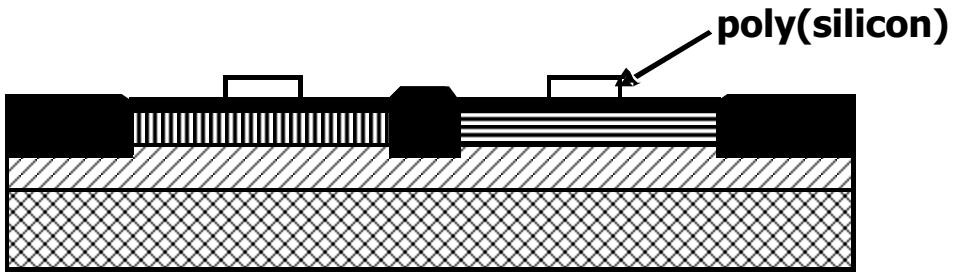


After n-well and V_{Tp} adjust implants

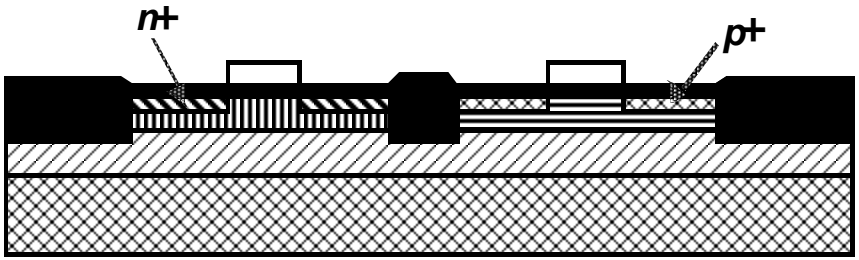


After p-well and V_{Tn} adjust implants

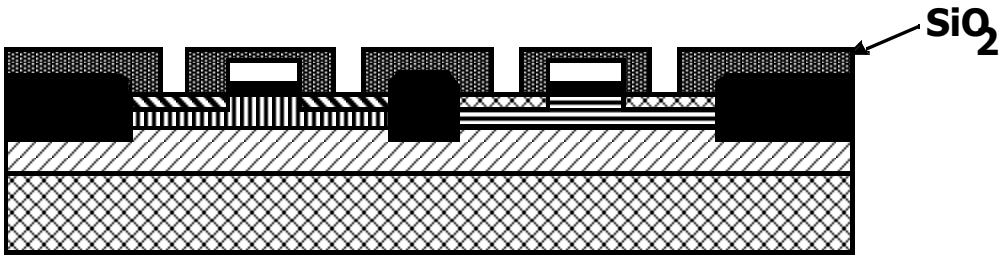
CMOS Process Walk-Through, con't



After polysilicon deposition and etch

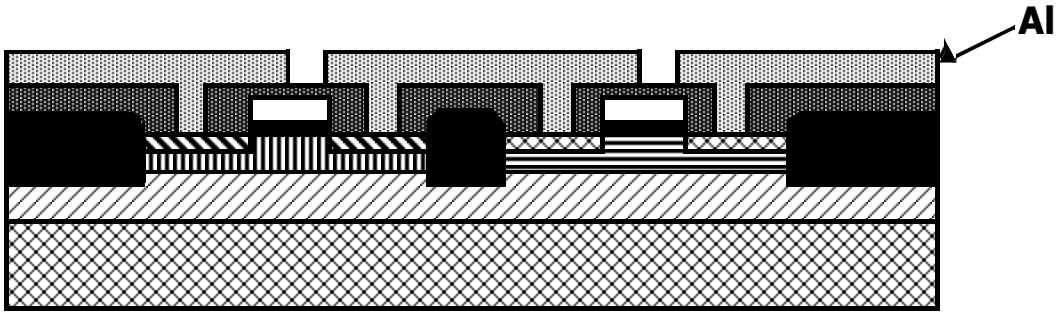


After n+ source/dram and p+ source/drain implants. These steps also dope the polysilicon.

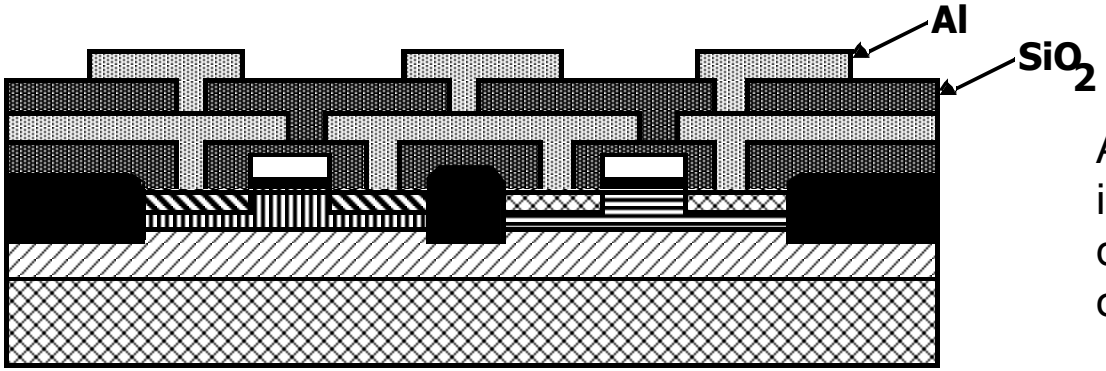


After deposition of SiO_2 insulator and contact hole etch

CMOS Process Walk-Through, con't

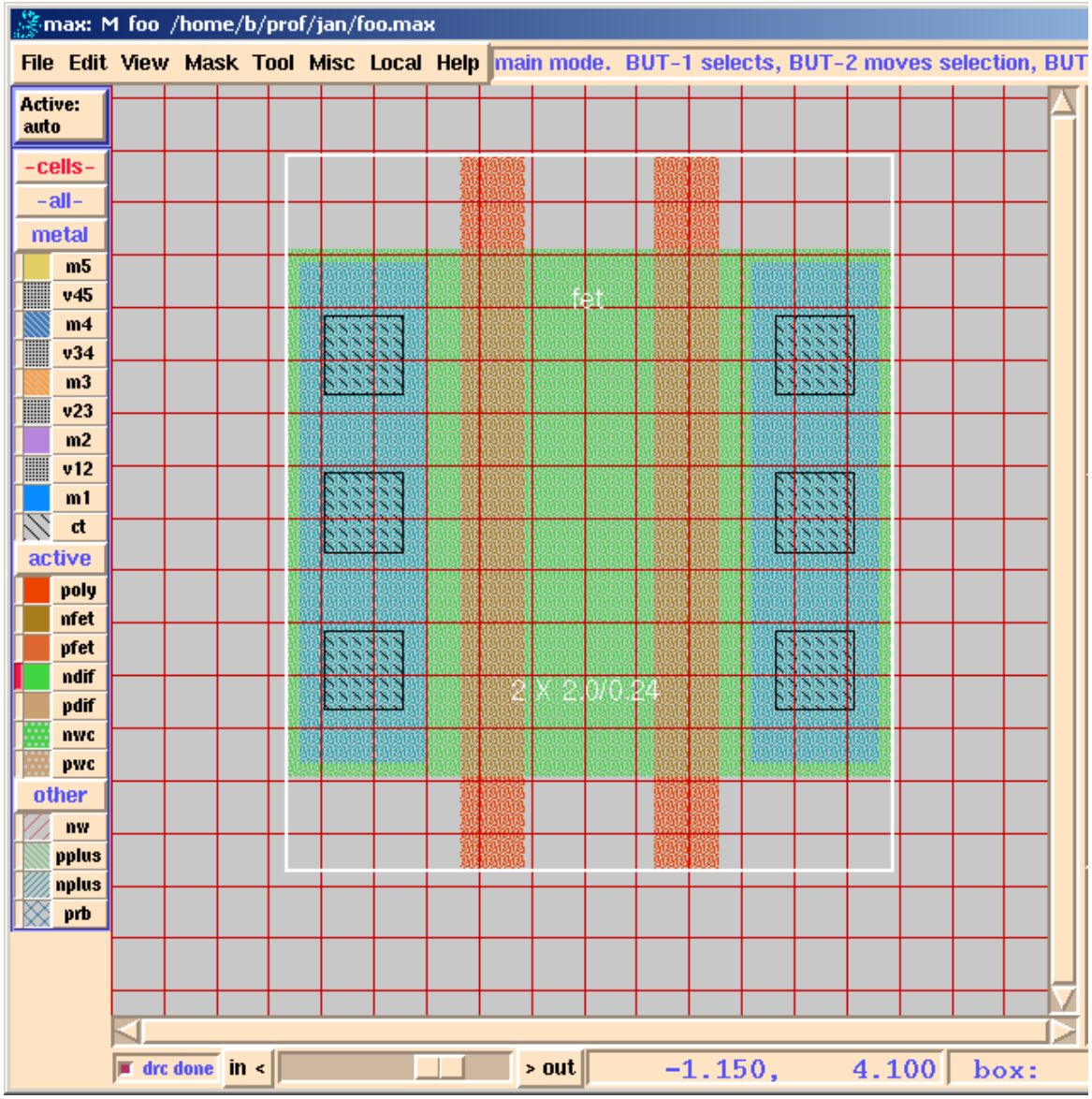


After deposition and patterning of first Al layer.

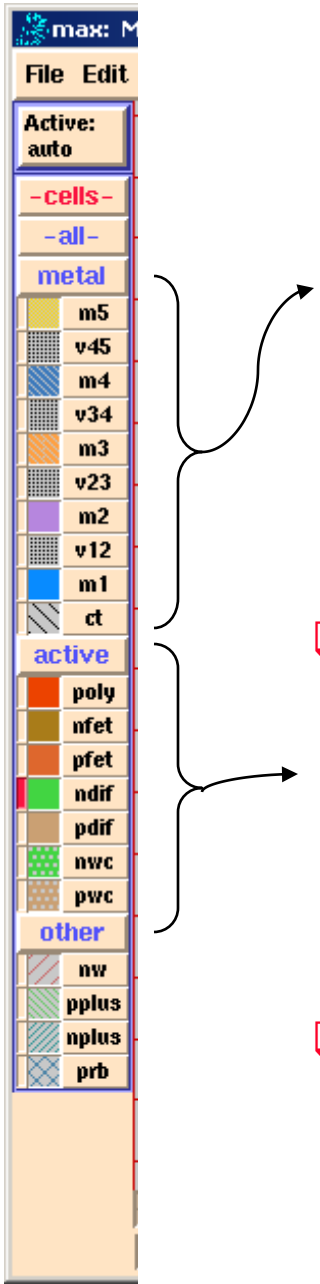


After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Layout Editor: *max* Design Frame

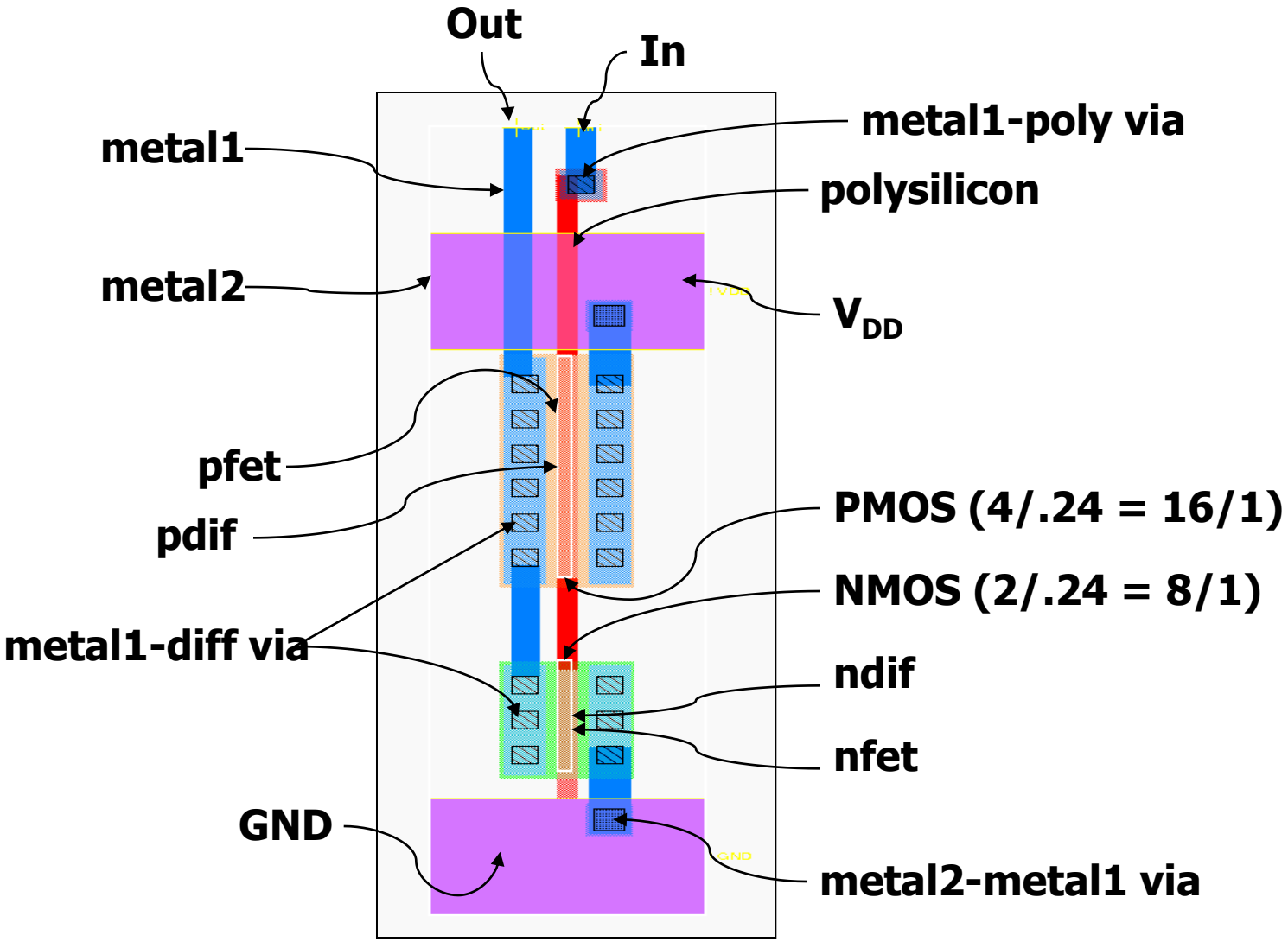


max Layer Representation



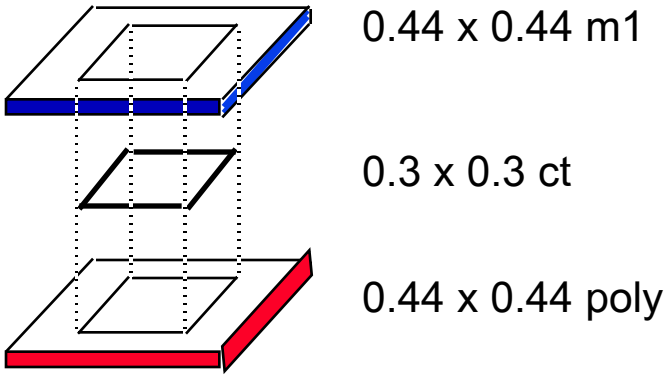
- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support “stacked vias”
- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))
- Wells (nw) and other select areas (pplus, nplus, prb)

CMOS Inverter *max* Layout

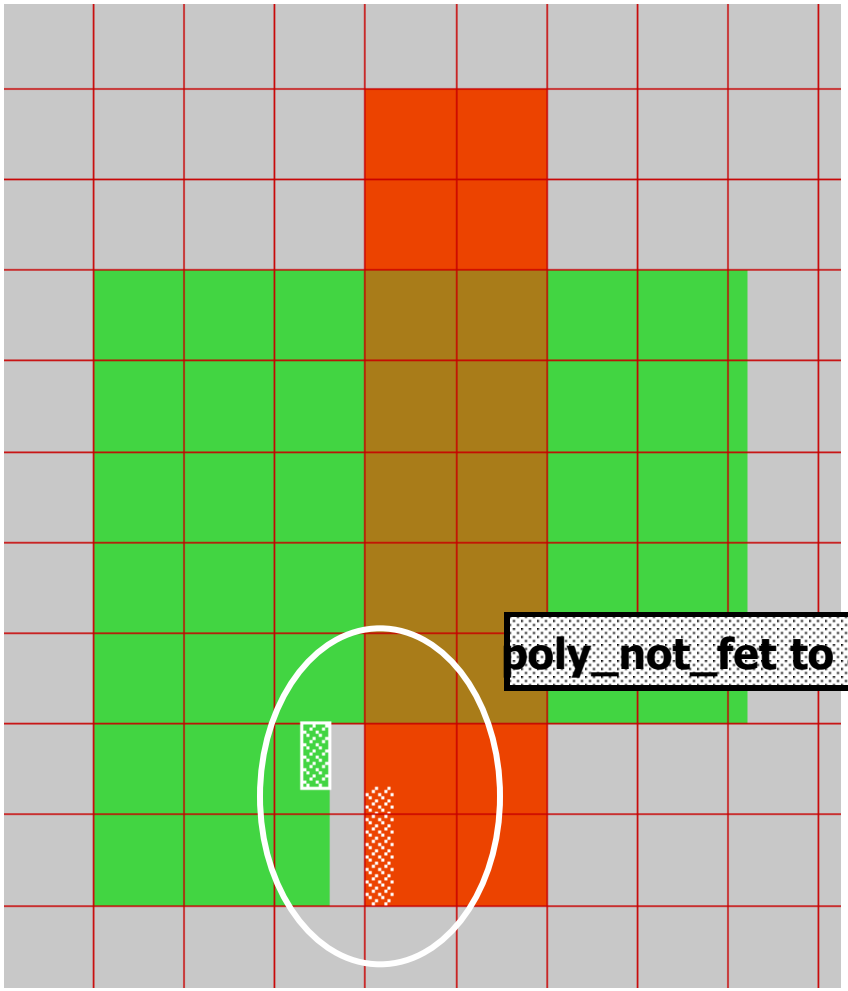


Simplified Layouts in *max*

- Online design rule checking (DRC)
- Automatic fet generation (just overlap poly and diffusion and it creates a transistor)
- Simplified via/contact generation
  - v12, v23, v34, v45
  - ct, nwc, pwc



Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um

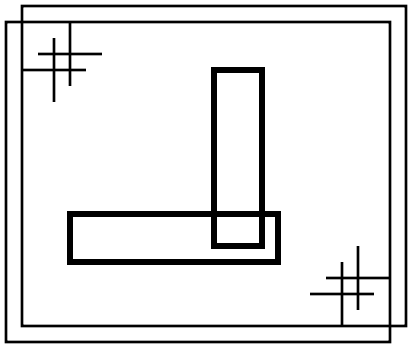
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

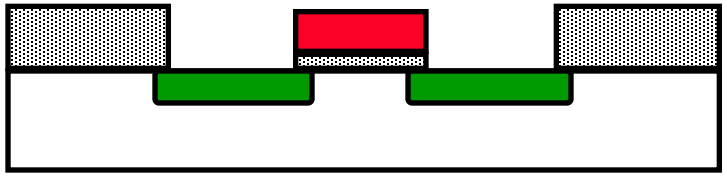
- To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

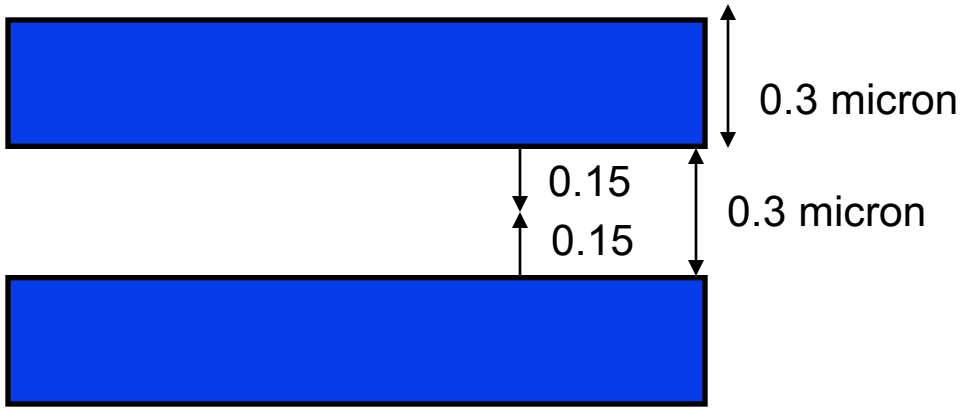
3. Process parameters (e.g., lateral diffusion)



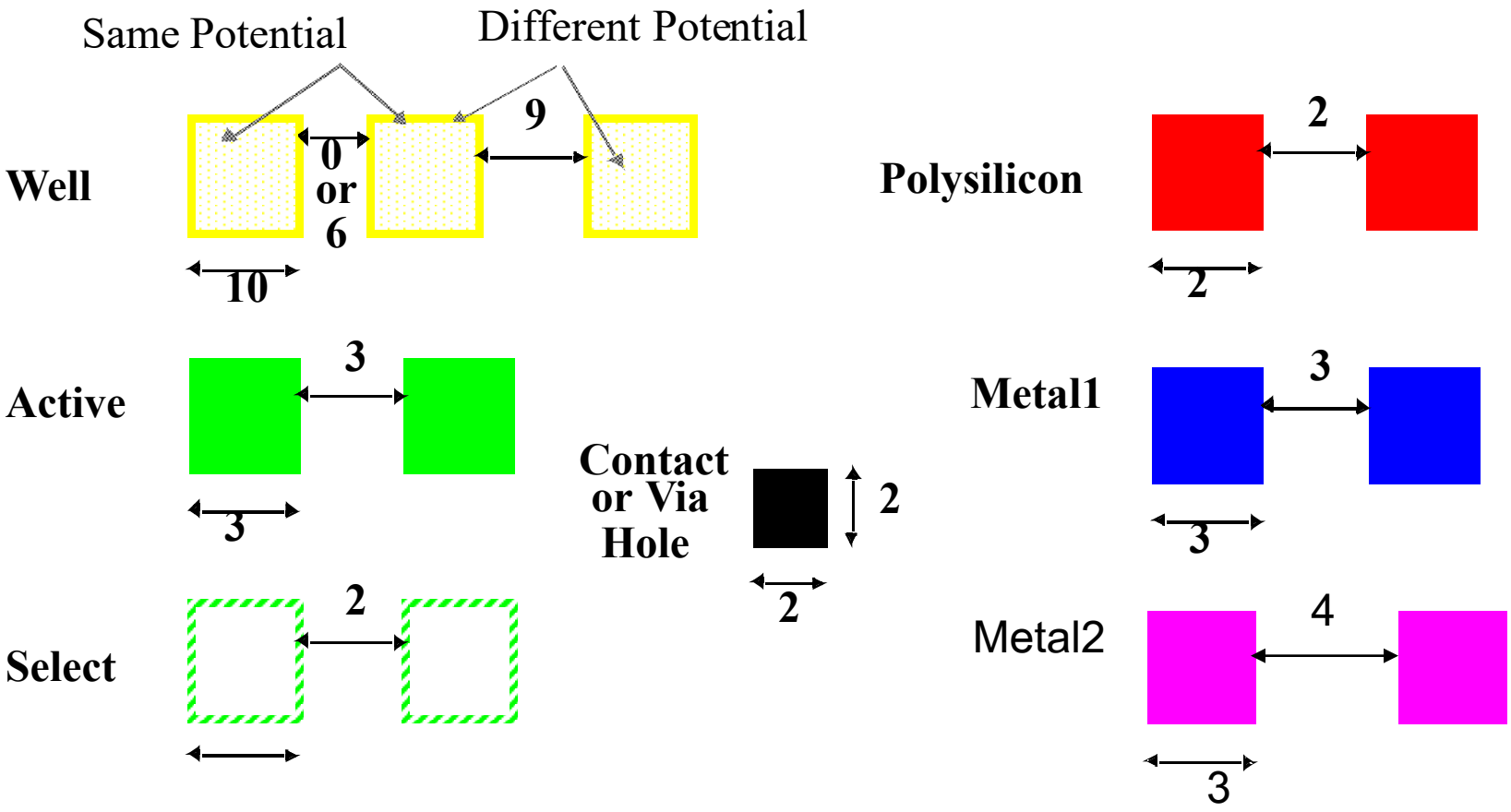
4. Rough surfaces

Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



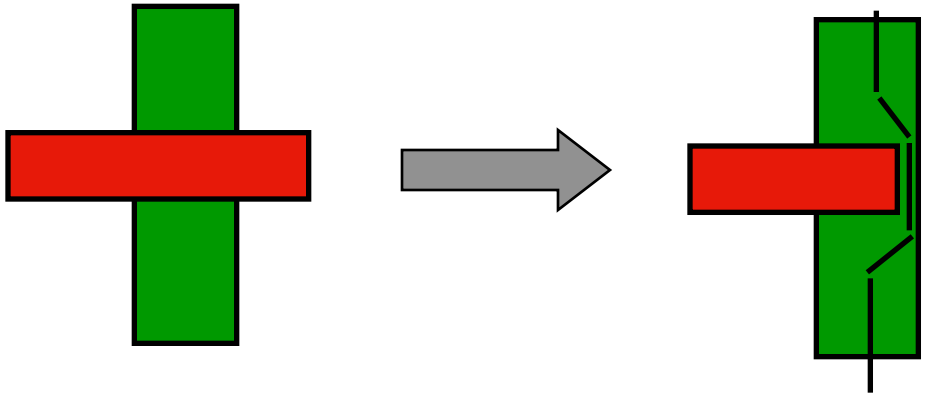
Intra-Layer Design Rules



Inter-Layer Design Rule Origins

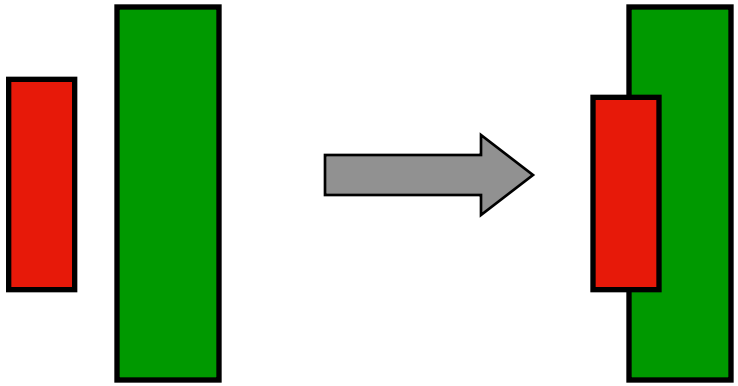
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors



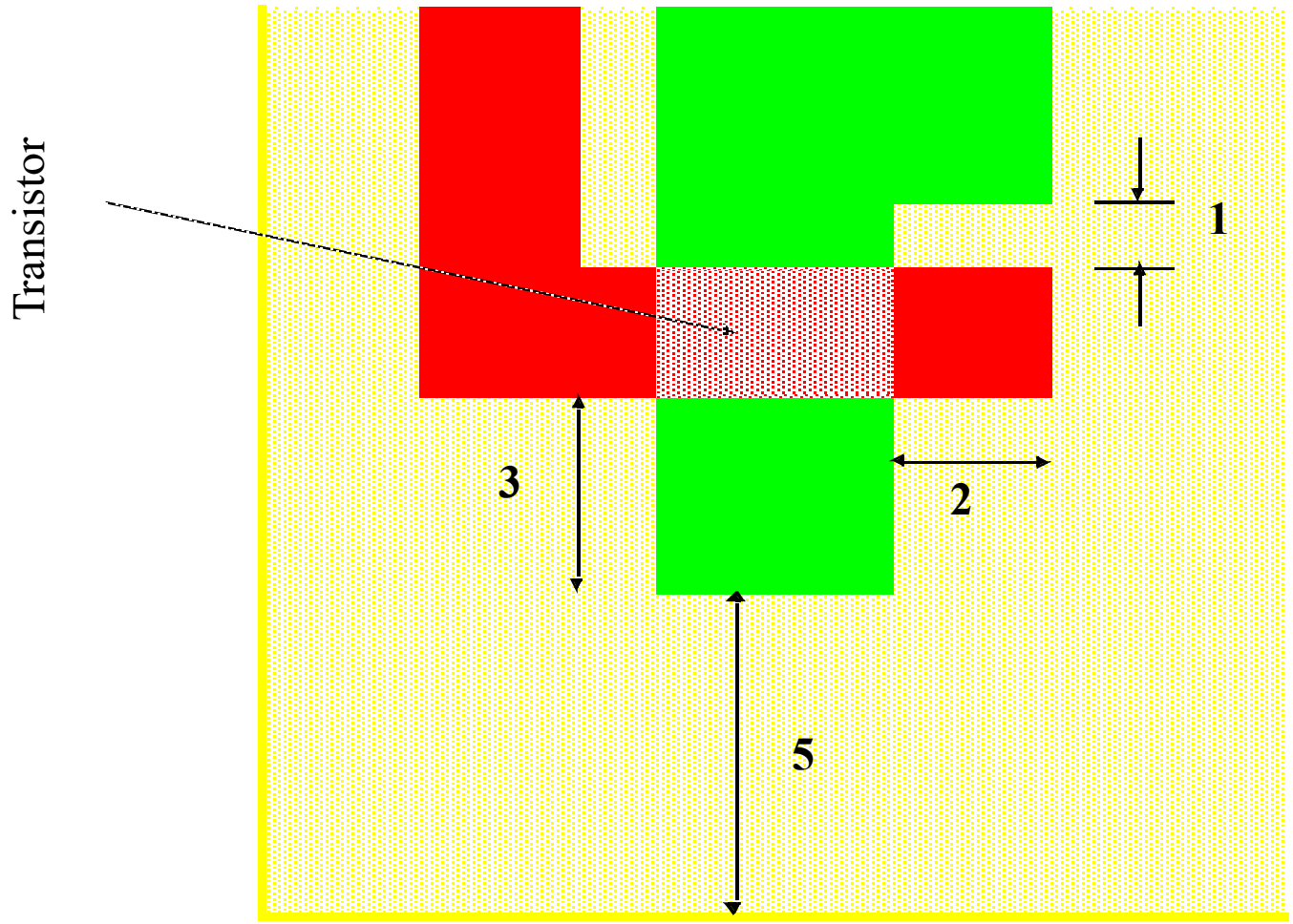
Catastrophic error

Unrelated Poly & Diffusion

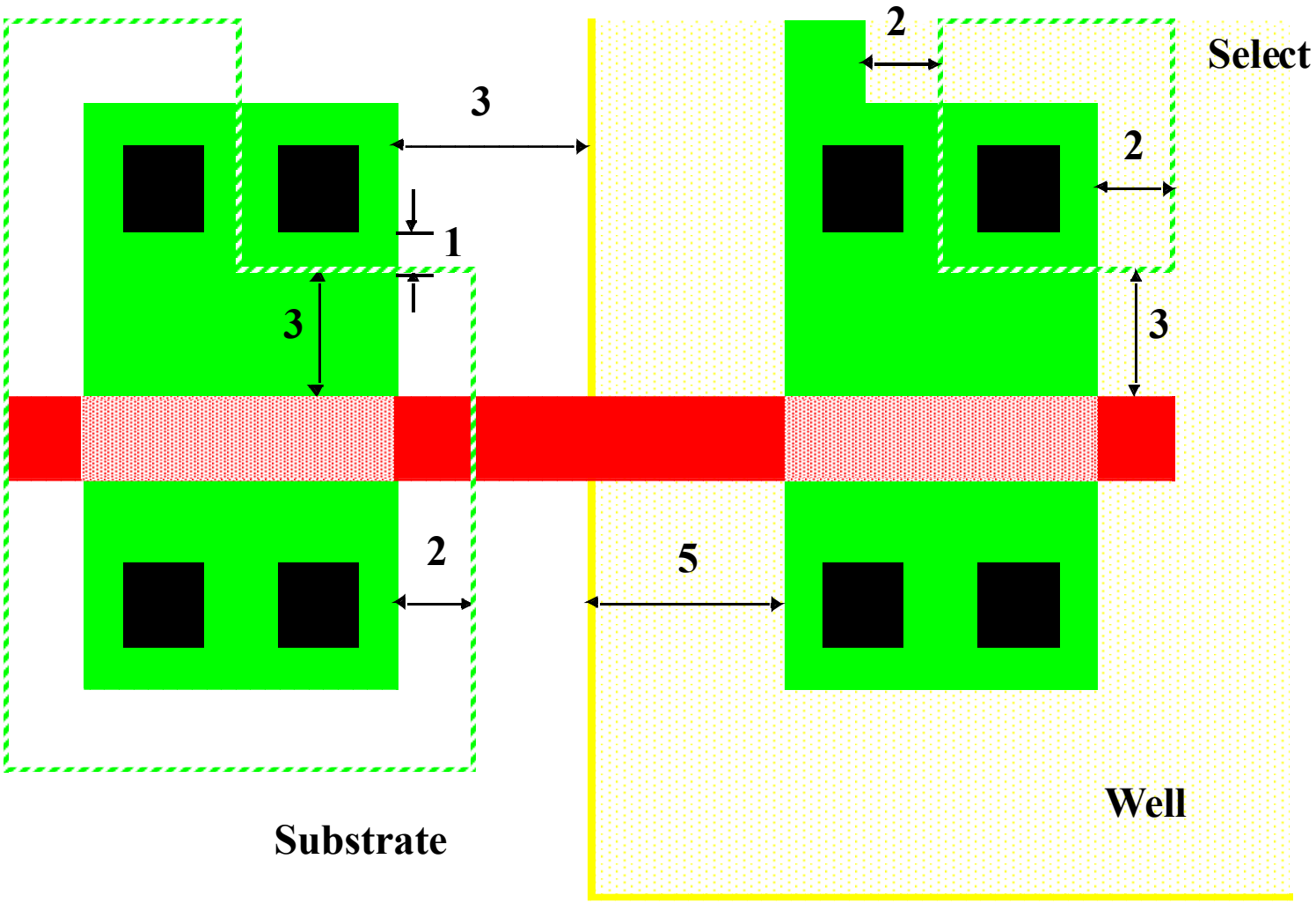


Thinner diffusion, but still working

Transistor Layout



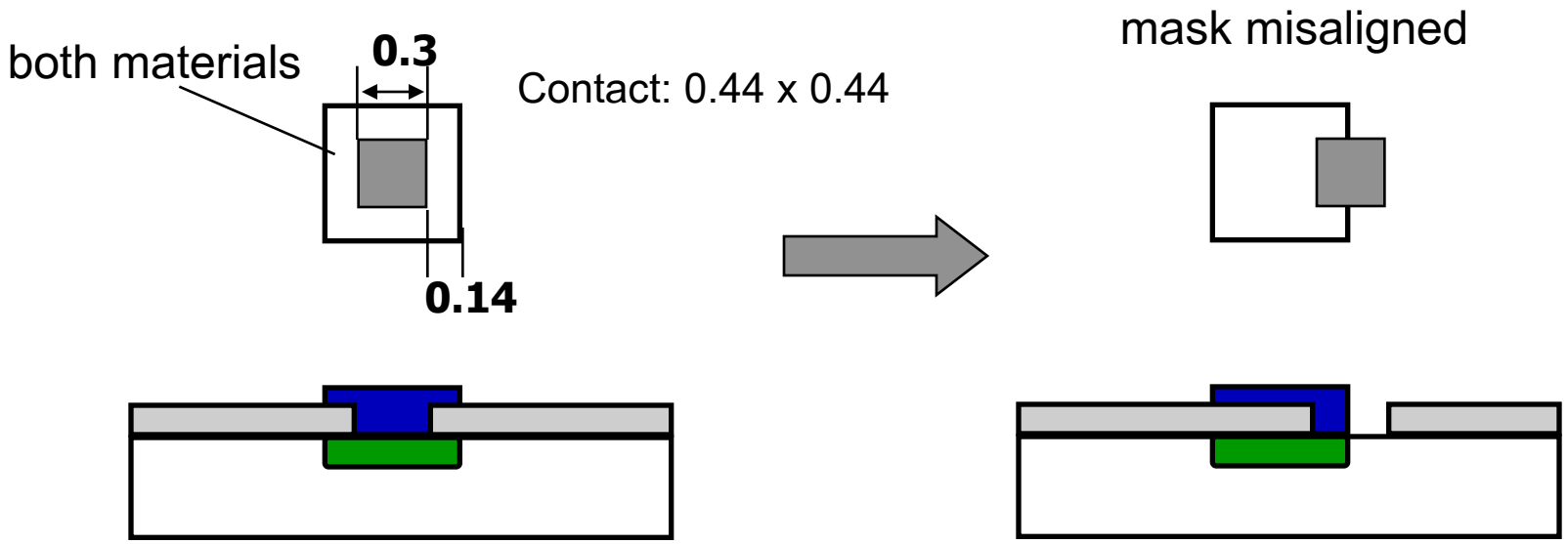
Select Layer



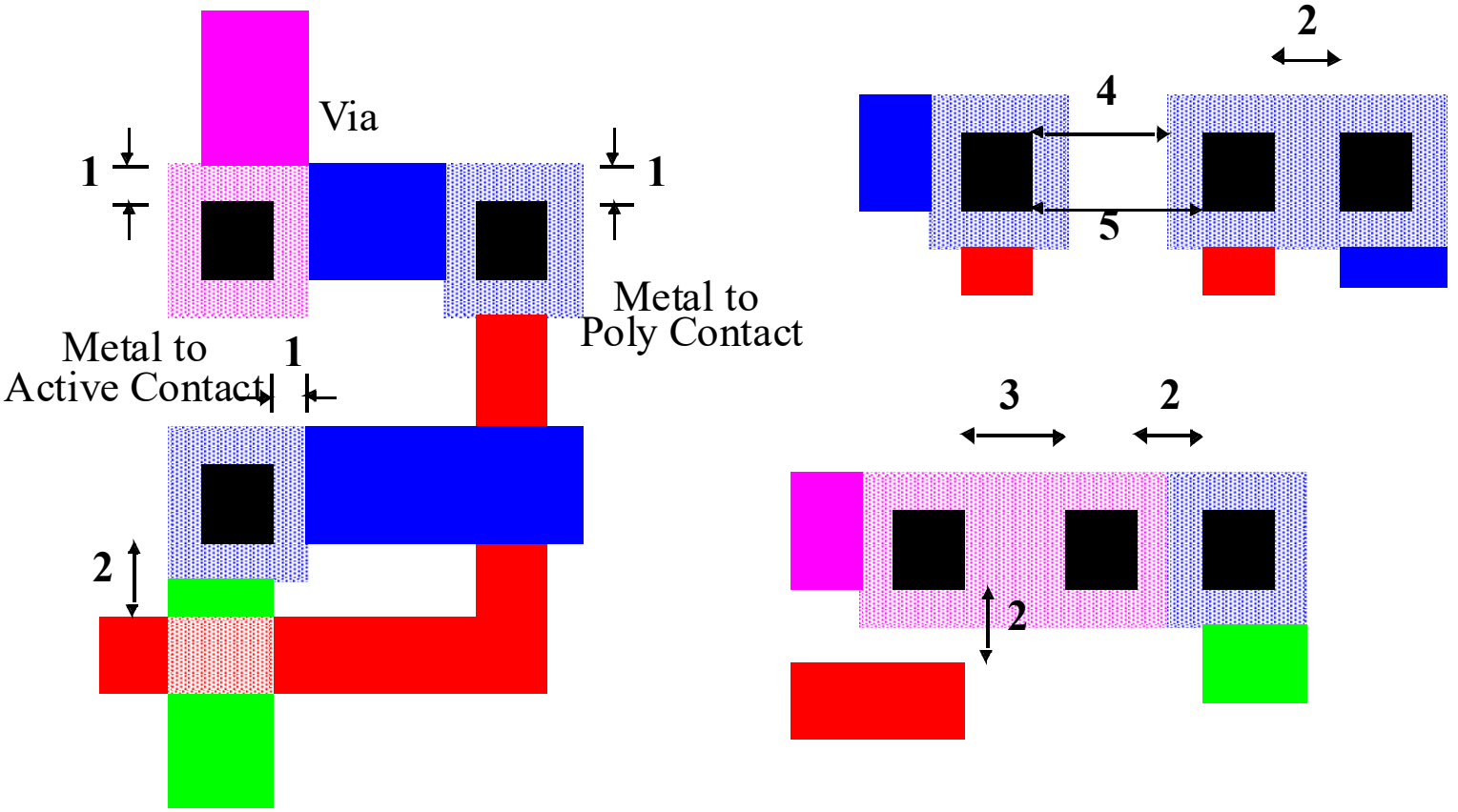
Inter-Layer Design Rule Origins, Con't

2. Contact and via rules

M1 contact to p-diffusion M1 contact to n-diffusion M1 contact to poly	Contact Mask
Mx contact to My	Via Masks



Vias and Contacts



Next Lecture and Reminders

- Next lecture
  - Static complementary CMOS gate design
    - Reading assignment – Rabaey, et al, 6.1-6.2.1

- Reminders
  - Project Title due September 12th (next class!)
  - HW2 due September 24th
  - Evening midterm exam scheduled
    - Wednesday, October 10th from 8:15 to 10:15pm in 260 Willard
    - Only one midterm conflict filed for so far