CSE477
VLSI Digital Circuits
Fall 2002

Lecture 17: Static Sequential Circuits

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: How to Choose a Logic Style

- Must consider ease of design, robustness (noise immunity), area, speed, power, system clocking requirements, fan-out, functionality, ease of testing

4-input NAND

Style	# Trans	Ease	Ratioed ?	Delay	Power
Comp Static	8	1	no	3	1
CPL*	12 + 2	2	no	4	3
domino	6 + 2	4	no	2	2 + clk
DCVSL*	10	3	yes	1	4

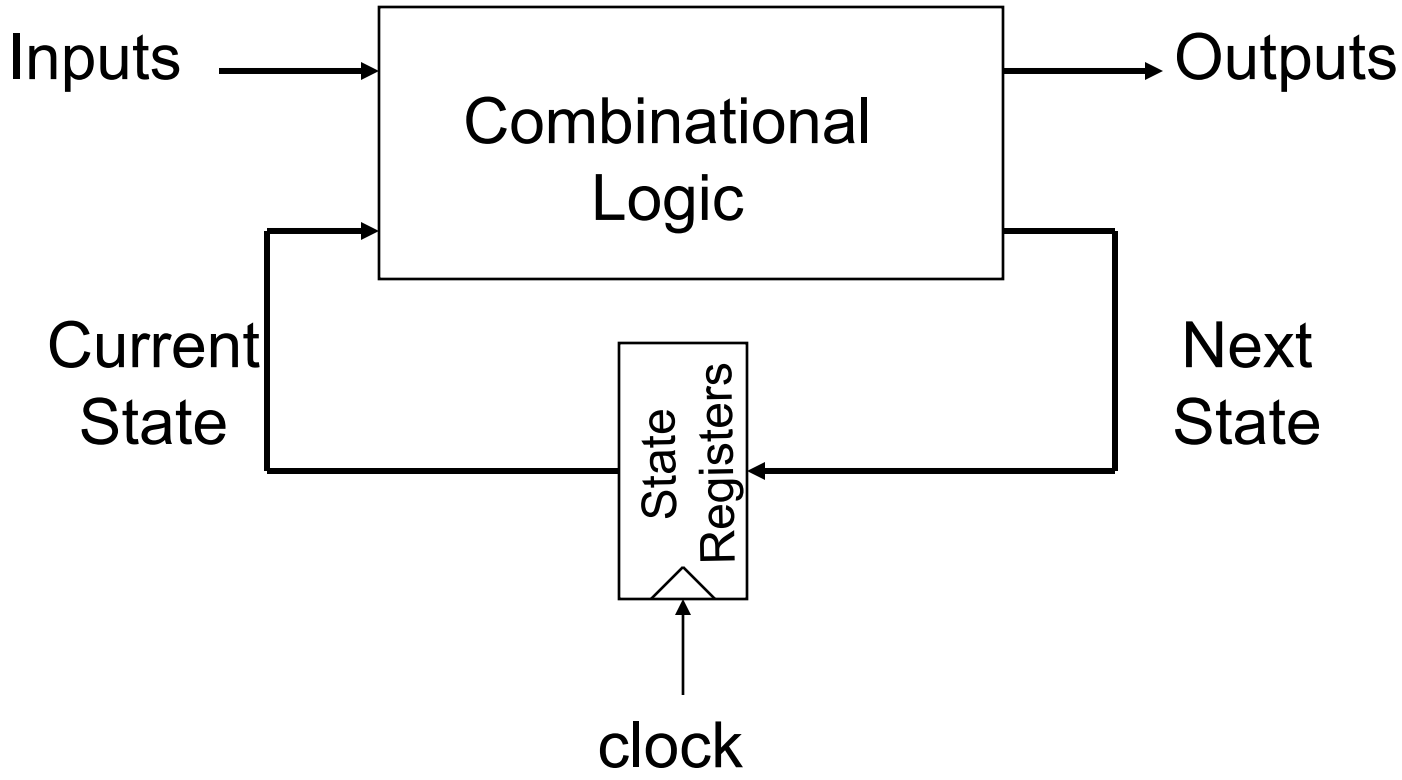
* Dual Rail

- Current trend is towards an increased use of complementary static CMOS: design support through DA tools, robust, more amenable to voltage scaling.

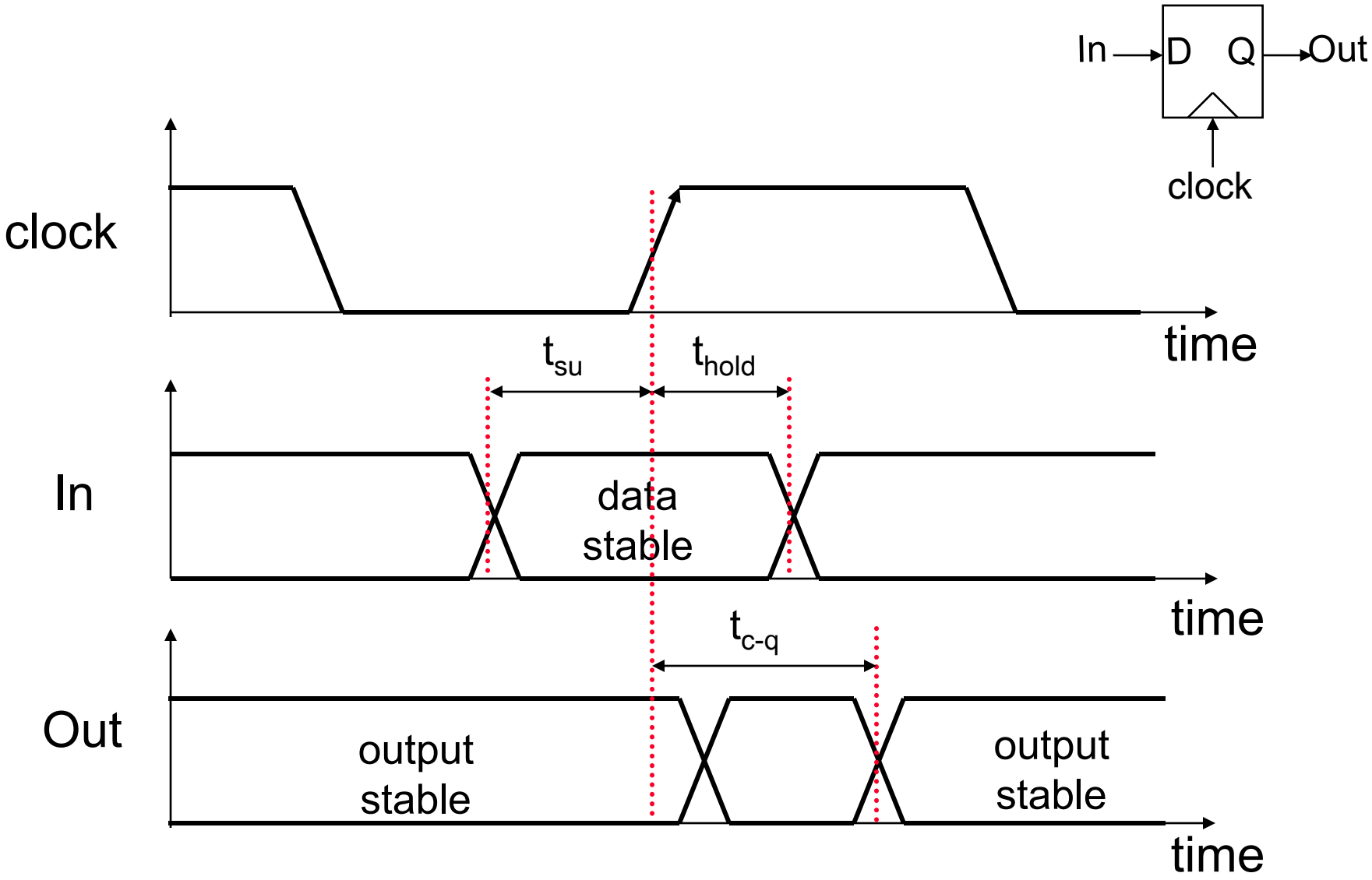
A time was probably coming when components would operate so quickly that the distance that signals had to travel would intimately affect the speed of most commercial computers. Then miniaturization and speed would become more nearly synonymous.

The Soul of a New Machine, Kidder, pg. 160

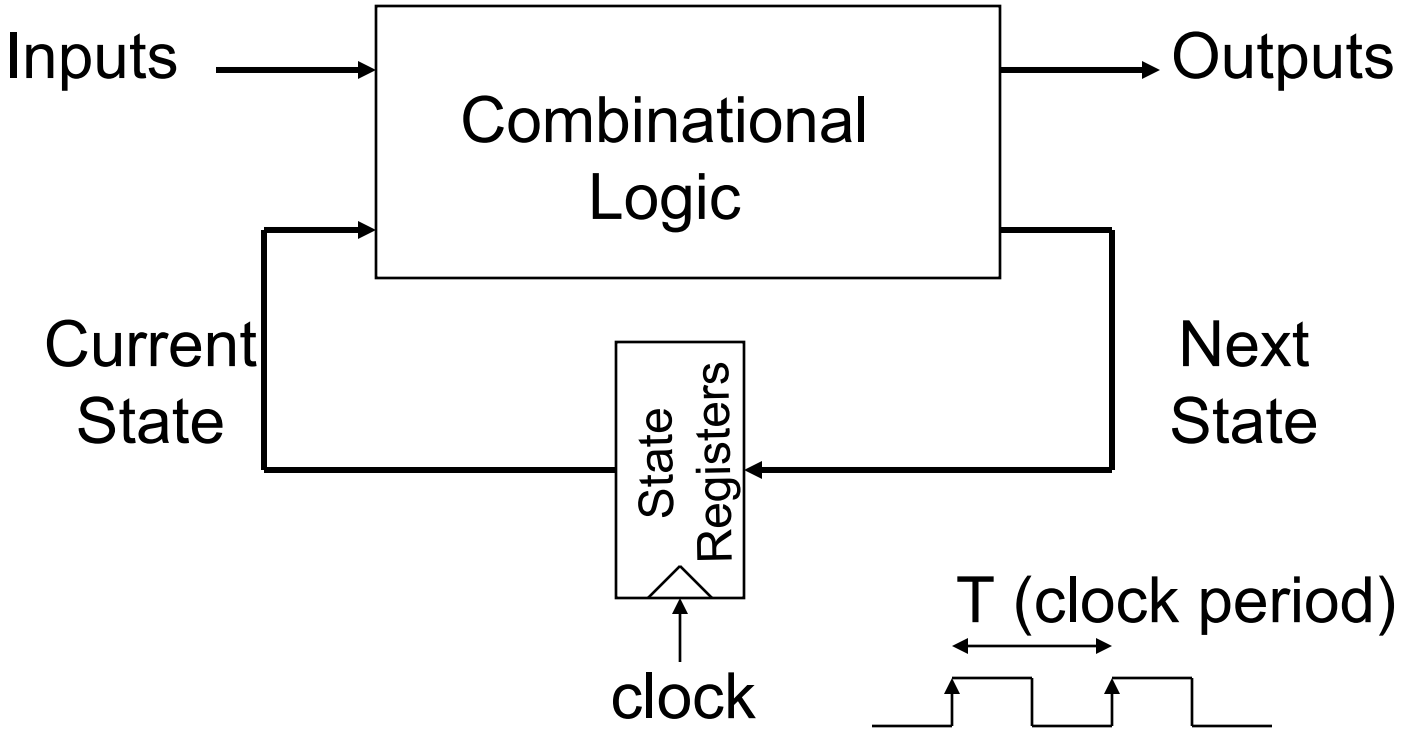
Sequential Logic



Timing Metrics



System Timing Constraints



$$t_{cdreg} + t_{cdlogic} \geq t_{hold}$$

$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

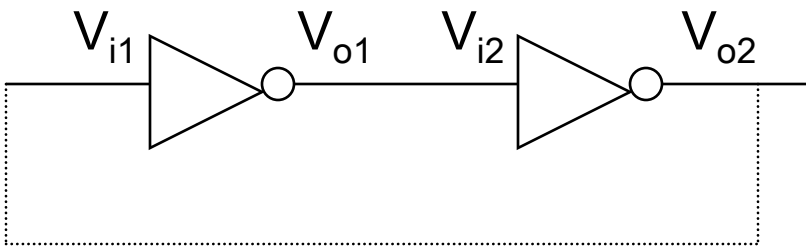
Static vs Dynamic Storage

- Static storage
  - preserve state as long as the power is on
  - have positive feedback (regeneration) with an internal connection between the output and the input
  - useful when updates are infrequent (clock gating)
- Dynamic storage
  - store state on parasitic capacitors
  - only hold state for short periods of time (milliseconds)
  - require periodic refresh
  - usually simpler, so higher speed and lower power

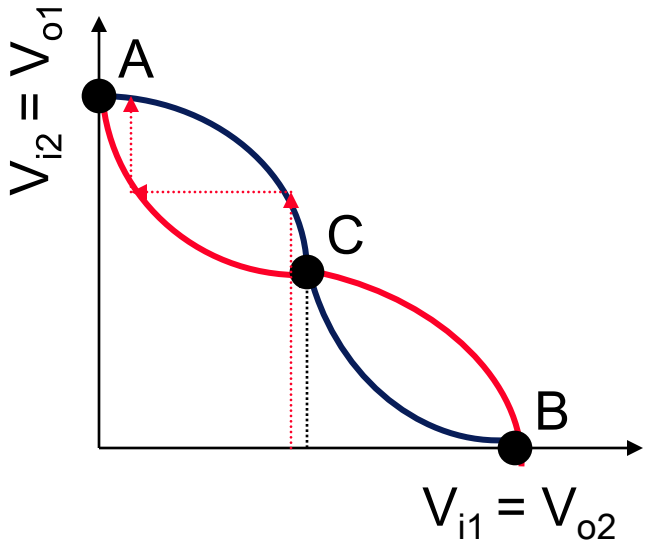
Latches vs Flipflops

- Latches
  - level sensitive circuit that passes inputs to Q when the clock is high (or low) - transparent mode
  - input sampled on the falling edge of the clock is held stable when clock is low (or high) - hold mode
- Flipflops (edge-triggered)
  - edge sensitive circuits that sample the inputs on a clock transition
    - positive edge-triggered: $0 \rightarrow 1$
    - negative edge-triggered: $1 \rightarrow 0$
  - built using latches (e.g., master-slave flipflops)

Review: The Regenerative Property



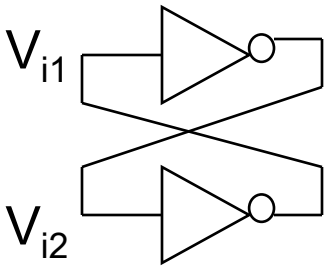
cascaded inverters



If the gain in the transient region is larger than 1, only A and B are stable operation points. C is a metastable operation point.

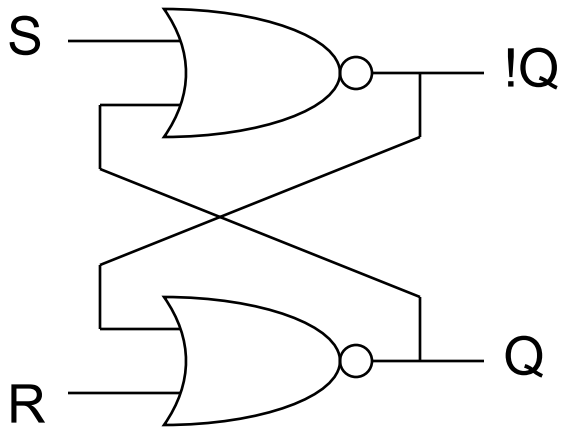
Bistable Circuits

- The cross-coupling of two inverters results in a bistable circuit (a circuit with two stable states)



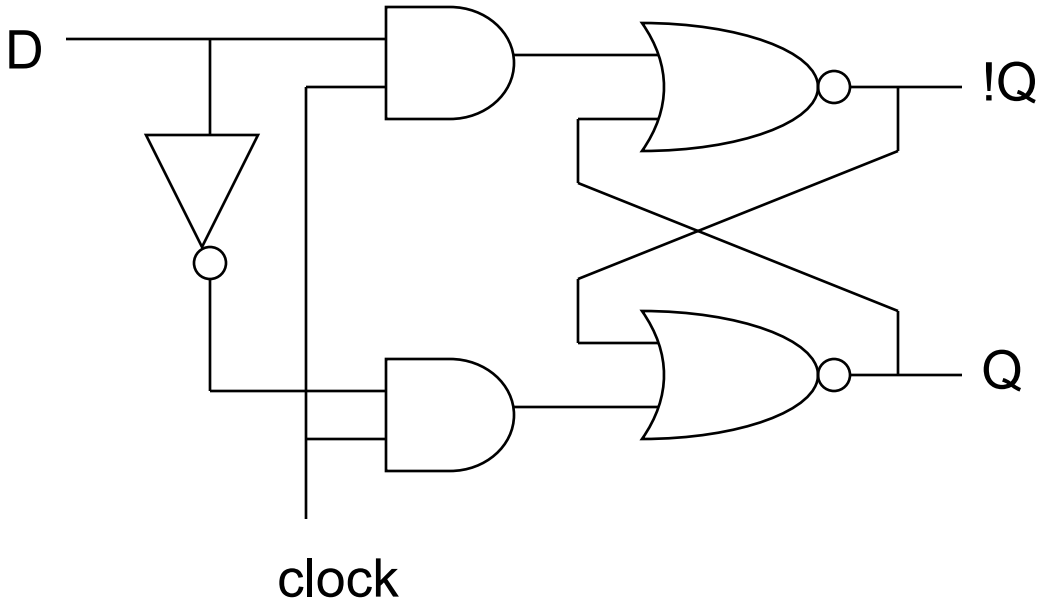
- Have to be able to change the stored value by making A (or B) temporarily unstable by increasing the loop gain to a value larger than 1
  - done by applying a trigger pulse at V_{i1} or V_{i2}
  - the width of the trigger pulse need be only a little larger than the total propagation delay around the loop circuit (twice the delay of an inverter)
- Two approaches used
  - cutting the feedback loop (mux based latch)
  - overpowering the feedback loop (as used in SRAMs)

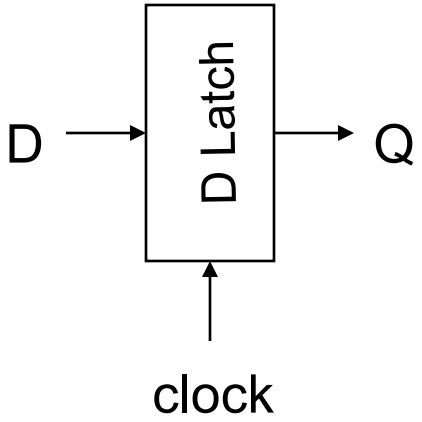
Review (from CSE 271): SR Latch

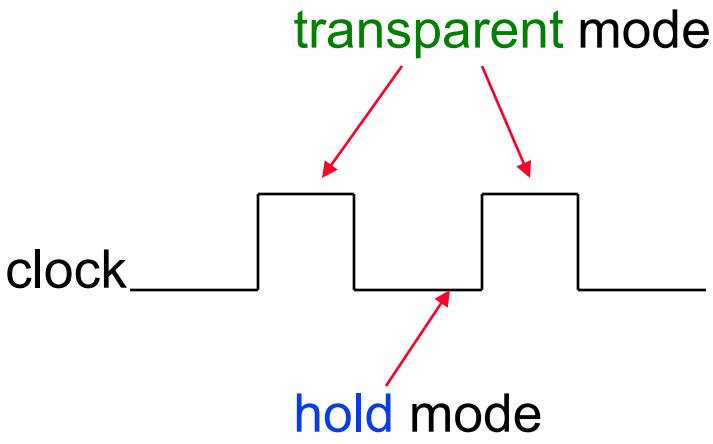


S	R	Q	!Q	
0	0	Q	!Q	memory
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	disallowed

Review (from CSE 271): Clocked D Latch

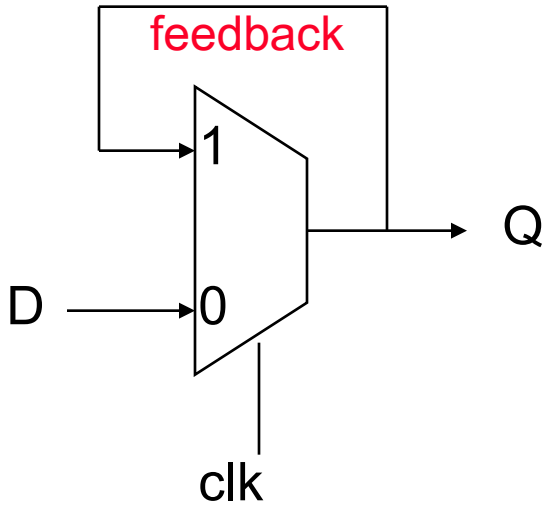






MUX Based Latches

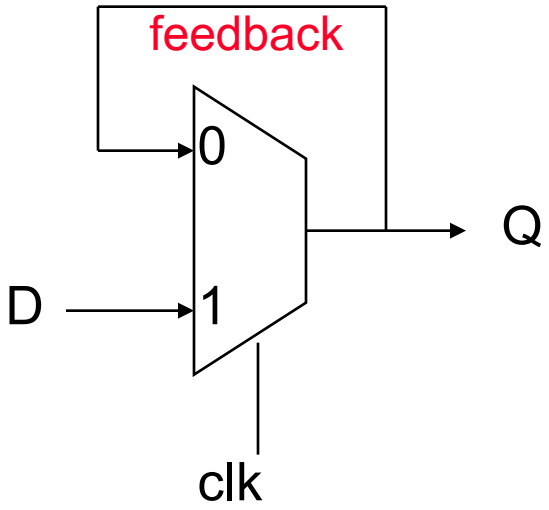
- Change the stored value by cutting the feedback loop



Negative Latch

Q = clk & Q | !clk & D

transparent when the clock is low

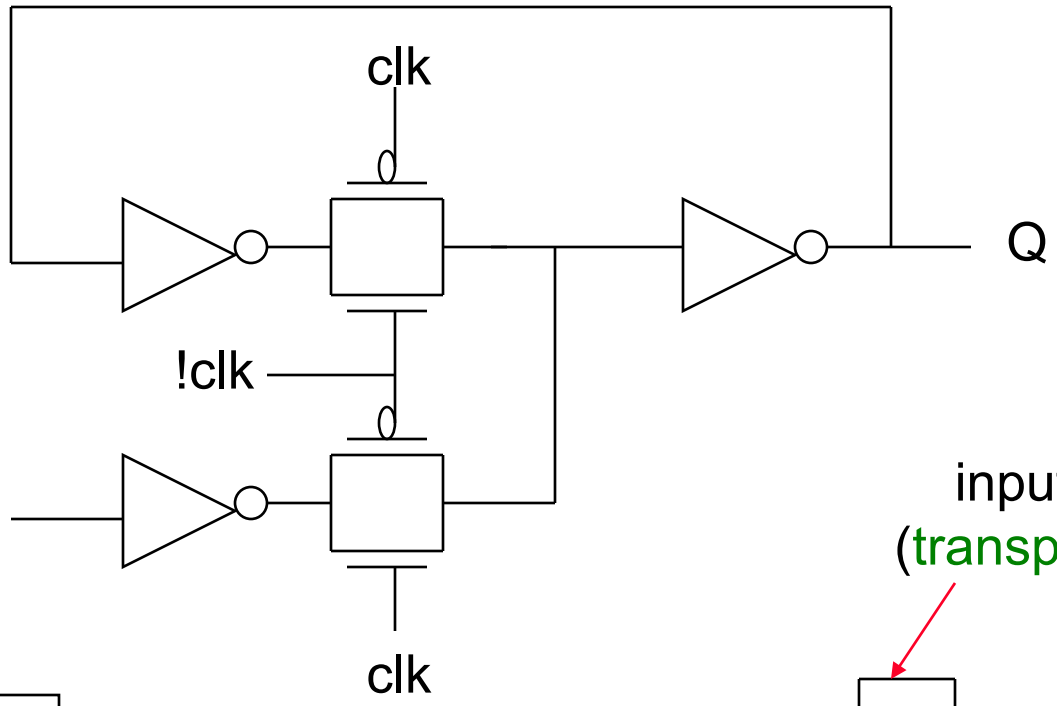


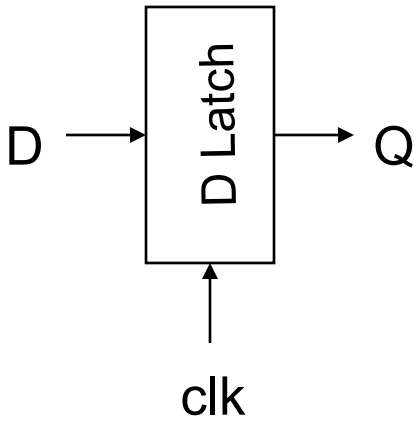
Positive Latch

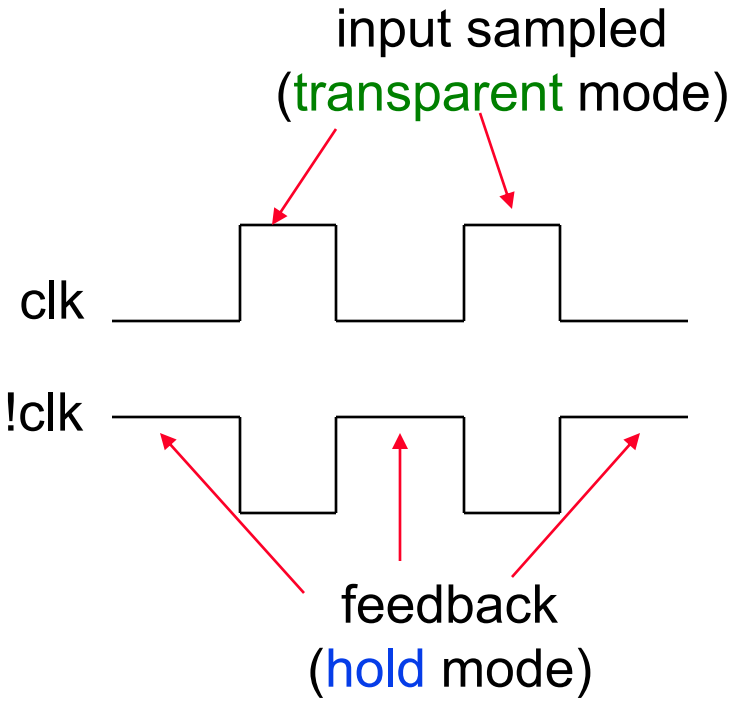
Q = !clk & Q | clk & D

transparent when the clock is high

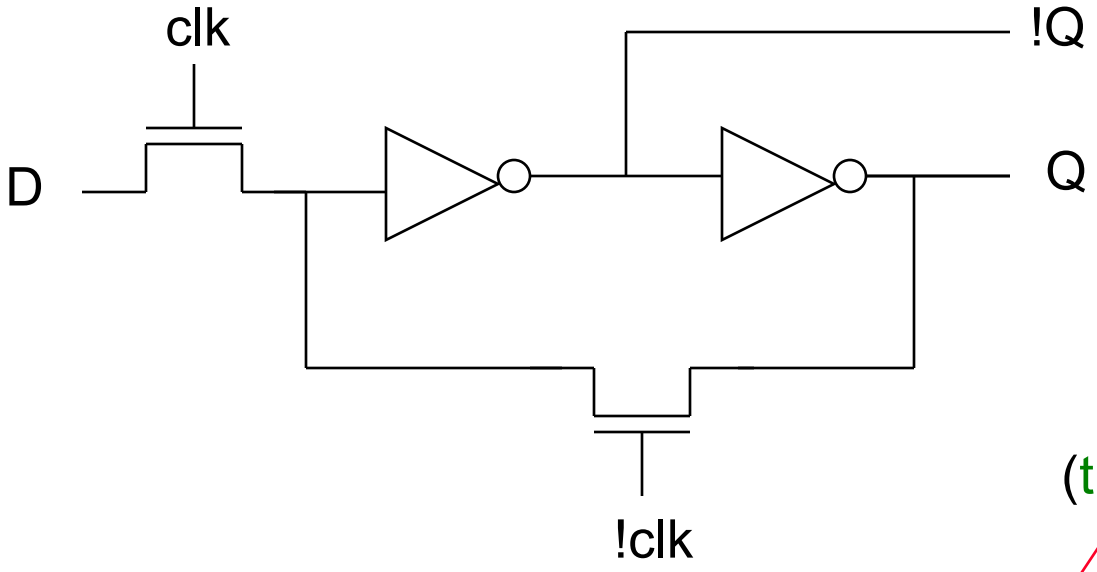
TG MUX Based Latch Implementation



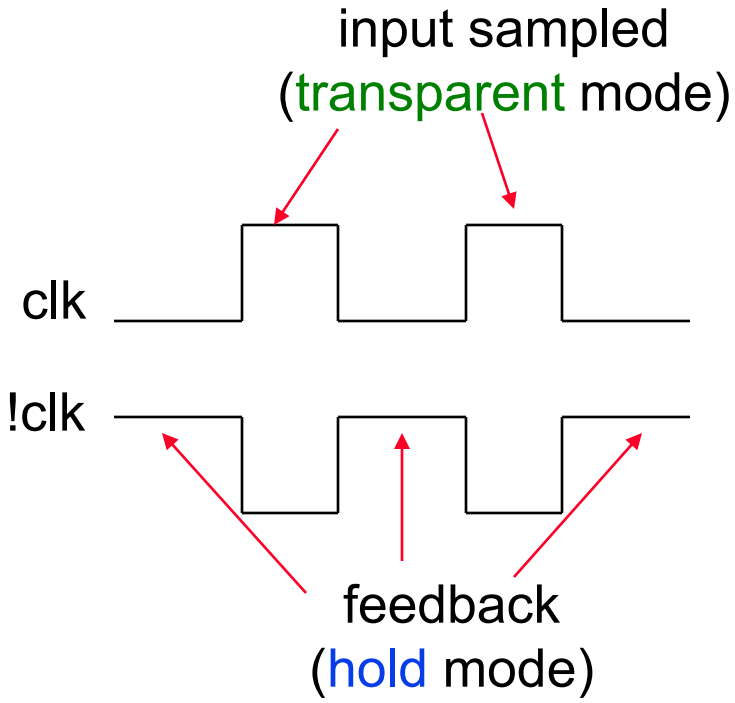




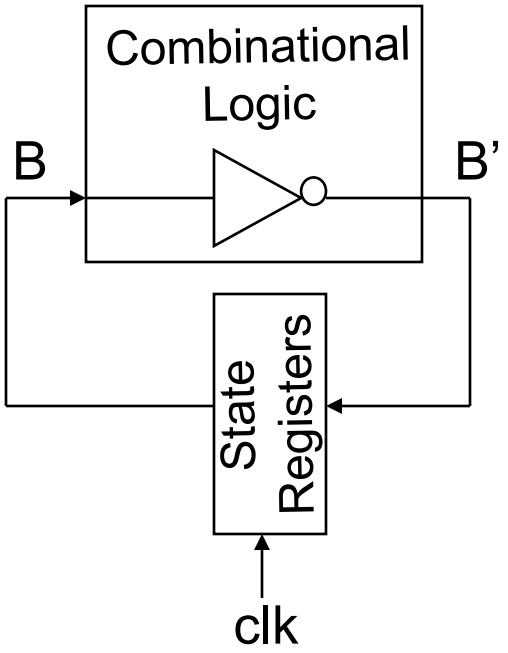
PT MUX Based Latch Implementation

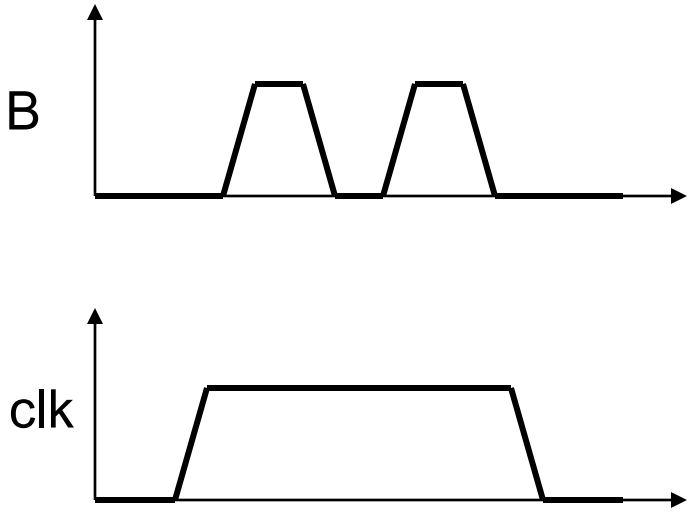


- Reduced clock load, but threshold drop at output of pass transistors so reduced noise margins and performance



Latch Race Problem





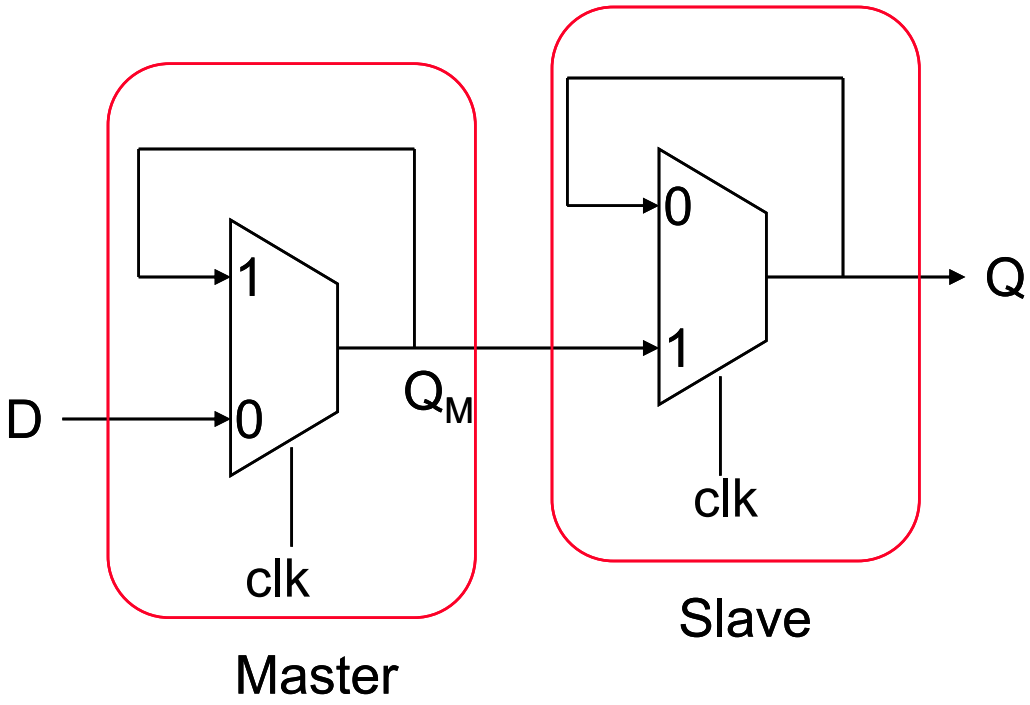
Which value of B is stored?

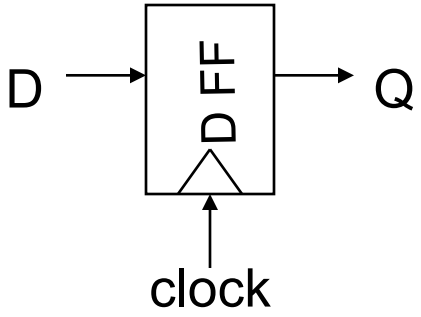
Two-sided clock constraint

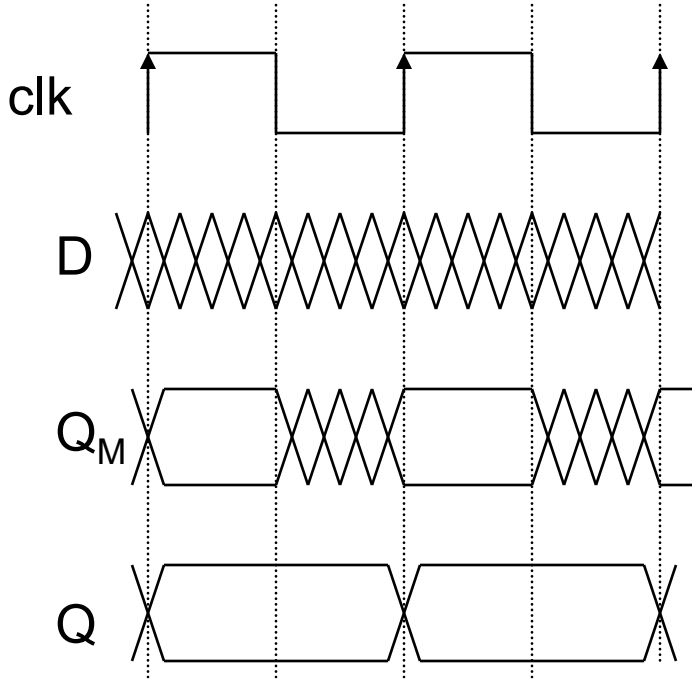
$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

$$T_{high} < t_{c\text{-}q} + t_{cdlogic}$$

Master Slave Based ET Flipflop



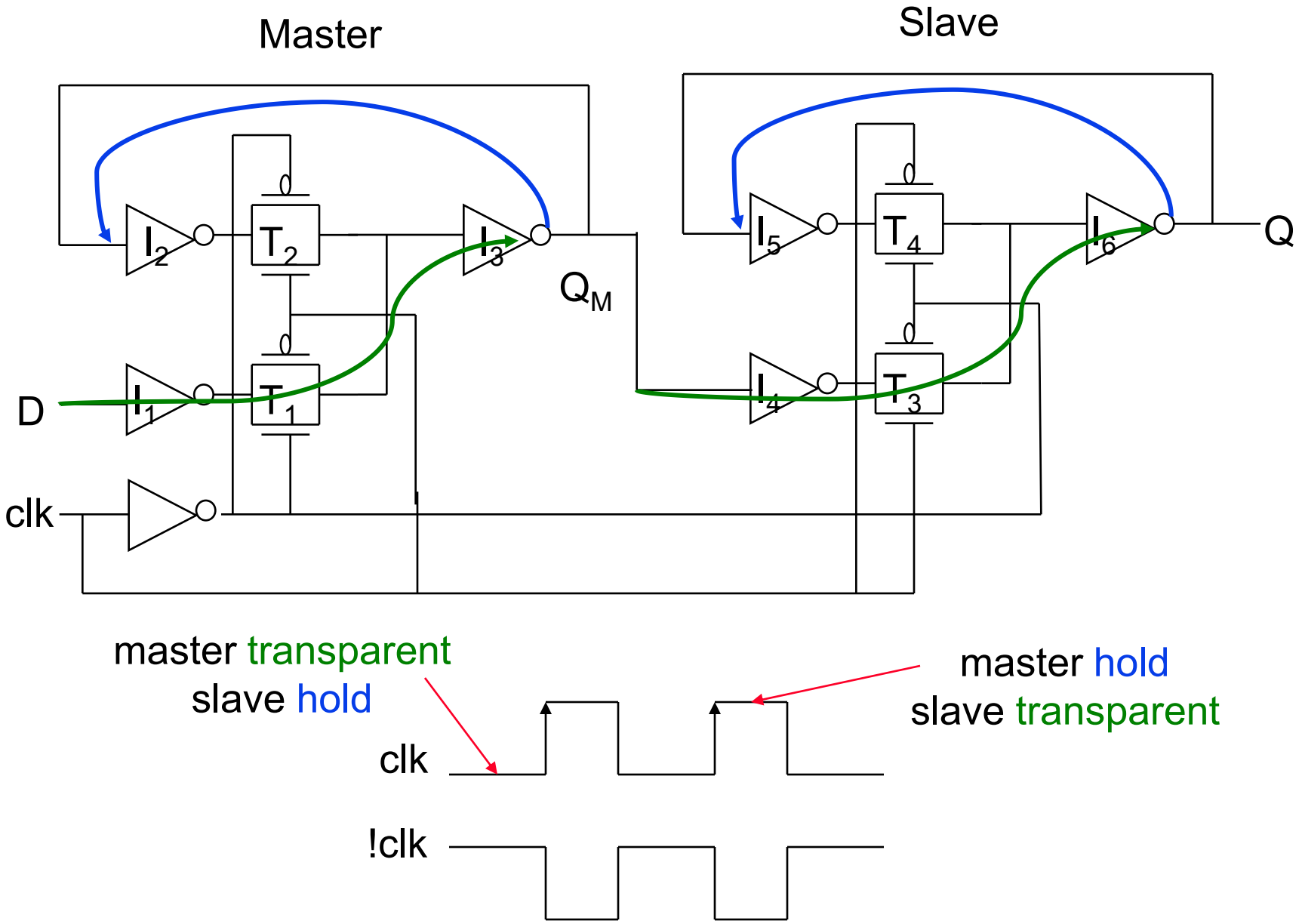




clk = 0 transparent hold

clk = 0→1 hold transparent

MS ET Implementation



MS ET Timing Properties

- Assume propagation delays are t_{pd_inv} and t_{pd_tx}, that the contamination delay is 0, and that the inverter delay to derive !clk is 0
- Set-up time - time before rising edge of clk that D must be valid

$$3 * t_{pd\_inv} + t_{pd\_tx}$$

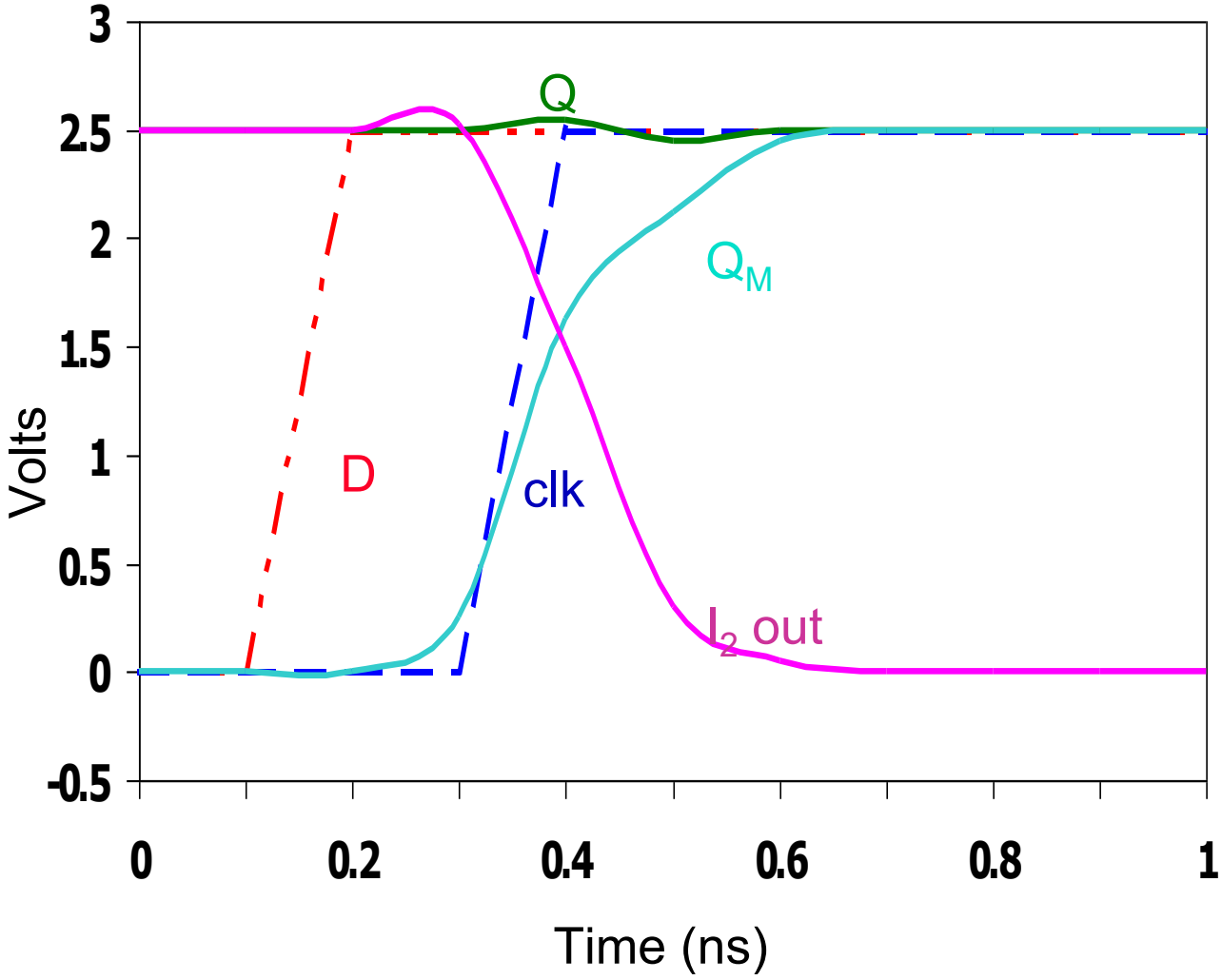
- Propagation delay - time for Q_M to reach Q

$$t_{pd\_inv} + t_{pd\_tx}$$

- Hold time - time D must be stable after rising edge of clk

zero

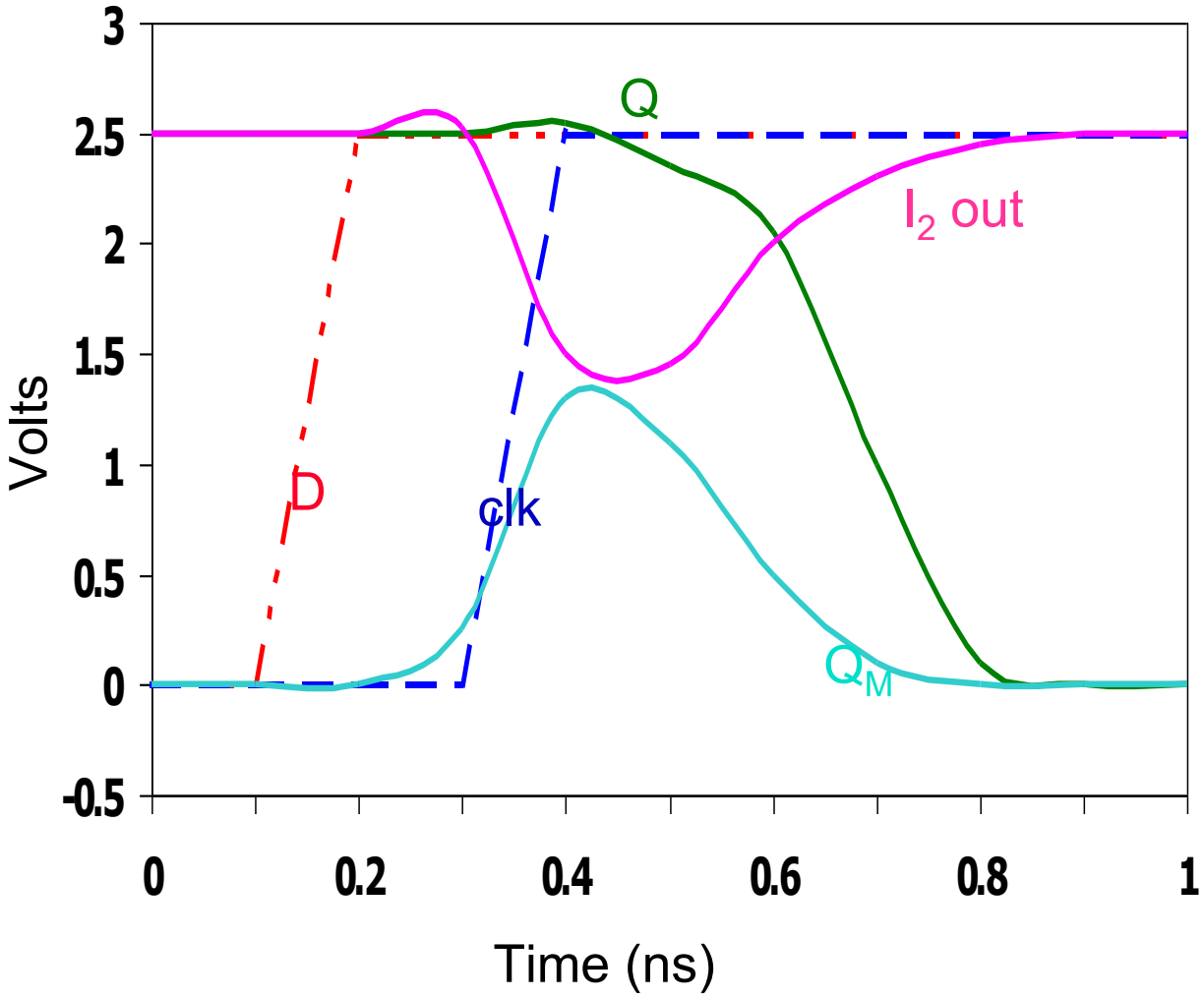
Set-up Time Simulation



t_{setup} = 0.21 ns

works correctly

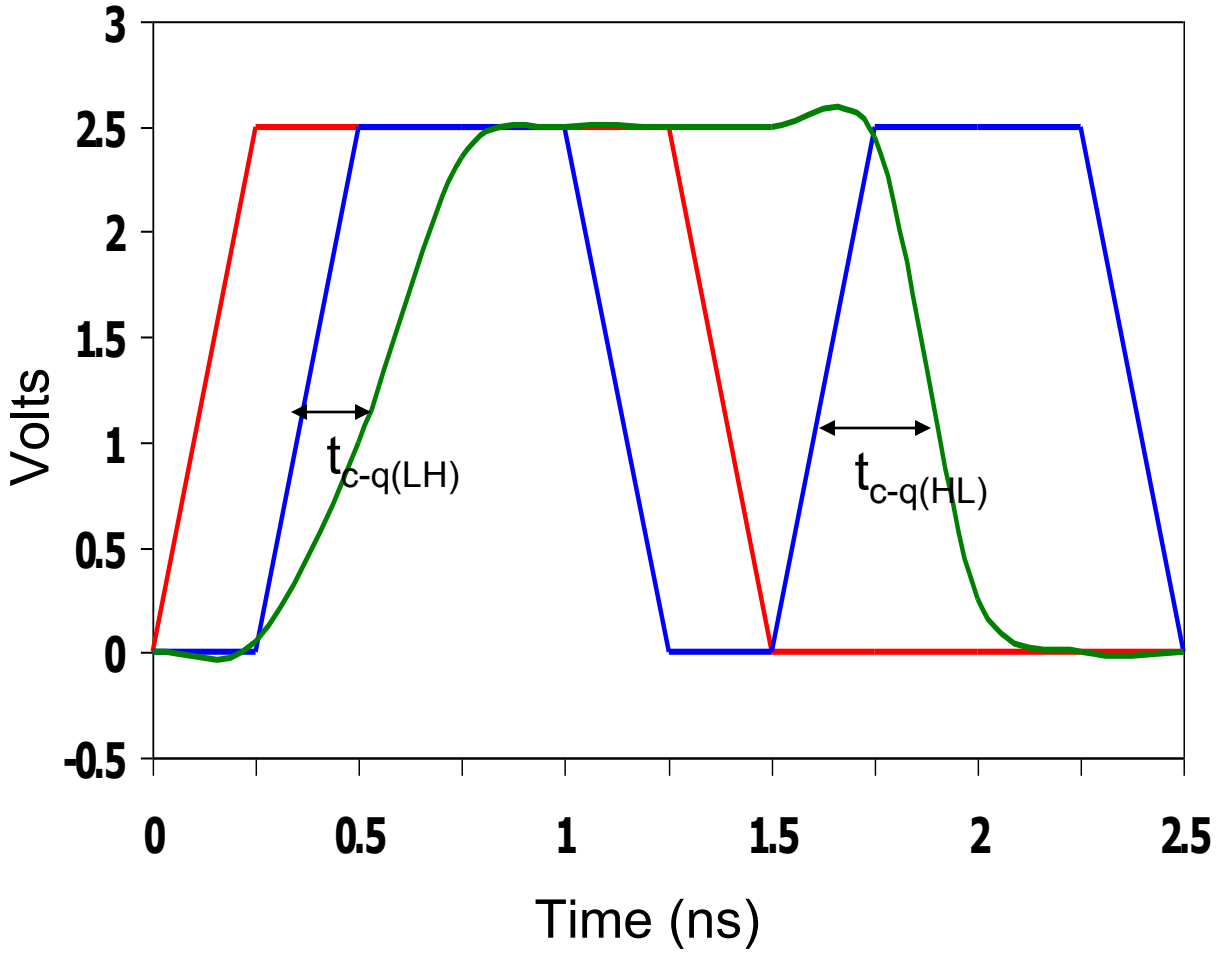
Set-up Time Simulation



t_{setup} = 0.20 ns

fails

Propagation Delay Simulation

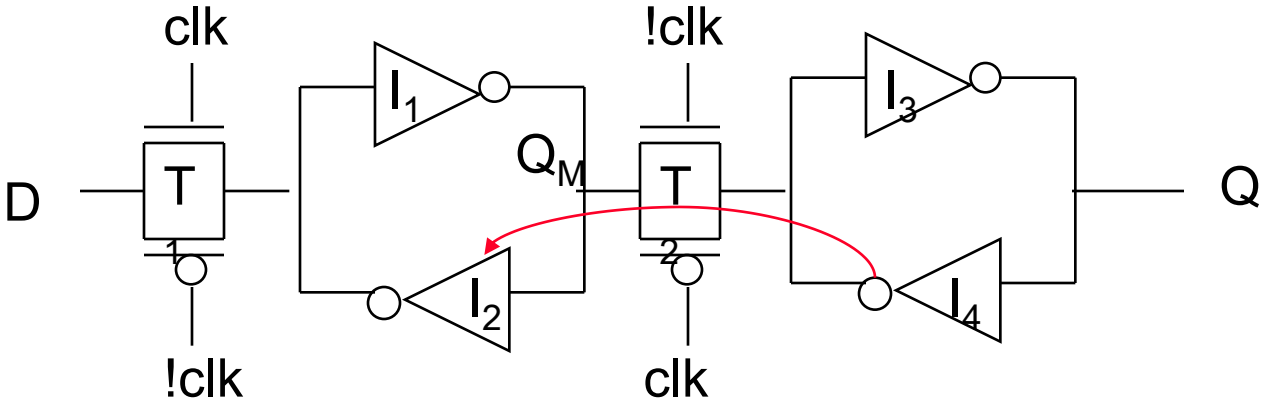


$t_{c\text{-}q(LH)}$ = 160 psec

$t_{c\text{-}q(HL)}$ = 180 psec

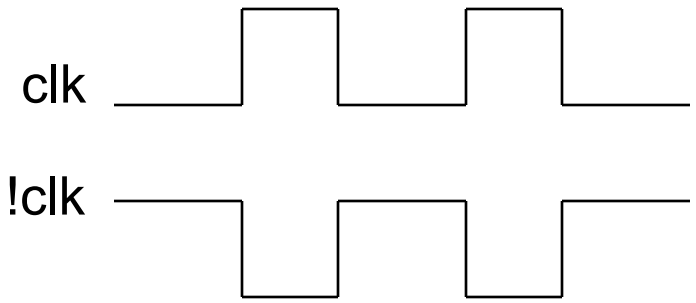
Reduced Load MS ET FF

- Clock load per register is important since it directly impacts the power dissipation of the clock network.
- Can reduce the clock load (at the cost of robustness) by making the circuit ratioed

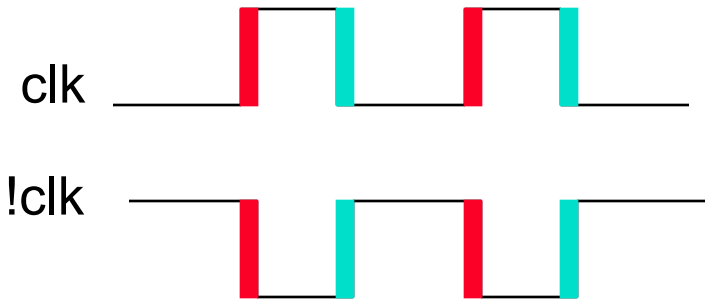


- to switch the state of the master, T_1 must be sized to overpower I_2
- to avoid reverse conduction, I_4 must be weaker than I_1

Non-Ideal Clocks



Ideal clocks



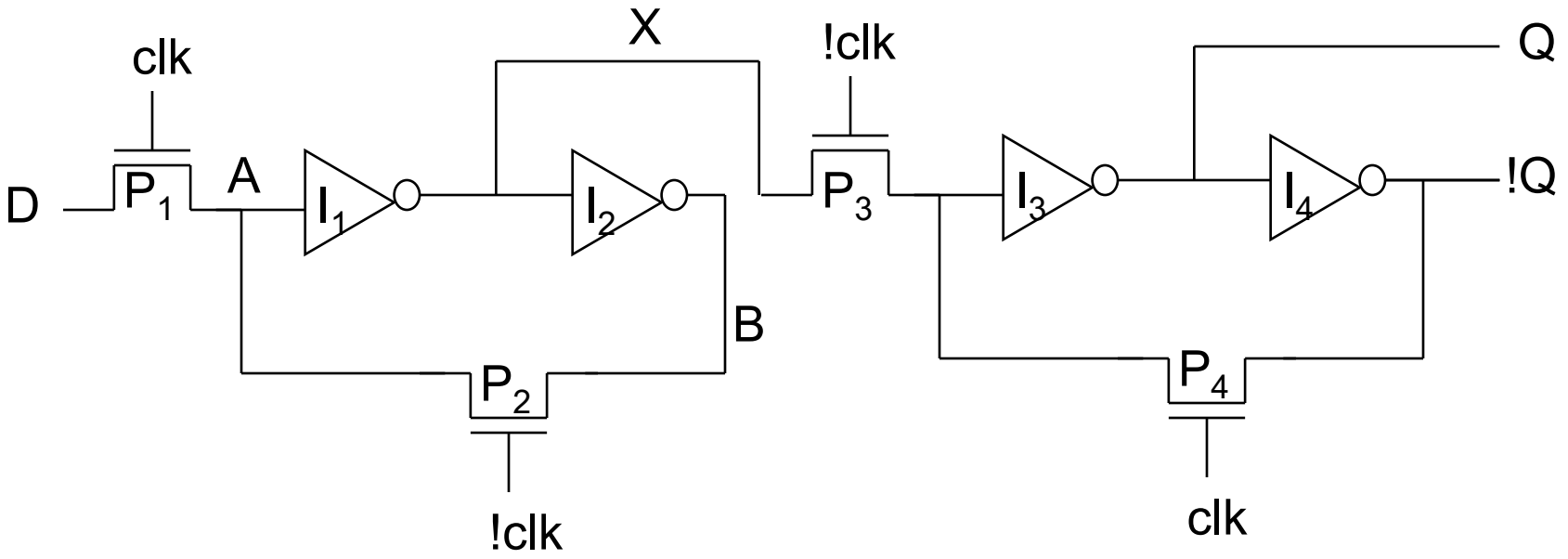
Non-ideal clocks

clock skew

1-1 overlap

0-0 overlap

Example of Clock Skew Problems

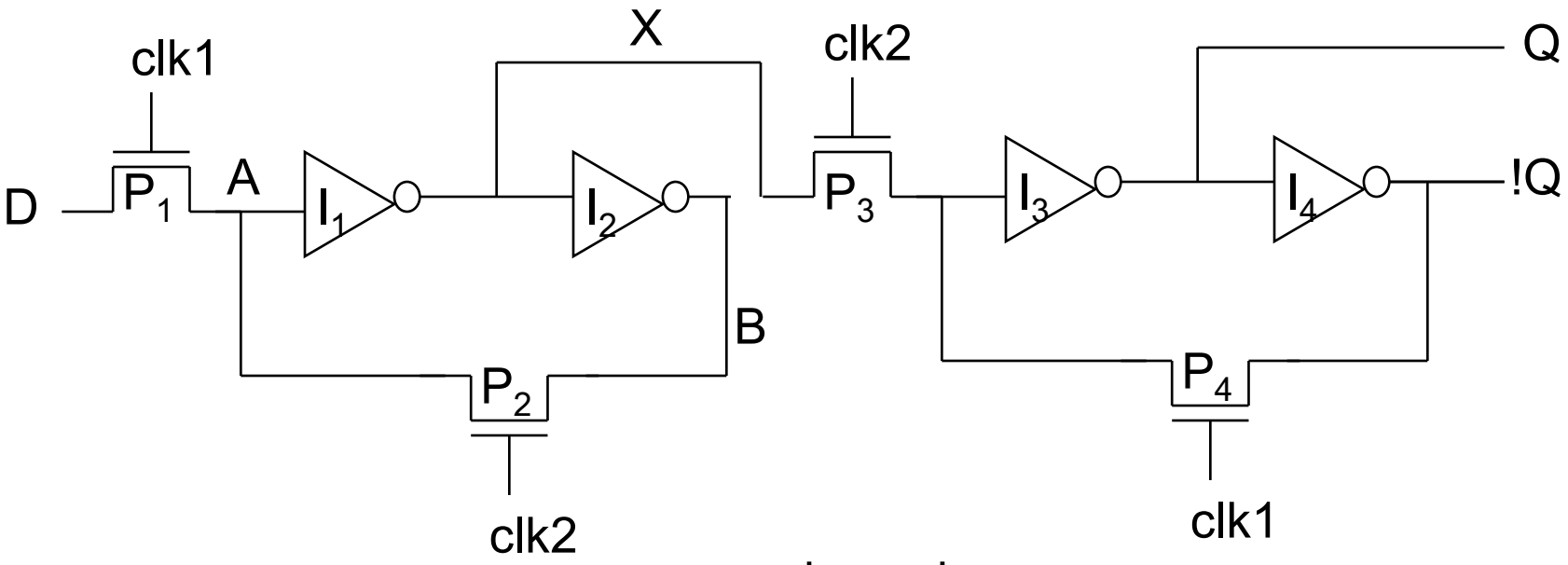


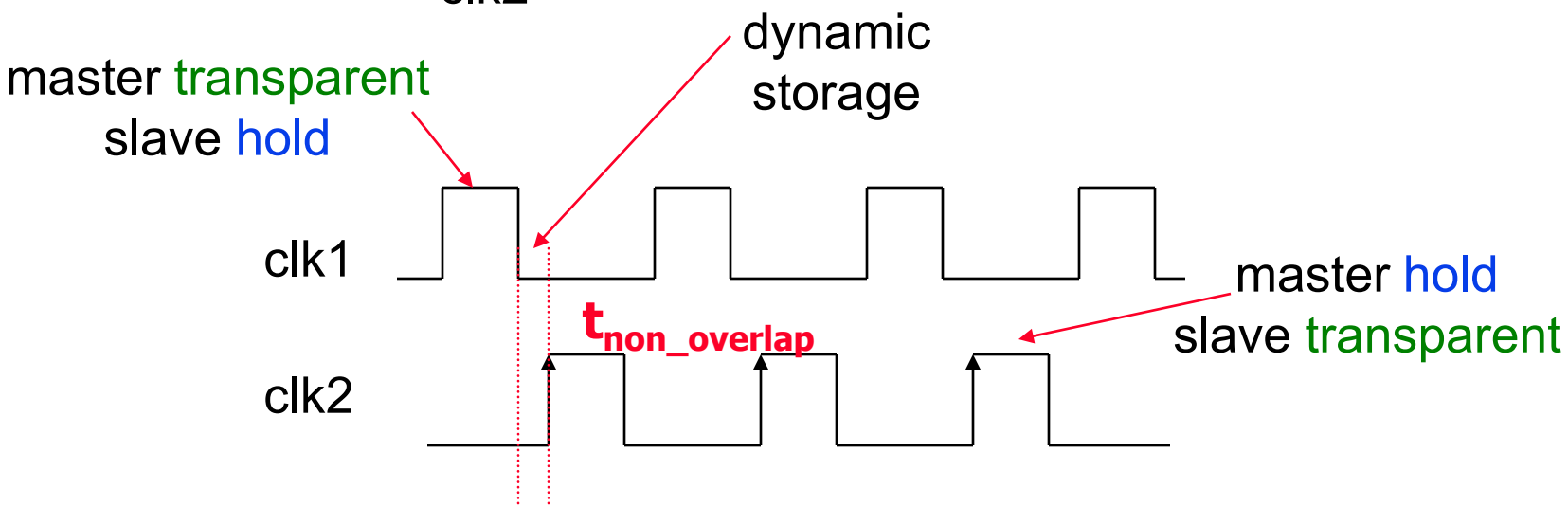
Race condition – direct path from D to Q during the short time when both clk and !clk are high (1-1 overlap)

Undefined state – both B and D are driving A when clk and !clk are both high

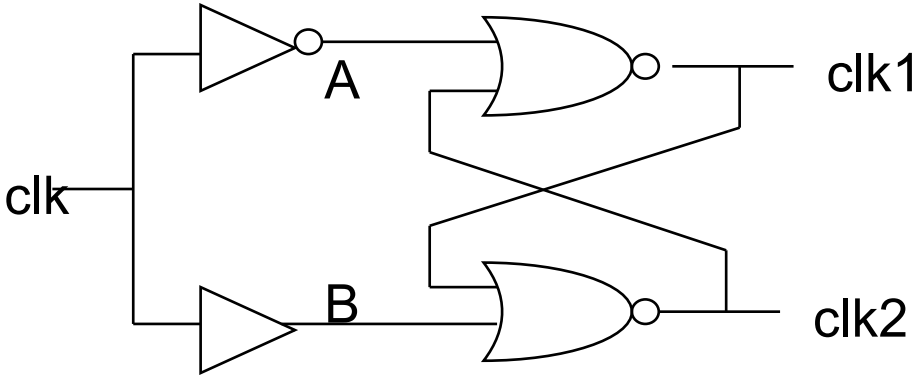
Dynamic storage – when clk and !clk are both low (0-0 overlap)

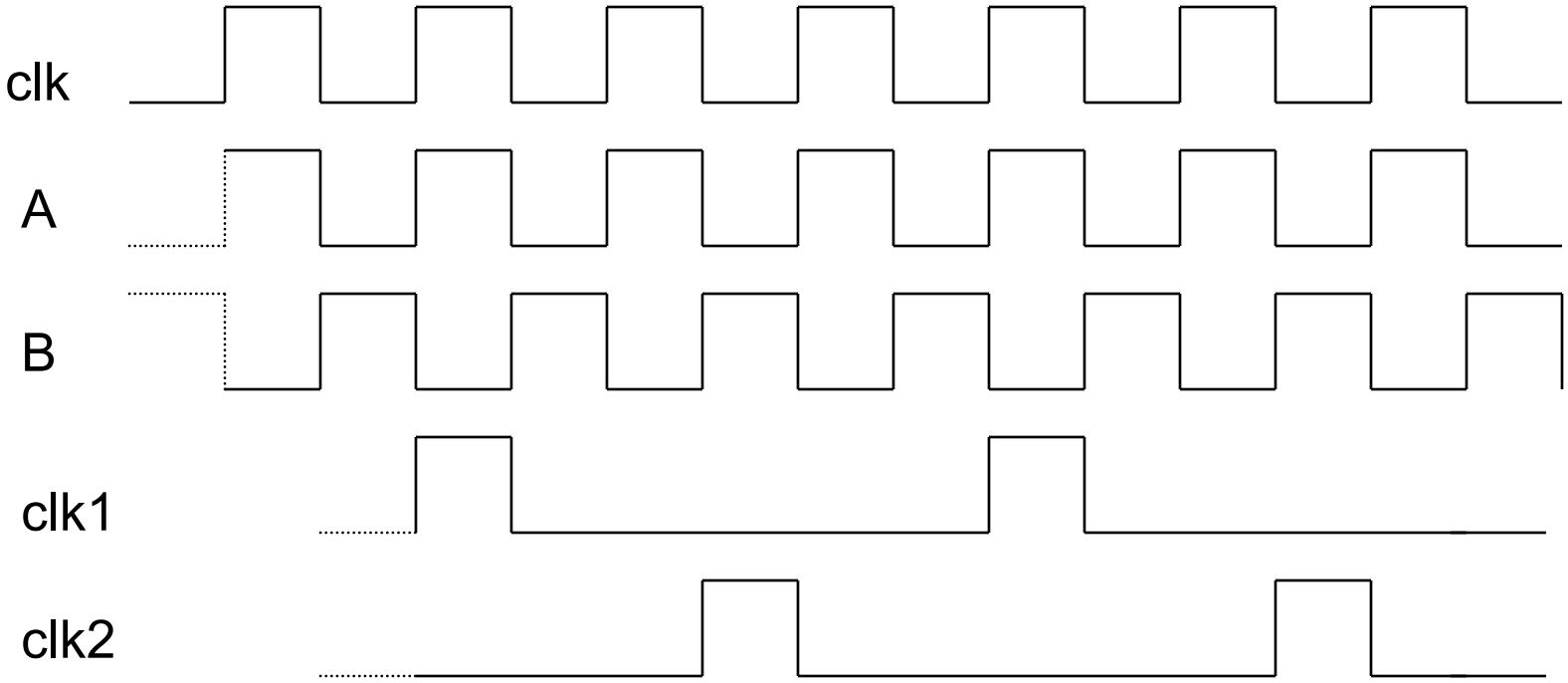
Pseudostatic Two-Phase ET FF



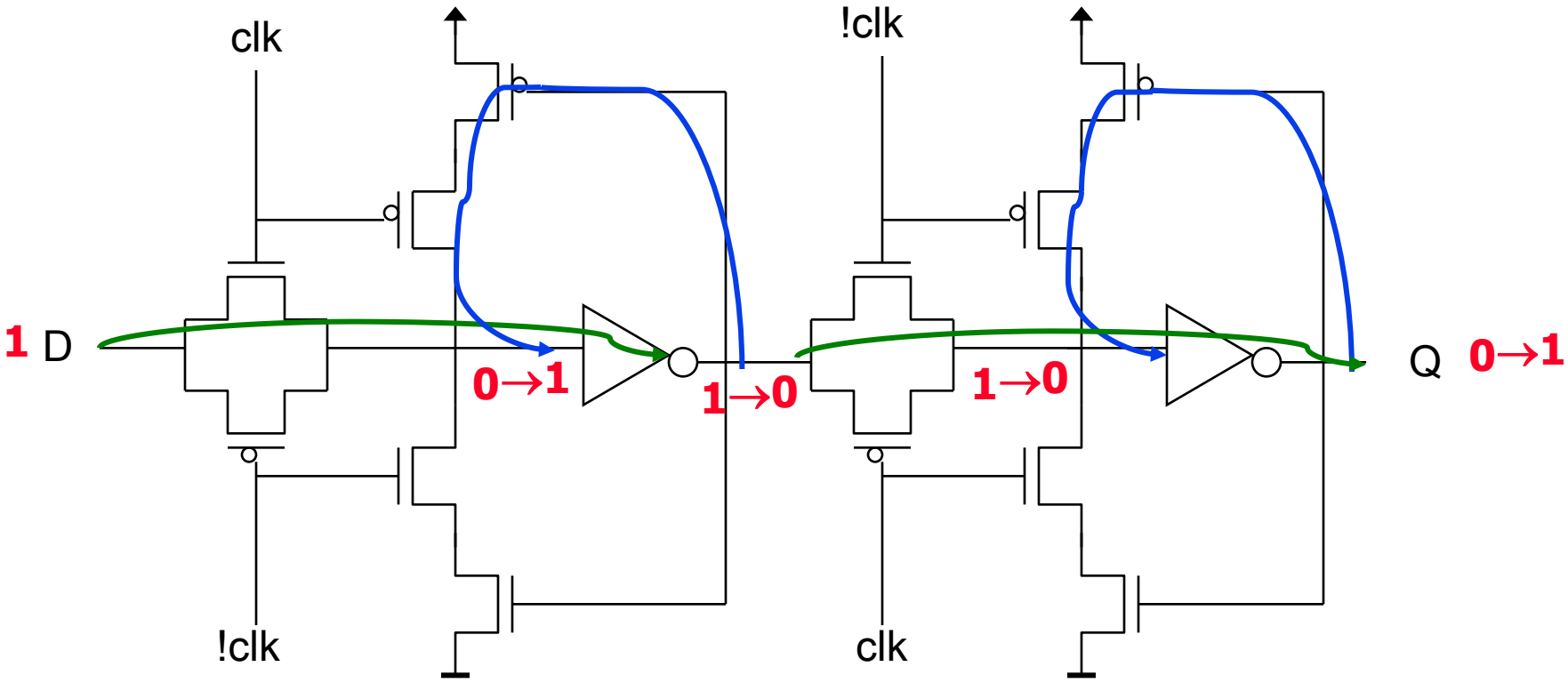


Two Phase Clock Generator



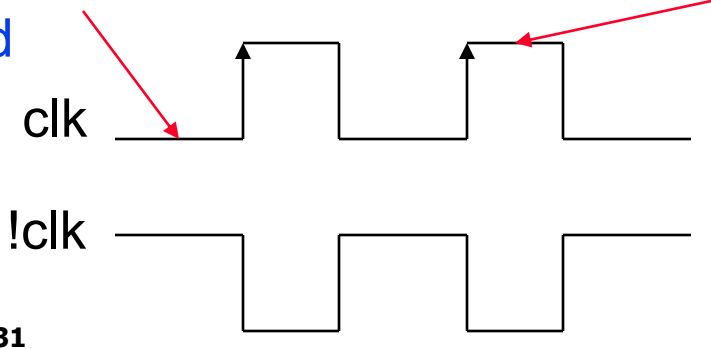


Power PC Flipflop

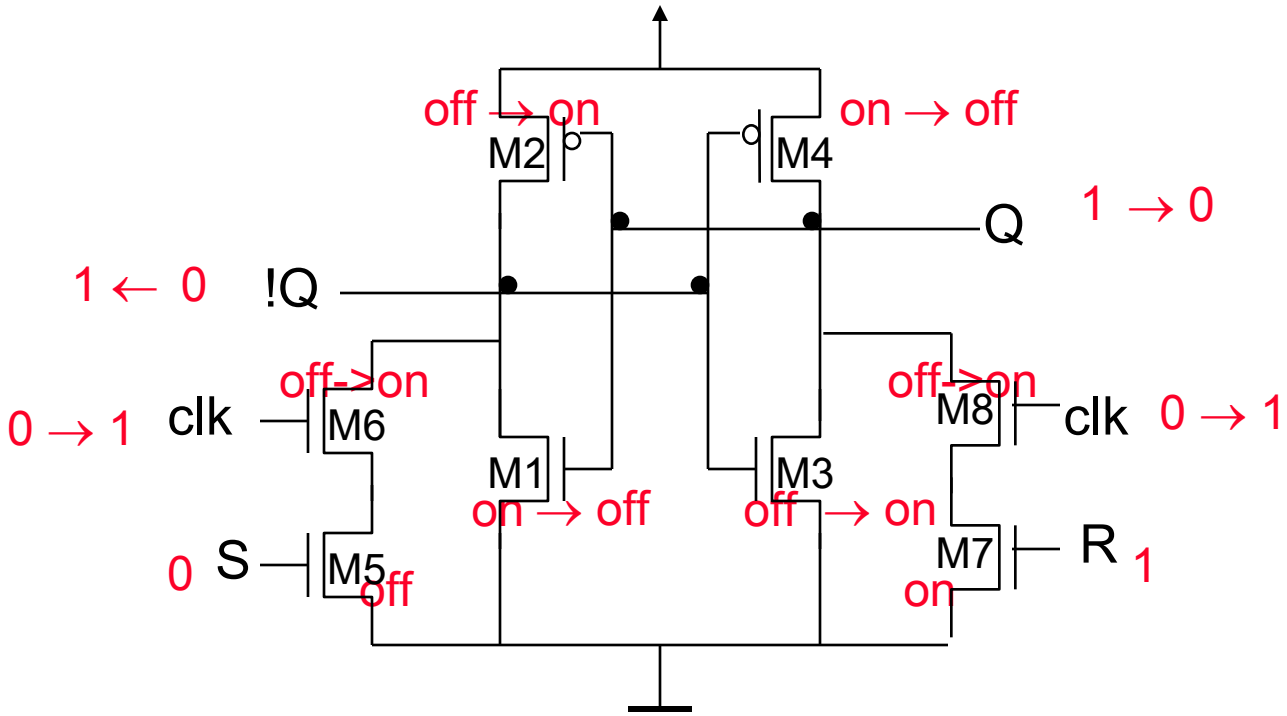


master transparent
slave hold

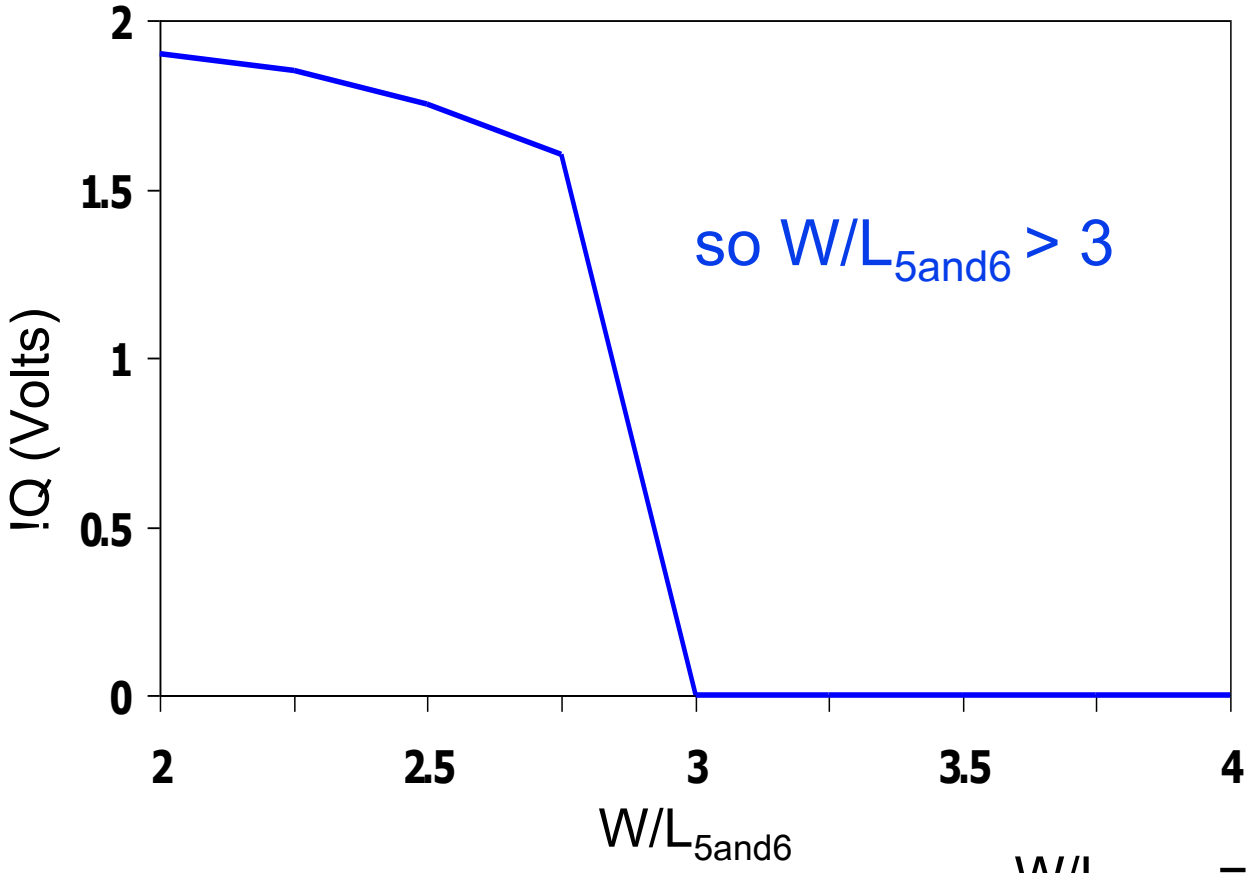
master hold
slave transparent



Ratioed CMOS Clocked SR Latch



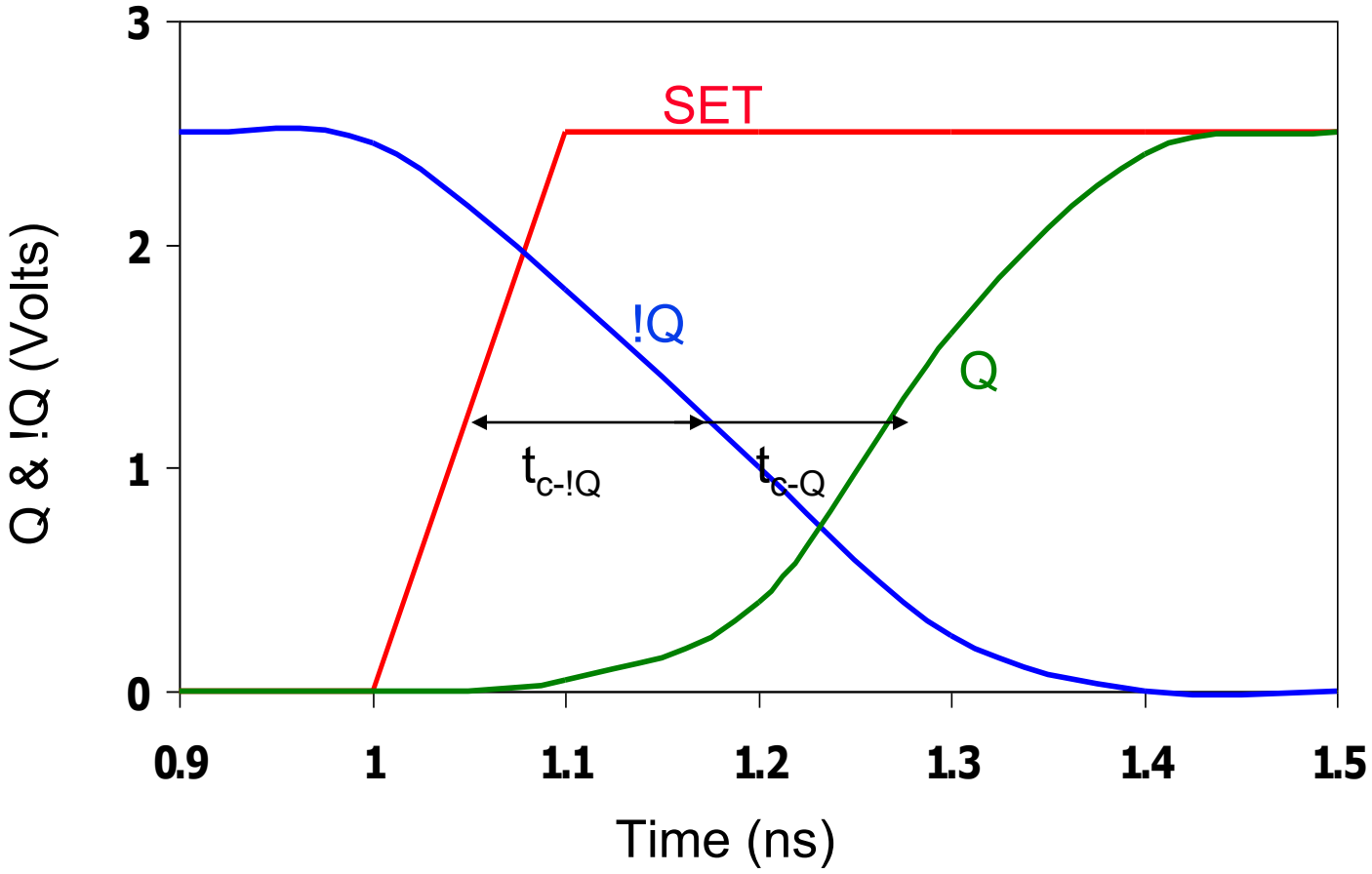
Sizing Issues



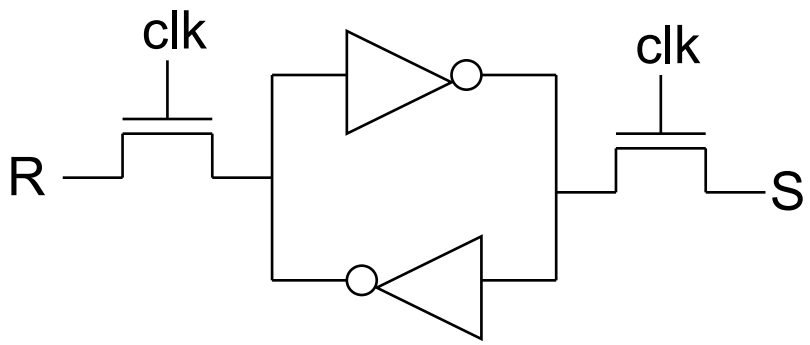
W/L_{2and4} = 1.5μm/0.25 μm

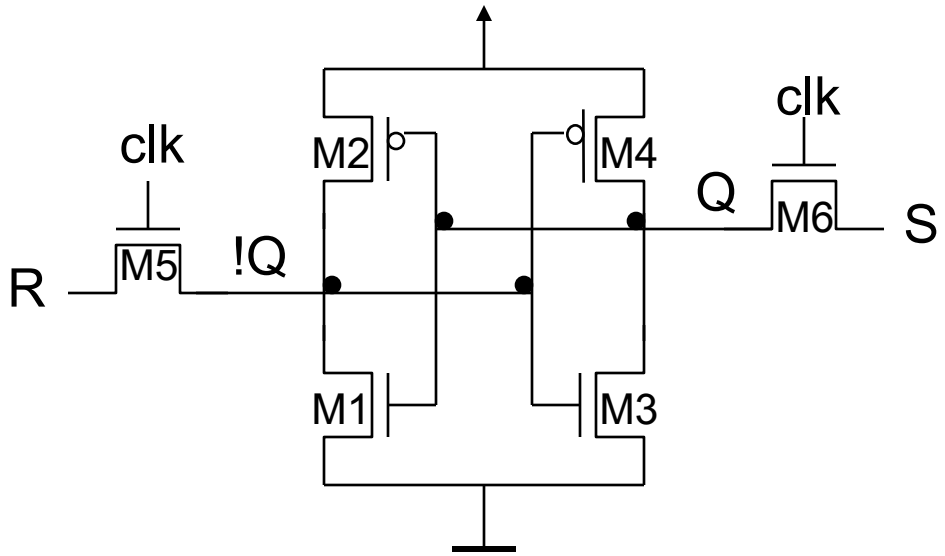
W/L_{1and3} = 0.5μm/0.25 μm

Transient Response



6 Transistor CMOS SR Latch





Next Lecture and Reminders

- Next lecture
  - Dynamic sequential circuits
    - Reading assignment – Rabaey, et al, 7.3, 7.7
- Reminders
  - Project prototypes due today
  - Project final reports due December 5th
  - HW4 due November 5th
  - HW5 out November 5th and due November 19th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in TBD