CSE477
VLSI Digital Circuits
Fall 2002

Lecture 02: Design Metrics

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Course Administration

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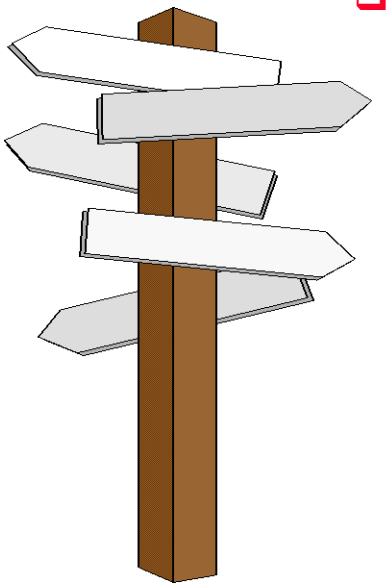
  Office Hrs: W & R 17:30 to 19:30 in 101 Pond
- Labs: Accounts on 101 Pond Lab machines
- URL: www.cse.psu.edu/~cg477
- Text: *Digital Integrated Circuits*, 2nd Edition
  Rabaey et. al., ©2002 (October)
- Handouts: Leftover handouts available outside my office door after class

Grading Information

- Grade determinates
  - Midterm Exam ~25%
    - Wednesday, October 16th , 20:15 to 22:15, 260 Willard
  - Final Exam ~25%
    - Monday, December 16th, 10:10 to noon, Location TBD
  - Homeworks/Lab Assignments (5) ~20%
    - Due at the beginning of class (or, if submitted electronically, by 17:00 on the due date). No late assignments will be accepted.
  - Design Project (teams of ~2) ~25%
  - In-class pop quizzes ~ 5%
- Please let me know about exam conflicts ASAP
- Grades will be posted on the course homepage
  - December 10th deadline for filing grade updates via email

Major Design Challenges

- Microscopic issues
  - ultra-high speeds
  - power dissipation and supply rail drop
  - growing importance of interconnect
  - noise, crosstalk
  - reliability, manufacturability
  - clock distribution



- Macroscopic issues
  - time-to-market
  - design complexity (millions of gates)
  - high levels of abstractions
  - design for test
  - reuse and IP, portability
  - systems on a chip (SoC)
  - tool interoperability

Year	Tech.	Complexity	Frequency	3 Yr. Design Staff Size	Staff Costs
1997	0.35	13 M Tr.	400 MHz	210	$90 M
1998	0.25	20 M Tr.	500 MHz	270	$120 M
1999	0.18	32 M Tr.	600 MHz	360	$160 M
2002	0.13	130 M Tr.	800 MHz	800	$360 M

Overview of Last Lecture

- Digital integrated circuits experience exponential growth in complexity (Moore's law) and performance
- Design in the deep submicron (DSM) era creates new challenges
  - Devices become somewhat different
  - Global clocking becomes more challenging
  - Interconnect effects play a more significant role
  - Power dissipation may be *the* limiting factor
- Our goal in this class will be to understand and design digital integrated circuits in the deep submicron era
- Today we look at some basic design metrics

Fundamental Design Metrics

- Functionality
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay)
  - Power consumption; energy
- Time-to-market

Cost of Integrated Circuits

- NRE (non-recurring engineering) costs
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products
- Recurring costs – proportional to product volume
  - silicon processing
    - also proportional to chip area
  - assembly (packaging)
  - test

$$\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}$$

NRE Cost is Increasing

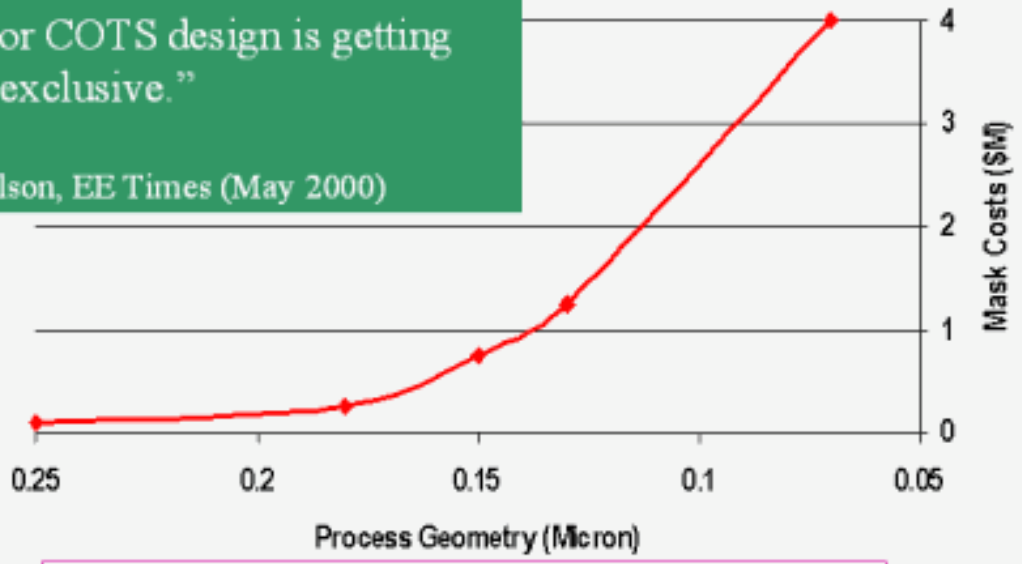
1996 1997 1998 1999 **2000 2001 2002 2003**

The Innovation Revolution

Exploding NRE / Mask Costs

"The club of people who can afford an extreme sub-micron ASIC or COTS design is getting pretty exclusive."

Ron Wilson, EE Times (May 2000)

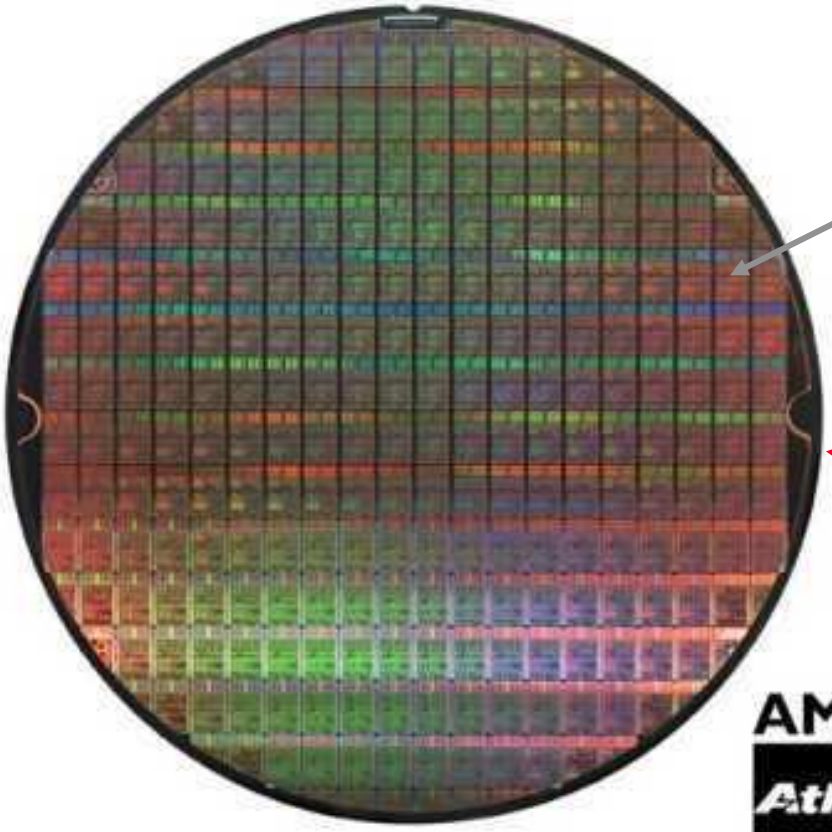


70nm ASICs will have $4M NRE

www.InnovationRevolution.com

ALTERA. Mentor Graphics XILINX

Silicon Wafer



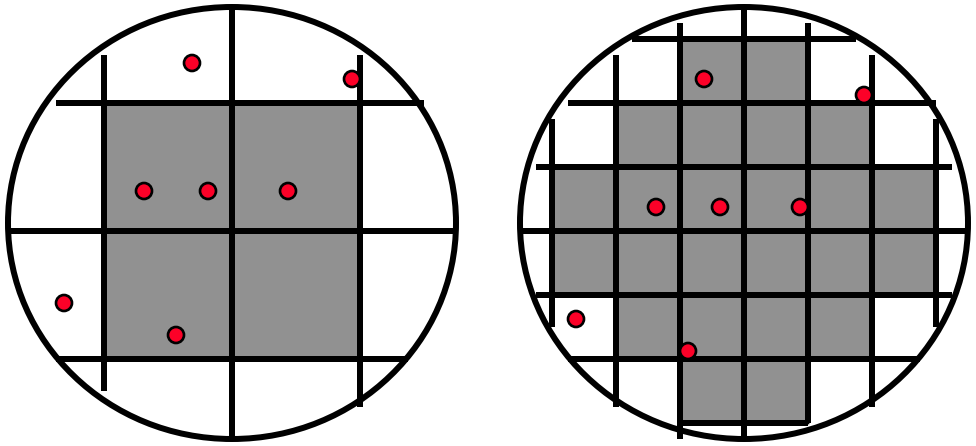
From http://www.amd.com

Recurring Costs

$$\text{variable cost} = \frac{\text{cost of die + cost of die test + cost of packaging}}{\text{final test yield}}$$

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}$$

$$\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



$$\text{die yield} = (1 + (\text{defects per unit area} \times \text{die area})/\alpha)^{-\alpha}$$

Yield Example

- Example
  - wafer size of 12 inches, die size of 2.5 cm^2, 1 defects/cm^2, α = 3 (measure of manufacturing process complexity)
  - 252 dies/wafer (remember, wafers round & dies square)
  - die yield of 16%
  - 252 x 16% = only 40 dies/wafer die yield !

- Die cost is strong function of die area
  - proportional to the third or fourth power of the die area

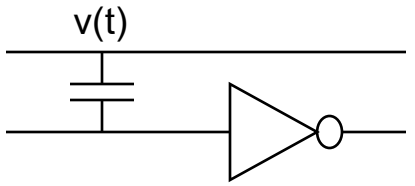
Examples of Cost Metrics (1994)

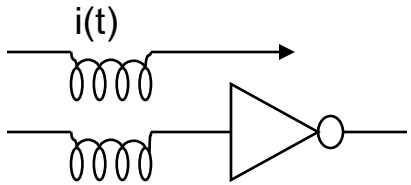
Chip	Metal layers	Line width	Wafer cost	Defects /cm^2	Area (mm^2)	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486DX2	3	0.80	$1200	1.0	81	181	54%	$12
PowerPC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super SPARC	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Reliability

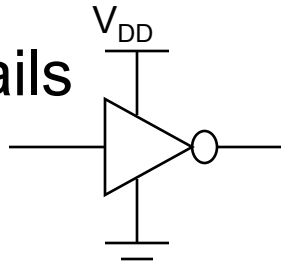
Noise in Digital Integrated Circuits

- Noise – unwanted variations of voltages and currents at the logic nodes
- from two wires placed side by side
  - capacitive coupling
    - voltage change on one wire can influence signal on the neighboring wire
    - cross talk
  - inductive coupling
    - current change on one wire can influence signal on the neighboring wire





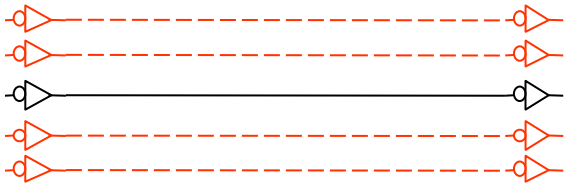
- from noise on the power and ground supply rails
  - can influence signal levels in the gate



Example of Capacitive Coupling

- Signal wire glitches as large as 80% of the supply voltage will be common due to crosstalk between neighboring wires as feature sizes continue to scale

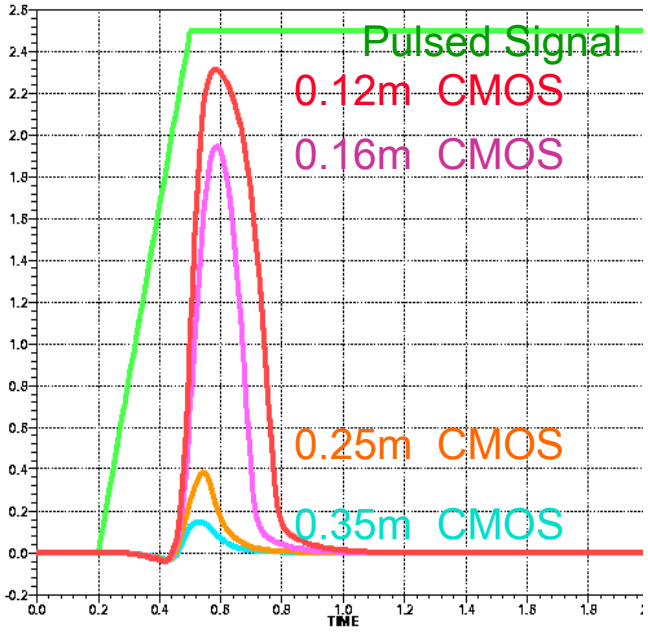
Crosstalk vs. Technology



Black line quiet

Red lines pulsed

Glitches strength vs technology



From Dunlop, Lucent, 2000

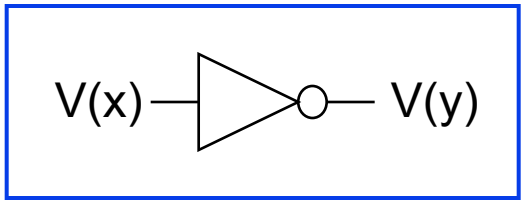
Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables

$$x \in \{0,1\}$$

- A logical variable is associated with a *nominal voltage level* for each logic state

$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$



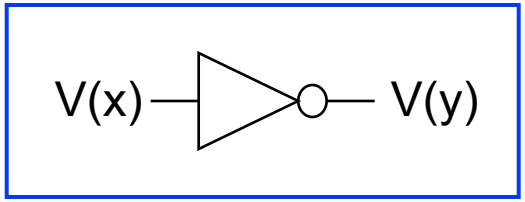
$V_{OH} = !\,(V_{OL})$

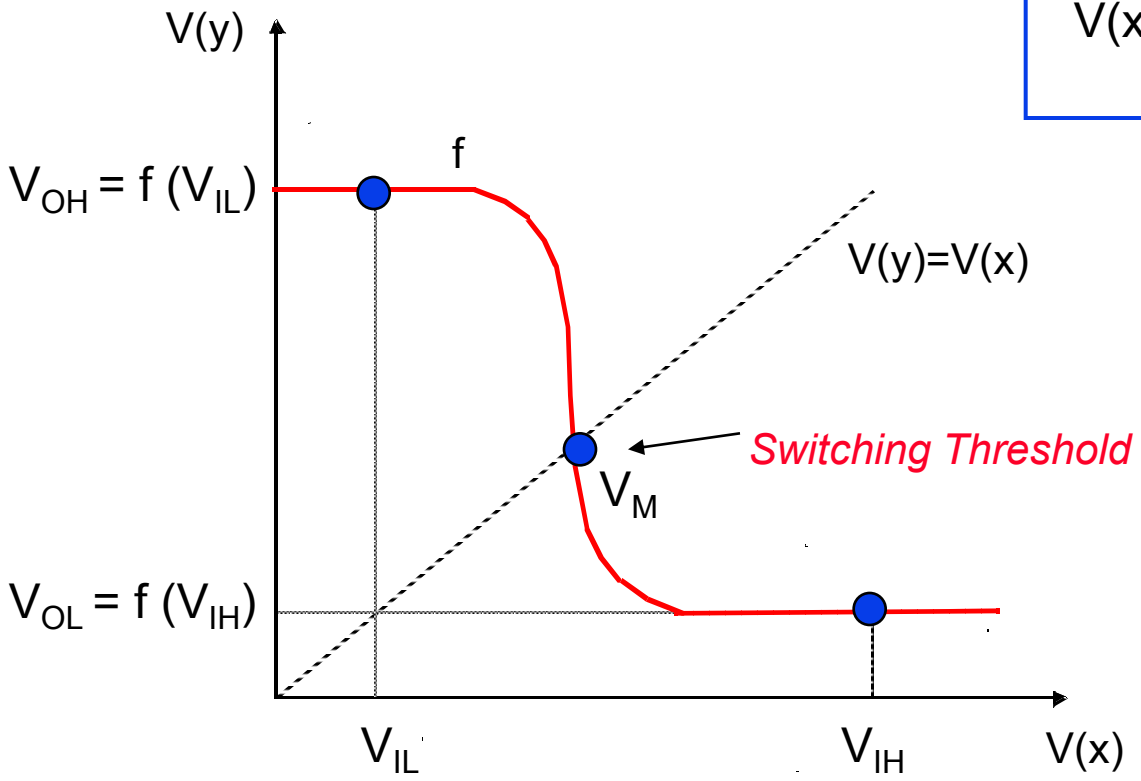
$V_{OL} = !\,(V_{OH})$

- Difference between V_{OH} and V_{OL} is the logic or *signal swing* V_{sw}

DC Operation
Voltage Transfer Characteristics (VTC)

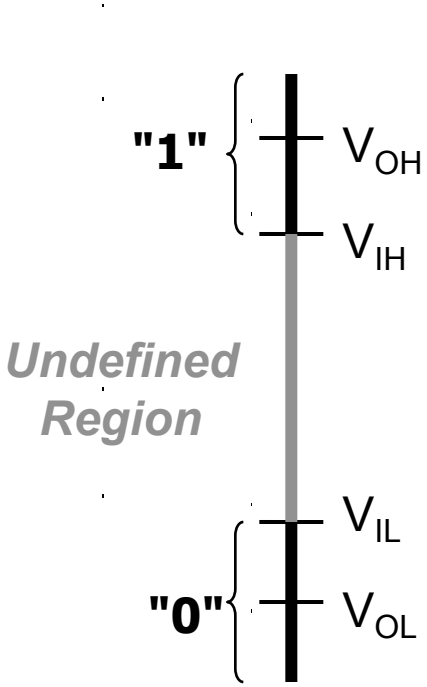
- Plot of output voltage as a function of the input voltage

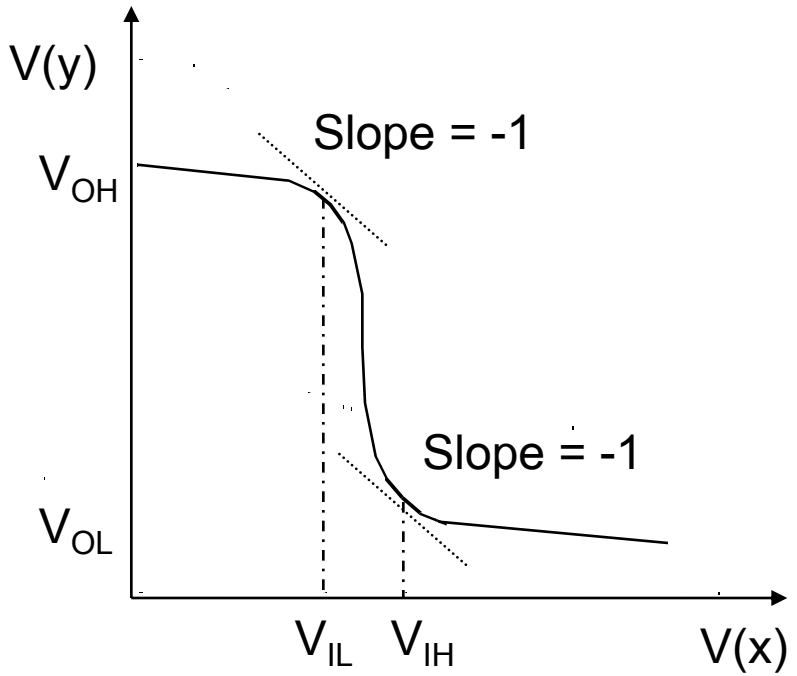




Mapping Logic Levels to the Voltage Domain

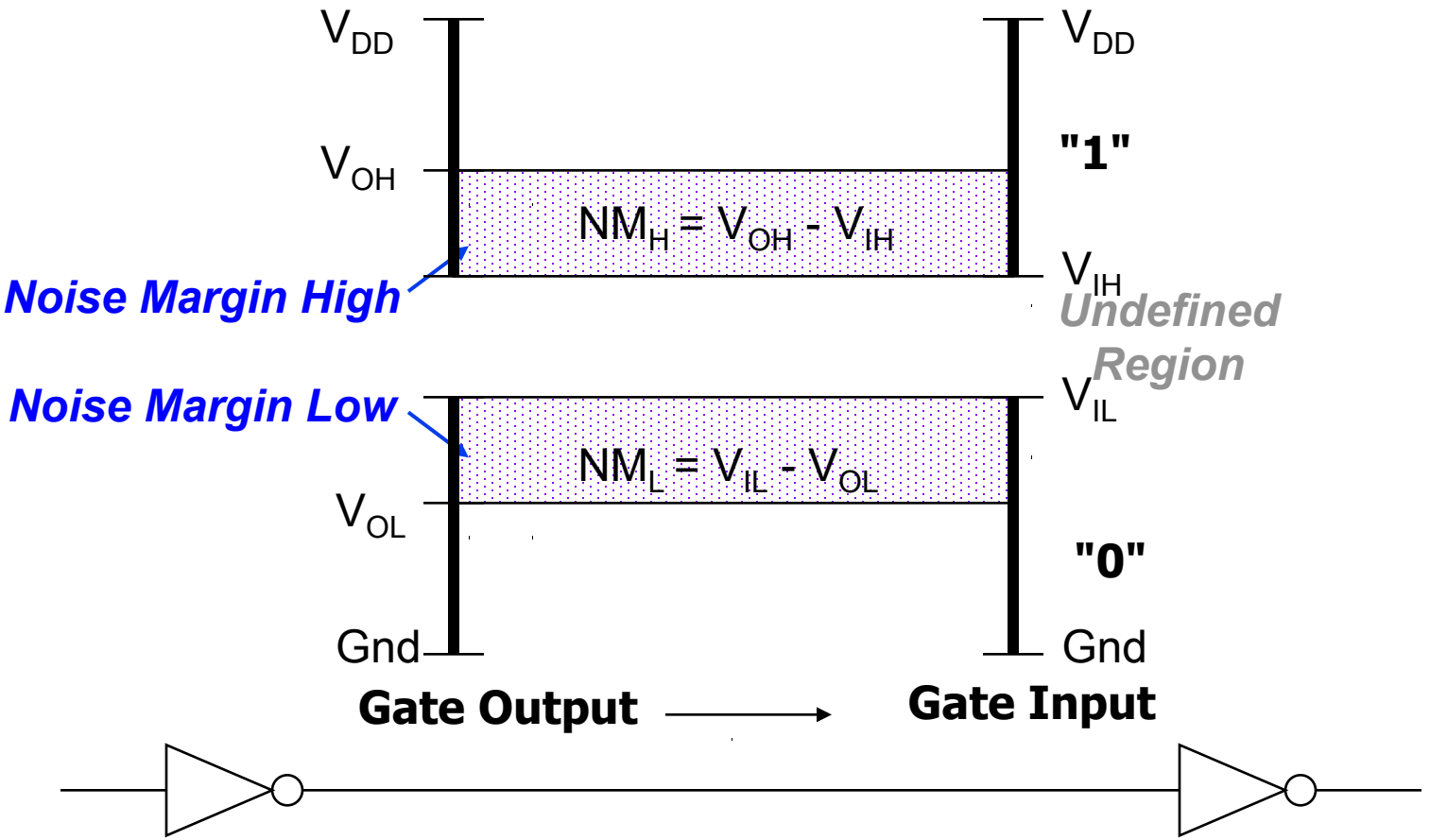
- The regions of acceptable high and low voltages are delimited by V_{IH} and V_{IL} that represent the points on the VTC curve where the gain = -1





Noise Margins

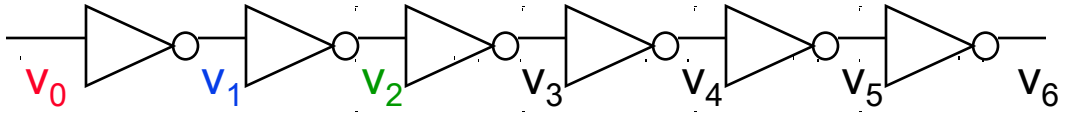
- For robust circuits, want the “0” and “1” intervals to be a s large as possible

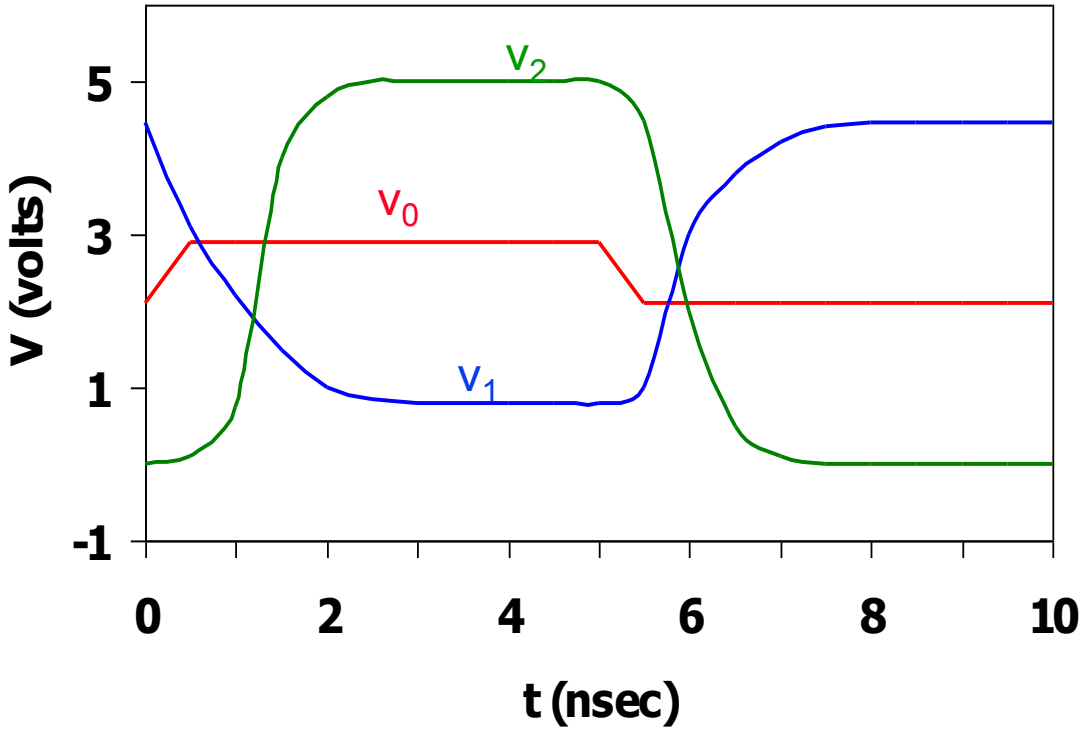


- Large noise margins are desirable, but not sufficient …

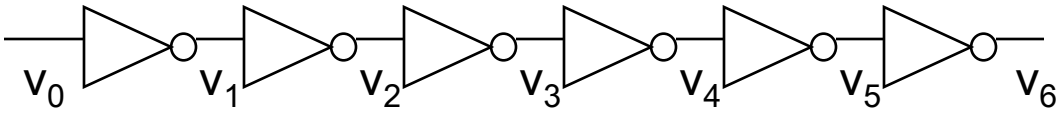
The Regenerative Property

- A gate with regenerative property ensure that a disturbed signal converges back to a nominal voltage level

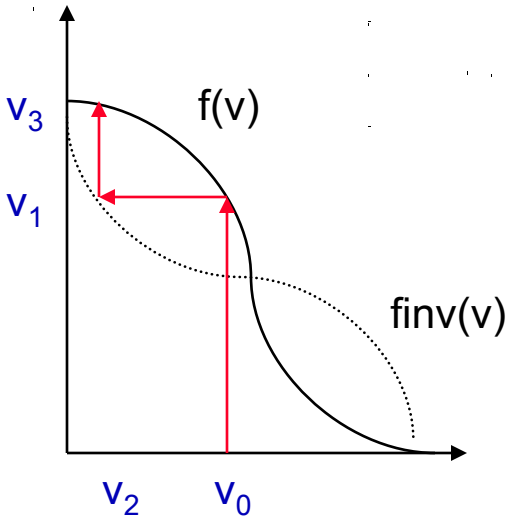




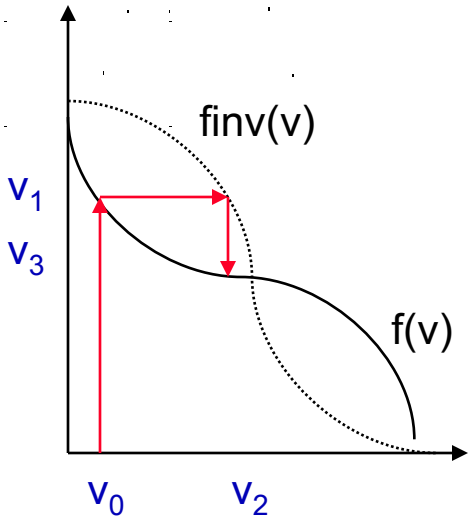
Conditions for Regeneration



$v_1 = f(v_0) \Rightarrow v_1 = finv(v_2)$



Regenerative Gate



Nonregenerative Gate

- To be regenerative, the VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.

Noise Immunity

- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, cross talk, interference, offset
- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between V_{OH} and V_{OL}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

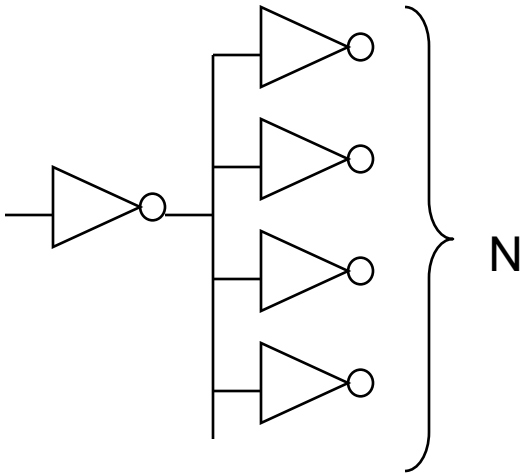
Directivity

- A gate must be *undirectional*: changes in an output level should not appear at any unchanging input of the same circuit
  - In real circuits *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)

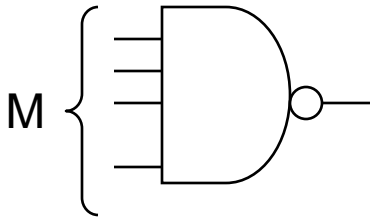
- Key metrics: *output impedance* of the driver and *input impedance* of the receiver
  - ideally, the output impedance of the driver should be zero
  - input impedance of the receiver should be infinity

Fan-In and Fan-Out

- Fan-out – number of load gates connected to the output of the driving gate
  - gates with large fan-out are slower

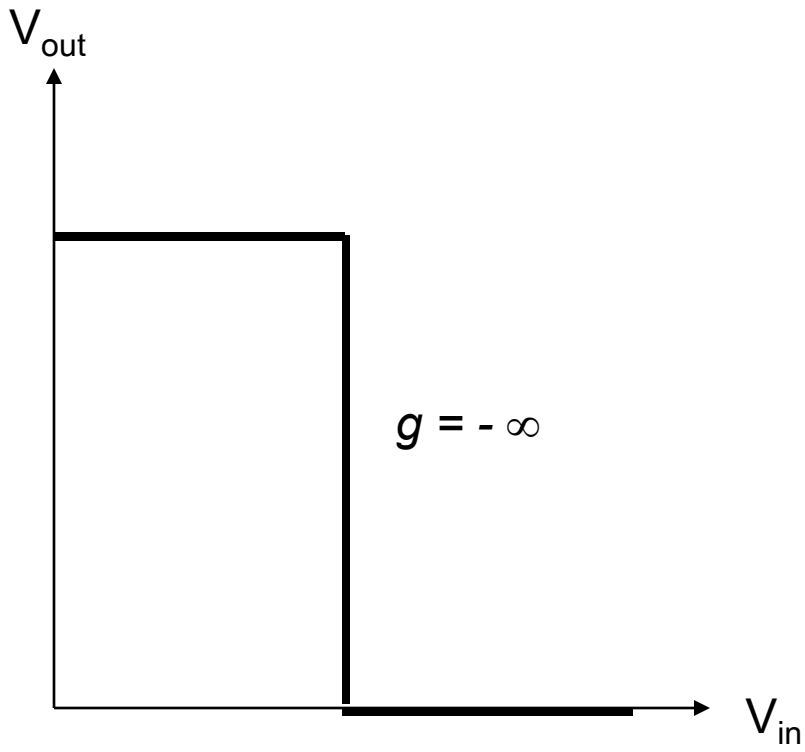


- Fan-in – the number of inputs to the gate
  - gates with large fan-in are bigger and slower



The Ideal Inverter

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.



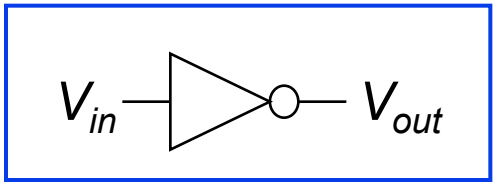
$R_i = \infty$

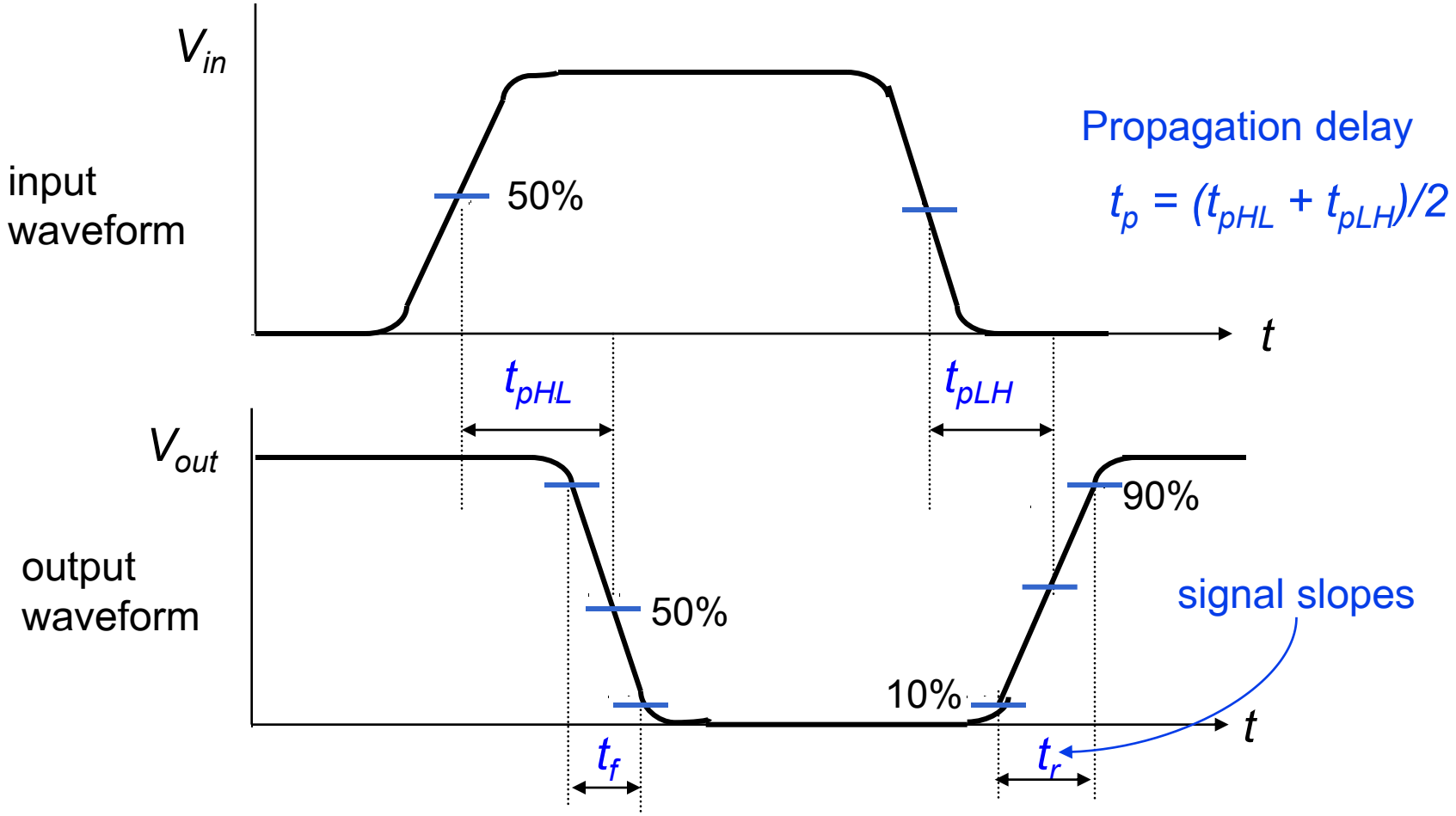
$R_o = 0$

Fanout = ∞

$NM_H = NM_L = VDD/2$

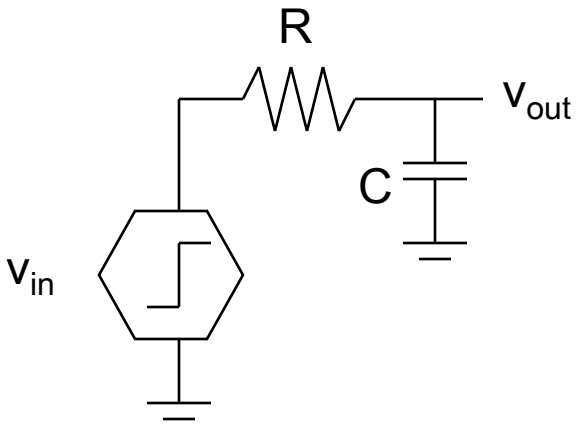
Delay Definitions





Modeling Propagation Delay

- Model circuit as first-order RC network



$$v_{out}(t) = (1 - e^{-t/\tau})V$$

where $\tau = RC$

Time to reach 50% point is
$t = \ln(2)\,\tau = 0.69\,\tau$

Time to reach 90% point is
$t = \ln(9)\,\tau = 2.2\,\tau$

- Matches the delay of an inverter gate

Power and Energy Dissipation

- Power consumption: how much energy is consumed per operation and how much heat the circuit dissipates
  - supply line sizing (determined by peak power)

$$P_{peak} = V_{dd} i_{peak}$$

  - battery lifetime (determined by average power dissipation)

$$p(t) = v(t)i(t) = V_{dd} i(t) \qquad P_{avg} = 1/T \int p(t)\,dt = V_{dd}/T \int i_{dd}(t)\,dt$$

  - packaging and cooling requirements

- Two important components: static and dynamic

$$E\ (\text{joules}) = C_L V_{dd}^2 P_{0\to1} + t_{sc} V_{dd} I_{peak} P_{0\to1} + V_{dd} I_{leakage}$$

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P\ (\text{watts}) = C_L V_{dd}^2 f_{0\to1} + t_{sc} V_{dd} I_{peak} f_{0\to1} + V_{dd} I_{leakage}$$

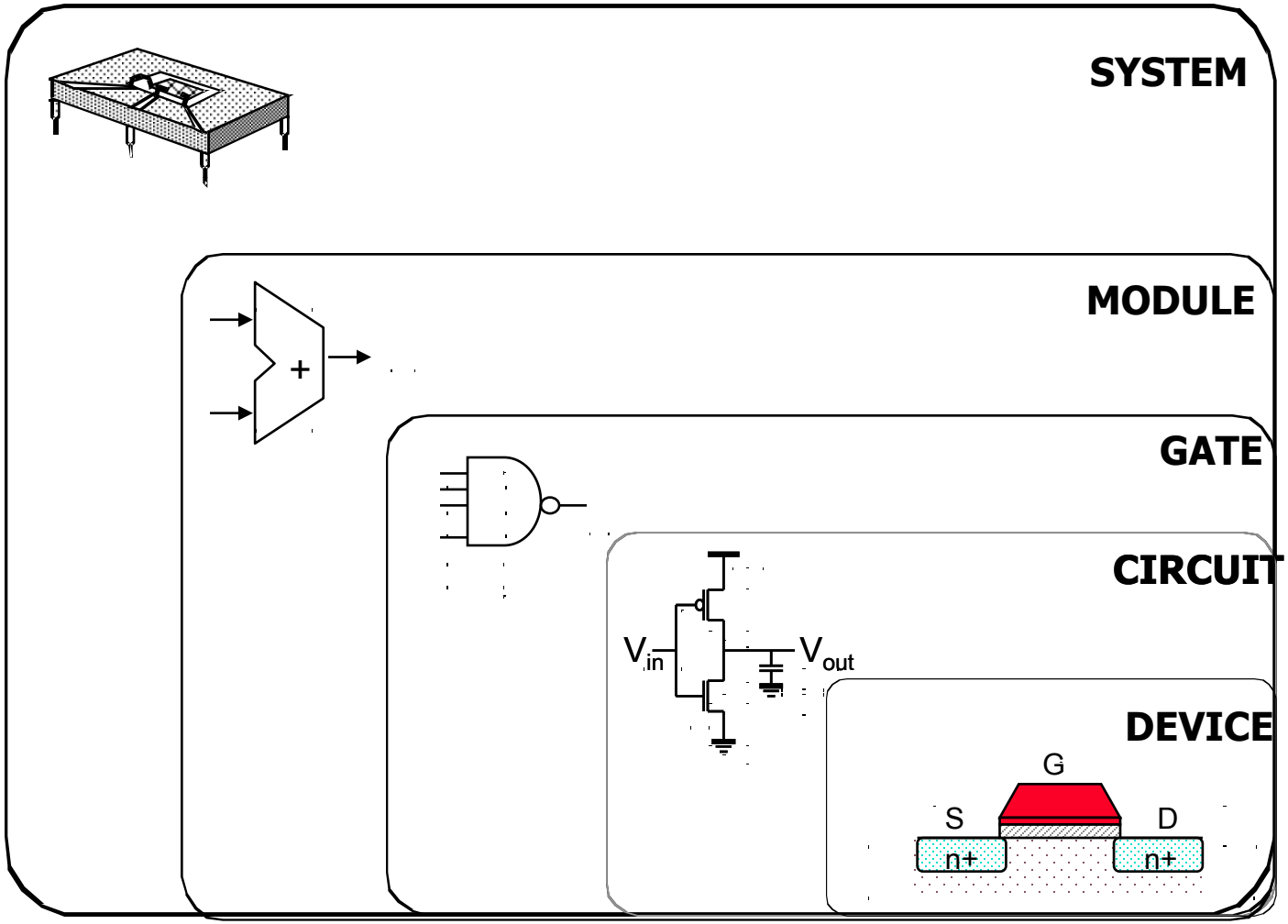
Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate
- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
  - Power-delay product (PDP) – energy consumed by the gate per switching event
- An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is
  - Energy-delay product (EDP) = power-delay ^{2}

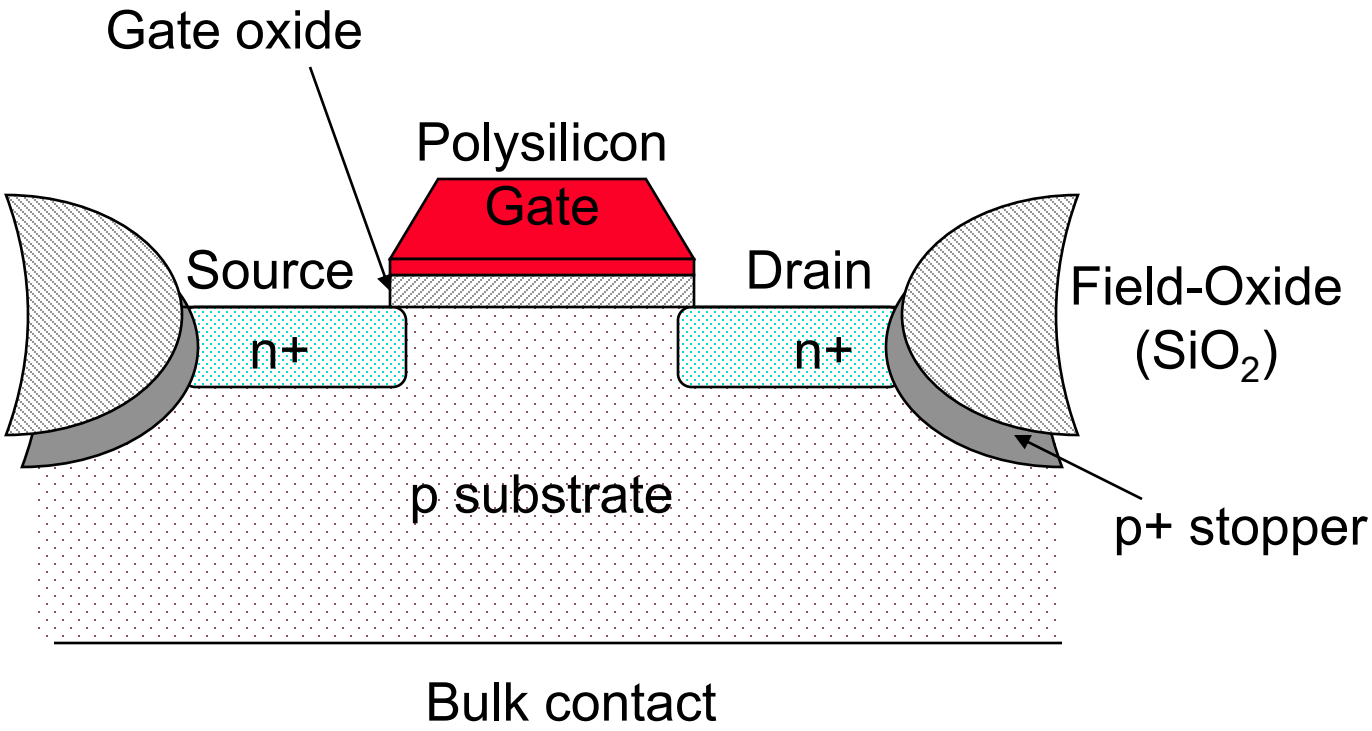
Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this course
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation

Design Abstraction Levels

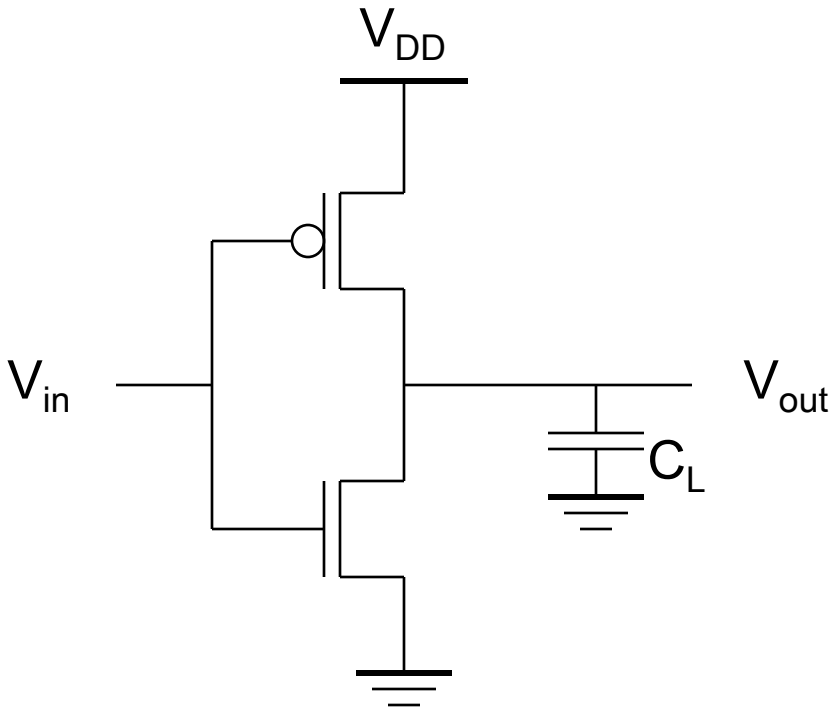


Device: The MOS Transistor



CROSS-SECTION of NMOS Transistor

Circuit: The CMOS Inverter



Next Lecture and Reminders

- Next lecture
  - MOS transistor
    - Reading assignment – Rabaey et al, 3.1-3.3.2

- Reminders
  - Hands on max tutorial *tonight*
    - Tonight in 101 Pond Lab
  - HW1 available on the web by 5:00pm
  - Project Description available on the web by 5:00pm tomorrow