CSE477
VLSI Digital Circuits
Fall 2002

Lecture 22: Shifters, Decoders, Muxes

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: Basic Building Blocks

❑ Datapath

    ❑ Execution units

        - Adder, multiplier, divider, shifter, etc.

    ❑ Register file and pipeline registers

    ❑ Multiplexers, decoders

❑ Control

    ❑ Finite state machines (PLA, ROM, random logic)
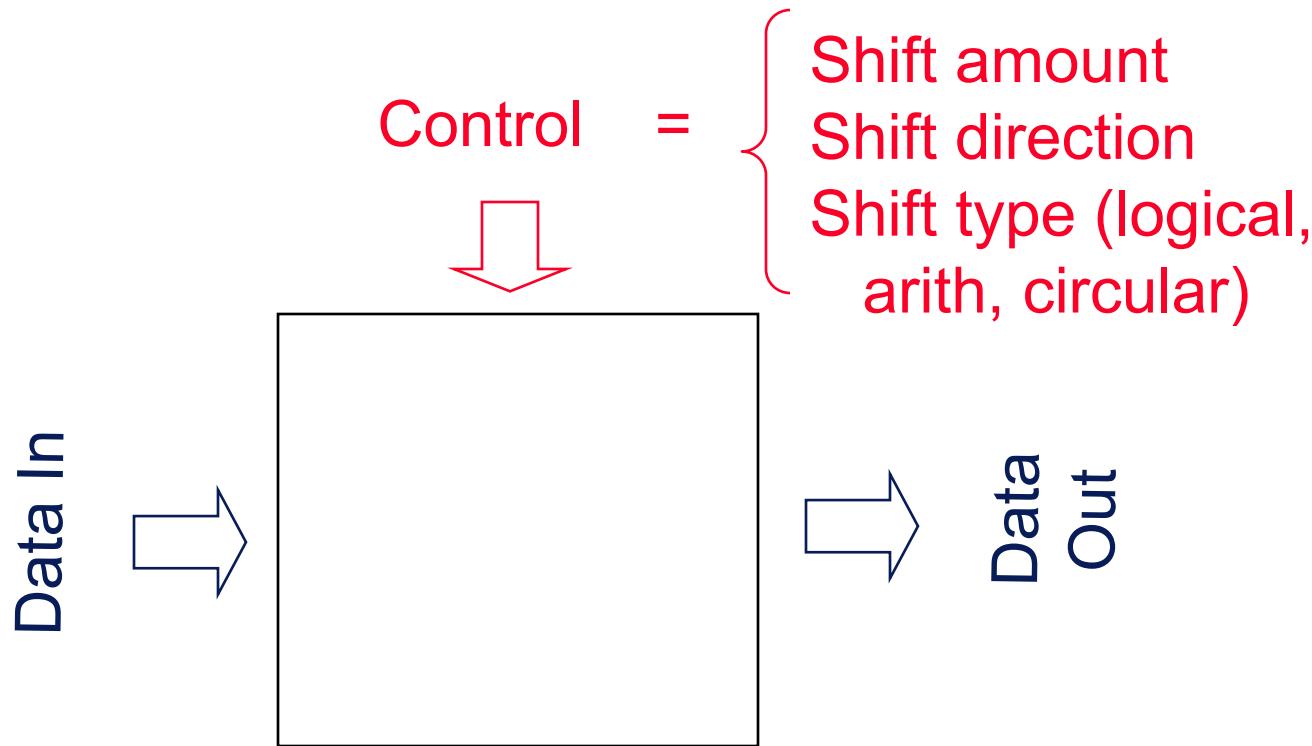
❑ Interconnect

    ❑ Switches, arbiters, buses

❑ Memory

    ❑ Caches (SRAMs), TLBs, DRAMs, buffers
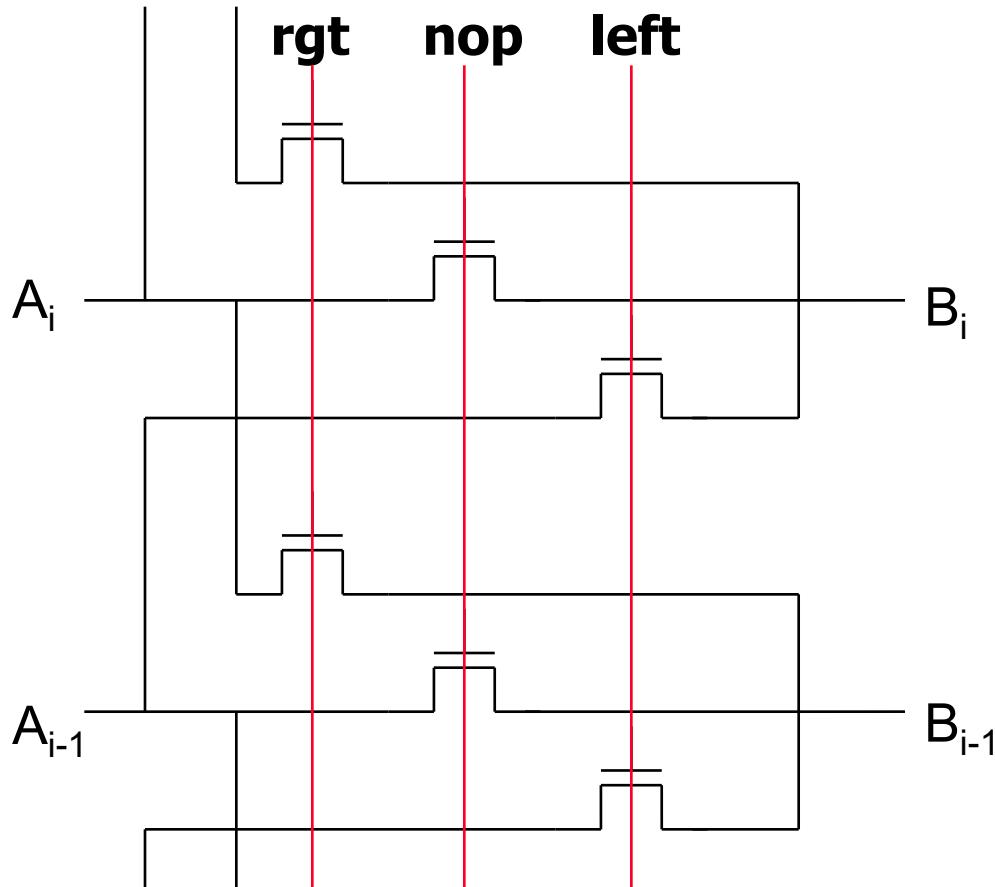
# Parallel Programmable Shifters

Control = { Shift amount
Shift direction
Shift type (logical, arith, circular) }

Data In →

Data Out →

Shifters used in multipliers, floating point units
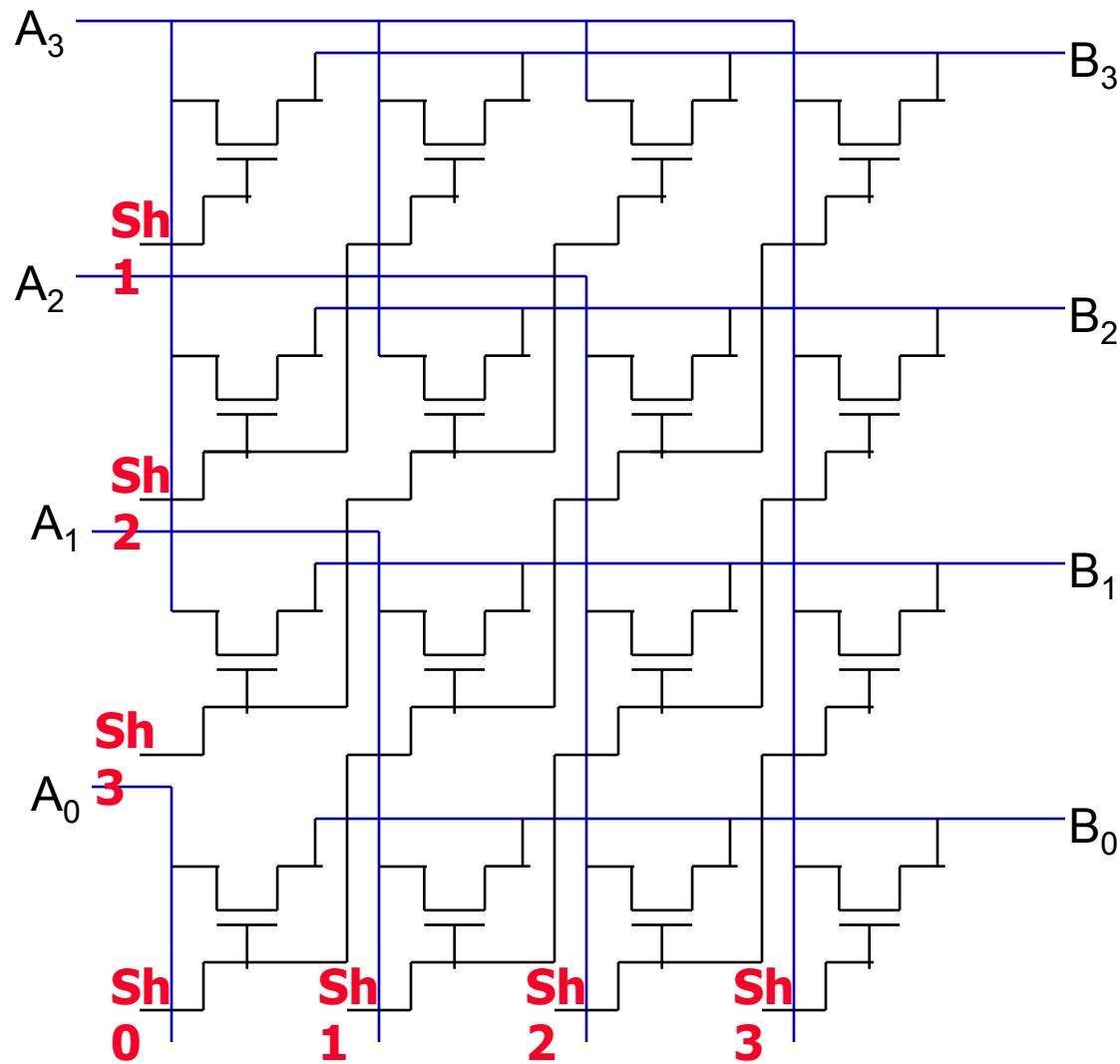
Consume lots of area if done in random logic gates

A Programmable Binary Shifter

A_i	A_{i-1}	rgt	nop	left	B_i	B_{i-1}
A_1	A_0	0	1	0	A_1	A_0
A_1	A_0	1	0	0	0	A_1
A_1	A_0	0	0	1	A_0	0

4-bit Barrel Shifter

Example: Sh0 = 1

$B_3B_2B_1B_0 = A_3A_2A_1A_0$

Sh1 = 1

$B_3B_2B_1B_0 = A_3A_3A_2A_1$

Sh2 = 1
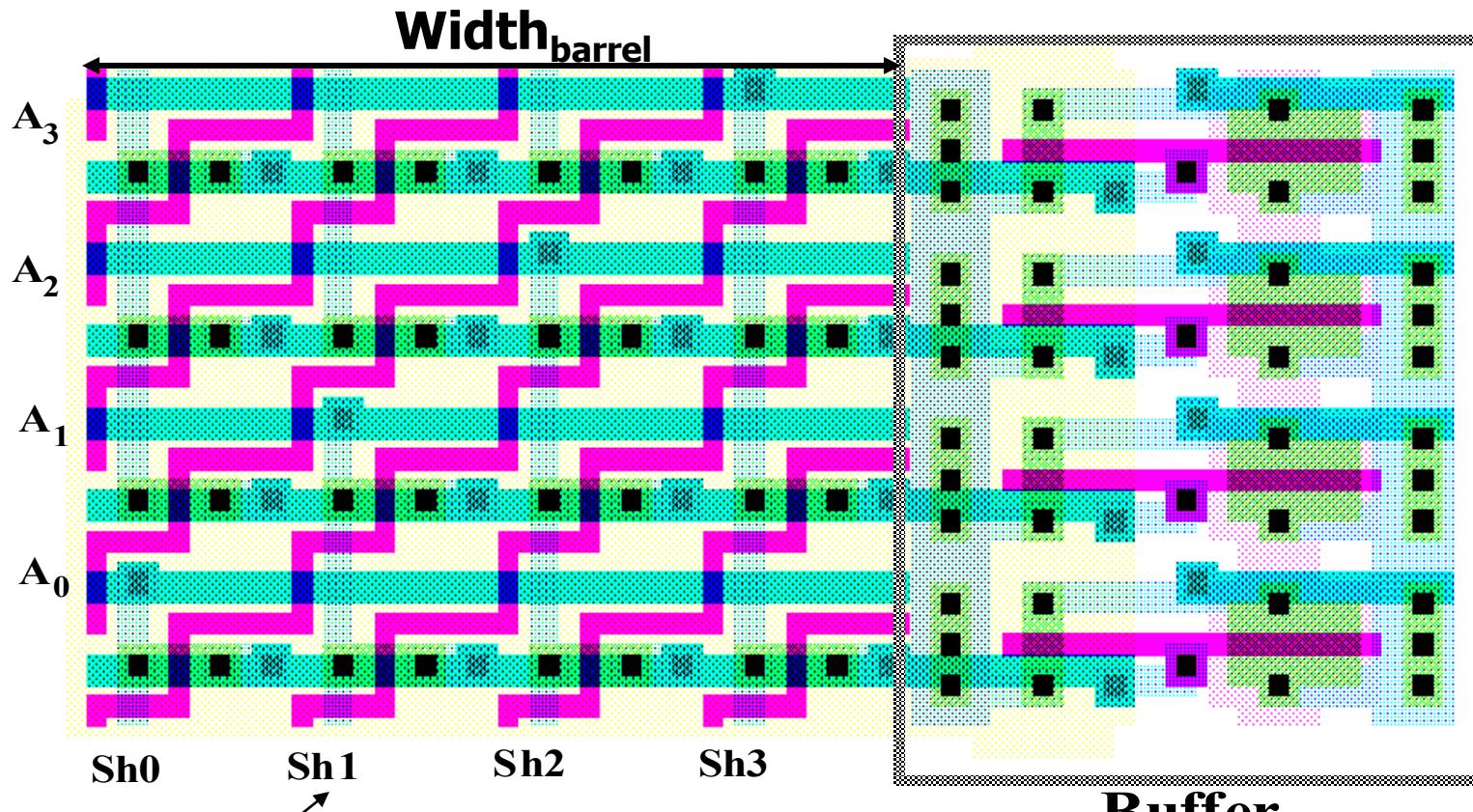
$B_3B_2B_1B_0 = A_3A_3A_3A_2$

Sh3 = 1

$B_3B_2B_1B_0 = A_3A_3A_3A_3$

Area dominated by wiring

4-bit Barrel Shifter Layout

A_3

A_2

A_1

A_0

Width$_{barrel}$

Sh0   Sh1   Sh2   Sh3

Buffer
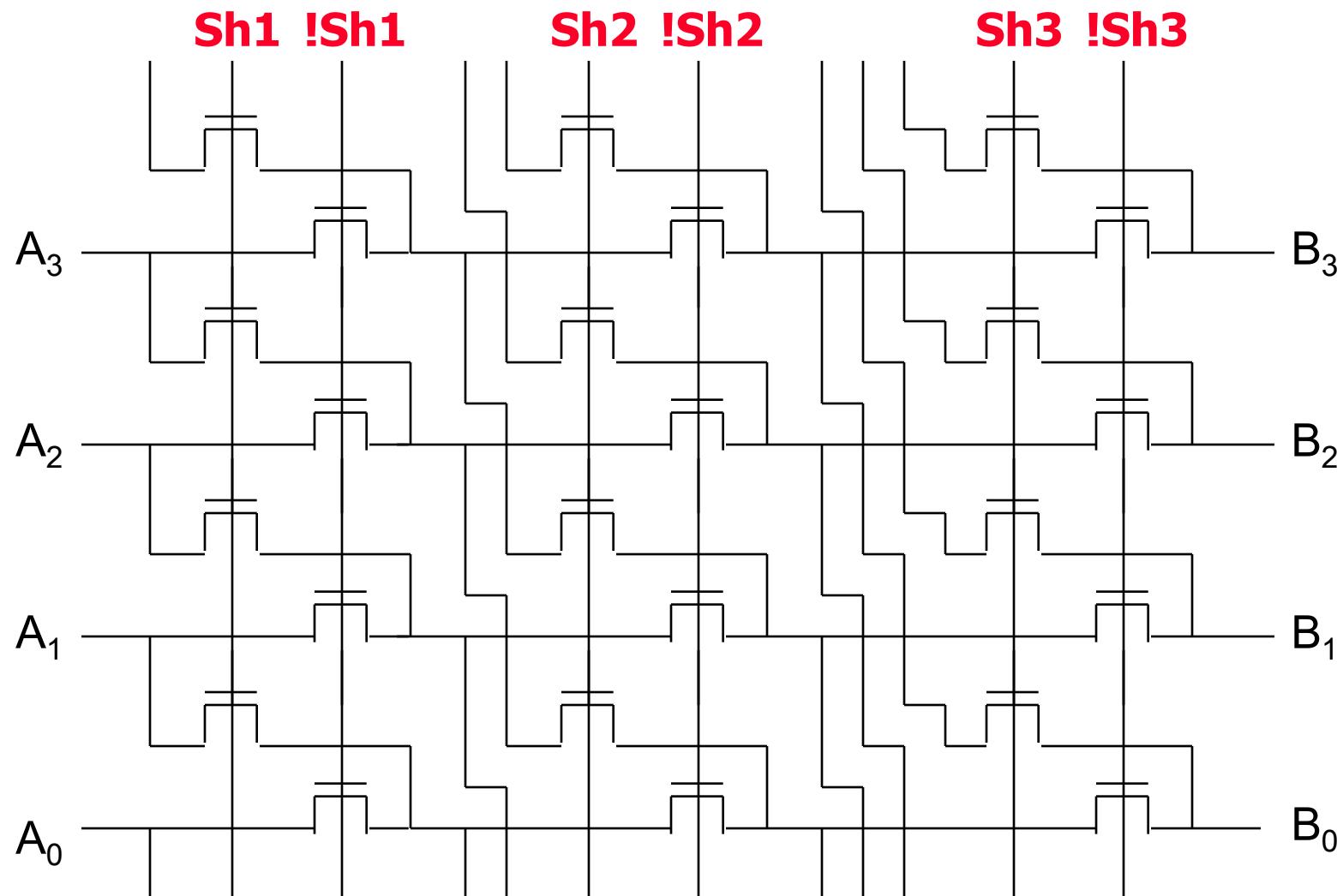
Only one Sh#
active at a time$_l$
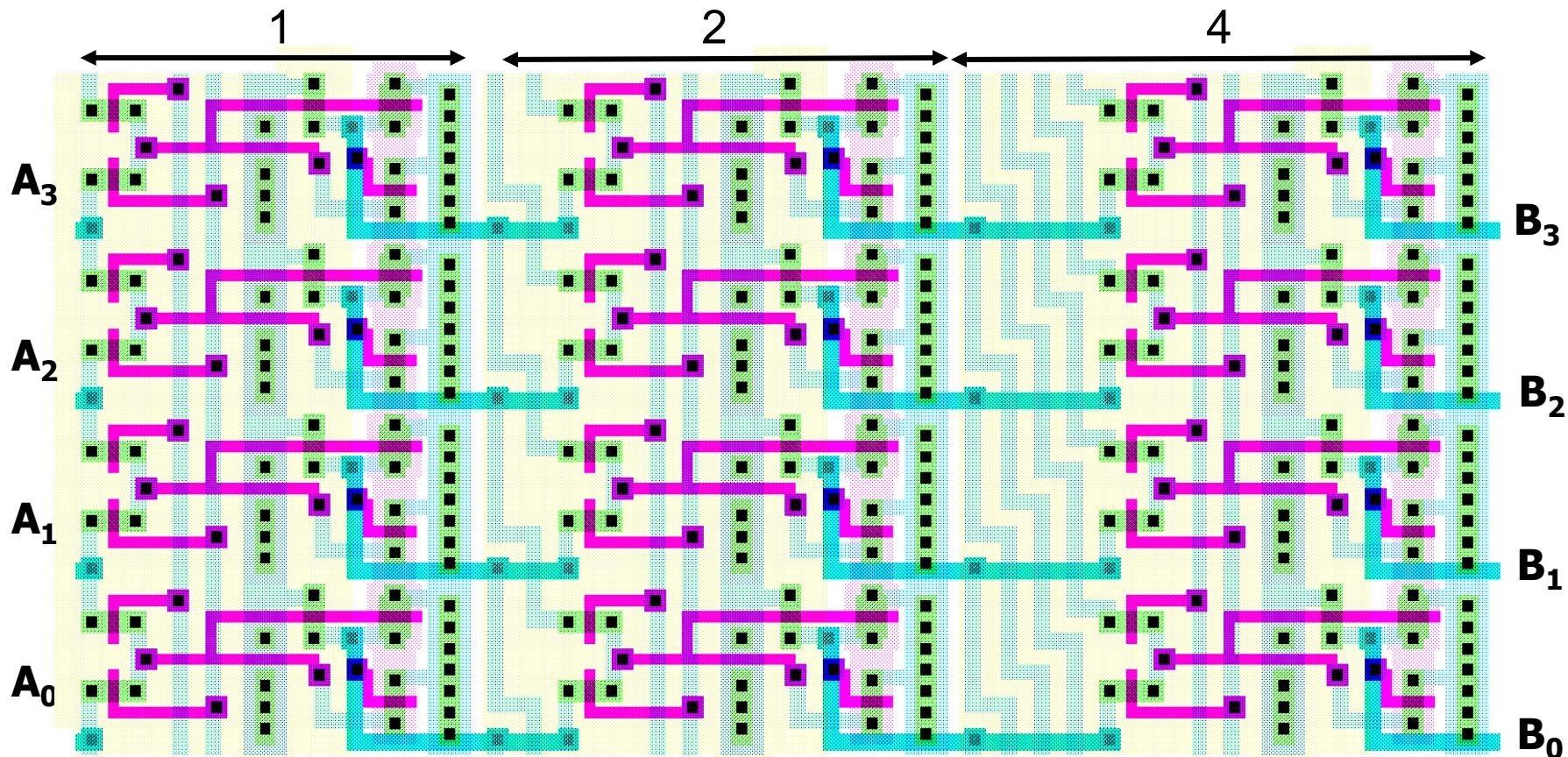
$$\text{Width}_{barrel} \sim 2\ p_m\ N$$
$$N = \text{max shift distance, } p_m = \text{metal pitch}$$
$$\text{Delay} \sim 1 \text{ fet} + N \text{ diff caps}$$

8-bit Logarithmic Shifter

Sh1 !Sh1   **Sh2 !Sh2**   **Sh3 !Sh3**

A_3 B_3

A_2 B_2

A_1 B_1

A_0 B_0

8-bit Logarithmic Shifter Layout Slice

$$\text{Width}_{log} \sim p_m(2K+(1+2+\ldots+2^{K-1})) = p_m(2^K+2K-1)$$

$$K = \log_2 N$$
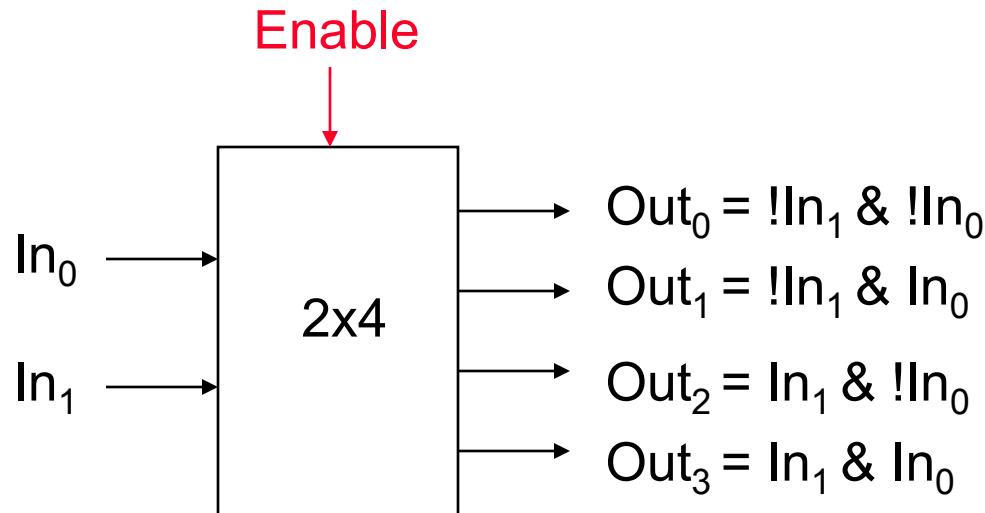
Delay ~ K fets + 2 diff caps

Shifter Implementation Comparisons

N	K	Barrel		Logarithmic	
		Width	Speed	Width	Speed
		$2 N p_m$	$1 + N$ diffs	$p_m(2^K+2K-1)$	$K + 2$ diffs
8	3	$16 p_m$	$1 + 8$	$13 p_m$	$3 + 2$
16	4	$32 p_m$	$1 + 16$	$23 p_m$	$4 + 2$
32	5	$64 p_m$	$1 + 32$	$41 p_m$	$5 + 2$
64	6	$128 p_m$	$1 + 64$	$75 p_m$	$6 + 2$
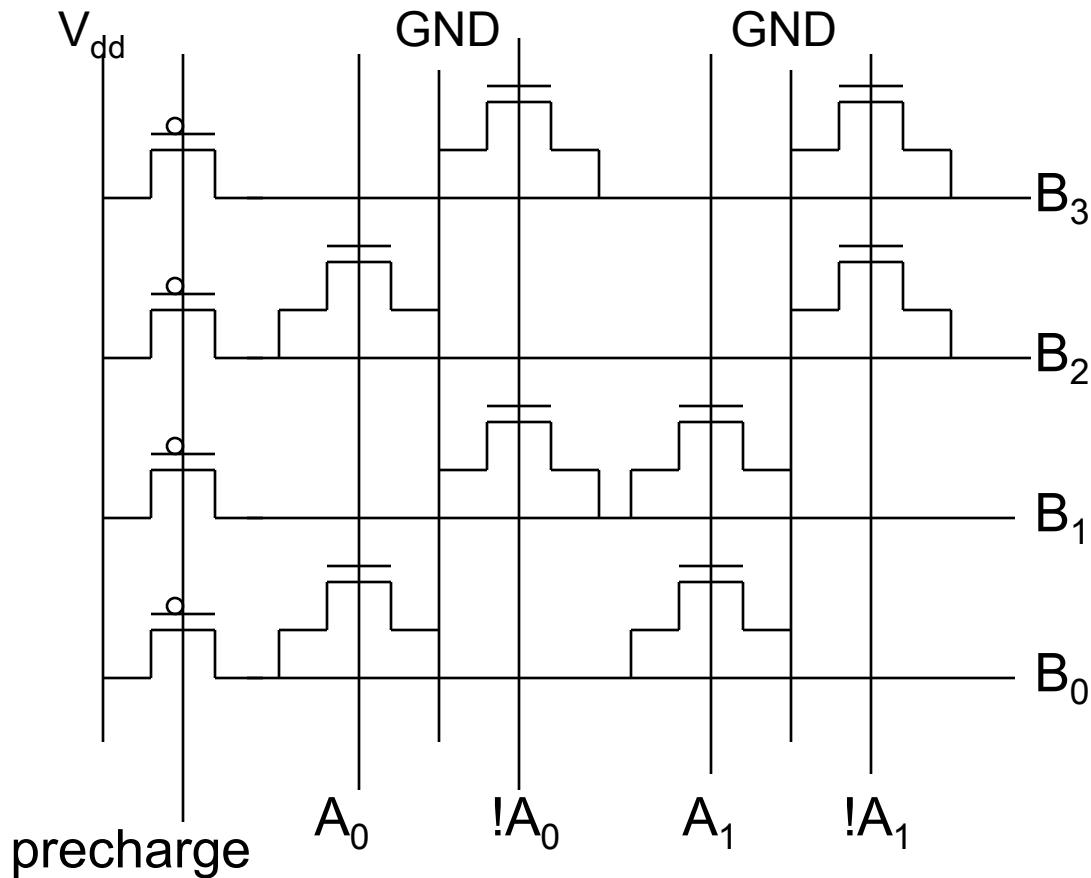
Decoders

❑ Decodes inputs to activate one of many outputs

Enable

In_0

In_1

2x4

$Out_0 = !In_1 \ \& \ !In_0$

$Out_1 = !In_1 \ \& \ In_0$

$Out_2 = In_1 \ \& \ !In_0$

$Out_3 = In_1 \ \& \ In_0$
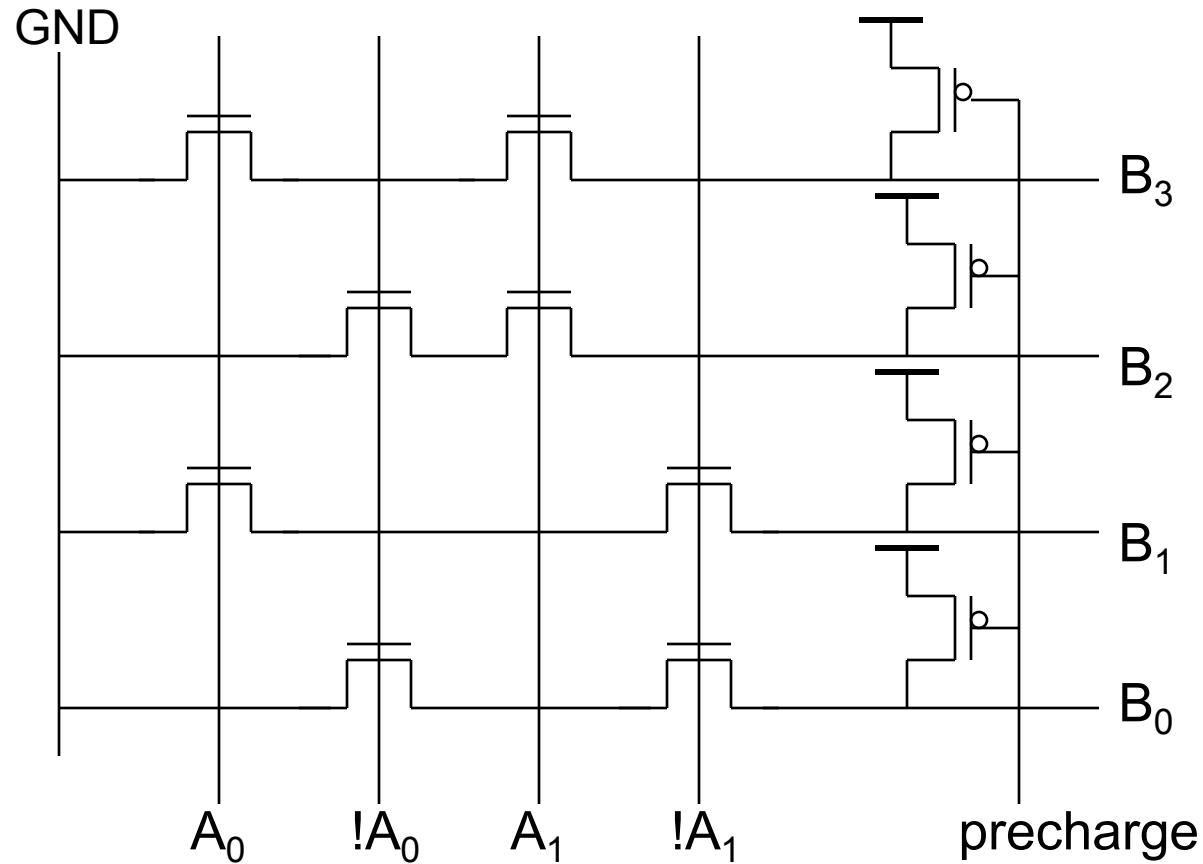
▫ two inverters, four 2-input nand gates, four inverters plus enable logic

▫ how about for a 3-to-8, 4-to-16, etc. decoder?
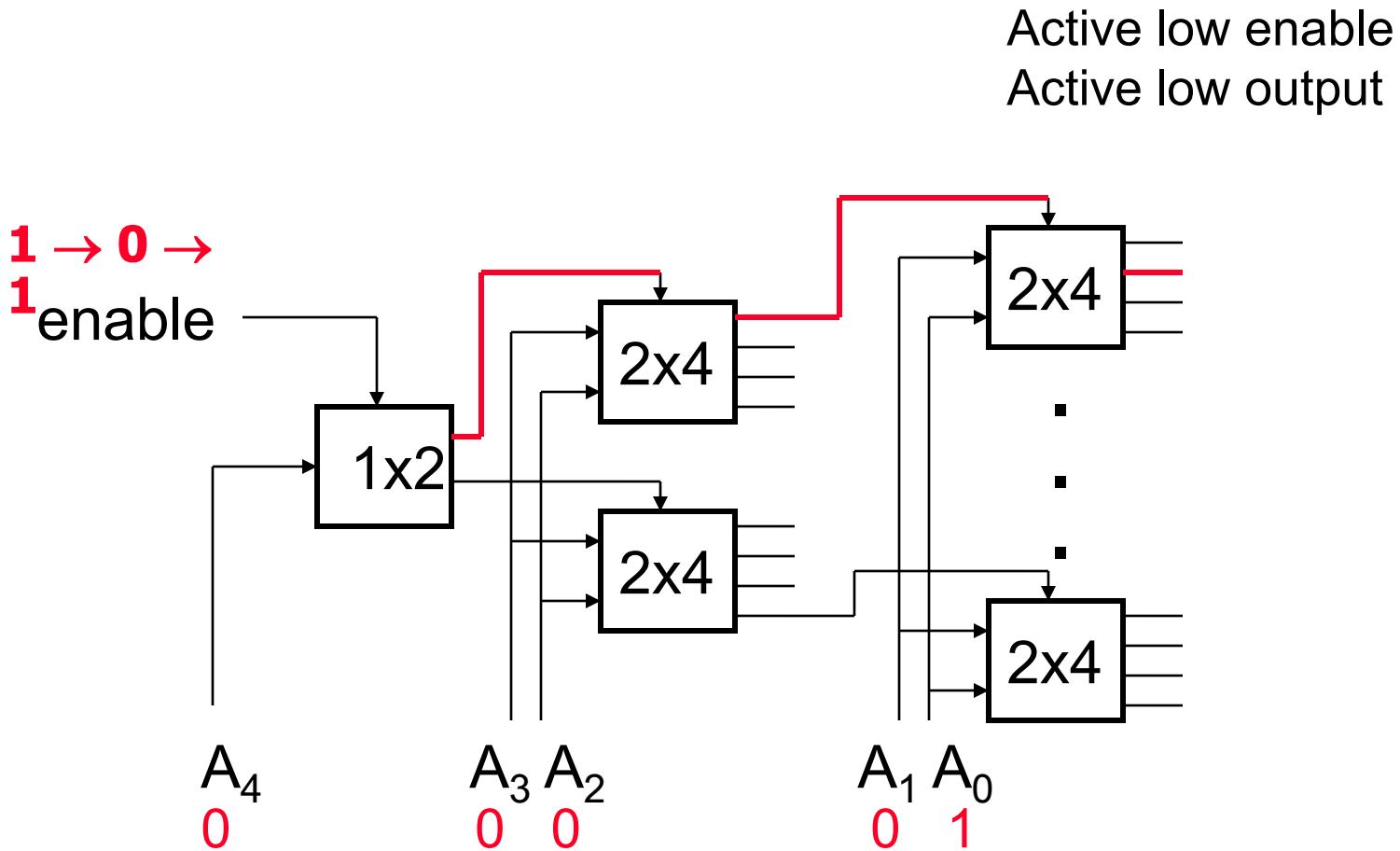
Dynamic NOR Decoder

Dynamic NAND Decoder
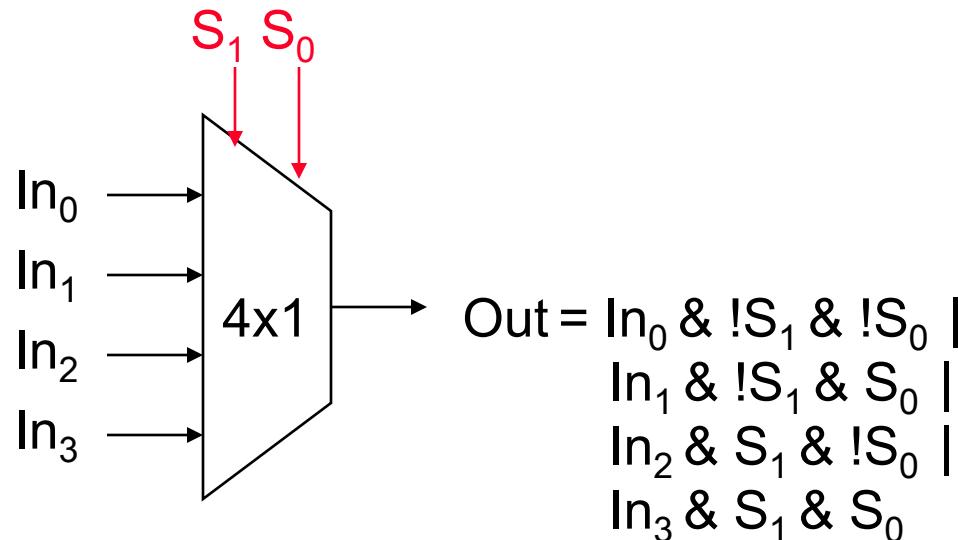
Building Big Decoders from Small

Active low enable
Active low output

$1 \rightarrow 0 \rightarrow$
1enable

1x2

2x4

2x4

2x4

2x4

.
.
.
.

A_4
0

A_3
0

A_2
0

A_1
0

A_0
1
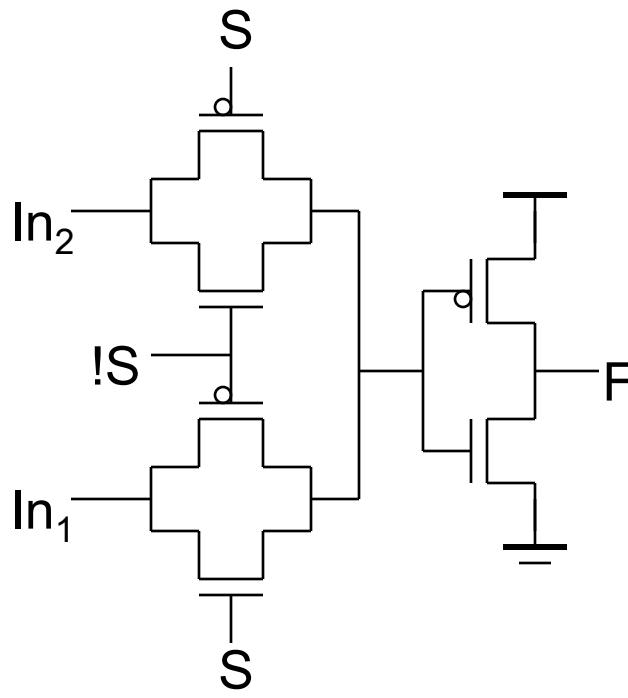
Multiplexers

❑ Selects one of several inputs to gate to the single output

S_1 S_0

In$_0$ →

In$_1$ →

In$_2$ → 4x1 → Out = In$_0$ & !S$_1$ & !S$_0$ |

In$_3$ →

$$\text{Out} = \text{In}_0 \ \& \ !S_1 \ \& \ !S_0 \ | \\ \text{In}_1 \ \& \ !S_1 \ \& \ S_0 \ | \\ \text{In}_2 \ \& \ S_1 \ \& \ !S_0 \ | \\ \text{In}_3 \ \& \ S_1 \ \& \ S_0$$
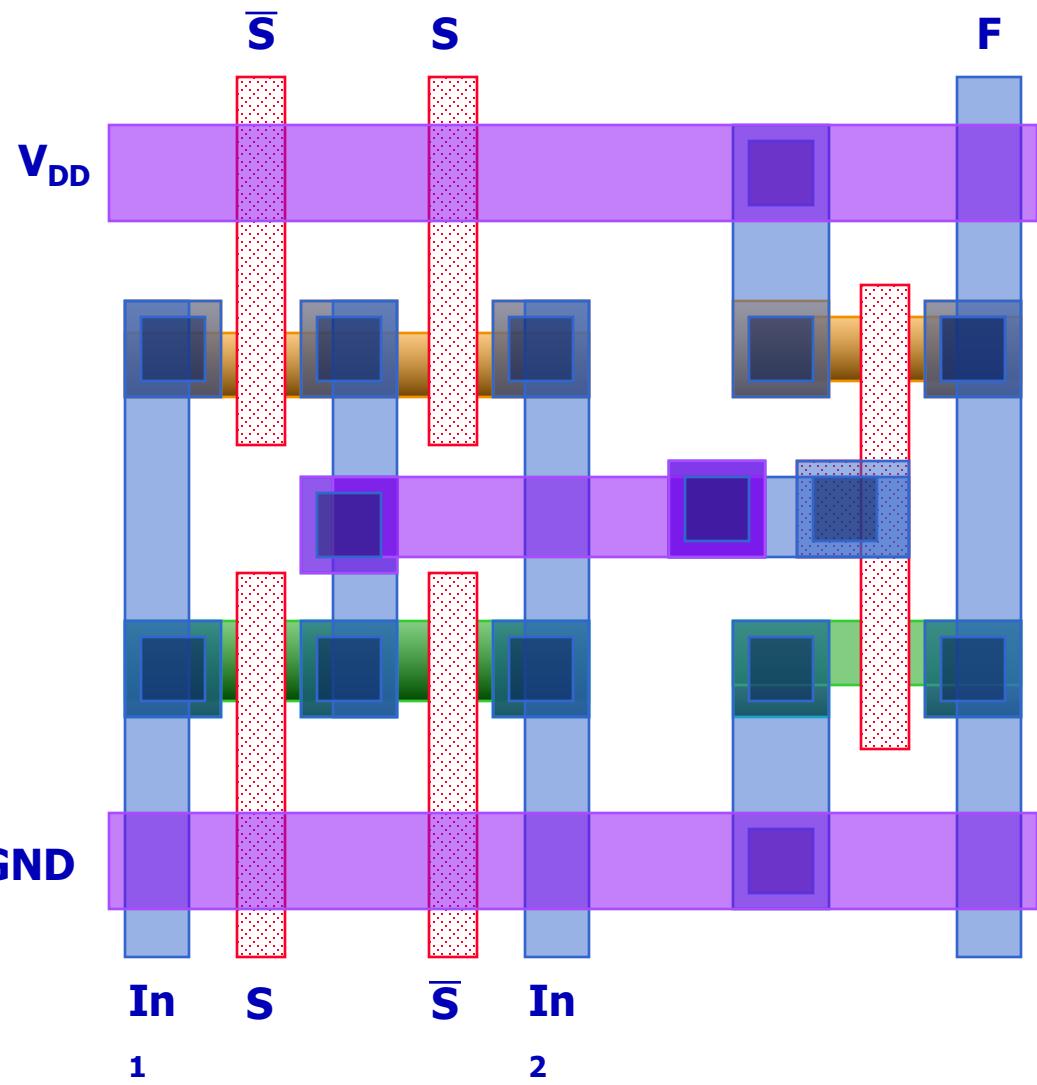
▫ two inverters, four 3-input nands, one 4-input nand

▫ how about for an 8x1, 16x1, etc. mux?
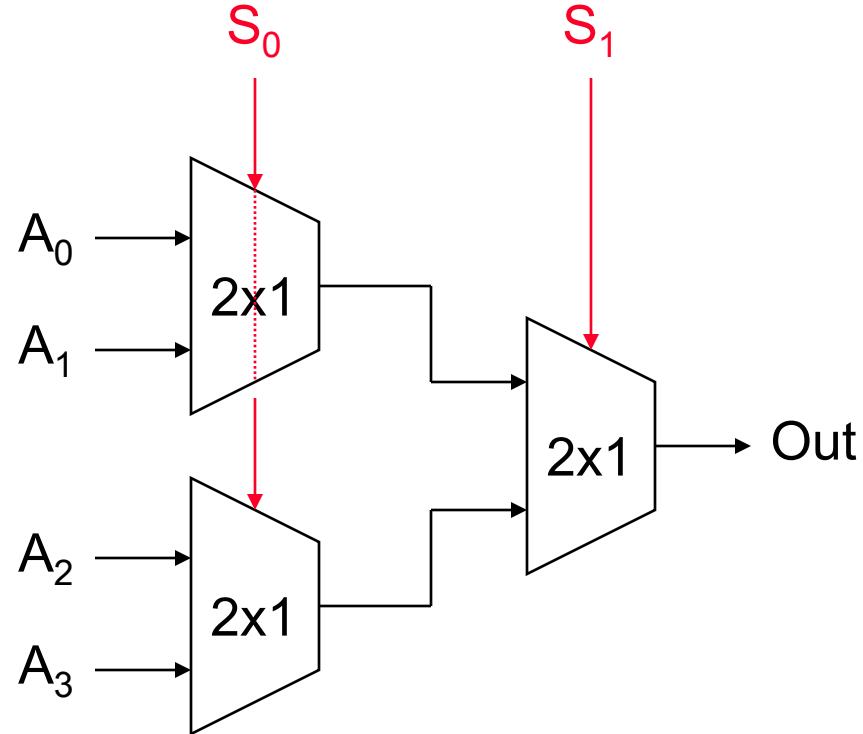
$$F = !((In_1 \& S) \mid (In_2 \& !S))$$
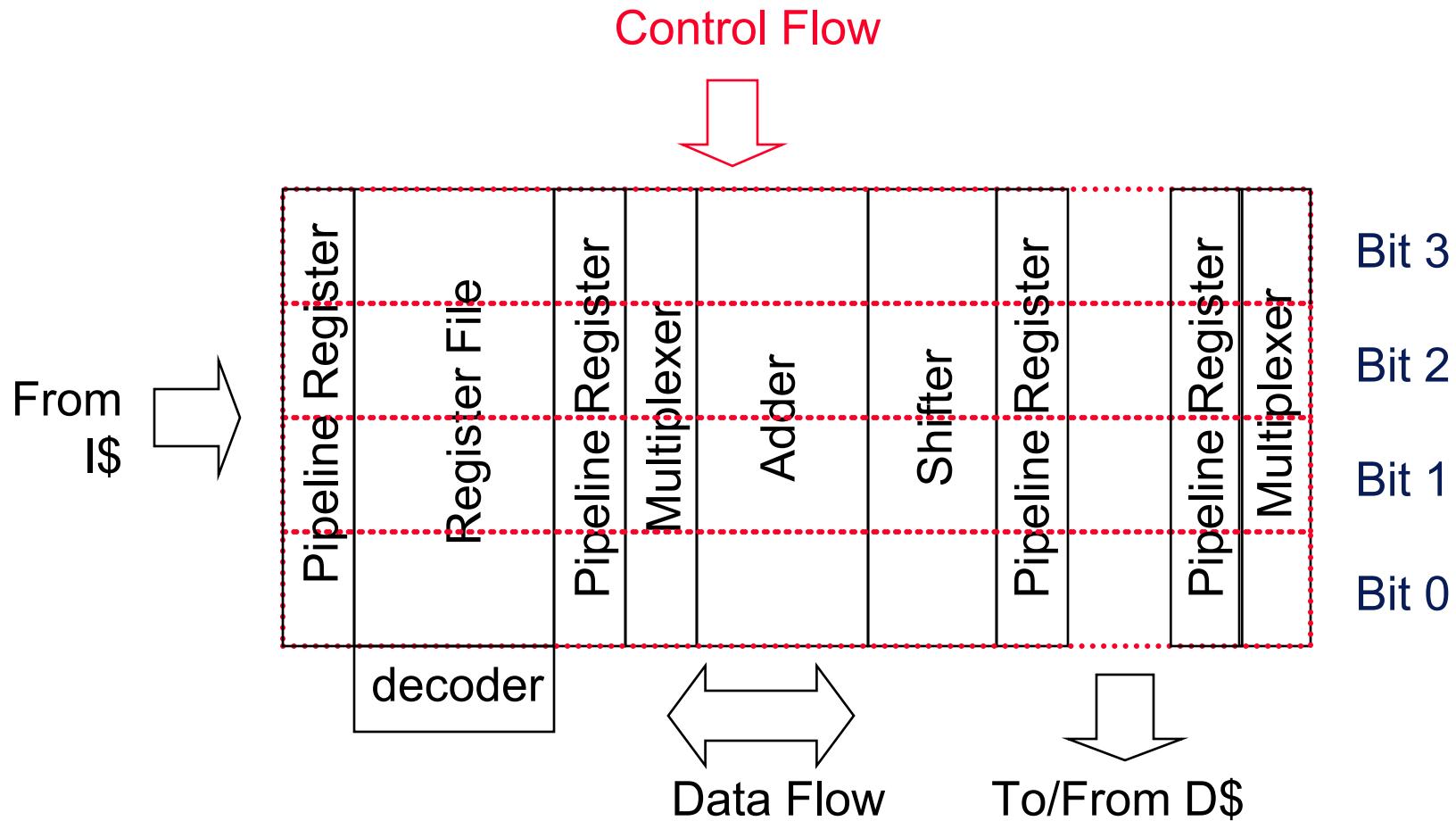
Building Big Muxes from Small
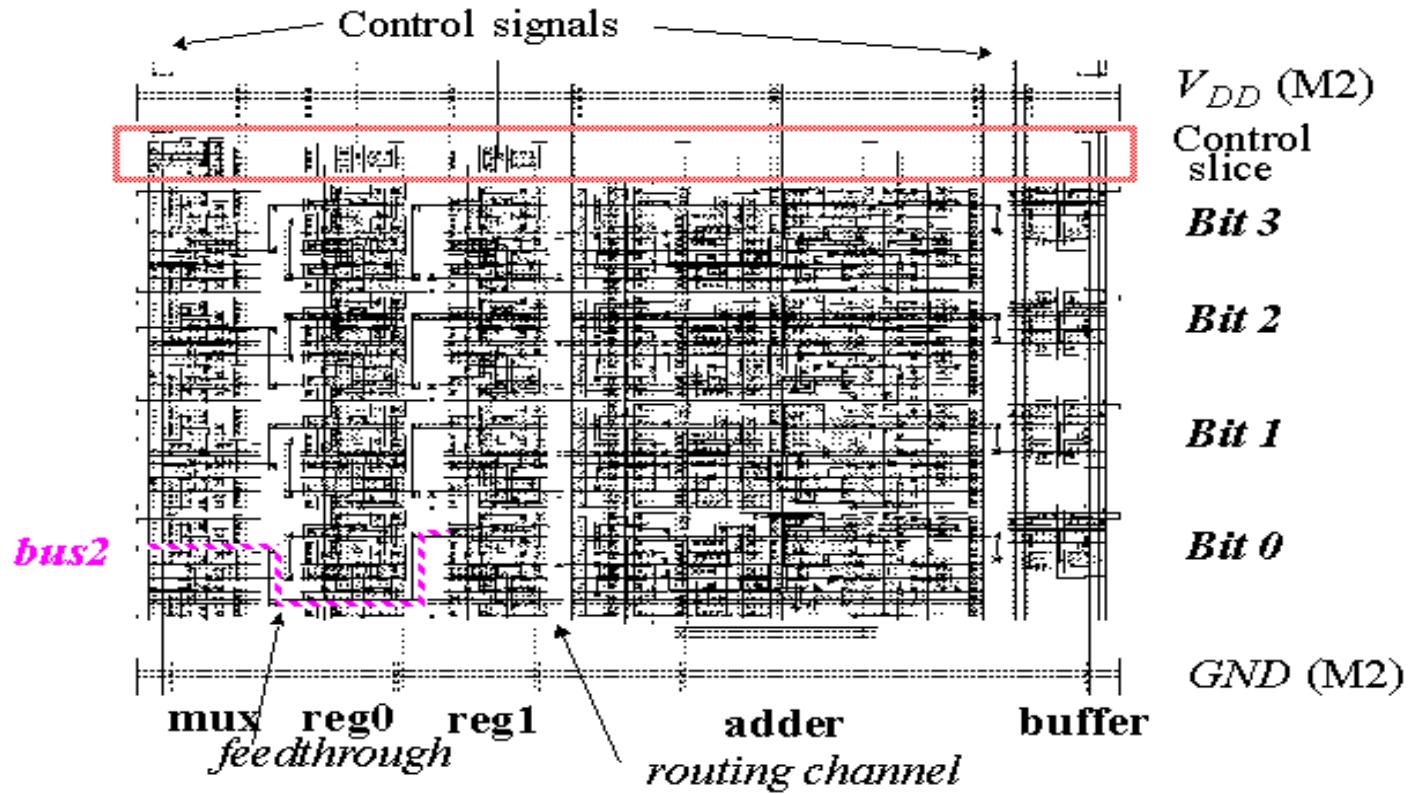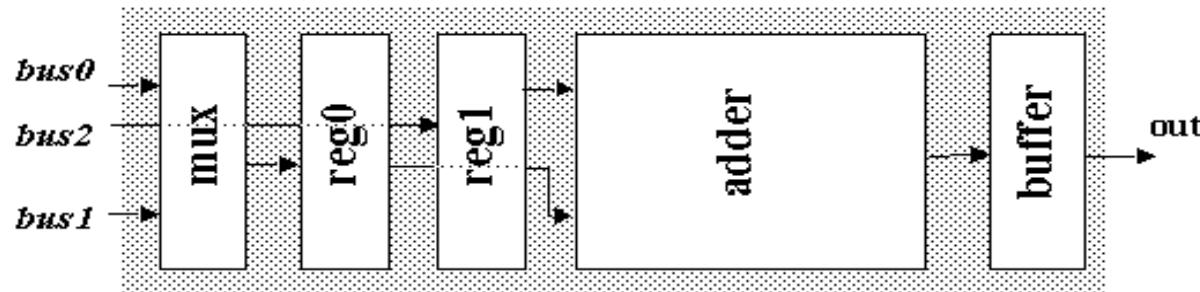
Review: Datapath Bit-Sliced Organization

Control Flow

From I$

| Pipeline Register | Register File | Pipeline Register | Multiplexer | Adder | Shifter | Pipeline Register | Pipeline Register | Multiplexer |

Bit 3

Bit 2

Bit 1

Bit 0

decoder

Data Flow

To/From D$
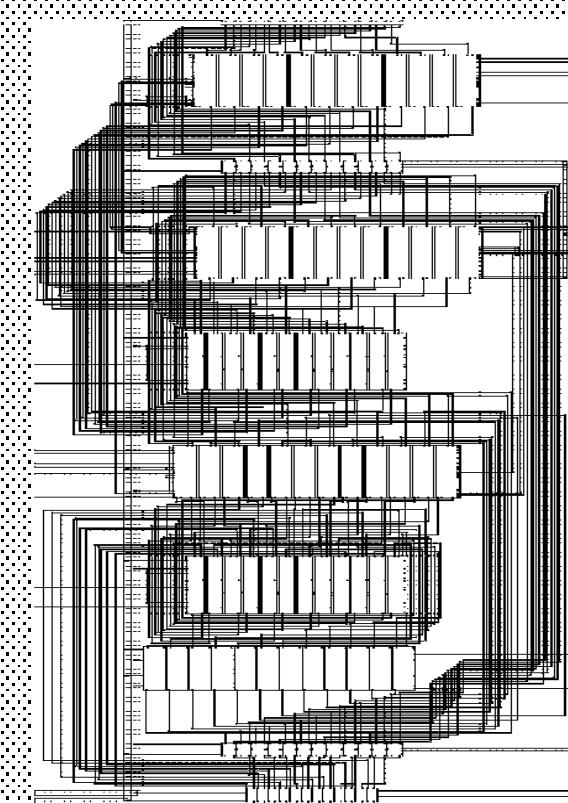
Tile identical bit-slice elements

Layout of Bit-Sliced Datapaths
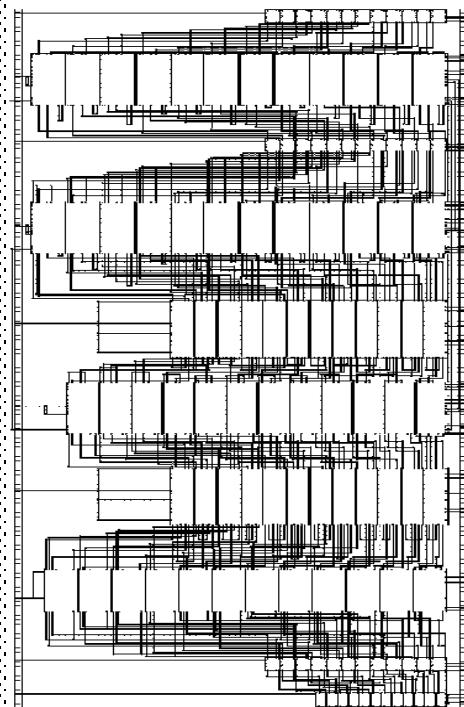
Layout of Bit-sliced Datapaths
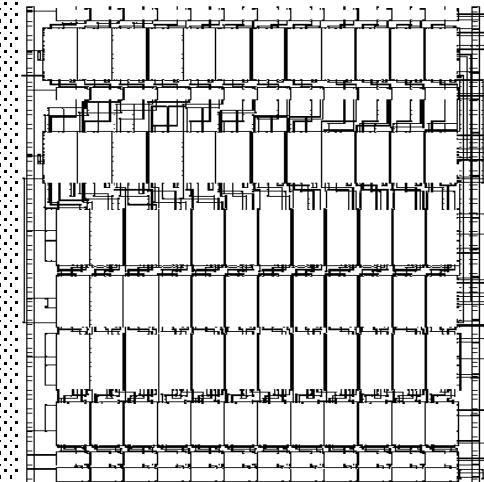
Without feedthroughs or pitch matching (4.2μm²)   **With feedthroughs (3.2μm²)**   **With feedthroughs and pitch matching (2.2μm²)**
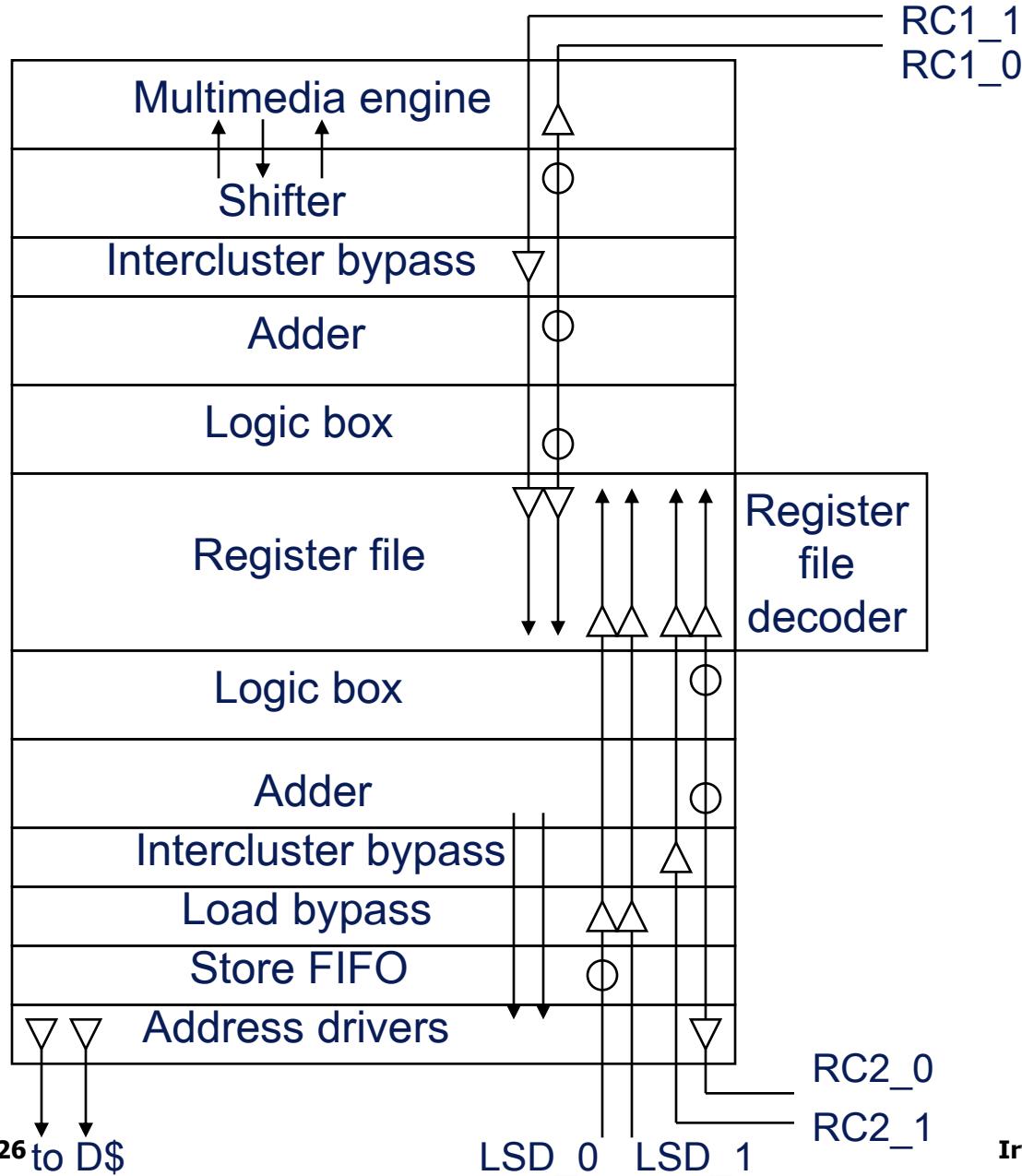
Alpha 21264 Integer Unit Datapath

RC1_1
RC1_0

Multimedia engine

Shifter

△ bus driver

○ tristate
bus driver

Intercluster bypass

Adder

Logic box

Register file

Register file decoder

Logic box

Adder

Intercluster bypass

Load bypass

Store FIFO

Address drivers

RC2_0
RC2_1

to D$ LSD_0 LSD_1   Irwin&Vijay, PSU, 2002

Next Lecture and Reminders

- Next lecture
  - Semiconductor memories
    - Reading assignment – Rabaey, et al, 12.1-12.2.1

- Reminders
  - Project final reports due December 5th
  - HW5 (last one!) due November 19th
  - Final grading negotiations/correction (except for the final exam) must be concluded by December 10th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in 118 and 121 Thomas