CSE477
VLSI Digital Circuits
Fall 2002

Lecture 21: Multiplier Design

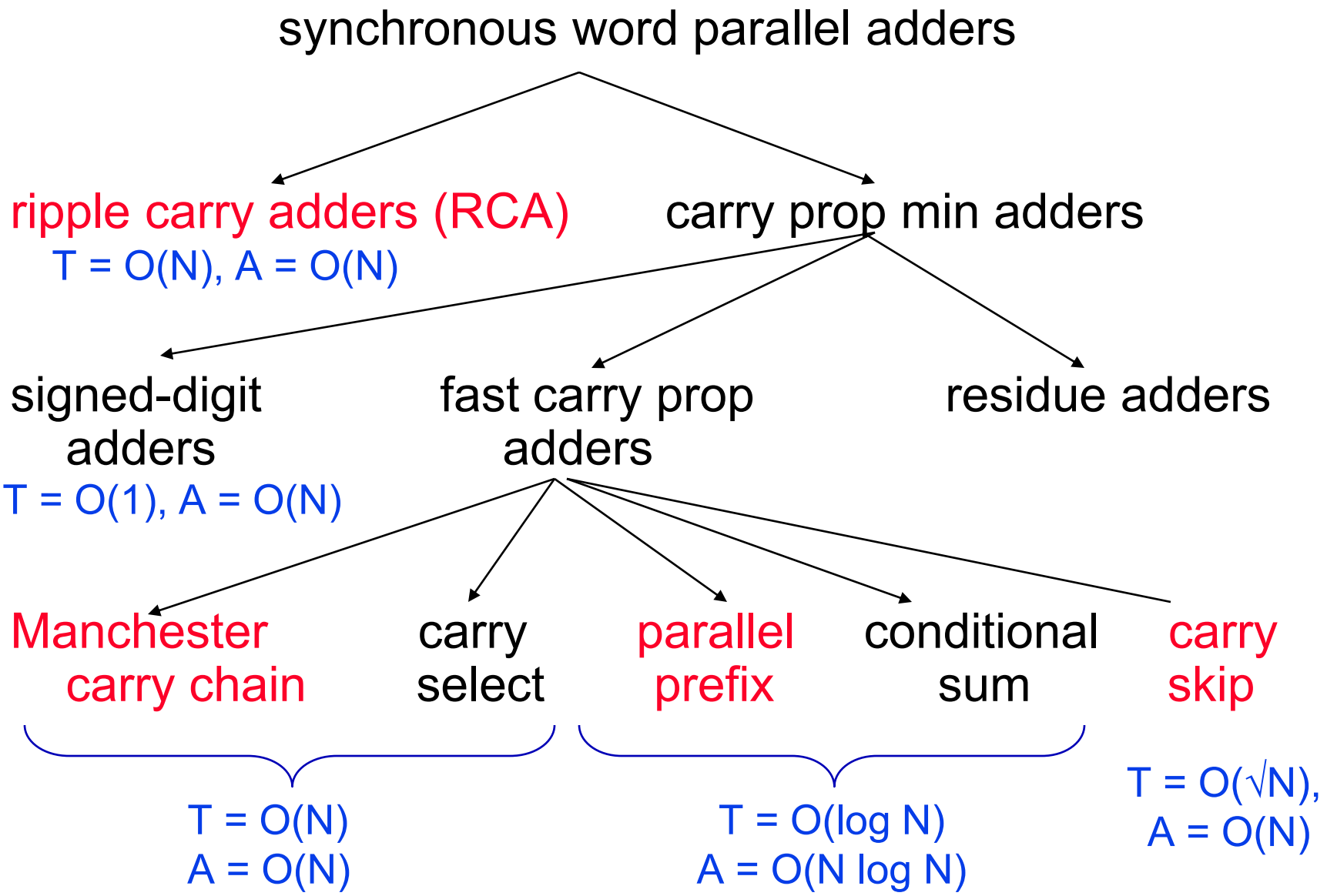
Mary Jane Irwin (www.cse.psu.edu/~mji)
www.cse.psu.edu/~cg477

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: Basic Building Blocks

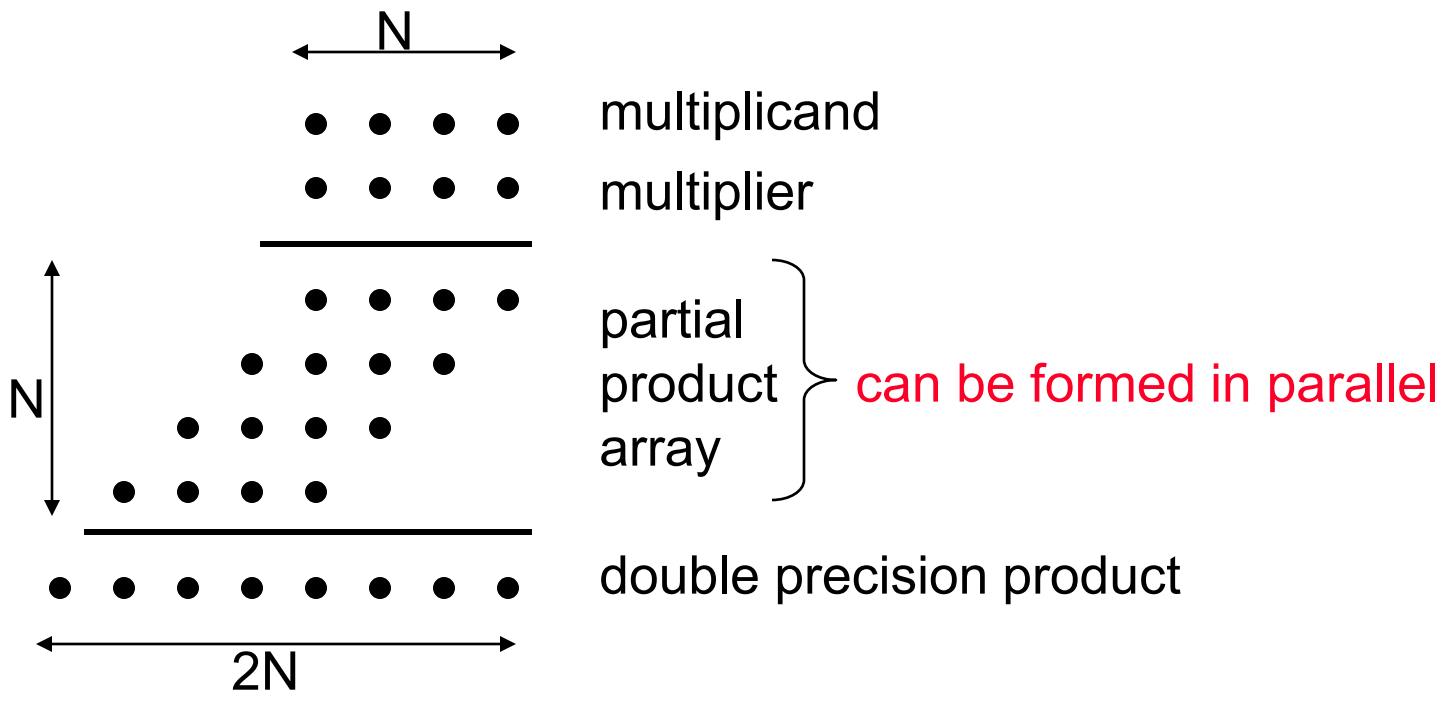
- Datapath
  - Execution units
    - Adder, multiplier, divider, shifter, etc.
  - Register file and pipeline registers
  - Multiplexers, decoders
- Control
  - Finite state machines (PLA, ROM, random logic)
- Interconnect
  - Switches, arbiters, buses
- Memory
  - Caches (SRAMs), TLBs, DRAMs, buffers

Review: Binary Adder Landscape



Multiply Operation

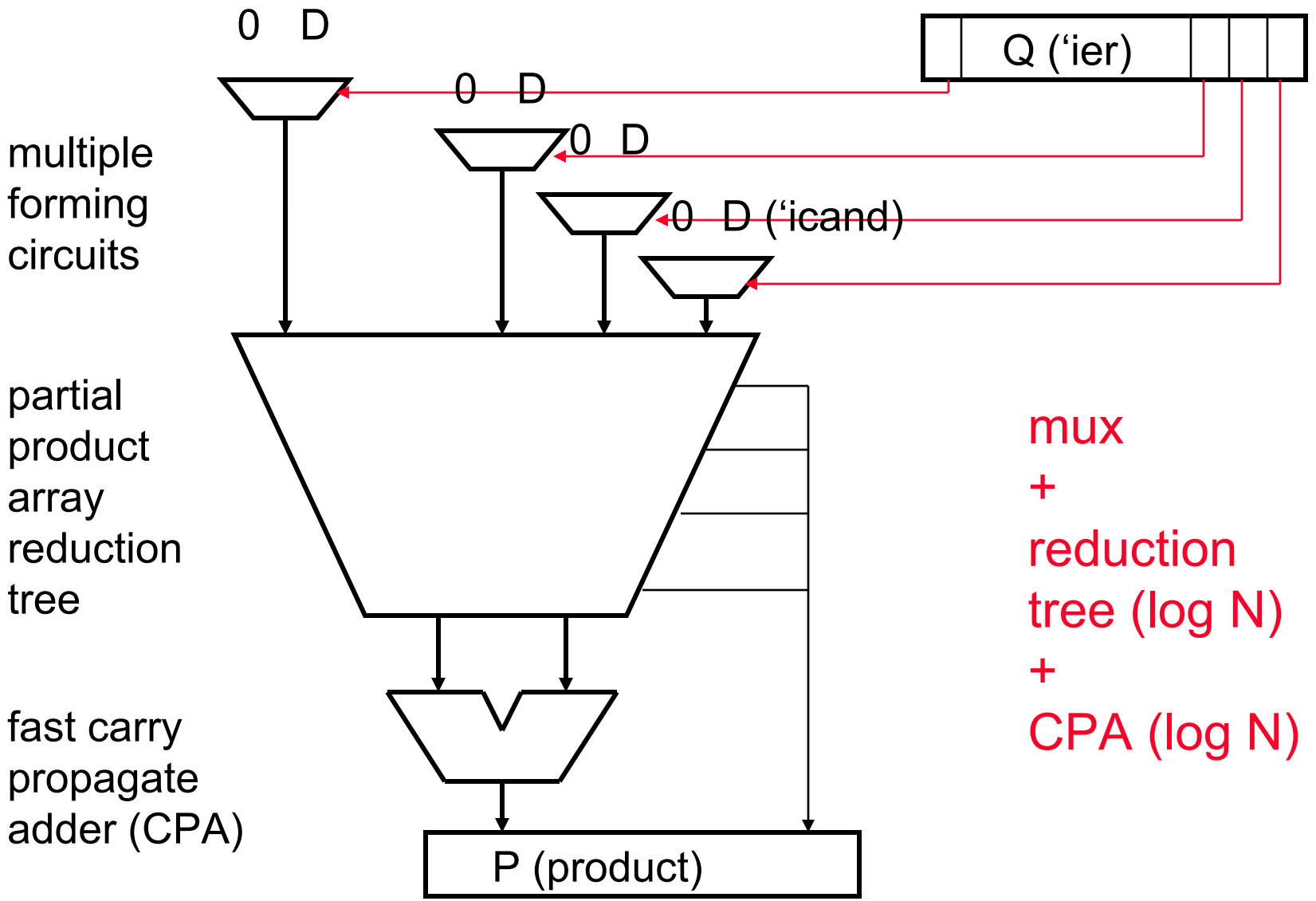
- Multiplication as repeated additions



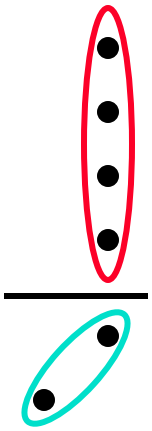
Shift & Add Multiplication

- Right shift and add
  - Partial product array rows are accumulated from top to bottom on an N-bit adder
  - After each addition, right shift (by one bit) the accumulated partial product to align it with the next row to add
  - Time for N bits $T_{serial\_mult} = O(N\,T_{adder}) = O(N^2)$ for a RCA
- Making it faster
  - Use a faster adder
  - Use higher radix (e.g., base 4) multiplication
    - Use multiplier recoding to simplify multiple formation
  - Form partial product array in parallel and add it in parallel
- Making it smaller (i.e., slower)
  - Use an array multiplier
    - Very regular structure with only short wires to nearest neighbor cells. Thus, very simple and efficient layout in VLSI
    - Can be easily and efficiently pipelined

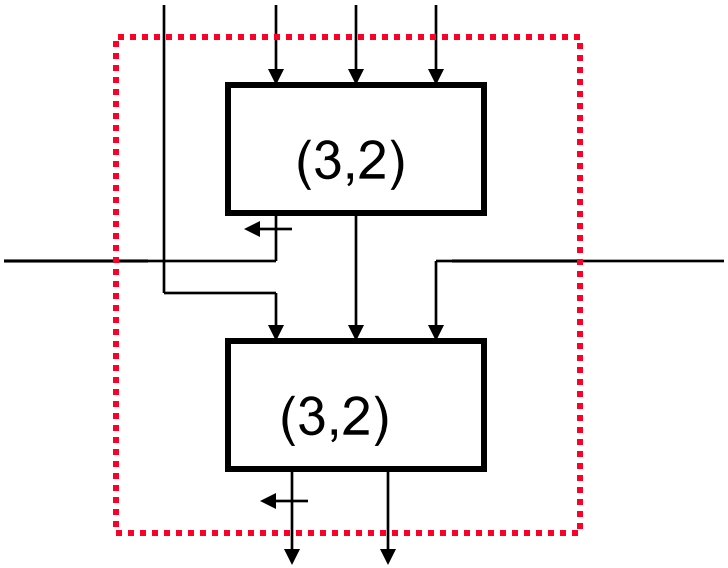
Tree Multiplier Structure



(4,2) Counter

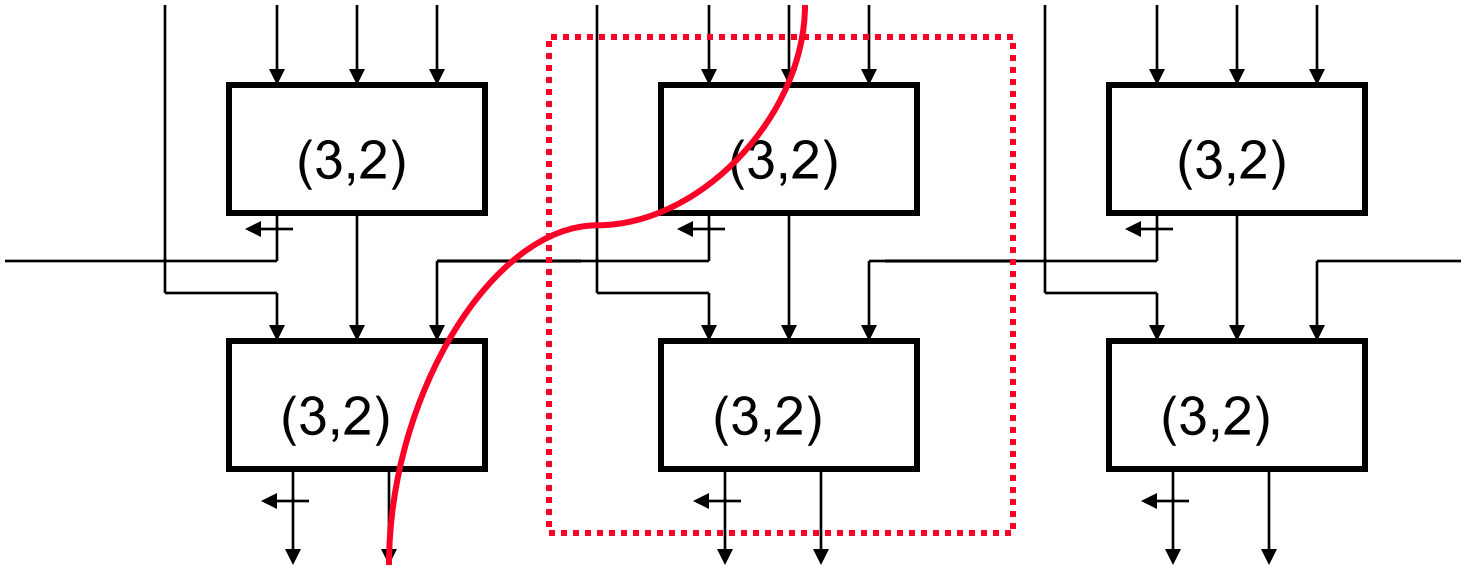


- Built out of two (3,2) counters (just FA's!)
  - all of the inputs (4 external plus one internal) have the same weight (i.e., are in the same bit position)
  - the internal output is carried to the next higher weight position (indicated by the ←)



Note: Two carry outs - one "internal" and one "external"

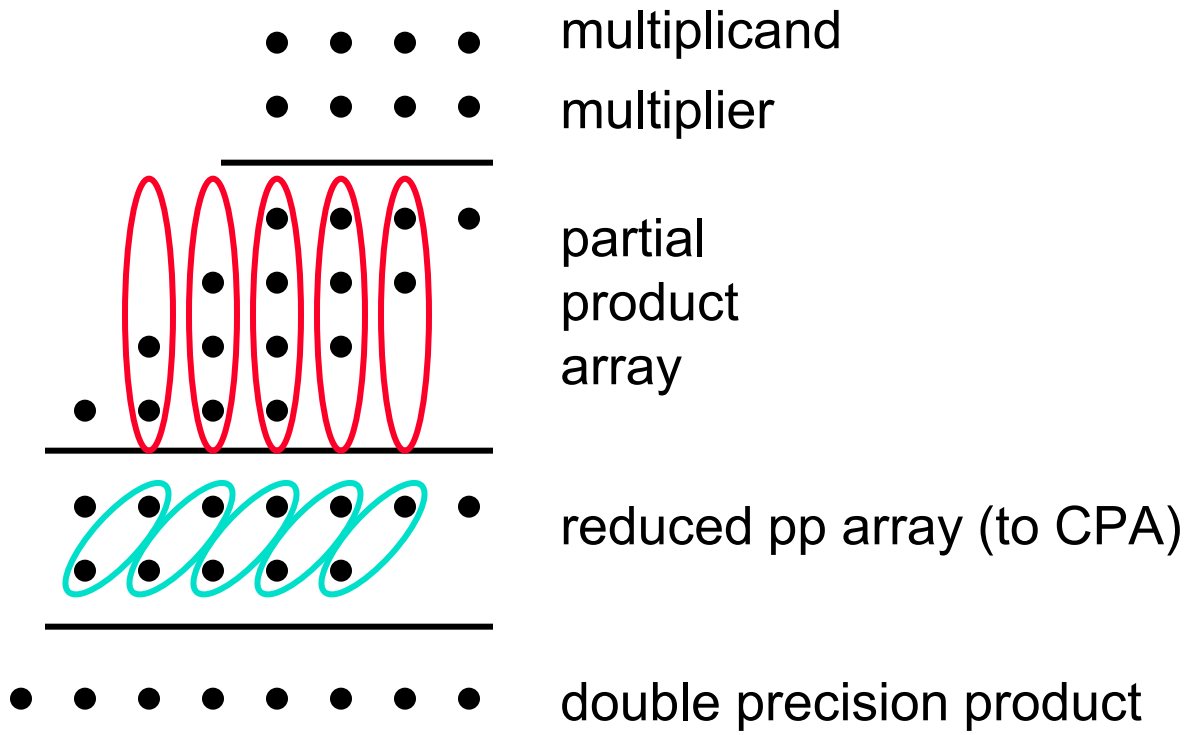
Tiling (4,2) Counters



- Reduces columns four high to columns only two high
  - Tiles with neighboring (4,2) counters
  - Internal carry in at same “level” (i.e., bit position weight) as the internal carry out

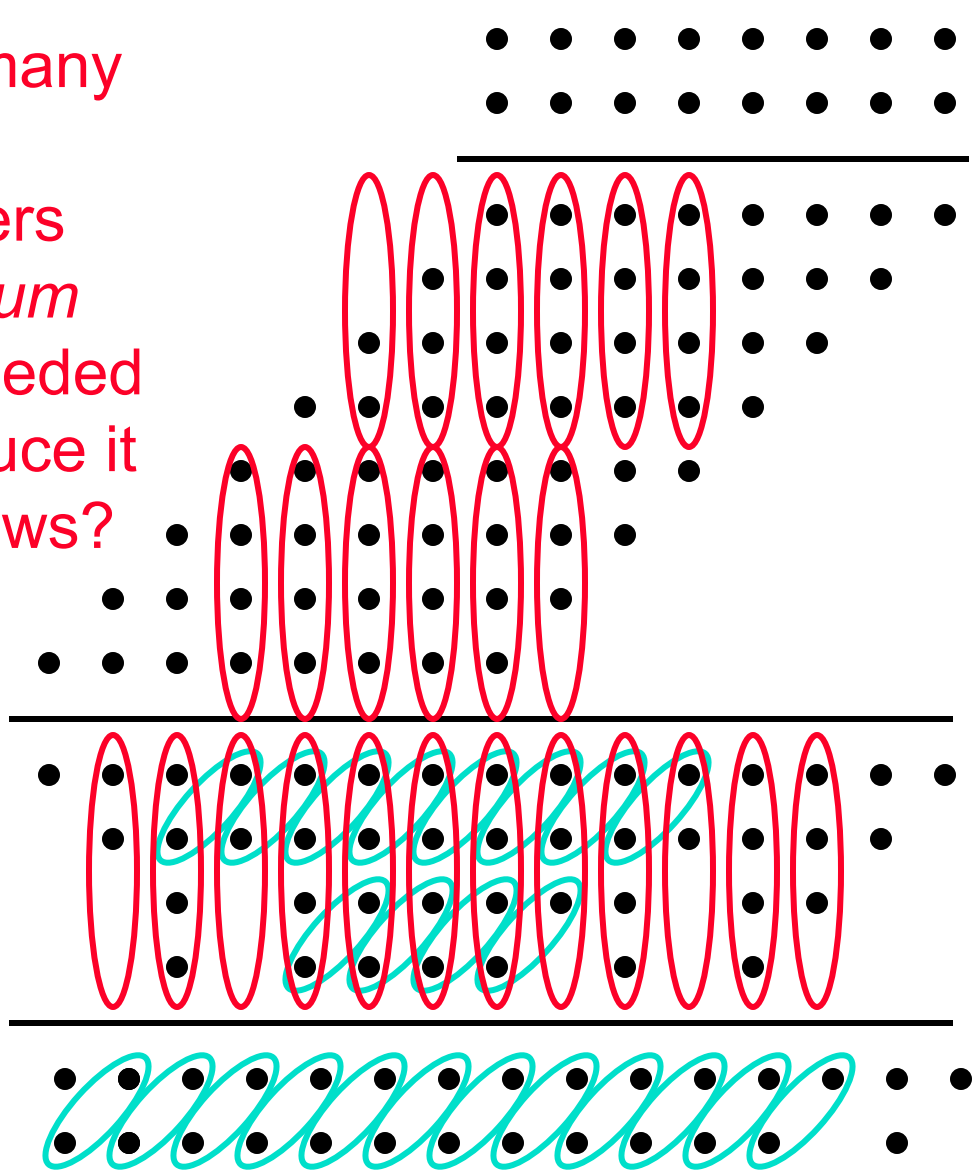
4x4 Partial Product Array Reduction

- Fast 4x4 multiplication using (4,2) counters



8x8 Partial Product Array Reduction

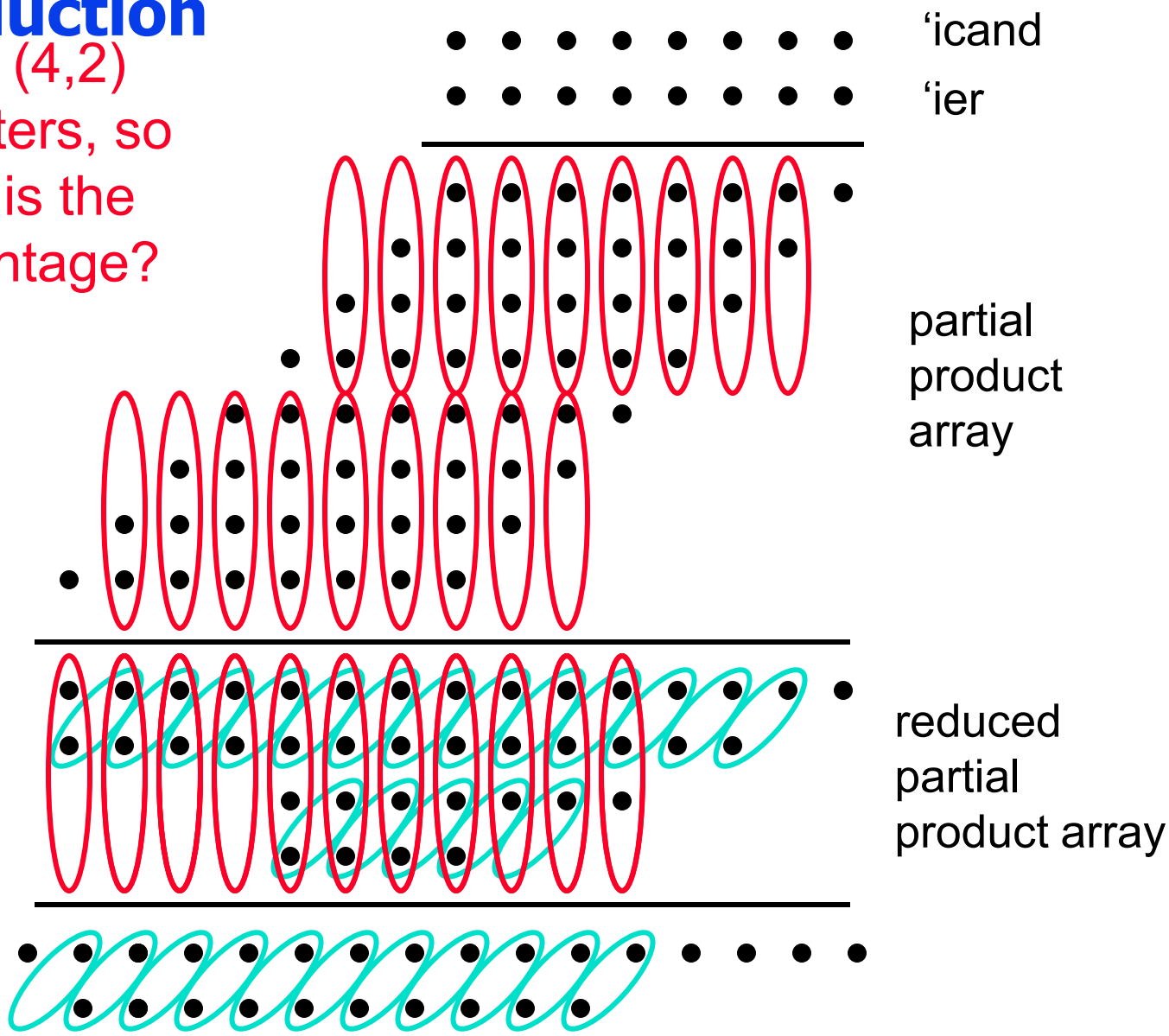
How many (4,2) counters *minimum* are needed to reduce it to 2 rows?



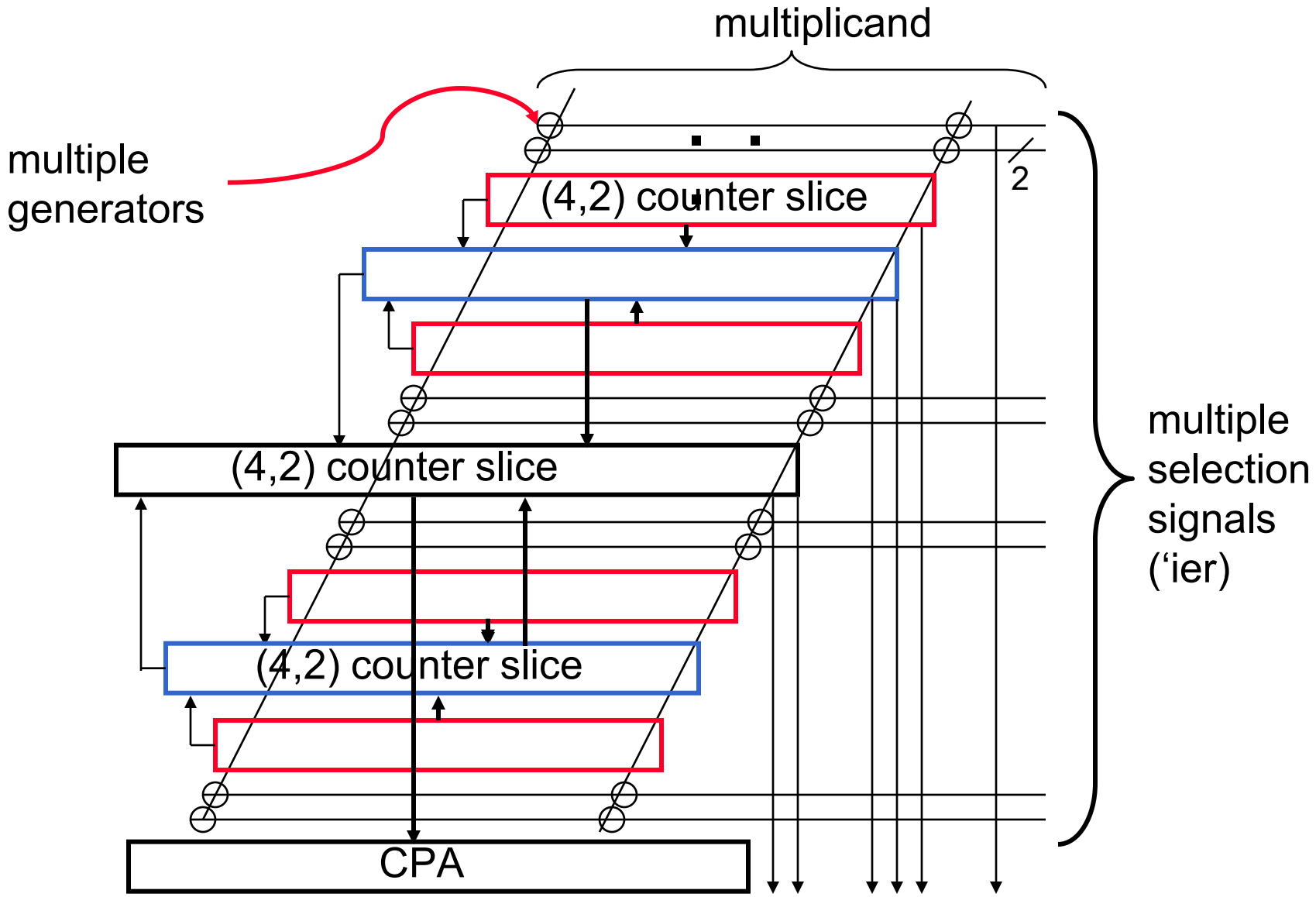
Answer: 24

Alternate 8x8 Partial Product Array Reduction

More (4,2) counters, so what is the advantage?



Array Reduction Layout Approach



Next Lecture and Reminders

- Next lecture
  - Shifters, decoders, and multiplexers
    - Reading assignment – Rabaey, et al, 11.5-11.6
- Reminders
  - Project final reports due December 5th
  - HW5 (last one!) due November 19th
  - Final grading negotiations/correction (except for the final exam) must be concluded by December 10th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in 118 and 121 Thomas