CSE477
VLSI Digital Circuits
Fall 2002

Lecture 24: RAM Cores

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

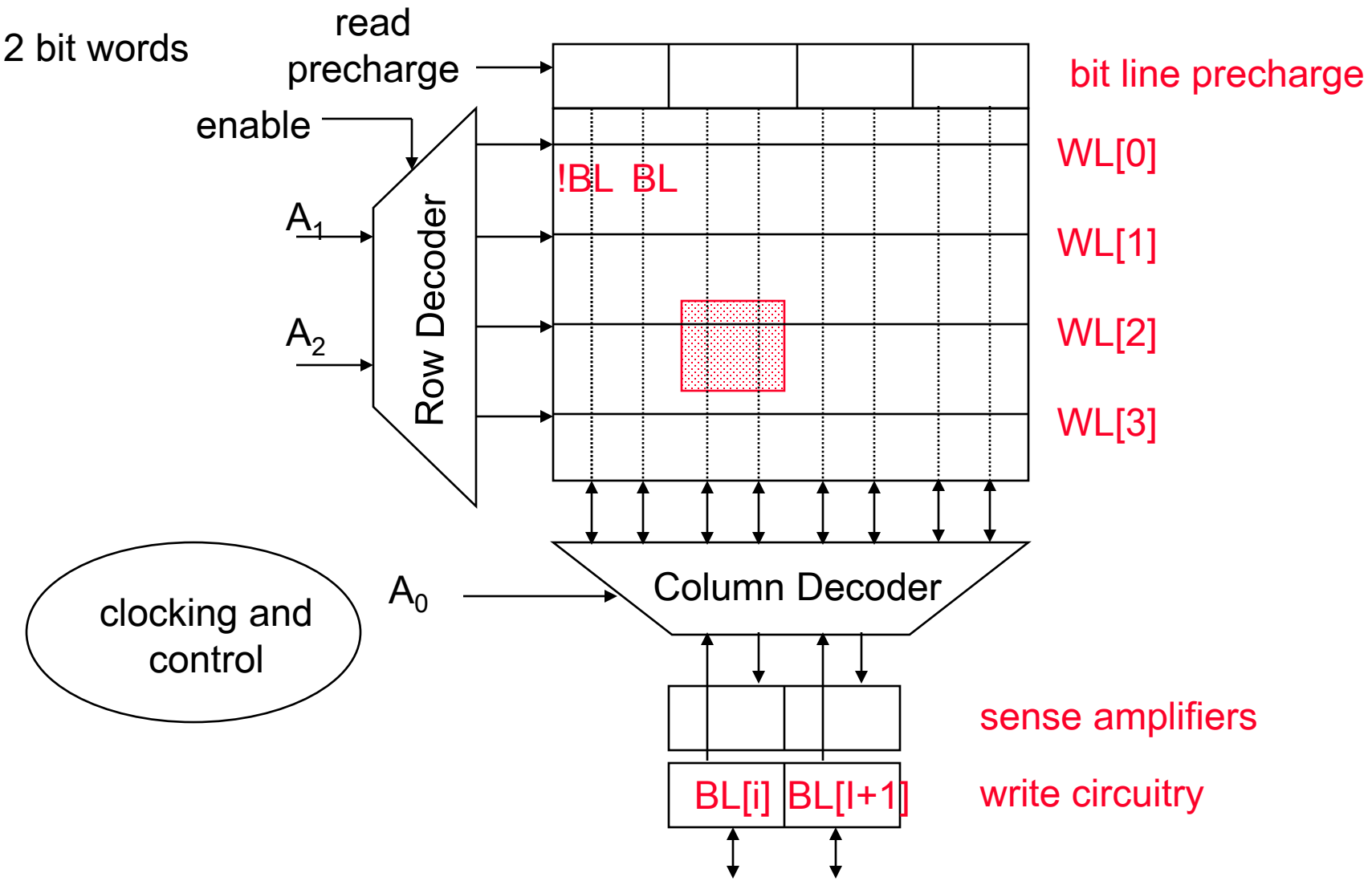
Review: Basic Building Blocks

- Datapath
  - Execution units
    - Adder, multiplier, divider, shifter, etc.
  - Register file and pipeline registers
  - Multiplexers, decoders
- Control
  - Finite state machines (PLA, ROM, random logic)
- Interconnect
  - Switches, arbiters, buses
- Memory
  - Caches (SRAMs), TLBs, DRAMs, buffers

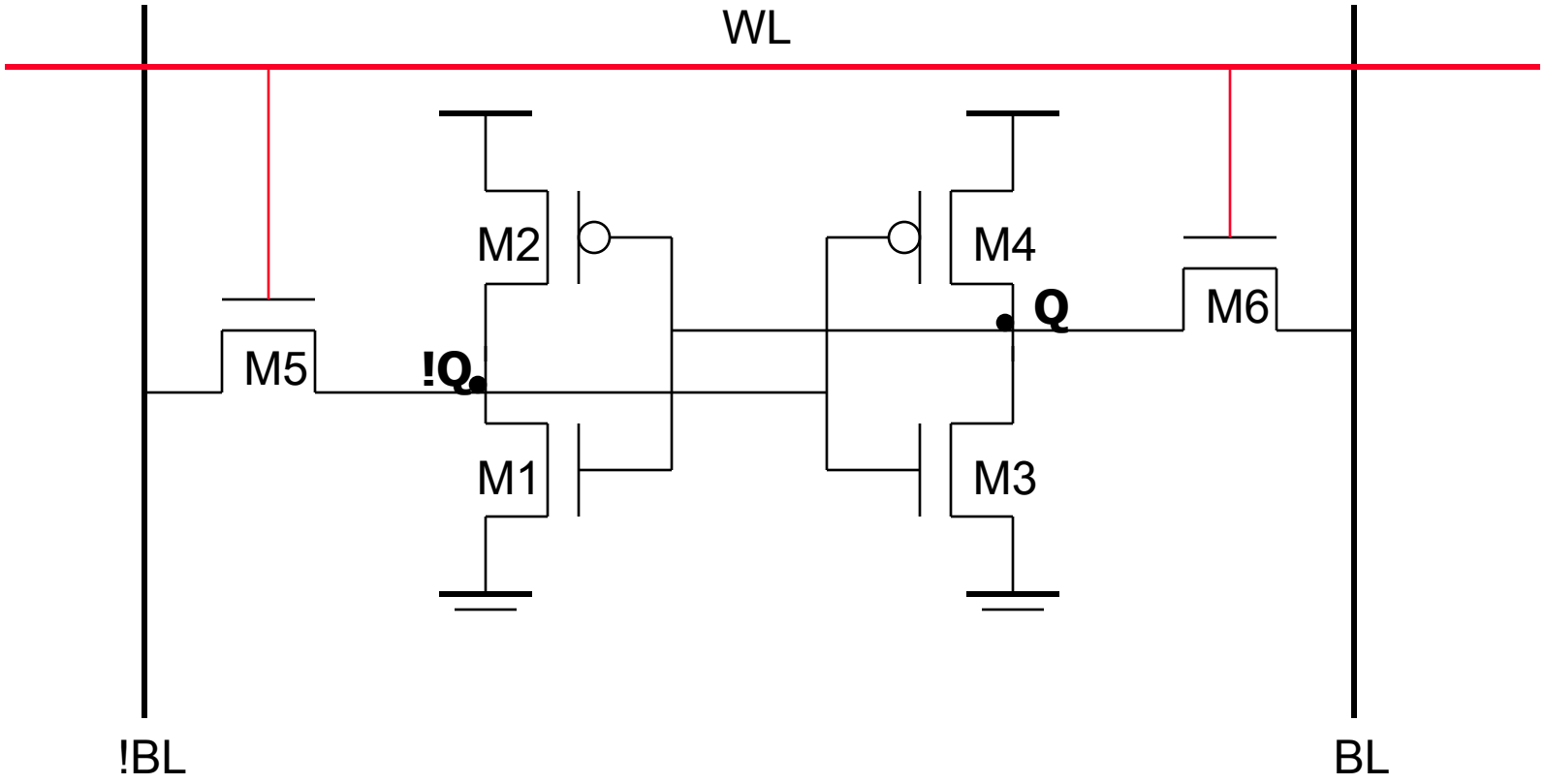
Review: Read-Write Memories (RAMs)

- Static – SRAM
  - data is stored as long as supply is applied
  - large cells (6 fets/cell) – so fewer bits/chip
  - fast – so used where speed is important (e.g., caches)
  - differential outputs (output BL and !BL)
  - use sense amps for performance
  - compatible with CMOS technology
- Dynamic – DRAM
  - periodic refresh required
  - small cells (1 to 3 fets/cell) – so more bits/chip
  - slower – so used for main memories
  - single ended output (output BL only)
  - need sense amps for correct operation
  - not typically compatible with CMOS technology

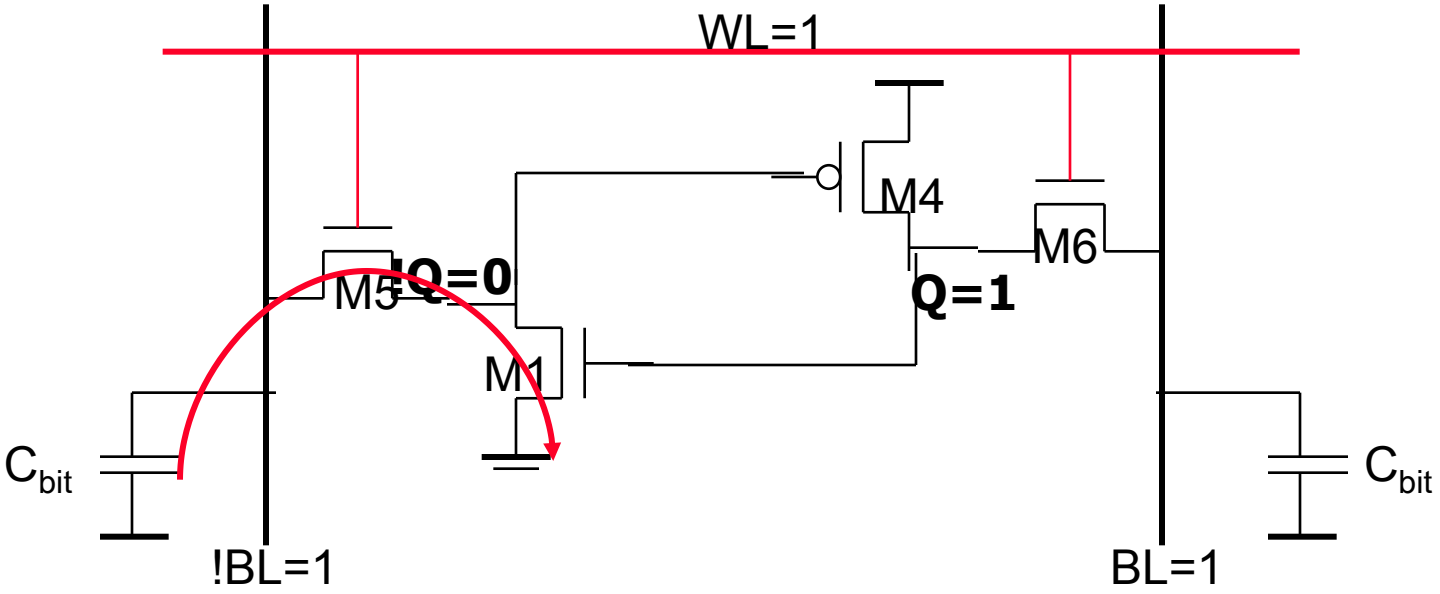
Review: 4x4 SRAM Memory



6-transistor SRAM Cell

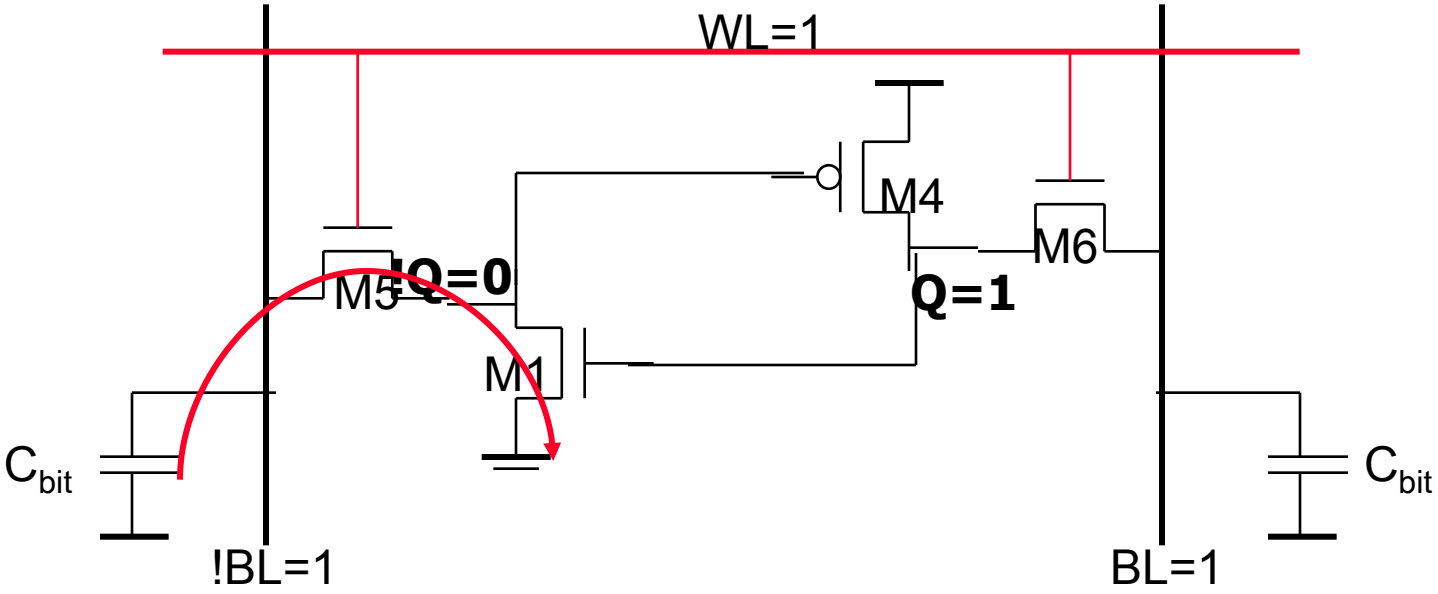


SRAM Cell Analysis (Read)



Read-disturb (read-upset): must carefully limit the allowed voltage rise on !Q to a value that prevents the read-upset condition from occurring while simultaneously maintaining acceptable circuit speed and area constraints

SRAM Cell Analysis (Read)

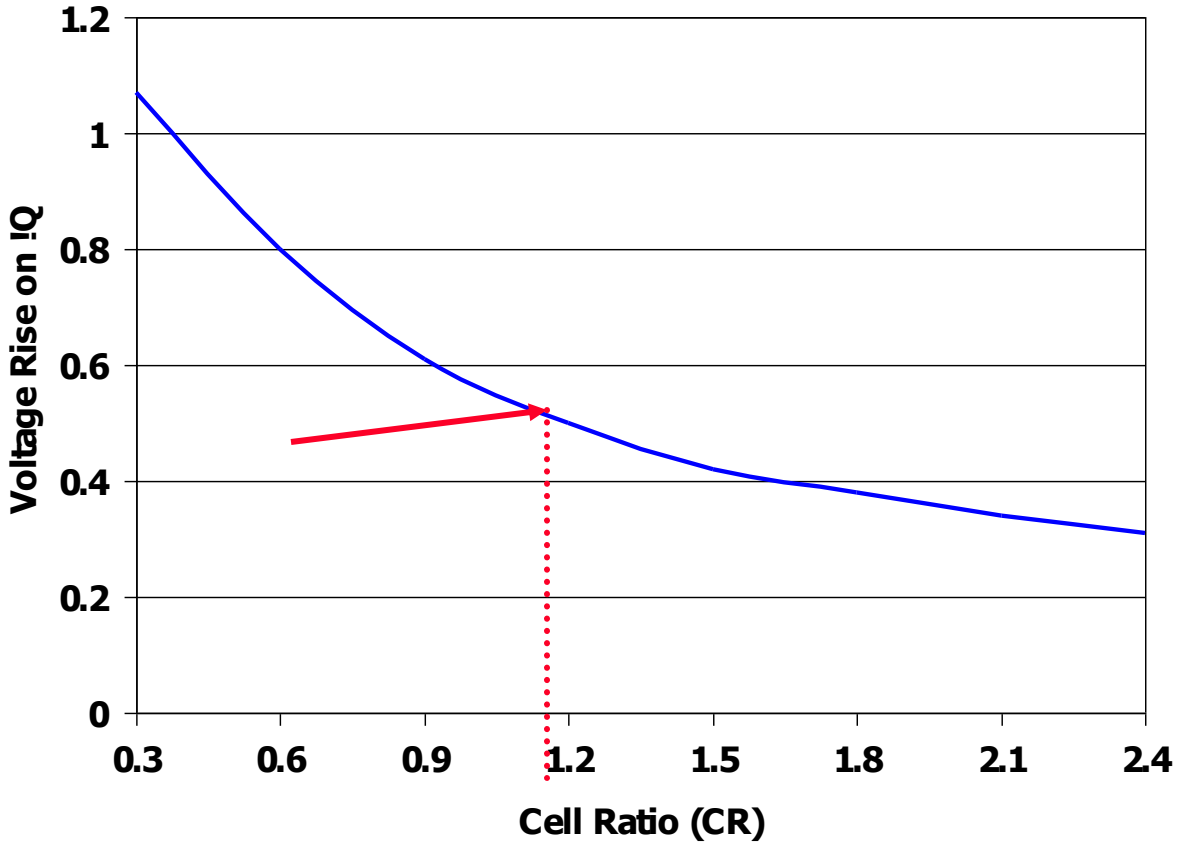


Cell Ratio (CR) = $(W_{M1}/L_{M1})/(W_{M5}/L_{M5})$

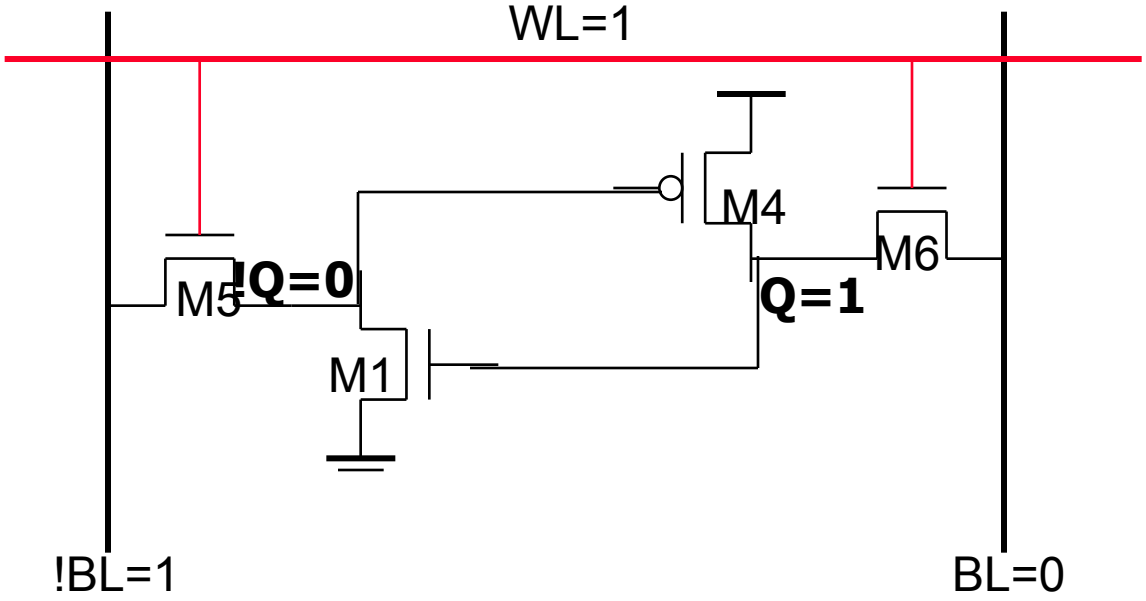
$V_{!Q} = [(V_{dd} - V_{Tn})(1 + CR \pm \sqrt{(CR(1 + CR))}]/(1 + CR)$

Read Voltages Ratios

V_{dd} = 2.5V
V_{Tn} = 0.5V



SRAM Cell Analysis (Write)

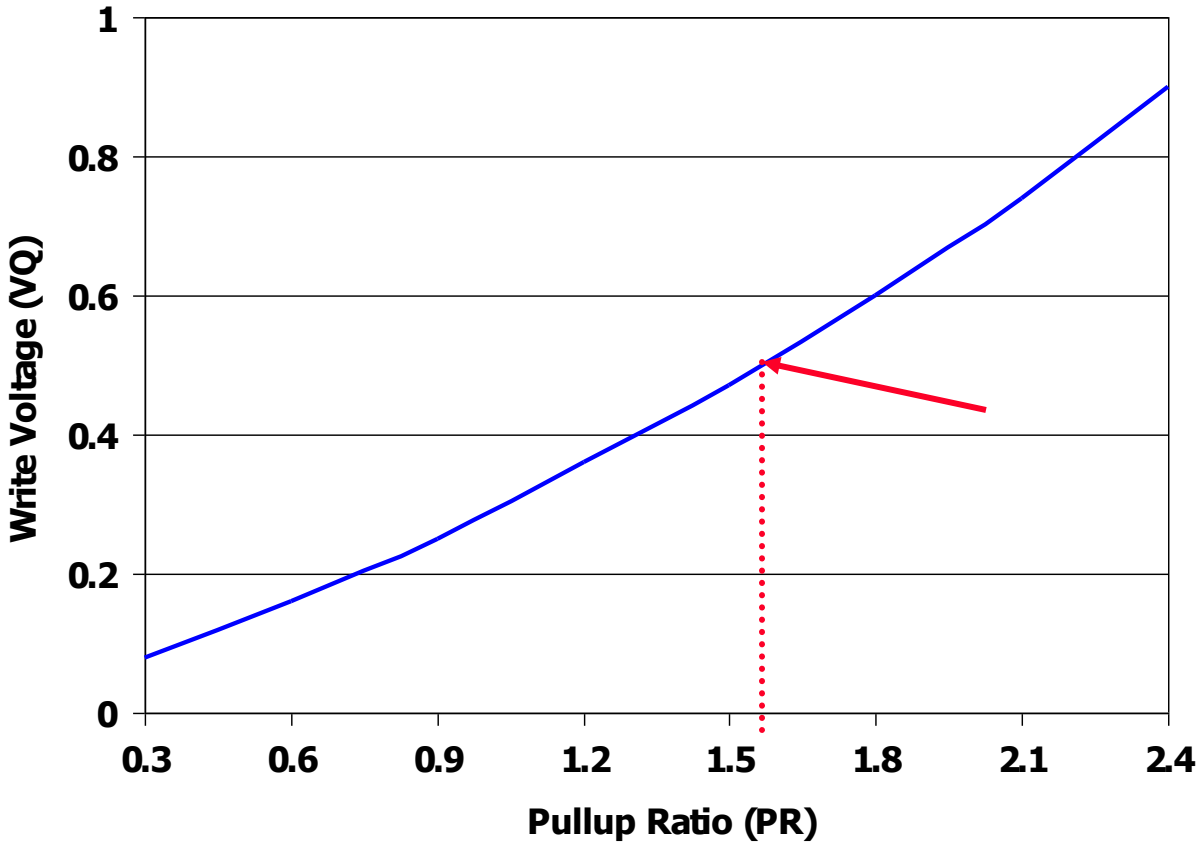


Pullup Ratio (PR) = $(W_{M4}/L_{M4})/(W_{M6}/L_{M6})$

$$V_Q = (V_{dd} - V_{Tn}) \pm \sqrt{((V_{dd} - V_{Tn})^2 - (\mu_p/\mu_n)(PR)((V_{dd} - V_{Tn} - V_{Tp})^2)}$$

Write Voltages Ratios

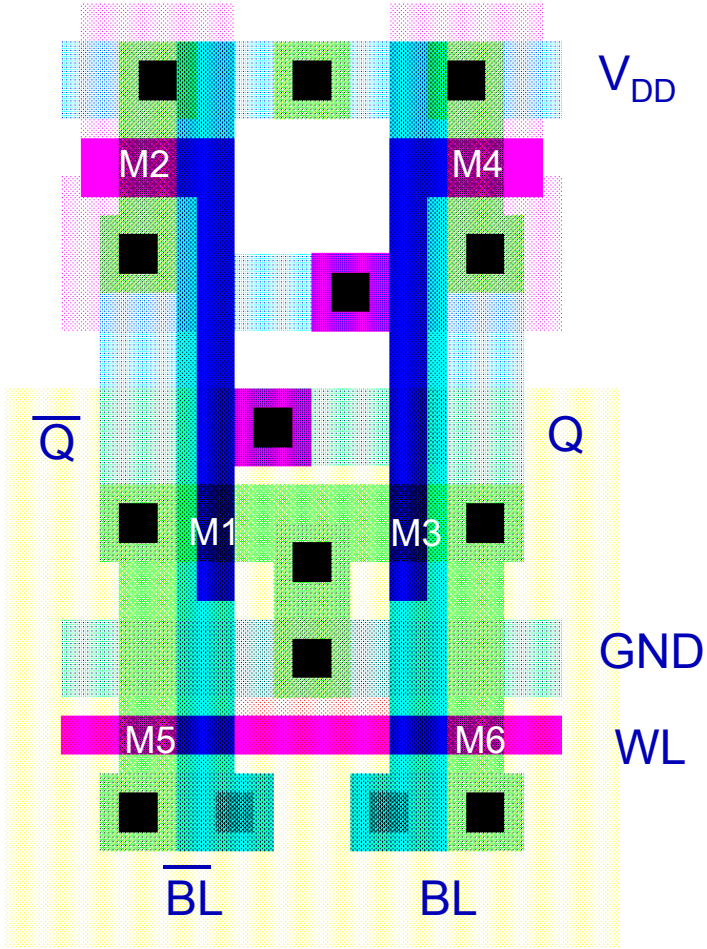
V_{dd} = 2.5V
$|V_{Tp}|$ = 0.5V
μ_p/μ_n = 0.5



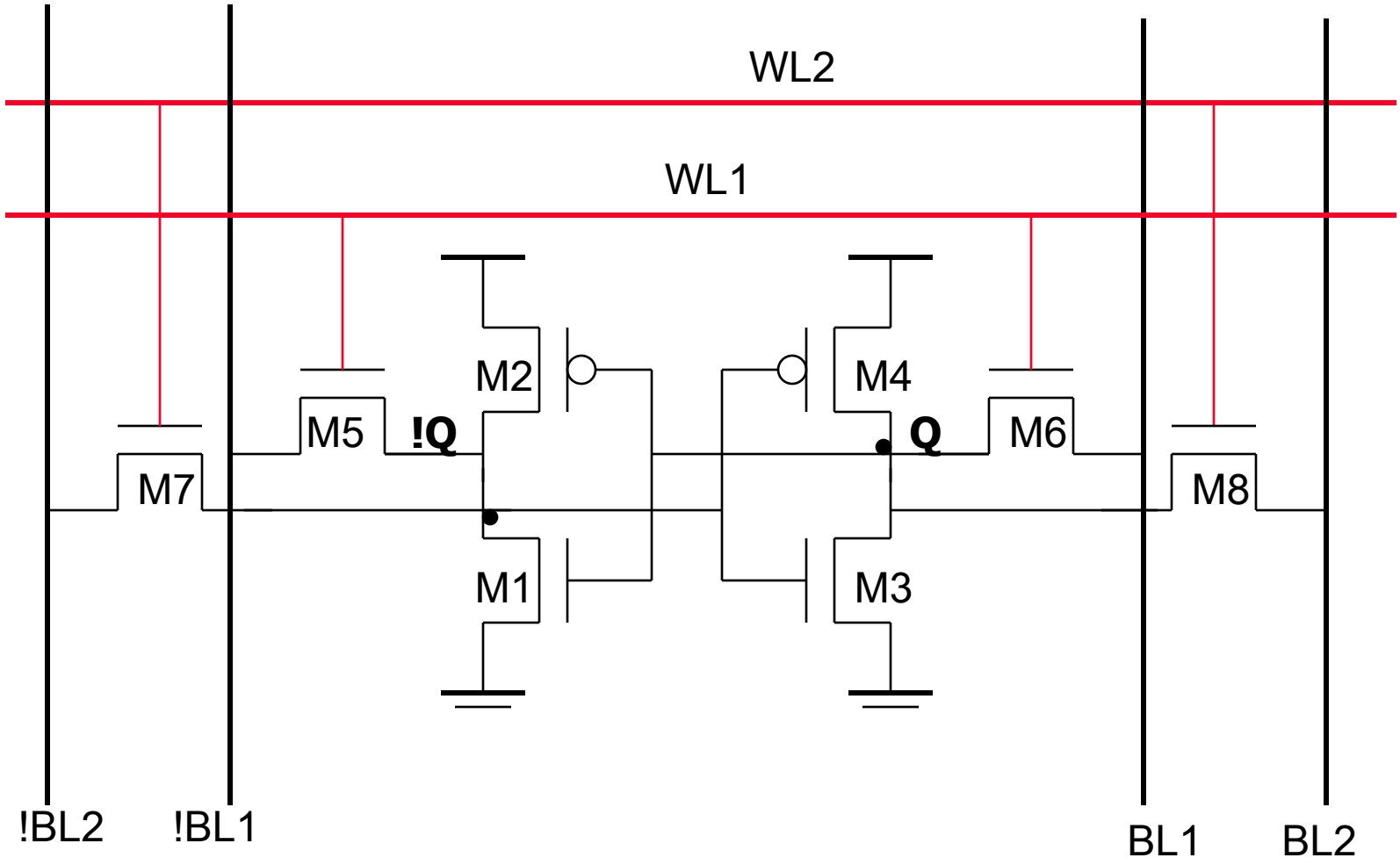
Cell Sizing

- Keeping cell size minimized is critical for large caches
- Minimum sized pull down fets (M1 and M3)
  - Requires minimum width and longer than minimum channel length pass transistors (M5 and M6) to ensure proper CR
  - But sizing of the pass transistors increases capacitive load on the word lines a*nd* limits the current discharged on the bit lines both of which can adversely affect the speed of the read cycle
- Minimum width and length pass transistors
  - Boost the width of the pull downs (M1 and M3)
  - Reduces the loading on the word lines and increases the storage capacitance in the cell – both are good! – but cell size may be slightly larger

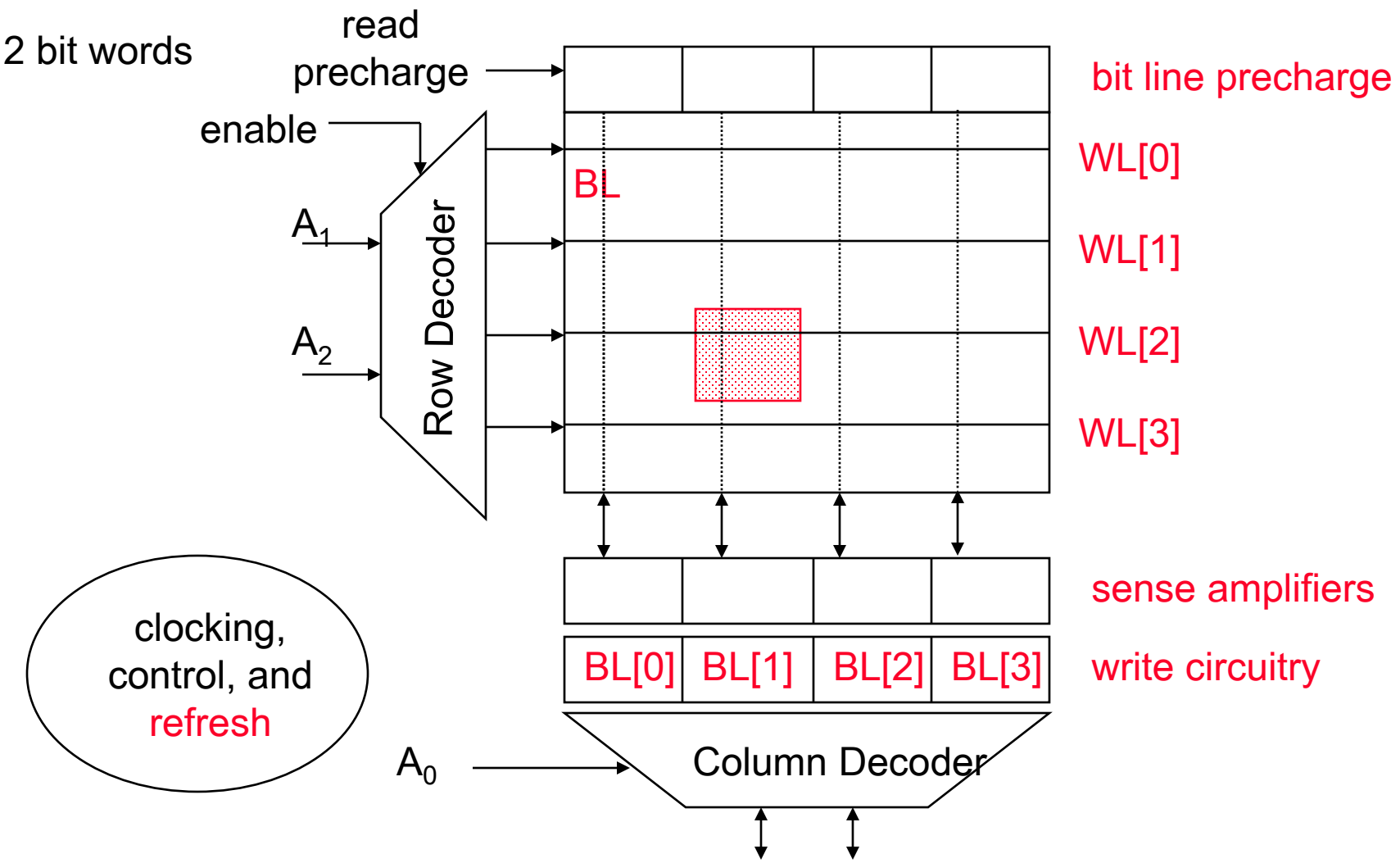
6T-SRAM Layout



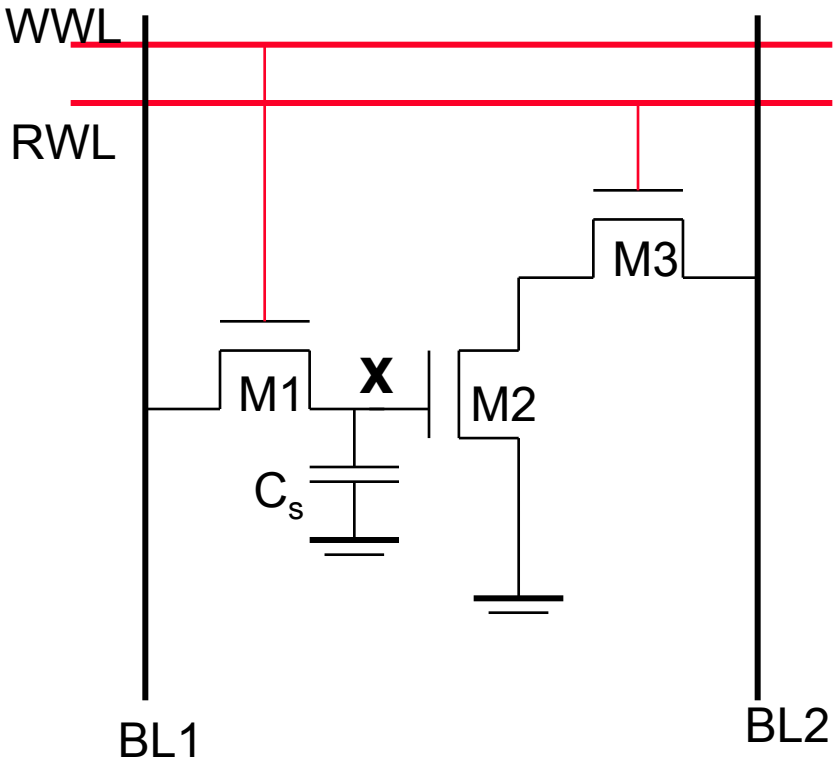
Multiple Read/Write Port Cell

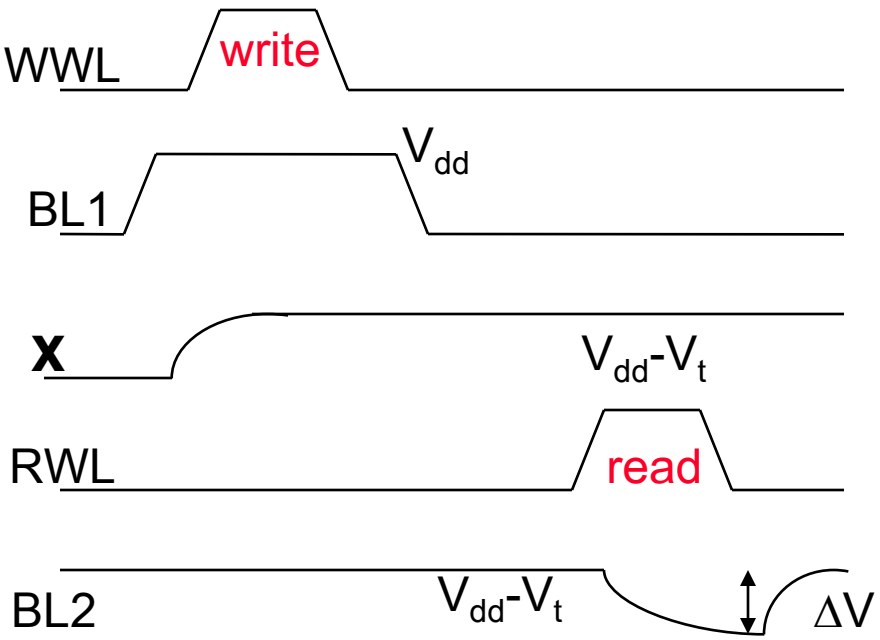


4x4 DRAM Memory



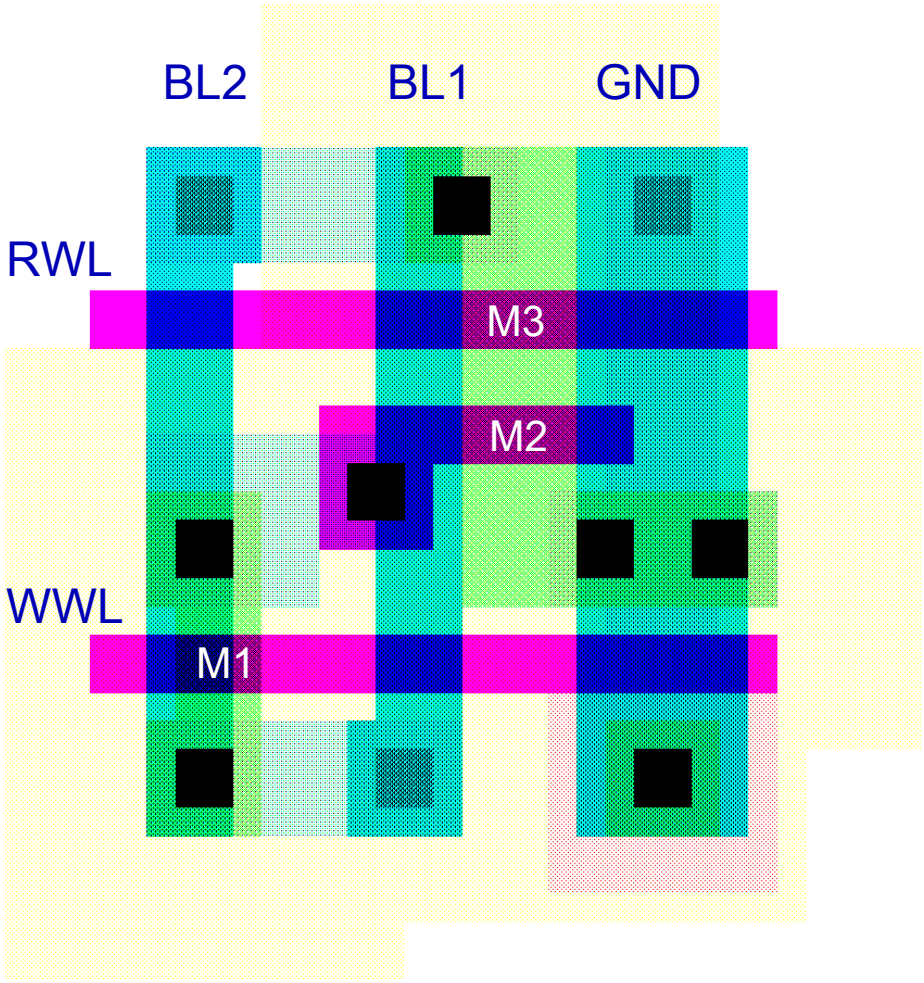
3-Transistor DRAM Cell



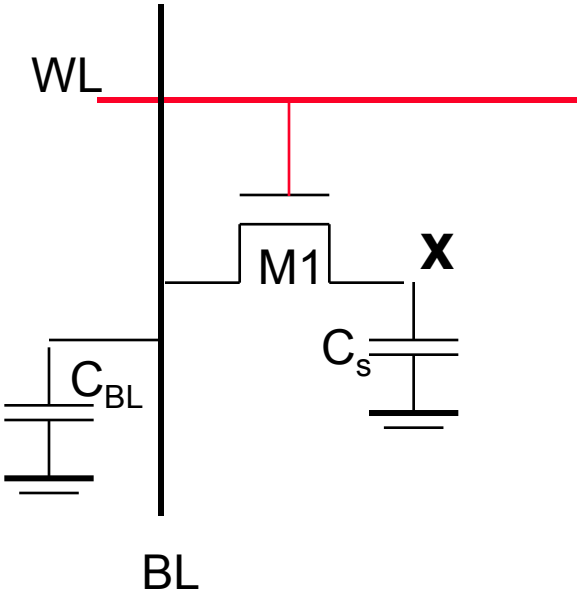


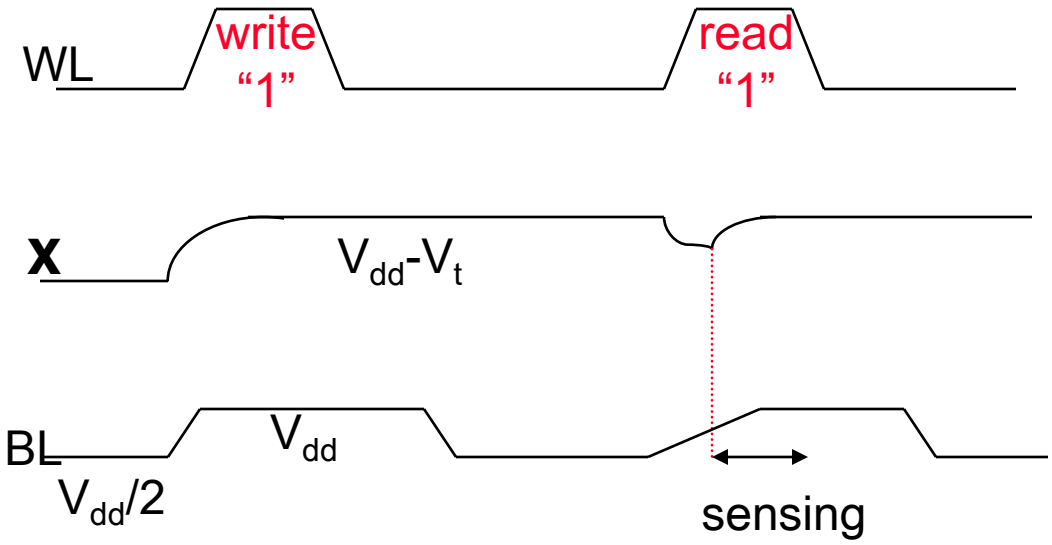
No constraints on device sizes (ratioless)
Reads are non-destructive
Value stored at node X when writing a "1" is V_{WWL} - V_{tn}

3T-DRAM Layout



1-Transistor DRAM Cell

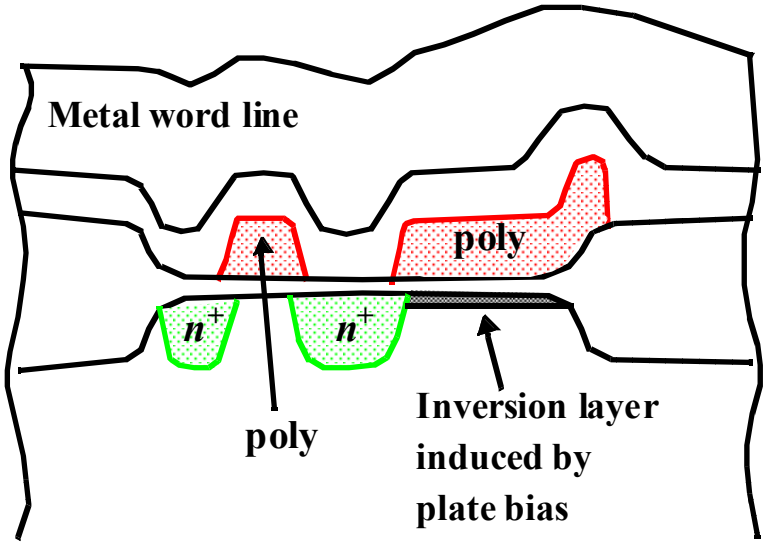




Write: C_s is charged (or discharged) by asserting WL and BL
Read: Charge redistribution occurs between C_{BL} and C_s

Read is destructive, so must refresh after read

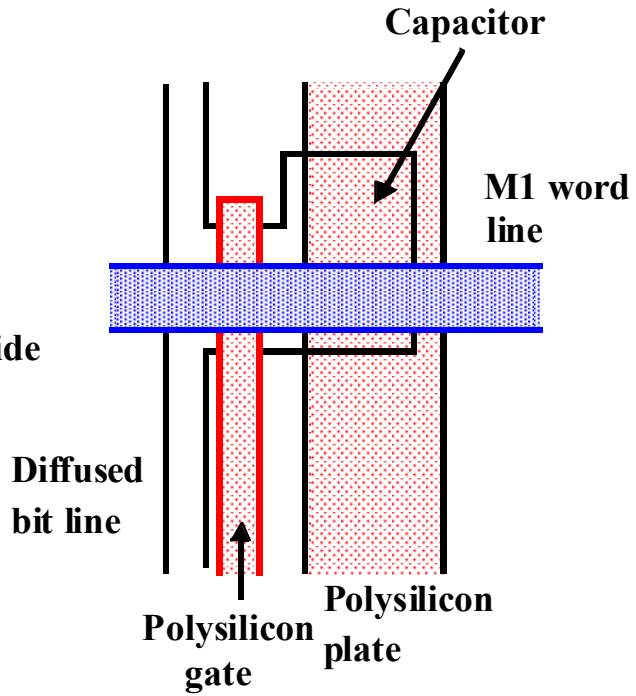
1-T DRAM Cell



SiO_2

Field Oxide

(a) Cross-section



(b) Layout

Used Polysilicon-Diffusion Capacitance

Expensive in Area

DRAM Cell Observations

- DRAM memory cells are single ended (complicates the design of the sense amp)
- 1T cell requires a sense amp for each bit line due to charge redistribution read
- 1T cell read is destructive; refresh must follow to restore data
- 1T cell requires an extra capacitor that must be explicitly included in the design
- A threshold voltage is lost when writing a 1 (can be circumvented by bootstrapping the word lines to a higher value than V_{dd})

Next Lecture and Reminders

- Next lecture
  - Peripheral memory circuits
    - Reading assignment – Rabaey, et al, 12.3
- Reminders
  - Project final reports due December 5th
  - Final grading negotiations/correction (except for the final exam) must be concluded by December 10th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in 118 and 121 Thomas