CSE477
VLSI Digital Circuits
Fall 2002

Lecture 09: Resistance

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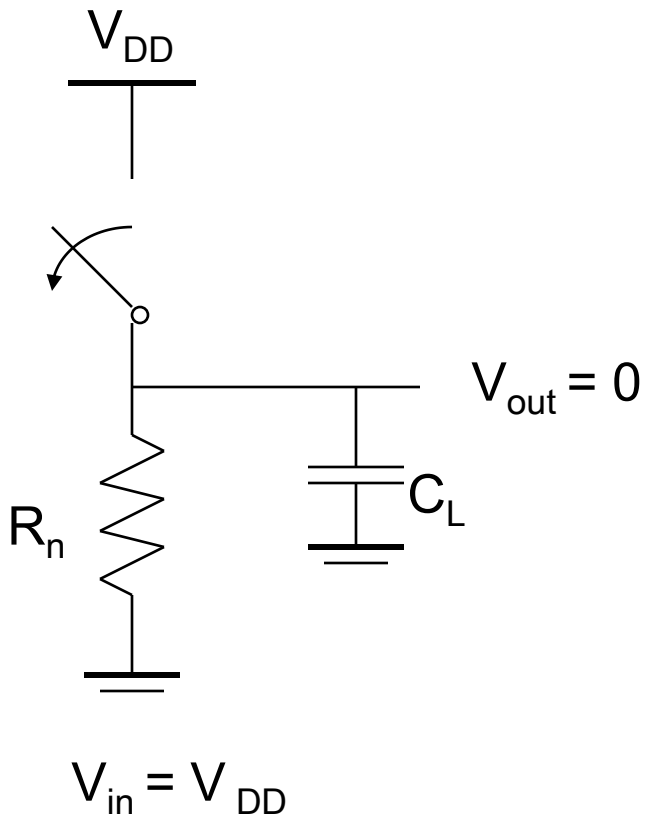
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

CMOS Inverter: Dynamic

- Transient, or dynamic, response determines the maximum speed at which a device can be operated.

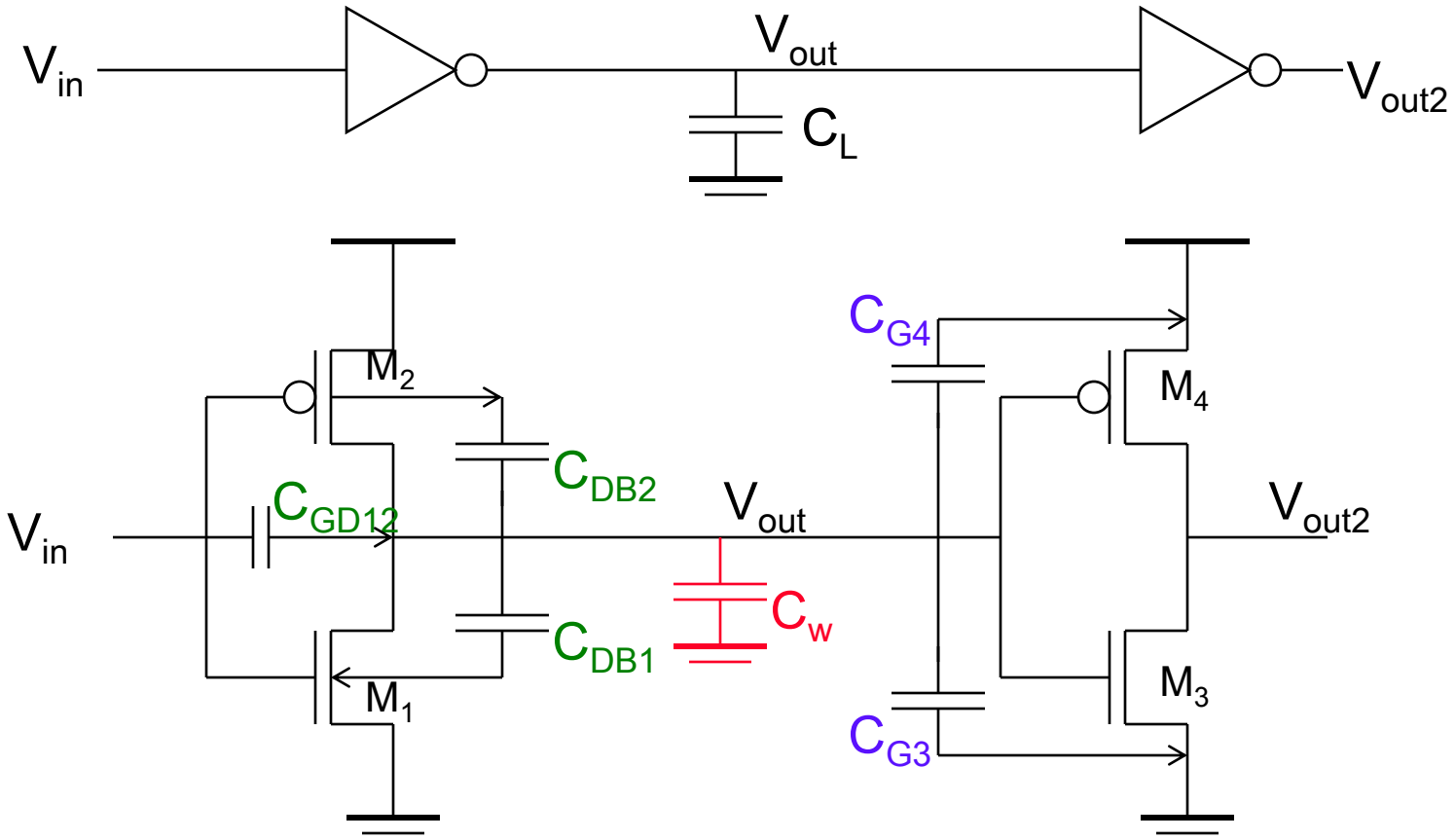


Last lecture's focus

$t_{pHL} = f(R_n, C_L)$

Today's focus

Review: Sources of Capacitance



intrinsic MOS transistor capacitances

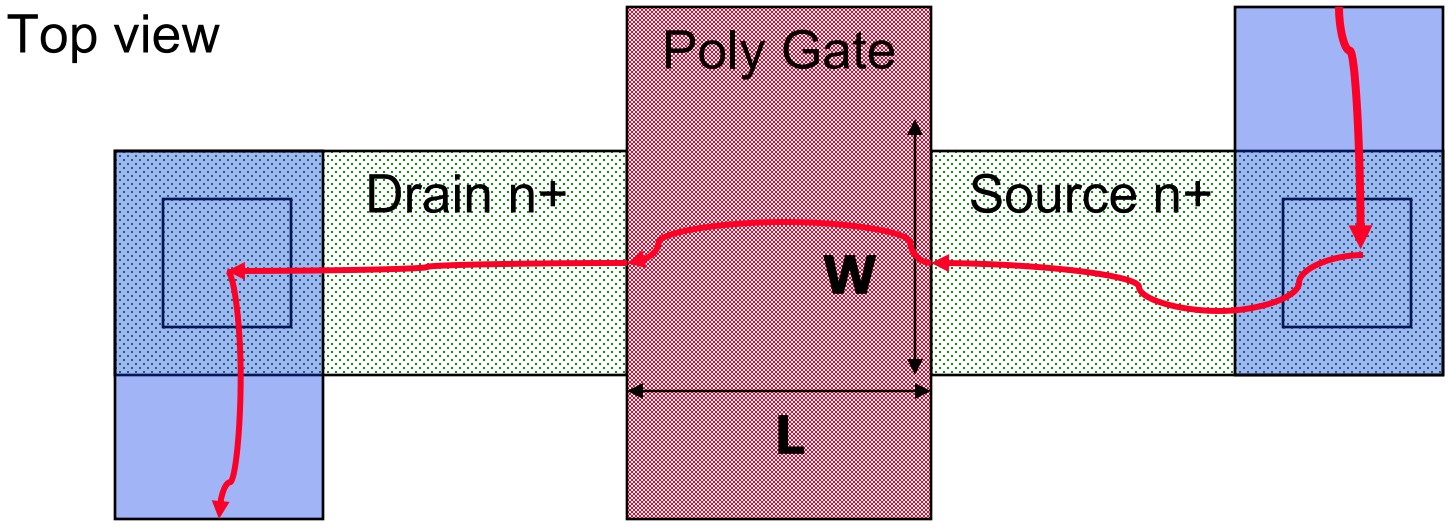
extrinsic MOS transistor (fanout) capacitances

wiring (interconnect) capacitance

Review: Components of C_L (0.25 μm)

C Term	Expression	Value (fF) H→L	Value (fF) L→H
C_{GD1}	$2\,C_{on}\,W_n$	0.23	0.23
C_{GD2}	$2\,C_{op}\,W_p$	0.61	0.61
C_{DB1}	$K_{eqbpn}AD_nC_j + K_{eqswn}PD_nC_{jsw}$	0.66	0.90
C_{DB2}	$K_{eqbpp}AD_pC_j + K_{eqswp}PD_pC_{jsw}$	1.5	1.15
C_{G3}	$(2\,C_{on})W_n + C_{ox}W_nL_n$	0.76	0.76
C_{G4}	$(2\,C_{op})W_p + C_{ox}W_pL_p$	2.28	2.28
C_w	from extraction	0.12	0.12
C_L	Σ	6.1	6.0

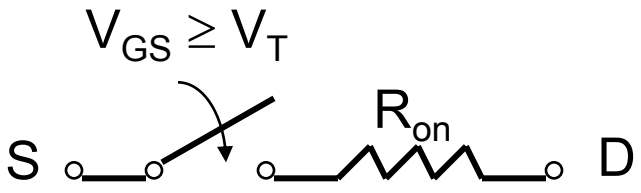
Sources of Resistance



- MOS structure resistance - R_{on}
- Source and drain resistance
- Contact (via) resistance
- Wiring resistance

MOS Structure Resistance

- The simplest model assumes the transistor is a switch with an infinite "off" resistance and a finite "on" resistance R_{on}



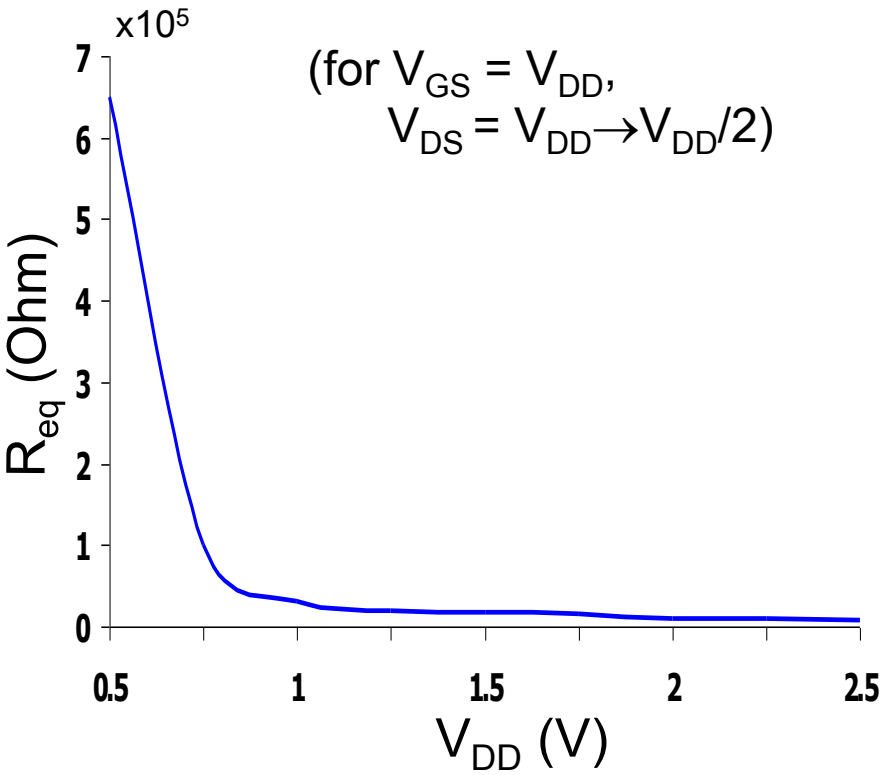
- However R_{on} is nonlinear, so use instead the average value of the resistances, R_{eq}, at the end-points of the transition (V_{DD} and $V_{DD}/2$)

$$R_{eq} = \hat{e} (R_{on}(t_1) + R_{on}(t_2))$$

$$R_{eq} = \text{ì } V_{DD}/I_{DSAT} (1 - 5/6 \ \lambda V_{DD})$$

Equivalent MOS Structure Resistance

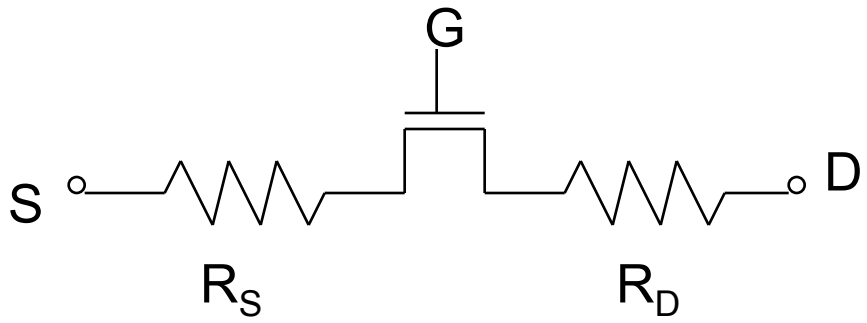
- The on resistance is inversely proportional to W/L. Doubling W halves R_{eq}
- For $V_{DD} >> V_T + V_{DSAT}/2$, R_{eq} is independent of V_{DD} (see plot). Only a minor improvement in R_{eq} occurs when V_{DD} is increased (due to channel length modulation)
- Once the supply voltage approaches V_T, R_{eq} increases dramatically



V_{DD}(V)	1	1.5	2	2.5
NMOS(kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

R_{eq} (for W/L = 1), for larger devices divide R_{eq} by W/L

Source and Drain Resistance



$$R_{S,D} = (L_{S,D}/W)R_{\square}$$

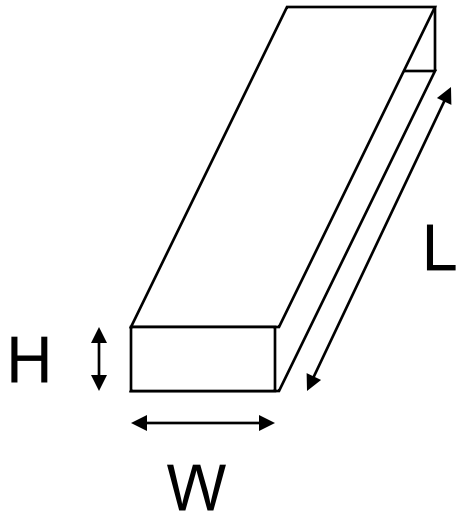
where $L_{S,D}$ is the length of the source or drain diffusion
$R_{\square}$ is the sheet resistance of the source or drain diffusion (20 to 100 Ω/□)

- More pronounced with scaling since junctions are shallower
- With silicidation $R_{\square}$ is reduced to the range 1 to 4 Ω/□

Contact Resistance

- Transitions between routing layers (contacts through via's) add extra resistance to a wire
  - keep signals wires on a single layer whenever possible
  - avoid excess contacts
  - reduce contact resistance by making vias larger (beware of current crowding that puts a practical limit on the size of vias) or by using multiple minimum-size vias to make the contact
- Typical contact resistances, R_C, (minimum-size)
  - 5 to 20 Ω for metal or poly to n+, p+ diffusion and metal to poly
  - 1 to 5 Ω for metal to metal contacts
- More pronounced with scaling since contact openings are smaller

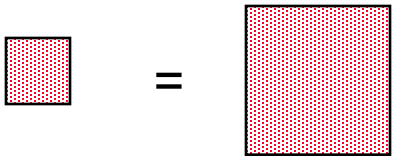
Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho L}{H W}$$

Sheet Resistance $R_{\square}$

$R_{1\square} = R_{2\square}$



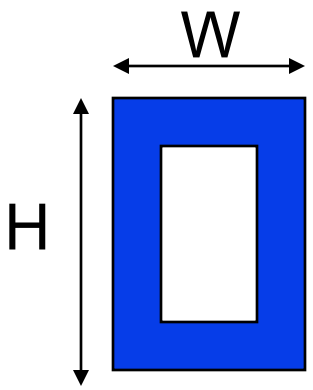
Material	ρ(Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Material	Sheet Res. (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

Irwin&Vijay, PSU, 2002

Skin Effect

- At high frequency, currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially with depth into the wire



$\delta = \sqrt{(\rho/(\pi f \mu))}$

where f is frequency

$\mu = 4\pi \times 10^{-7}$ H/m

$\delta = 2.6\ \mu m$ for Al at 1 GHz

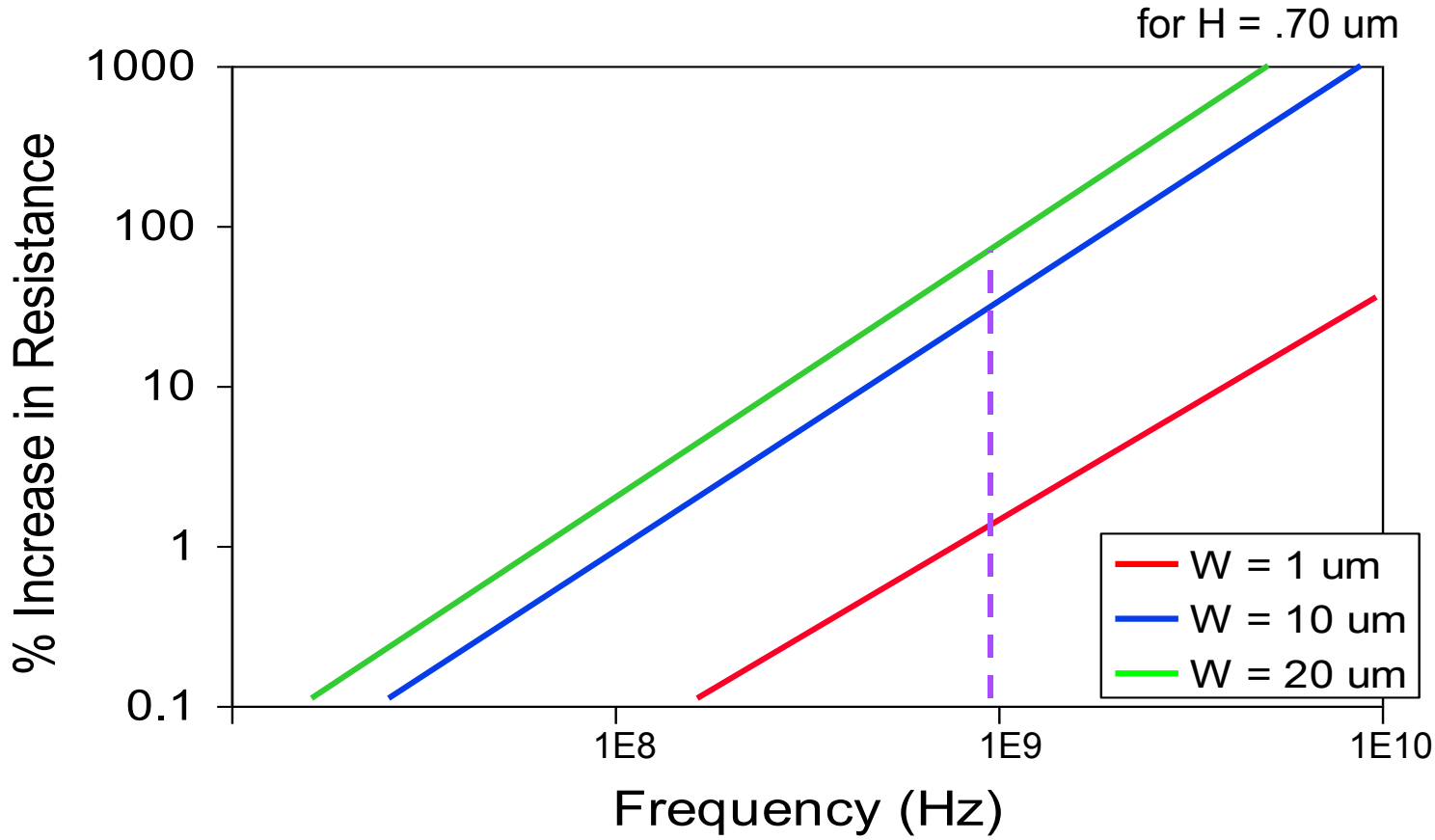
so the overall cross section is ~ $2(W+H)\delta$

- The onset of skin effect is at f_s - where the skin depth is equal to half the largest dimension of the wire.

$$f_s = 4\ \rho\ /\ (\pi\ \mu\ (\max(W,H))^2)$$

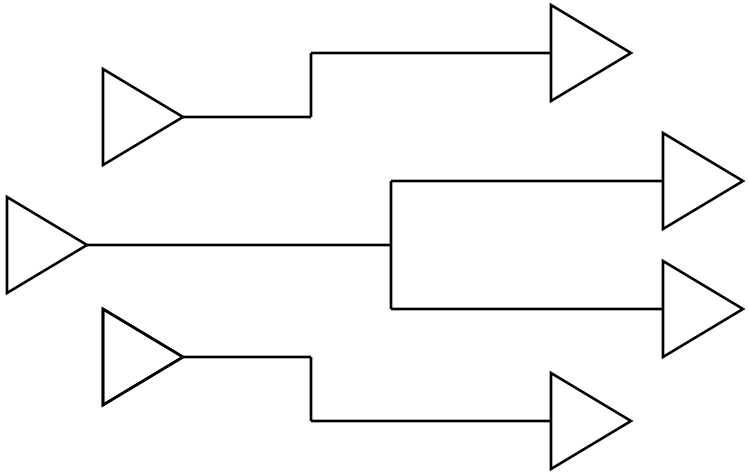
- An issue for high frequency, wide (tall) wires (i.e., clocks!)

Skin Effect for Different W's



- A 30% increase in resistance is observe for 20 μm Al wires at 1 GHz (versus only a 1% increase for 1 μm wires)

The Wire



transmitters

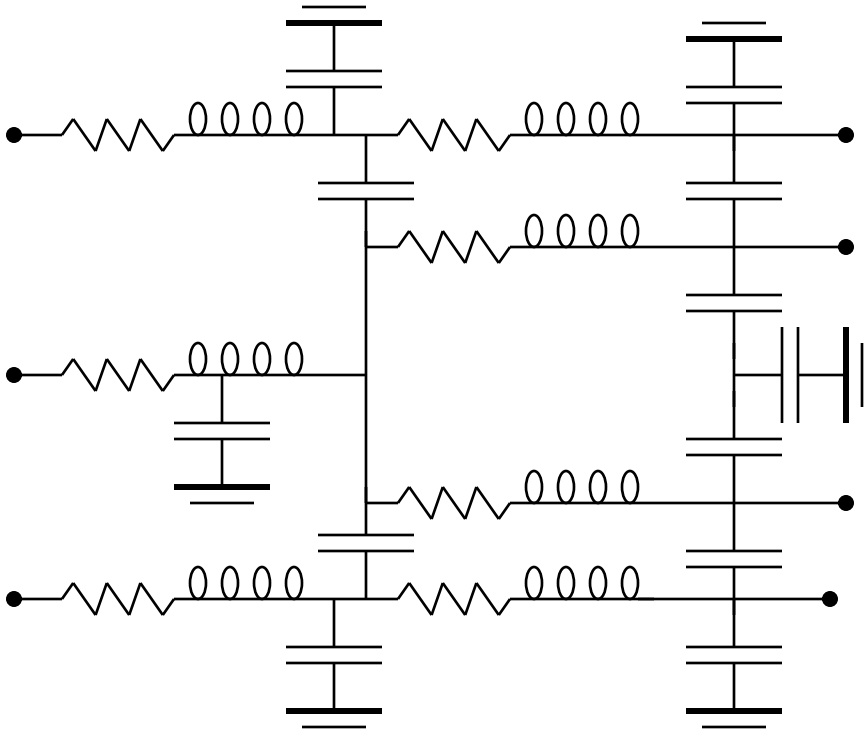
receivers

schematic

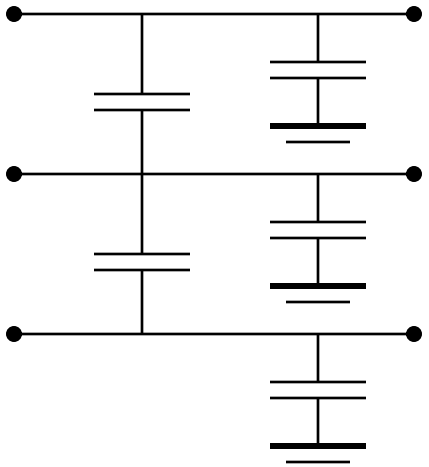
physical

Wire Models

- Interconnect parasitics (capacitance, resistance, and inductance)
  - reduce reliability
  - affect performance and power consumption



All-inclusive (C,R,I) model

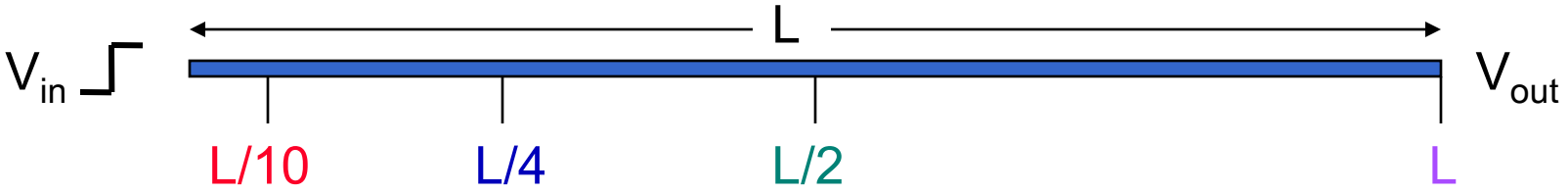


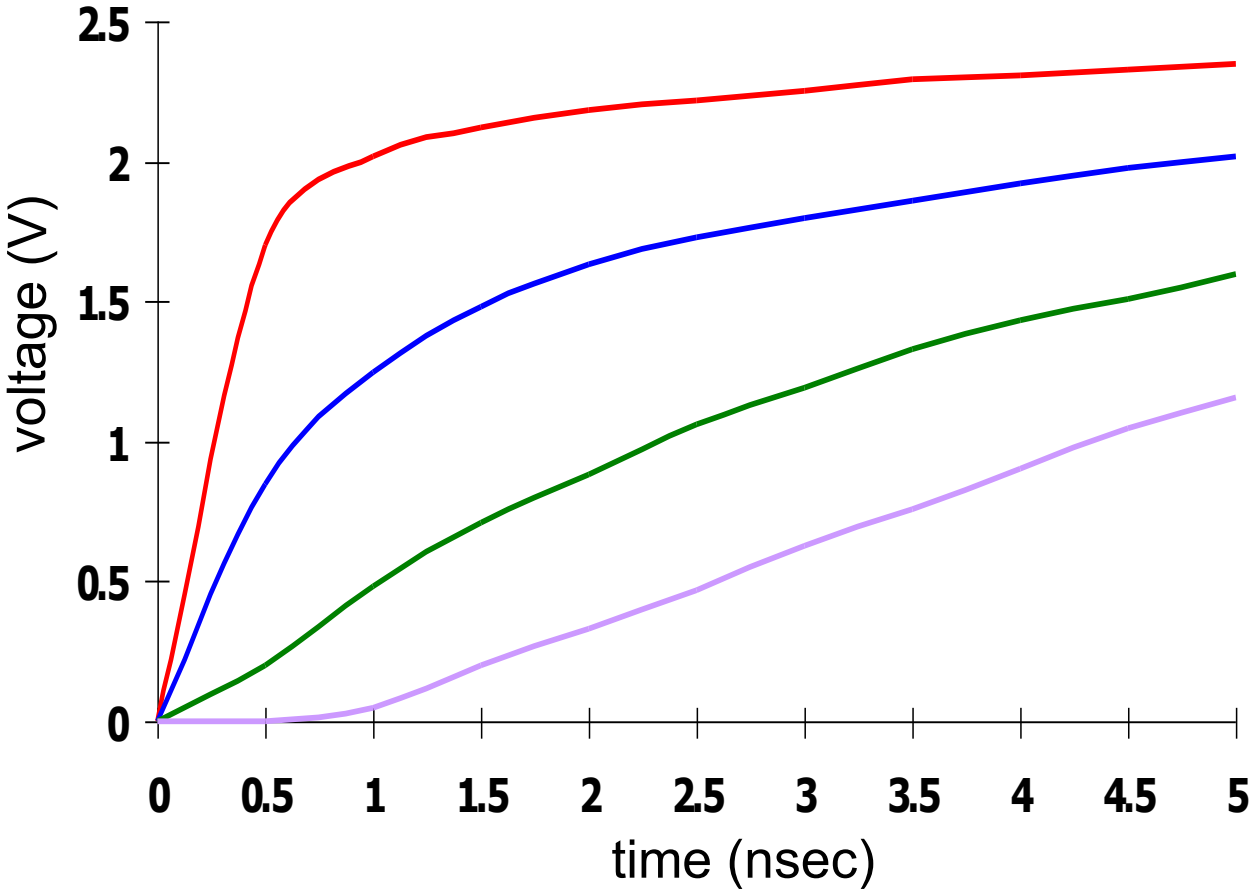
Capacitance-only

Parasitic Simplifications

- Inductive effects can be ignored
  - if the resistance of the wire is substantial enough (as is the case for long Al wires with small cross section)
  - if the rise and fall times of the applied signals are slow enough
- When the wire is short, or the cross-section is large, or the interconnect material has low resistivity, a capacitance only model can be used
- When the separation between neighboring wires is large, or when the wires run together for only a short distance, interwire capacitance can be ignored and all the parasitic capacitance can be modeled as capacitance to ground

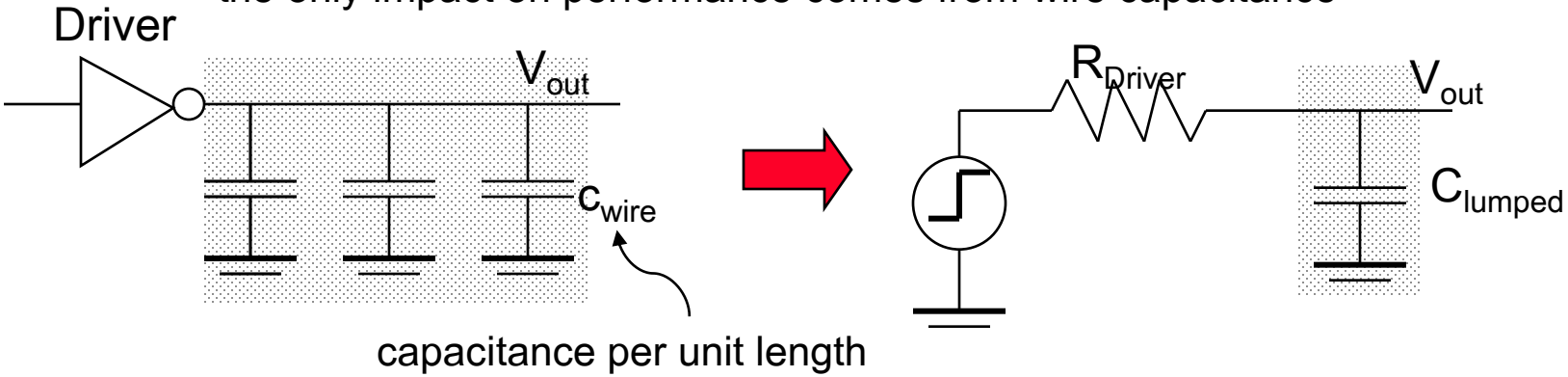
Simulated Wire Delays





Wire Delay Models

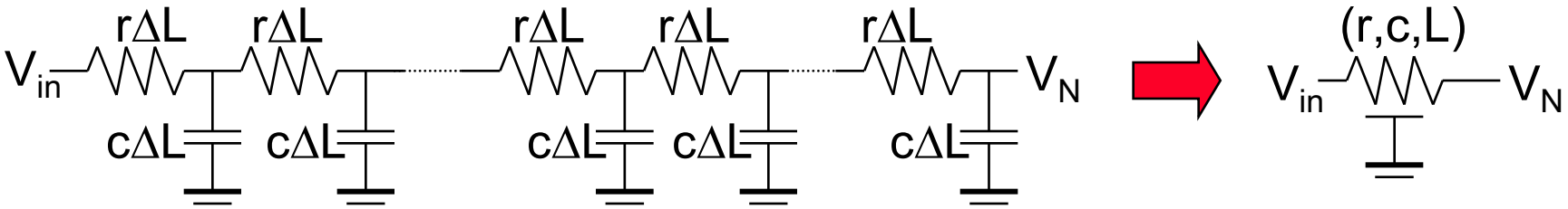
- Ideal wire
  - same voltage is present at every segment of the wire at every point in time - at equi-potential
  - only holds for *very short* wires, i.e., interconnects between *very* nearest neighbor gates
- Lumped C model
  - when only a single parasitic component (C, R, or L) is dominant the different fractions are lumped into a single circuit element
    - When the resistive component is small and the switching frequency is low to medium, can consider only C; the wire itself does not introduce any delay; the only impact on performance comes from wire capacitance



  - good for short wires; pessimistic and inaccurate for long wires

Wire Delay Models, con't

- Lumped RC model
  - total wire resistance is lumped into a single R and total capacitance into a single C
  - good for short wires; pessimistic and inaccurate for long wires
- Distributed RC model
  - circuit parasitics are distributed along the length, L, of the wire
    - c and r are the capacitance and resistance per unit length

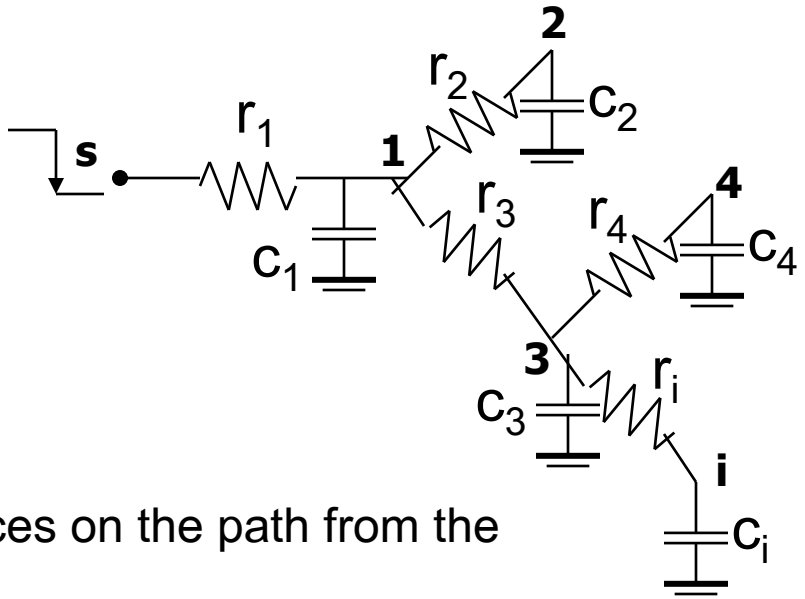


  - Delay is determined using the Elmore delay equation

$$\tau_{Di} = \sum_{k=1}^{N} c_k r_{ik}$$

RC Tree Definitions

- RC tree characteristics
  - A unique resistive path exists between the source node and any node of the network
    - Single input (source) node, s
    - All capacitors are between a node and GND
    - No resistive loops



  - Path resistance (sum of the resistances on the path from the input node to node *i*)

$$r_{ii} = \sum_{j=1}^{i} r_j \Rightarrow (r_j \in [\text{path}(s \rightarrow i)]$$

  - Shared path resistance (resistance shared along the paths from the input node to nodes *i* and *k*)

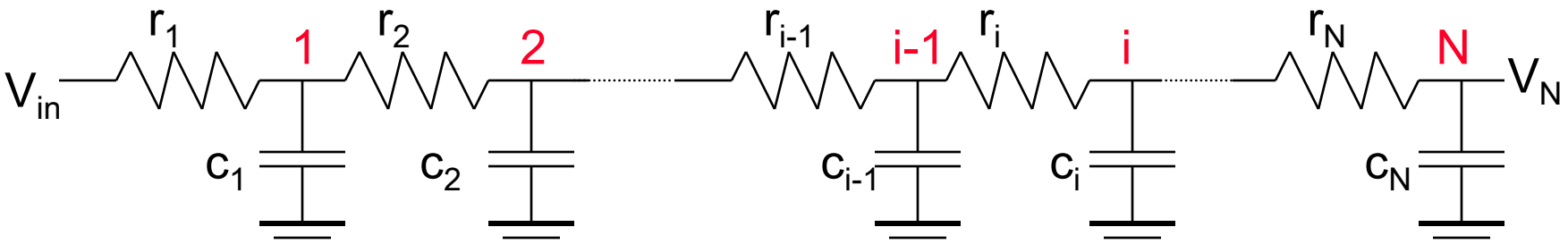
$$r_{ik} = \sum_{j=1}^{N} r_j \Rightarrow (r_j \in [\text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k)])$$

- A typical wire is a chain network with (simplified) Elmore delay of

$$\tau_{DN} = \sum_{i=1}^{N} c_i r_{ii}$$

Chain Network Elmore Delay

$\tau_{D1}=c_1r_1$ $\tau_{D2}=c_1r_1 + c_2(r_1+r_2)$



$\tau_{Di}=c_1r_1+ c_2(r_1+r_2)+\ldots+c_i(r_1+r_2+\ldots+r_i)$

Elmore delay equation $\tau_{DN} = \sum c_i r_{ii} = \sum^{N} c_i \sum^{i} r_j$

$\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\ldots+ ic_ir_{eq}$

Elmore Delay Models Uses

- Modeling the delay of a wire
- Modeling the delay of a series of pass transistors
- Modeling the delay of a pull-up and pull-down networks

Distributed RC Model for Simple Wires

- A length L RC wire can be modeled by N segments of length L/N
  - The resistance and capacitance of each segment are given by r L/N and c L/N

$$\tau_{DN} = (L/N)^2(cr+2cr+\ldots+Ncr) = (crL^2)\,(N(N+1))/(2N^2) = CR((N+1)/(2N))$$

where R (= rL) and C (= cL) are the total lumped resistance and capacitance of the wire

- For large N

$$\tau_{DN} = RC/2 = rcL^2/2$$

  - Delay of a wire is a quadratic function of its length, L
  - The delay is 1/2 of that predicted (by the lumped model)

Step Response Points

Voltage Range	Lumped RC	Distributed RC
$0 \rightarrow 50\%$ (t_p)	0.69 RC	0.38 RC
$0 \rightarrow 63\%$ (τ)	RC	0.5 RC
$10\% \rightarrow 90\%$ (t_r)	2.2 RC	0.9 RC
$0 \rightarrow 90\%$	2.3 RC	1.0 RC

Time to reach the 50% point is $t = \ln(2)\tau = 0.69\tau$

Time to reach the 90% point is $t = \ln(9)\tau = 2.2\tau$

- Example: Consider a Al1 wire 10 cm long and 1 μm wide
  - Using a lumped C only model with a source resistance (R_{Driver}) of 10 kΩ and a total lumped capacitance (C_{lumped}) of 11 pF

$$t_{50\%} = 0.69 \times 10\ k\Omega \times 11pF = 76\ ns$$

$$t_{90\%} = 2.2 \times 10\ k\Omega \times 11pF = 242\ ns$$

  - Using a distributed RC model with c = 110 aF/μm and r = 0.075 Ω/μm

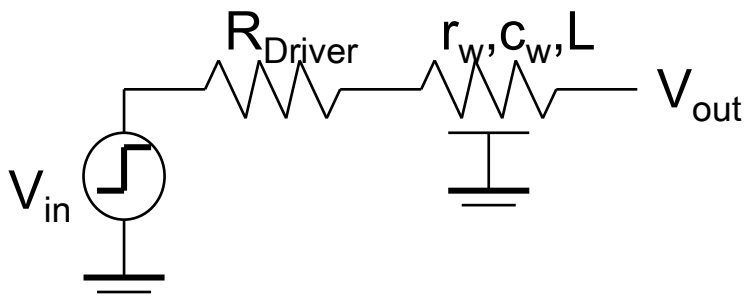
$$t_{50\%} = 0.38 \times (0.075\ \Omega/\mu m) \times (110\ aF/\mu m) \times (10^5\ \mu m)^2 = 31.4\ ns$$

$$t_{90\%} = 0.9 \times (0.075\ \Omega/\mu m) \times (110\ aF/\mu m) \times (10^5\ \mu m)^2 = 74.25\ ns$$

Poly: $t_{50\%} = 0.38 \times (150\ \Omega/\mu m) \times (88+2\times54\ aF/\mu m) \times (10^5\ \mu m)^2 = 112\ \mu s$

Al5: $t_{50\%} = 0.38 \times (0.0375\ \Omega/\mu m) \times (5.2+2\times12\ aF/\mu m) \times (10^5\ \mu m)^2 = 4.2\ ns$

Putting It All Together



- Total propagation delay consider driver and wire

$$\tau_D = R_{Driver}C_w + (R_wC_w)/2 = R_{Driver}C_w + 0.5r_wc_wL^2$$

and $t_p = 0.69\ R_{Driver}C_w + 0.38\ R_wC_w$

where $R_w = r_wL$ and $C_w = c_wL$

- The delay introduced by wire resistance becomes dominant when $(R_wC_w)/2 \geq R_{Driver}\ C_W$ (when $L \geq 2R_{Driver}/R_w$)
  - For an R_{Driver} = 1 kΩ driving an 1 μm wide Al1 wire, L_{crit} is 2.67 cm

Design Rules of Thumb

- rc delays should be considered when $t_{pRC} > t_{pgate}$ of the driving gate

$$L_{crit} > \sqrt{(t_{pgate}/0.38rc)}$$

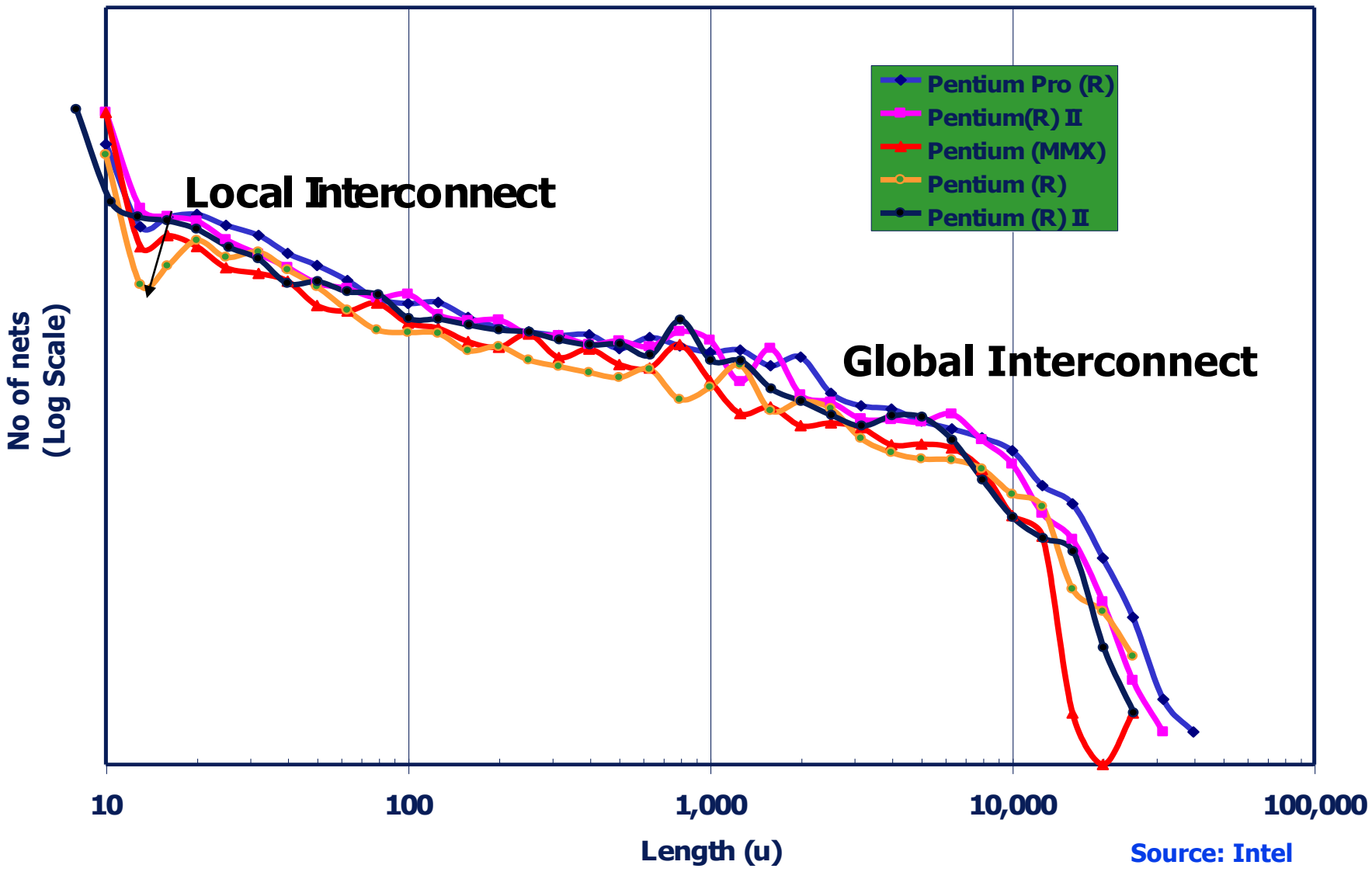
  - actual L_{crit} depends upon the size of the driving gate and the interconnect material

- rc delays should be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

$$t_{rise} < RC$$

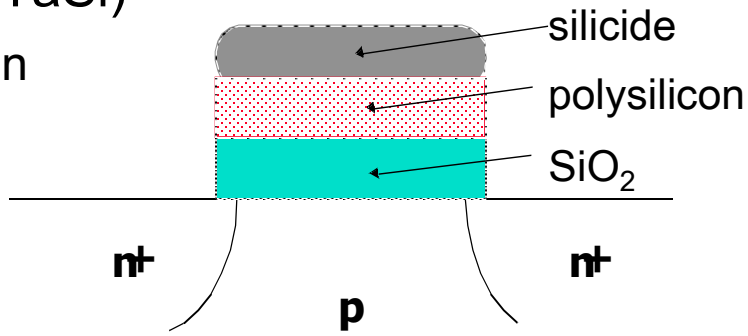
  - when not met, the change in the signal is slower than the propagation delay of the wire so a lumped C model suffices

Nature of Interconnect



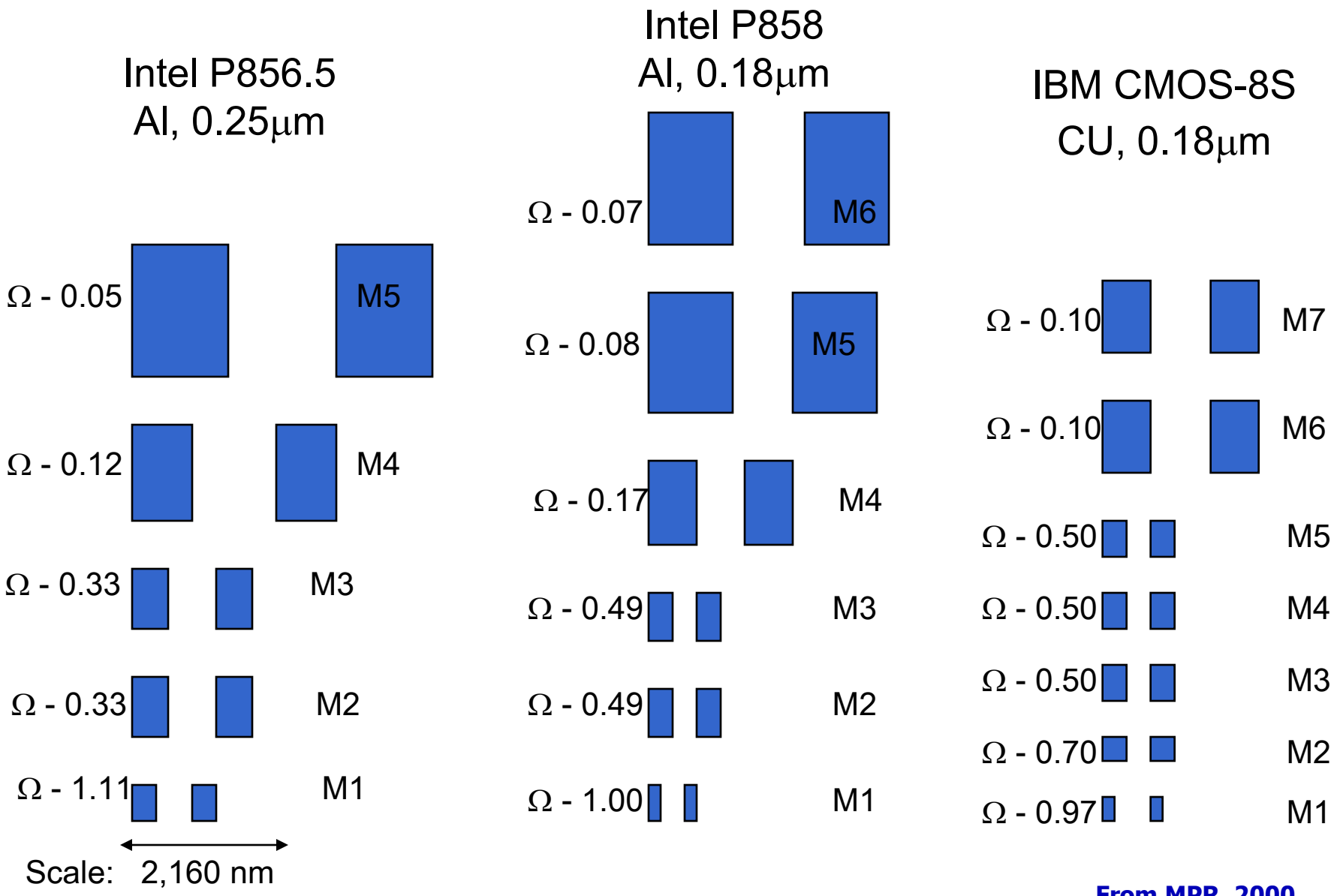
Overcoming Interconnect Resistance

- Selective technology scaling
  - scale W while holding H constant
- Use better interconnect materials
  - lower resistivity materials like copper
    - As processes shrink, wires get shorter (reducing C) but they get closer together (increasing C) and narrower (increasing R). So RC wire delay increases and capacitive coupling gets worse.
    - Copper has about 40% lower resistivity than aluminum, so copper wires can be thinner (reducing C) without increasing R
  - use silicides (WSi_2, $TiSi_2$, $PtSi_2$ and TaSi)
    - Conductivity is 8-10 times better than poly alone



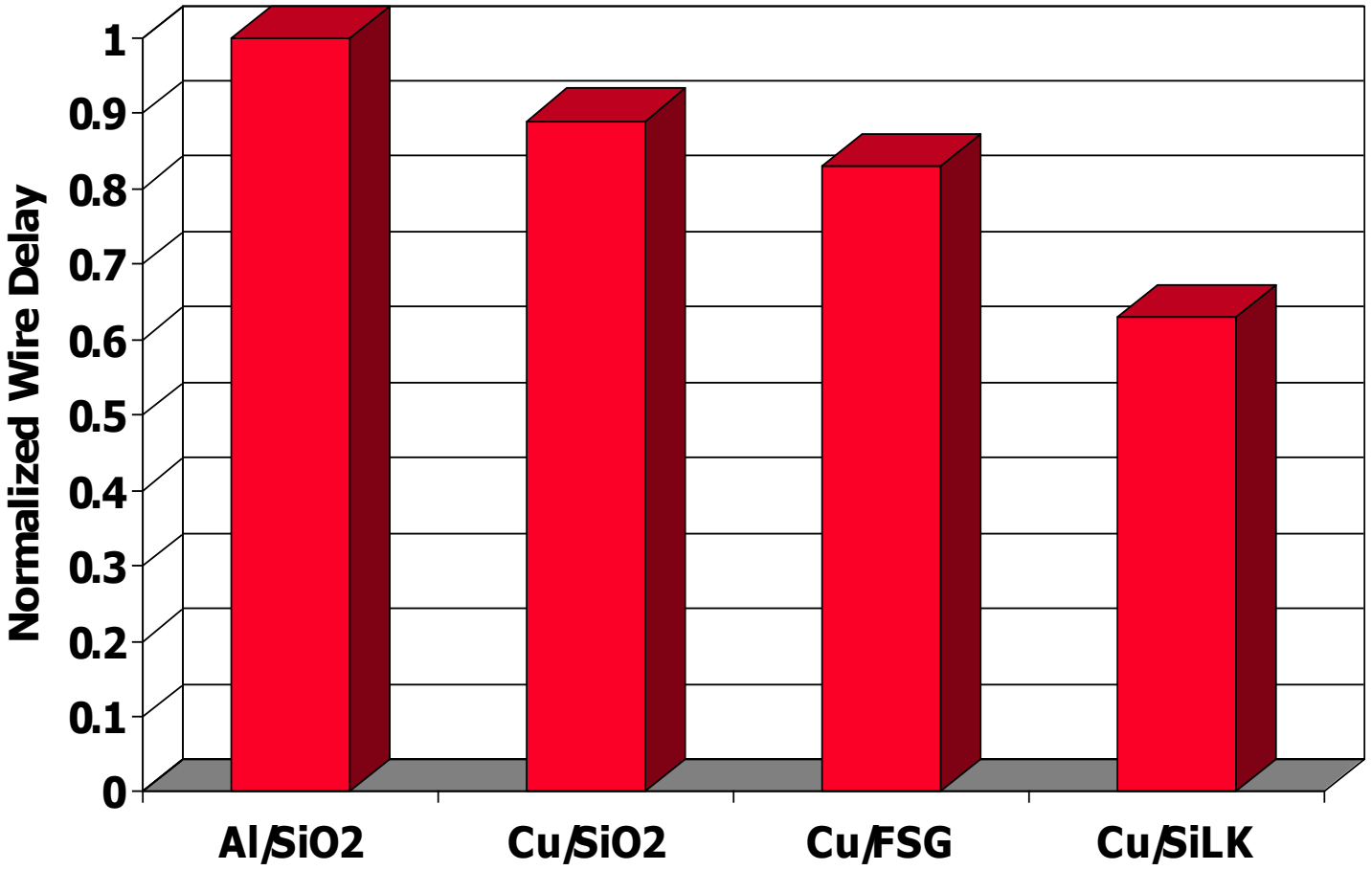
- Use more interconnect layers
  - reduces the average wire length L (but beware of extra contacts)

Wire Spacing Comparisons



From MPR, 2000

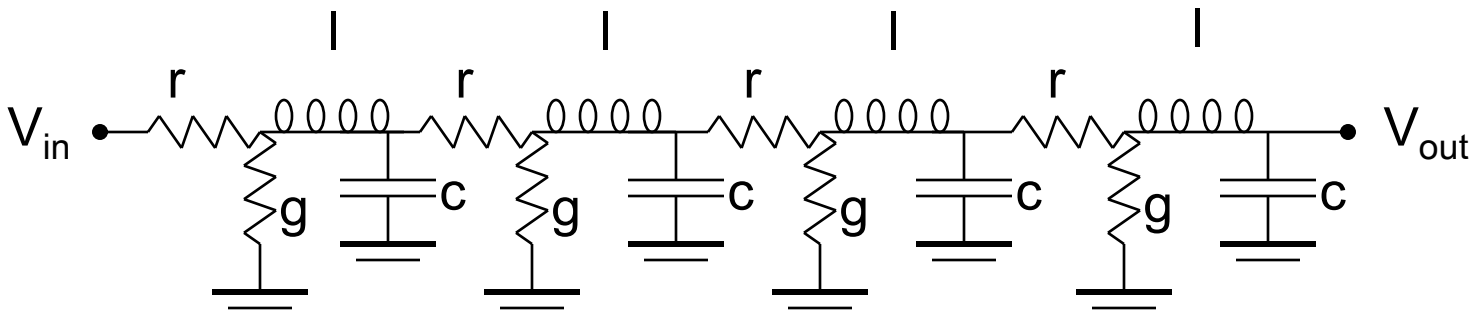
Comparison of Wire Delays



From MPR, 2000

Inductance

- When the rise and fall times of the signal become comparable to the time of flight of the signal waveform across the line, then the inductance of the wire starts to dominate the delay behavior



- Must consider wire transmission line effects
  - Signal propagates over the wire as a wave (rather than diffusing as in rc only models)
    - Signal propagates by alternately transferring energy from capacitive to inductive modes

More Design Rules of Thumb

- Transmission line effects should be considered when the rise or fall time of the input signal (t_r, t_f) is smaller than the time-of-flight of the transmission line (t_{flight})

$$t_r \ (t_f) \ < \ 2.5 \ t_{flight} \ = \ 2.5 \ L/v$$

  - For on-chip wires with a maximum length of 1 cm, we only worry about transmission line effects when $t_r < 150$ ps

- Transmission line effects should only be considered when the total resistance of the wire is limited

$$R < 5 \ Z_0 = 5 \ (V/I)$$

Next Lecture and Reminders

- Next lecture
  - The CMOS inverter dynamic view
    - Reading assignment – Rabaey, et al, 5.4.2-5.4.3
- Reminders
  - Project specifications due next lecture (October 3rd)
  - HW3 due Oct 10th (hand in to TA)
  - Class cancelled on Oct 10th as make up for evening midterm
  - I will be out of town Oct 10th through Oct 15th and Oct 18th through Oct 23rd, so office hours during those periods are cancelled
  - Evening midterm exam scheduled
    - Wednesday, October 16th from 8:15 to 10:15pm in 260 Willard
    - Only one midterm conflict filed for so far