CSE477
VLSI Digital Circuits
Fall 2002

Lecture 23: Semiconductor Memories

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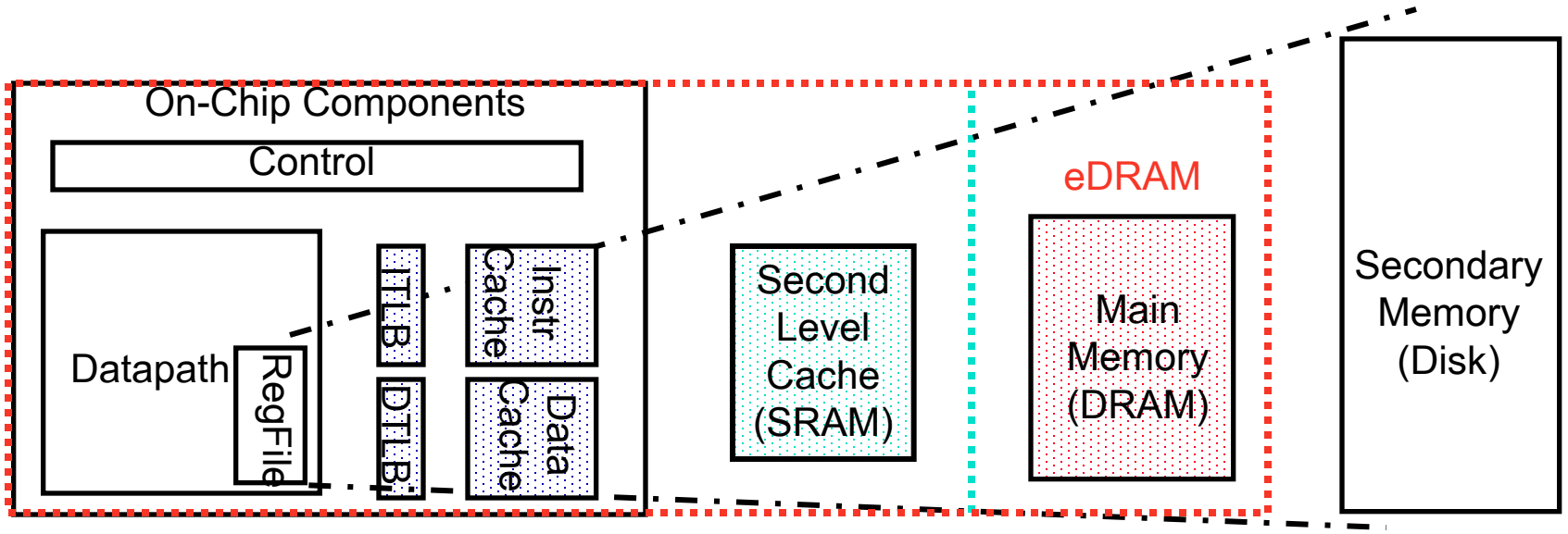
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: Basic Building Blocks

- Datapath
  - Execution units
    - Adder, multiplier, divider, shifter, etc.
  - Register file and pipeline registers
  - Multiplexers, decoders
- Control
  - Finite state machines (PLA, ROM, random logic)
- Interconnect
  - Switches, arbiters, buses
- Memory
  - Caches (SRAMs), TLBs, DRAMs, buffers

A Typical Memory Hierarchy

- By taking advantage of the principle of locality:
  - Present the user with as much memory as is available in the cheapest technology.
  - Provide access at the speed offered by the fastest technology.

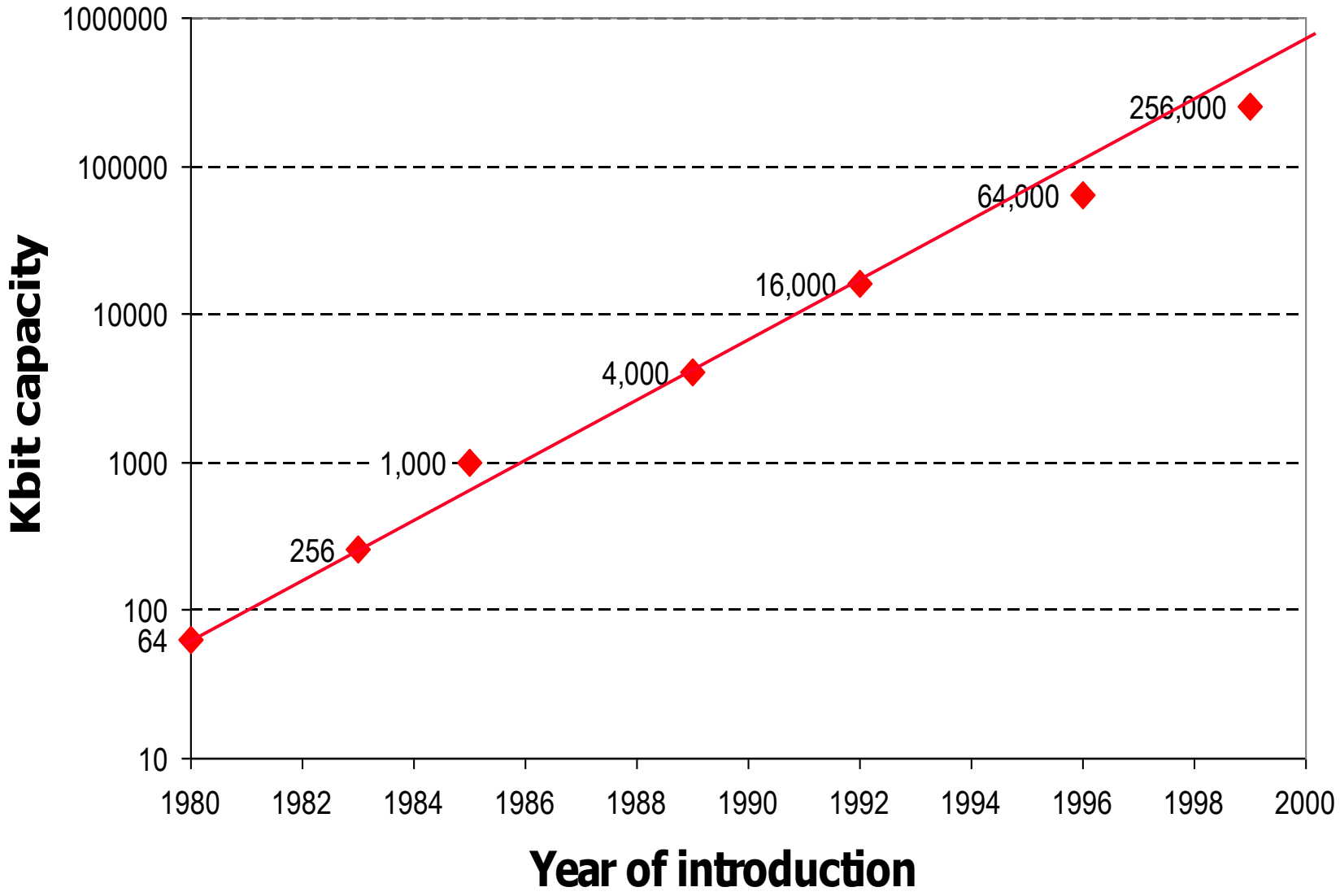


Speed (ns):	.1's	1's	10's	100's	1,000's
Size (bytes):	100's	K's	10K's	M's	T's
Cost:	highest				lowest

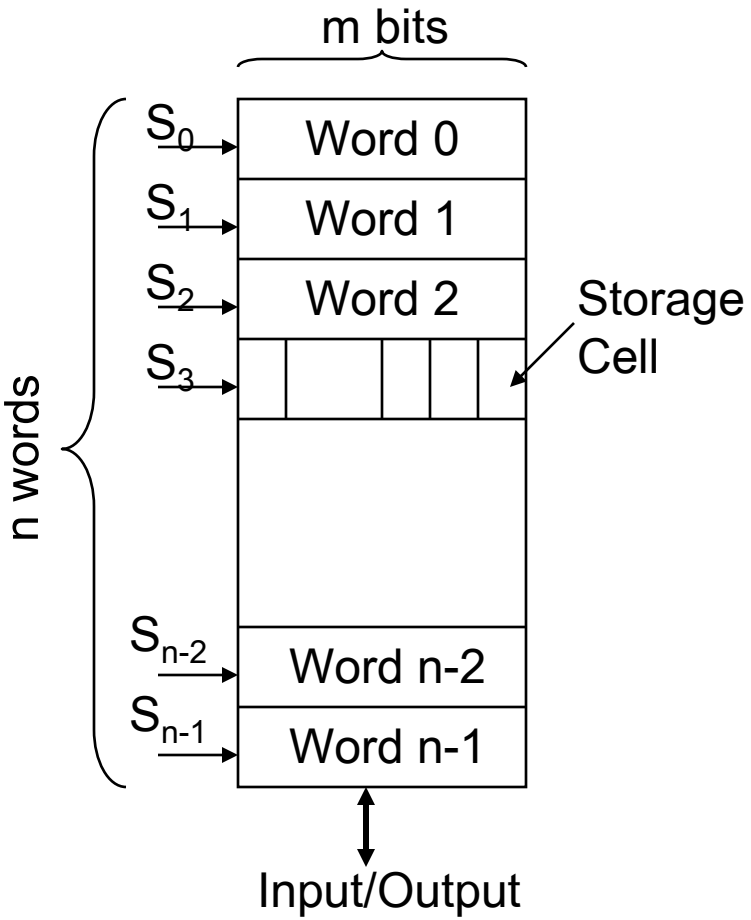
Semiconductor Memories

RWM		NVRWM	ROM
Random Access	Non-Random Access	EPROM	Mask-programmed
SRAM (cache, register file)	FIFO/LIFO	E^2PROM	
DRAM	Shift Register	FLASH	Electrically-programmed (PROM)
	CAM		

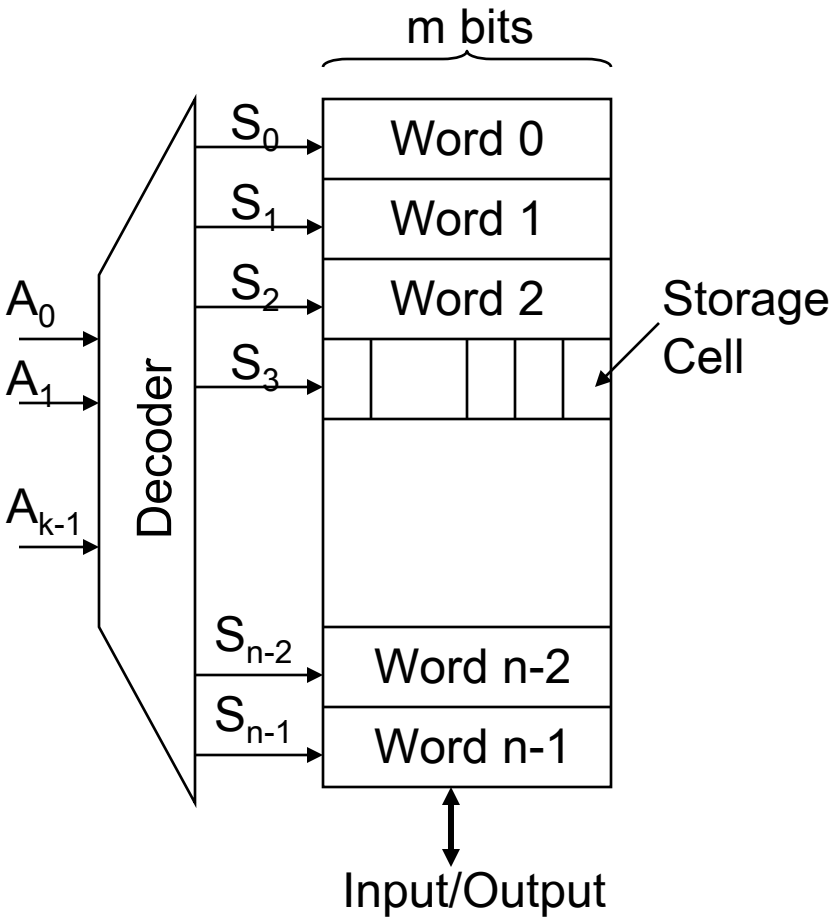
Growth in DRAM Chip Capacity



1D Memory Architecture



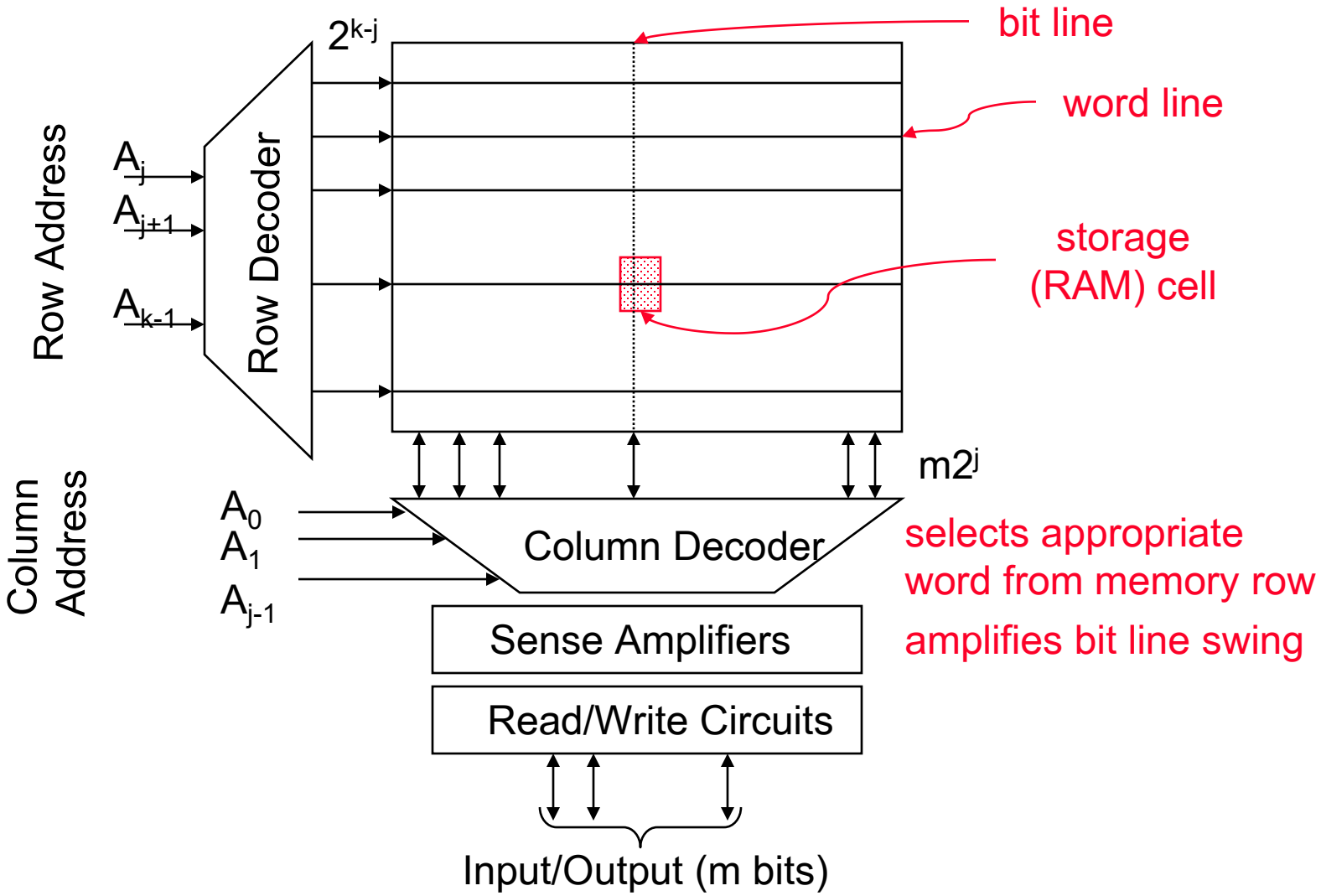
n words → n select signals



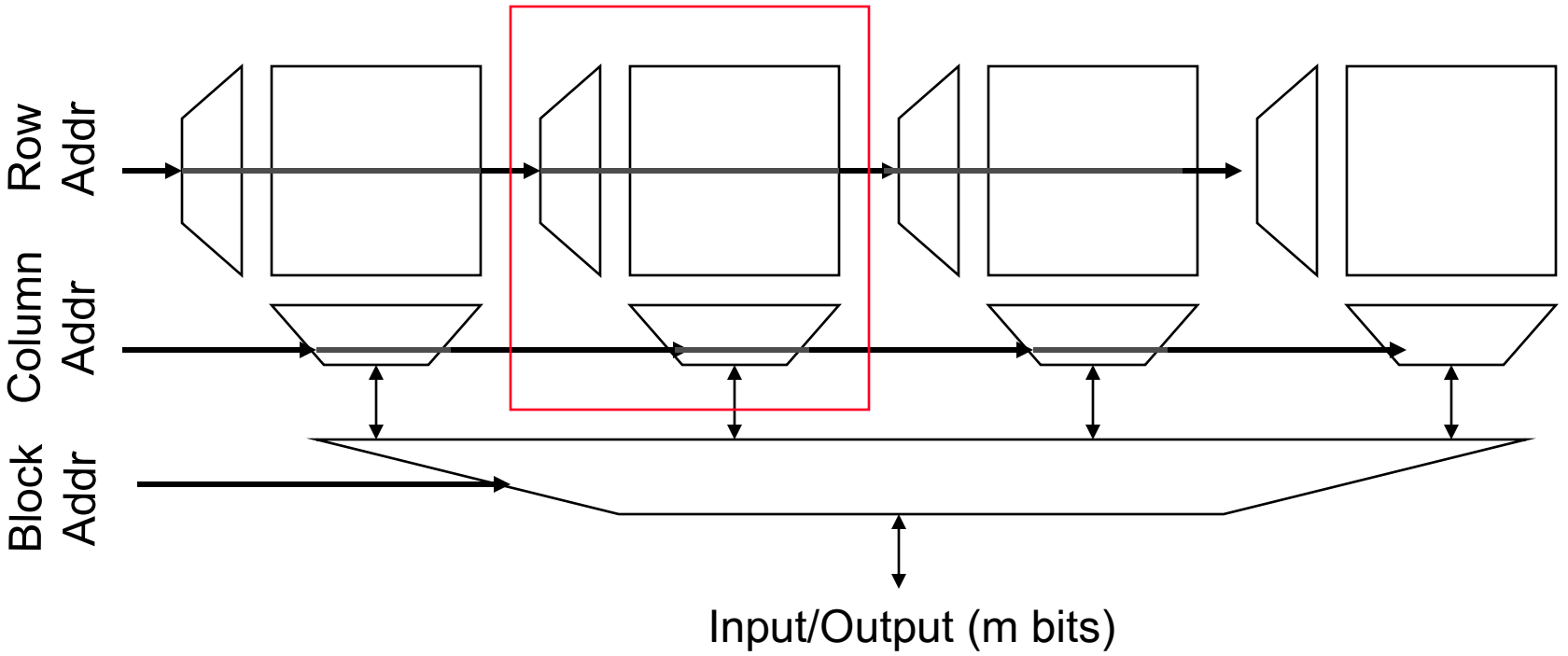
Decoder reduces # of inputs

$k = \log_2 n$

2D Memory Architecture



3D Memory Architecture

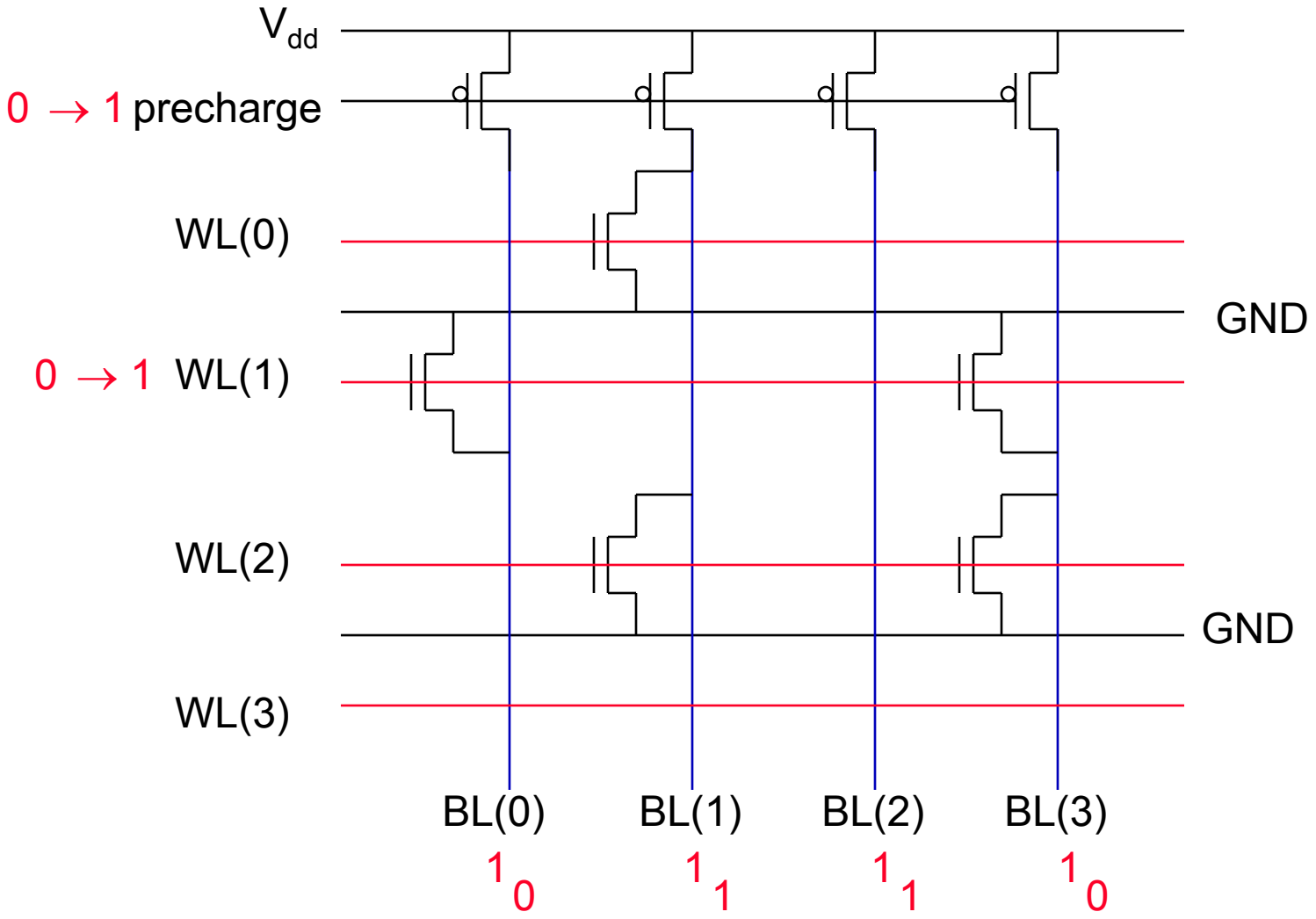


Advantages:

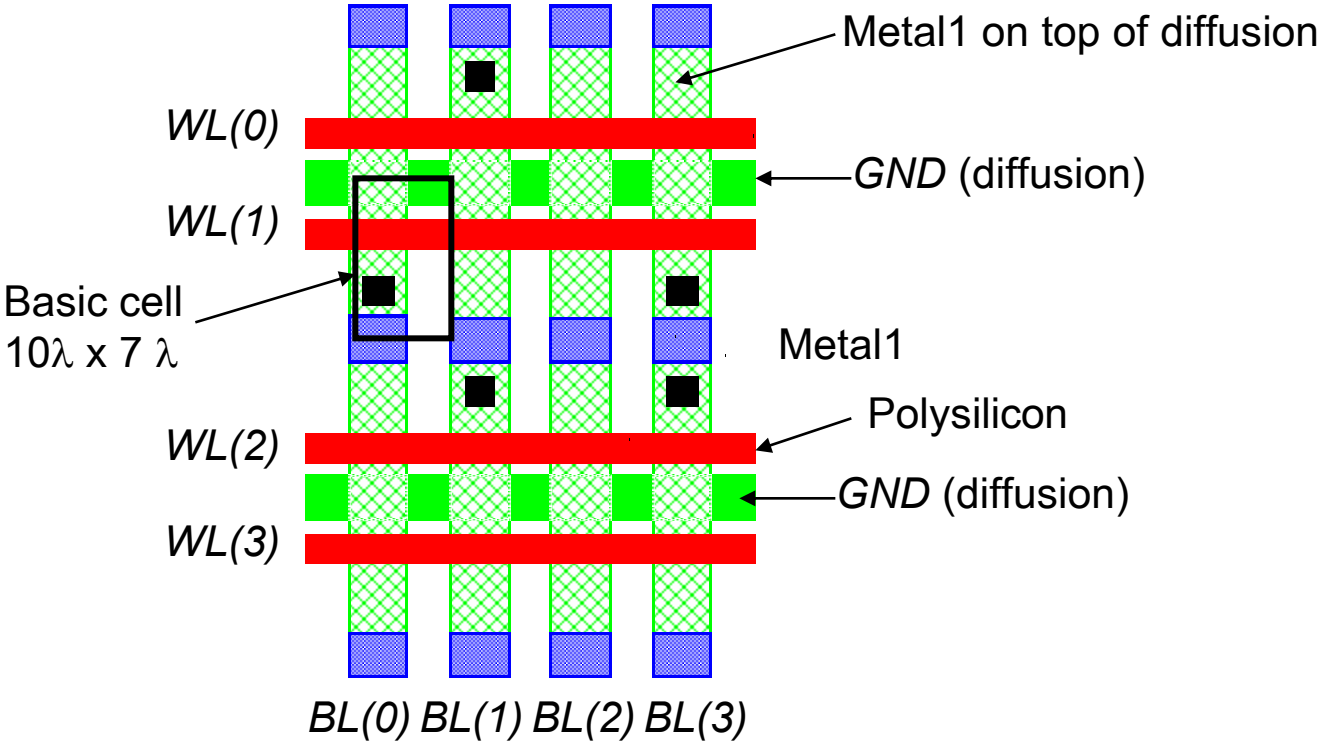
1. Shorter word and/or bit lines
2. Block addr activates only 1 block saving power

Read Only Memories (ROMs)

Precharged MOS NOR ROM

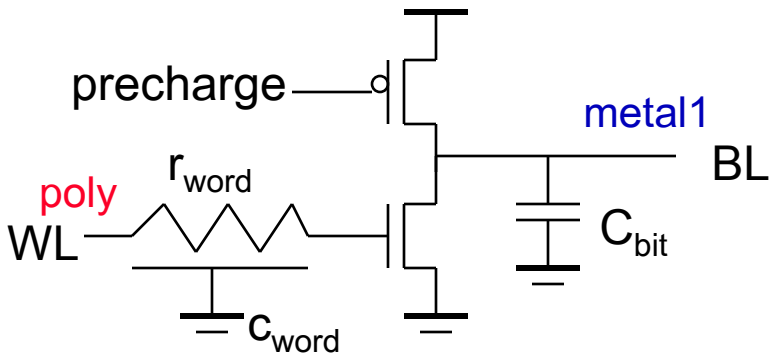


MOS NOR ROM Layout



Only 1 layer (contact mask) is used to program memory array, so programming of the ROM can be delayed to one of the last process steps.

Transient Model for NOR ROM



Word line parasitics

Resistance/cell: 35Ω

Wire capacitance/cell: 0.65 fF

Gate capacitance/cell: 5.10 fF

Bit line parasitics

Resistance/cell: 0.15Ω

Wire capacitance/cell: 0.83 fF

Drain capacitance/cell: 2.60 fF

Propagation Delay of NOR ROM

- Word line delay
  - Delay of a distributed rc-line containing M cells

$$t_{word} = 0.38(r_{word} \times c_{word}) M^2$$

$$= 20 \text{ nsec for } M = 512$$

- Bit line delay
  - Assuming min size pull-down and 3*min size pull-up with reduced swing bit lines (5V to 2.5V)

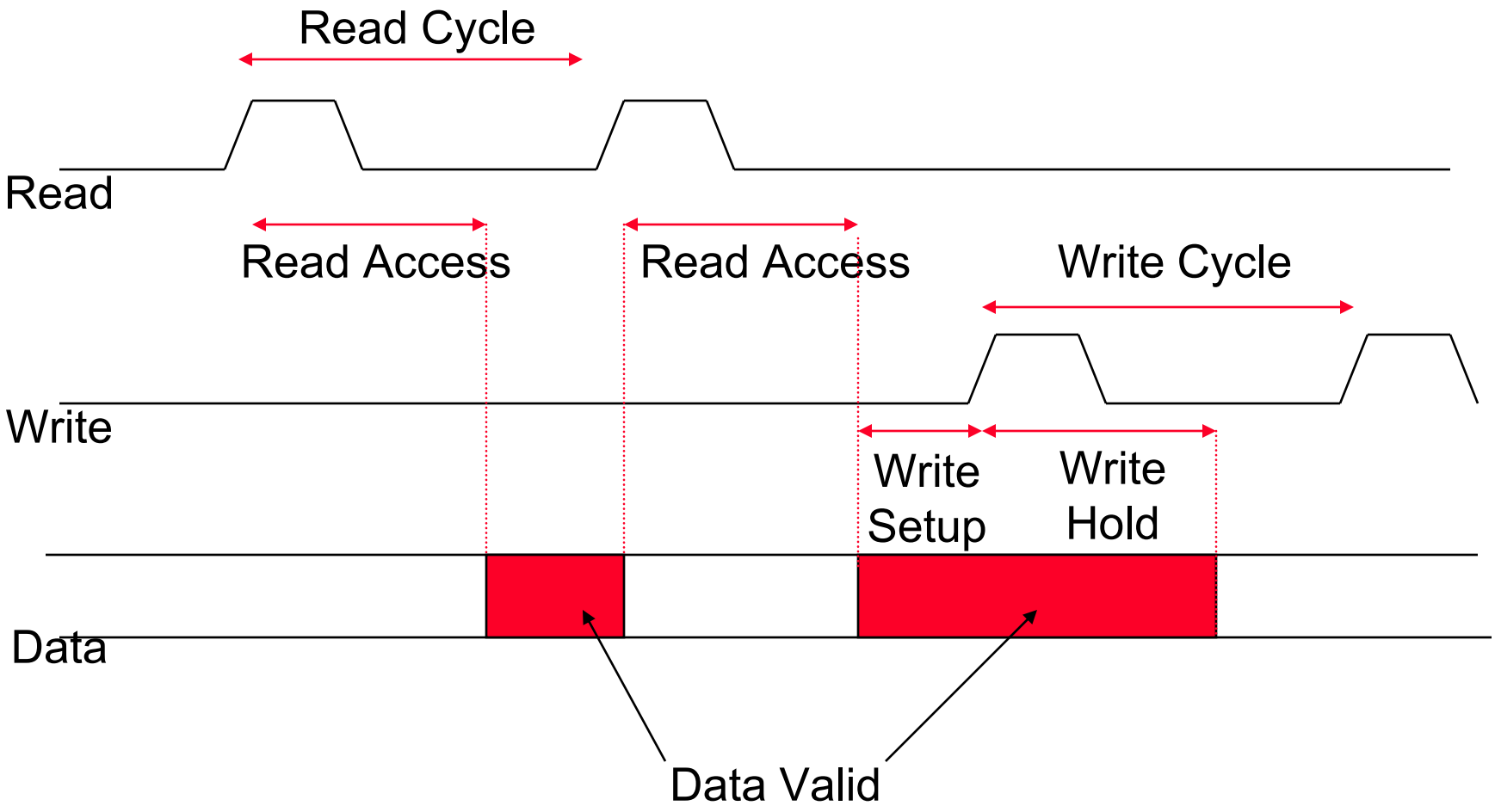
$$C_{bit} = 1.7 \text{ pF and } I_{avHL} = 0.36 \text{ mA so}$$

$$t_{HL} = t_{LH} = 5.9 \text{ nsec}$$

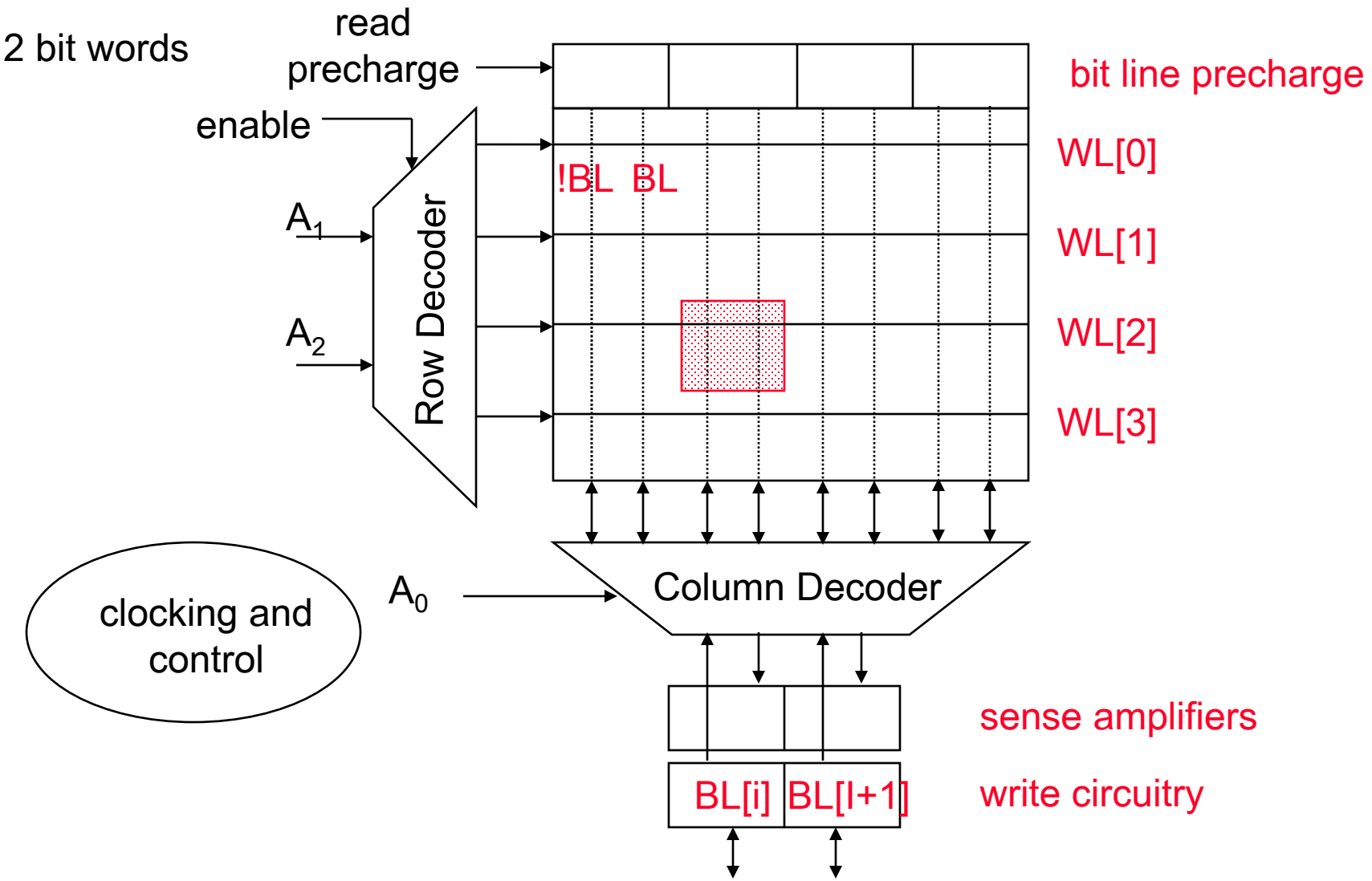
Read-Write Memories (RAMs)

- Static – SRAM
  - data is stored as long as supply is applied
  - large cells (6 fets/cell) – so fewer bits/chip
  - fast – so used where speed is important (e.g., caches)
  - differential outputs (output BL and !BL)
  - use sense amps for performance
  - compatible with CMOS technology
- Dynamic – DRAM
  - periodic refresh required
  - small cells (1 to 3 fets/cell) – so more bits/chip
  - slower – so used for main memories
  - single ended output (output BL only)
  - need sense amps for correct operation
  - not typically compatible with CMOS technology

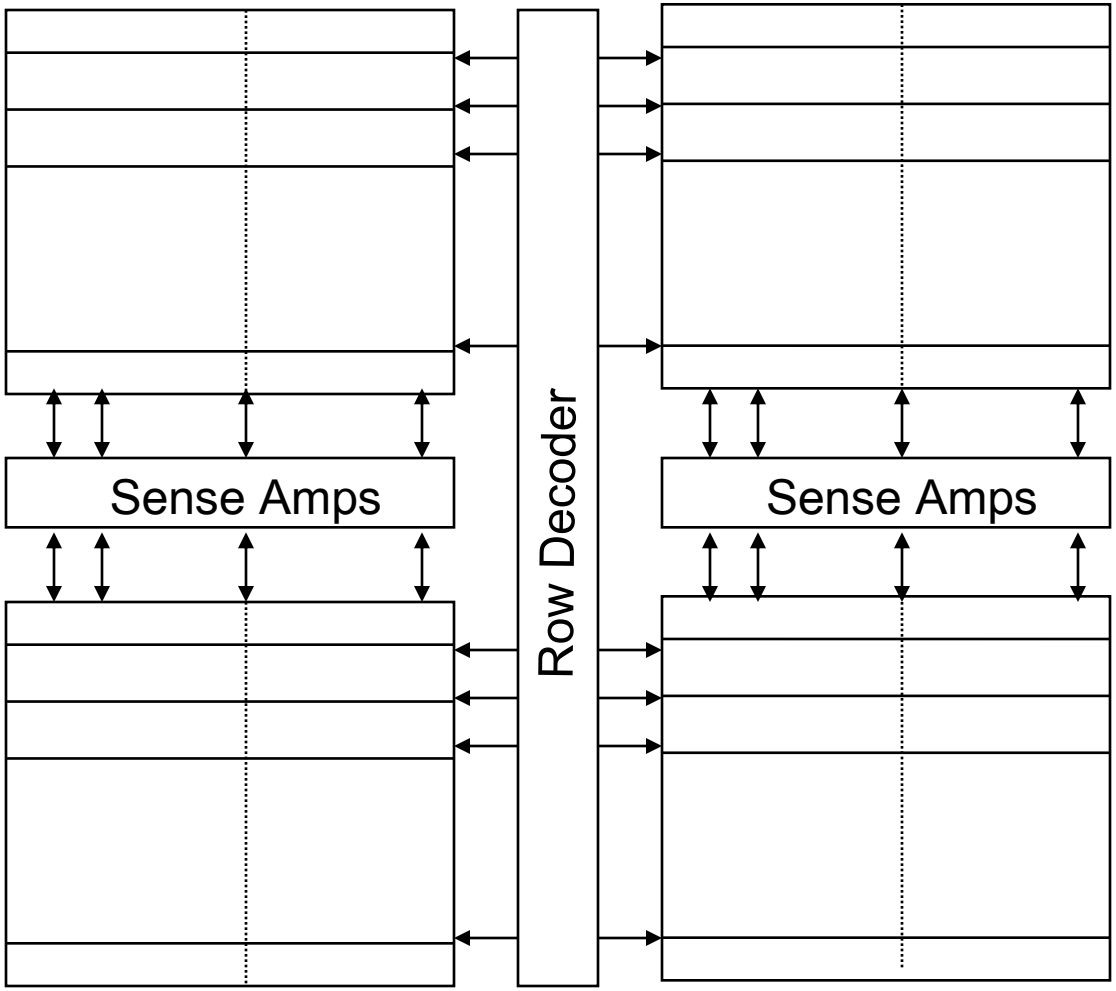
Memory Timing Definitions



4x4 SRAM Memory



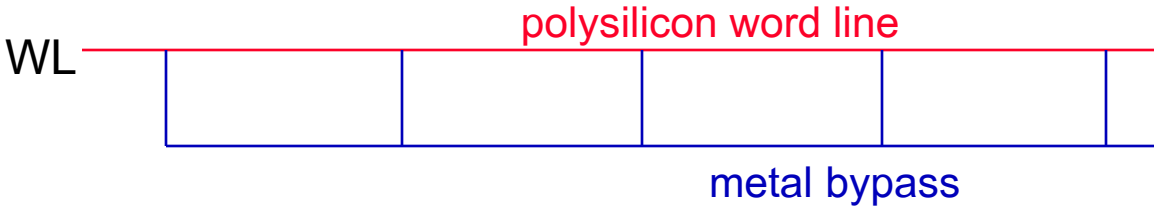
2D Memory Configuration



Decreasing Word Line Delay

- Drive the word line from both sides

- Use a metal bypass

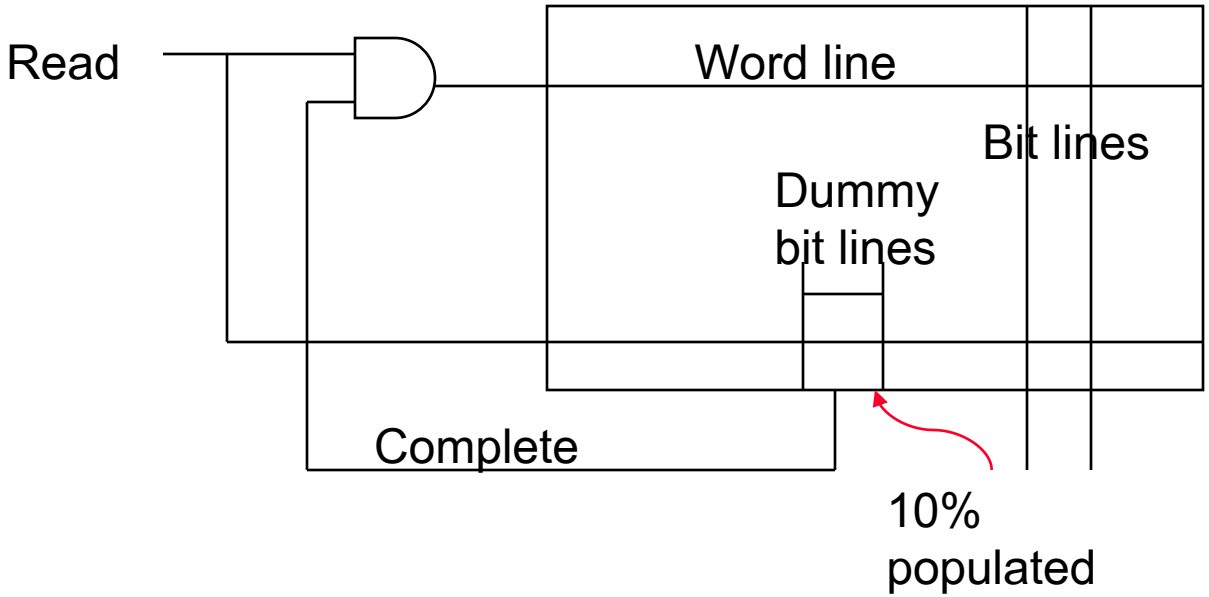


- Use silicides

Decreasing Bit Line Delay (and Energy)

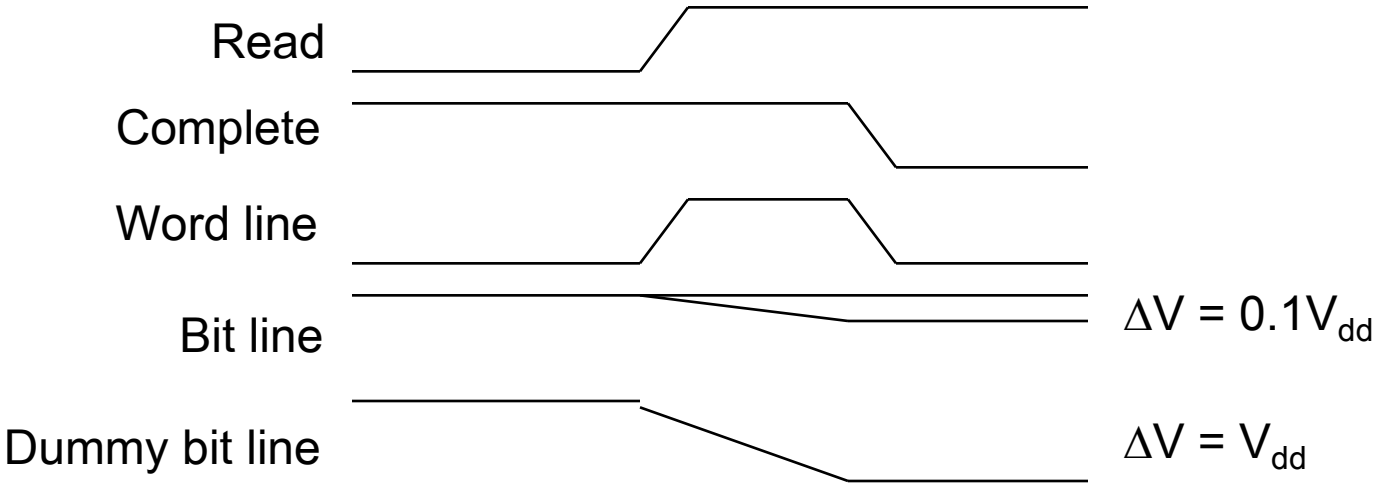
- Reduce the bit line voltage swing
  - need sense amp for each column to sense/restore signal
- Isolate memory cells from the bit lines after sensing (to prevent the cells from changing the bit line voltage further) - pulsed word line
  - generation of word line pulses very critical
    - too short - sense amp operation may fail
    - too long - power efficiency degraded (because bit line swing size depends on duration of the word line pulse)
  - use feedback signal from bit lines
- Isolate sense amps from bit lines after sensing (to prevent bit lines from having large voltage swings) - bit line isolation

Pulsed Word Line Feedback Signal



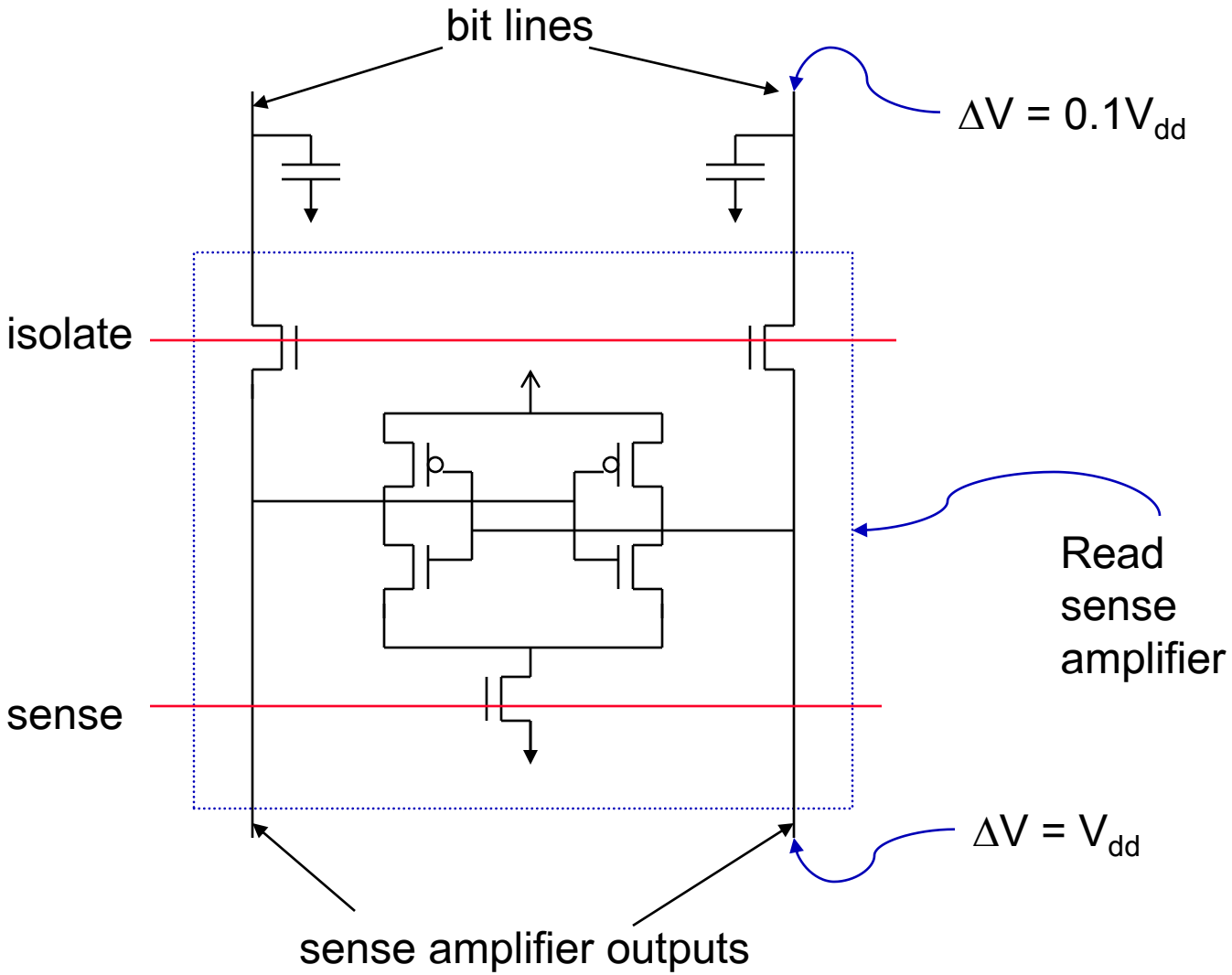
- Dummy column
  - height set to 10% of a regular column and its cells are tied to a fixed value
  - capacitance is only 10% of a regular column

Pulsed Word Line Timing

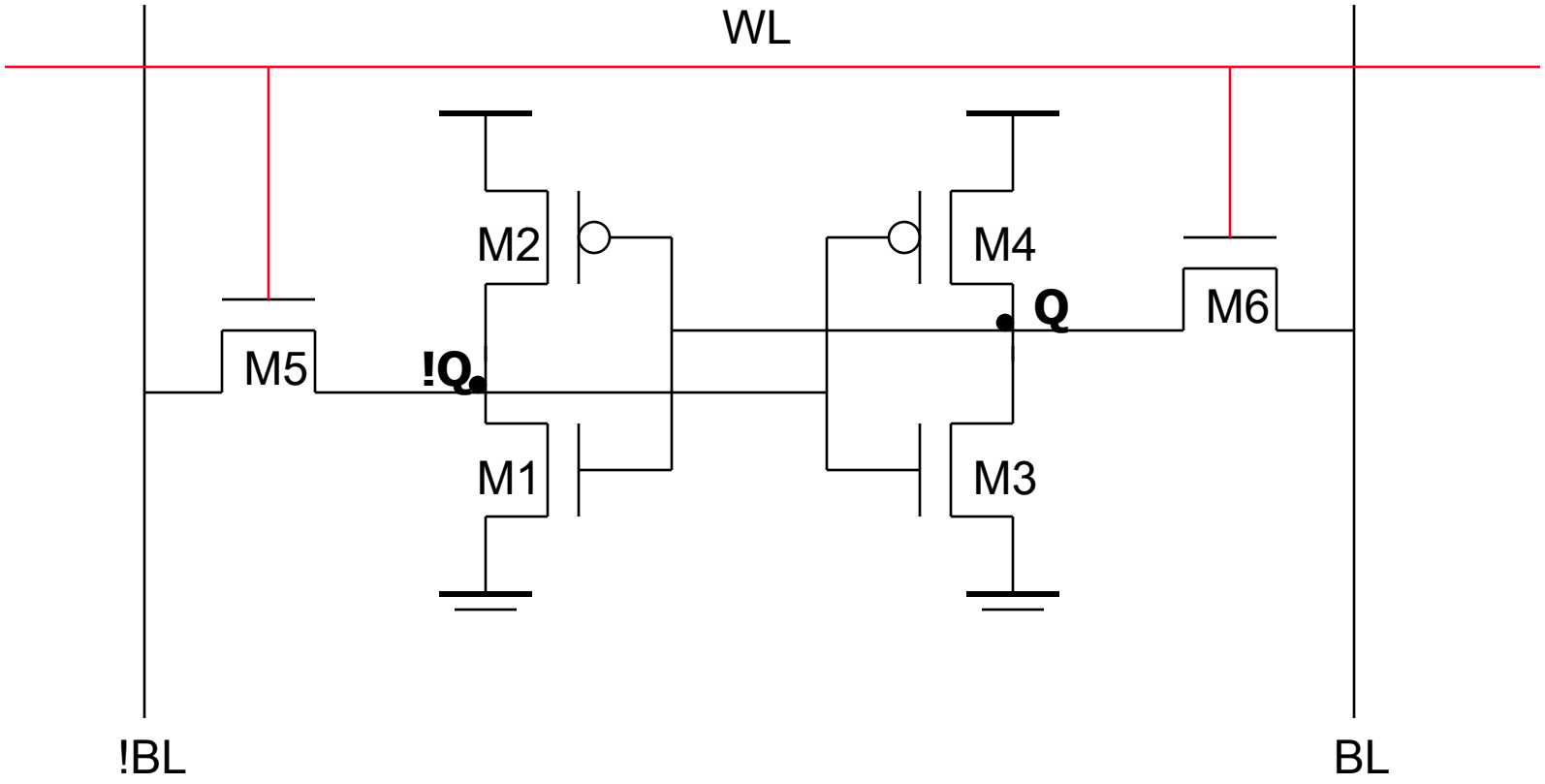


- Dummy bit lines have reached full swing and trigger pulse shut off when regular bit lines reach 10% swing

Bit Line Isolation



6-transistor SRAM Cell



Next Lecture and Reminders

- Next lecture
  - SRAM, DRAM, and CAM cores
    - Reading assignment – Rabaey, et al, 12.2.2-12.2.3
- Reminders
  - Project final reports due December 5th
  - Final grading negotiations/correction (except for the final exam) must be concluded by December 10th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in 118 and 121 Thomas