CSE477
VLSI Digital Circuits
Fall 2002

Lecture 03: MOS Transistor

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Course Administration

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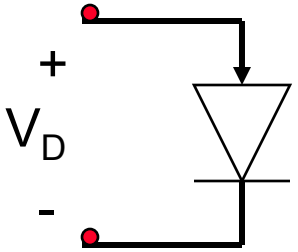
- Labs: Accounts on 101 Pond Lab machines
- URL: www.cse.psu.edu/~cg477
- Text: *Digital Integrated Circuits*, 2nd Edition
  Rabaey et. al., ©2002 (October)
- Handouts: Leftover handouts available outside my office door after class

Review: Fundamental Design Metrics

- Functionality
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay)
  - Power consumption; energy
- Time-to-market

Review: Reverse Bias Diode

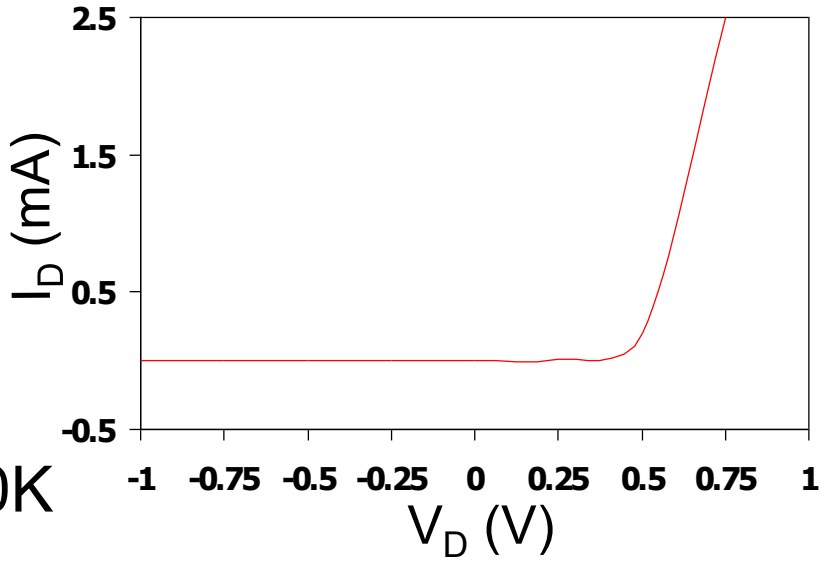
- The *ideal diode equation* (for both forward and reverse-bias conditions) is



$$I_D = I_S(e^{V_D/\phi_T} - 1)$$

where V_D is the voltage applied to the junction

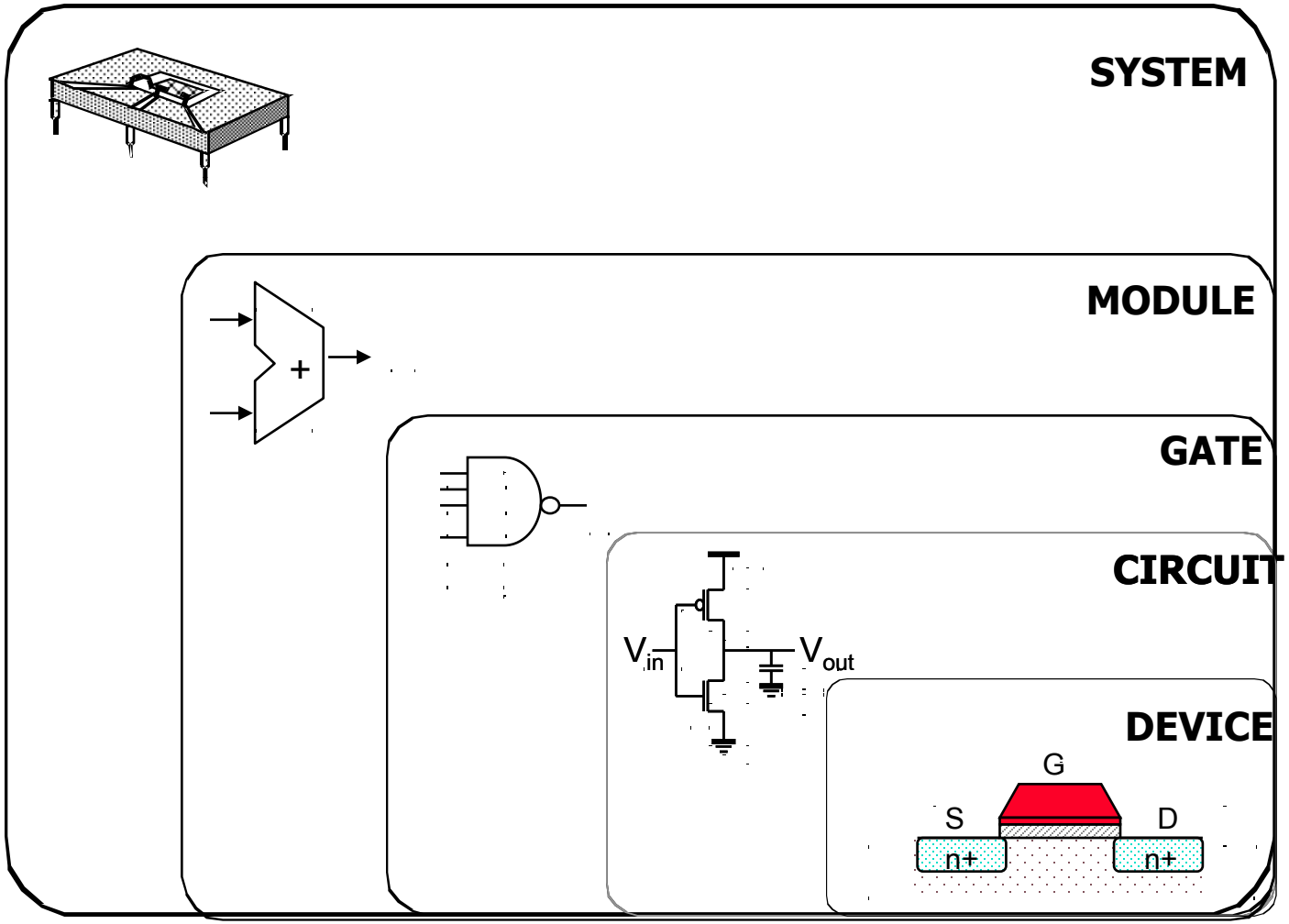
- a forward-bias lowers the potential barrier allowing carriers to flow across the diode junction
- a reverse-bias raises the potential barrier and the diode becomes nonconducting



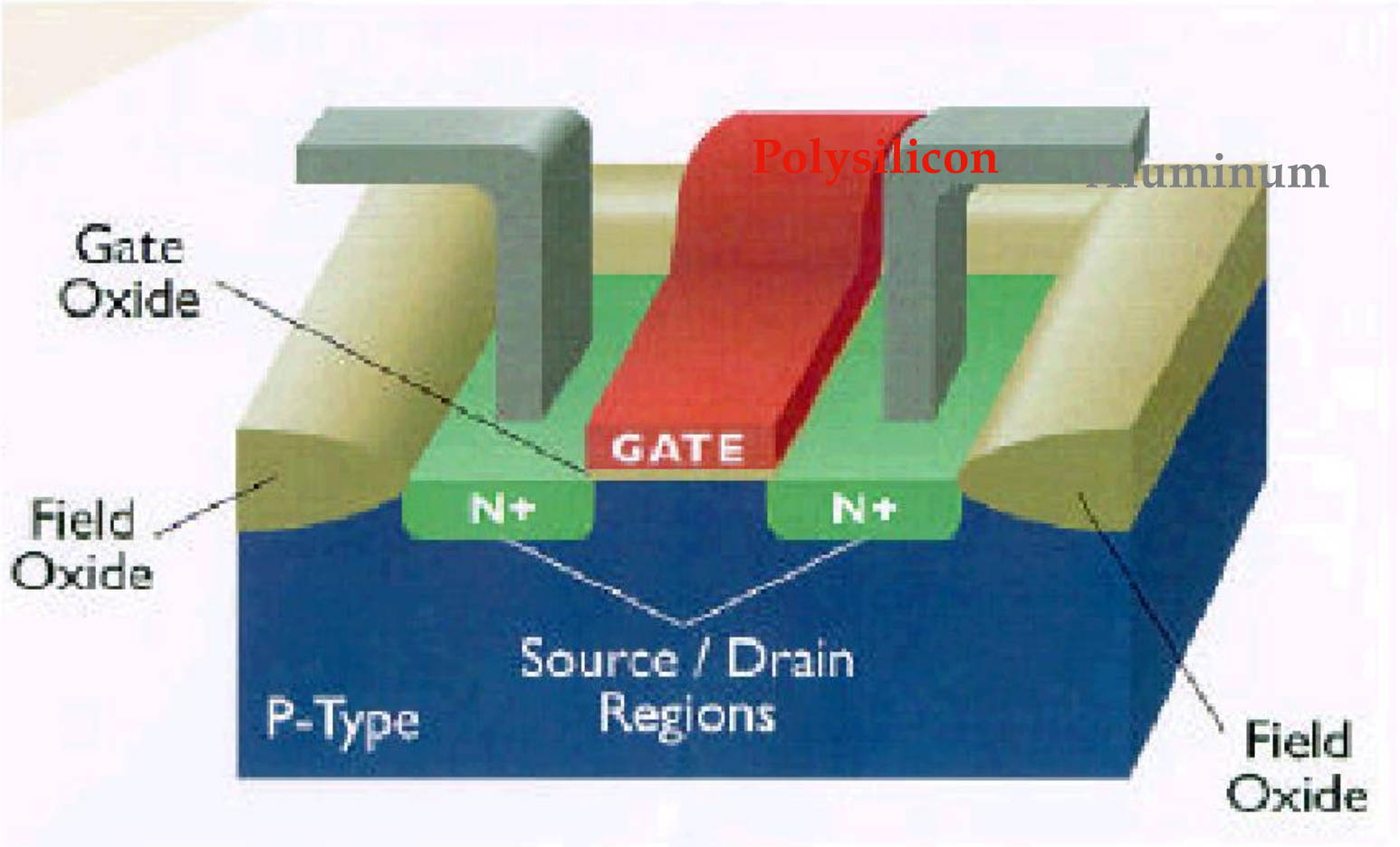
$\phi_T = kT/q = 26mV$ at 300K

I_S is the saturation current of the diode

Review: Design Abstraction Levels

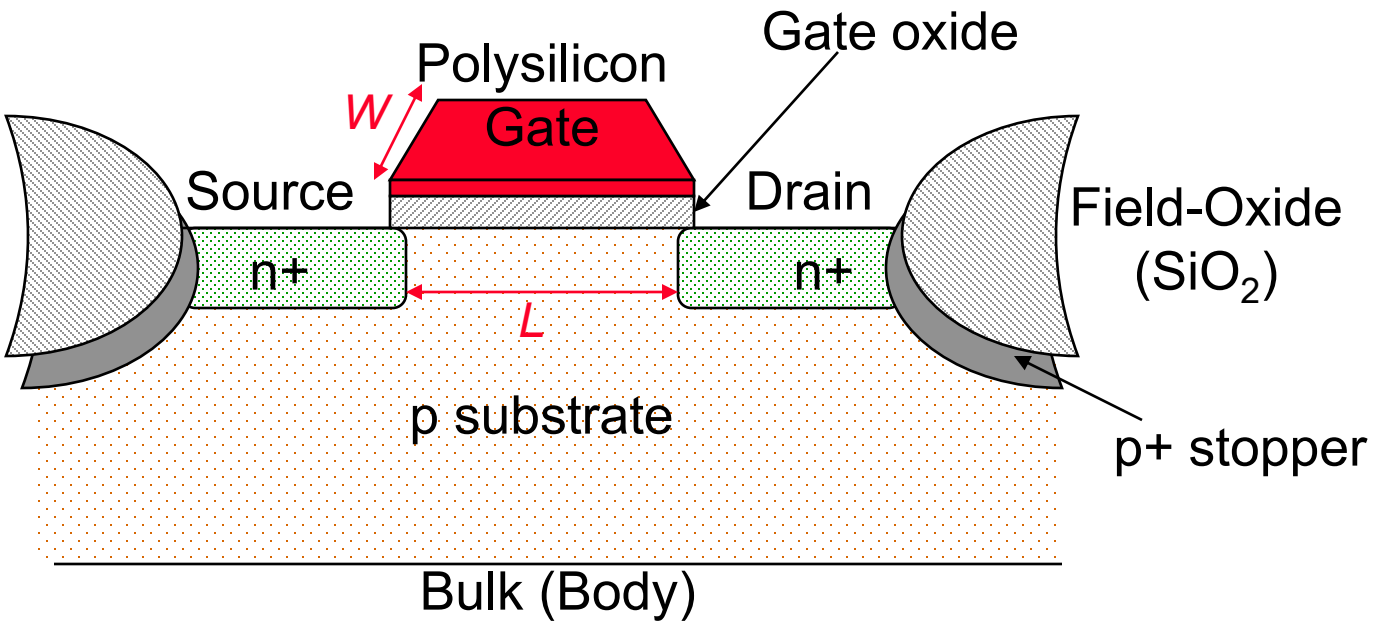


The MOS Transistor



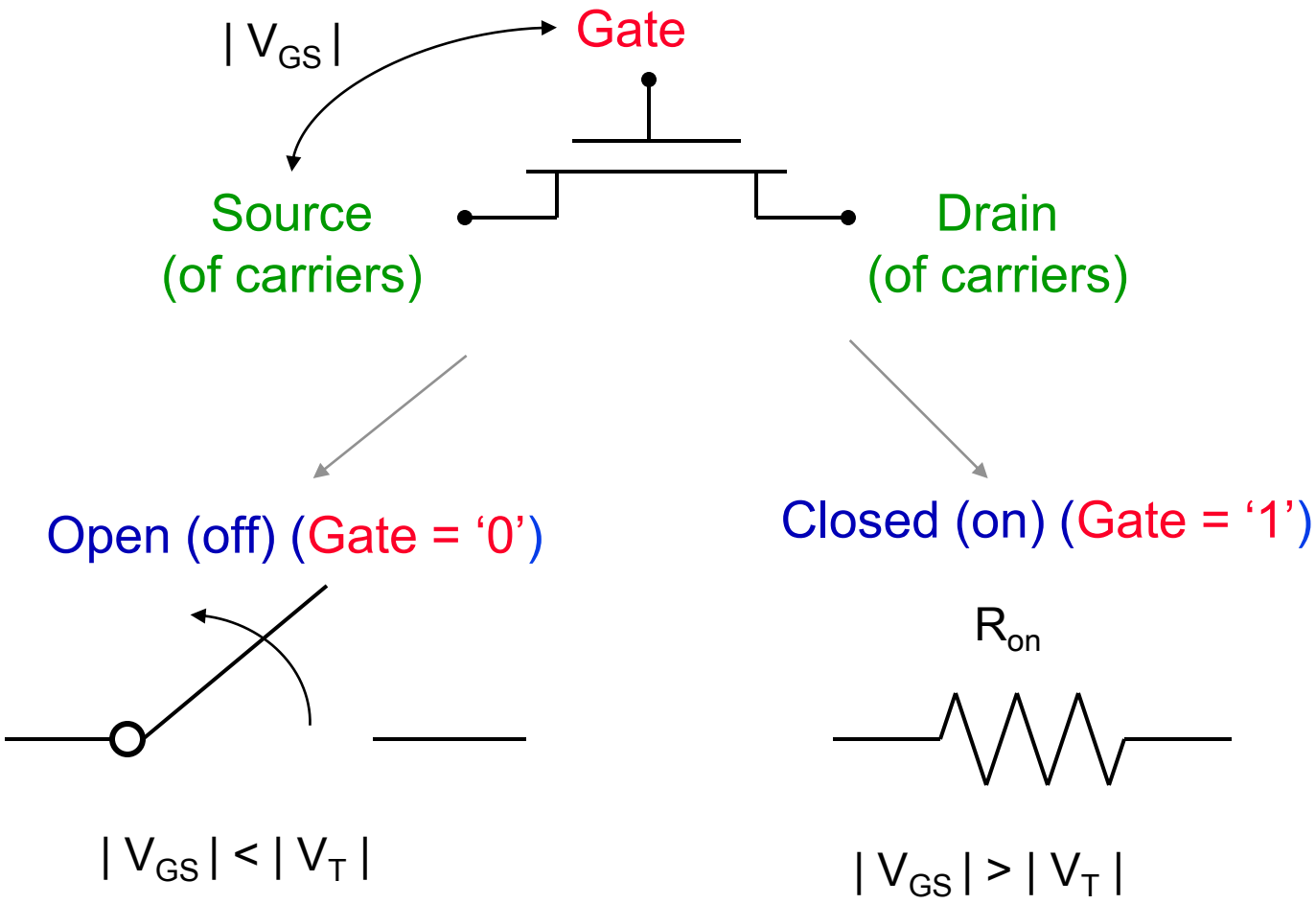
The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration N_D - electrons are the majority carriers

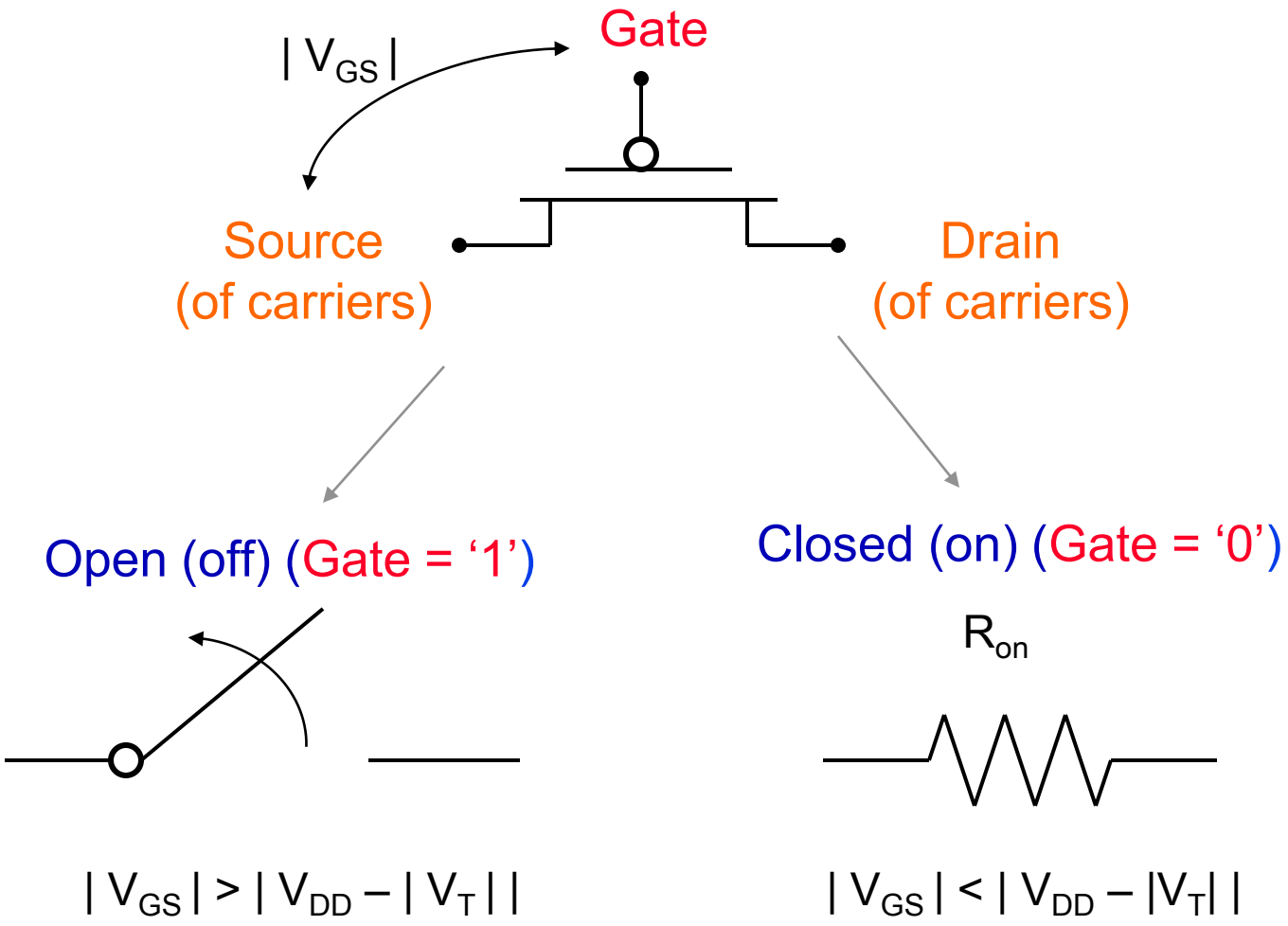


p areas have been doped with acceptor ions (boron) of concentration N_A - holes are the majority carriers

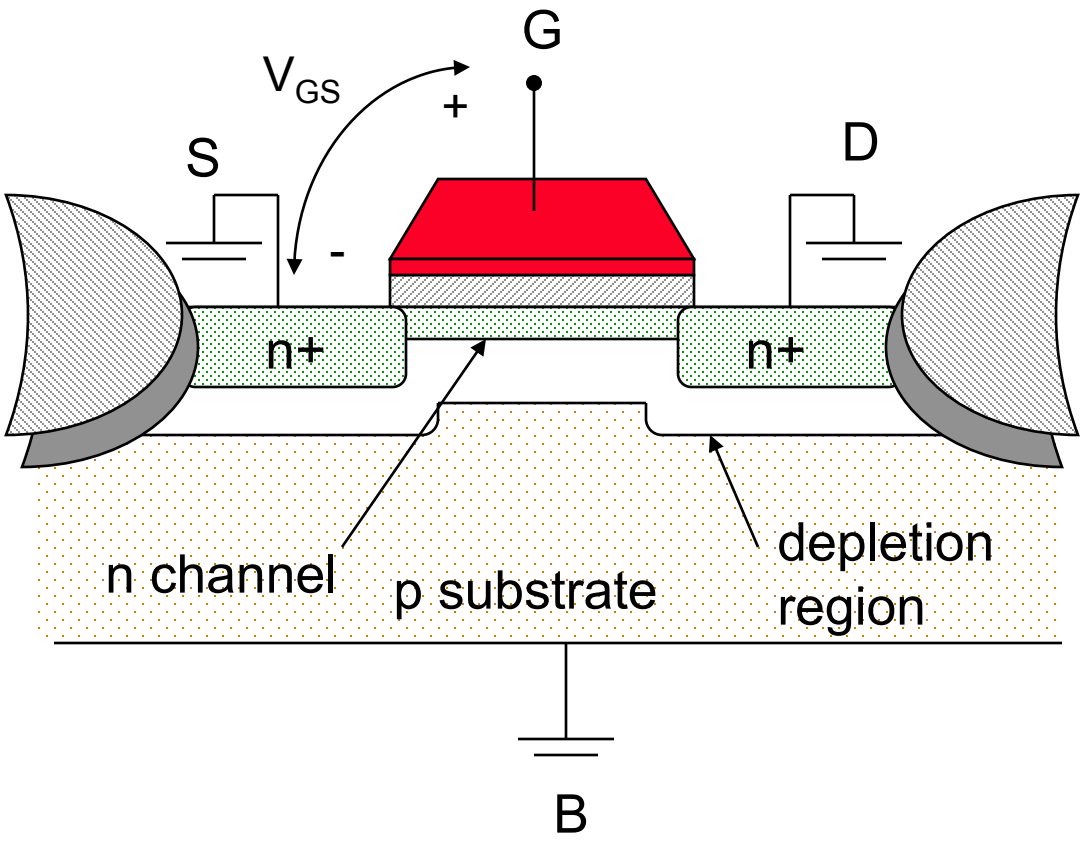
Switch Model of NMOS Transistor



Switch Model of PMOS Transistor



Threshold Voltage Concept



The value of V_{GS} where strong inversion occurs is called the threshold voltage, V_T

The Threshold Voltage

where $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

V_{T0} is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process

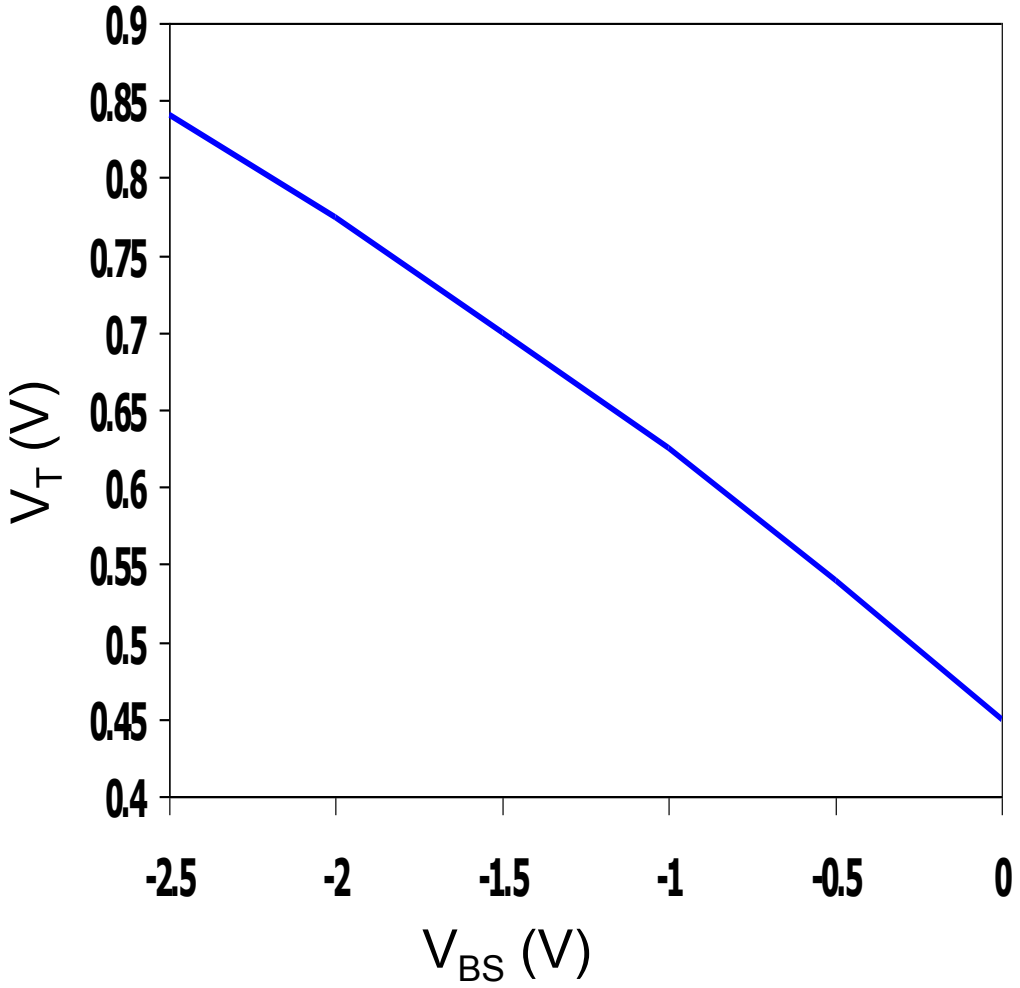
- Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

V_{SB} is the source-bulk voltage

$\phi_F = -\phi_T \ln(N_A/n_i)$ is the Fermi potential ($\phi_T = kT/q = 26mV$ at 300K is the thermal voltage; N_A is the acceptor ion concentration; $n_i \approx 1.5 \times 10^{10}$ cm^{-3} at 300K is the intrinsic carrier concentration in pure silicon)

$\gamma = \sqrt{(2q\varepsilon_{si}N_A)}/C_{ox}$ is the body-effect coefficient (impact of changes in V_{SB}) ($\varepsilon_{si}=1.053 \times 10^{-10}$F/m is the permittivity of silicon; $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance with $\varepsilon_{ox}=3.5 \times 10^{-11}$F/m)

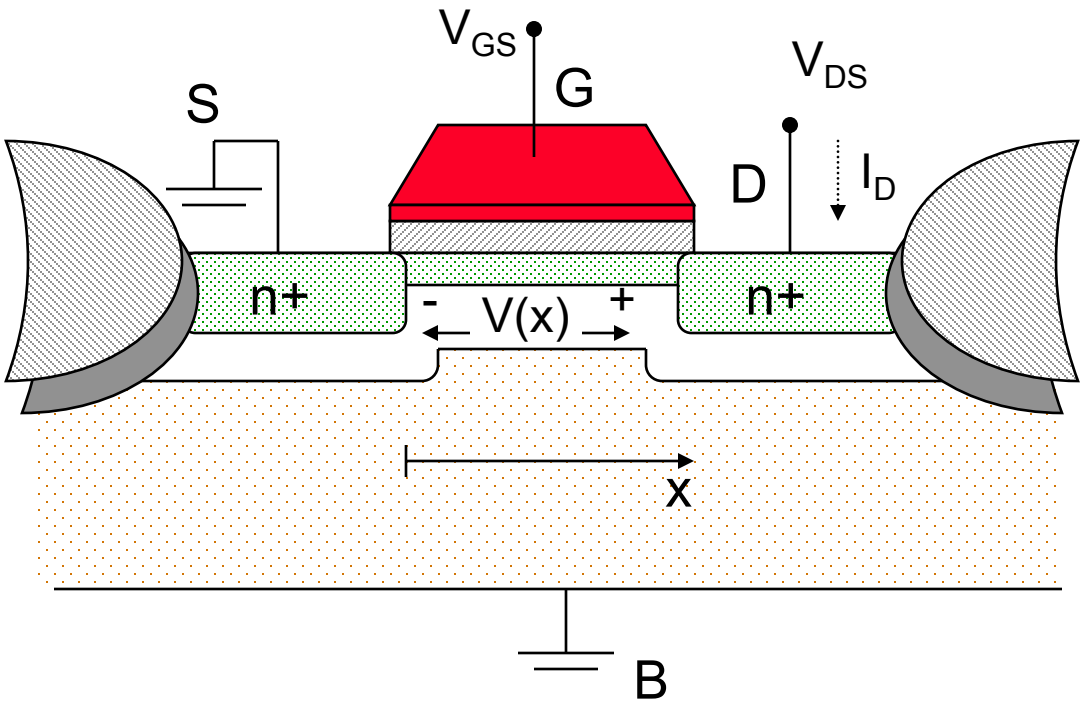
The Body Effect



- V_{SB} is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes V_T to increase from 0.45V to 0.85V

Transistor in Linear Mode

Assuming $V_{GS} > V_T$



The current is a linear function of both V_{GS} and V_{DS}

Voltage-Current Relation: Linear Mode

For long-channel devices (L > 0.25 micron)

- When $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \, W/L \, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

where

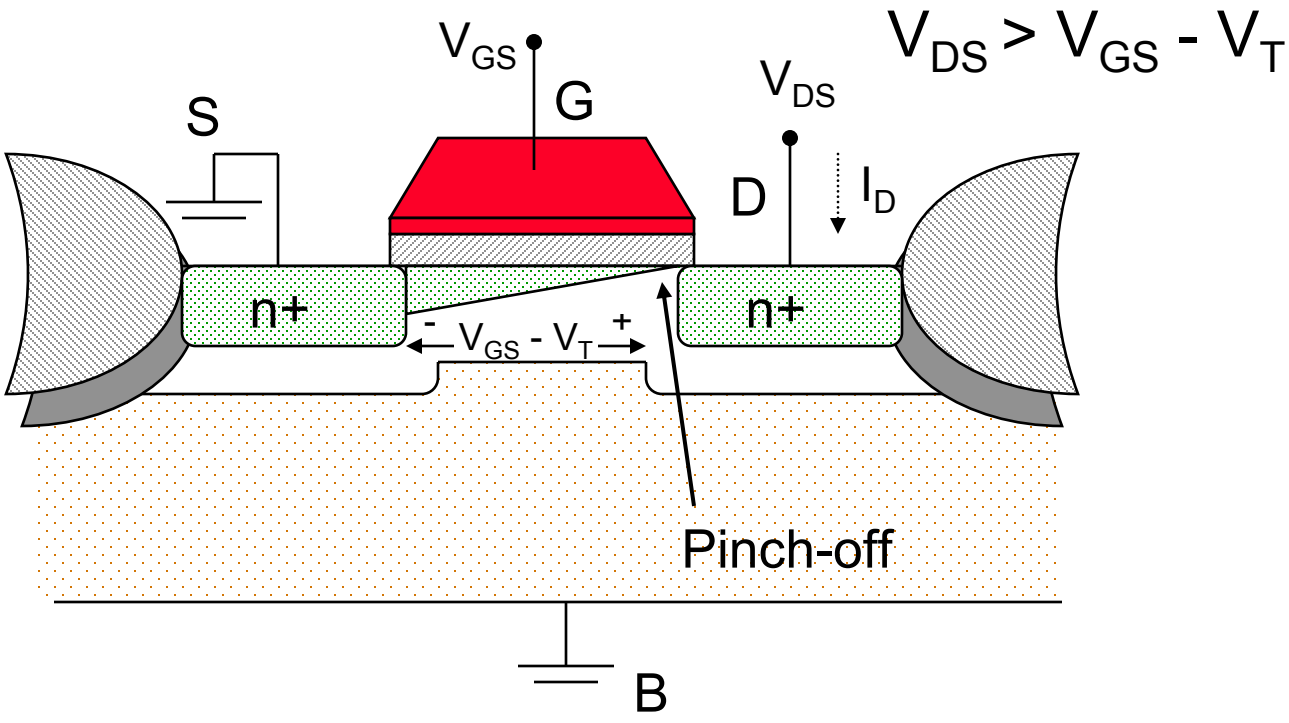
$k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$ = is the process transconductance parameter (μ_n is the carrier mobility (m^2/Vsec))

$k_n = k'_n \, W/L$ is the gain factor of the device

For small V_{DS}, there is a linear dependence between V_{DS} and I_D, hence the name resistive or linear region

Transistor in Saturation Mode

Assuming $V_{GS} > V_T$



The current remains constant (saturates).

Voltage-Current Relation: Saturation Mode

For long channel devices

- When $V_{DS} \geq V_{GS} - V_T$

$$I_D' = k'_n/2 \; W/L \; [(V_{GS} - V_T)^2]$$

since the voltage difference over the induced channel (from the pinch-off point to the source) remains fixed at $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied V_{DS}, so

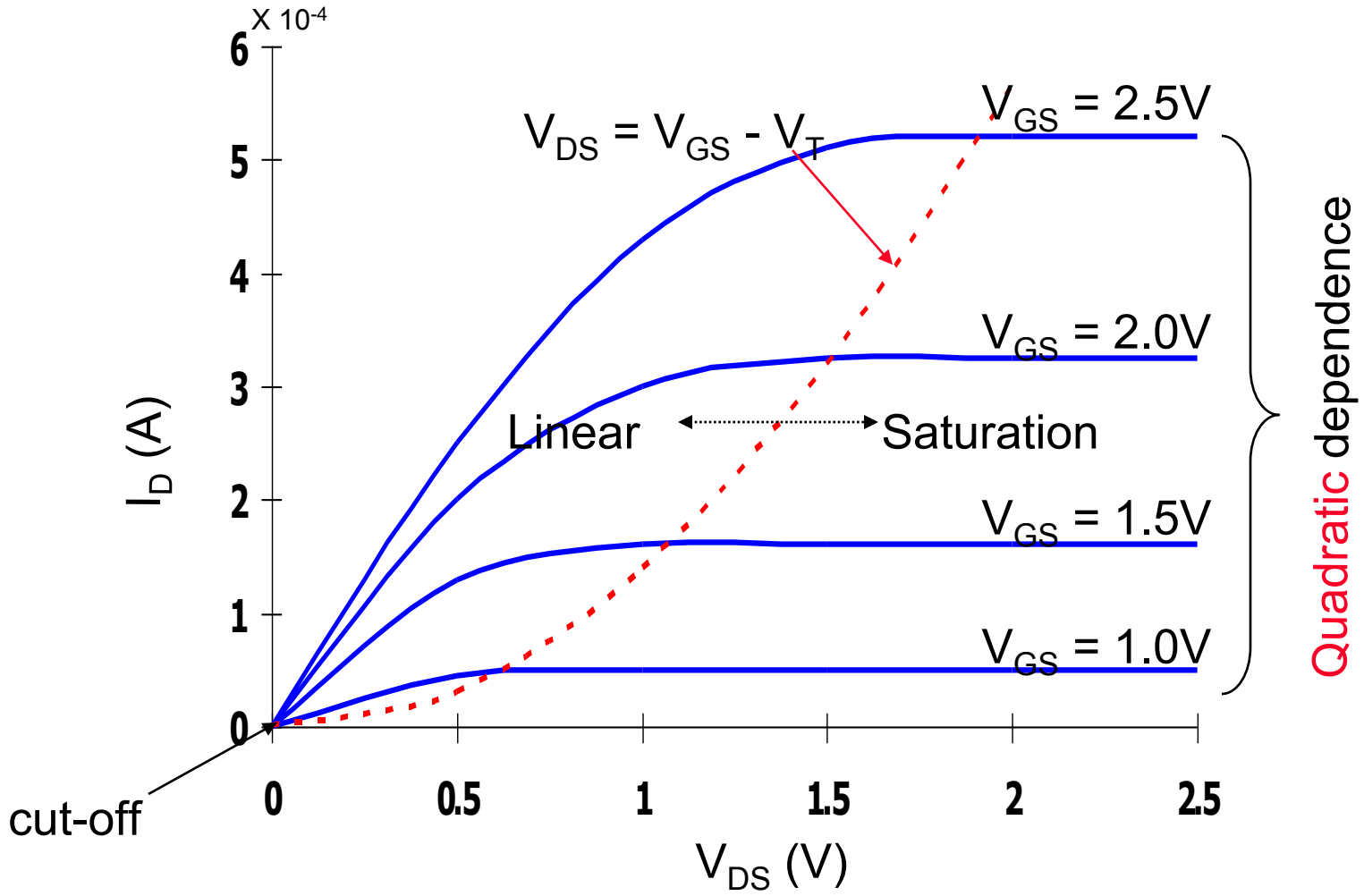
$$I_D = I_D' (1 + \lambda V_{DS})$$

where λ is the channel-length modulation (varies with the inverse of the channel length)

Current Determinates

- For a fixed V_{DS} and V_{GS} (> V_T), I_{DS} is a function of
  - the distance between the source and drain – L
  - the channel width – W
  - the threshold voltage – V_T
  - the thickness of the SiO_2 – t_{ox}
  - the dielectric of the gate insulator (SiO_2) – ε_{ox}
  - the carrier mobility
    - for nfets: μ_n = 500 cm^2/V-sec
    - for pfets: μ_p = 180 cm^2/V-sec

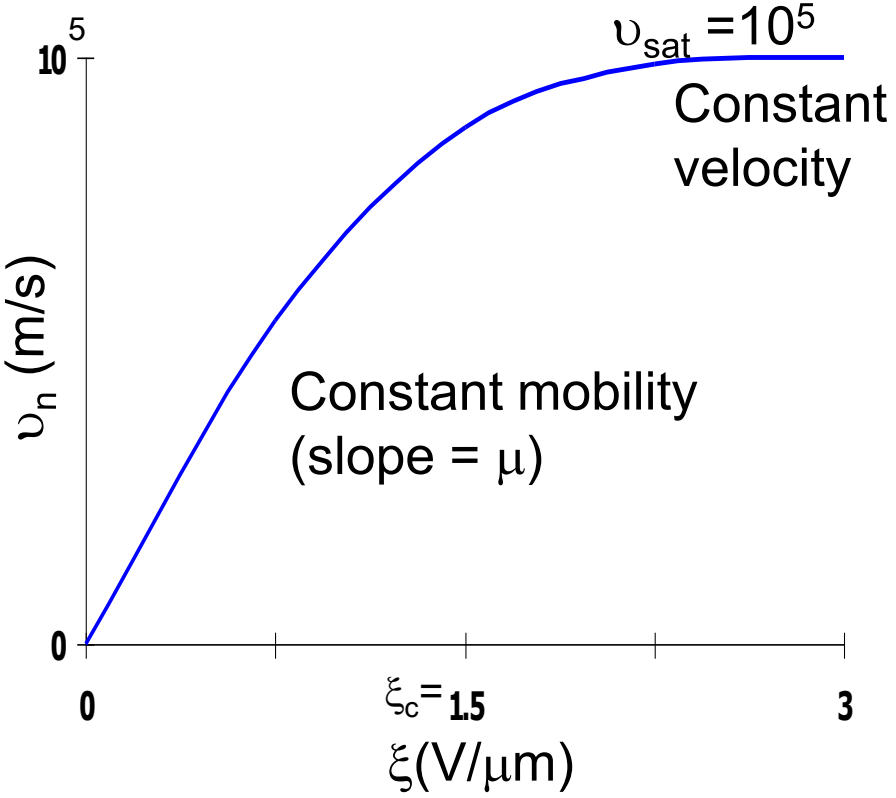
Long Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

Short Channel Effects

- Behavior of short channel device mainly due to



- Velocity saturation – the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

- For an NMOS device with L of .25μm, only a couple of volts difference between D and S are needed to reach velocity saturation

Voltage-Current Relation: Velocity Saturation

For short channel devices

- Linear: When $V_{DS} \leq V_{GS} - V_T$

$$I_D = \kappa(V_{DS})\, k'_n\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

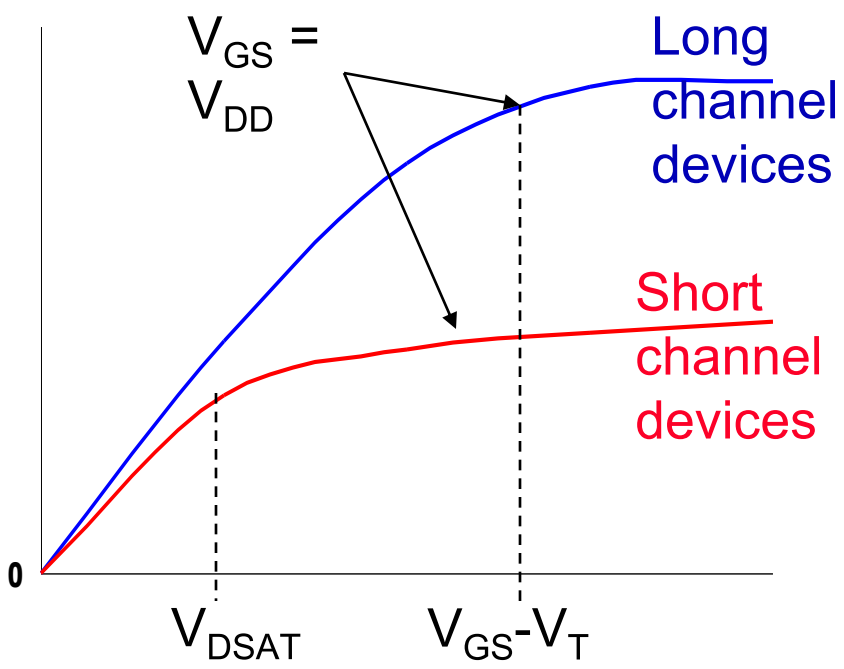
where

$\kappa(V) = 1/(1 + (V/\xi_c L))$ is a measure of the degree of velocity saturation

- Saturation: When $V_{DS} = V_{DSAT} \geq V_{GS} - V_T$

$$I_{DSat} = \kappa(V_{DSAT})\, k'_n\, W/L\, [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2]$$

Velocity Saturation Effects

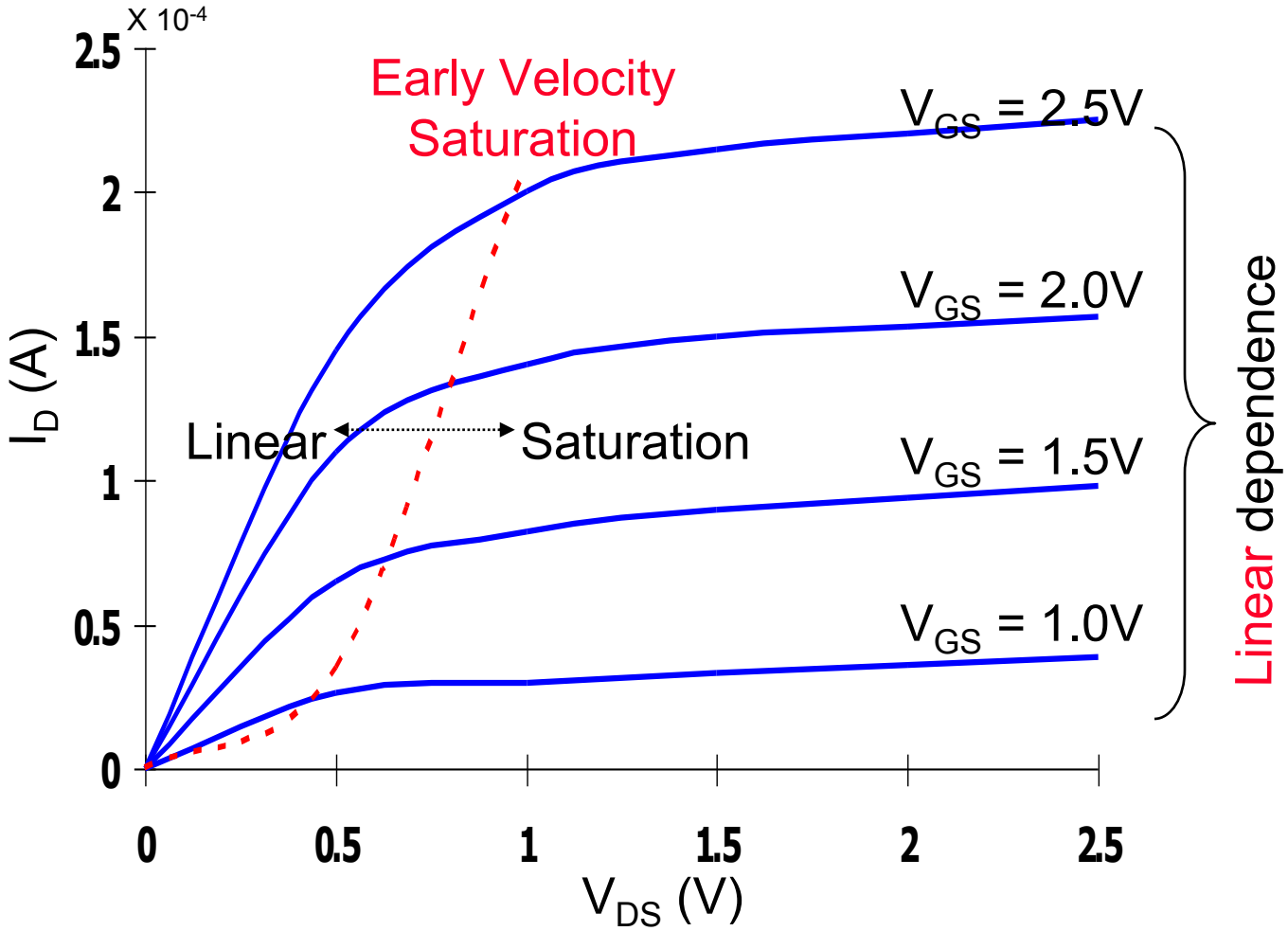


For short channel devices and large enough $V_{GS} - V_T$

- $V_{DSAT} < V_{GS} - V_T$ so the device enters saturation before V_{DS} reaches $V_{GS} - V_T$ and operates more often in saturation

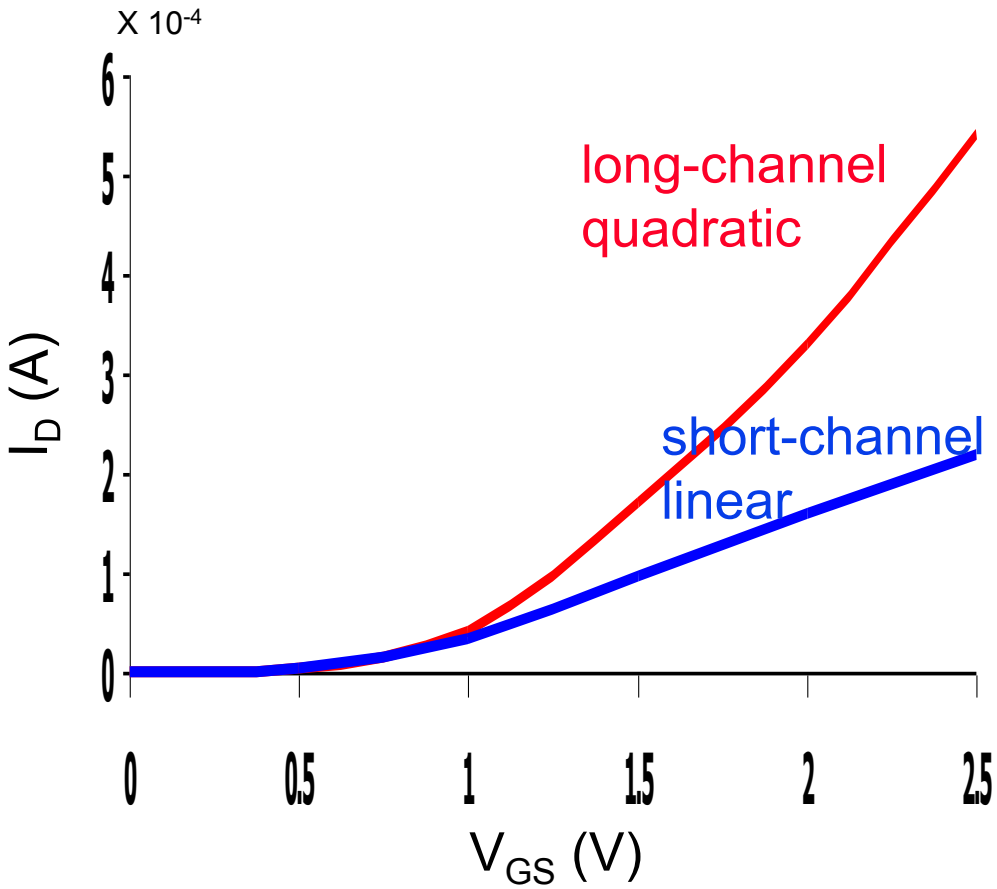
- I_{DSAT} has a linear dependence wrt V_{GS} so a reduced amount of current is delivered for a given control voltage

Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

MOS I_D-V_{GS} Characteristics

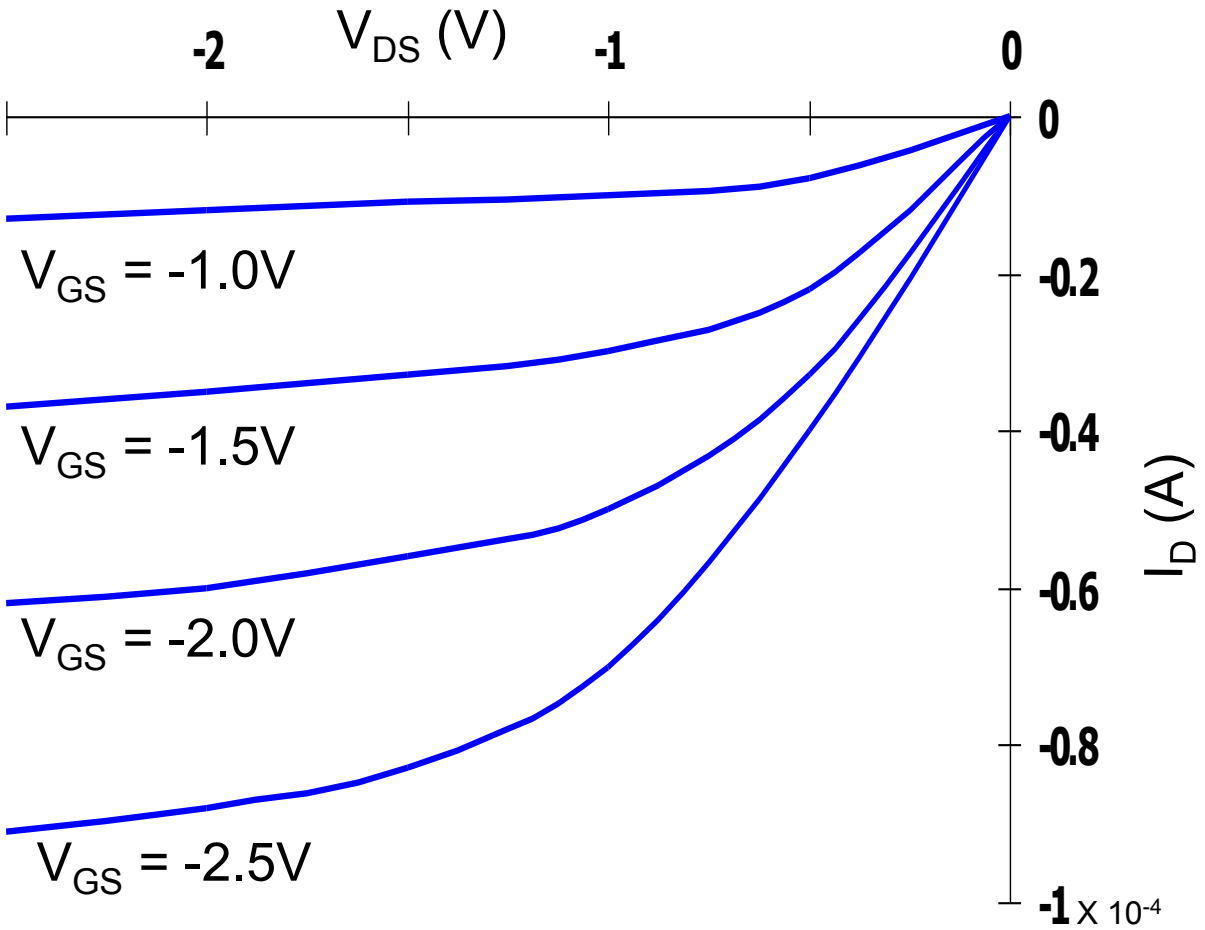


(for V_{DS} = 2.5V, W/L = 1.5)

- Linear (short-channel) versus quadratic (long-channel) dependence of I_D on V_{GS} in saturation
- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of V_{DS} resulting in a substantial drop in current drive

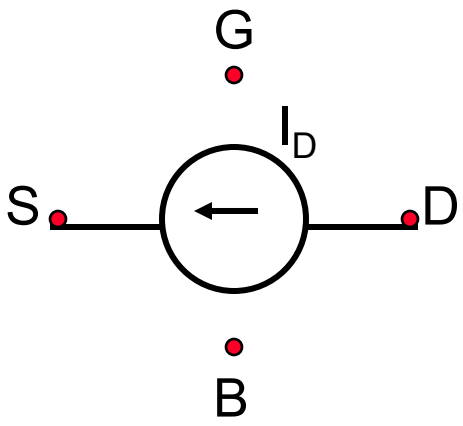
Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed



PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

The MOS Current-Source Model



$I_D = 0$ for $V_{GS} - V_T \leq 0$

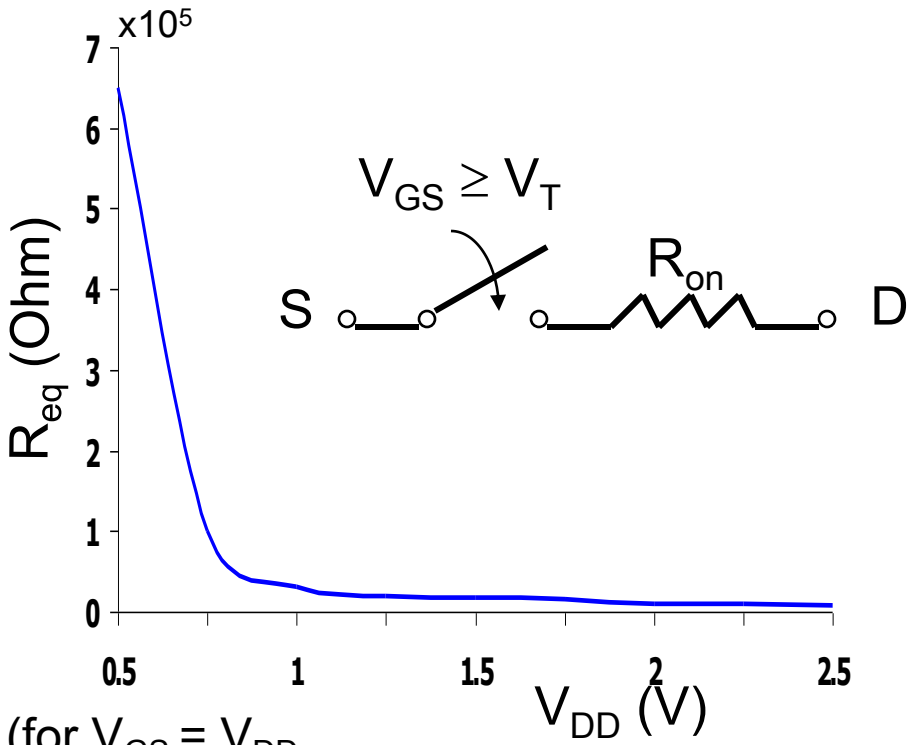
$I_D = k' W/L [(V_{GS} - V_T)V_{min} - V_{min}^2/2](1+\lambda V_{DS})$
for $V_{GS} - V_T \geq 0$

with $V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT})$
and $V_{GT} = V_{GS} - V_T$

- Determined by the voltages at the four terminals and a set of five device parameters

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

The Transistor Modeled as a Switch



(for $V_{GS} = V_{DD}$, $V_{DS} = V_{DD} \rightarrow V_{DD}/2$)

Modeled as a switch with infinite off resistance and a finite on resistance, R_{on}

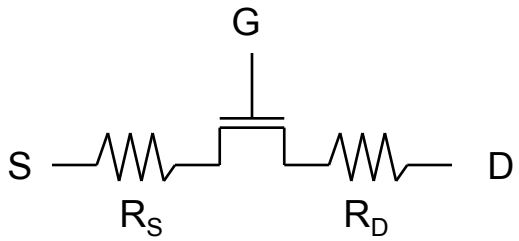
- Resistance inversely proportional to W/L (doubling W halves R_{on})
- For $V_{DD} >> V_T + V_{DSAT}/2$, R_{on} independent of V_{DD}
- Once V_{DD} approaches V_T, R_{on} increases dramatically

V_{DD}(V)	1	1.5	2	2.5
NMOS(kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

R_{on} (for W/L = 1)
For larger devices divide R_{eq} by W/L

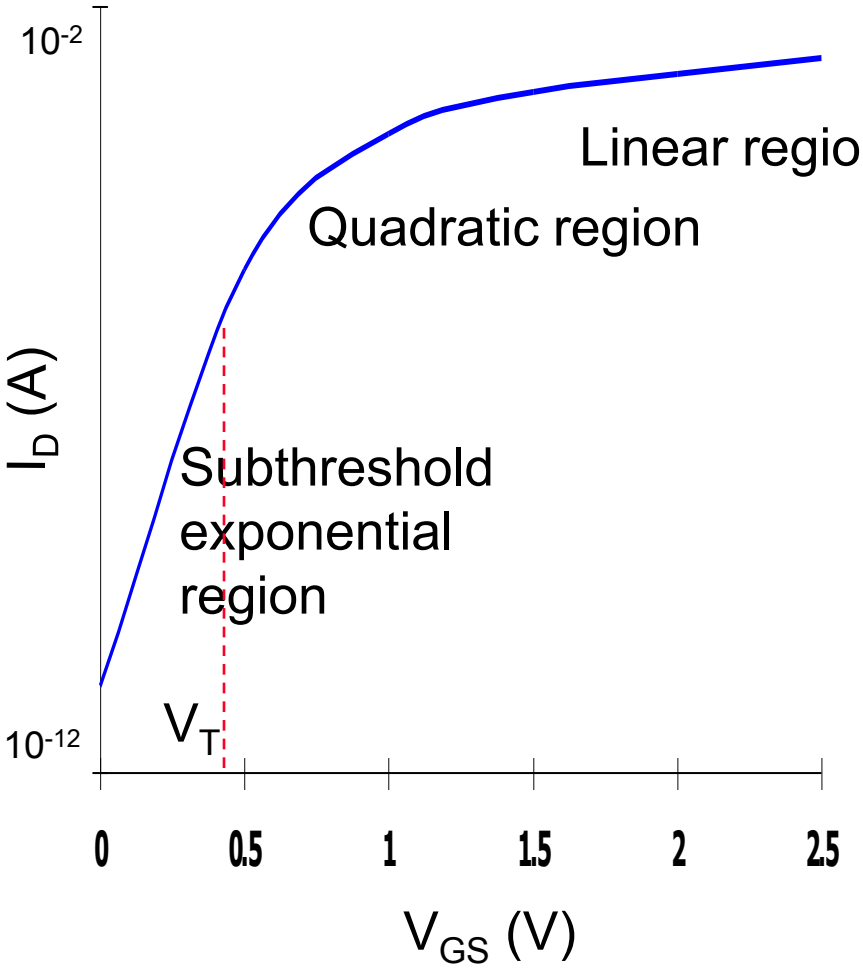
Other (Submicon) MOS Transistor Concerns

- Velocity saturation
- Subthreshold conduction
  - Transistor is already partially conducting for voltages below V_T
- Threshold variations
  - In long-channel devices, the threshold is a function of the length (for low V_{DS})
  - In short-channel devices, there is a drain-induced threshold barrier lowering at the upper end of the V_{DS} range (for low L)
- Parasitic resistances
  - resistances associated with the source and drain contacts



- Latch-up

Subthreshold Conductance



$I_D \sim I_S e^{(qV_{GS}/nkT)}$ where $n \geq 1$

- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature

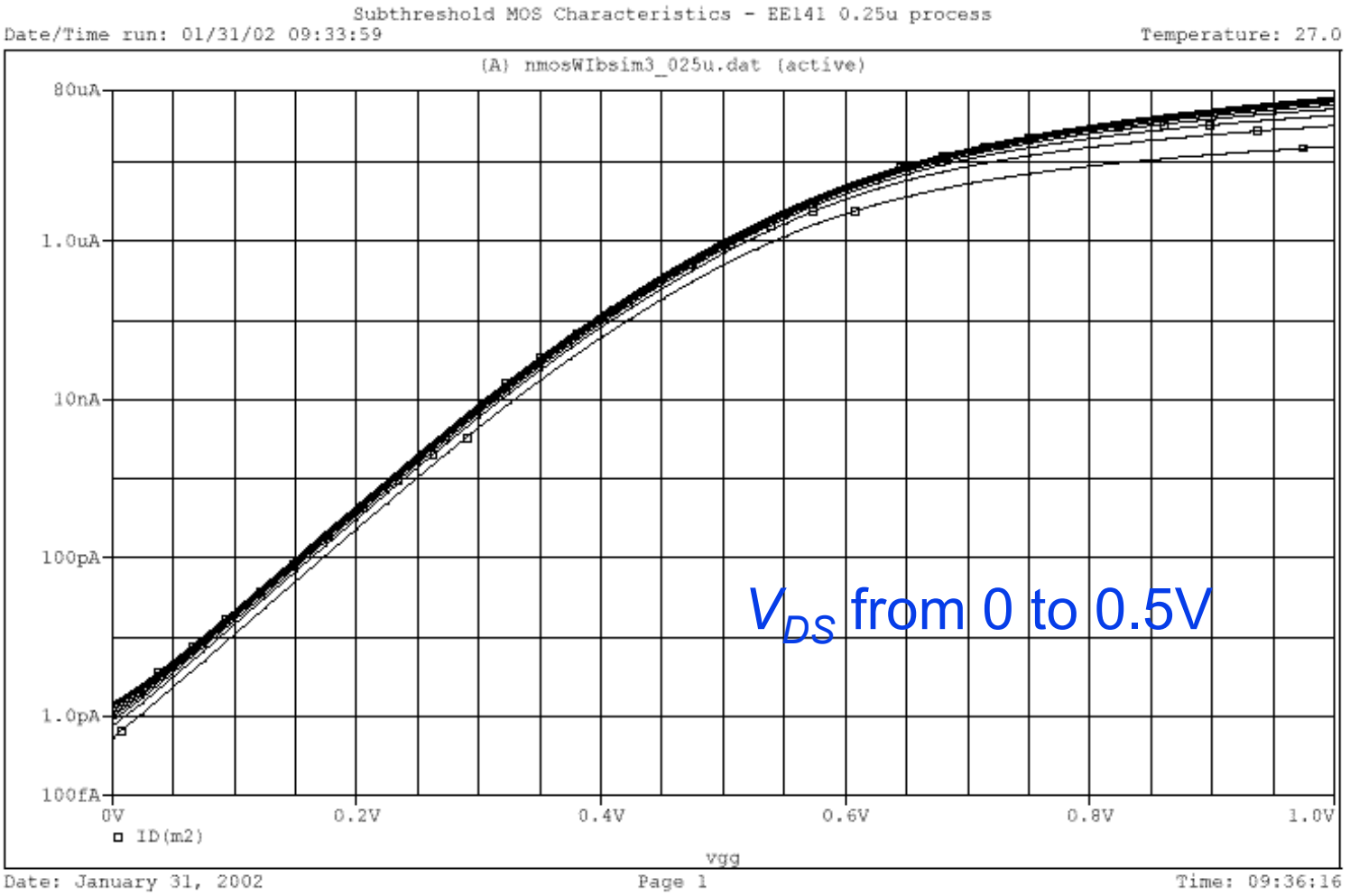
$$S = n\,(kT/q)\,\ln(10)$$

(typical values 60 to 100 mV/decade)

- Has repercussions in dynamic circuits and for power consumption

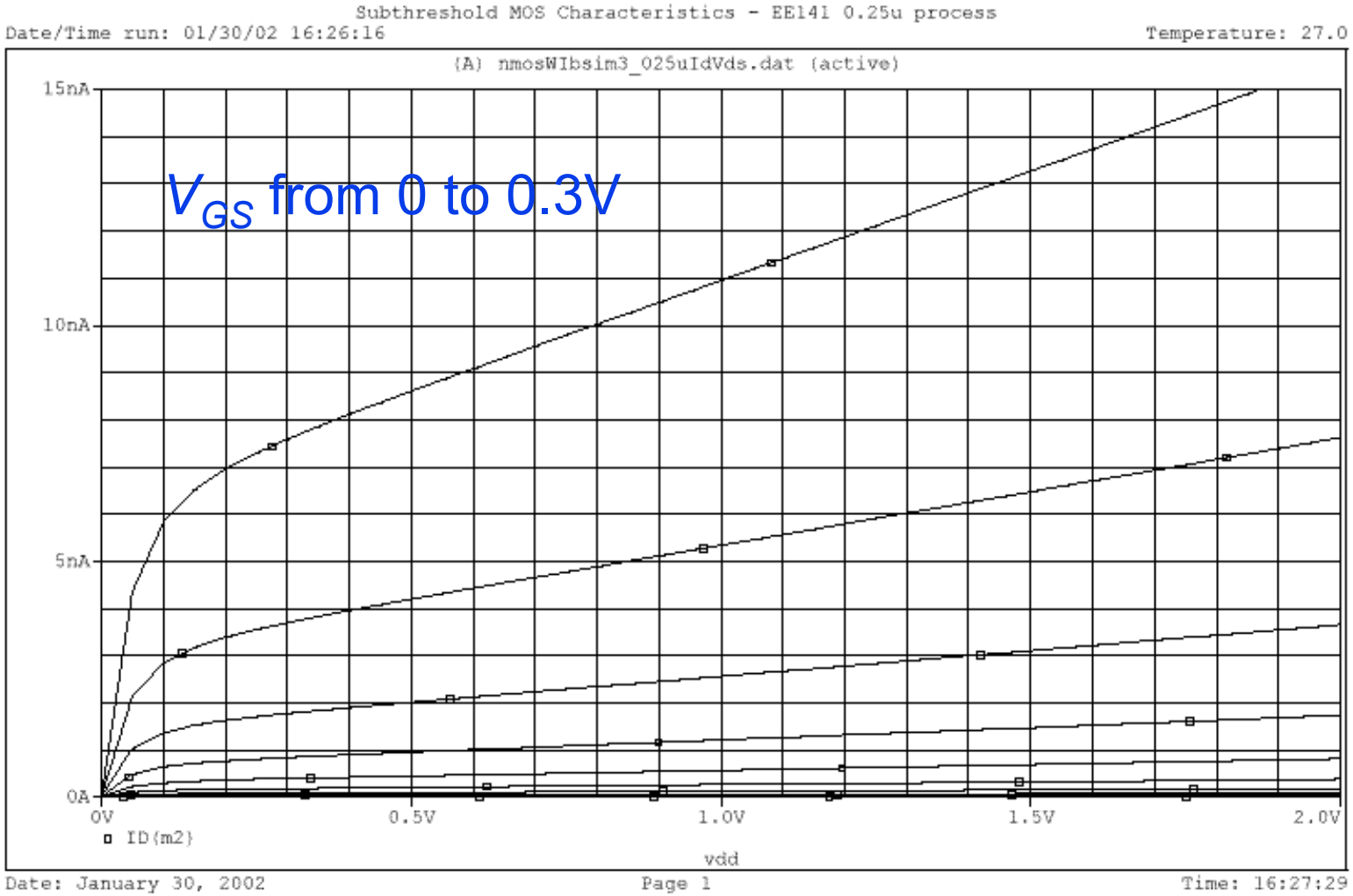
Subthreshold I_D vs V_{GS}

$$I_D = I_S\, e^{(qV_{GS}/nkT)}\,(1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$



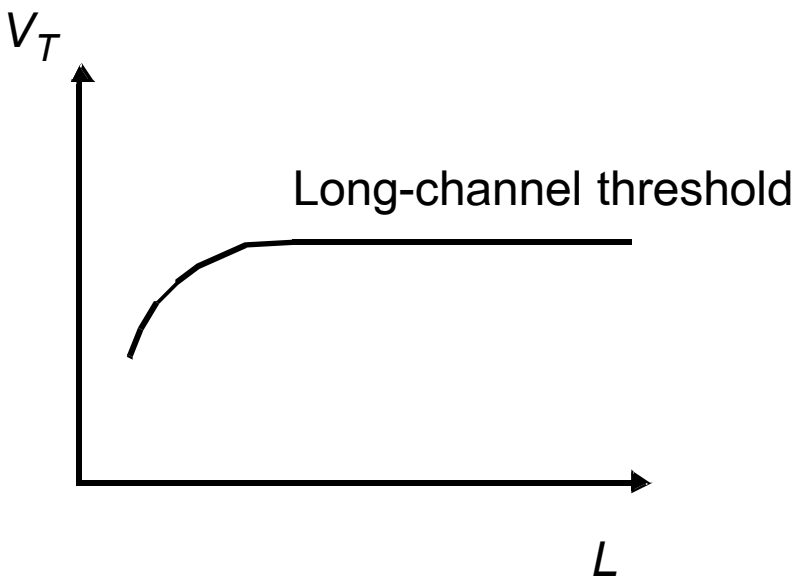
Subthreshold I_D vs V_{DS}

$$I_D = I_S\, e^{(qV_{GS}/nkT)}\,(1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$

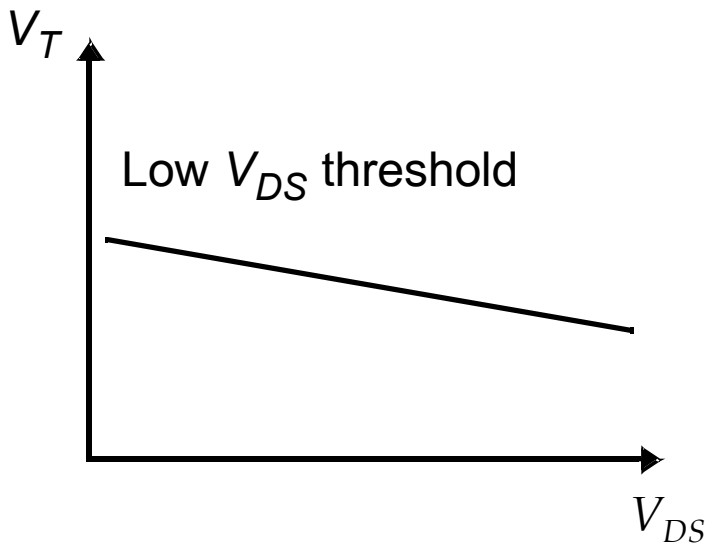


V_{GS} from 0 to 0.3V

Threshold Variations

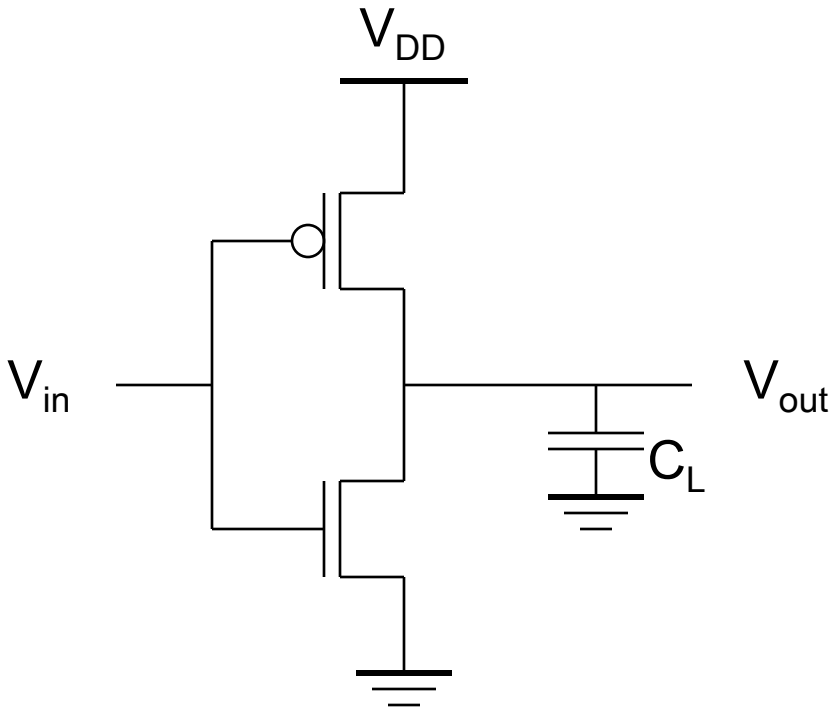


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Next Time: The CMOS Inverter



Next Lecture and Reminders

- Next lecture
  - CMOS inverter – a static view
    - Reading assignment – Rabaey, et al, 5.1-5.3

- Reminders
  - HW1 due September 10th (one week)
  - Project Title due September 12th (one week from Thursday)
  - Evening midterm exam scheduled
    - Wednesday, October 10th from 8:15 to 10:15pm in 260 Willard