CSE477
VLSI Digital Circuits
Fall 2002

Lecture 01: Introduction

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[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Course Contents

- Introduction to digital integrated circuits
  - CMOS devices and manufacturing technology. CMOS logic gates and their layout. Propagation delay, noise margins, and power dissipation. Combinational (e.g., arithmetic) and sequential circuit design. Memory design.
- Course goals
  - Ability to design and implement CMOS digital circuits and optimize them with respect to different constraints: size (cost), speed, power dissipation, and reliability
- Course prerequisites
  - EE 310. Electronic Circuit Design
  - CSE 471. Logic Design of Digital Systems

Course Administration

- Instructor: Mary Jane Irwin
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  227 Pond Lab
  Office Hrs: M 13:30-14:45 & R 9:30-10:45
- TA: Vijay Degalahal
  degalaha@cse.psu.edu
  225 Pond Lab
  Office Hrs: W & R 17:30 to 19:30 in 101 Pond
- Labs: Accounts on 101 Pond Lab machines
- URL: www.cse.psu.edu/~cg477
- Text: *Digital Integrated Circuits*, 2nd Edition
  Rabaey et. al., ©2002 (prerelease of the first nine chapters at the Penn State Bookstore)
  Lecture slides (pdf) – on the web

Grading Information

- Grade determinates
  - Midterm Exam ~25%
    - Wednesday, October 16th , 20:15 to 22:15, 260 Willard
  - Final Exam ~25%
    - Monday, December 16th, 10:10 to noon, Location TBD
  - Homeworks/Lab Assignments (5) ~20%
    - Due at the beginning of class (or, if submitted electronically, by 17:00 on the due date). No late assignments will be accepted.
  - Design Project (teams of ~2) ~25%
  - In-class pop quizzes ~ 5%
- Please let me know about exam conflicts ASAP
- Grades will be posted on the course homepage
  - Must submit email request for change of grade after discussions with the TA (Homeworks/Lab Assignments) or instructor (Exams)
  - December 10th deadline for filing grade corrections; no requests for grade changes will be accepted after this date

Background from CSE471 and EE310

- Basic circuit theory
  - resistance, capacitance, inductance
  - MOS gate characteristics
- Hardware description language
  - VHDL or verilog
- Use of modern EDA tools
  - simulation, synthesis, validation (Synopsys)
  - schematic capture tools (LogicWorks)
- Logic design
  - logical minimization, FSMs, component design

Course Structure

- Design and tool intensive class
  - Micromagic (MMI) “max” and “sue” for layout
    - Online documentation and tutorials
  - HSPICE for circuit simulation
- Lectures:
  - 2 weeks on the CMOS inverter
  - 3 weeks on static and dynamic CMOS gates
  - 2 weeks on C, R, and L effects
  - 2 week on sequential CMOS circuits
  - 2 weeks on design of datapath structures
  - 2 weeks on memory design
  - 1 week on design for test, margining, scaling, trends
  - 1 week exams

"Executives might make the final decisions about what would be produced, but engineers would provide most of the ideas for new products. After all, engineers were the people who really knew the state of the art and who were therefore best equipped to prophesy changes in it."

The Soul of a New Machine, Kidder, pg 35

Transistor Revolution

- Transistor –Bardeen (Bell Labs) in 1947
- Bipolar transistor – Schockley in 1949
- First bipolar digital logic gate – Harris in 1956
- First monolithic IC – Jack Kilby in 1959
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990's
- ECL – 1974 into the 1980's

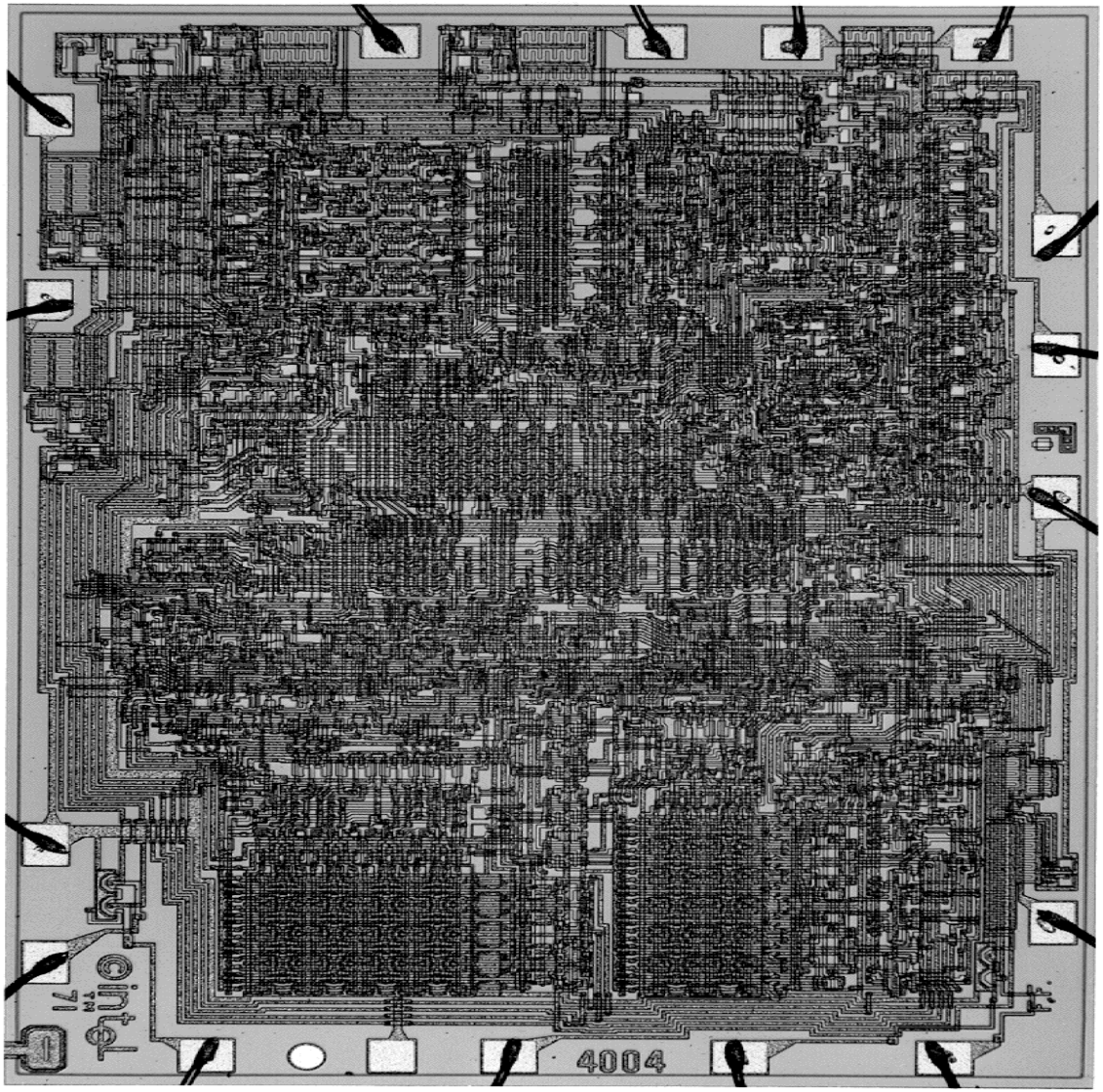
MOSFET Technology

- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, but plagued with manufacturing problems
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – preferred MOSFET technology because of power benefits
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI, Copper-Low K, …

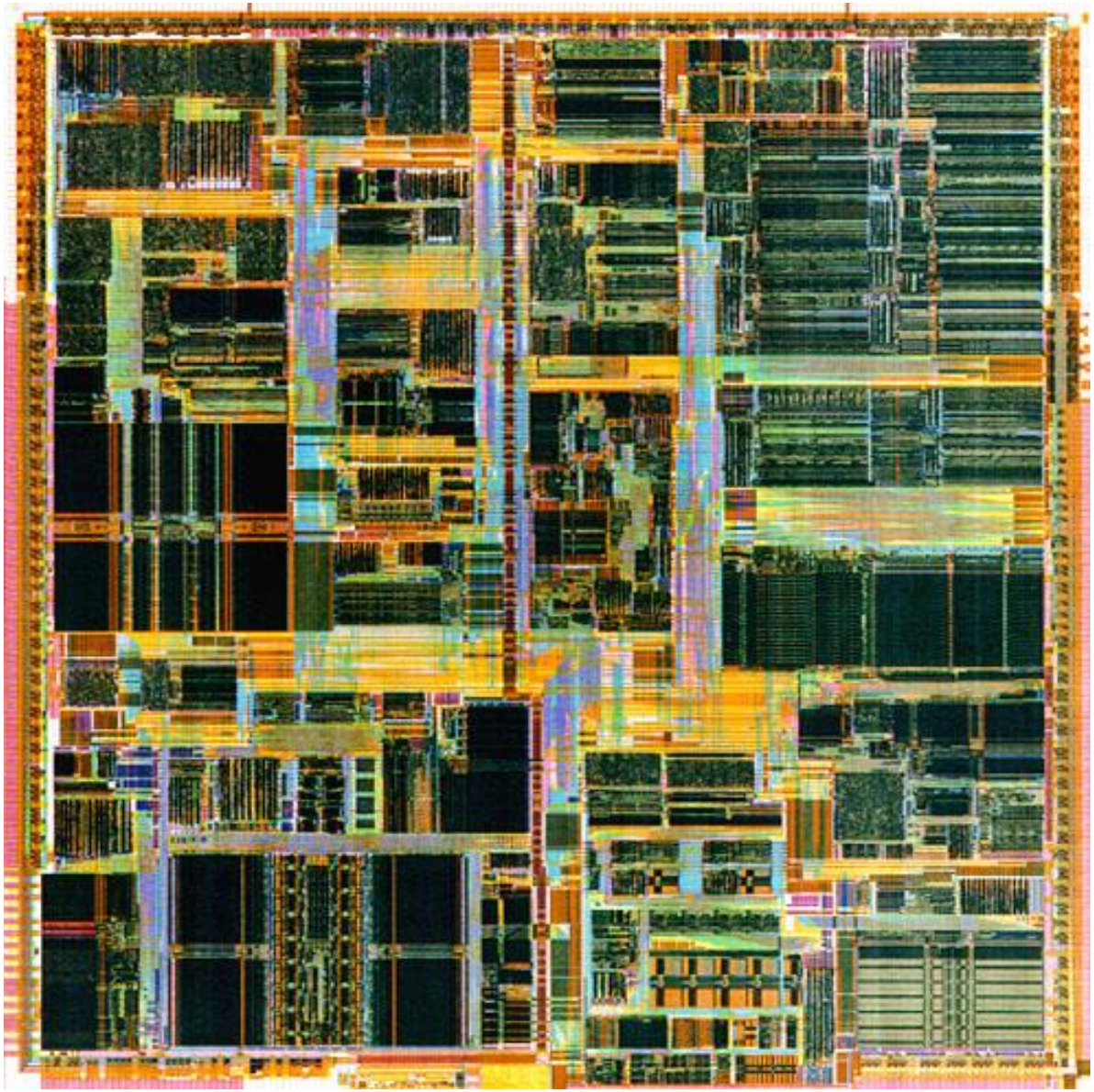
Moore's Law

- In 1965, Gordon Moore predicted that the number of transistors that can be integrated on a die would double every 18 to 14 months (i.e., grow exponentially with time).
- Amazingly visionary – million transistor/chip barrier was crossed in the 1980's.
  - 2300 transistors, 1 MHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

Intel 4004 Microprocessor



Intel Pentium (IV) Microprocessor

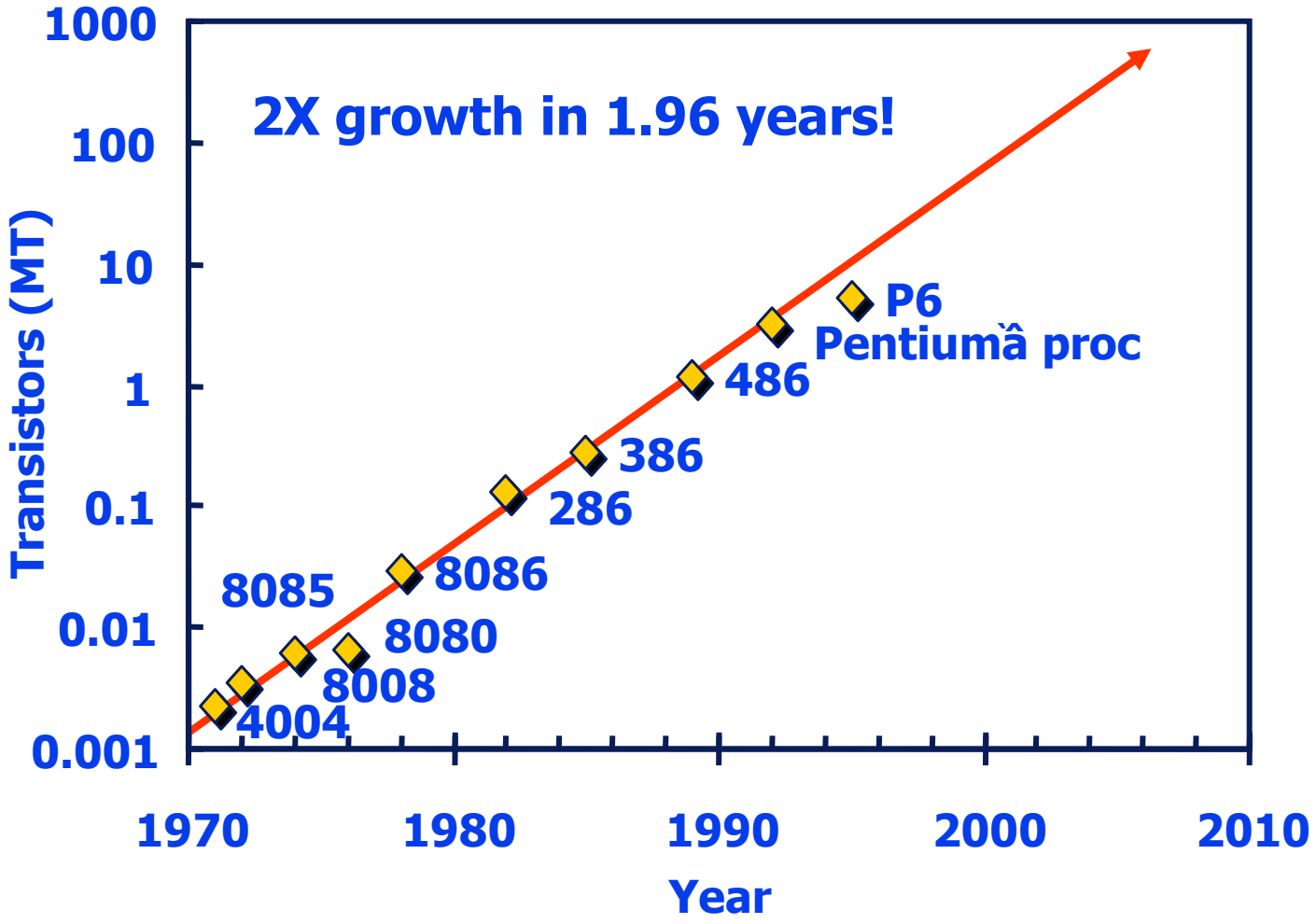


State-of-the Art: Lead Microprocessors

Processor	Alpha 21264B	AMD Athlon	HP PA-8600	IBM Power3-II	Intel Pentium III	Intel Pentium 4	MIPS R12000	Sun Ultra-II	Sun Ultra-III
Clock Rate	833MHz	1.33GHz	552MHz	450MHz	1.0GHz	1.7GHz	400MHz	480MHz	900MHz
Cache (I/D/L2)	64K/64K	64K/64K/256K	512K/1M	32K/64K	16K/16K/256K	12K/8K/256K	32K/32K	16K/16K	32K/64K
Issue Rate	4 issue	3 x86 instr	4 issue	4 issue	3 x86 instr	3 ROPs	4 issue	4 issue	4 issue
Pipeline Stages	7/9 stages	9/11 stages	7/9 stages	7/8 stages	12/14 stages	22/24 stages	6 stages	6/9 stages	14/15 stages
Out of Order	80 instr	72ROPs	56 instr	32 instr	40 ROPs	126 ROPs	48 instr	None	None
Rename regs	48/41	36/36	56 total	16 int/24 fp	40 total	128 total	32/32	None	None
BHT Entries	4K x 9 bits	4K x 2 bits	2K x 2 bits	2K x 2 bits	≥ 512	4K x 2 bits	2K x 2 bits	512 x 2 bits	16K x 2 bits
TLB Entries	128/128	280/288	120 unified	128/128	32I/64D	128I/64D	64 unified	64I/64D	128I/512D
Memory B/W	2.66GB/s	2.1GB/s	1.54GB/s	1.6GB/s	1.06GB/s	3.2GB/s	539 MB/s	1.9GB/s	4.8GB/s
Package	CPGA-588	PGA-462	LGA-544	SCC-1088	PGA-370	PGA-423	CPGA-527	CLGA-787	1368 FC-LGA
IC Process	0.18µ 6M	0.18µ 6M	0.25µ 2M	0.22µ 6M	0.18µ 6M	0.18µ 6M	0.25µ 4M	0.29µ 6M	0.18µ 7M
Die Size	115mm^2	117mm^2	477mm^2	163mm^2	106mm^2	217mm^2	204mm^2	126mm^2	210mm^2
Transistors	15.4 million	37 million	130 million	23 million	24 million	42 million	7.2 million	3.8 million	29 million
Est mfg cost	$160	$62	$330	$110	$39	$100	$125	$70	$145
Power (max)	75W*	76W	60W*	36W*	30W	64W(TDP)	25W*	20W*	65W
Availability	1Q01	1Q01	3Q00	4Q00	2Q00	2Q01	2Q00	3Q0	4Q00

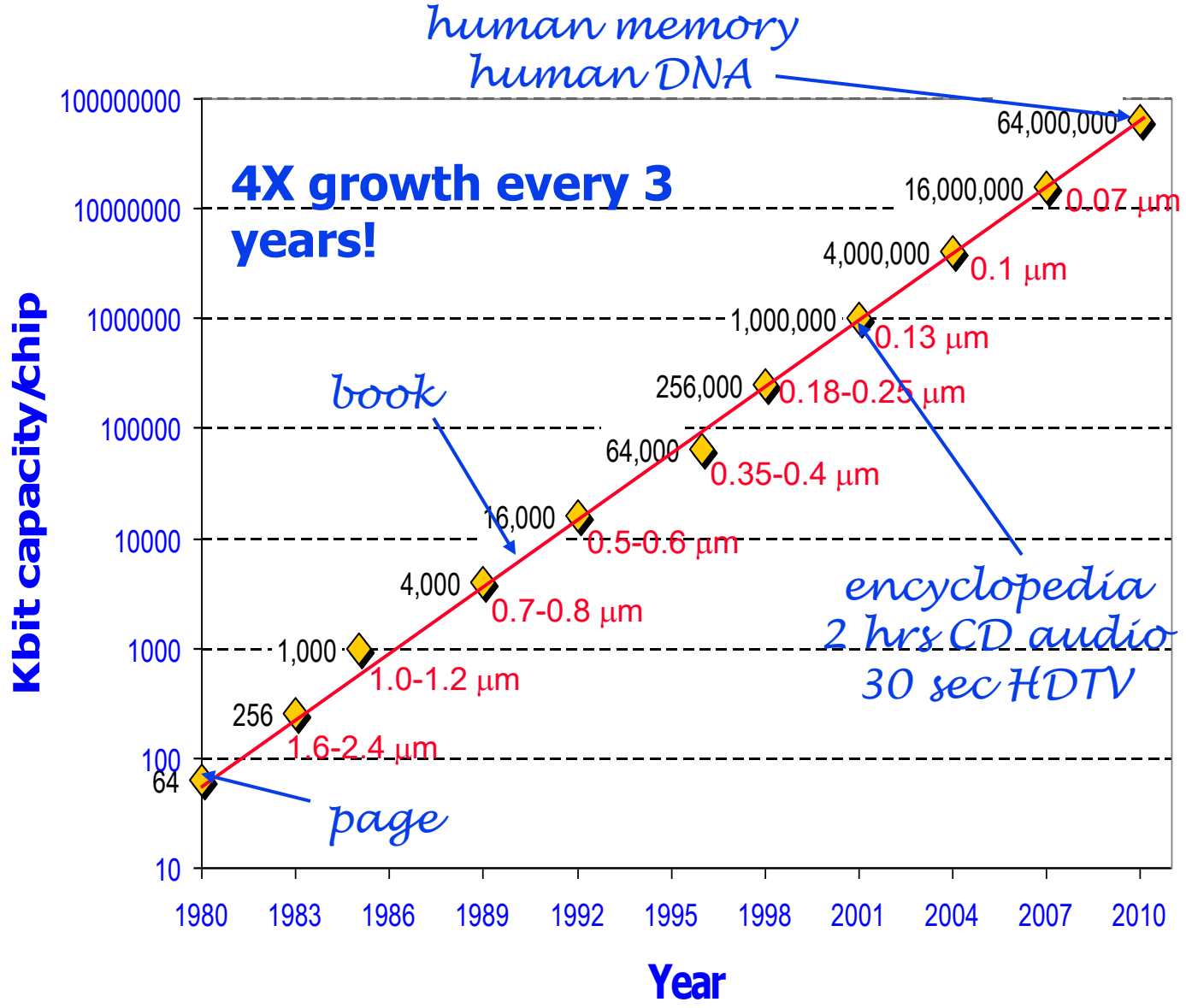
Moore's Law in Microprocessors

Transistors on lead microprocessors double every 2 years



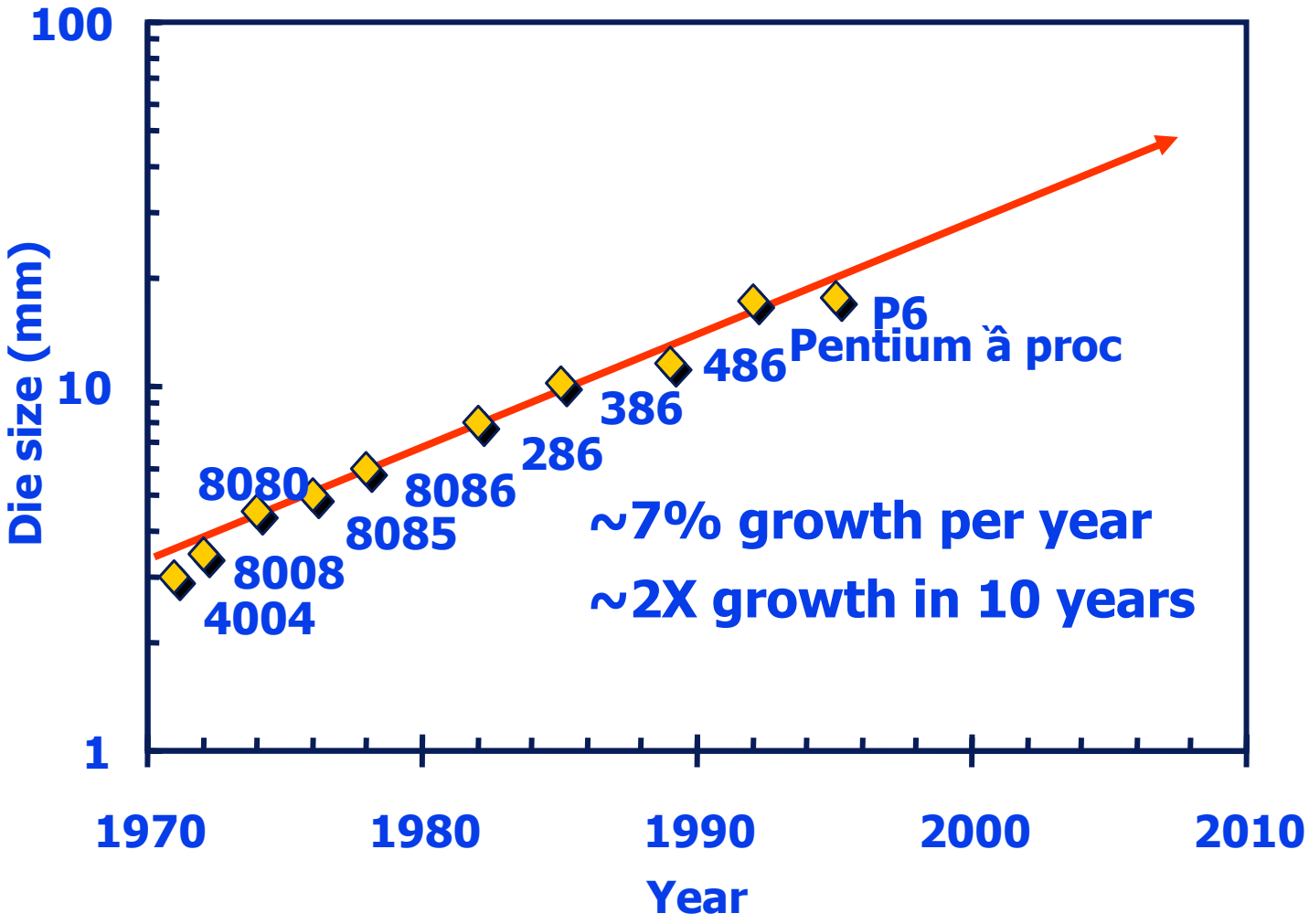
Courtesy, Intel

Evolution in DRAM Chip Capacity



Die Size Growth

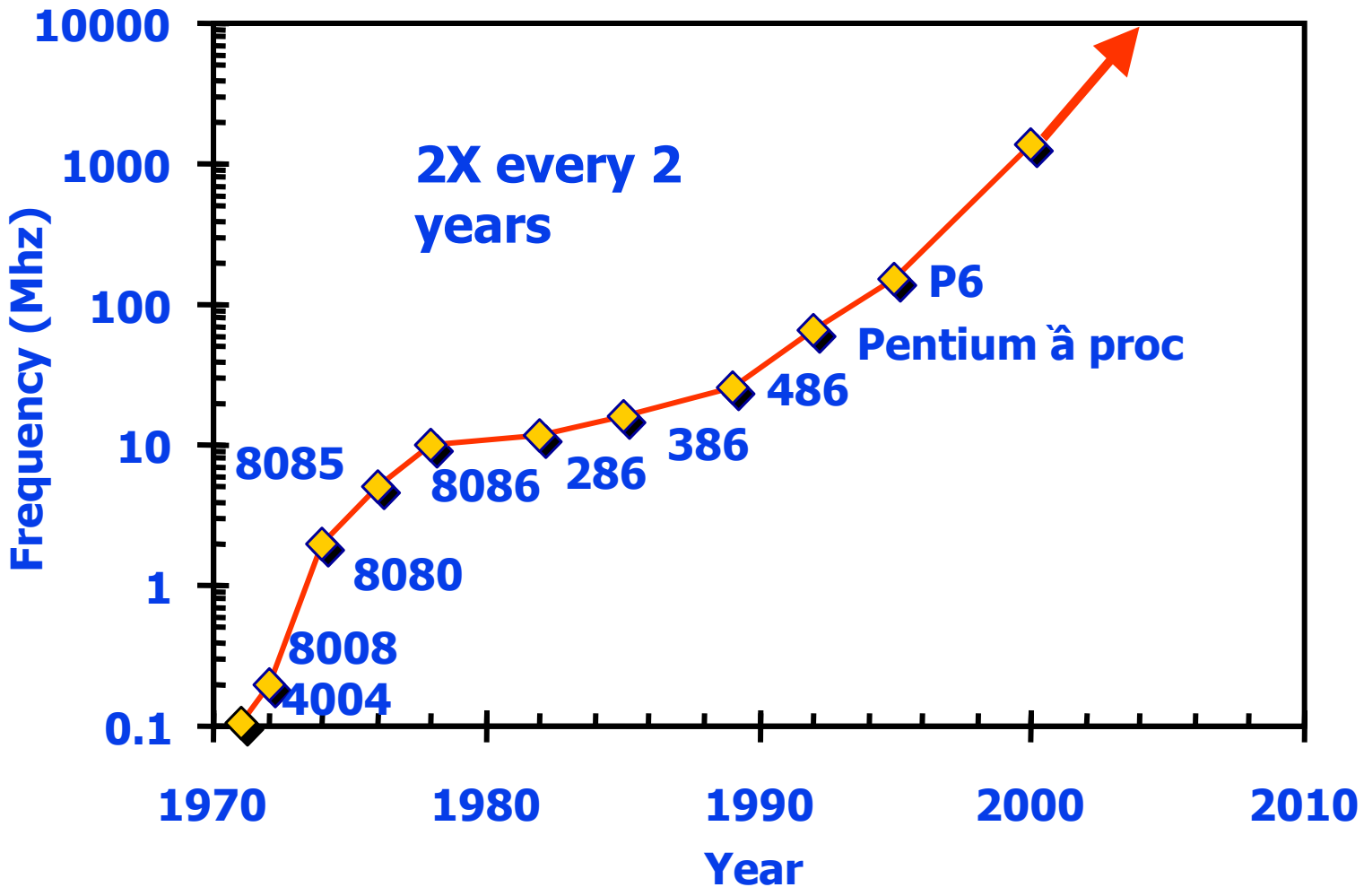
Die size grows by 14% to satisfy Moore's Law



Courtesy, Intel

Clock Frequency

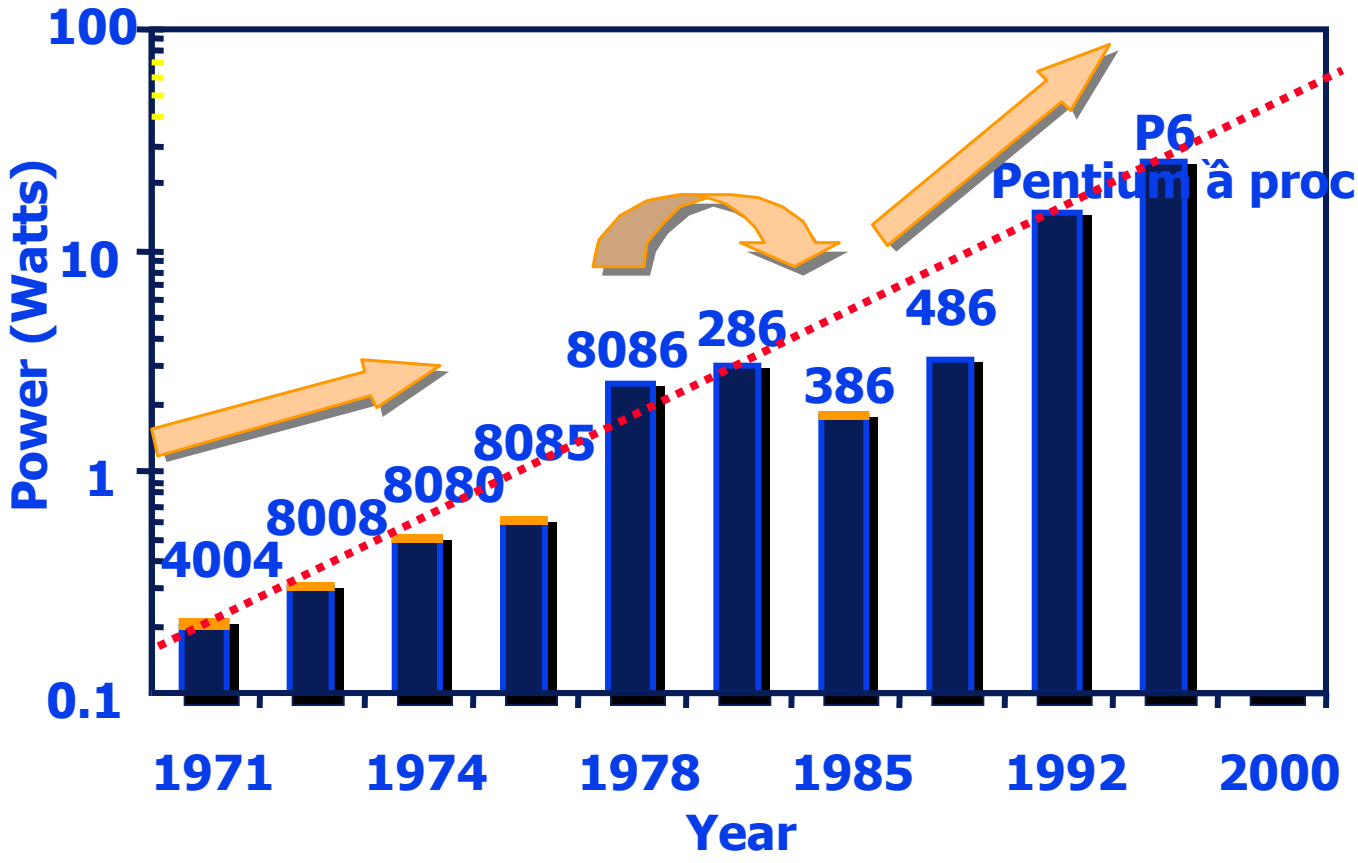
Lead microprocessors frequency doubles every 2 years



Courtesy, Intel

Power Dissipation

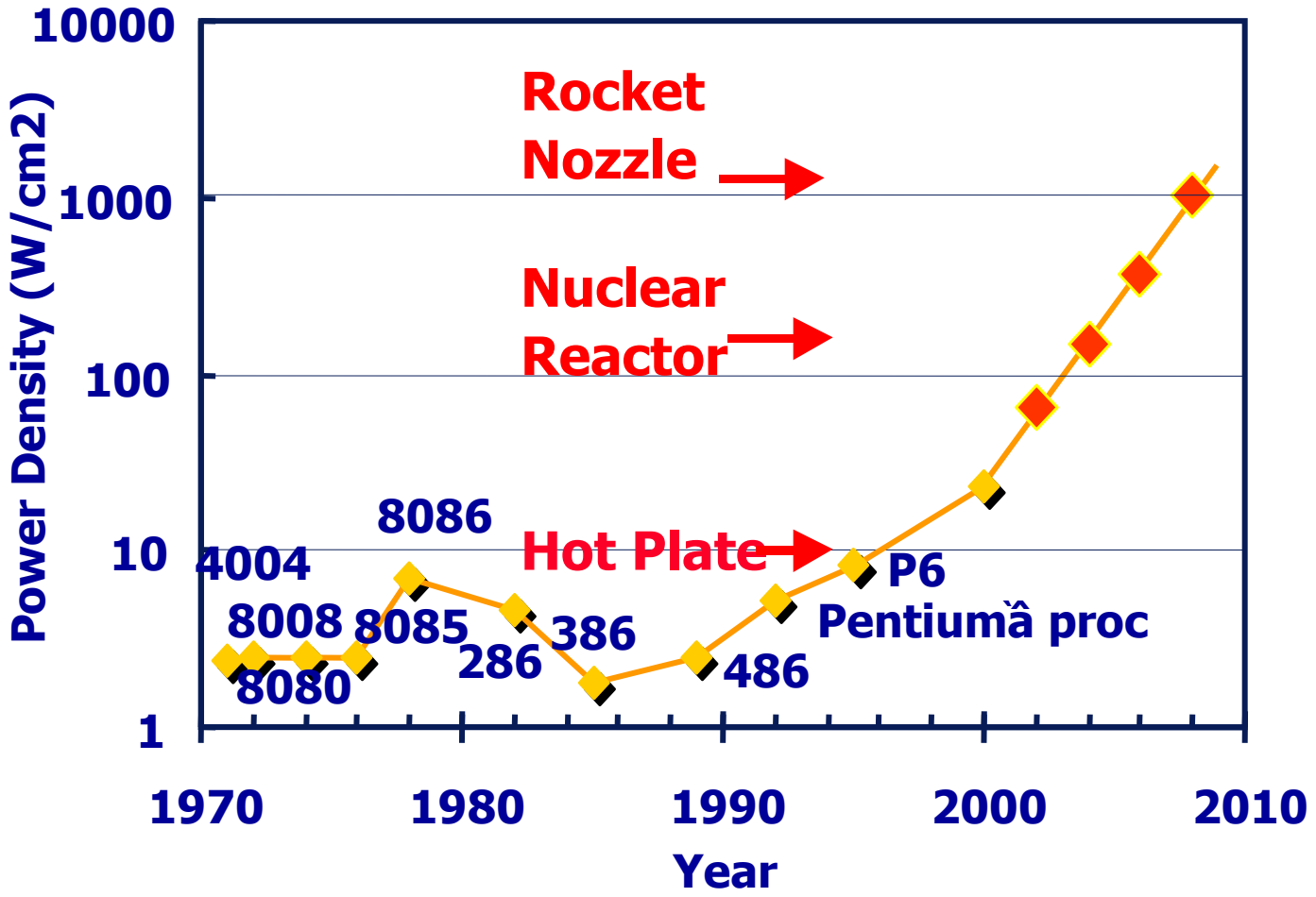
Lead Microprocessors power continues to increase



Power delivery and dissipation will be prohibitive

Courtesy, Intel

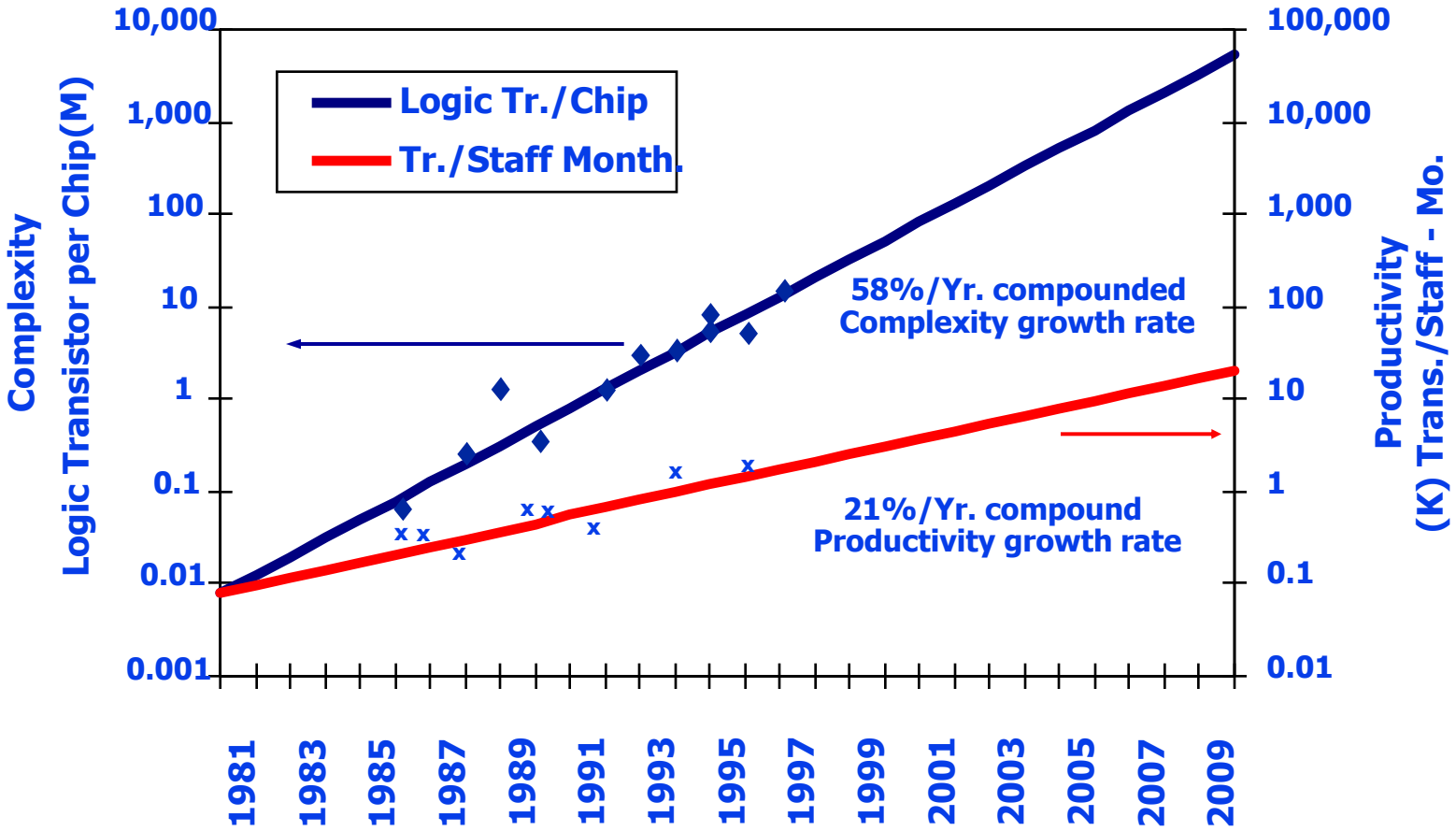
Power Density



Power density too high to keep junctions at low temp

Courtesy, Intel

Design Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Technology Directions: SIA Roadmap

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Mtrans/cm^2	7	14-26	47	115	284	701
Chip size (mm^2)	170	170-214	235	269	308	354
Signal pins/chip	768	1024	1024	1280	1408	1472
Clock rate (MHz)	600	800	1100	1400	1800	2200
Wiring levels	6-7	7-8	8-9	9	9-10	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.6
High-perf power (W)	90	130	160	170	174	183
Battery power (W)	1.4	2.0	2.4	2.0	2.2	2.4

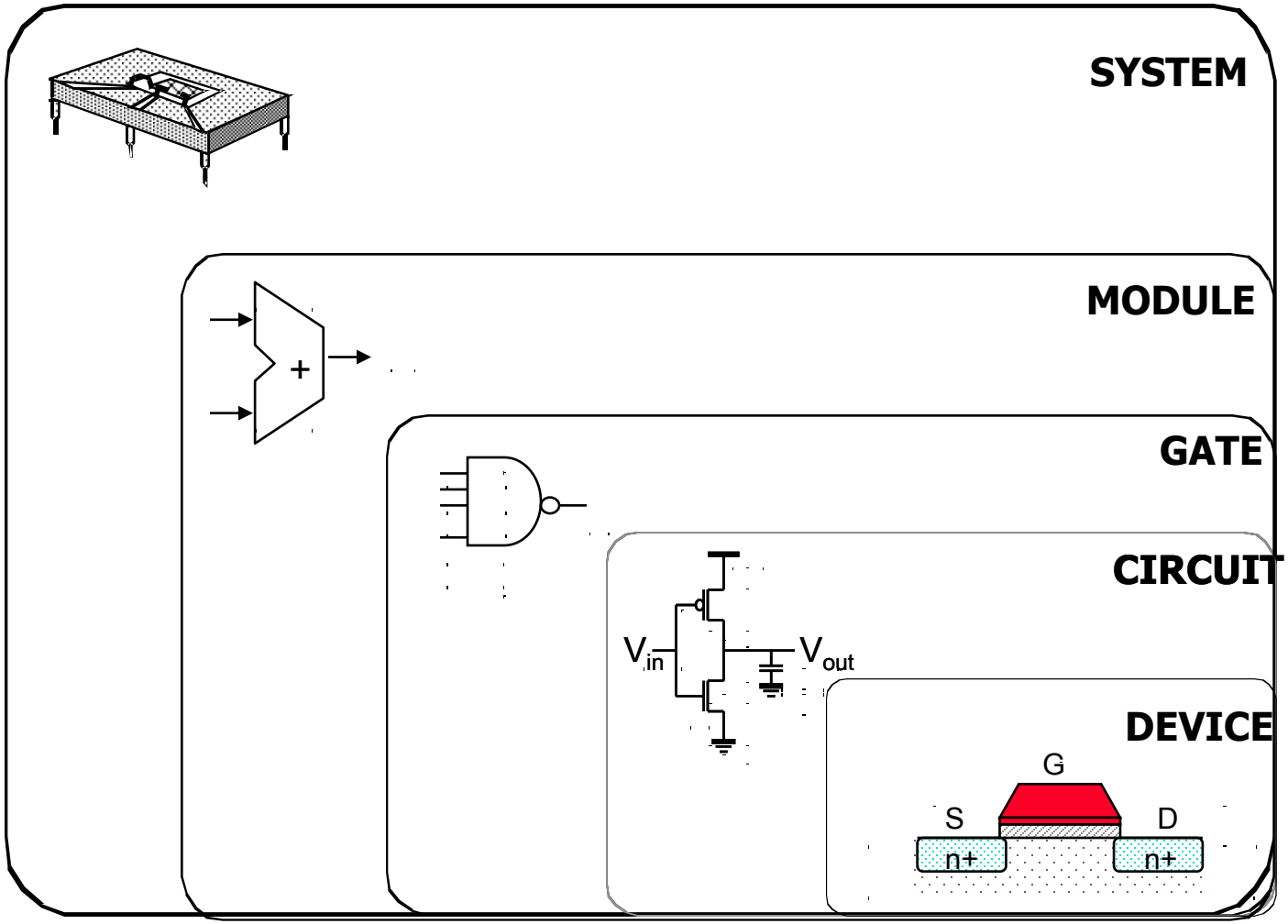
For Cost-Performance MPU (L1 on-chip SRAM cache; 32KB/1999 doubling every two years)

http://www.itrs.net/ntrs/publntrs.nsf

Why Scaling?

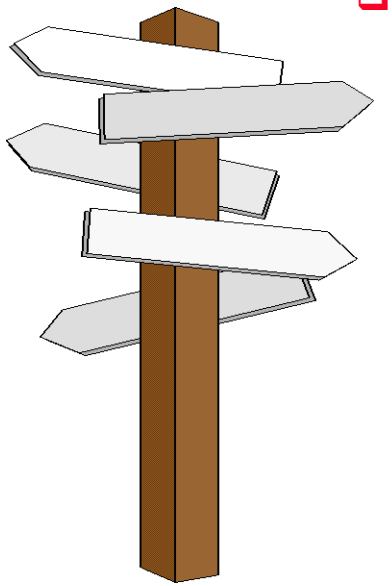
- Technology shrinks by ~0.7 per generation
- With every generation can integrate 2x more functions on a chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels



Major Design Challenges

- Microscopic issues
  - ultra-high speeds
  - power dissipation and supply rail drop
  - growing importance of interconnect
  - noise, crosstalk
  - reliability, manufacturability
  - clock distribution



- Macroscopic issues
  - time-to-market
  - design complexity (millions of gates)
  - high levels of abstractions
  - reuse and IP, portability
  - systems on a chip (SoC)
  - tool interoperability

Year	Tech.	Complexity	Frequency	3 Yr. Design Staff Size	Staff Costs
1997	0.35	13 M Tr.	400 MHz	210	$90 M
1998	0.25	20 M Tr.	500 MHz	270	$120 M
1999	0.18	32 M Tr.	600 MHz	360	$160 M
2002	0.13	130 M Tr.	800 MHz	800	$360 M

Next Lecture and Reminders

- Next lecture
  - Design metrics
    - Reading assignment – 1.3

- Reminders
  - Hands on max tutorial
    - Thursday evening from 7:00 to 9:00 pm in 101 Pond Lab
  - HW1 due September 10th
  - Evening midterm exam scheduled
    - Wednesday, October 16th , 20:15 to 22:15, 260 Willard
    - Please let me know ASAP (via email) if you have a conflict