CSE477
VLSI Digital Circuits
Fall 2002

Lecture 25: Peripheral Memory Circuits

Mary Jane Irwin (www.cse.psu.edu/~mji)
www.cse.psu.edu/~cg477

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]
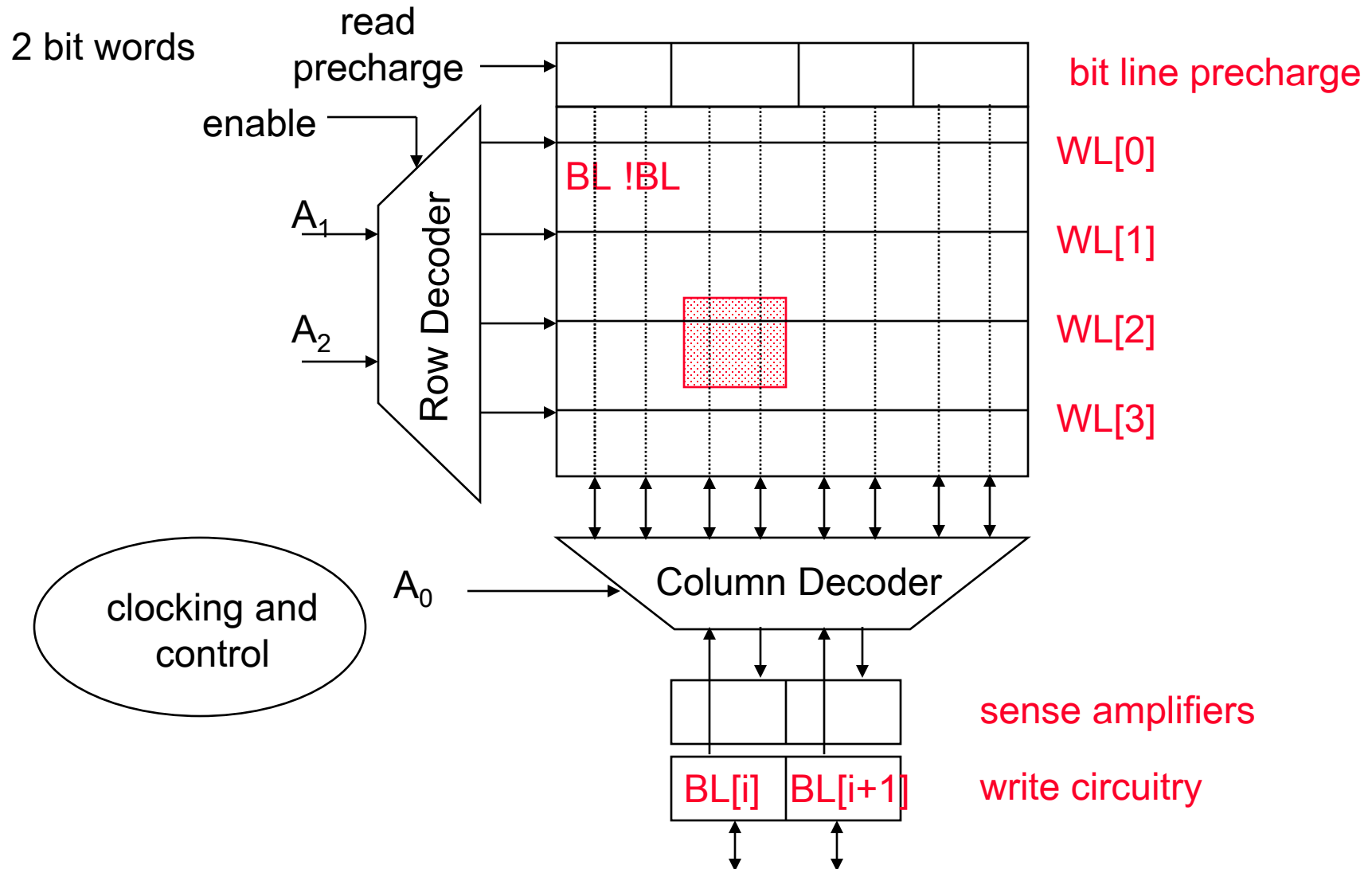
Review: Read-Write Memories (RAMs)

❑ Static – SRAM

  ❑ data is stored as long as supply is applied

  ❑ large cells (6 fets/cell) – so fewer bits/chip

  ❑ fast – so used where speed is important (e.g., caches)

  ❑ differential outputs (output BL and !BL)

  ❑ use sense amps for performance

  ❑ compatible with CMOS technology

❑ Dynamic – DRAM

  ❑ periodic refresh required

  ❑ small cells (1 to 3 fets/cell) – so more bits/chip

  ❑ slower – so used for main memories

  ❑ single ended output (output BL only)

  ❑ need sense amps for correct operation

  ❑ not typically compatible with CMOS technology

Review: 4x4 SRAM Memory

2 bit words

read precharge

bit line precharge

enable

BL !BL

WL[0]

A_1

Row Decoder

WL[1]

A_2

WL[2]

WL[3]

clocking and control

A_0

Column Decoder

sense amplifiers

BL[i] BL[i+1]

write circuitry

Peripheral Memory Circuitry

- ❑ Row and column decoders

- ❑ Sense amplifiers

- ❑ Read/write circuitry

- ❑ Timing and control

Row Decoders

- ❏ Collection of 2^M complex logic gates organized in a regular, dense fashion

- ❏ (N)AND decoder

$$WL(0) = !A_9!A_8!A_7!A_6!A_5!A_4!A_3!A_2!A_1!A_0$$

$$\ldots$$
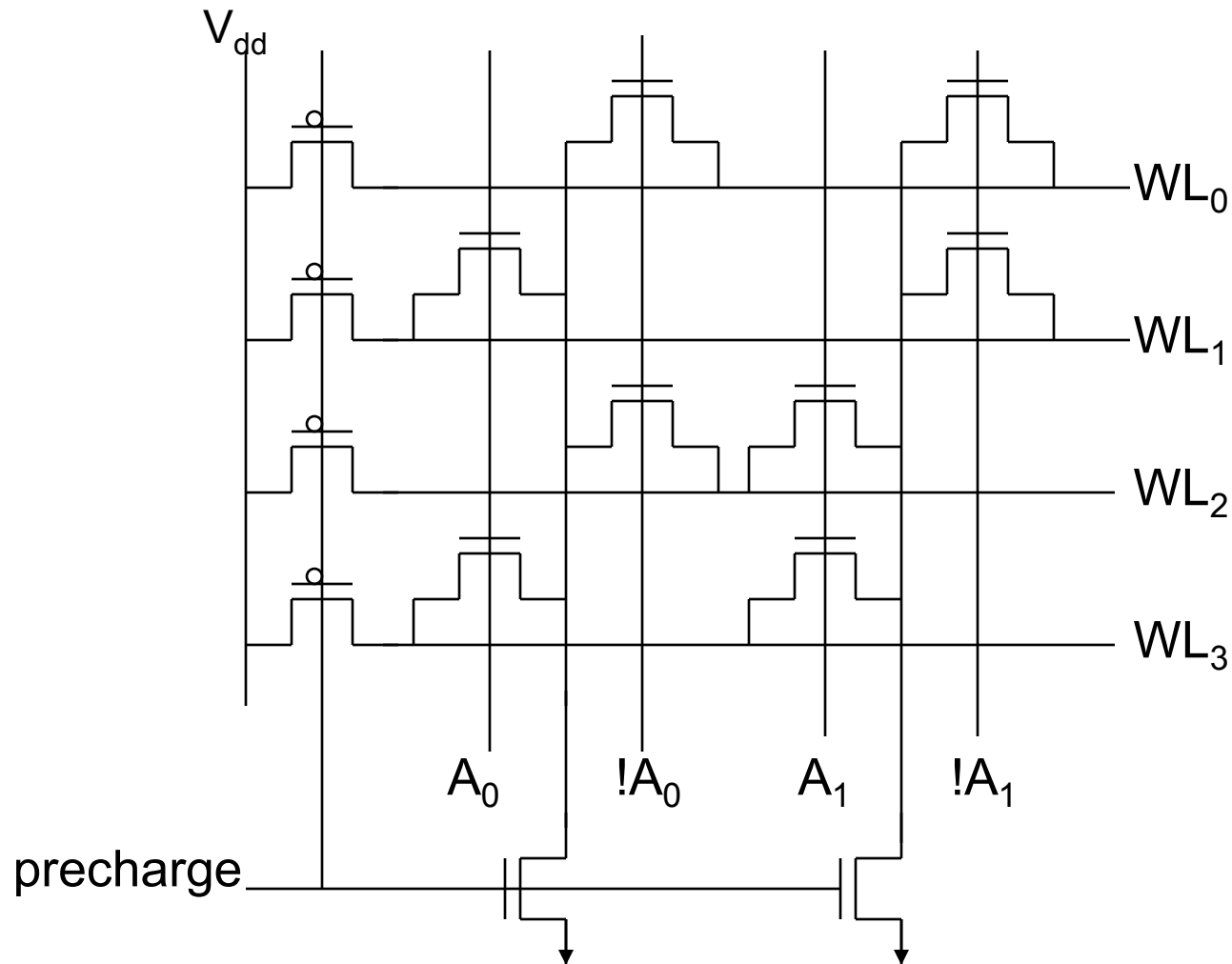
$$WL(511) = !A_9A_8A_7A_6A_5A_4A_3A_2A_1A_0$$

- ❏ NOR decoder

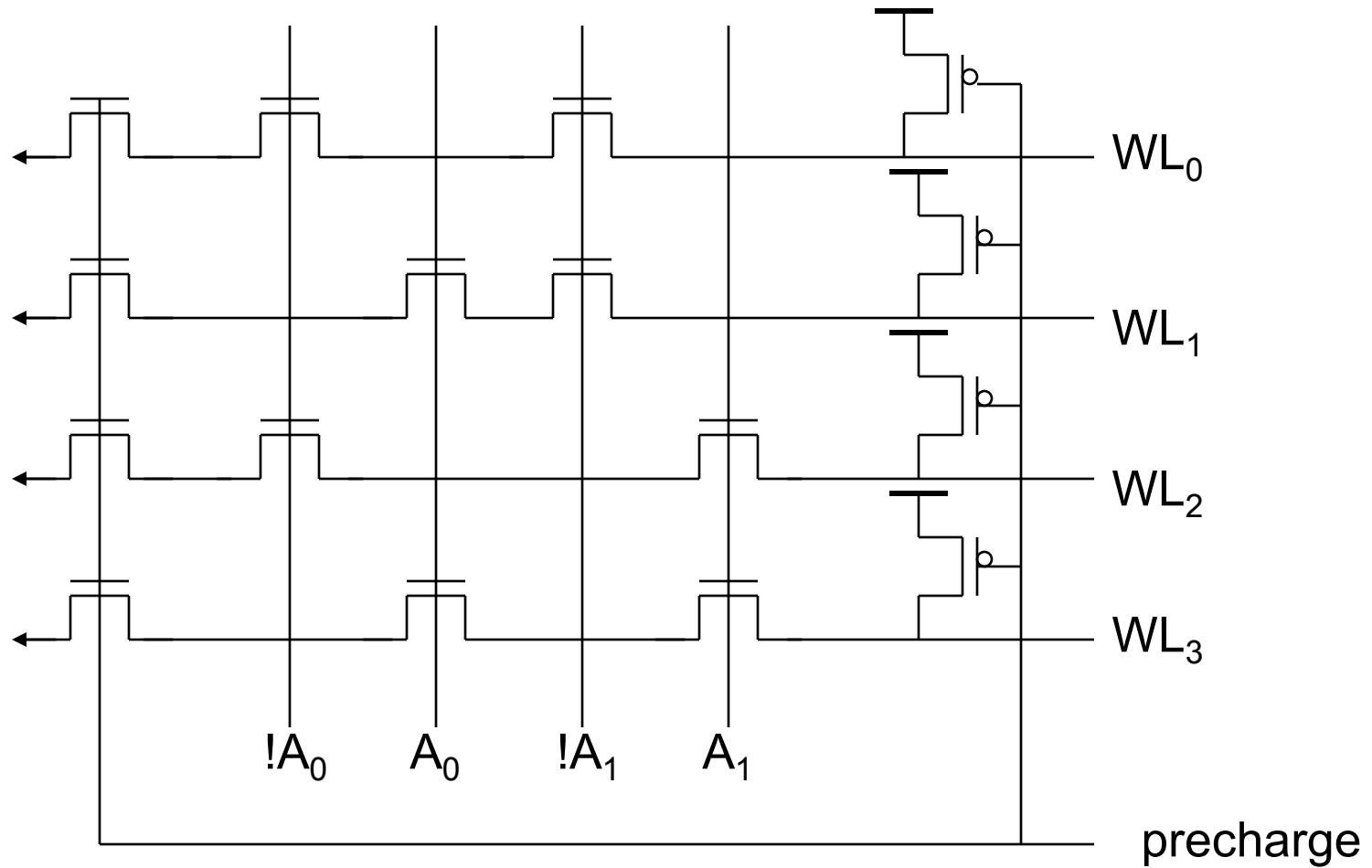$$WL(0) = !(A_9+A_8+A_7+A_6+A_5+A_4+A_3+A_2+A_1+A_0)$$

$$\ldots$$

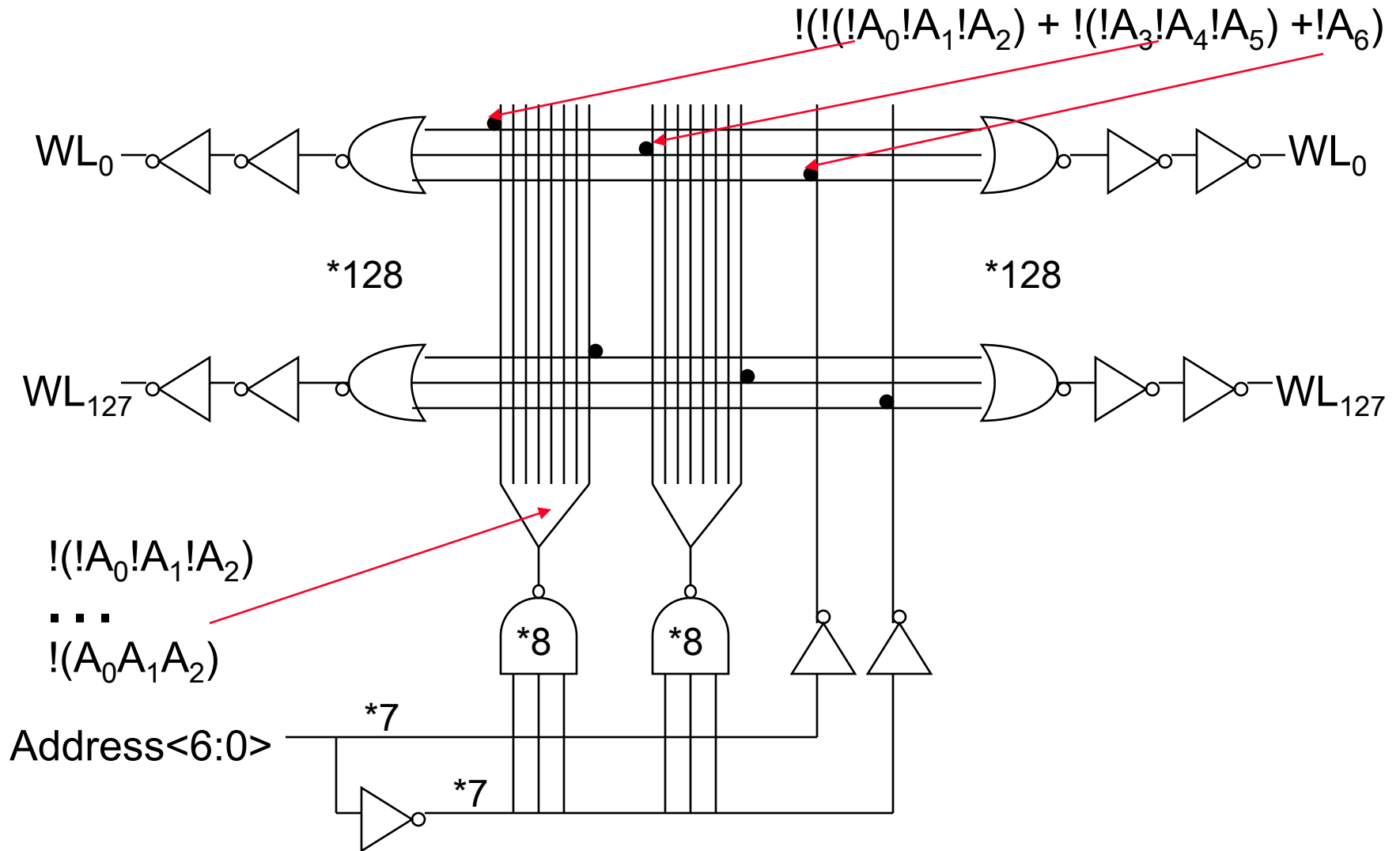$$WL(511) = !(A_9+!A_8+!A_7+!A_6+!A_5+!A_4+!A_3+!A_2+!A_1+!A_0)$$
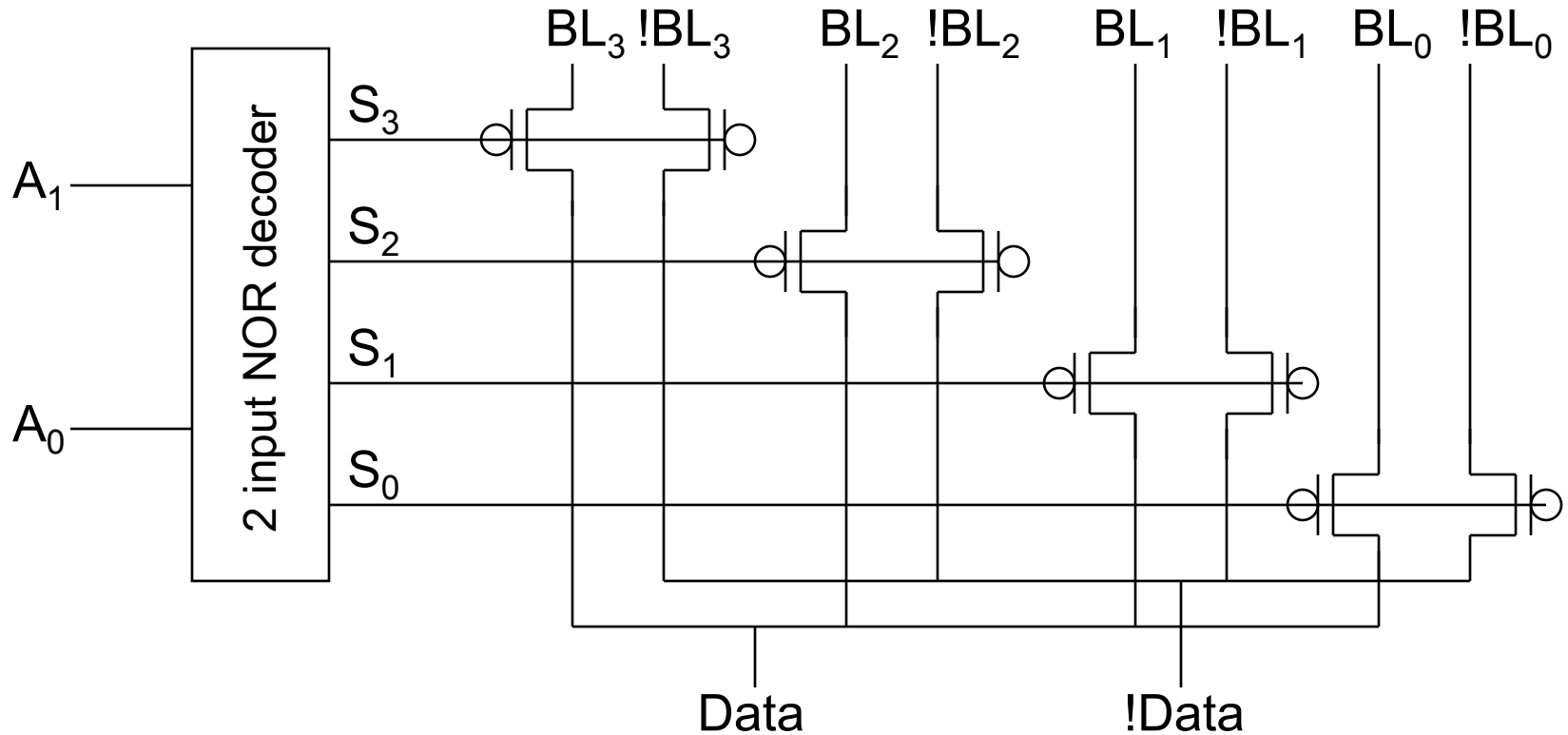
Dynamic NOR Row Decoder

Dynamic NAND Row Decoder

WL$_0$

WL$_1$

WL$_2$

WL$_3$

!A$_0$ A$_0$!A$_1$ A$_1$

precharge

Split Row Decoder

$!(!(!A_0!A_1!A_2) + !(!A_3!A_4!A_5) +!A_6)$

WL_0

*128

*128

WL_0

WL_{127}

WL_{127}

$!(!A_0!A_1!A_2)$
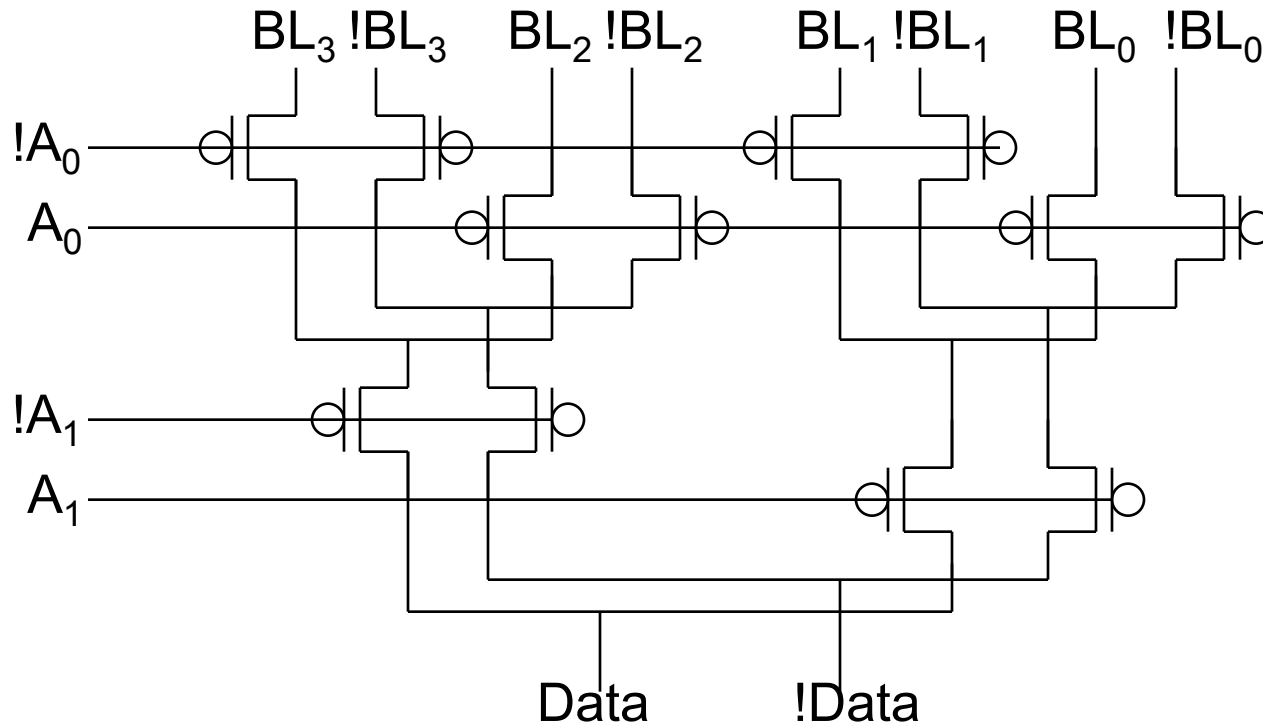. . .
$!(A_0A_1A_2)$

*8

*8

Address<6:0>

*7

*7

Pass Transistor Based Column Decoder

❑ Advantage: speed since there is only one extra transistor in the signal path
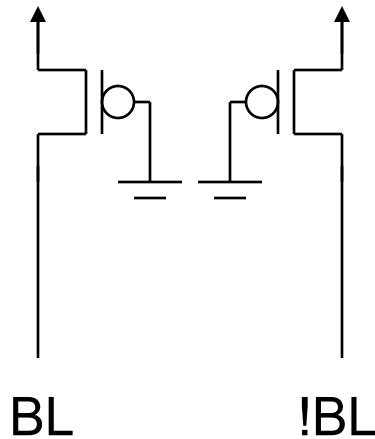
❑ Disadvantage: large transistor count

Tree Based Column Decoder

BL_3 $!BL_3$ BL_2 $!BL_2$ BL_1 $!BL_1$ BL_0 $!BL_0$
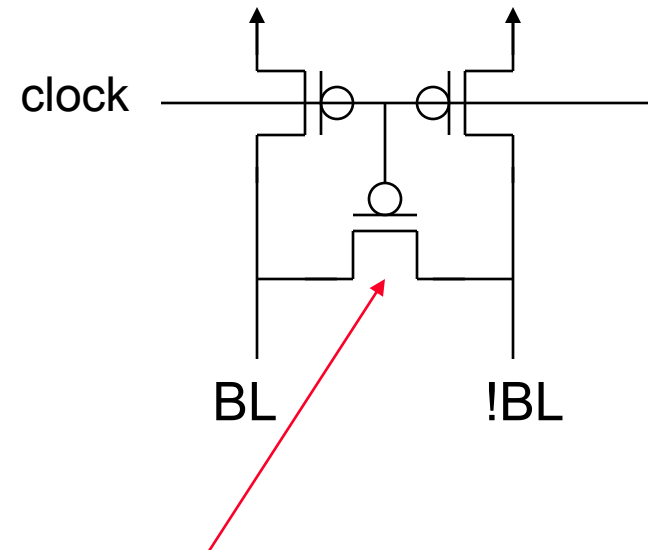
$!A_0$

A_0

$!A_1$

A_1

Data   !Data

- ❑ Advantage: number of transistors drastically reduced

- ❑ Disadvantage: delay increases quadratically with the number of sections (so prohibitive for large decoders)

  - • fix with buffers, progressive sizing, combination of tree and pass transistor approaches

Bit Line Precharging

Static Pull-up Precharge

Clocked Precharge

clock

BL   !BL

BL   !BL

equalization transistor - speeds up equalization of the two bit lines by allowing the capacitance and pull-up device of the nondischarged bit line to assist in precharging the discharged line
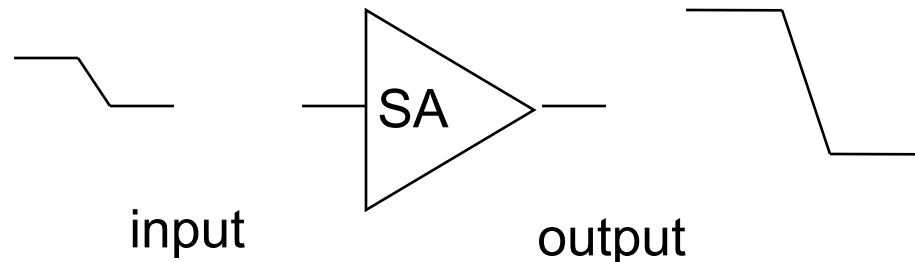
Sense Amplifiers
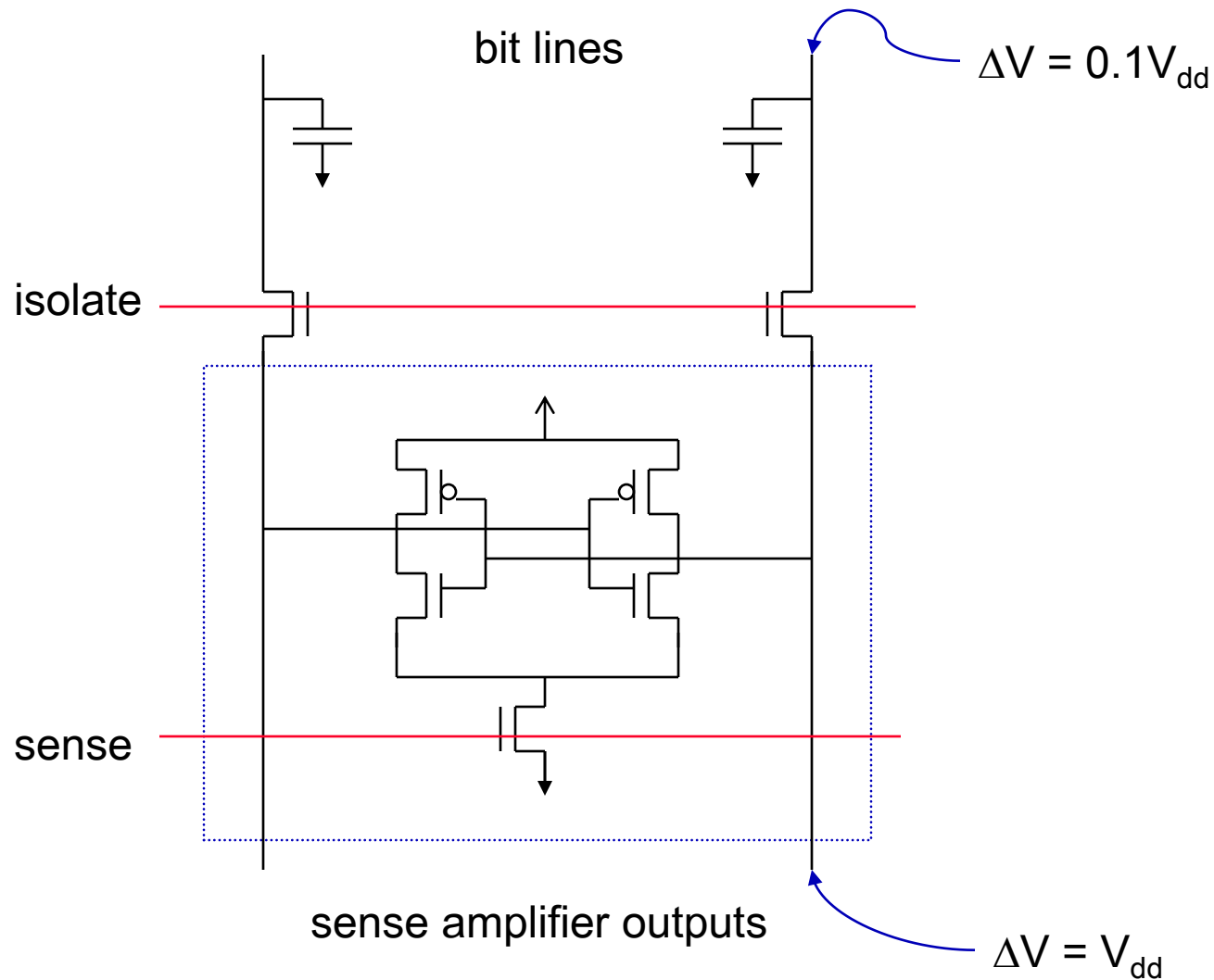
$$t_p = (C * \Delta V) / I_{av}$$

small

large

make ΔV as small as possible
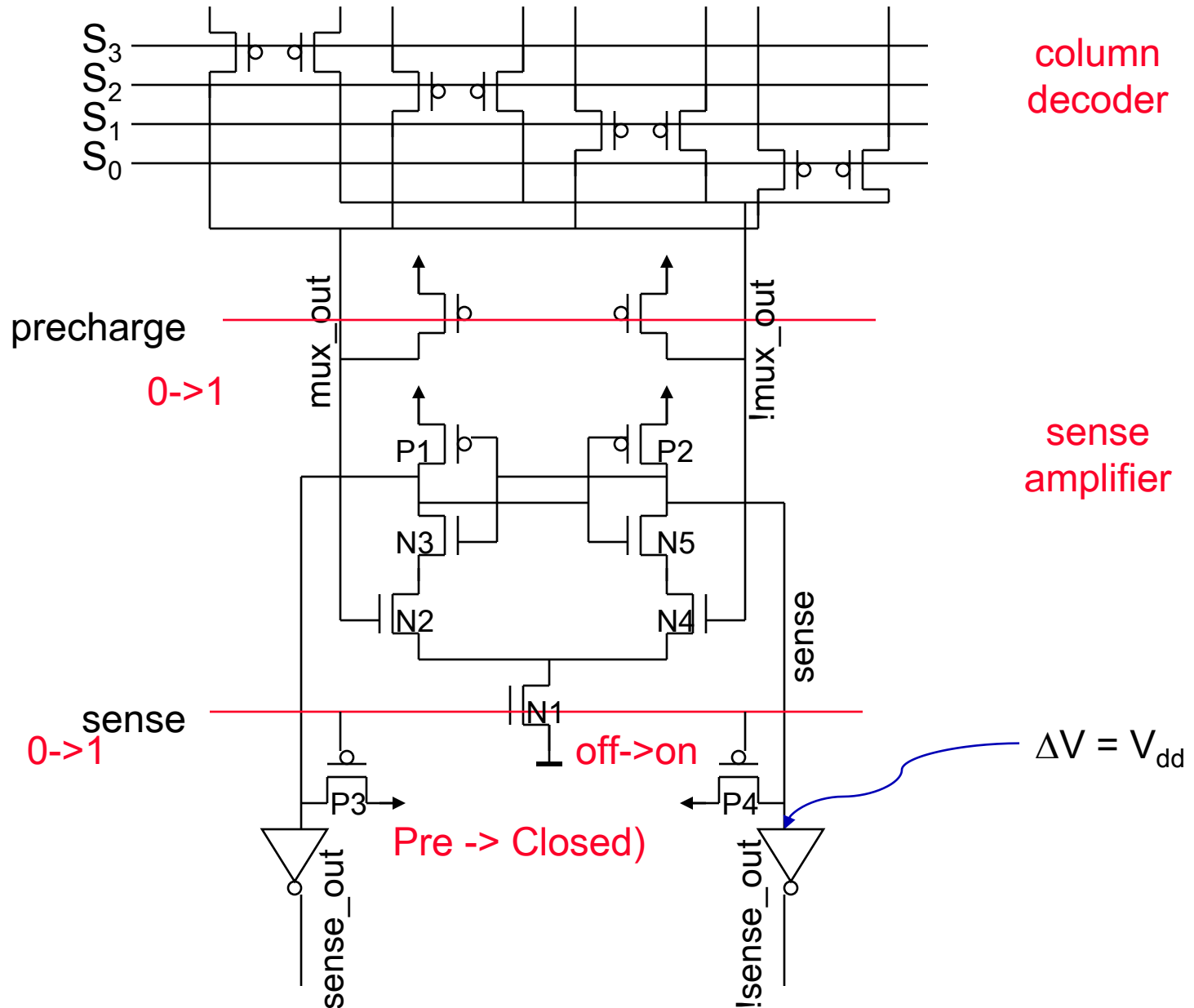
❑ Use sense amplifiers (SA) to amplify the small swing on the bit lines to the full rail-to-rail swing needed at the output

input   SA   output
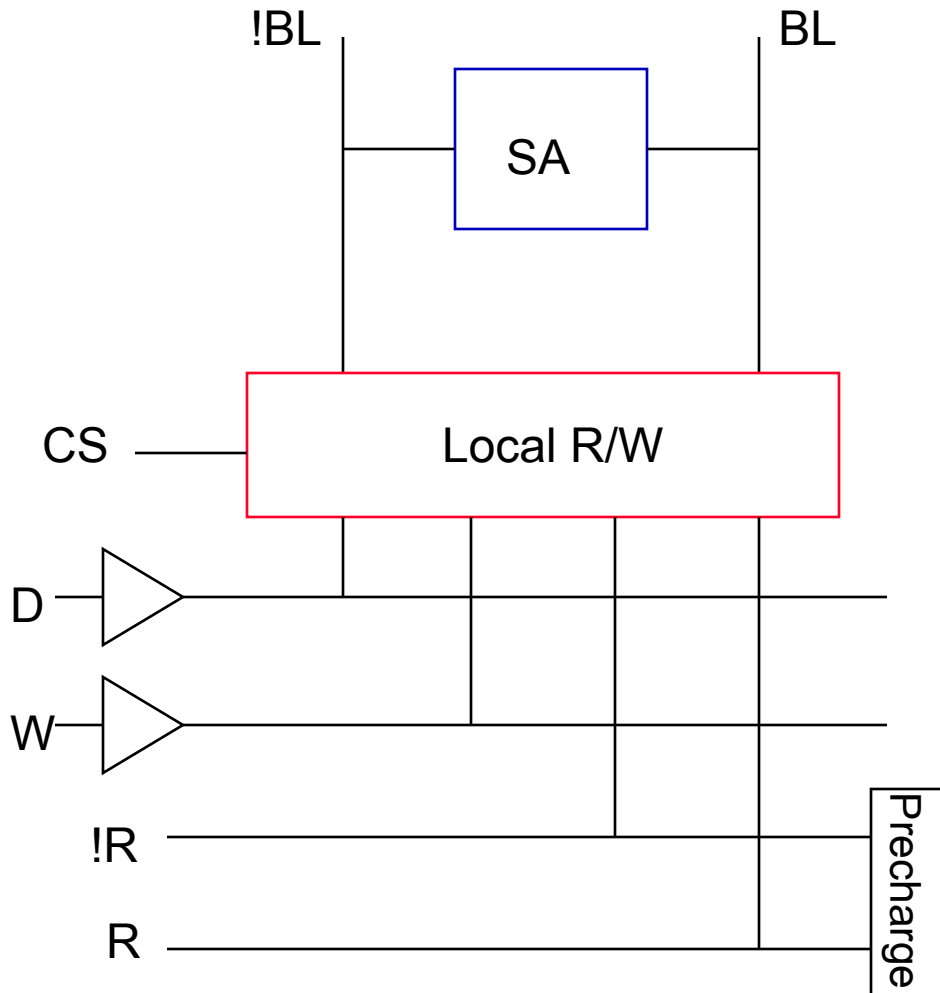
Latch Based Sense Amplifier

bit lines

$\Delta V = 0.1V_{dd}$

isolate

sense

sense amplifier outputs

$\Delta V = V_{dd}$

Alpha Differential Amplifier/Latch

Read/Write Circuitry

!BL   BL

SA

CS —— Local R/W

D —▷

W —▷

!R

R

Precharge

D: data (write) bus
R: read bus
W: write signal
CS: column select
     (column decoder)

Local W (write):
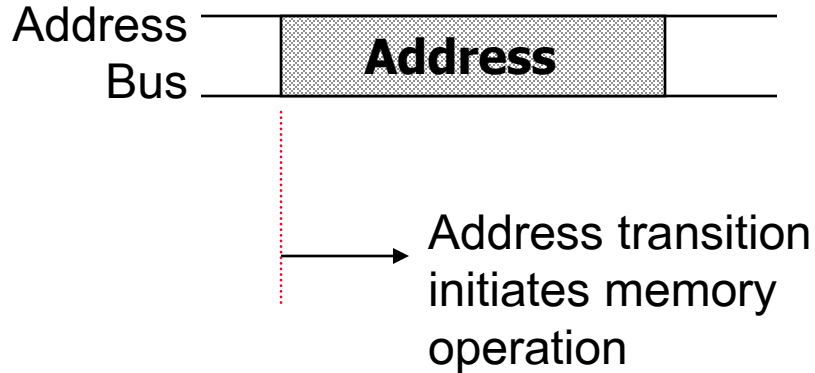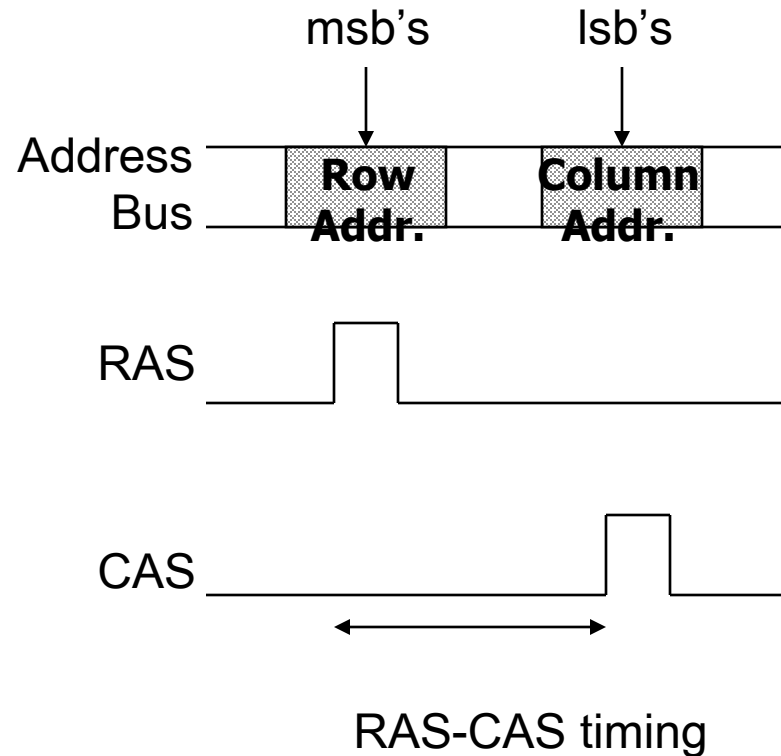 BL = D, !BL = !D
  enabled by W & CS
Local R (read):
  R = BL, !R = !BL
  enabled by !W & CS
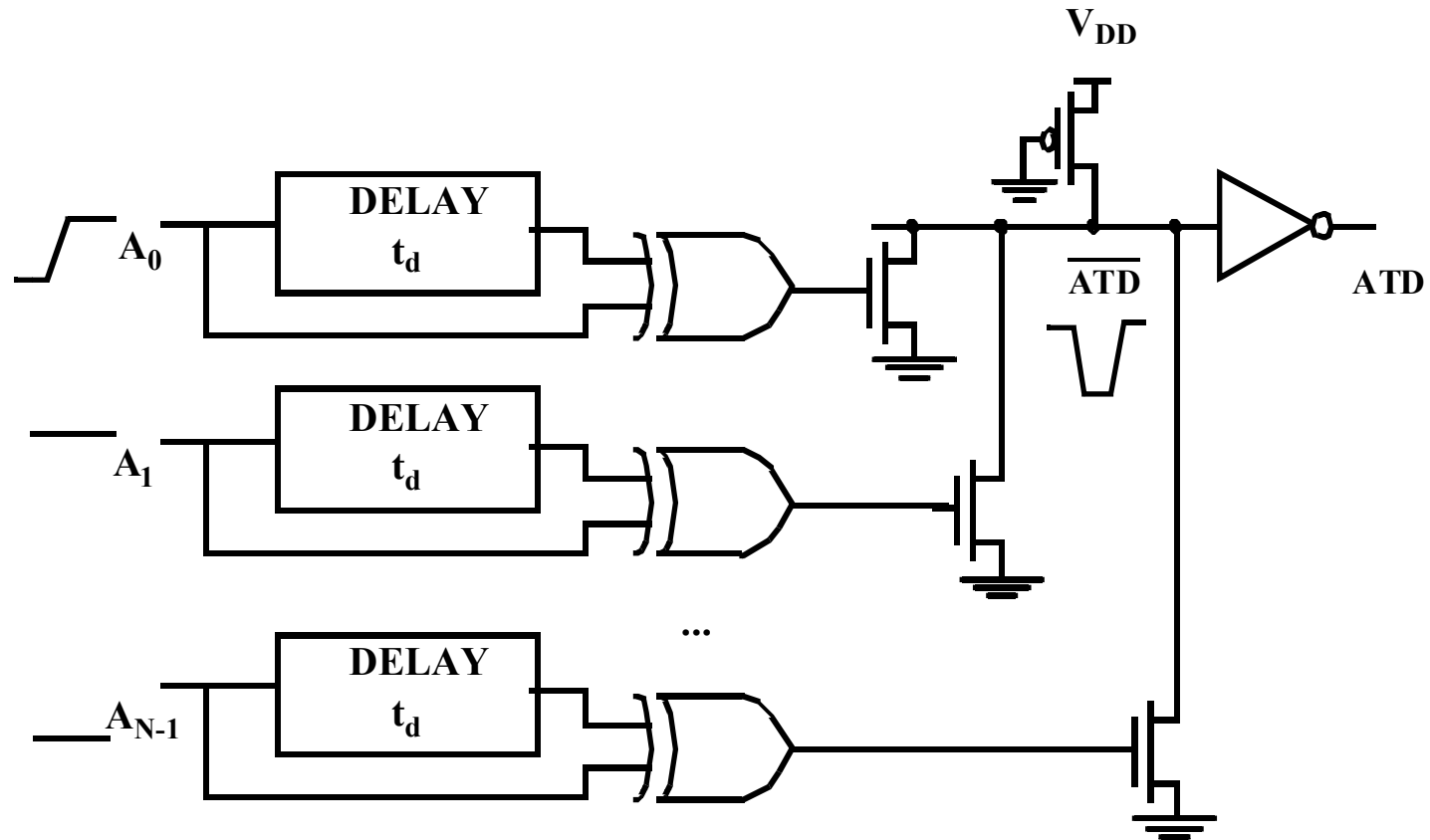
Approaches to Memory Timing

SRAM Timing
Self-Timed

DRAM Timing
Multiplexed Addressing

msb's   lsb's

Address
Bus   **Row Addr.**   **Column Addr.**

Address
Bus   **Address**

RAS

Address transition
initiates memory
operation

CAS

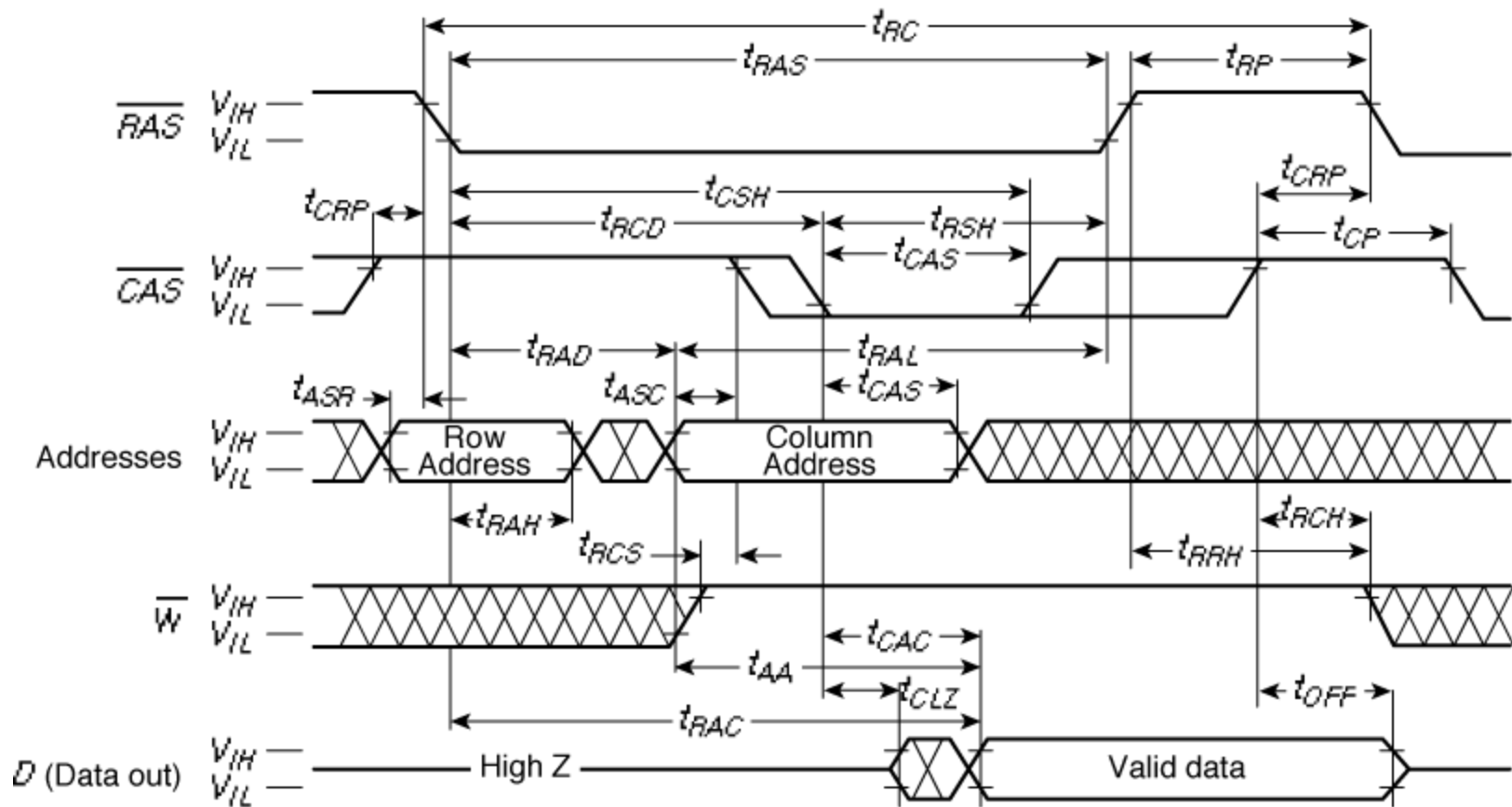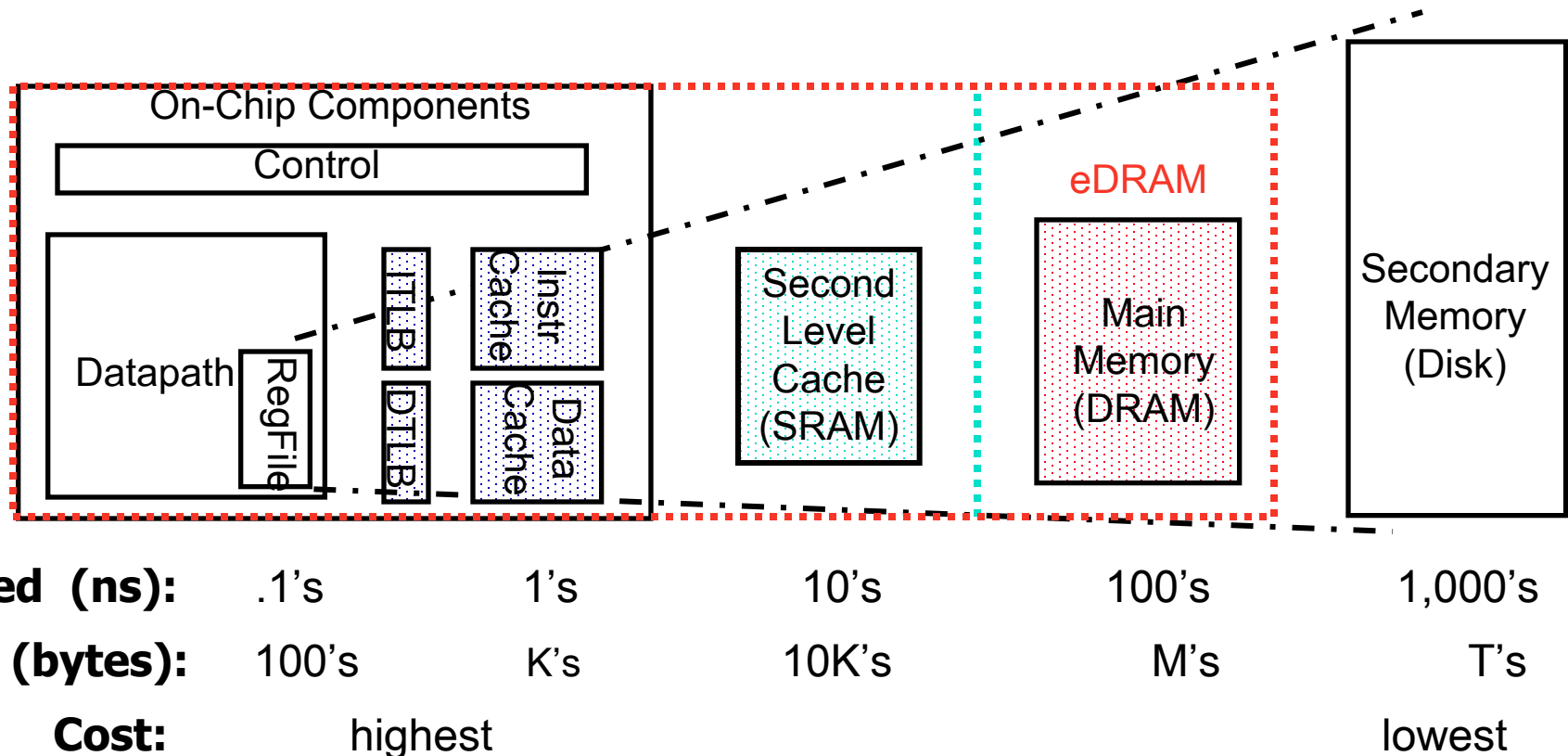RAS-CAS timing

SRAM Address Transition Detection

DRAM Timing

Review: A Typical Memory Hierarchy

❑ By taking advantage of the principle of locality:

◻ Present the user with as much memory as is available in the cheapest technology.

◻ Provide access at the speed offered by the fastest technology.

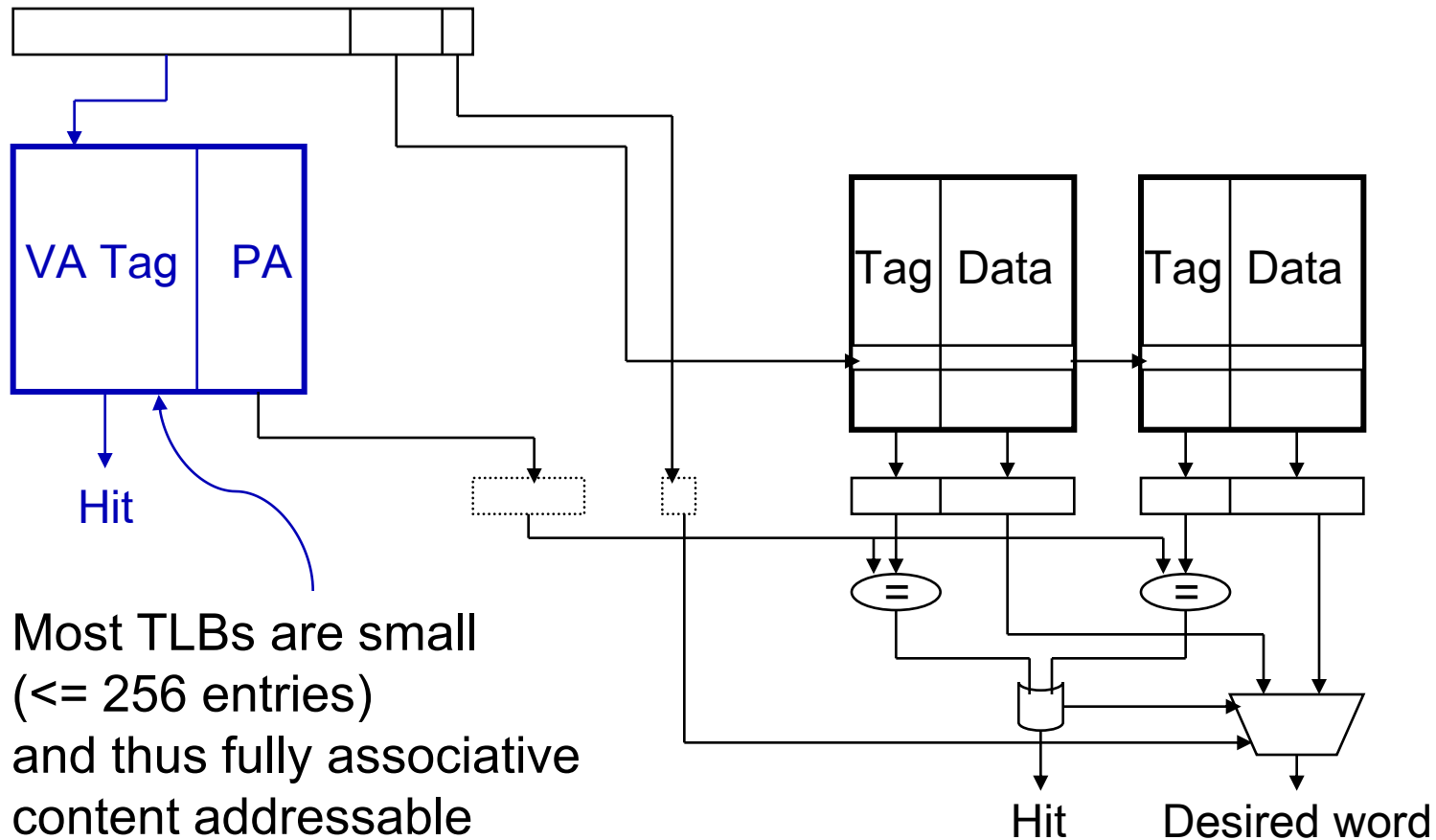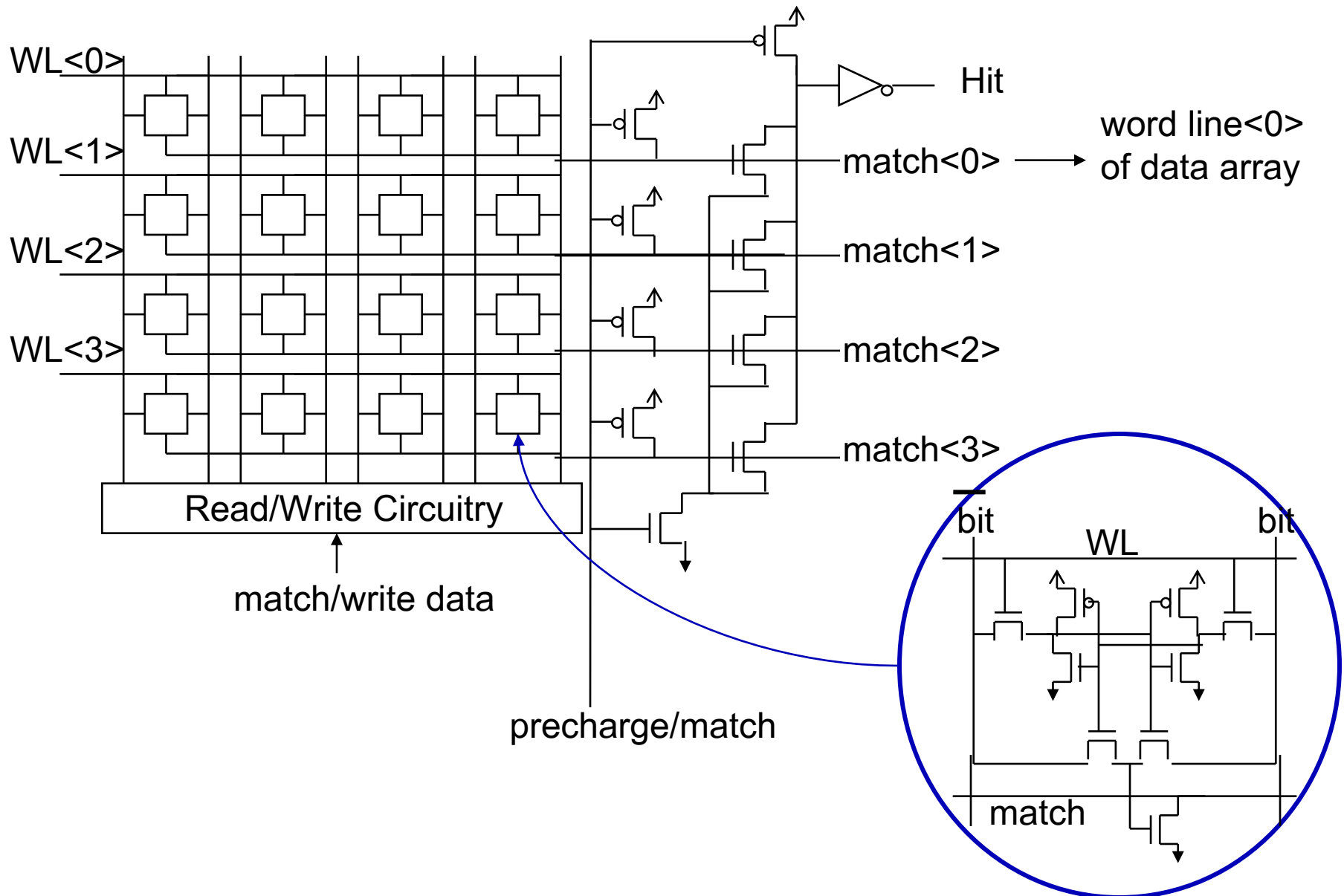|				
Speed (ns):	.1's	1's	10's	100's	1,000's
Size (bytes):	100's	K's	10K's	M's	T's
Cost:	highest				lowest

Translation Lookaside Buffers (TLBs)

❑ Small caches used to speed up address translation in processors with virtual memory

❑ All addresses have to be translated before cache access

❑ I$ can be virtually indexed/virtually tagged

TLB Structure

Address issued by CPU (page size = index bits + byte select bits)

VA Tag | PA

Hit

Most TLBs are small
(<= 256 entries)
and thus fully associative
content addressable
memories (CAMs)

Tag | Data

Tag | Data

=

=

Hit   Desired word

CAM Design

WL<0>

WL<1>

WL<2>

WL<3>

Read/Write Circuitry

match/write data

Hit

match<0> word line<0>
of data array

match<1>

match<2>

match<3>

precharge/match

bit   bit

WL

match

Reliability and Yield

❑ Semiconductor memories trade-off noise margin for density and performance

   Thus, they are highly sensitive to noise (cross talk, supply noise)
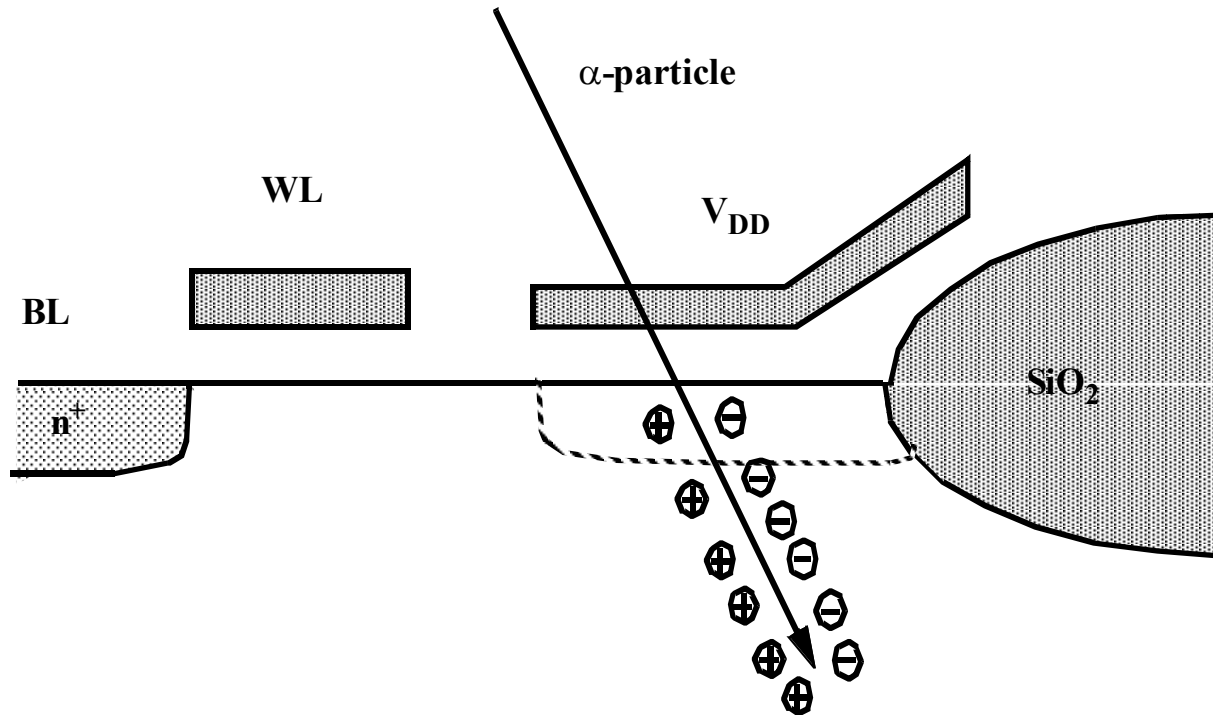
❑ High density and large die size causes yield problems

$$\text{Yield} = 100 \ \frac{\text{\# of good chips/wafer}}{\text{\# of chips/wafer}}$$
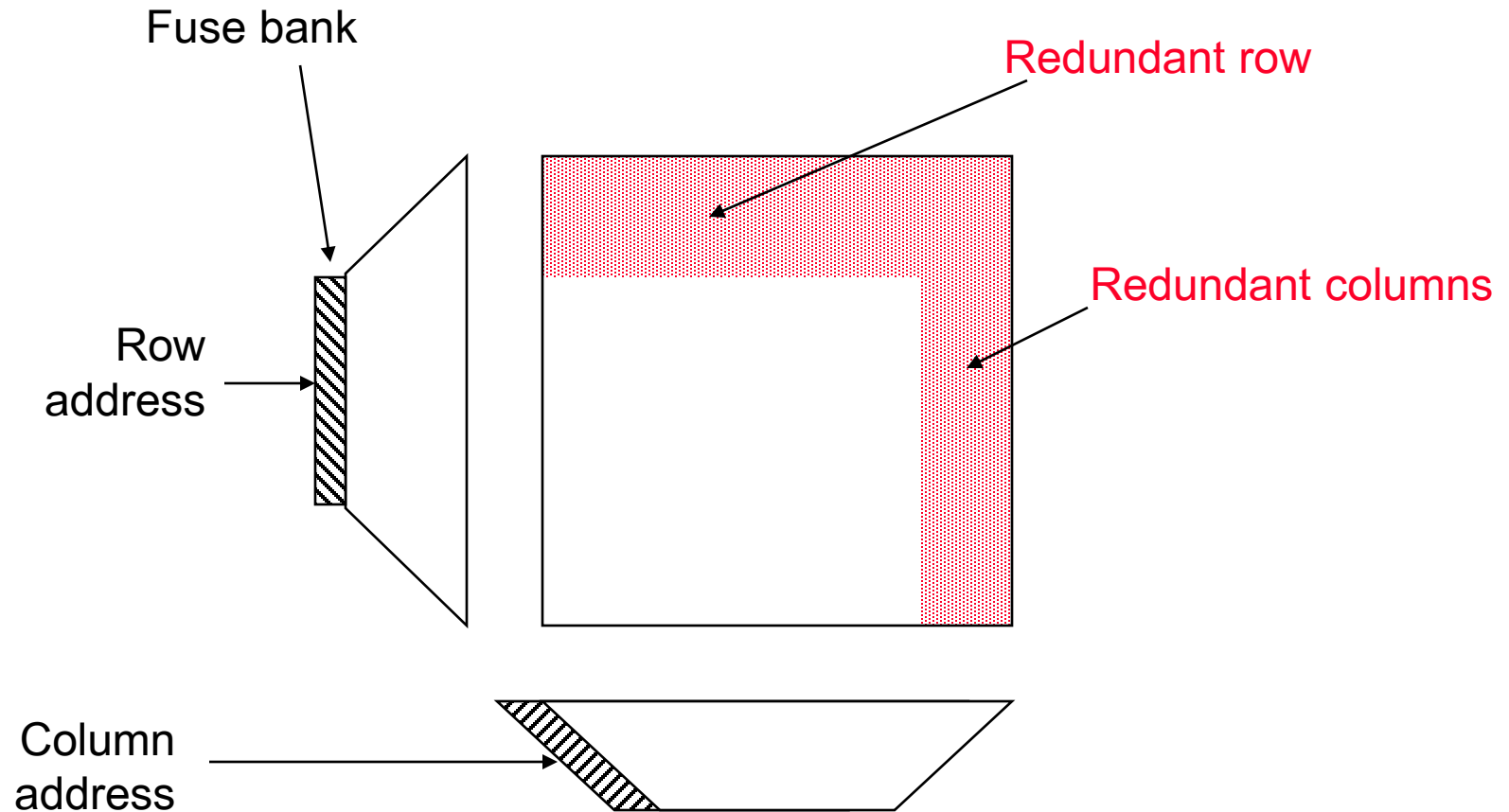
$$Y = [(1 - e^{-AD})/(AD)]^2$$

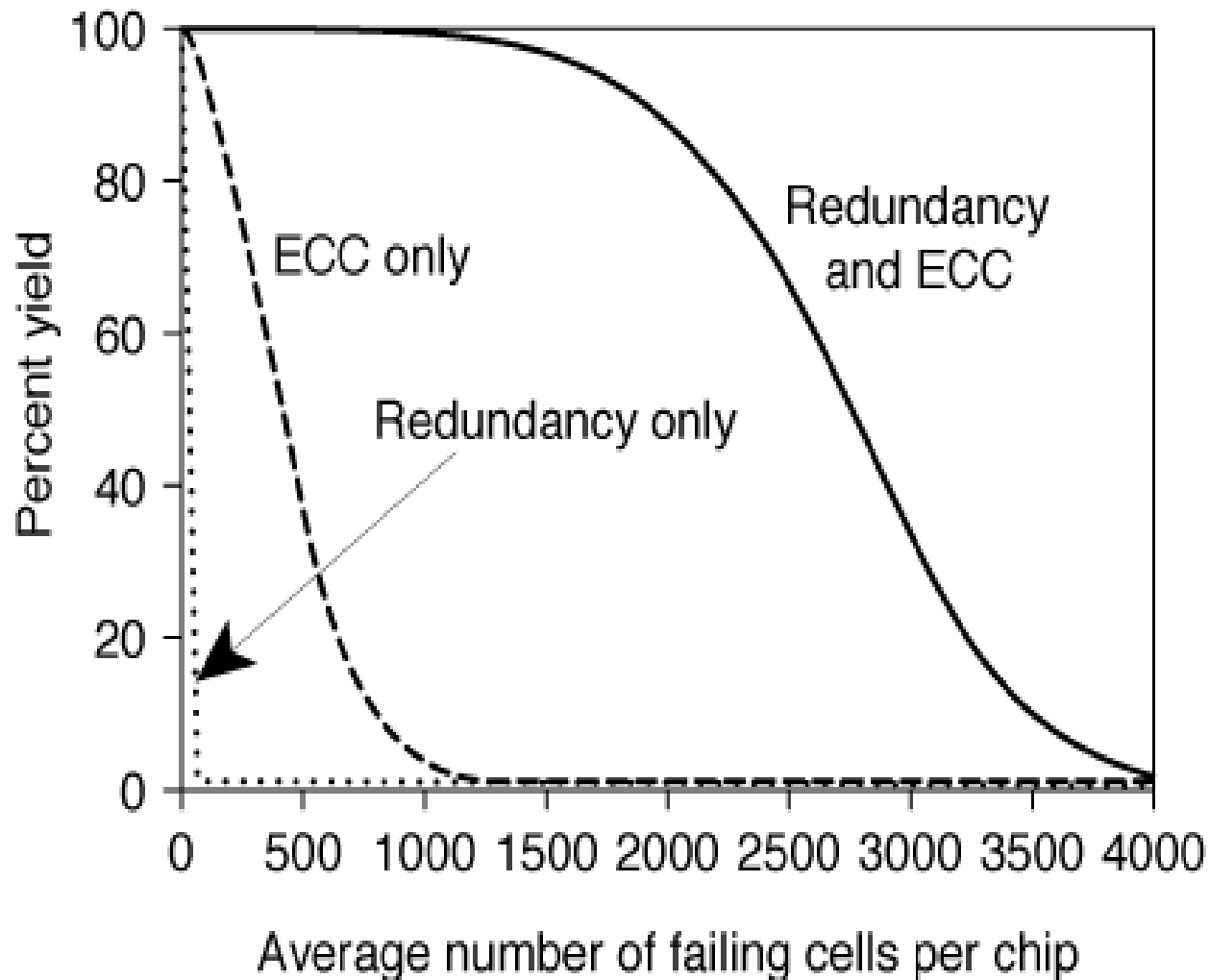❑ Increase yield using error correction and redundancy

Alpha Particles

1 particle ~ 1 million carriers

Redundancy in the Memory Structure

Fuse bank

Redundant row

Redundant columns

Row address

Column address

Redundancy and Error Correction

Next Lecture and Reminders

- **Next lecture**
  - System level interconnect
    - Reading assignment – Rabaey, et al, xx

- **Reminders**
  - Project final reports due December 5th
  - Final grading negotiations/correction (except for the final exam) must be concluded by December 10th
  - Final exam scheduled
    - Monday, December 16th from 10:10 to noon in 118 and 121 Thomas