CSE477
VLSI Digital Circuits
Fall 2002

Lecture 06: Static CMOS Logic

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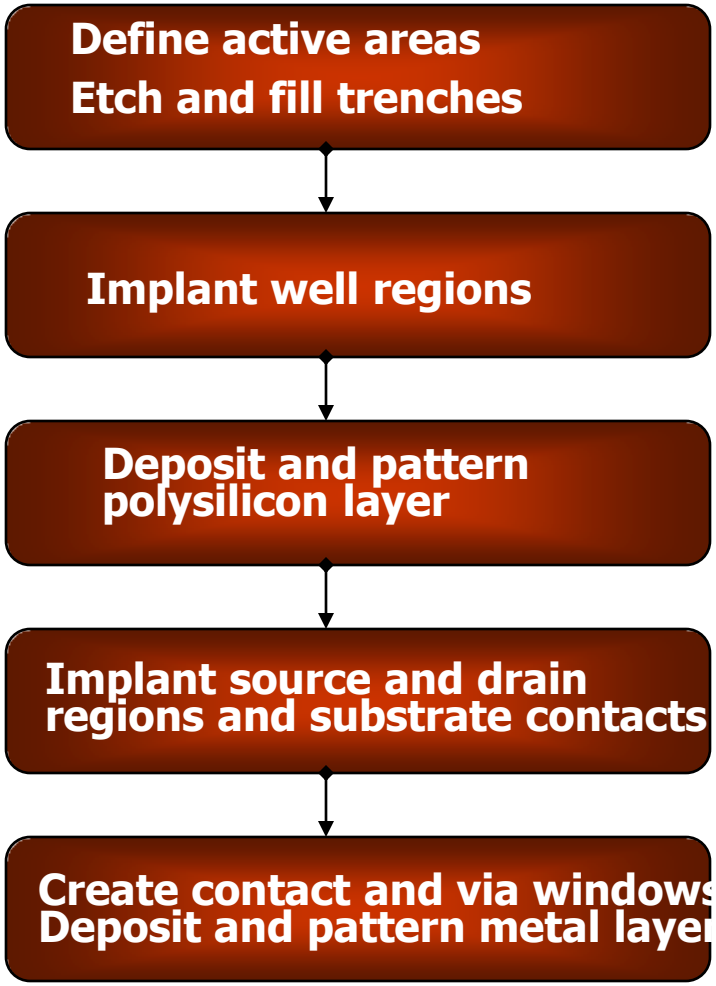
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Review: CMOS Process at a Glance



- One full photolithography sequence per layer (mask)
- Built (roughly) from the bottom up
  - 4 metal
  - 2 polysilicon
  - 3 source and drain diffusions
  - 1 tubs (aka wells, active areas)

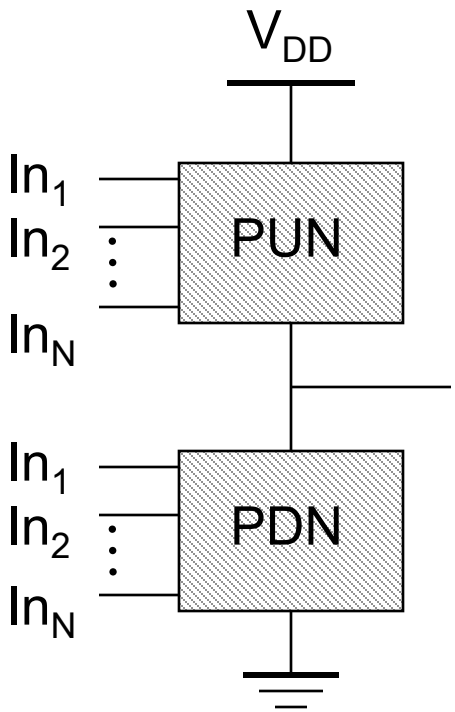
exception!

CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either V_{DD} or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - V_{OH} and V_{OL} are at V_{DD} and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between V_{DD} and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)
- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

Static Complementary CMOS

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

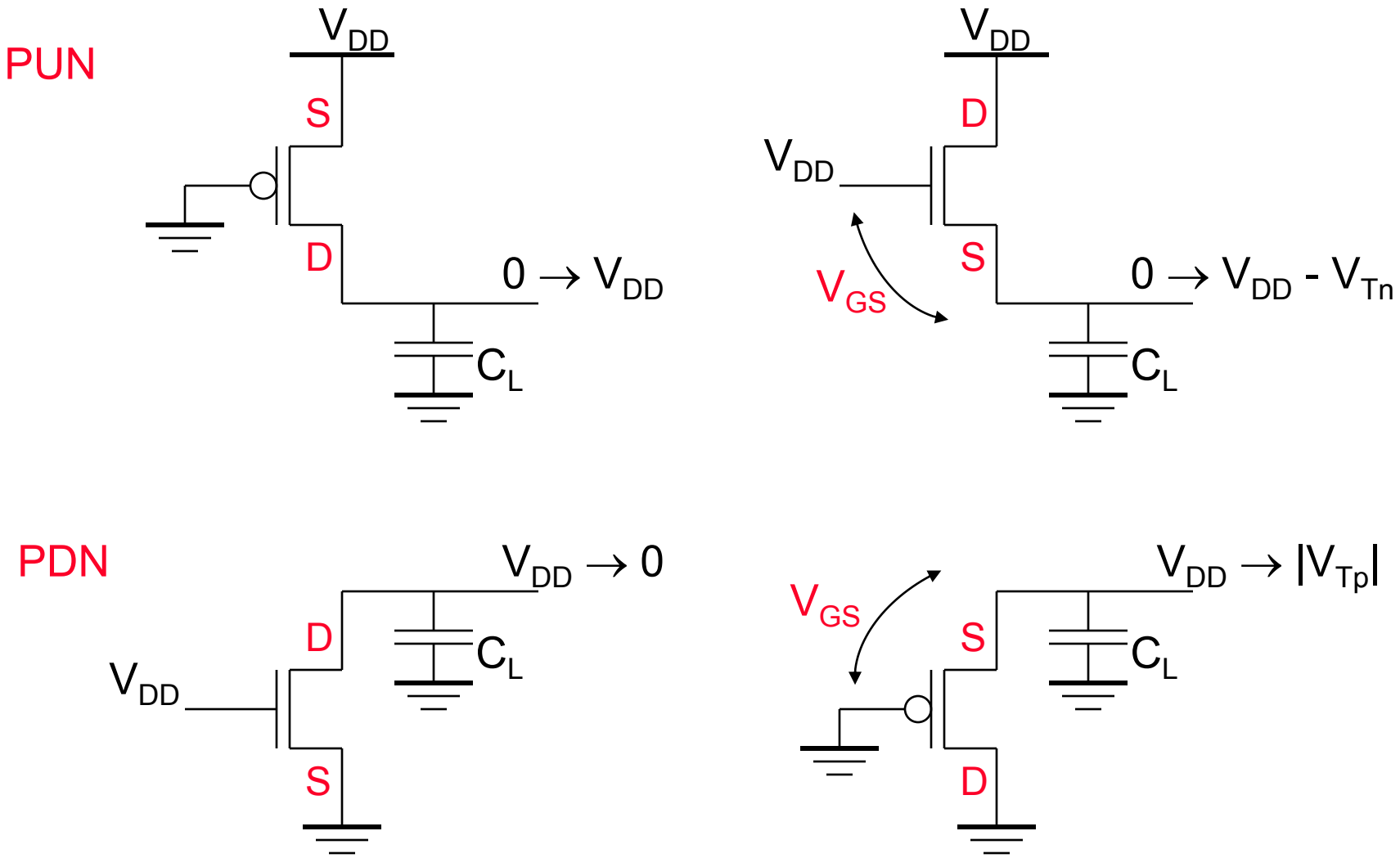
pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

NMOS transistors only

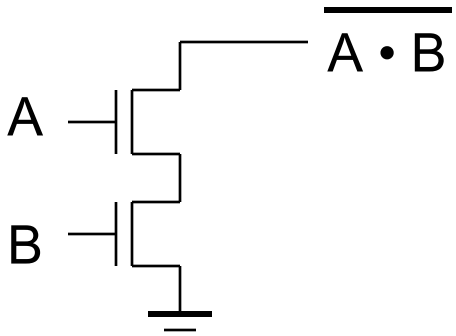
PUN and PDN are dual logic networks

Threshold Drops

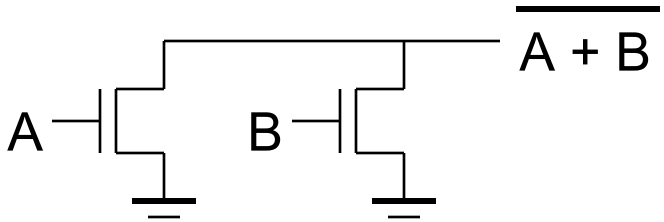


Construction of PDN

- NMOS devices in series implement a NAND function



- NMOS devices in parallel implement a NOR function



Dual PUN and PDN

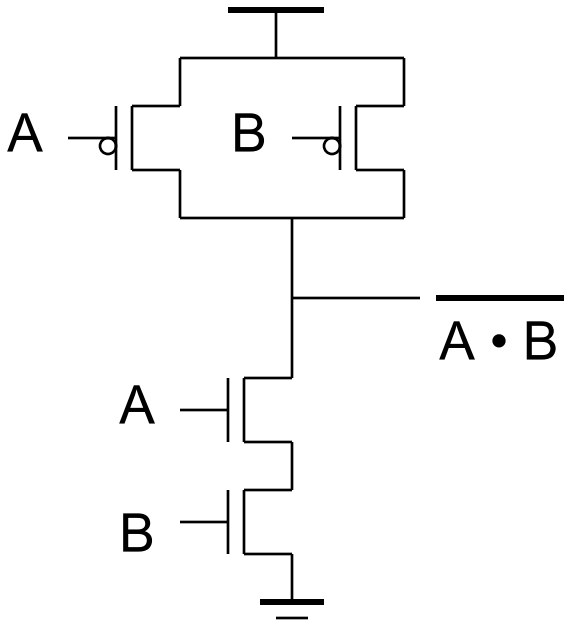
- PUN and PDN are dual networks
  - DeMorgan's theorems

$$\overline{A + B} = \overline{A} \cdot \overline{B} \quad [!(A + B) = !A \cdot !B \text{ or } !(A \mid B) = !A \,\&\, !B]$$

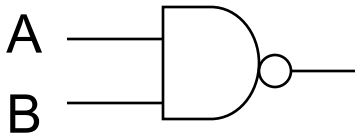
$$\overline{A \cdot B} = \overline{A} + \overline{B} \quad [!(A \cdot B) = !A + !B \text{ or } !(A \,\&\, B) = !A \mid !B]$$

  - a parallel connection of transistors in the PUN corresponds to a series connection of the PDN
- Complementary gate is naturally inverting (NAND, NOR, AOI, OAI)
- Number of transistors for an N-input logic gate is 2N

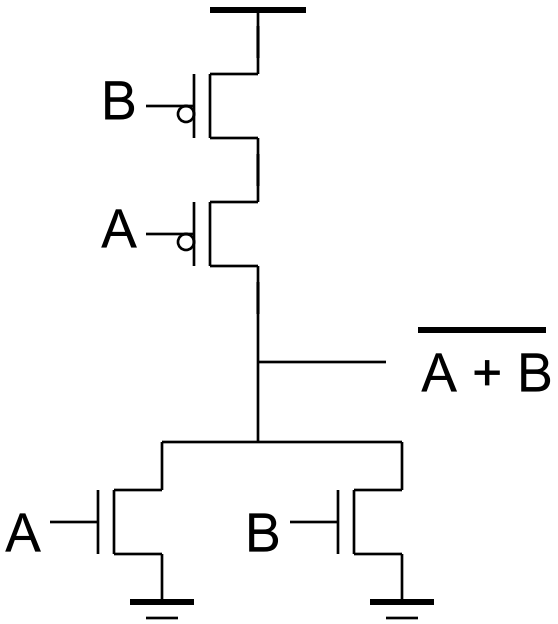
CMOS NAND



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



CMOS NOR



A	B	F
0	0	1
0	1	0
1	0	0
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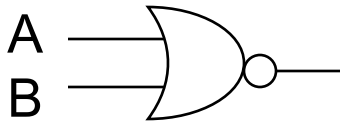
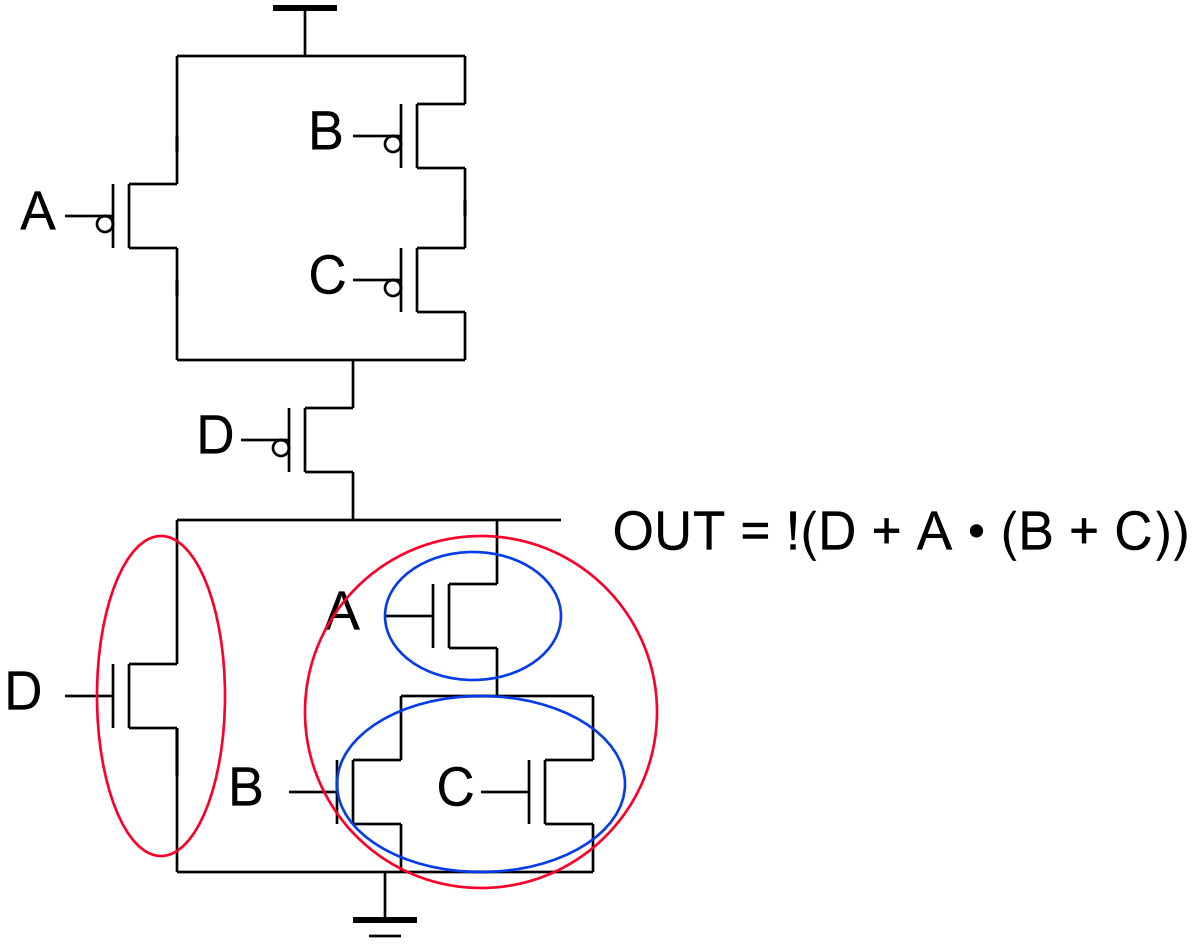
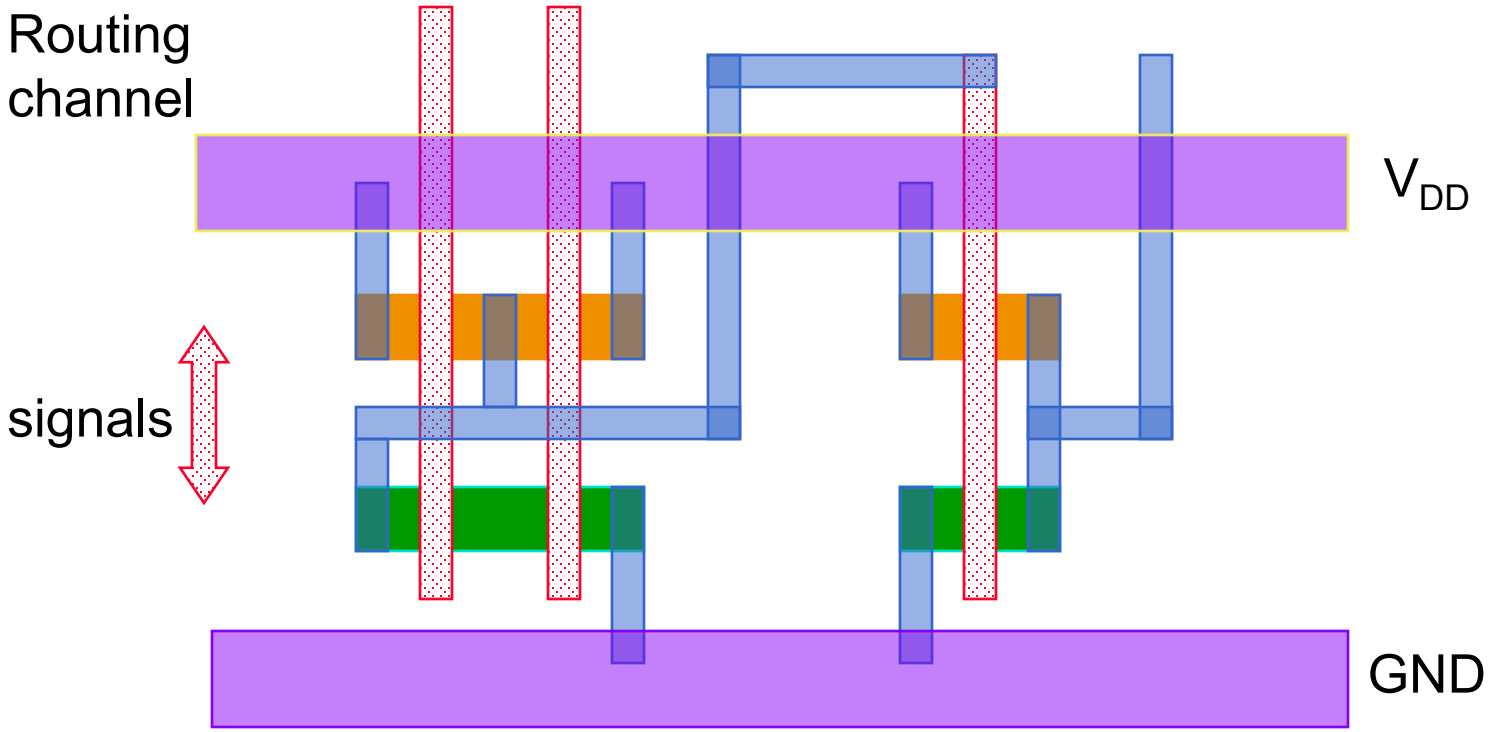


Complex CMOS Gate

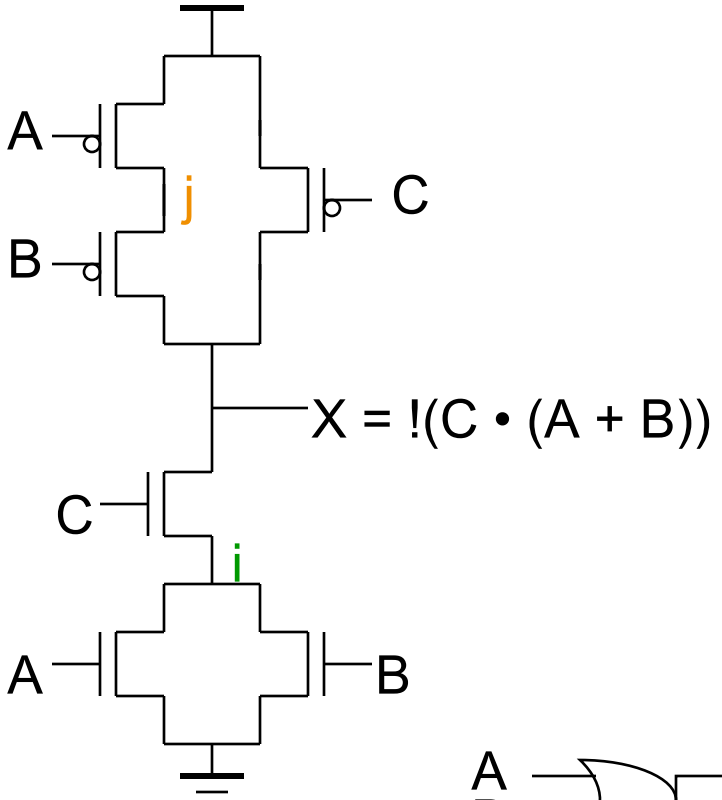


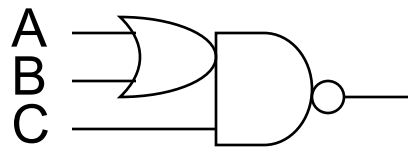
Standard Cell Layout Methodology

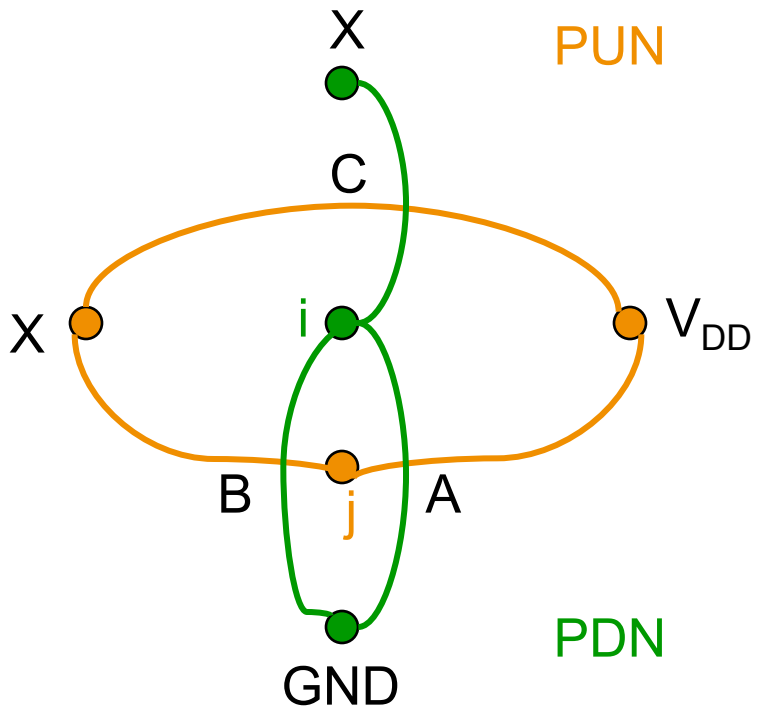


What logic function is this?

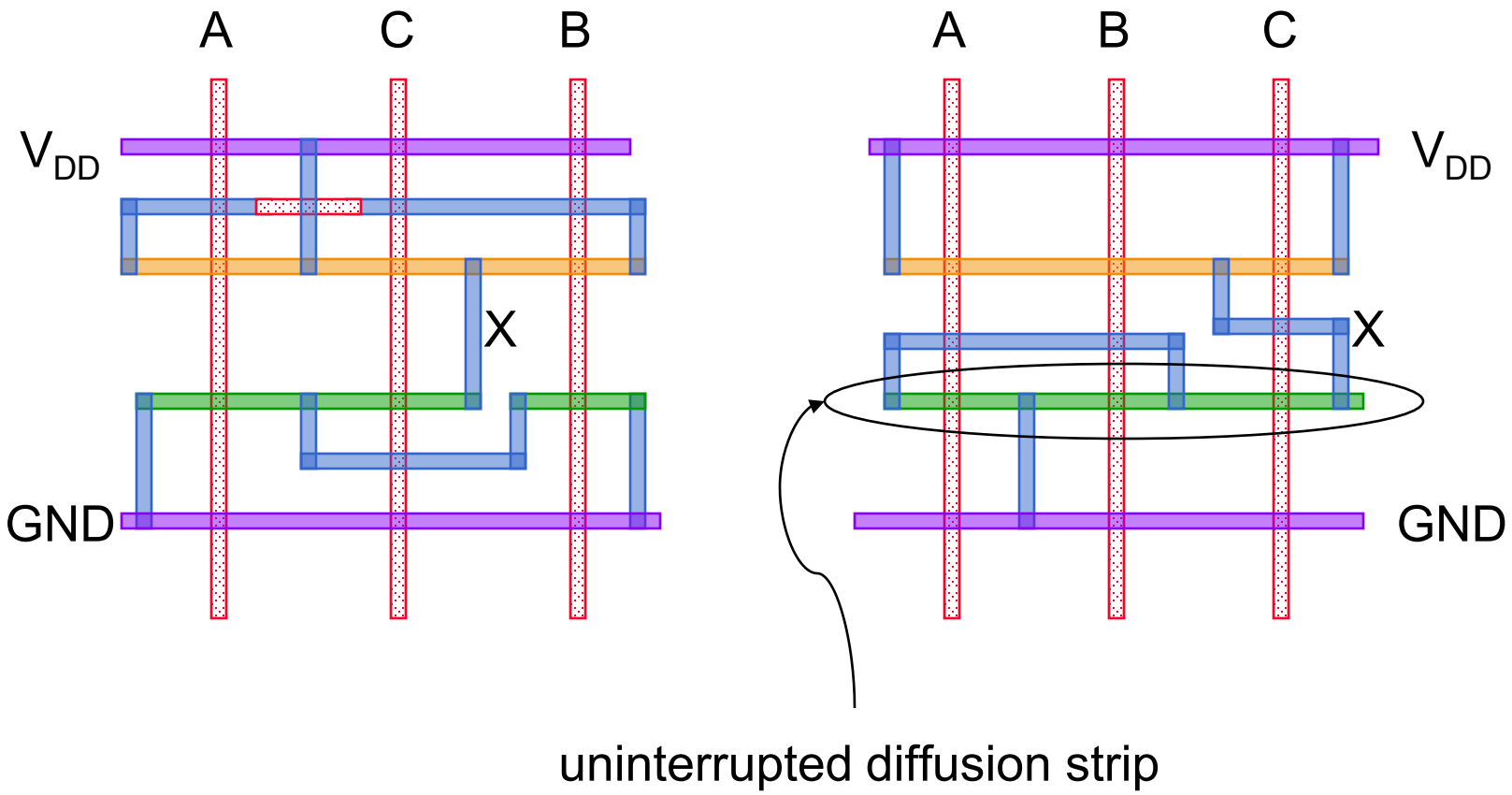
OAI21 Logic Graph





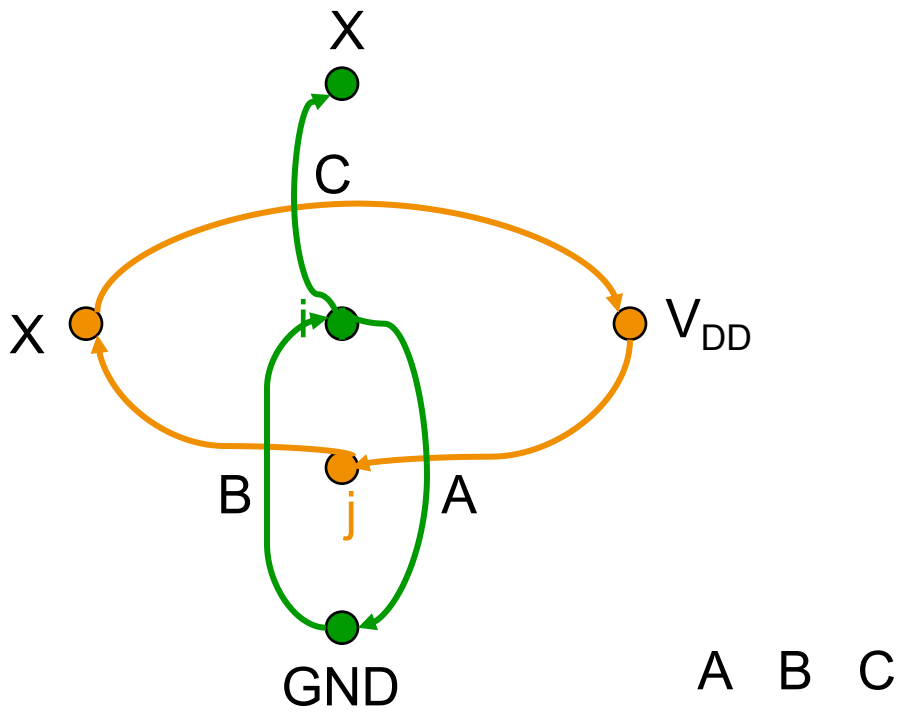


Two Stick Layouts of !(C • (A + B))



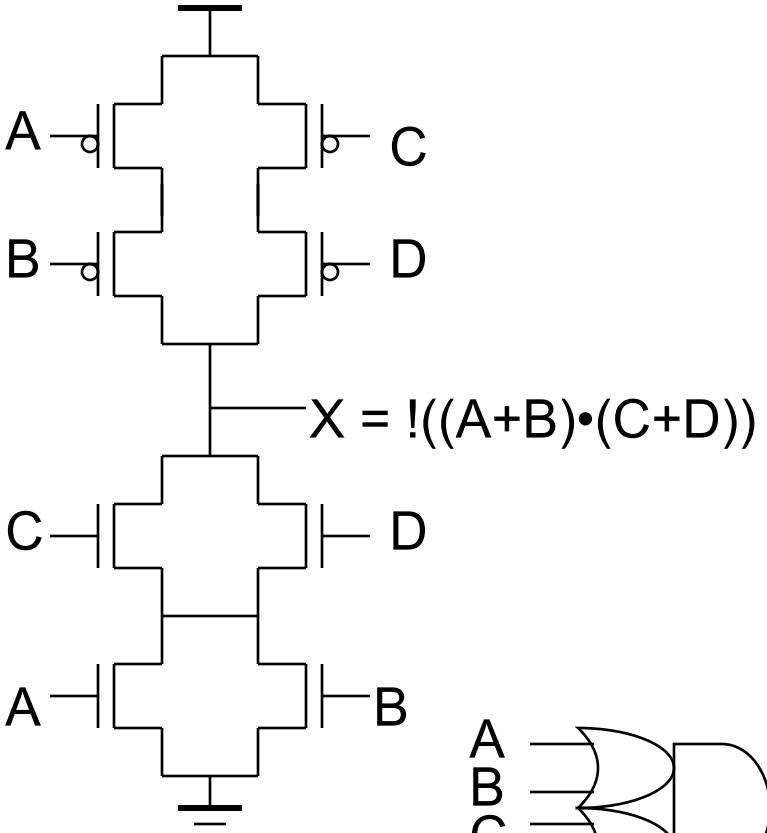
Consistent Euler Path

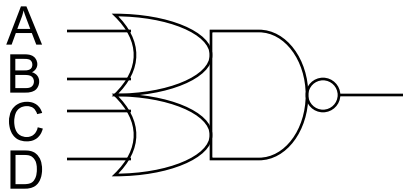
- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

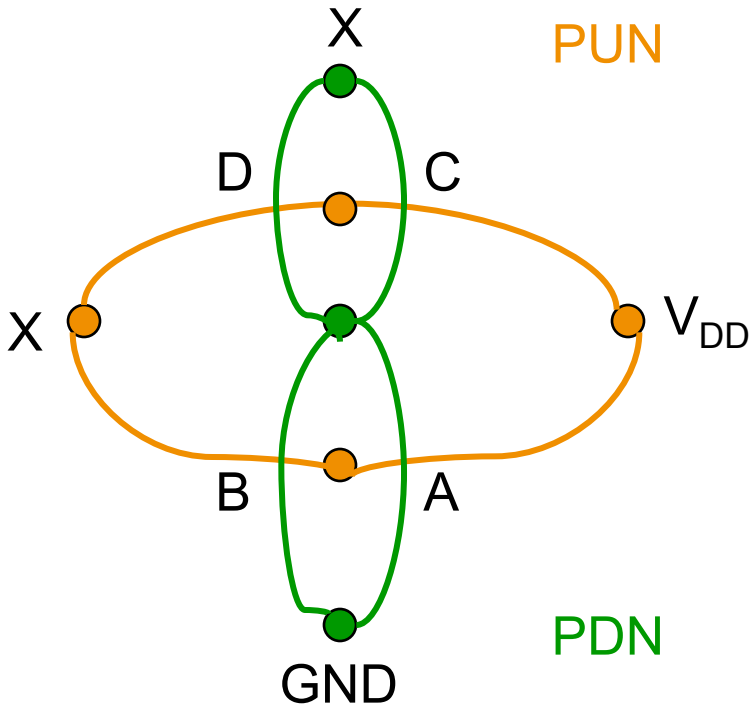


- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

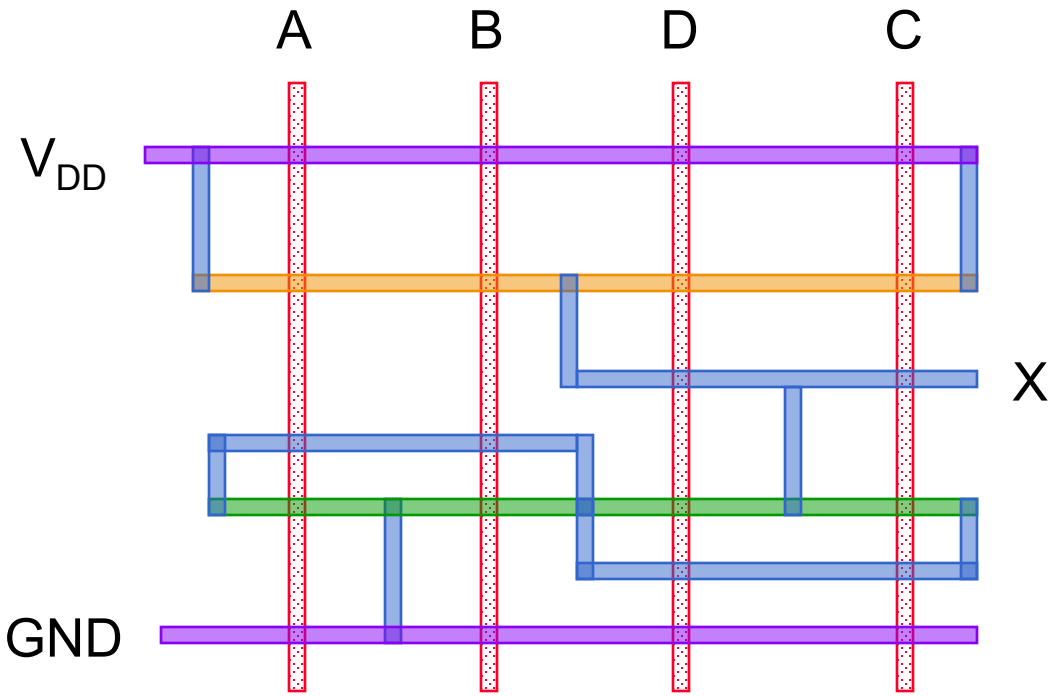
OAI22 Logic Graph







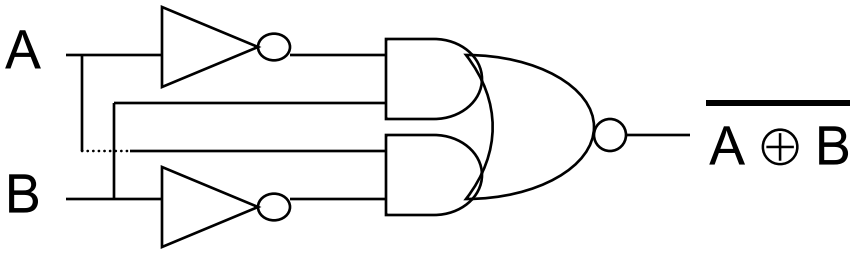
OAI22 Layout



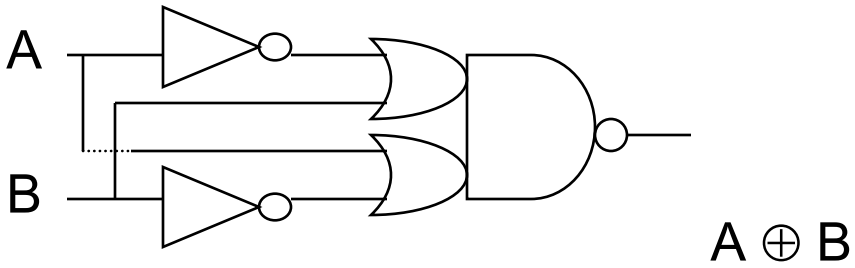
- Some functions have no consistent Euler path like x = !(a + bc + de) (but x = !(bc + a + de) does!)

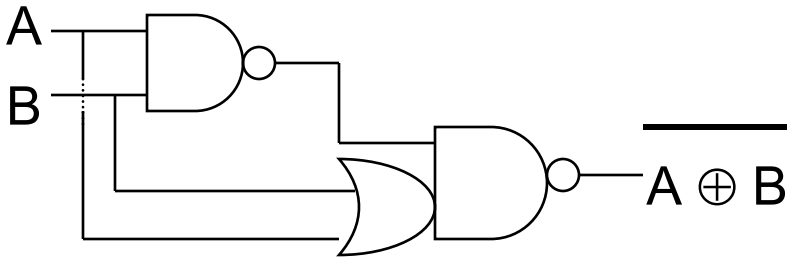
XNOR/XOR Implementation

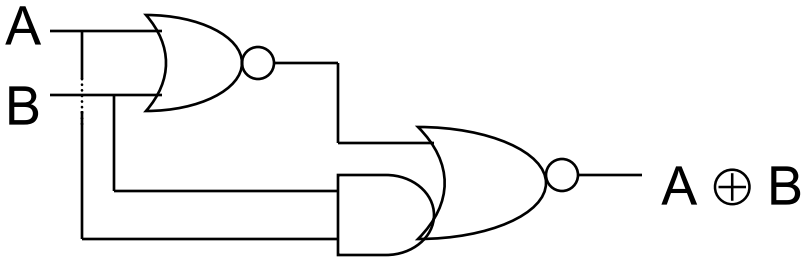
XNOR



XOR

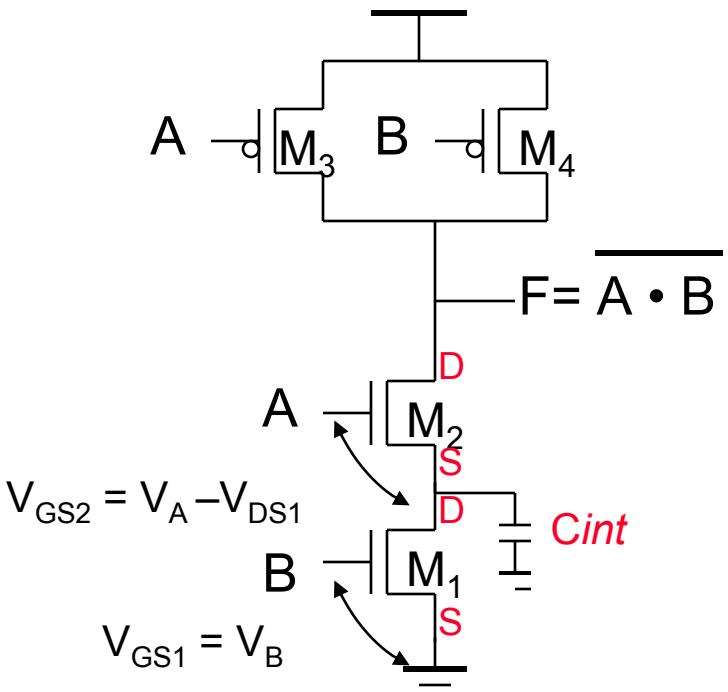


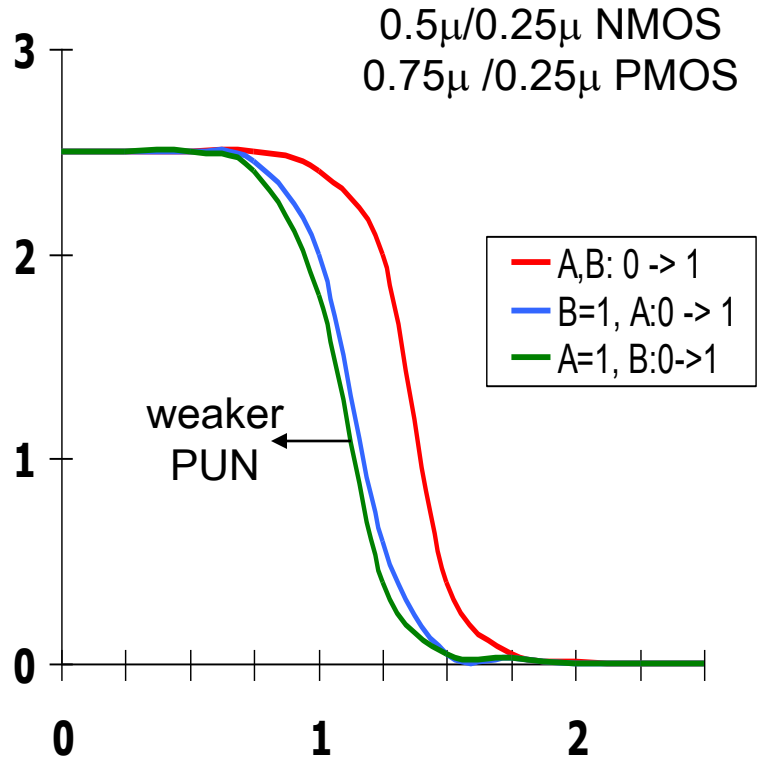




- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?

VTC is Data-Dependent





- The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

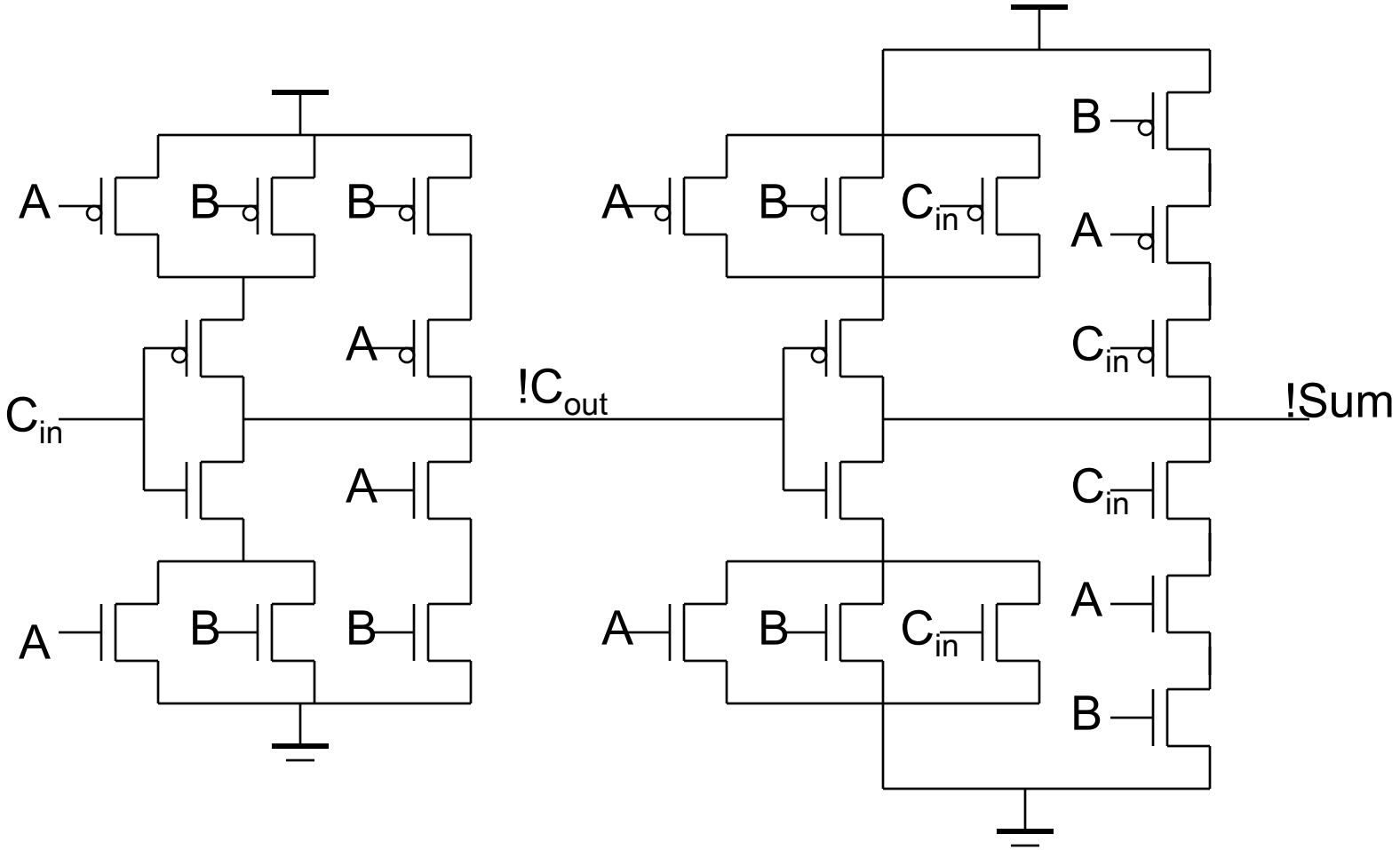
$V_{Tn1} = V_{Tn0}$

$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{(|2\phi_F| + V_{int})} - \sqrt{|2\phi_F|})$

since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of C*int*

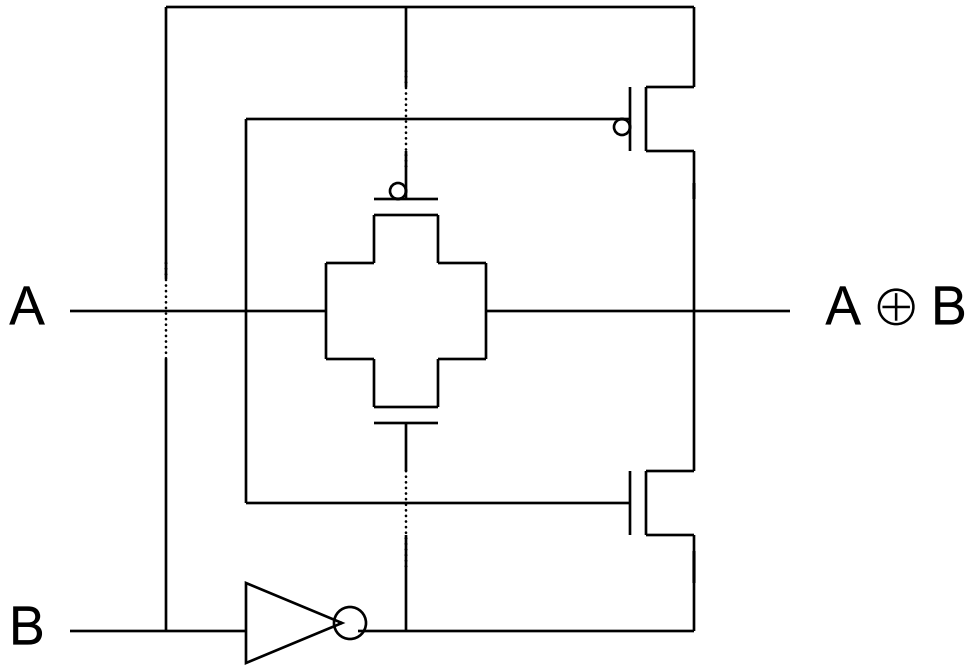
Static CMOS Full Adder Circuit

$!C_{out} = !C_{in} \,\&\, (!A \mid !B) \mid (!A \,\&\, !B)$ $!Sum = C_{out} \,\&\, (!A \mid !B \mid !C_{in}) \mid (!A \,\&\, !B \,\&\, !C_{in})$



$C_{out} = C_{in} \,\&\, (A \mid B) \mid (A \,\&\, B)$ $Sum = !C_{out} \,\&\, (A \mid B \mid C_{in}) \mid (A \,\&\, B \,\&\, C_{in})$

Next Time: Pass Transistor Circuits



Next Lecture and Reminders

- Next lecture
  - Pass transistor logic
    - Reading assignment – Rabaey, et al, 6.2.3

- Reminders
  - Project Title due today !
  - Lecture 5 will be *next* Thursday (guest lecturer)
  - HW2 due September 24th
  - Evening midterm exam scheduled
    - Wednesday, October 10th from 8:15 to 10:15pm in 260 Willard
    - Only one midterm conflict filed for so far