Chapter 13 Output Stages and Power Amplifiers

- 13.1 General Considerations
- 13.2 Emitter Follower as Power Amplifier
- 13.3 Push-Pull Stage
- 13.4 Improved Push-Pull Stage
- 13.5 Large-Signal Considerations
- 13.6 Short Circuit Protection
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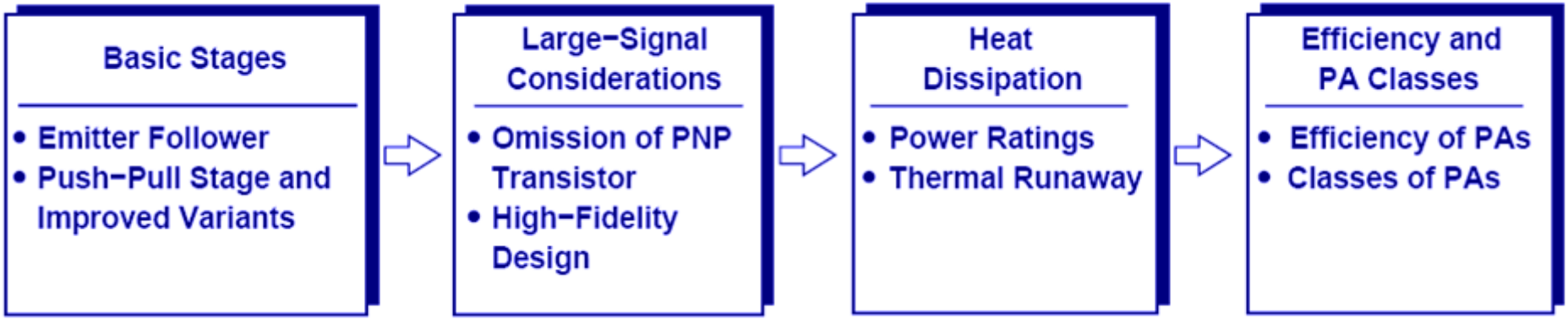
Why Power Amplifiers?

- Drive a load with high power.
- Cell phone needs 1W of power at the antenna.
- Audio system needs tens to hundreds Watts of power.
- Ordinary Voltage/Current amplifiers are not equipped for such applications

Chapter Outline



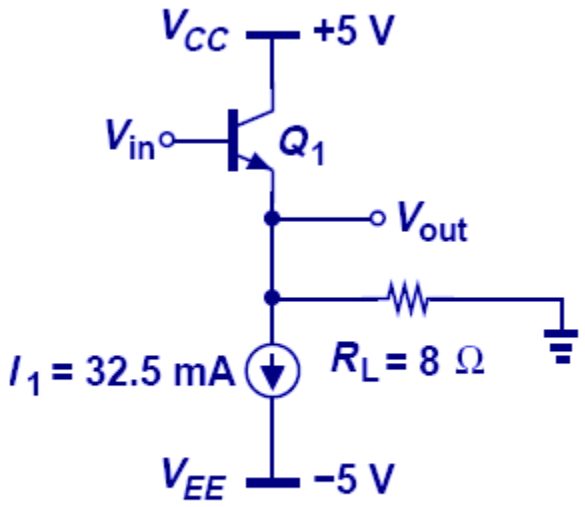
Power Amplifier Characteristics

- Experiences small load resistance.
- Delivers large current levels.
- Requires large voltage swings.
- Draws a large amount of power from supply.
- Dissipates a large amount of power, therefore gets “hot”.

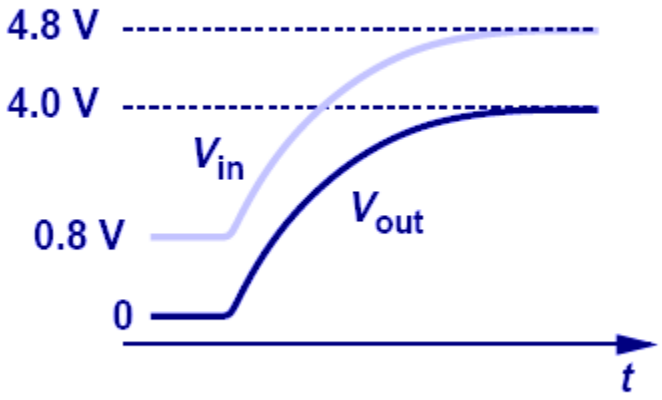
Power Amplifier Performance Metrics

- **Linearity**
- **Power Efficiency**
- **Voltage Rating**

Emitter Follower Large-Signal Behavior I



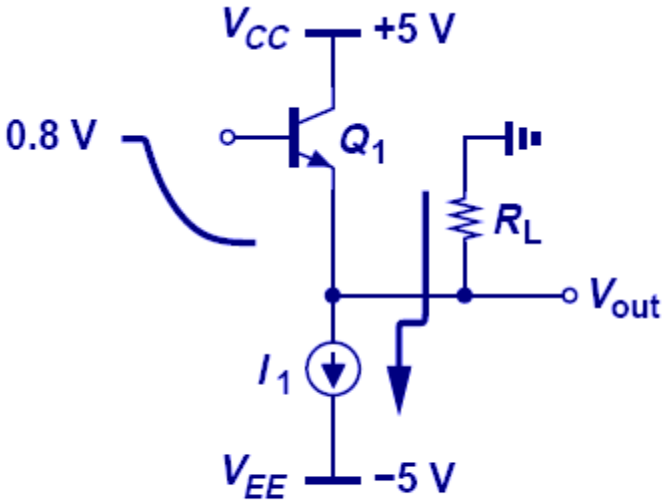
(a)



(b)

- As V_{in} increases V_{out} also follows and Q_1 provides more current.

Emitter Follower Large-Signal Behavior II



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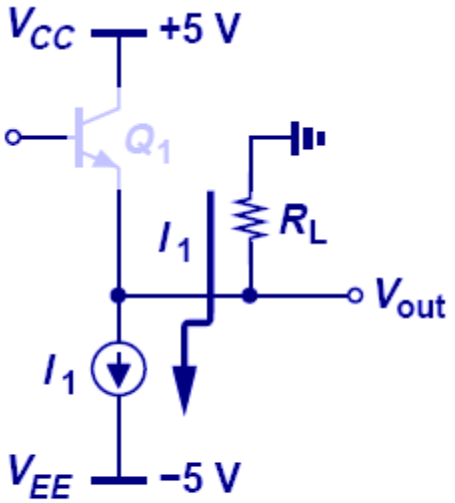
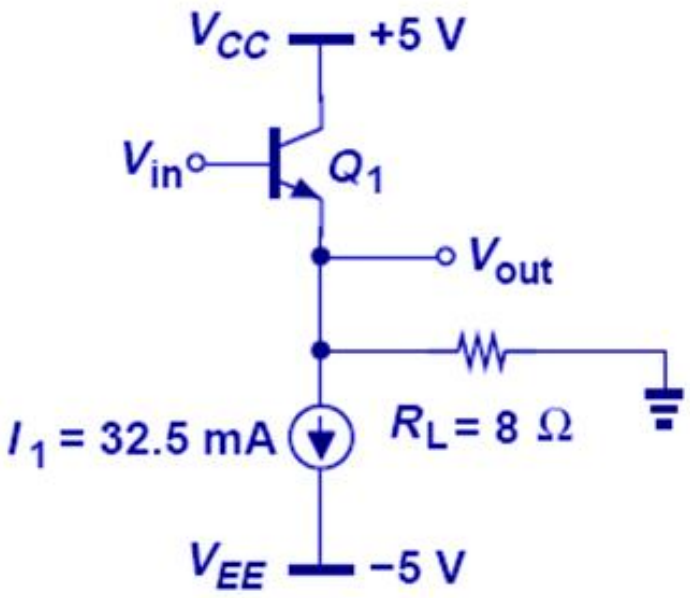


(d)

- **However as V_{in} decreases, V_{out} also decreases, shutting off Q_1 and resulting in a constant V_{out}.**

Example: Emitter Follower



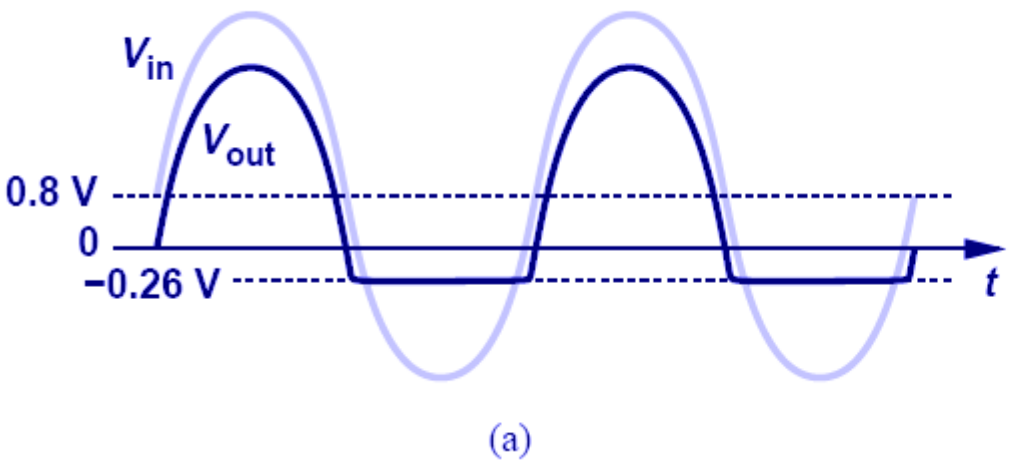
$$V_{in} - V_T \ln\left[\left(\frac{V_{out}}{R_L} + I_1\right)\frac{1}{I_S}\right] = V_{out}$$

$$V_{in} = 0.5V \Rightarrow V_{out} \approx -211mV$$

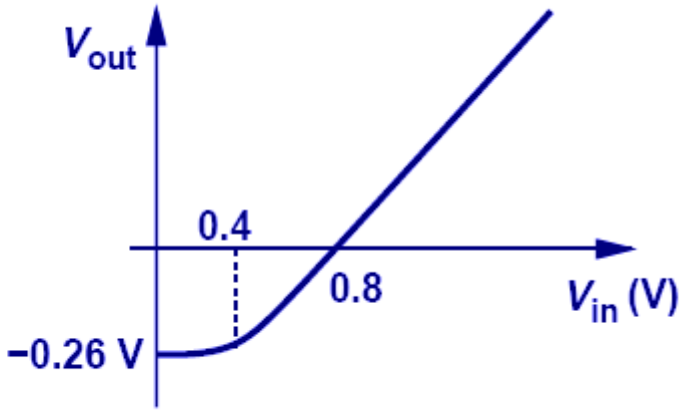
$$V_{in} = V_T \ln\frac{I_{C1}}{I_S} + \left(I_{C1} - I_1\right)R_L$$

$$I_{C1} \approx 0.01I_1 \Rightarrow V_{in} \approx 390mV$$

Linearity of an Emitter Follower



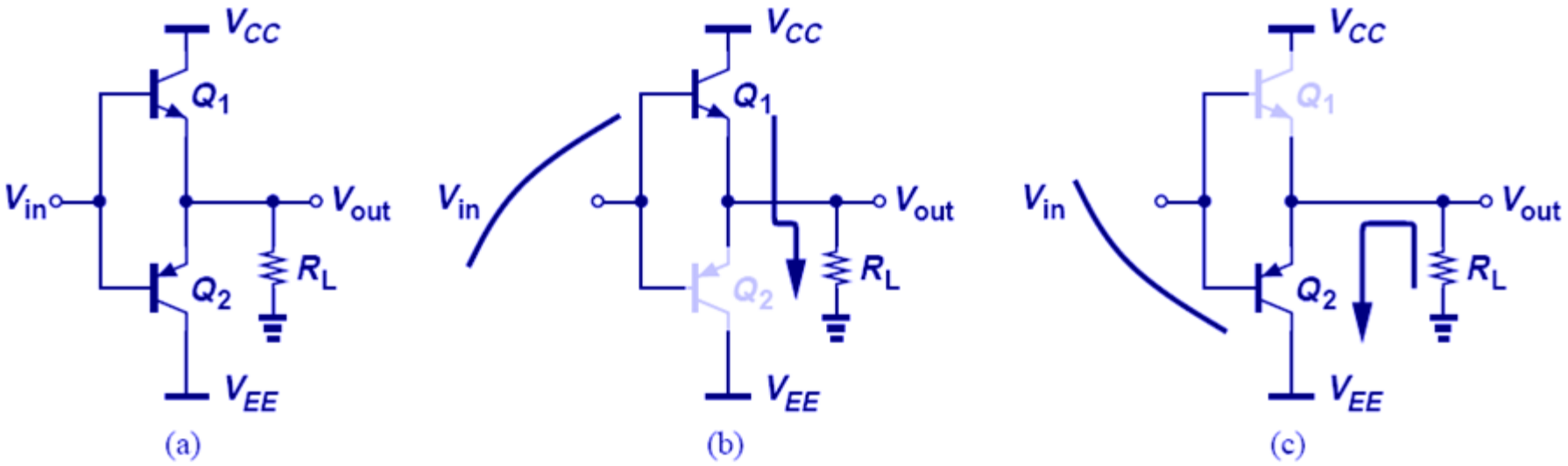
(a)



(b)

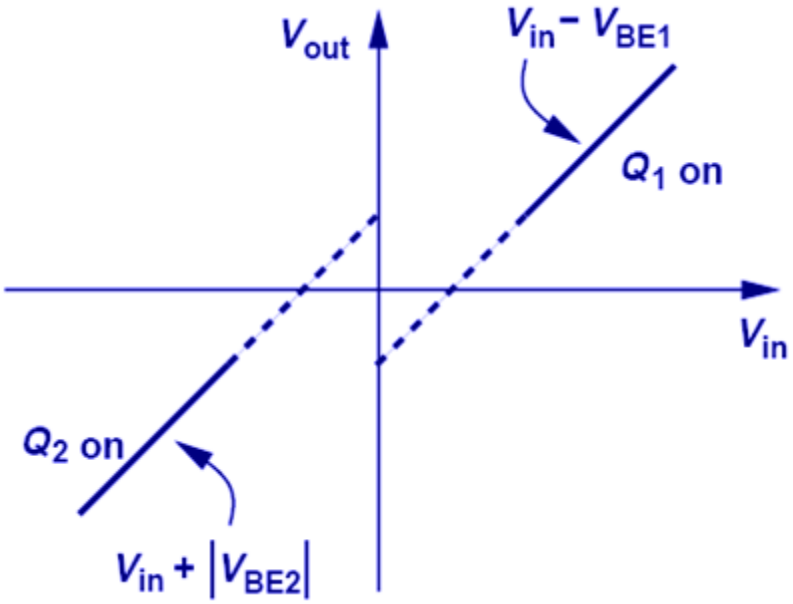
- **As Vin decreases the output waveform will be clipped, introducing nonlinearity in I/O characteristics.**

Push-Pull Stage



- As V_{in} increases, Q_1 is on and pushes a current into R_L.
- As V_{in} decreases, Q_2 is on and pulls a current out of R_L.

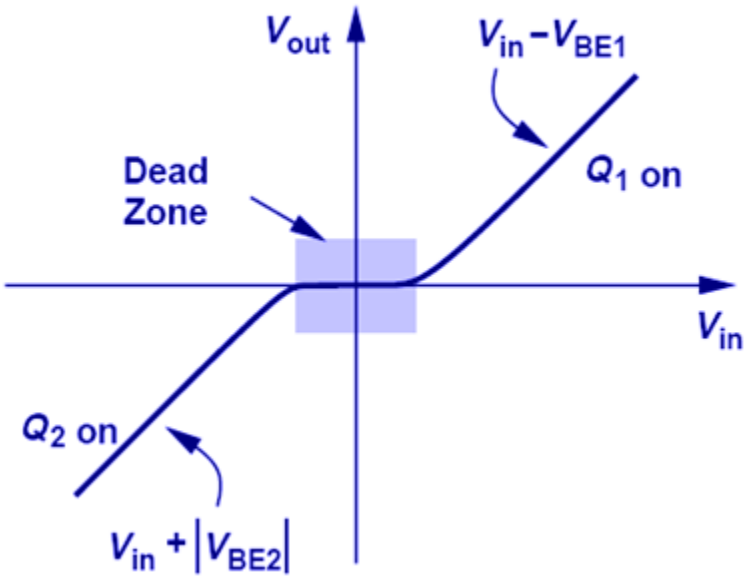
I/O Characteristics for Large V_{in}



$V_{out}=V_{in}-V_{BE1}$ for large $+V_{in}$
$V_{out}=V_{in}+|V_{BE2}|$ for large $-V_{in}$

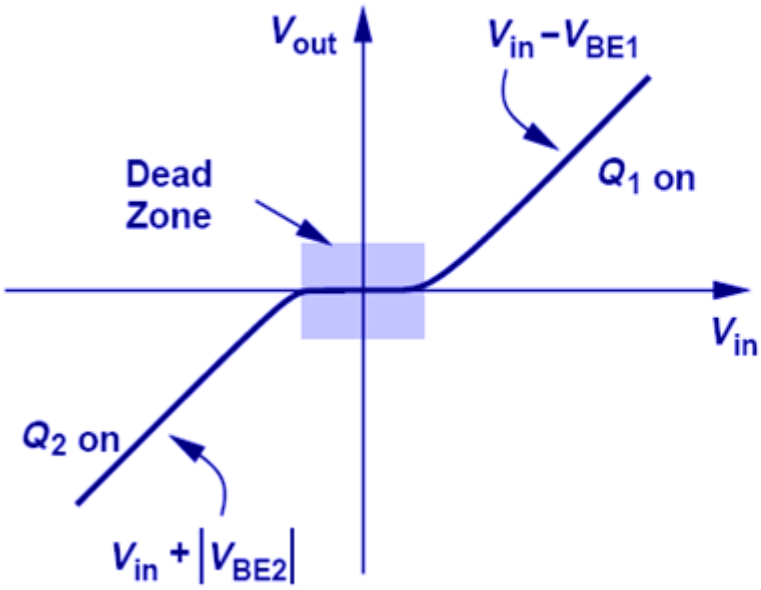
- **For positive V_{in}, Q_1 shifts the output down and for negative V_{in}, Q_2 shifts the output up.**

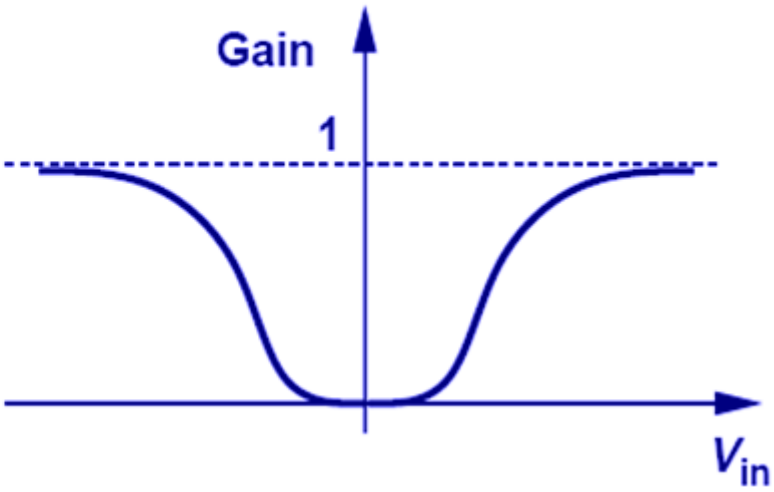
Overall I/O Characteristics of Push-Pull Stage



- **However, for small V_{in}, there is a dead zone (both Q_1 and Q_2 are off) in the I/O characteristic, resulting in gross nonlinearity.**

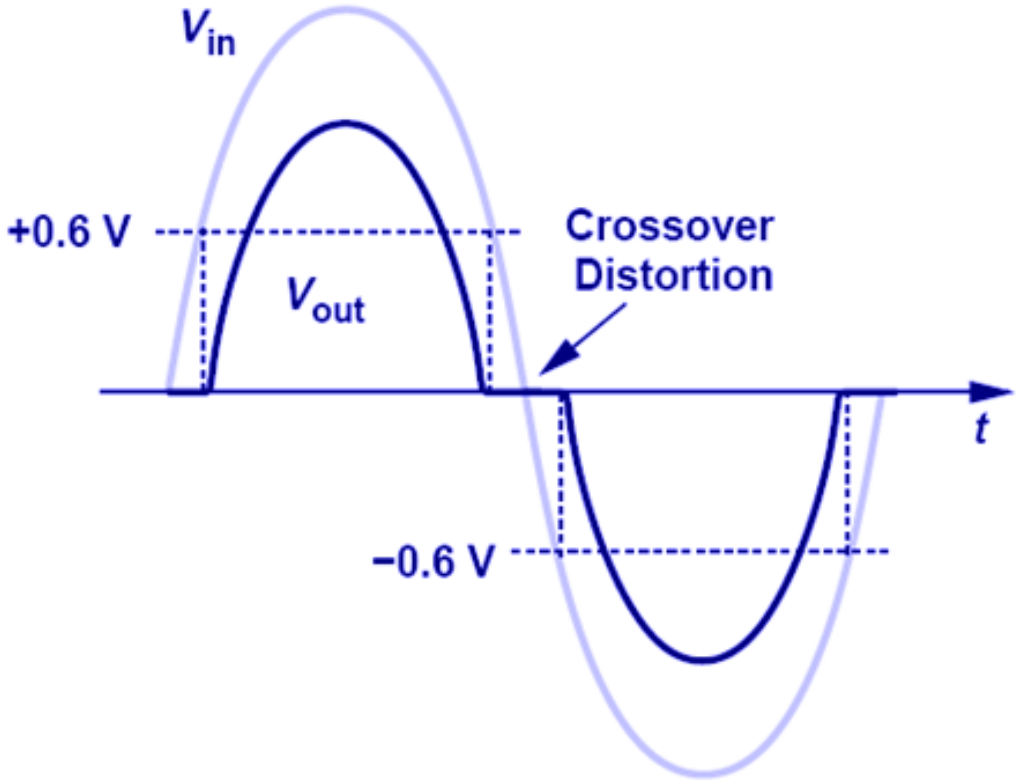
Small-Signal Gain of Push-Pull Stage





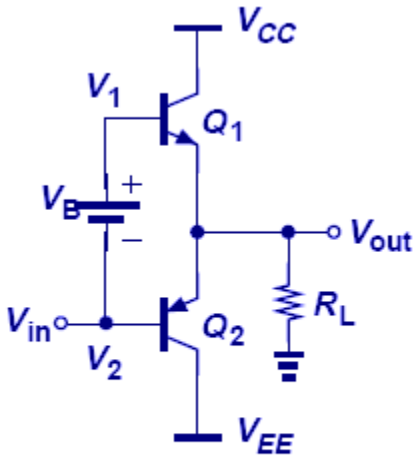
- The push-pull stage exhibits a gain that tends to unity when either Q1 or Q2 is on.
- When Vin is very small, the gain drops to zero.

Sinusoidal Response of Push-Pull Stage

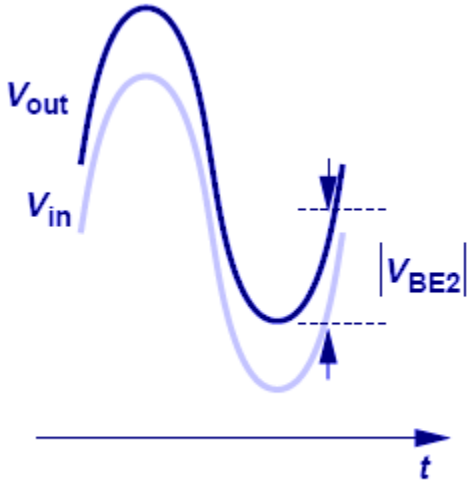


- **For large Vin, the output follows the input with a fixed DC offset, however as Vin becomes small the output drops to zero and causes "Crossover Distortion."**

Improved Push-Pull Stage



(a)



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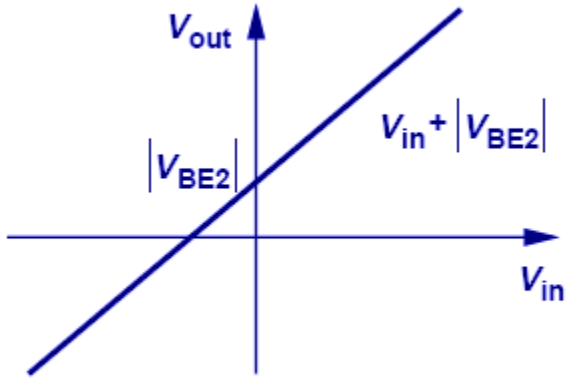
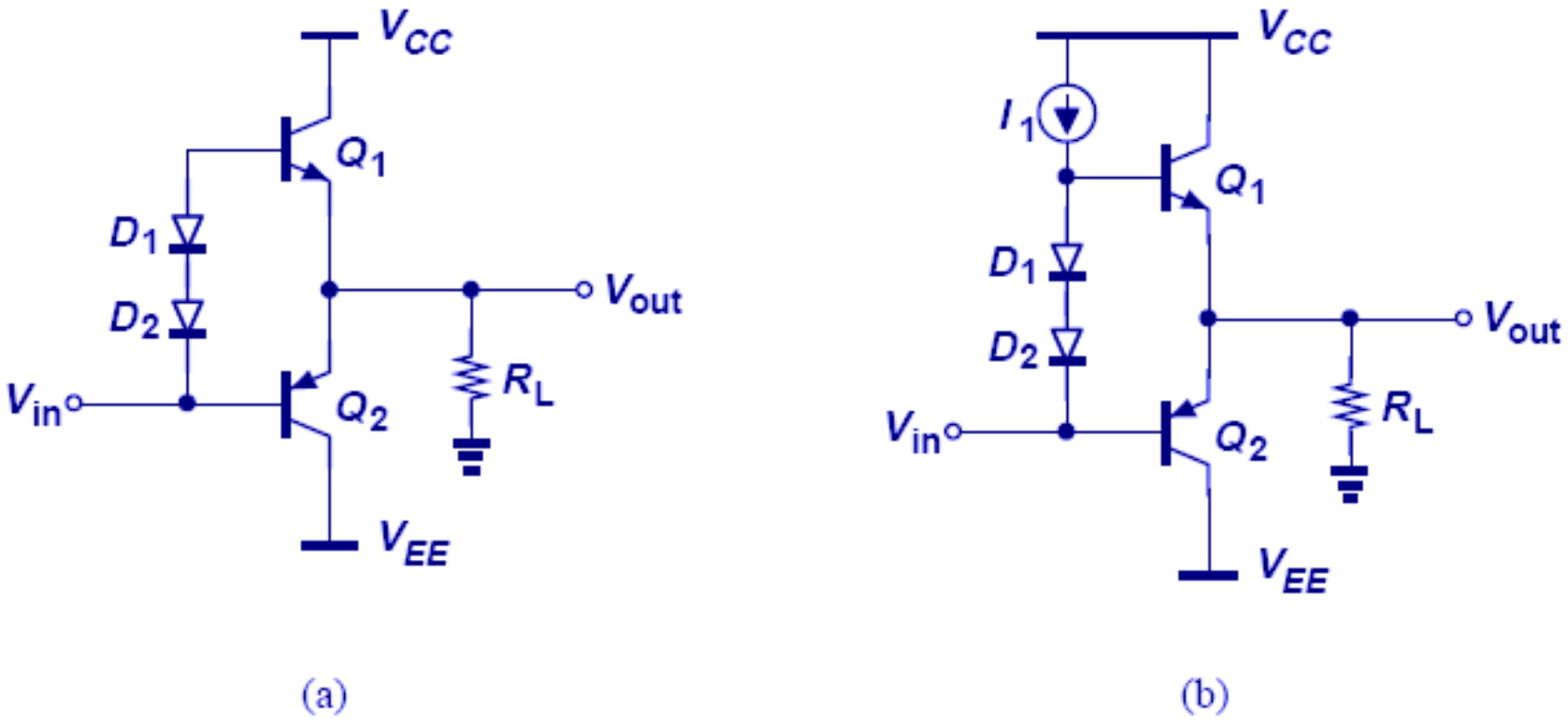


(c)

$$V_B = V_{BE1} + |V_{BE2}|$$

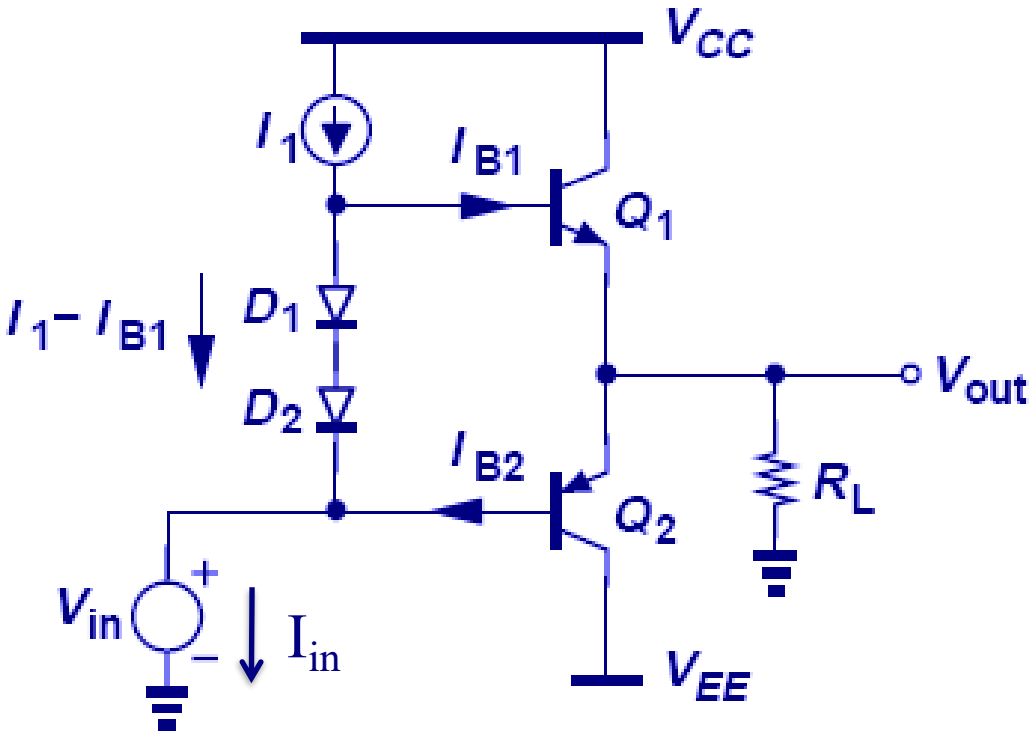
- **With a battery of V_B inserted between the bases of Q_1 and Q_2, the dead zone is eliminated.**

Implementation of V_B



- Since $V_B=V_{BE1}+|V_{BE2}|$, a natural choice would be two diodes in series.
- I_1 in figure (b) is used to bias the diodes and Q_1.

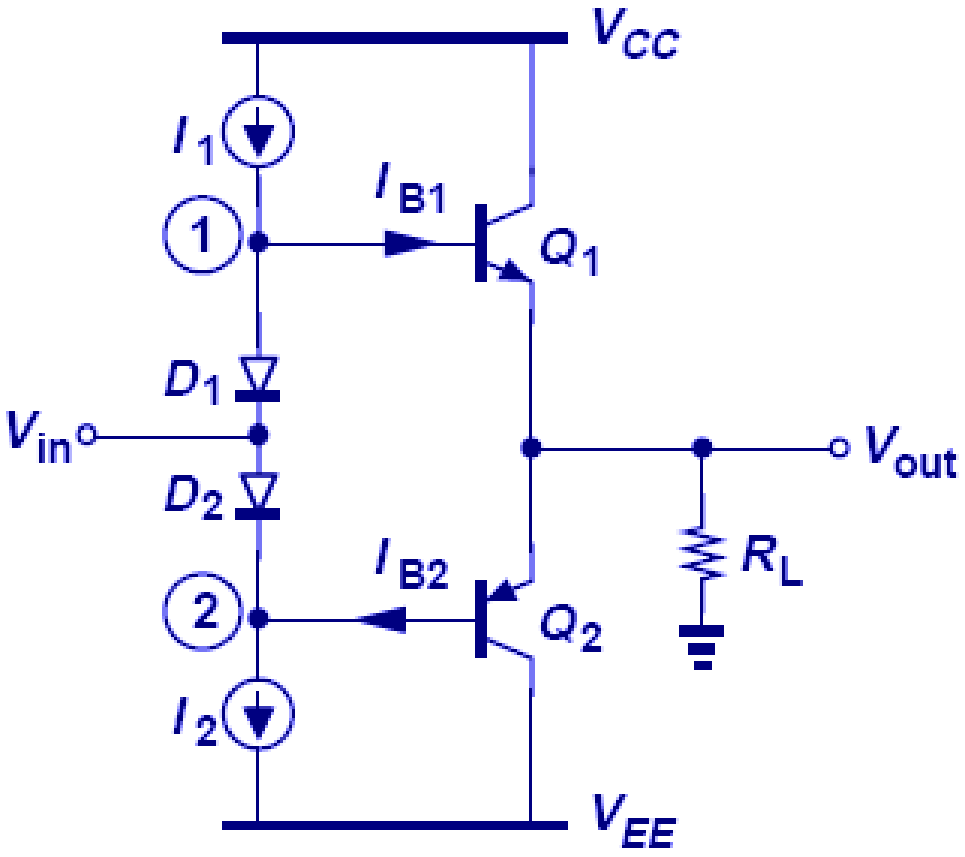
Example: Current Flow I



$$I_{in} = I_1 - I_{B1} + |I_{B2}|$$

If $V_{out}=0$ & $\beta_1=\beta_2>>1$
$\Rightarrow I_{B1}=I_{B2}$

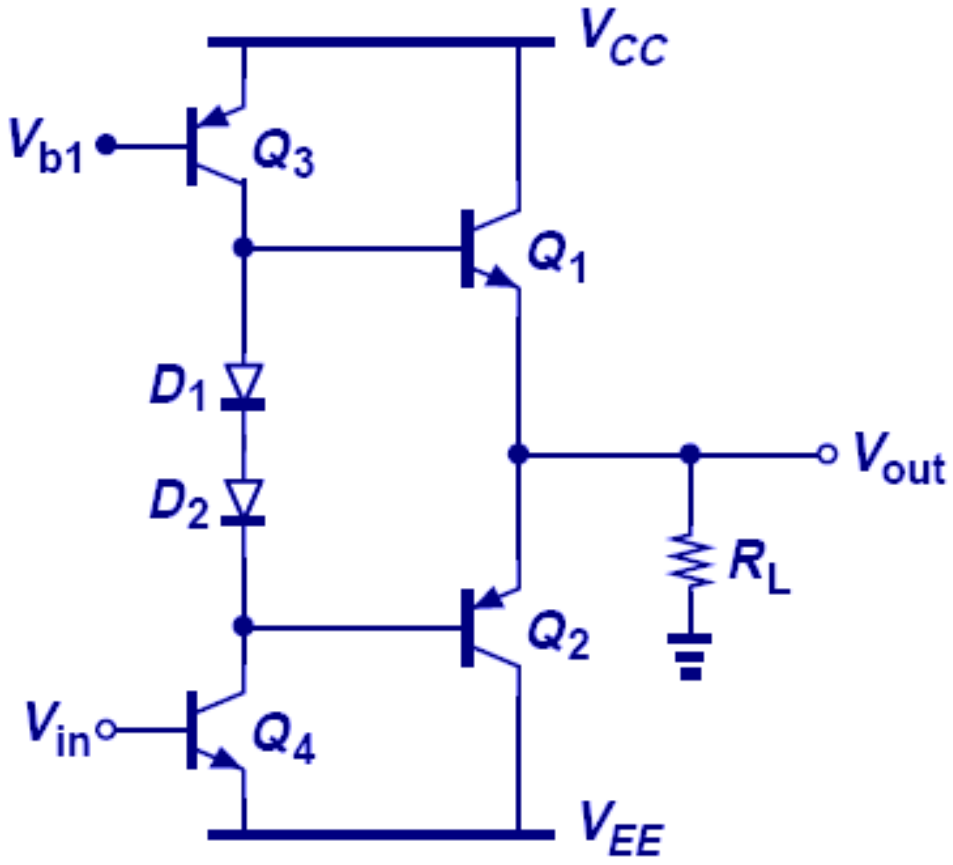
Example: Current Flow II



$V_{D1} \approx V_{BE} \rightarrow V_{out} \approx V_{in}$

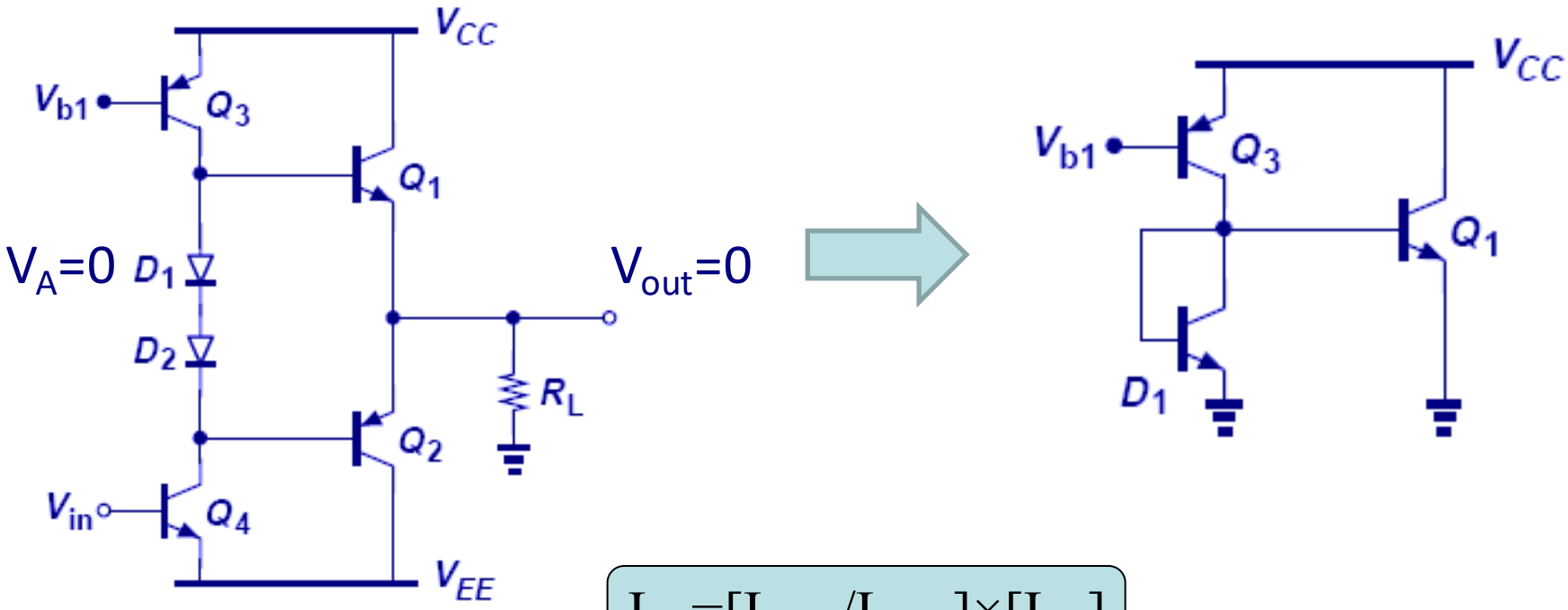
If $I_1 = I_2$ & $I_{B1} \approx I_{B2}$
$\rightarrow I_{in} = 0$ when $V_{out} = 0$

Addition of CE Stage



- **A CE stage (Q_4) is added to provide voltage gain from the input to the bases of Q_1 and Q_2.**

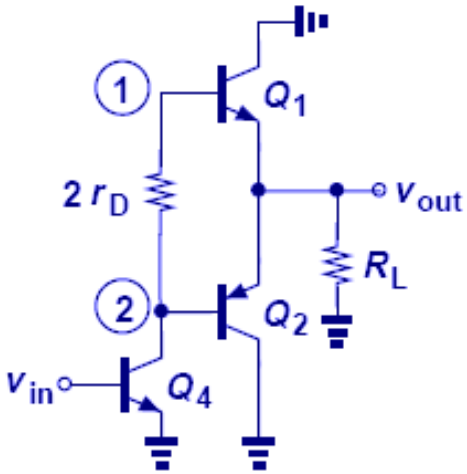
Bias Point Analysis

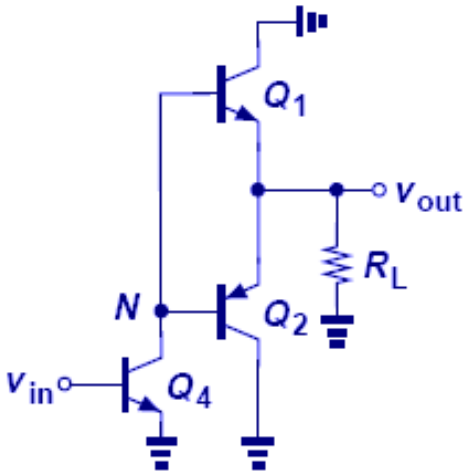


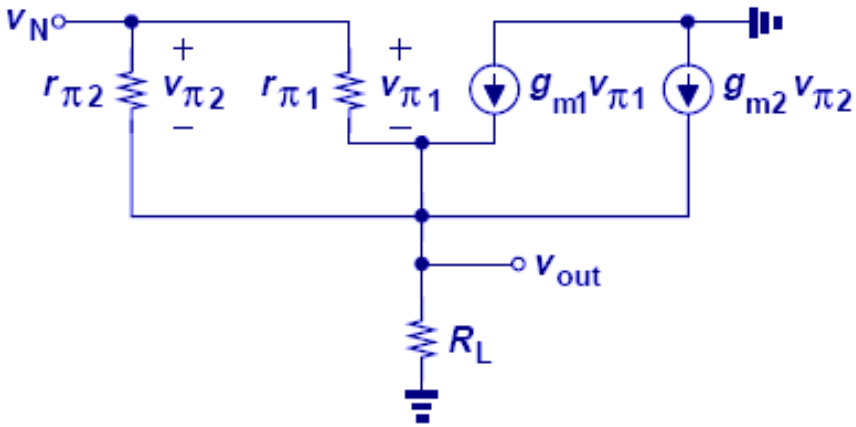
$$I_{C1}=[I_{S,Q1}/I_{S,D1}]\times[I_{C3}]$$

- **For bias point analysis, the circuit can be simplified to the one on the right, which resembles a current mirror.**
- **The relationship of I_{C1} and I_{Q3} is shown above.**

Small-Signal Analysis



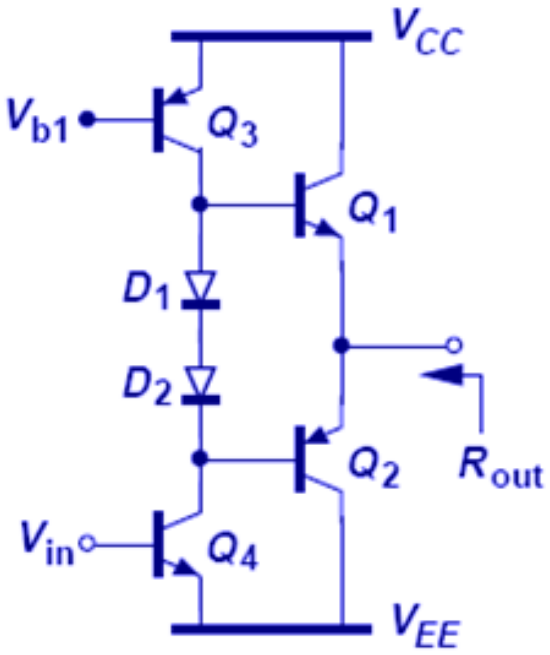


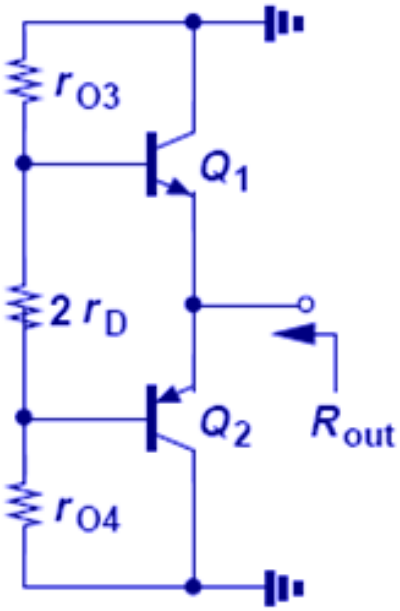


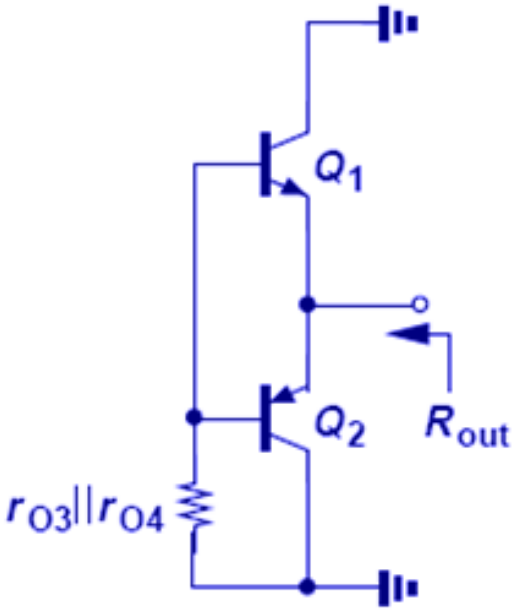
$$A_V = -g_{m4}(r_{\pi 1} \| r_{\pi 2})(g_{m1}+g_{m2})R_L$$

- **Assuming $2r_D$ is small and $(g_{m1}+g_{m2})R_L$ is much greater than 1, the circuit has a voltage gain shown above.**

Output Resistance Analysis



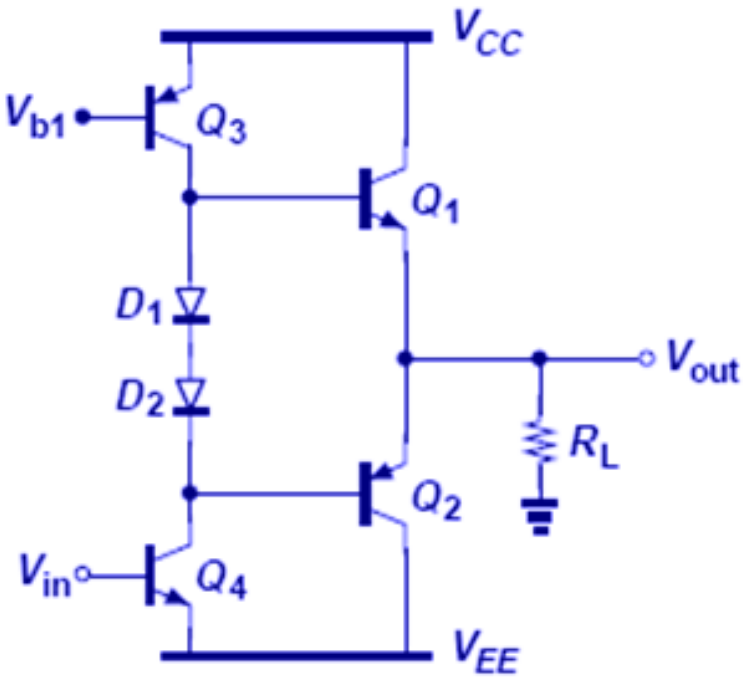




$$R_{out} \approx \frac{1}{g_{m1}+g_{m2}} + \frac{r_{O3} \| r_{O4}}{(g_{m1}+g_{m2})(r_{\pi 1} \| r_{\pi 2})}$$

- **If β is low, the second term of the output resistance will rise, which will be problematic when driving a small resistance.**

Example: Biasing



CE A_V=5
Output Stage A_V=0.8
R_L=8Ω
$\beta_{npn} = 2\beta_{pnp}$=100
$I_{C1} \approx I_{C2}$

$$g_{m1} + g_{m2} = \frac{1}{2\Omega}$$

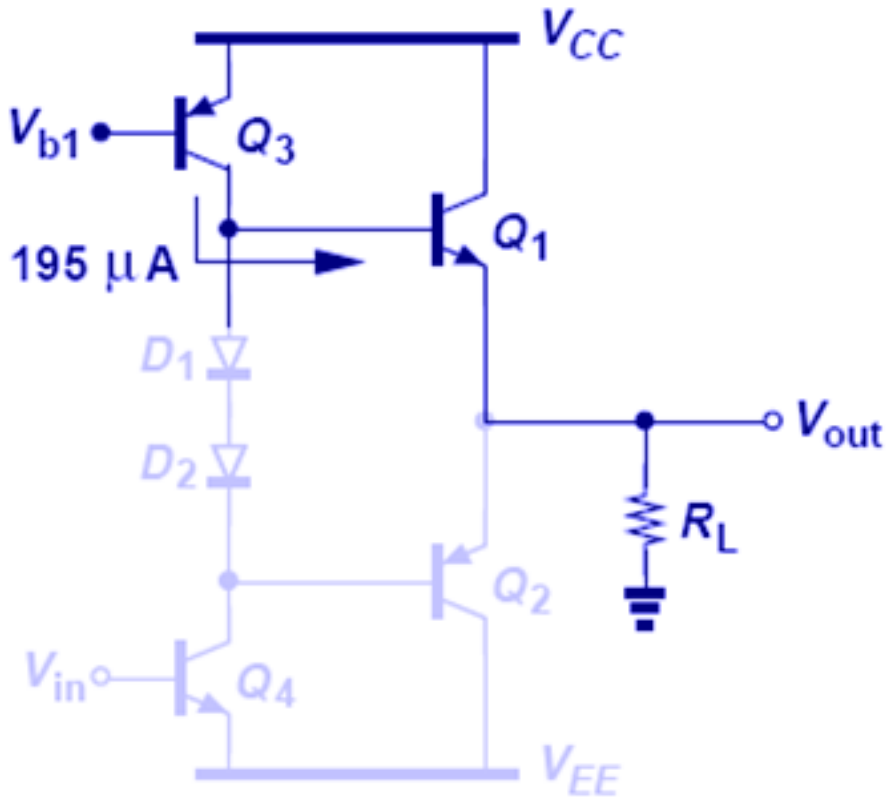
$$g_{m1} \approx g_{m2} \approx (4\Omega)^{-1}$$

$$I_{C1} \approx I_{C2} \approx 6.5mA$$

$$r_{\pi 1} \| r_{\pi 2} = 133\Omega$$

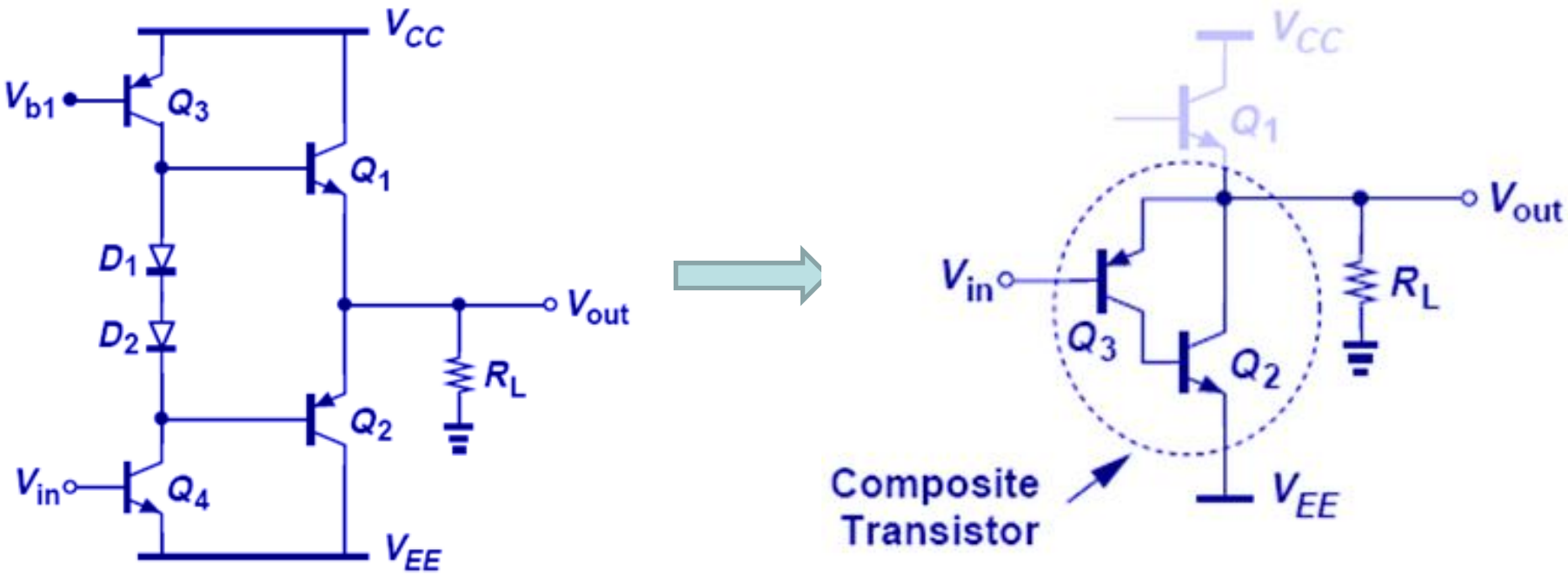
$$I_{C3} \approx I_{C4} \approx 195\mu A$$

Problem of Base Current



- **195 μA of base current in Q_1 can only support 19.5 mA of collector current, insufficient for high current operation (hundreds of mA).**

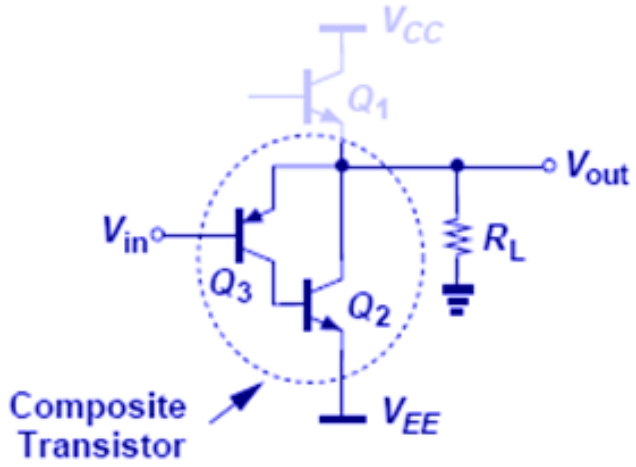
Modification of the PNP Emitter Follower

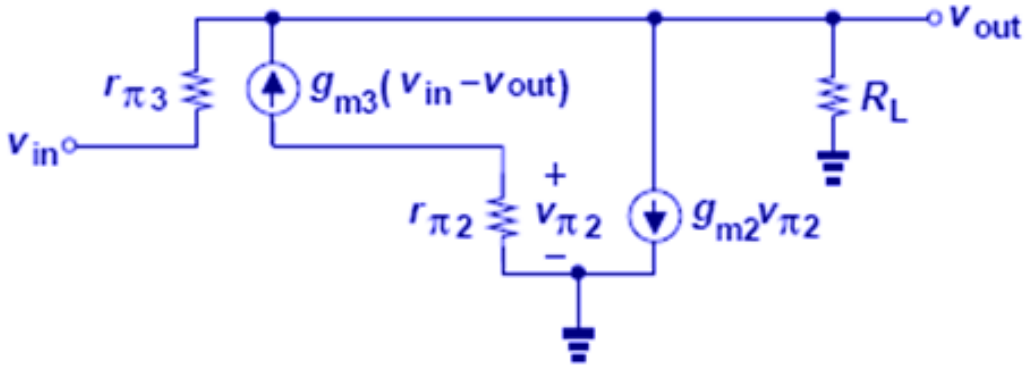


$$R_{out} \approx \frac{1}{(\beta_2 + 1) g_{m3}}$$

- **Instead of having a single PNP as the emitter-follower, it is now combined with an NPN (Q_2), providing a lower output resistance.**

Example: Input Resistance

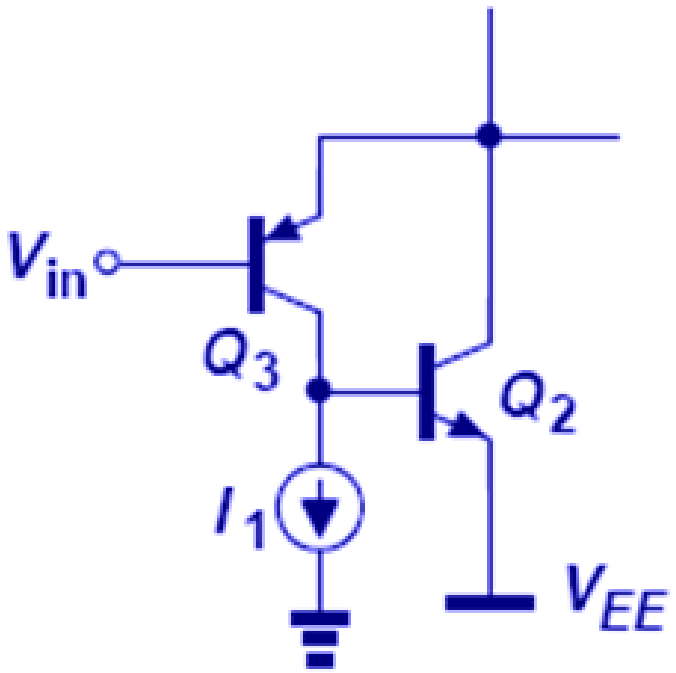




$$i_{in} = \frac{1}{r_{\pi 3}}\left(v_{in} - v_{in}\frac{R_L}{R_L + \dfrac{1}{(\beta_2 + 1)g_{m3}}} \right)$$

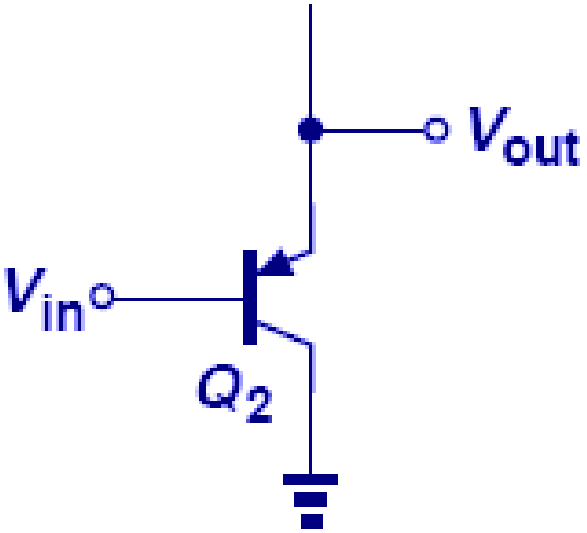
$$r_{in} = \beta_3(\beta_2 + 1)R_L + r_{\pi 3}$$

Additional Bias Current

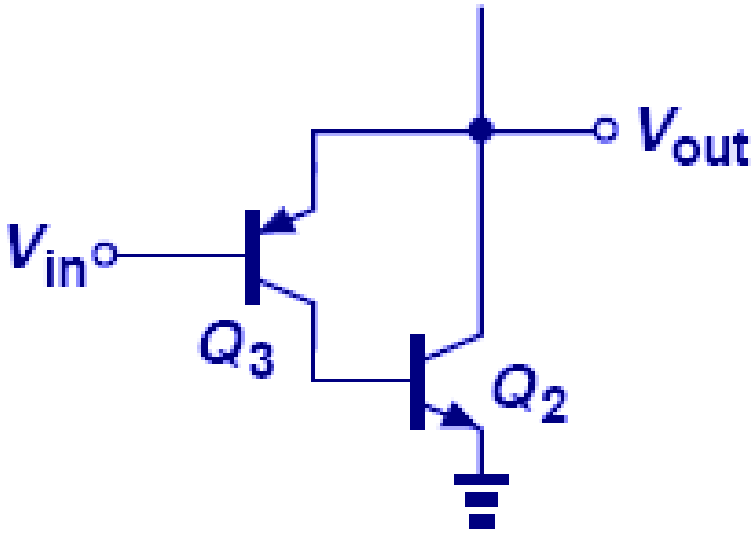


- **I_1 is added to the base of Q_2 to provide an additional bias current to Q_3 so the capacitance at the base of Q_2 can be charged/discharged quickly.**

Example: Minimum V_{in}



(a)

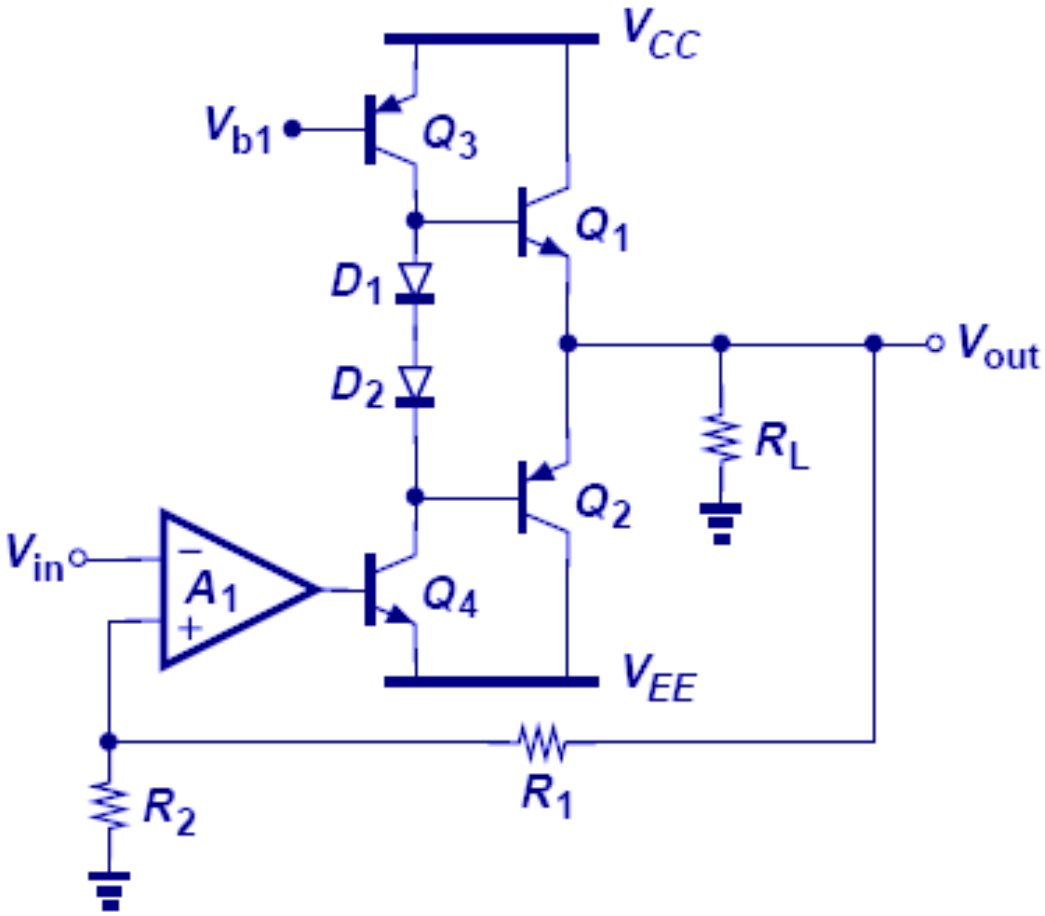


(b)

Min $V_{in} \approx 0$
$V_{out} \approx |V_{EB2}|$

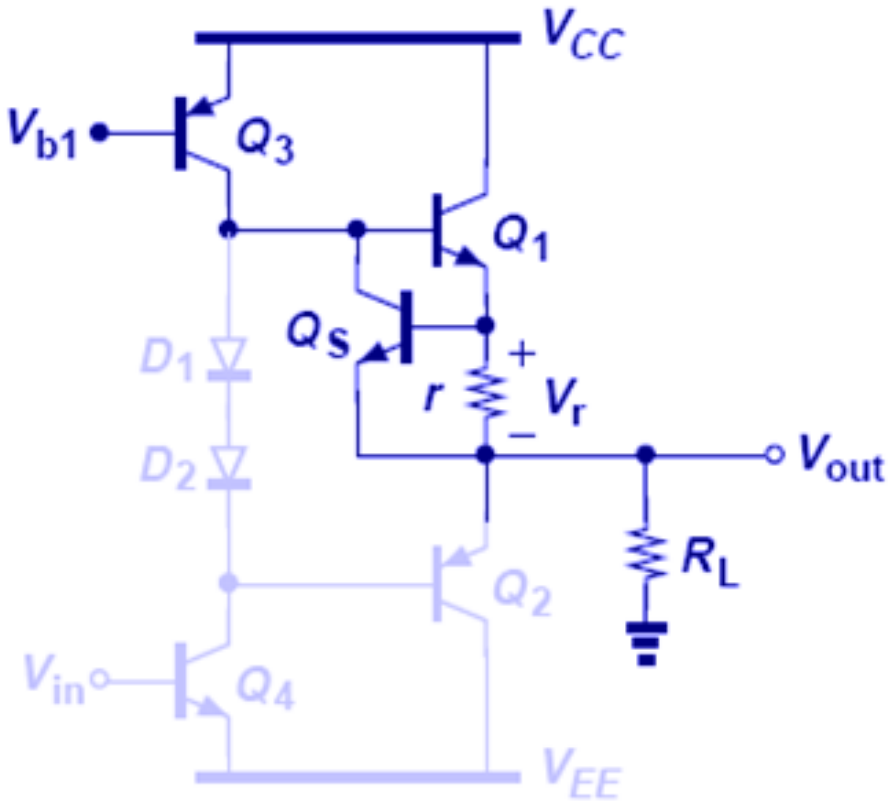
Min $V_{in} \approx V_{BE2}$
$V_{out} \approx |V_{EB3}| + V_{BE2}$

HiFi Design



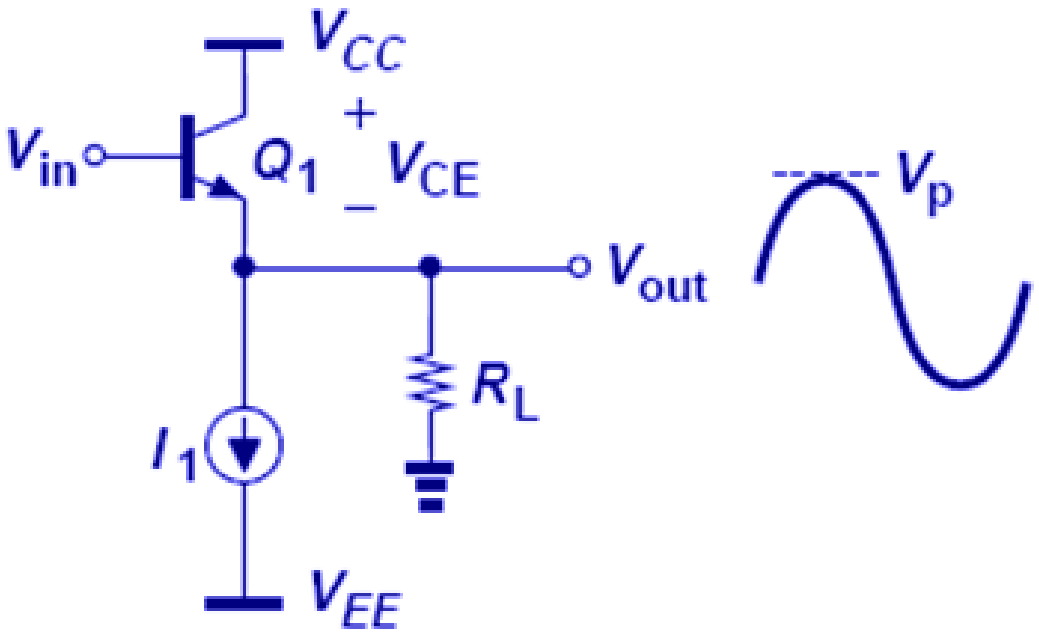
- **Using negative feedback, linearity is improved, providing higher fidelity.**

Short-Circuit Protection



- **Q_s and r are used to "steal" some base current away from Q_1 when the output is accidentally shorted to ground, preventing short-circuit damage.**

Emitter Follower Power Rating

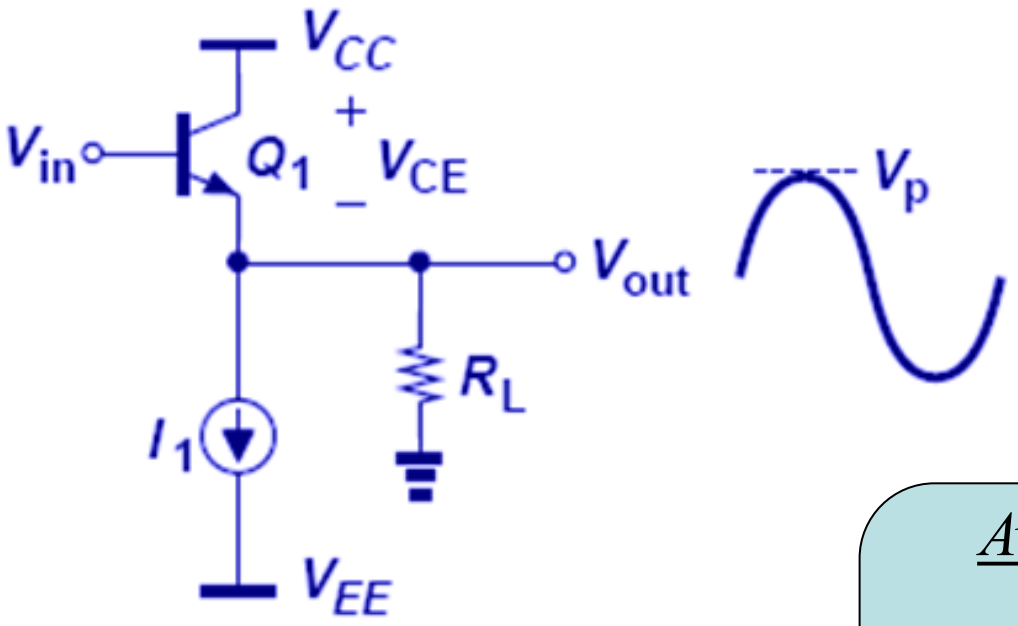


$$P_{av} = I_1\left(V_{CC} - \frac{V_P}{2}\right)$$

$$P_{av,\max} = T_1 V_{CC}$$

- **Maximum power dissipated across Q_1 occurs in the *absence* of a signal.**

Example: Power Dissipation

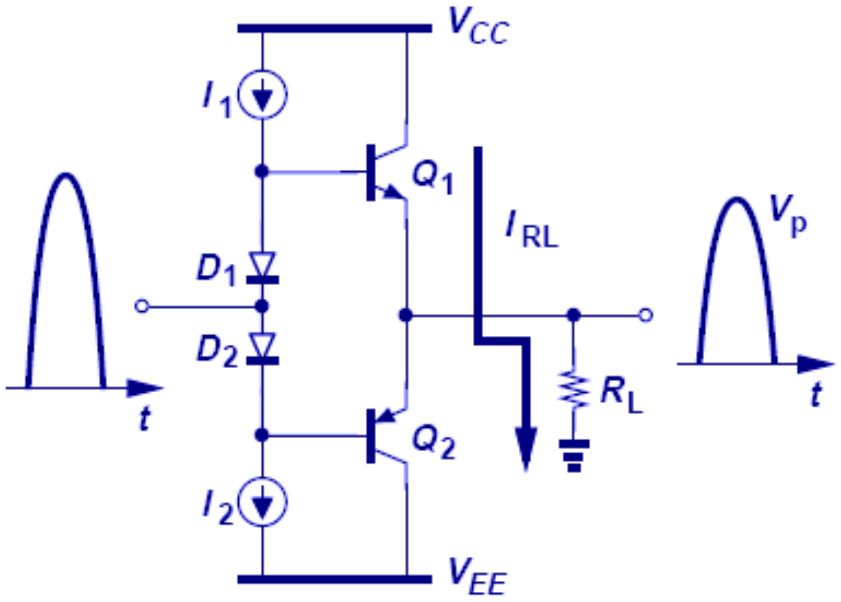


Avg Power Dissipated in I_1

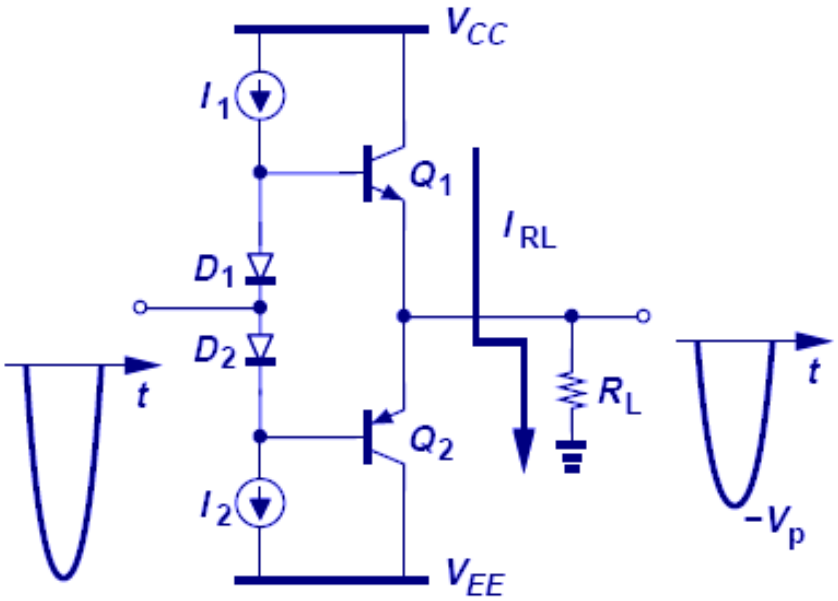
$$P_{I1} = \frac{1}{T}\int_0^T I_1\left(V_p \sin \omega t - V_{EE}\right)dt$$

$$P_{I1} = -I_1 V_{EE}$$

Push-Pull Stage Power Rating



(a)



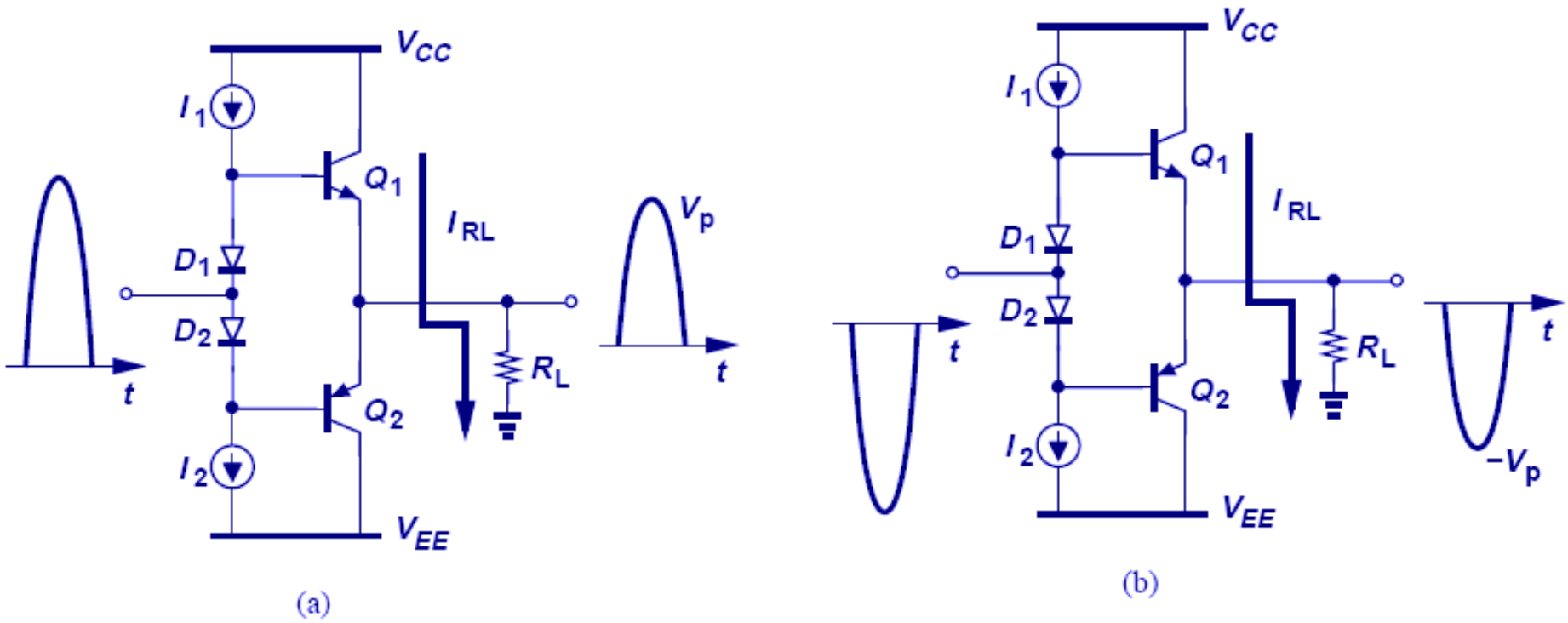
(b)

$$P_{av} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

$$P_{av,\max} = \frac{V_{CC}^2}{\pi^2 R_L}$$

- **Maximum power occurs between V_p=0 and $4V_{cc}/\pi$.**

Example: Push-Pull P_{av}

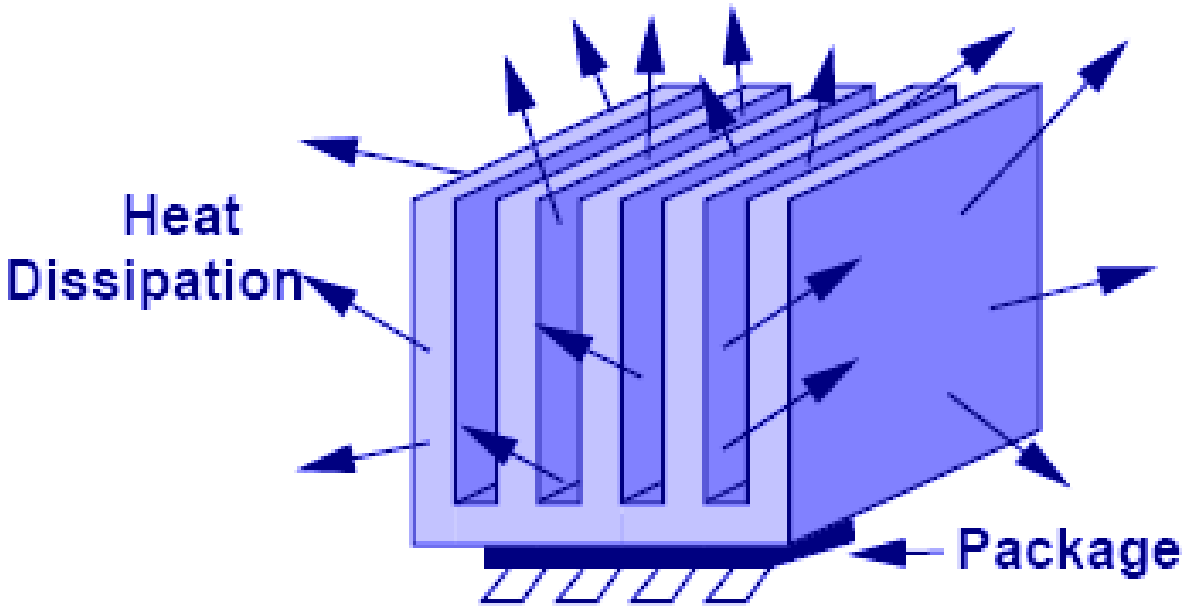


$$P_{av} = \frac{V_P}{R_L}\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

If $V_p = 4V_{CC}/\pi \rightarrow P_{av}=0$

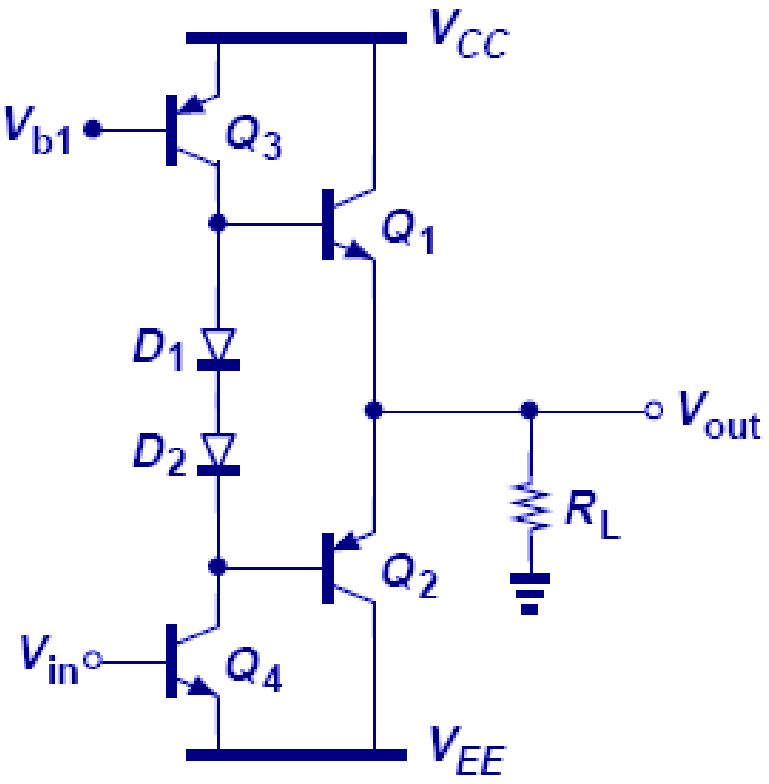
Impossible since V_p cannot go above supply (V_{CC})

Heat Sink



- **Heat sink, provides large surface area to dissipate heat from the chip.**

Thermal Runaway Mitigation



$$\frac{I_{D1}I_{D2}}{I_{S,D1}I_{S,D2}} = \frac{I_{C1}I_{C2}}{I_{S,Q1}I_{S,Q2}}$$

- **Using diode biasing prevents thermal runaway since the currents in Q_1 and Q_2 will track those of D_1 and D_2 as long as theie I_s's track with temperature.**

Efficiency

$$\eta = \frac{P_{out}}{P_{out} + P_{ckt}}$$

Emitter Follower

$$\eta_{EF} = \frac{V_P^2/2R_L}{V_P^2/2R_L + I_1\left(2V_{CC} - V_P/2\right)}$$

$$\eta_{EF} = \frac{V_P}{4V_{CC}} \qquad I_1 = V_P/R_L$$

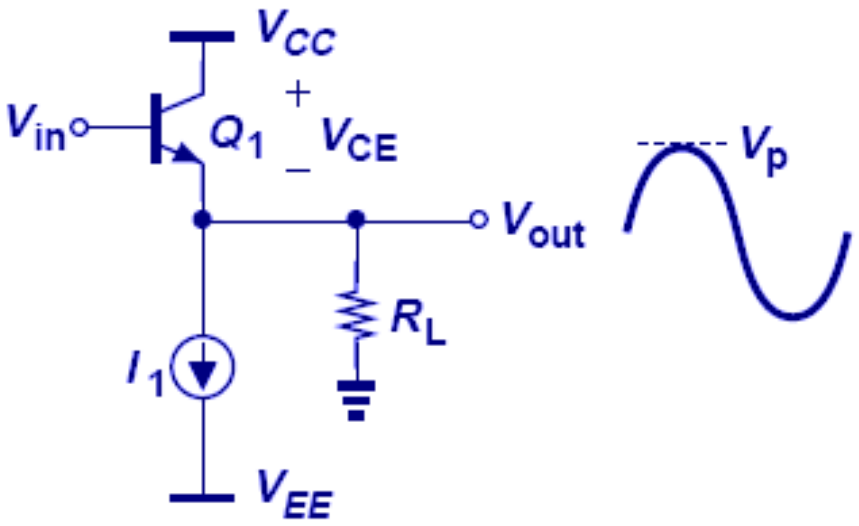
Push-Pull Stage

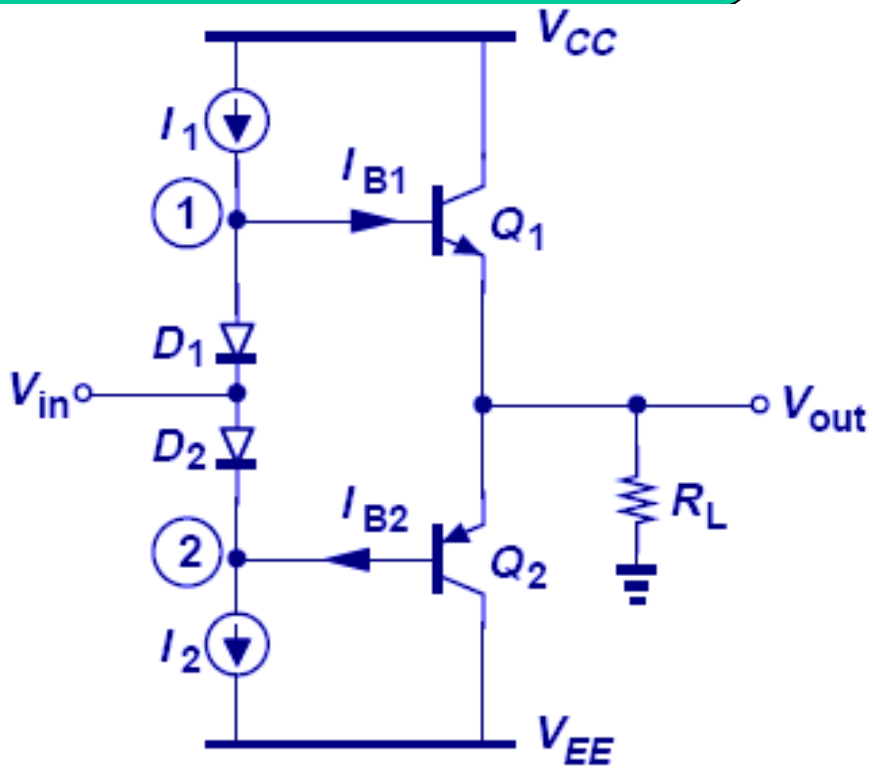
$$\eta_{PP} = \frac{V_P^2/2R_L}{V_P^2/2R_L + 2I_1\left(V_{CC}/\pi - V_P/4\right)}$$

$$\eta_{PP} = \frac{\pi}{4}\frac{V_P}{V_{CC}} \qquad I_1 = V_P/R_L$$

- **Efficiency is defined as the average power delivered to the load divided by the power drawn from the supply**

Example: Efficiency





Emitter Follower

$V_P = V_{CC}/2$

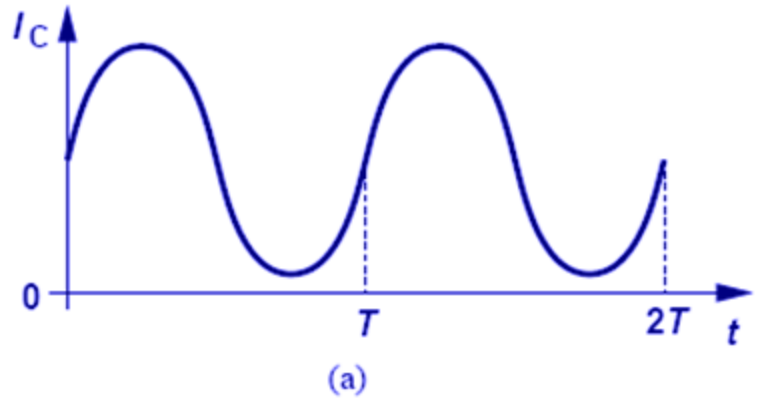
$$\eta = \frac{1}{15}$$

Push-Pull

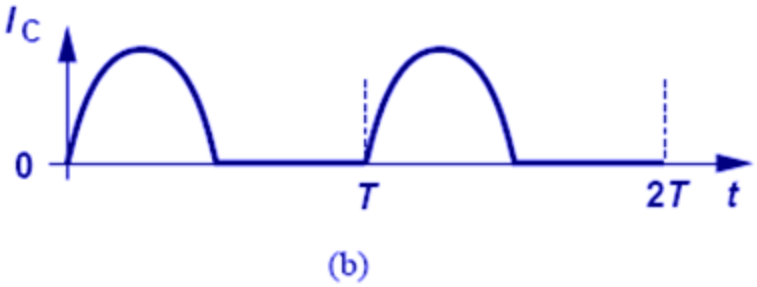
$I_1 = (V_P/R_L)/\beta$

$$\eta = \frac{1}{4}\frac{V_P}{V_{CC}/\pi + V_P/\beta}$$

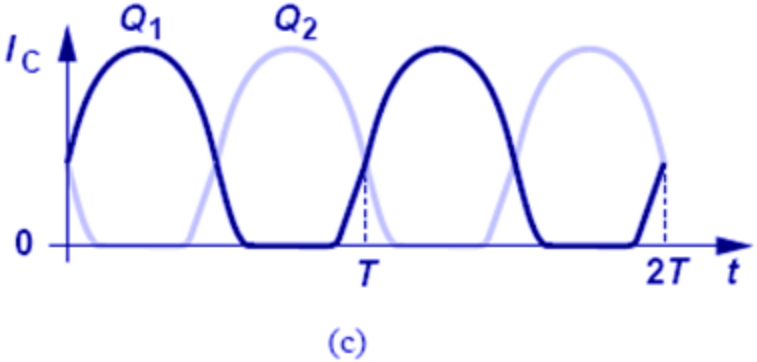
Power Amplifier Classes



Class A: High linearity, low efficiency



Class B: High efficiency, low linearity

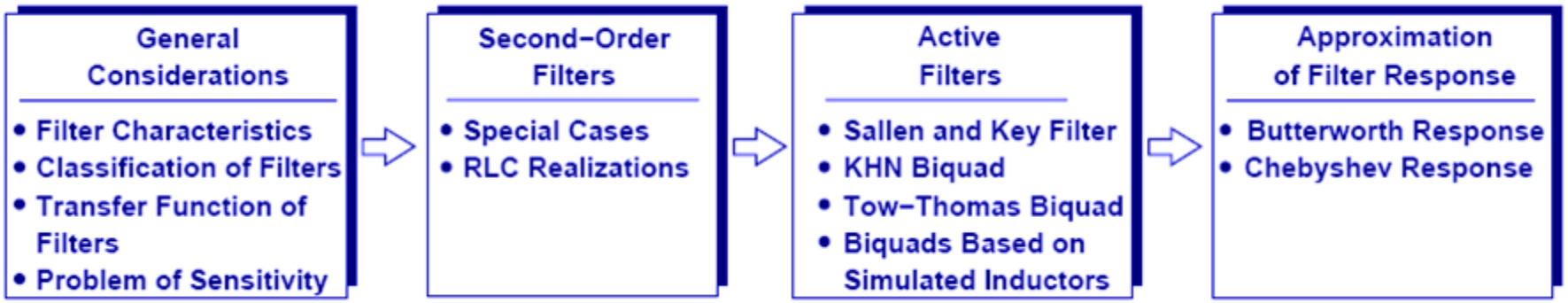


Class AB: Compromise between Class A and B

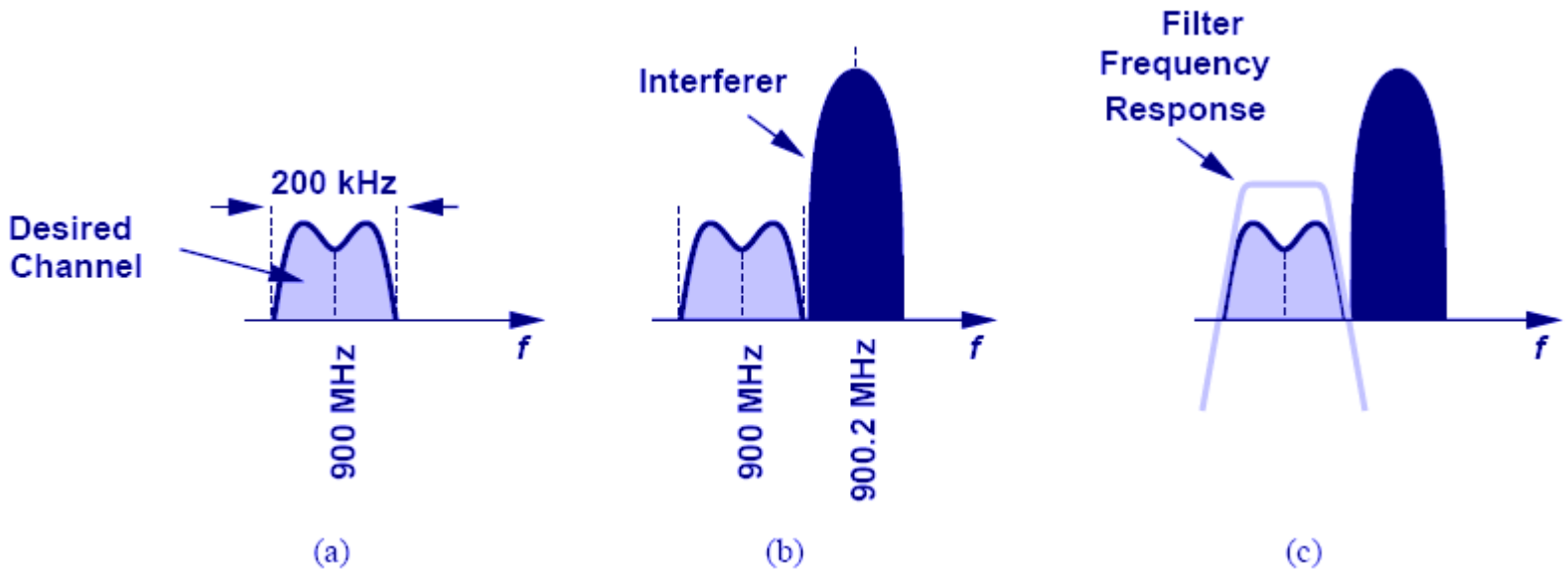
Chapter 14 Analog Filters

- 14.1 General Considerations
- 14.2 First-Order Filters
- 14.3 Second-Order Filters
- 14.4 Active Filters
- 14.5 Approximation of Filter Response

Outline of the Chapter

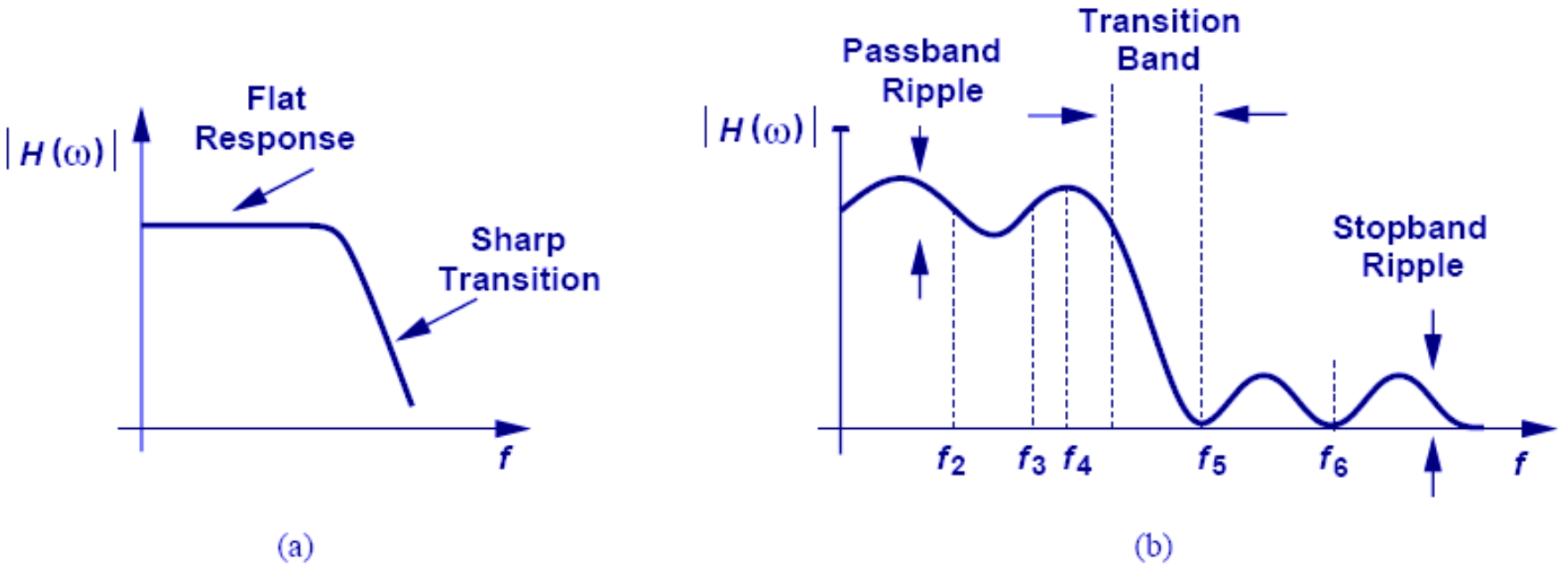


Why We Need Filters



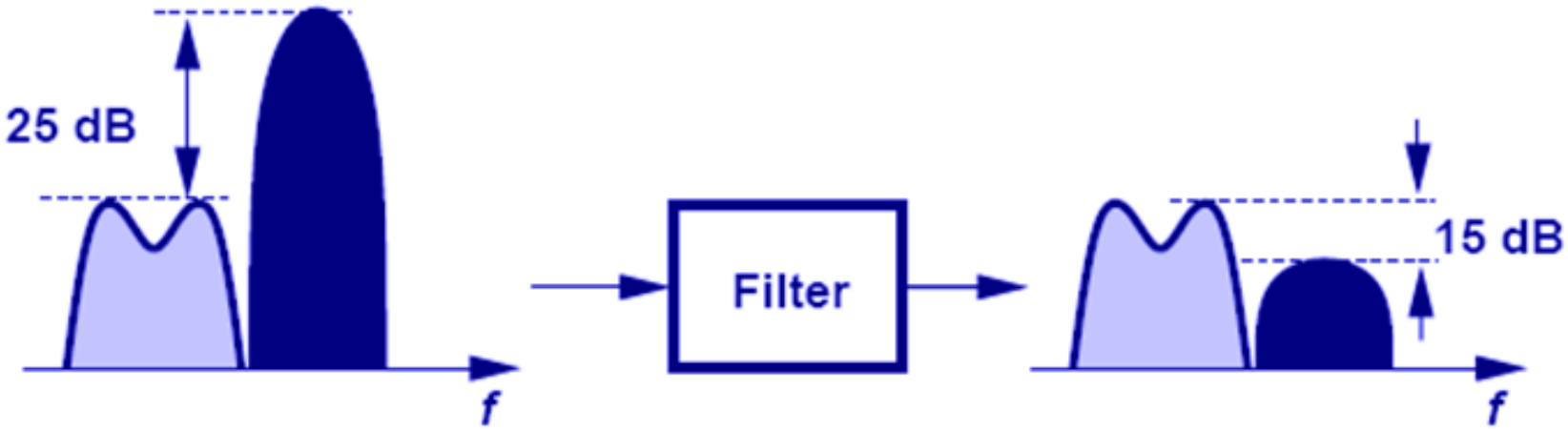
- **In order to eliminate the unwanted interference that accompanies a signal, a filter is needed.**

Filter Characteristics



- **Ideally, a filter needs to have a flat pass band and a sharp roll-off in its transition band.**
- **Realistically, it has a rippling pass/stop band and a transition band.**

Example: Filter I

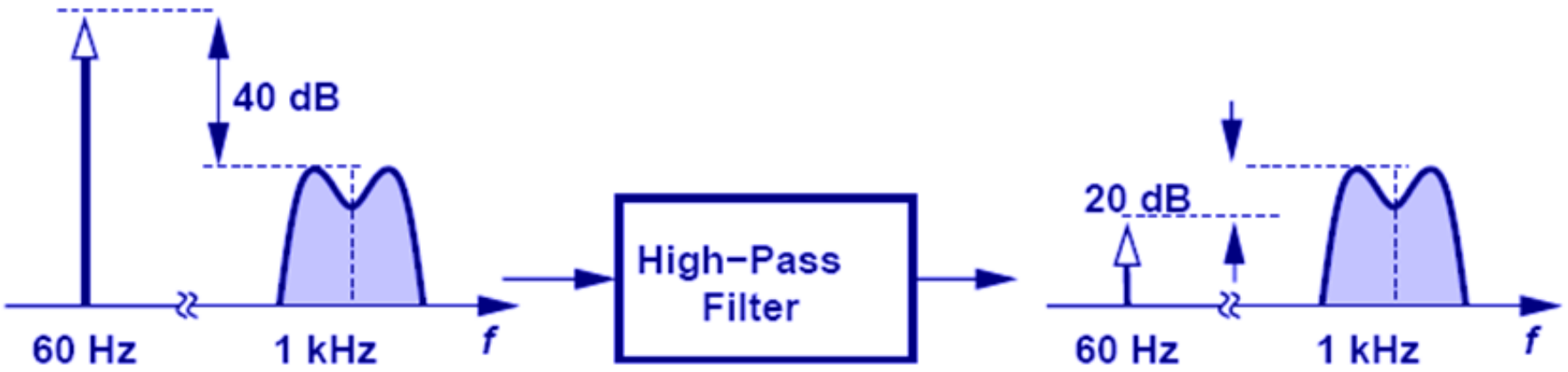


Given: Adjacent channel Interference is 25 dB above the signal

Design goal: Signal to Interference ratio of 15 dB

Solution: A filter with stop band of 40 dB

Example: Filter II

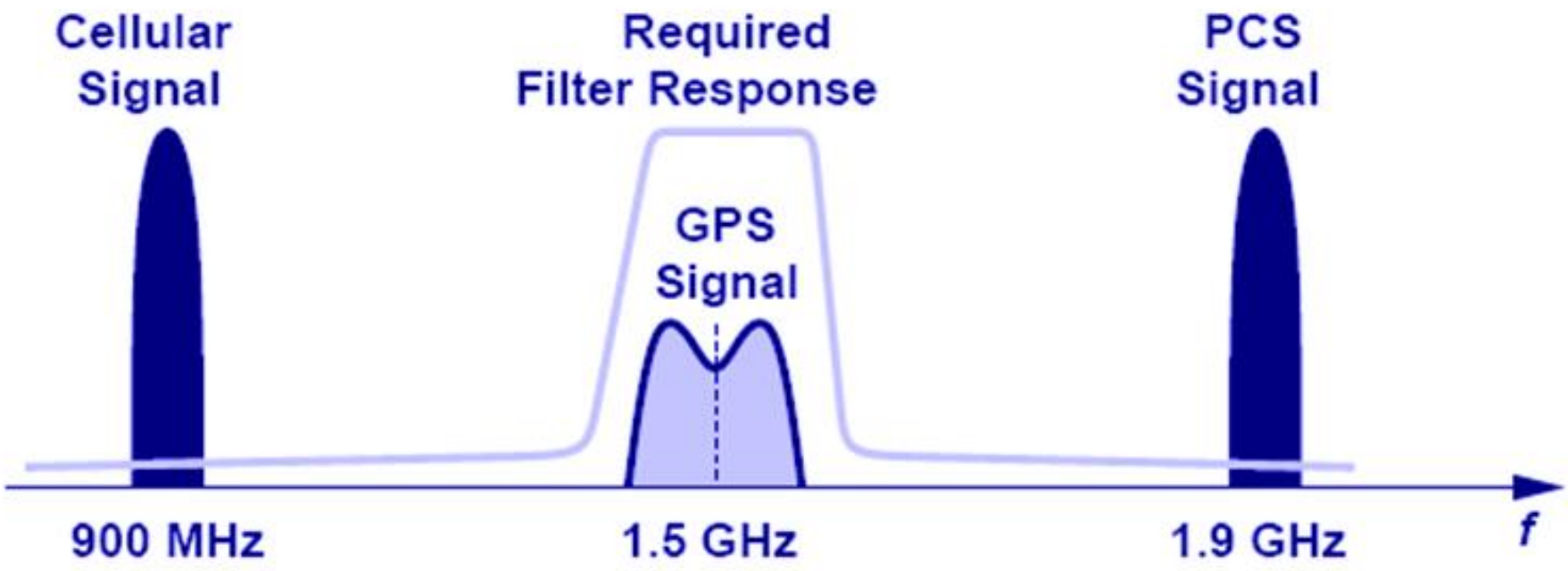


Given: Adjacent channel Interference is 40 dB above the signal

Design goal: Signal to Interference ratio of 20 dB

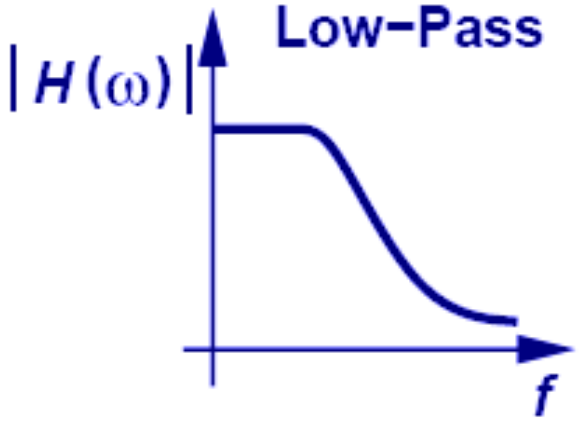
Solution: A filter with stop band of 60 dB at 60 Hz

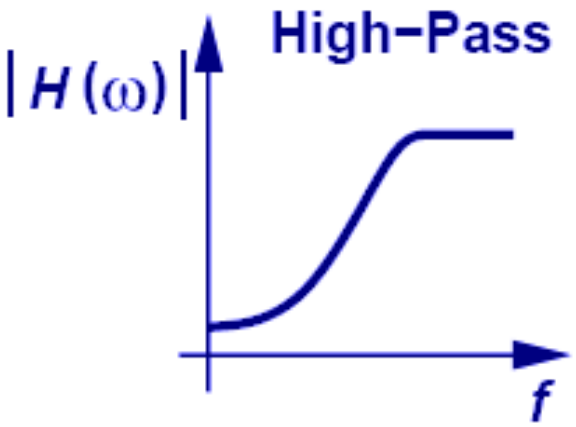
Example: Filter III

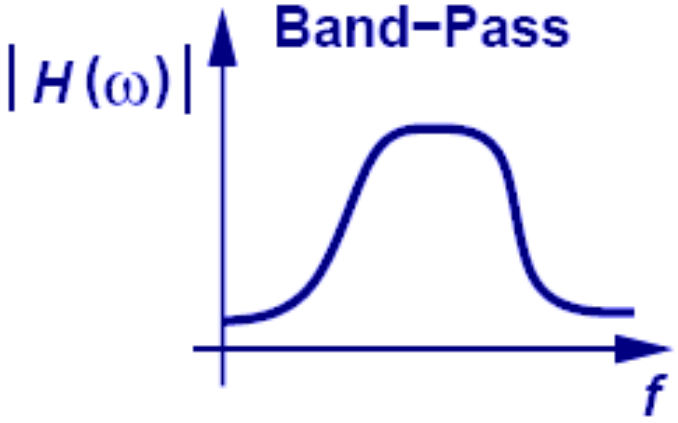


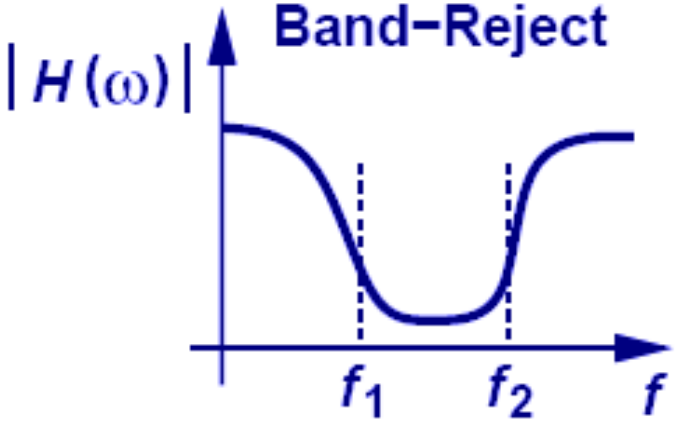
- **A bandpass filter around 1.5 GHz is needed to reject the adjacent Cellular and PCS signals.**

Classification of Filters I

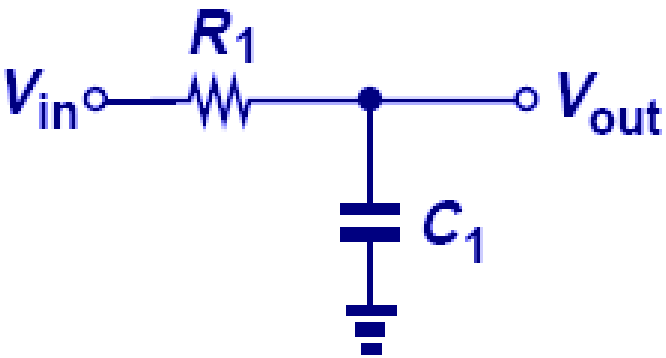




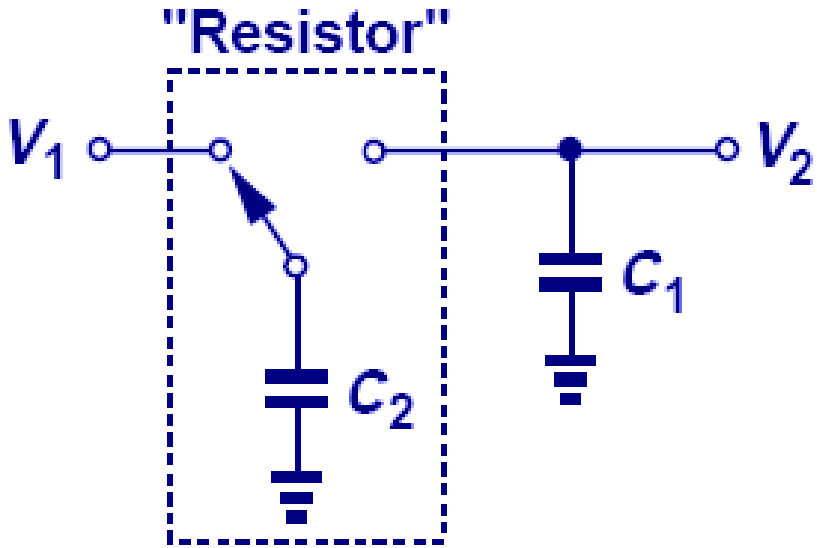




Classification of Filters II



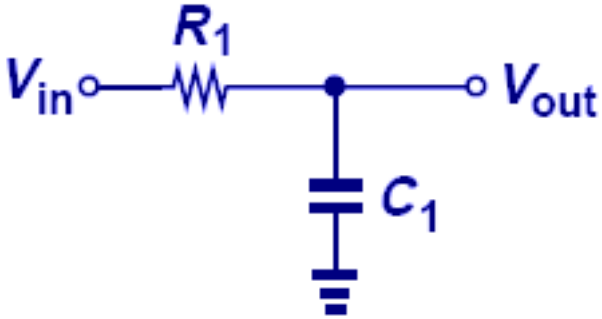
$$R_{eff} = \frac{1}{C_2 f}$$



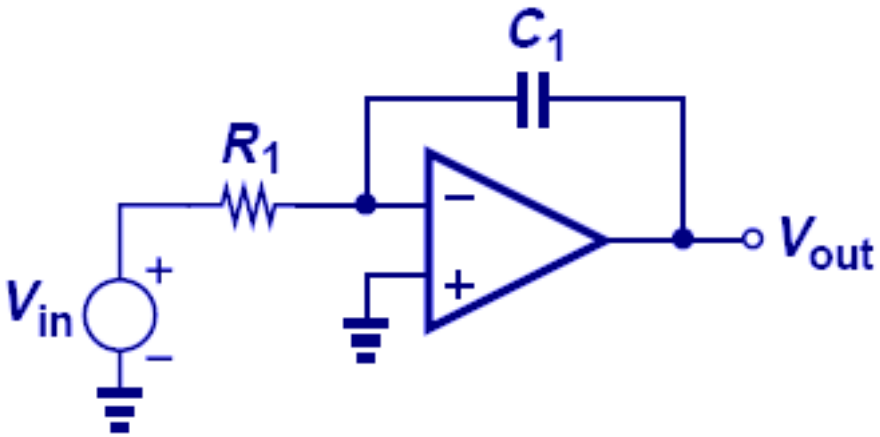
Continuous-time

Discrete-time

Classification of Filters III

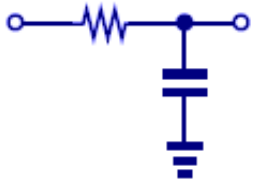
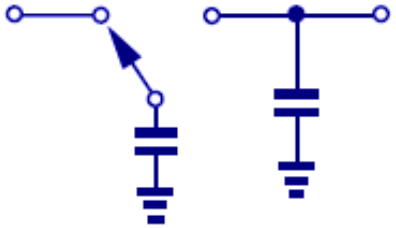
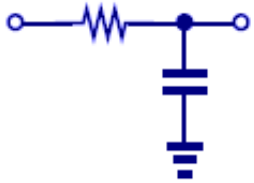
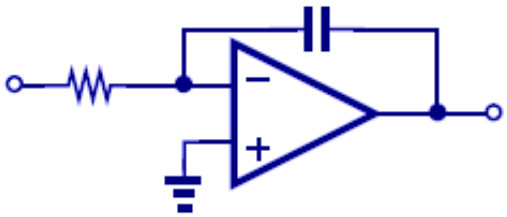


Passive

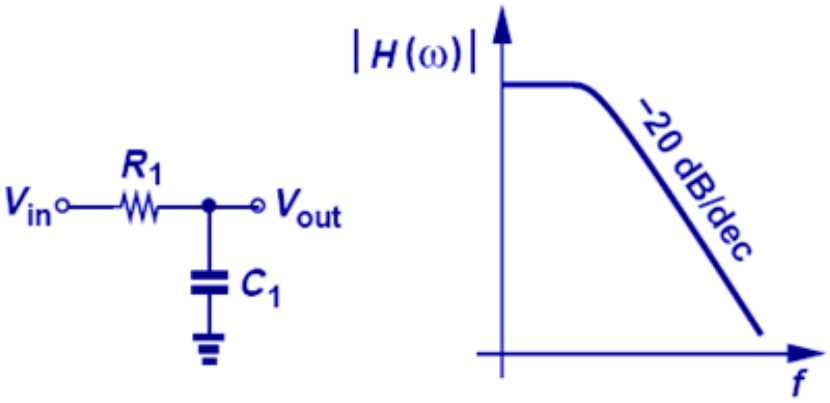


Active

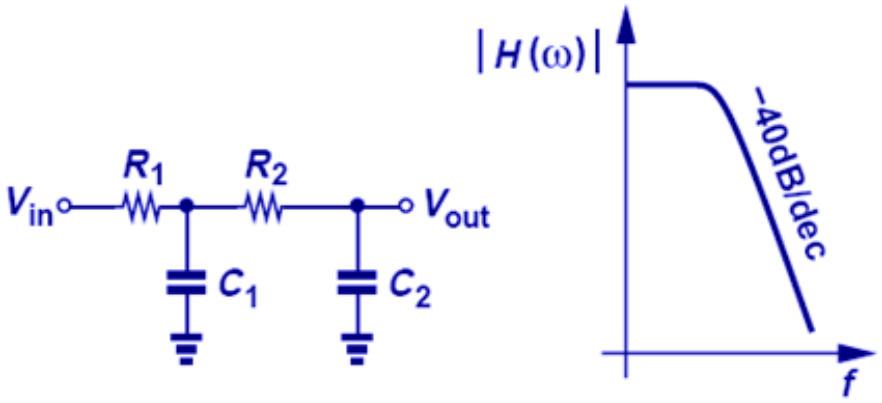
Summary of Filter Classifications

Frequency Response	Low-Pass	High-Pass	Band-Pass	Band-Reject
Continuous-Time and Discrete-Time				
Passive and Active				

Filter Transfer Function



A



B

- **Filter a) has a transfer function with -20dB/dec roll-off**
- **Filter b) has a transfer function with -40dB/dec roll-off, better selectivity.**

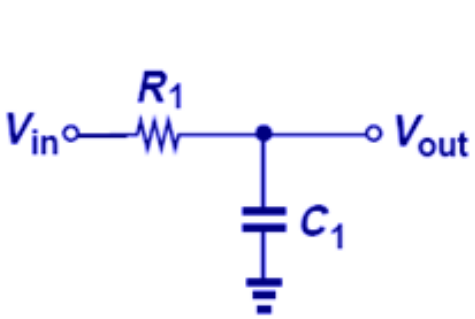
General Transfer Function

$$H(s) = \alpha \frac{(s - Z_1)(s - Z_2)\mathrm{L}\ (s - Z_m)}{(s - P_1)(s - P_2)\mathrm{L}\ (s - P_m)}$$

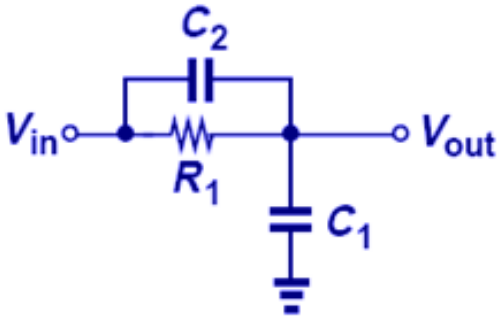
Z_m=m'th zero

P_n =n'th pole

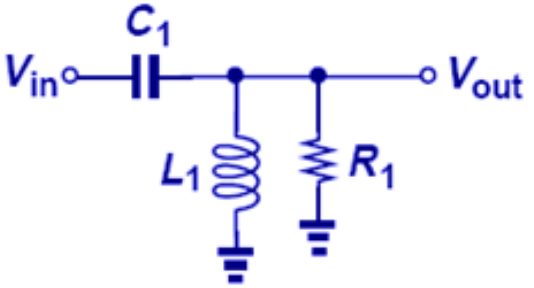
Pole-Zero Diagram



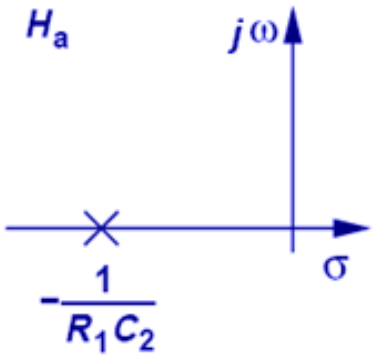
(a)



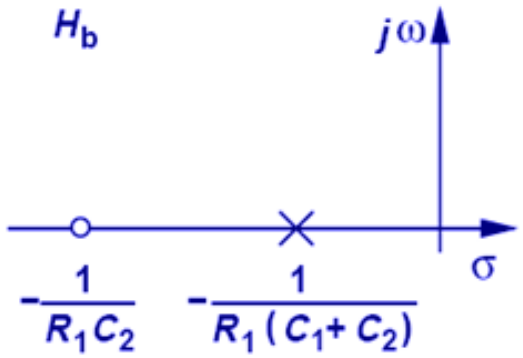
(b)



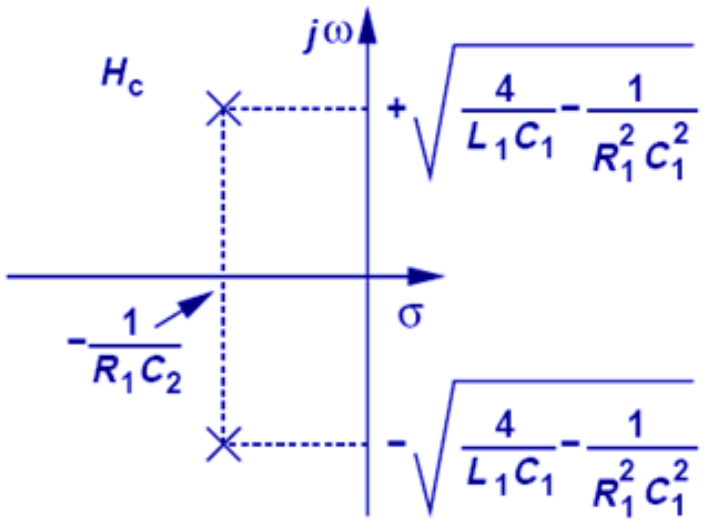
(c)



(a)

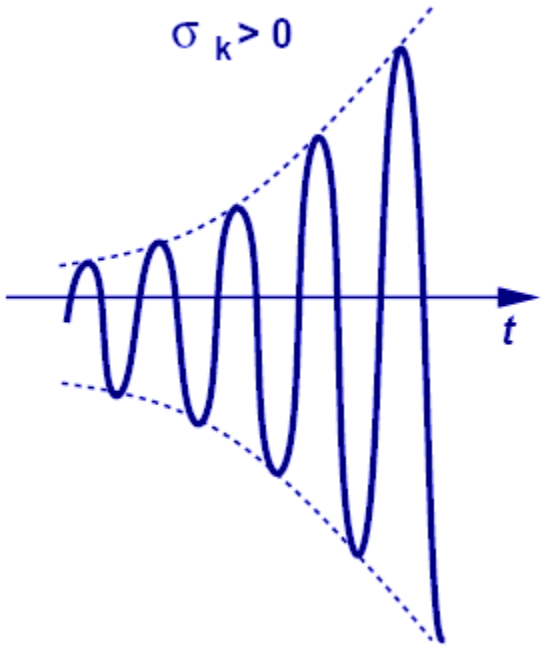


(b)

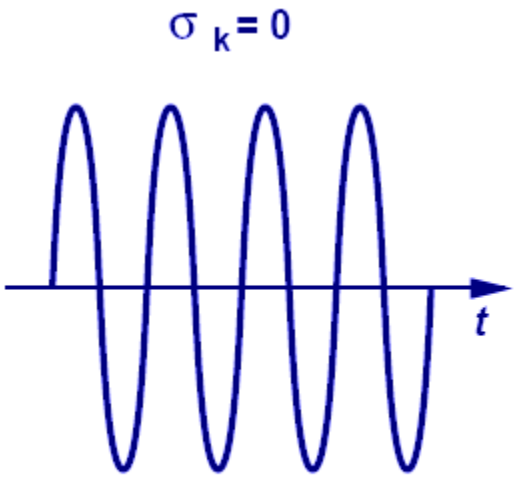


(c)

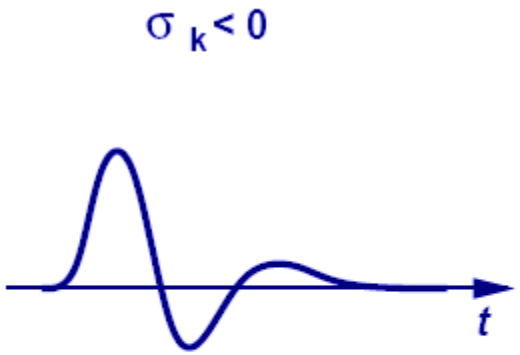
Position of the Poles



Poles on the RHP
Unstable
(no good)

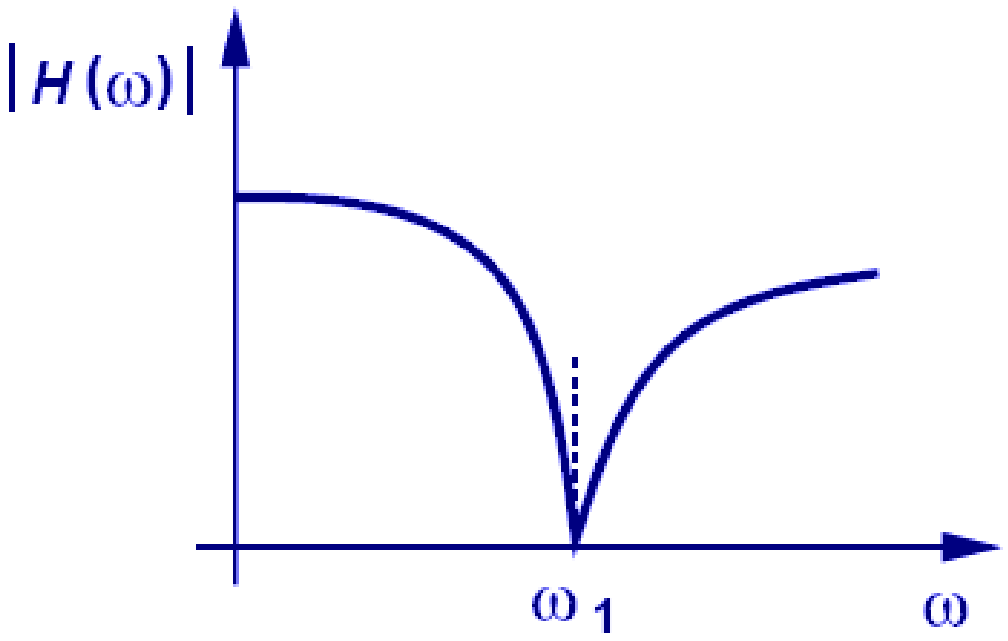


Poles on the jω axis
Oscillatory
(no good)



Poles on the LHP
Decaying
(good)

Imaginary Zero



- **Imaginary zero is used to create a null at certain frequency.**

Sensitivity

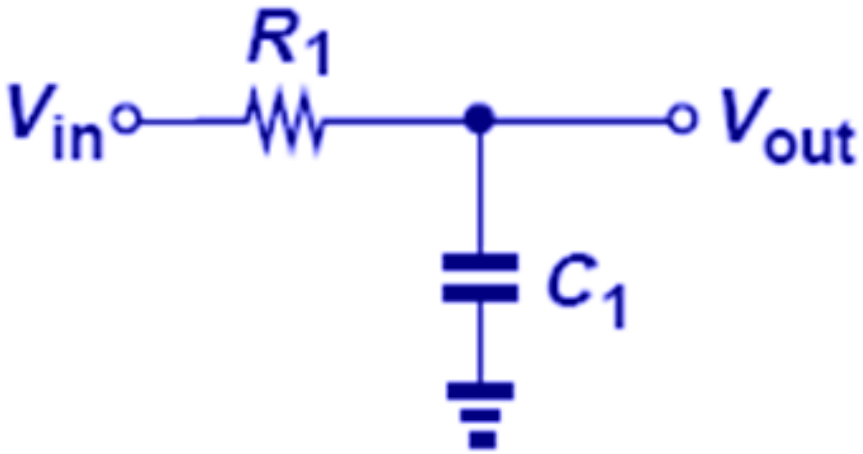
$$S_C^P = \frac{dP}{P} \Big/ \frac{dC}{C}$$

P=Parameter

C=Component

- **Sensitivity measures the variation of a filter parameter due to variation of a filter component.**

Example: Sensitivity



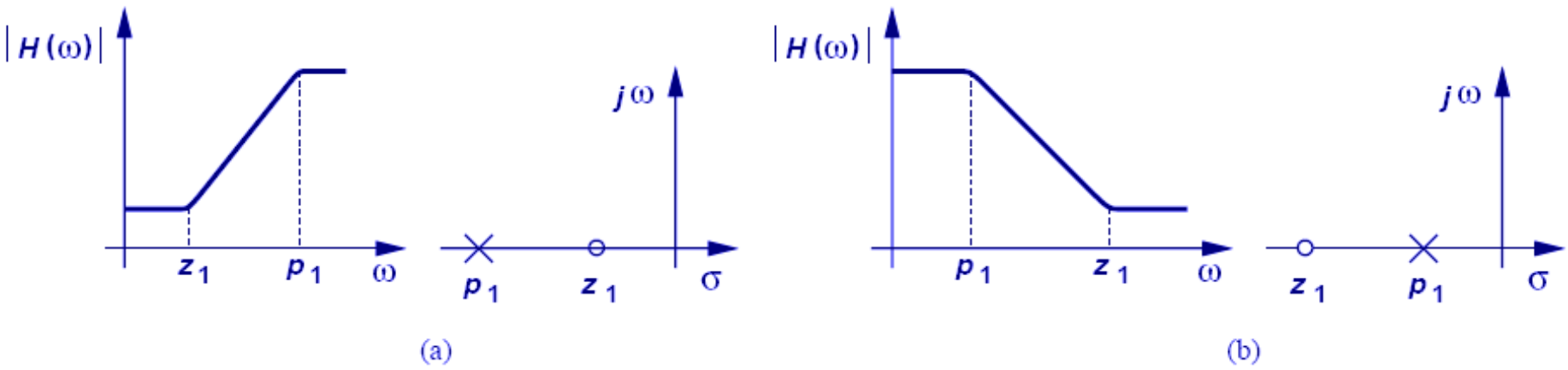
$$\omega_0 = 1/\left(R_1 C_1\right)$$

$$\frac{d\omega_0}{dR_1} = \frac{-1}{R_1^2 C_1}$$

$$\frac{d\omega_0}{\omega_0} = -\frac{dR_1}{R_1}$$

$$S_{R_1}^{\omega_0} = -1$$

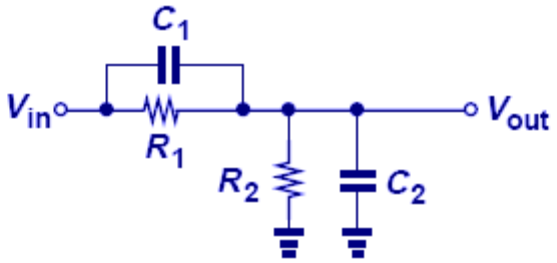
First-Order Filters



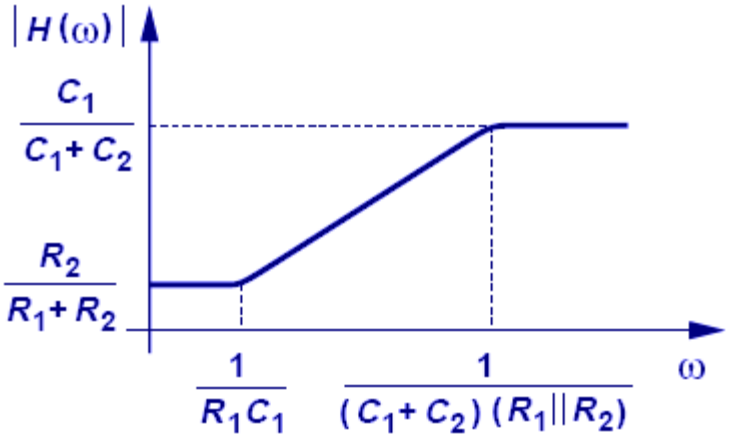
$$H(s) = \alpha \frac{s + z_1}{s + p_1}$$

- First-order filters are represented by the transfer function shown above.
- Low/high pass filters can be realized by changing the relative positions of poles and zeros.

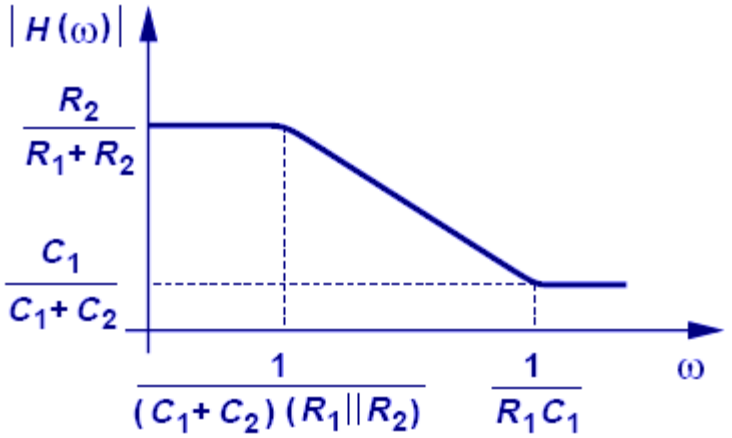
Example: First-Order Filter I



(a)



(b)

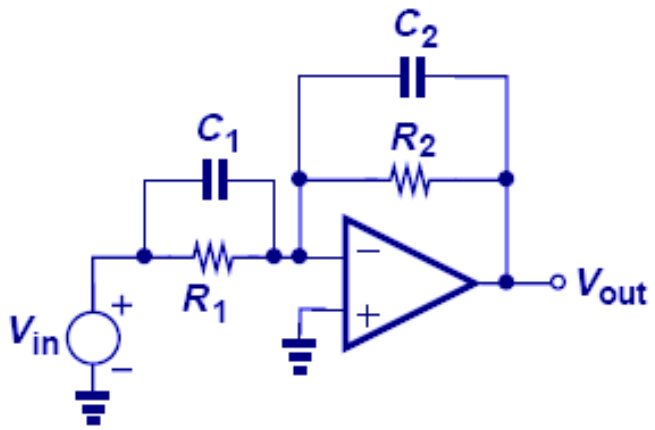


(c)

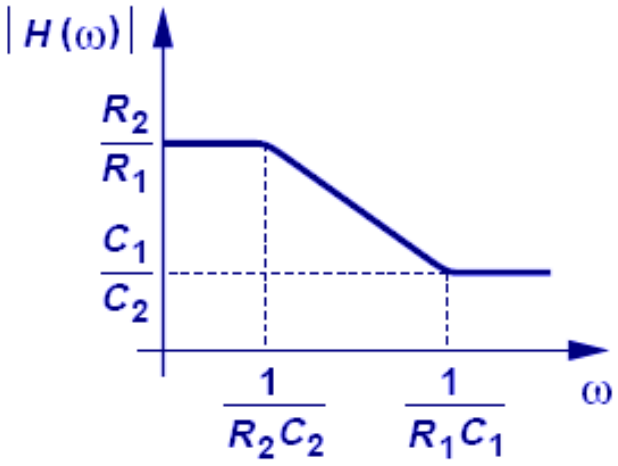
$R_2C_2 < R_1C_1$

$R_2C_2 > R_1C_1$

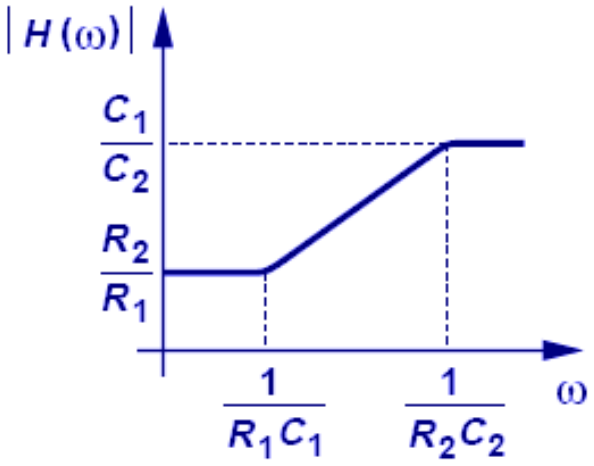
Example: First-Order Filter II



(a)



(b)



(c)

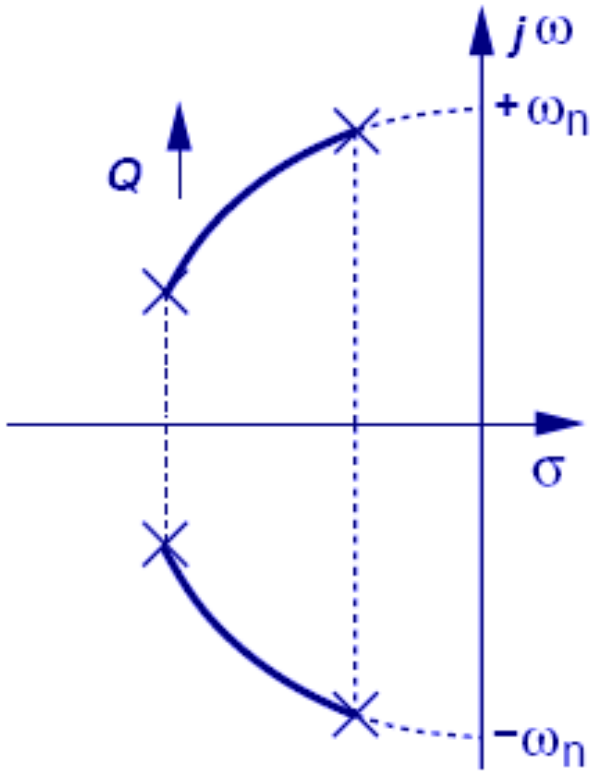
$R_2C_2 < R_1C_1$

$R_2C_2 > R_1C_1$

Second-Order Filters

$$H(s) = \frac{\alpha s^2 + \beta s + \gamma}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2}$$

$$p_{1,2} = -\frac{\omega_n}{2Q} \pm j\omega_n \sqrt{1 - \frac{1}{4Q^2}}$$

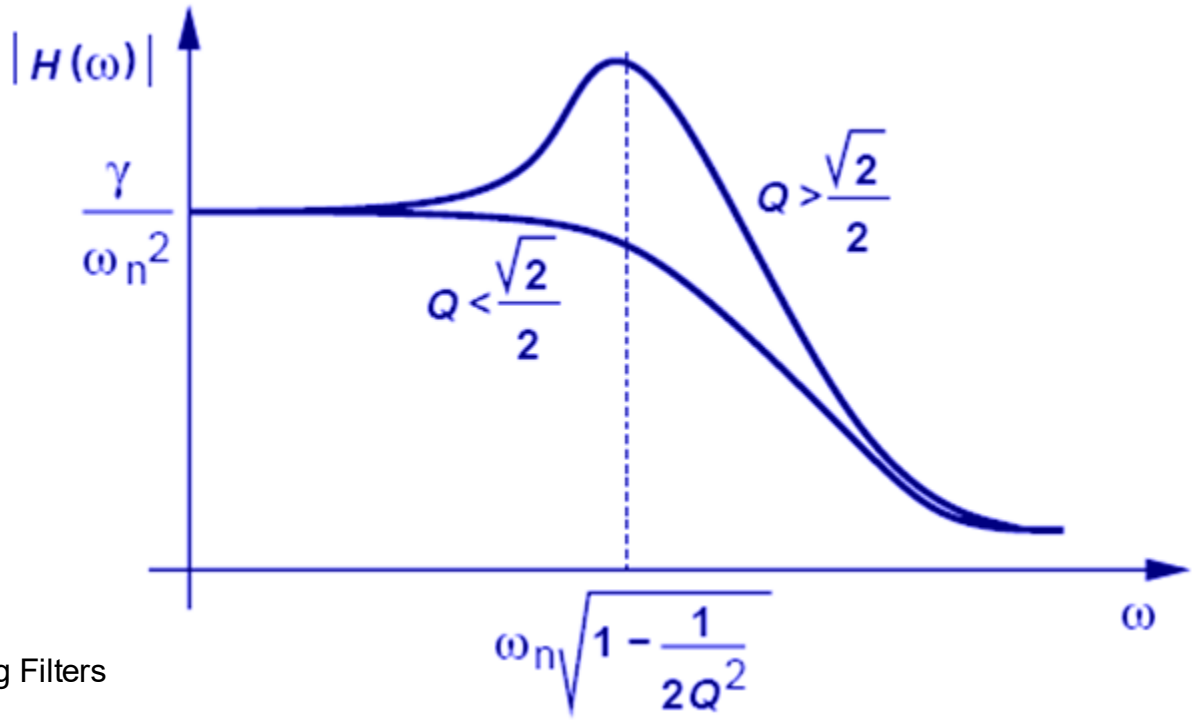


- **Second-order filters are characterized by the "biquadratic" equation with two complex poles shown above.**

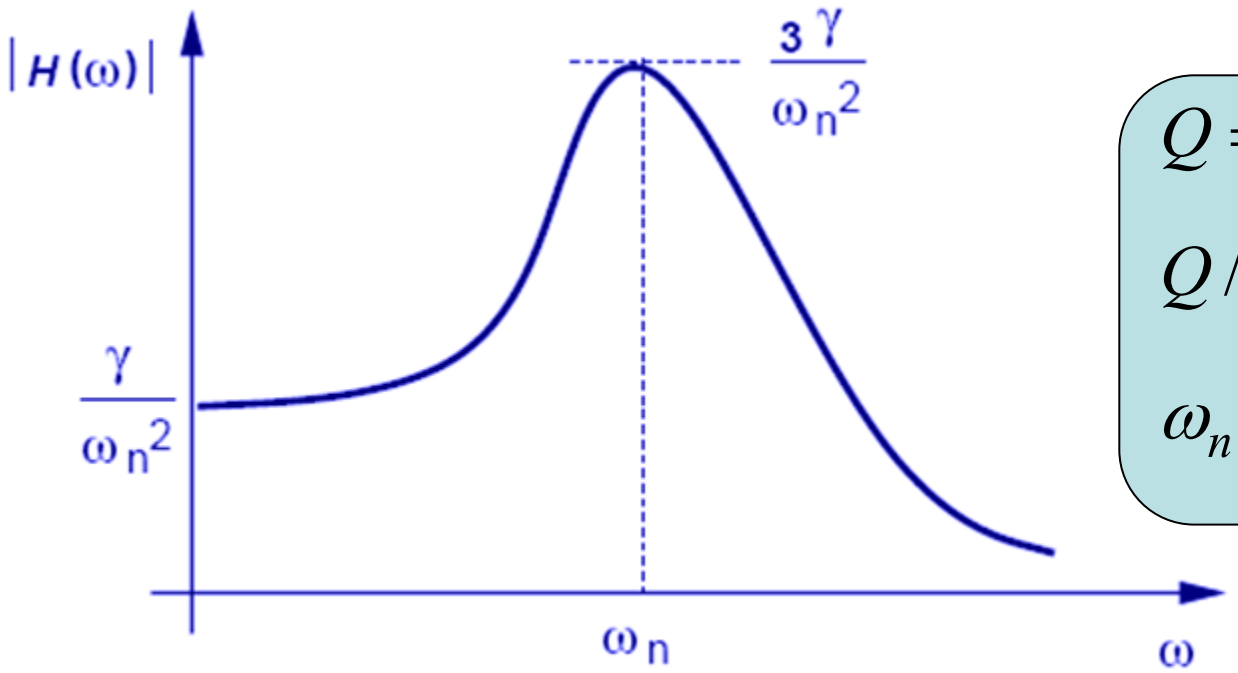
Second-Order Low-Pass Filter

$$|H(j\omega)|^2 = \frac{\gamma^2}{\left(\omega_n^2 - \omega^2\right)^2 + \left(\frac{\omega_n}{Q}\omega\right)^2}$$

α=β=0



Example: Second-Order LPF



$$Q = 3$$

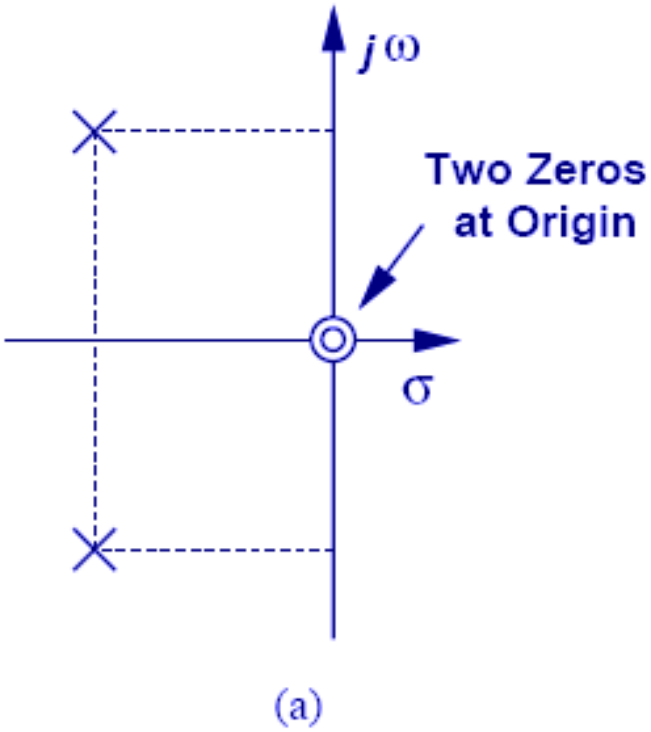
$$Q / \sqrt{1 - 1/(4Q^2)} \approx 3$$

$$\omega_n \sqrt{1 - 1/(2Q^2)} \approx \omega_n$$

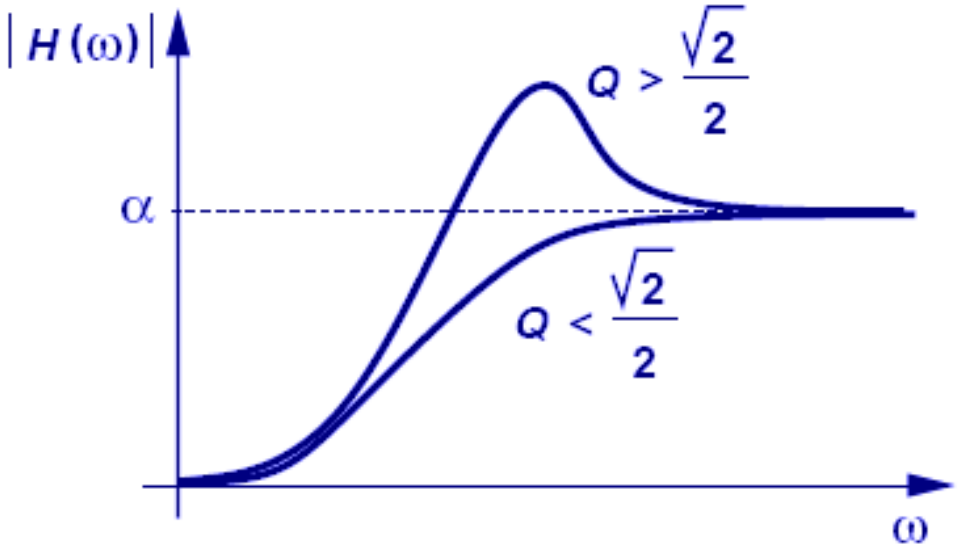
Second-Order High-Pass Filter

$$H(s) = \frac{\alpha s^2}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2}$$

β=γ=0



(a)

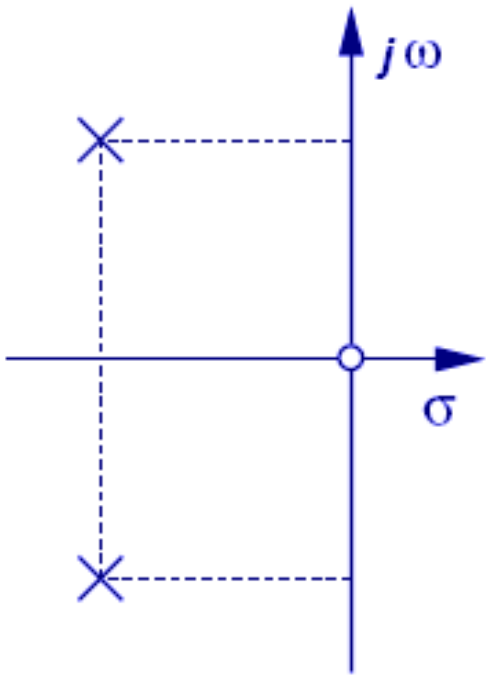


(b)

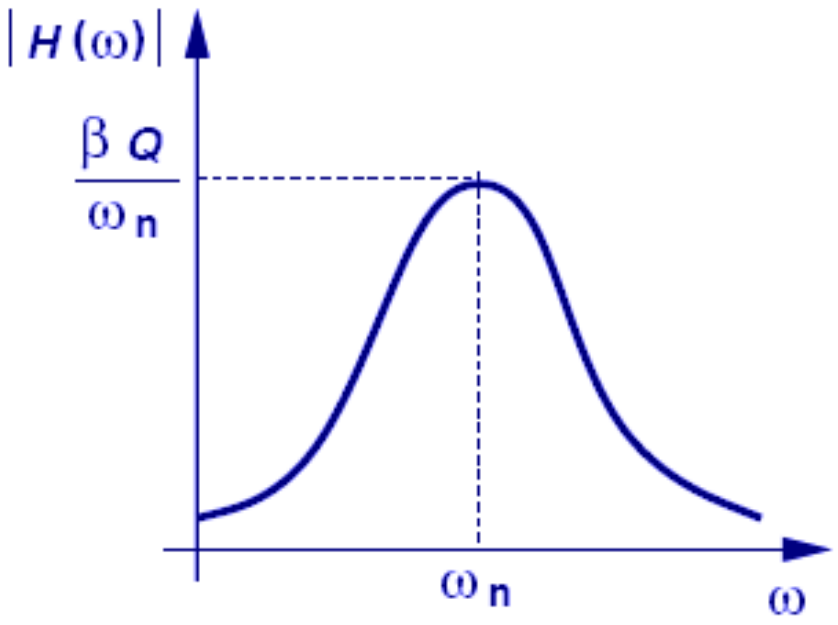
Second-Order Band-Pass Filter

$$H(s) = \frac{\beta s}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2}$$

α=γ=0

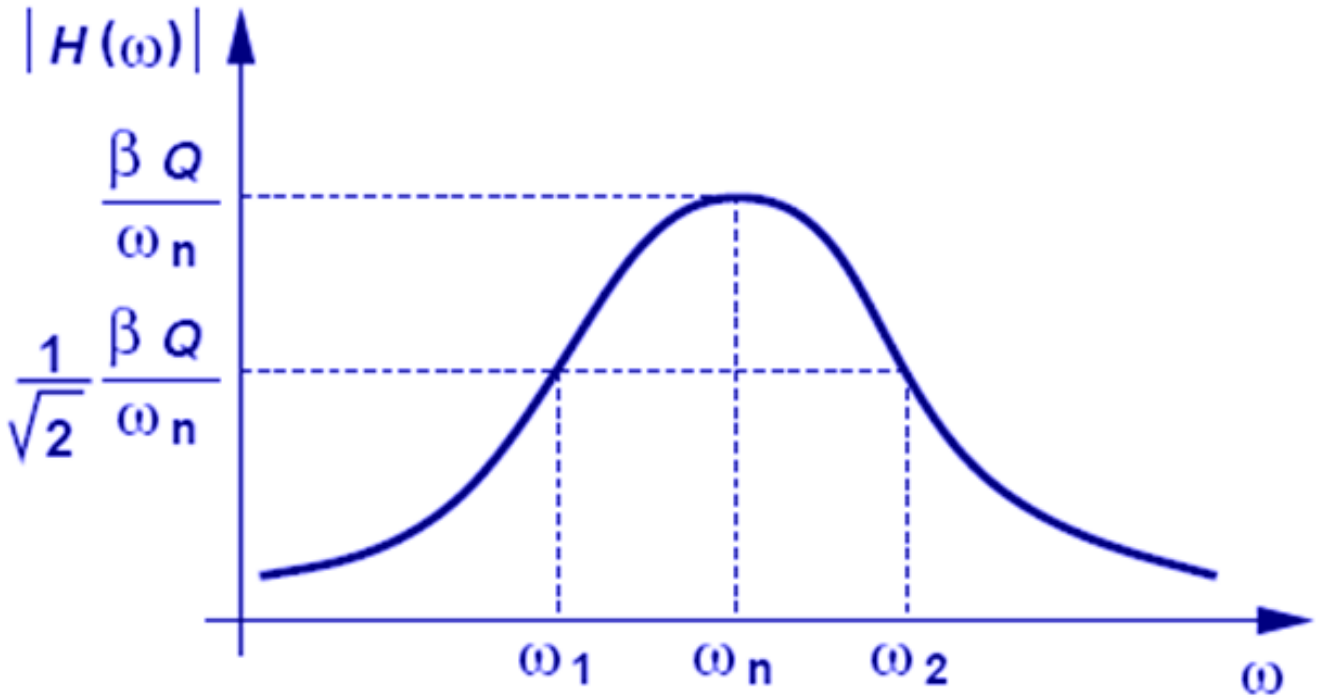


(a)



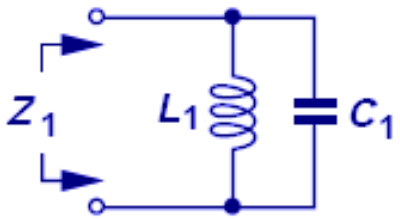
(b)

Example: -3-dB Bandwidth

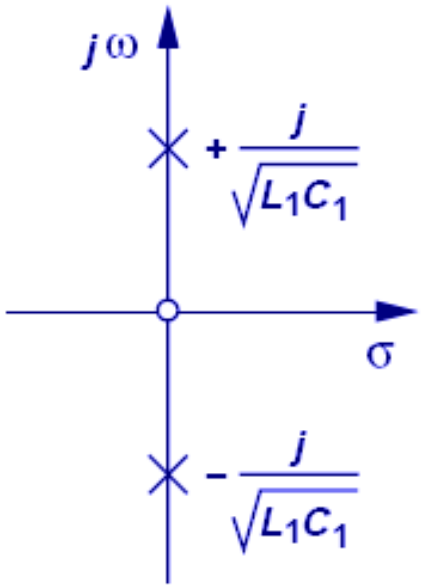


$$Z_2 = \frac{R_1 L_1 s}{R_1 L_1 C_1 s^2 + L_1 s + R_1}$$

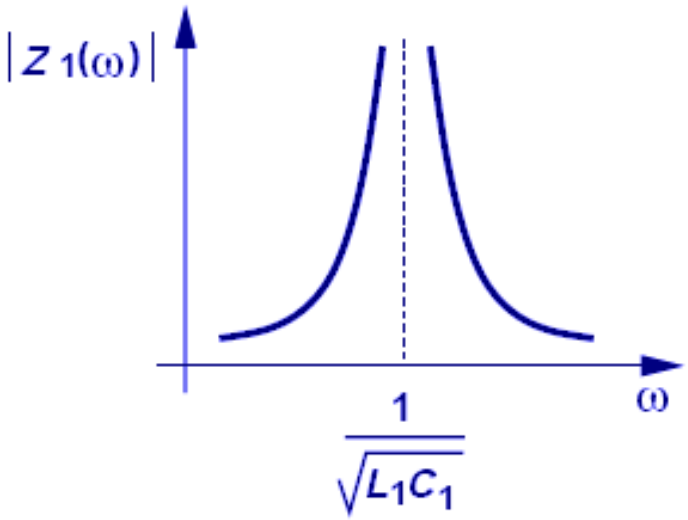
LC Realization of Second-Order Filters



(a)



(b)

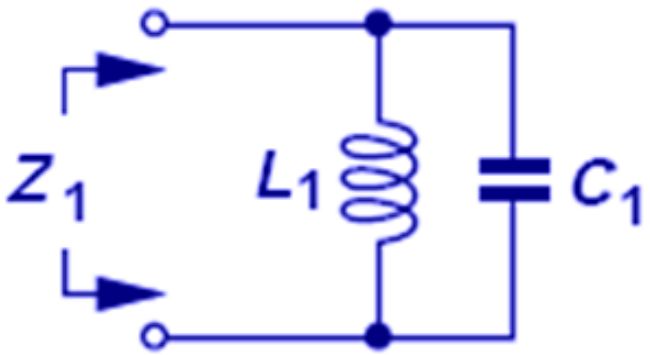


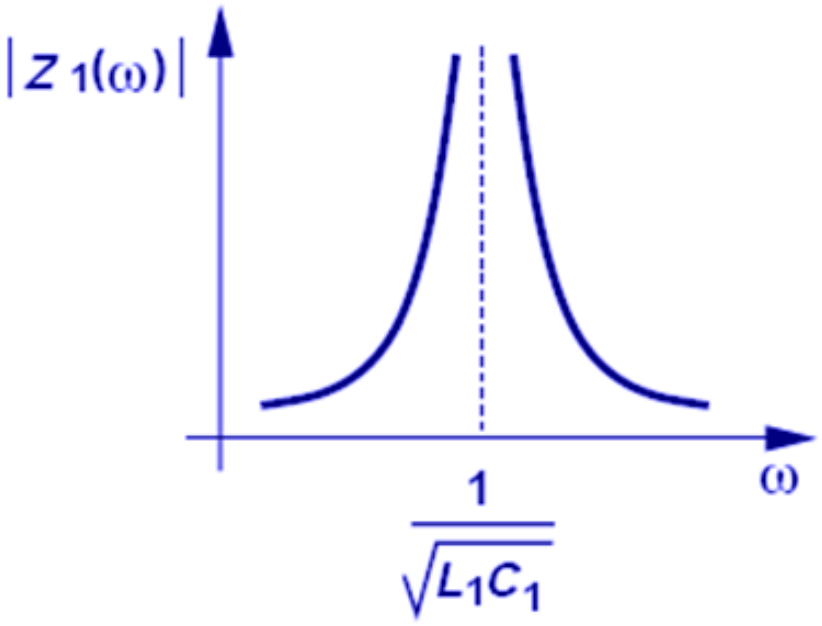
(c)

$$Z_1 = \frac{L_1 s}{L_1 C_1 s^2 + 1}$$

- An LC tank realizes a second-order band-pass filter with two imaginary poles at $\pm j/(L_1C_1)^{1/2}$, which implies infinite impedance at $\omega=1/(L_1C_1)^{1/2}$.

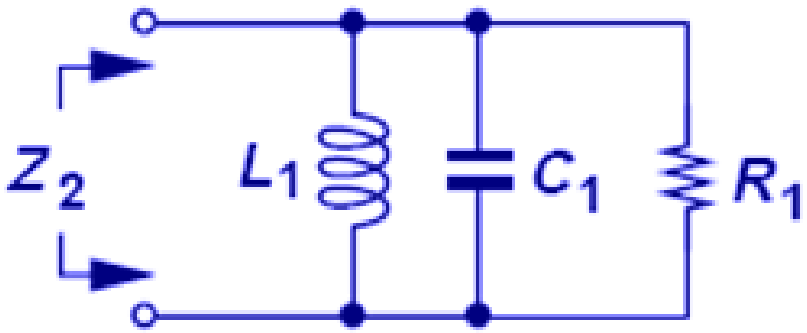
Example: Tank





- ω=0, the inductor acts as a short.
- ω=∞, the capacitor acts as a short.

RLC Realization of Second-Order Filters

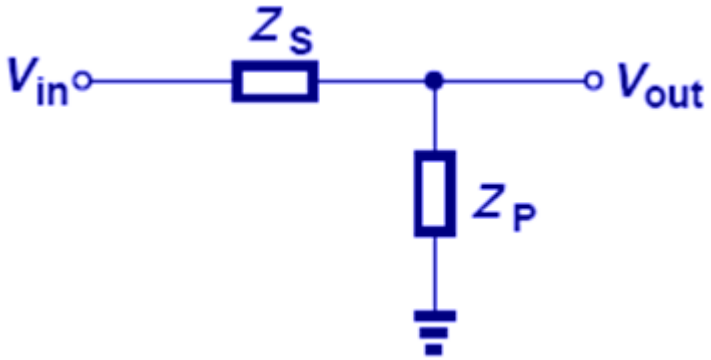


$$Z_2 = \frac{R_1 L_1 s}{R_1 L_1 C_1 s^2 + L_1 s + R_1}$$

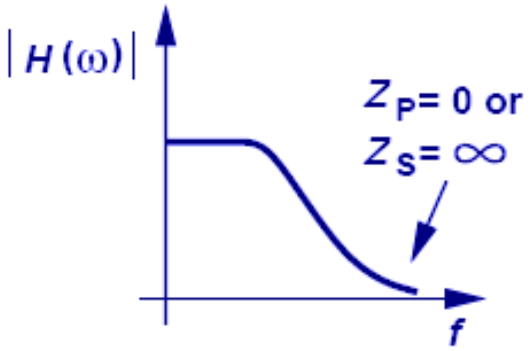
$$p_{1,2} = -\frac{1}{2R_1 C_1} \pm j \frac{1}{\sqrt{L_1 C_1}} \sqrt{1 - \frac{L_1}{4R_1^2 C_1}}$$

- **With a resistor, the poles are no longer pure imaginary which implies there will be no infinite impedance at any ω.**

Voltage Divider Using General Impedances

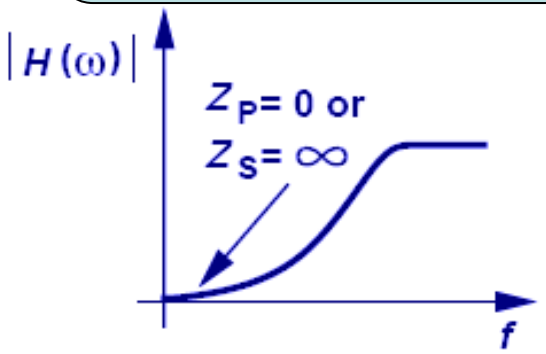


$$\frac{V_{out}}{V_{in}}(s) = \frac{Z_P}{Z_S + Z_P}$$



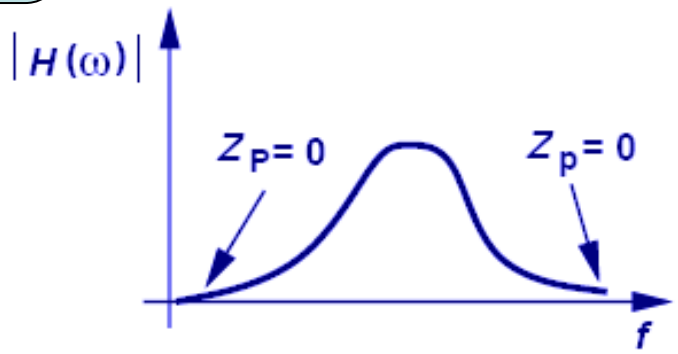
(a)

Low-pass



(b)

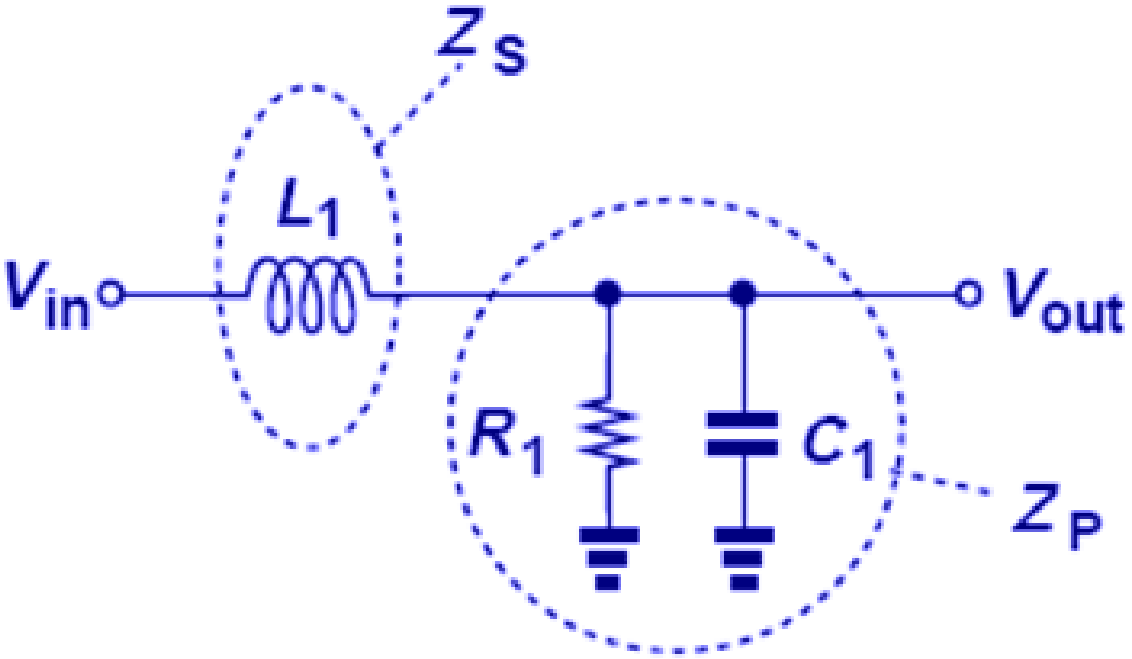
High-pass



(c)

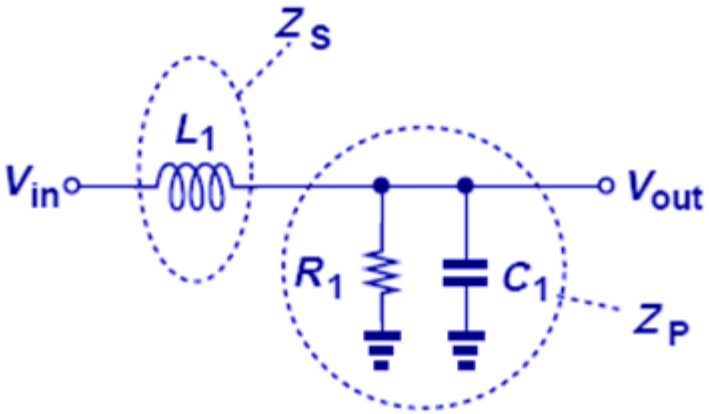
Band-pass

Low-pass Filter Implementation with Voltage Divider

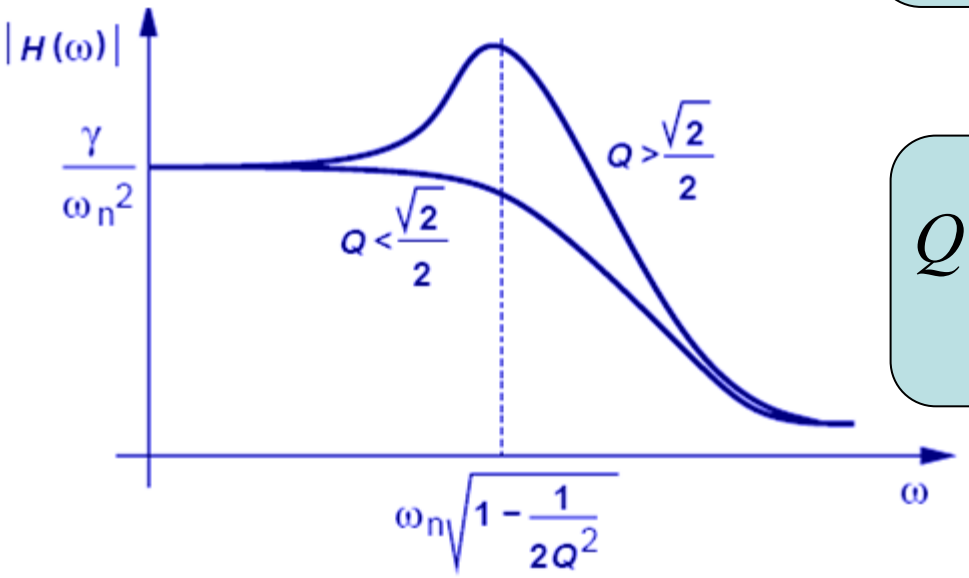


$$\frac{V_{out}}{V_{in}}(s) = \frac{R_1}{R_1 C_1 L_1 s^2 + L_1 s + R_1}$$

Example: Frequency Peaking



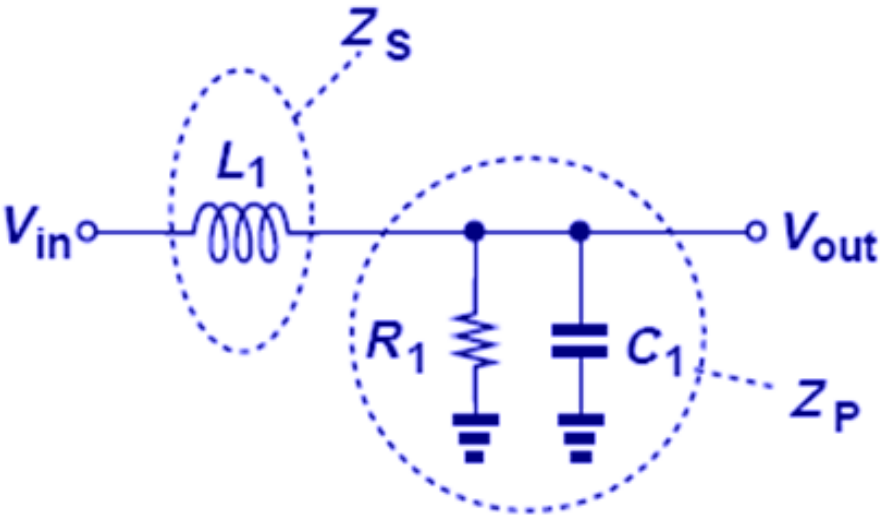
$$\frac{V_{out}}{V_{in}}(s) = \frac{R_1}{R_1 C_1 L_1 s^2 + L_1 s + R_1}$$



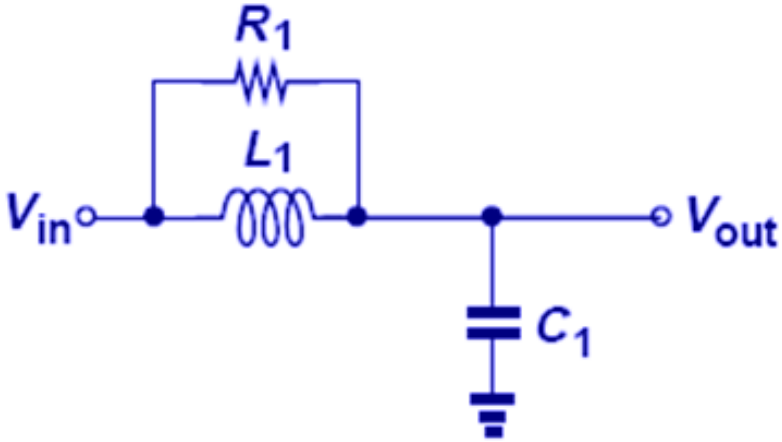
$$Q > \frac{1}{\sqrt{2}}$$

Peaking exists
Voltage gain larger than unity

Low Pass Circuit Comparison



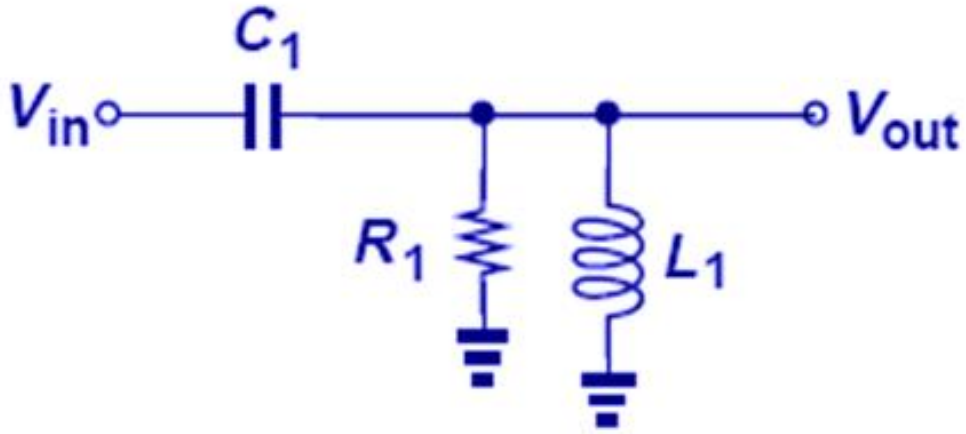
Good



Bad

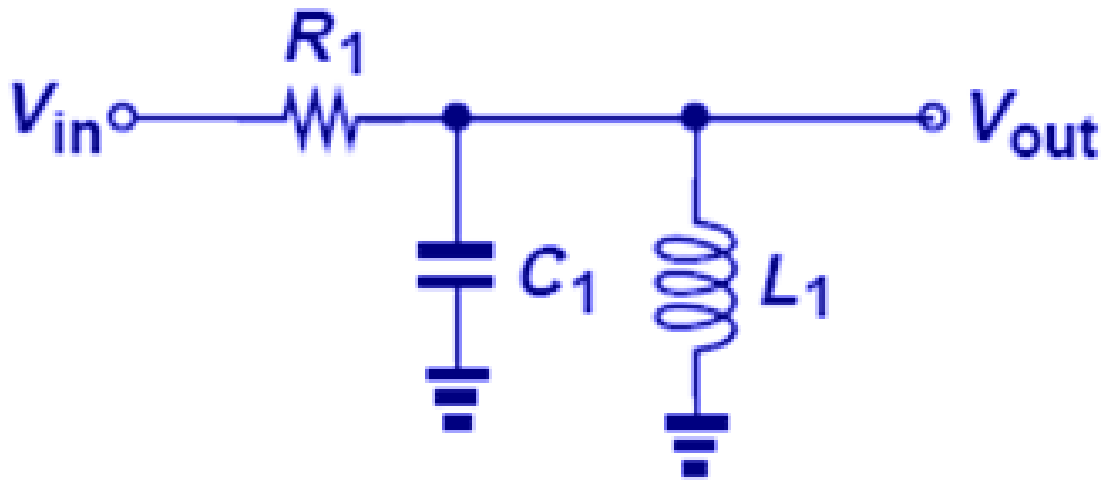
- **The circuit on the left has a sharper roll-off at high frequency than the circuit on the right.**

High-pass Filter Implementation with Voltage Divider



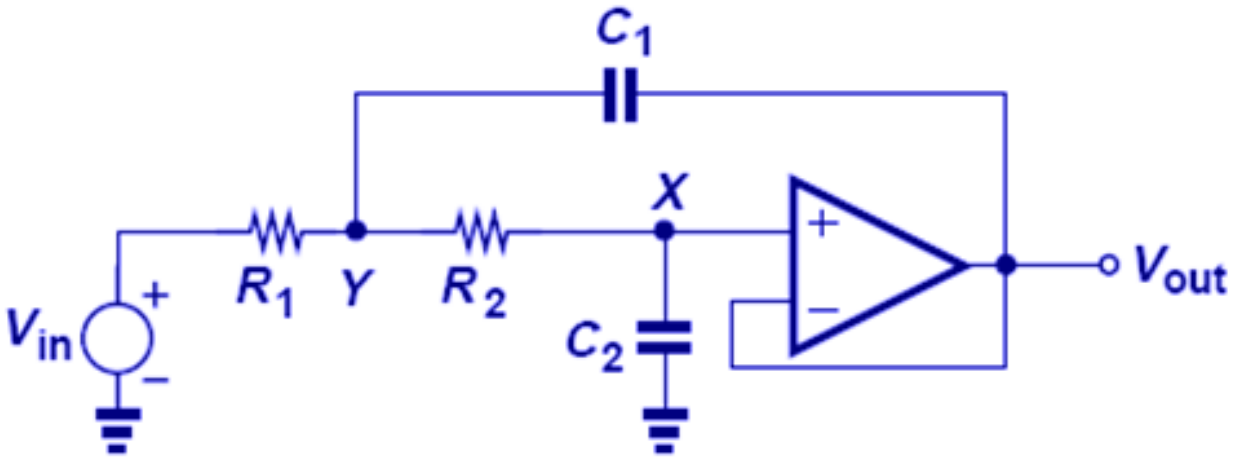
$$\frac{V_{out}}{V_{in}}(s) = \frac{L_1 C_1 R_1 s^2}{R_1 C_1 L_1 s^2 + L_1 s + R_1}$$

Band-pass Filter Implementation with Voltage Divider



$$\frac{V_{out}}{V_{in}}(s) = \frac{L_1 s^2}{R_1 C_1 L_1 s^2 + L_1 s + R_1}$$

Sallen and Key (SK) Filter: Low-Pass



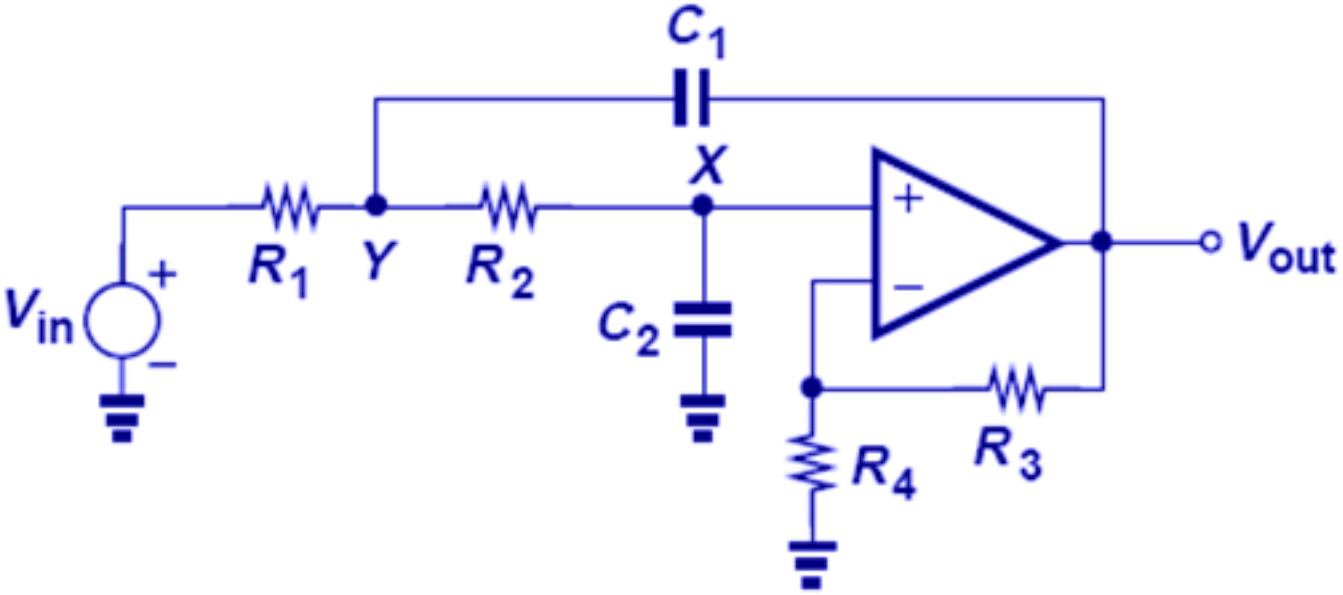
$$\frac{V_{out}}{V_{in}}(s) = \frac{1}{R_1 R_2 C_1 C_2 s^2 + (R_1 + R_2) C_2 s + 1}$$

$$Q = \frac{1}{R_1 + R_2}\sqrt{R_1 R_2 \frac{C_1}{C_2}}$$

$$\omega_n = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

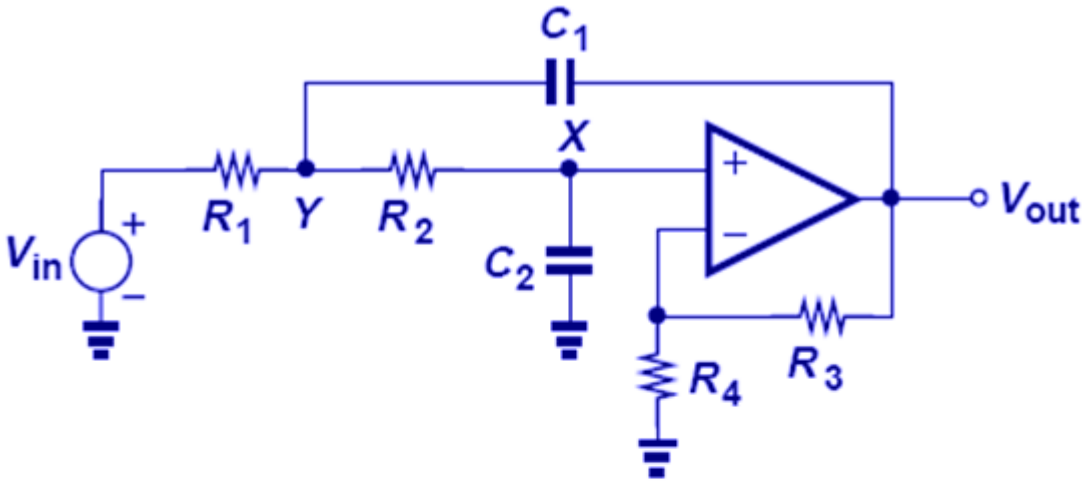
- **Sallen and Key filters are examples of active filters. This particular filter implements a low-pass, second-order transfer function.**

Sallen and Key (SK) Filter: Band-pass



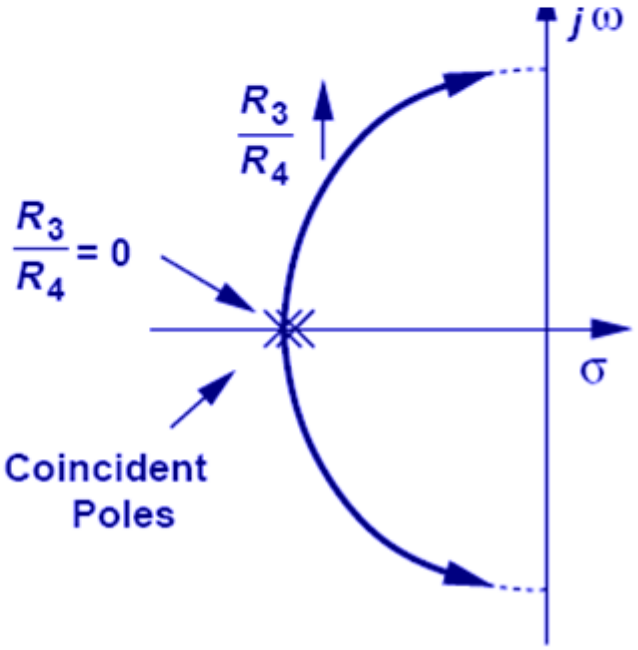
$$\frac{V_{out}}{V_{in}}(s) = \frac{1+\frac{R_3}{R_4}}{R_1R_2C_1C_2s^2 + \left(R_1C_2 + R_2C_2 - R_1\frac{R_3}{R_4}C_1\right)s + 1}$$

Example: SK Filter Poles

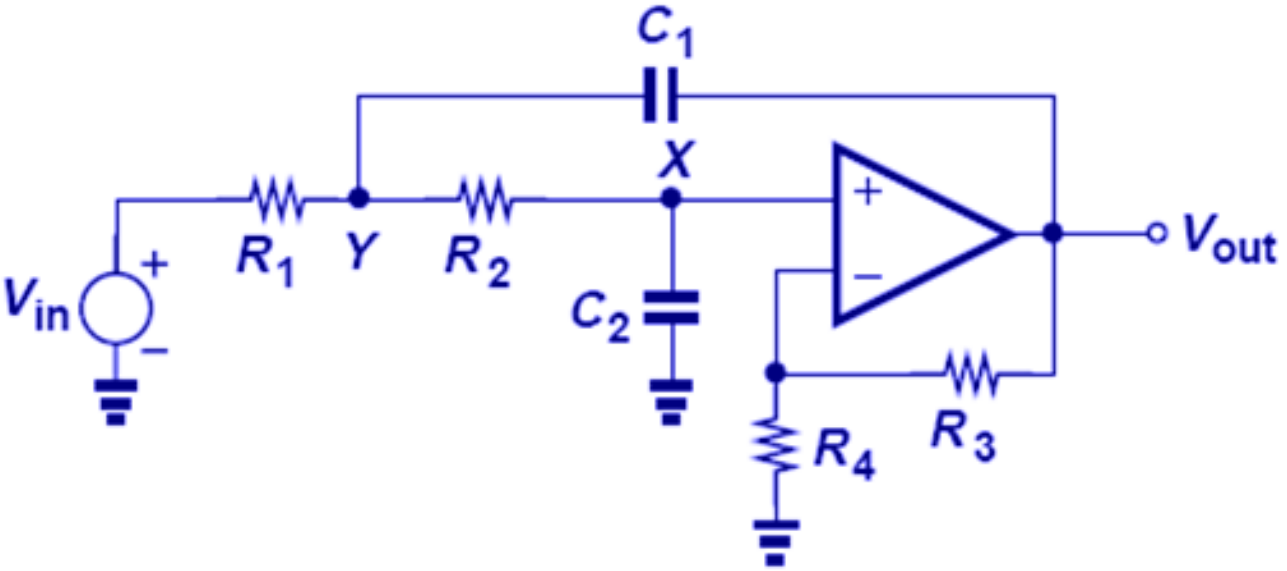


$C_1 = C_2$

$R_1 = R_2$



Sensitivity in Band-Pass SK Filter



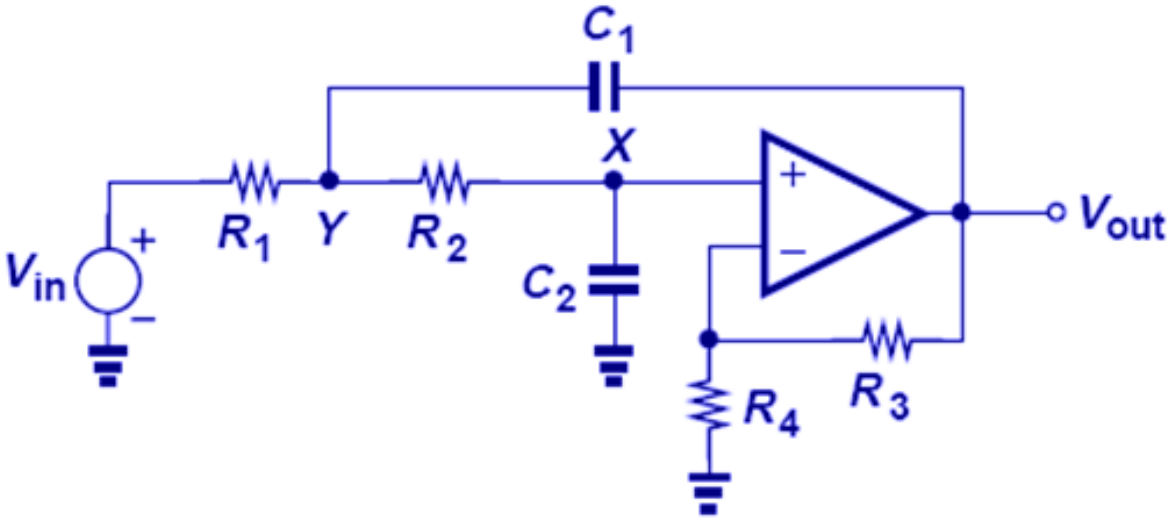
$$S_{R_1}^{\omega_n} = S_{R_2}^{\omega_n} = S_{C_1}^{\omega_n} = S_{C_2}^{\omega_n} = -\frac{1}{2}$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = -\frac{1}{2} + Q\left(\sqrt{\frac{R_2C_2}{R_1C_1}} + \sqrt{\frac{R_1C_2}{R_2C_1}}\right)$$

$$S_{R_1}^{Q} = -S_{R_2}^{Q} = -\frac{1}{2} + Q\sqrt{\frac{R_2C_2}{R_1C_1}}$$

$$S_{K}^{Q} = QK\sqrt{\frac{R_1C_1}{R_2C_2}} \qquad K = 1 + R_3/R_4$$

Example: SK Filter Sensitivity I



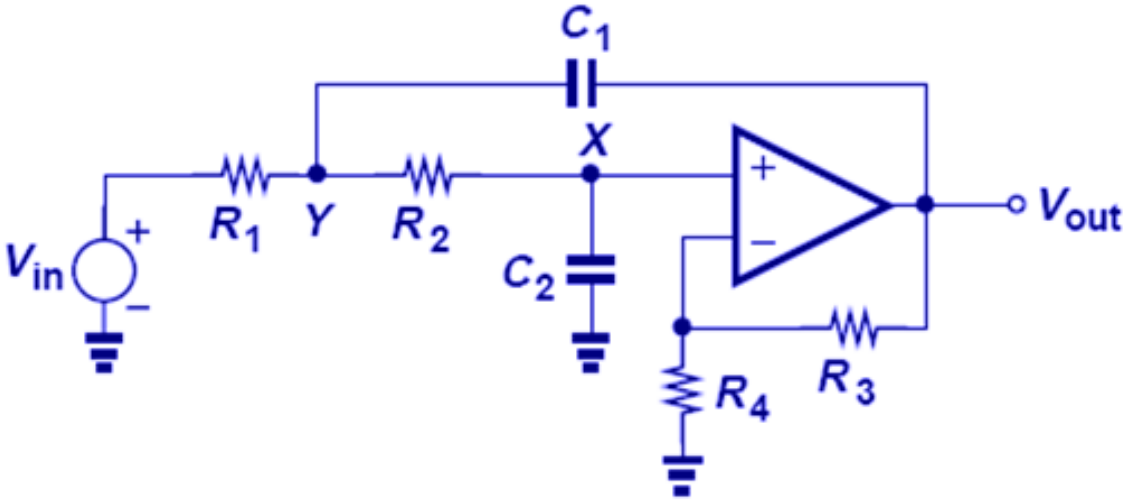
$$R_1 = R_2 = R$$
$$C_1 = C_2 = C$$

$$S_{R_1}^{Q} = -S_{R_2}^{Q} = -\frac{1}{2} + \frac{1}{3-K}$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = -\frac{1}{2} + \frac{2}{3-K}$$

$$S_{K}^{Q} = \frac{K}{3-K}$$

Example: SK Filter Sensitivity II



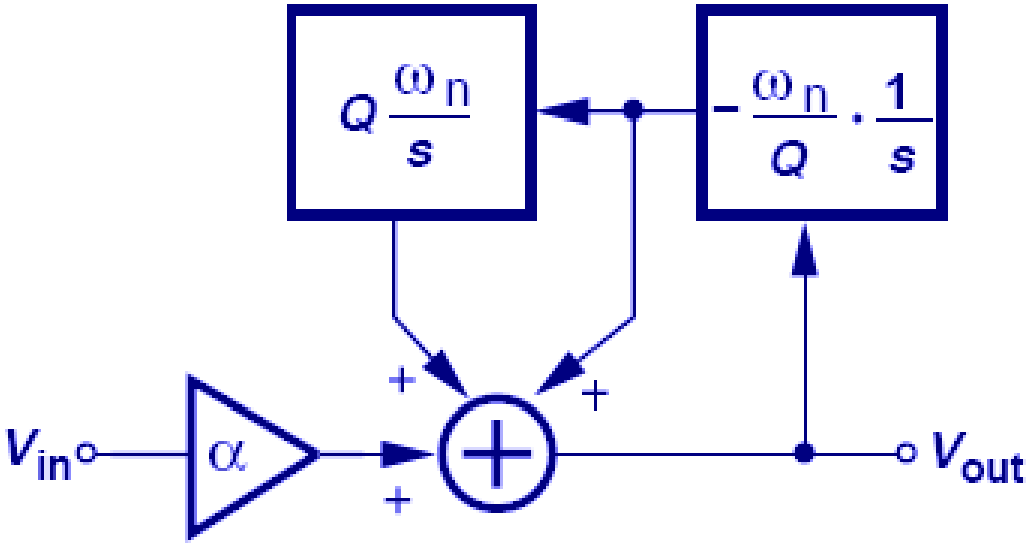
$$Q = 2$$
$$K = 2$$

$$\sqrt{\frac{R_2 C_2}{R_1 C_1}} = \frac{3}{4} \Rightarrow S_{R_1}^{Q} = 1$$

$$\sqrt{\frac{R_1 C_1}{R_2 C_2}} = \frac{1}{8} \Rightarrow S_{C_1}^{Q} = \frac{5}{4}$$

$$S_K^Q = \frac{8}{1.5}$$

Integrator-Based Biquads

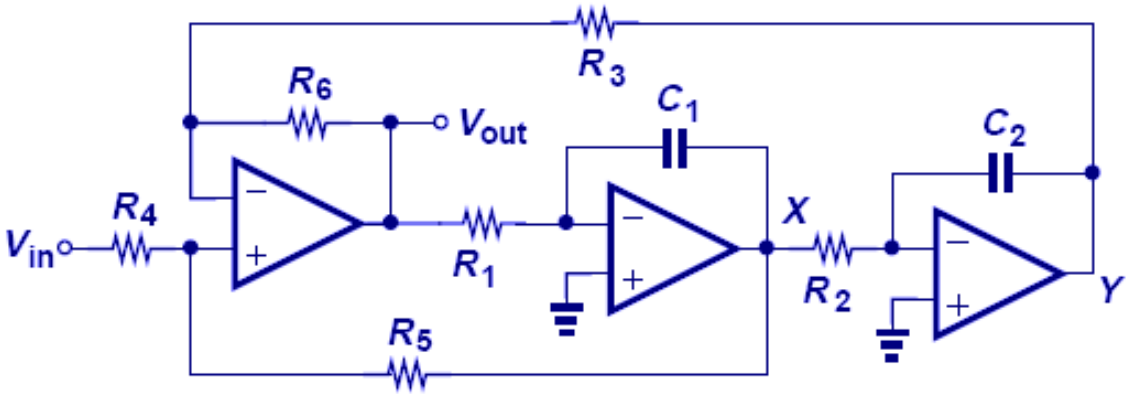


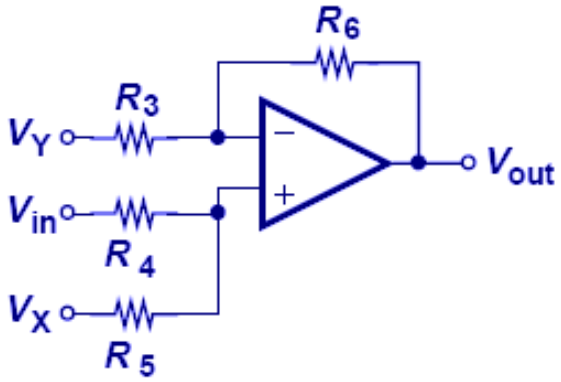
$$\frac{V_{out}}{V_{in}}(s)=\frac{\alpha s^2}{s^2+\frac{\omega_n}{Q}s+\omega_n^2}$$

$$V_{out}(s)=\alpha V_{in}(s)-\frac{\omega_n}{Q}\cdot\frac{1}{s}V_{out}(s)-\frac{\omega_n^2}{s^2}V_{out}(s)$$

- It is possible to use integrators to implement biquadratic transfer functions.
- The block-diagram above illustrates how.

KHN Biquads





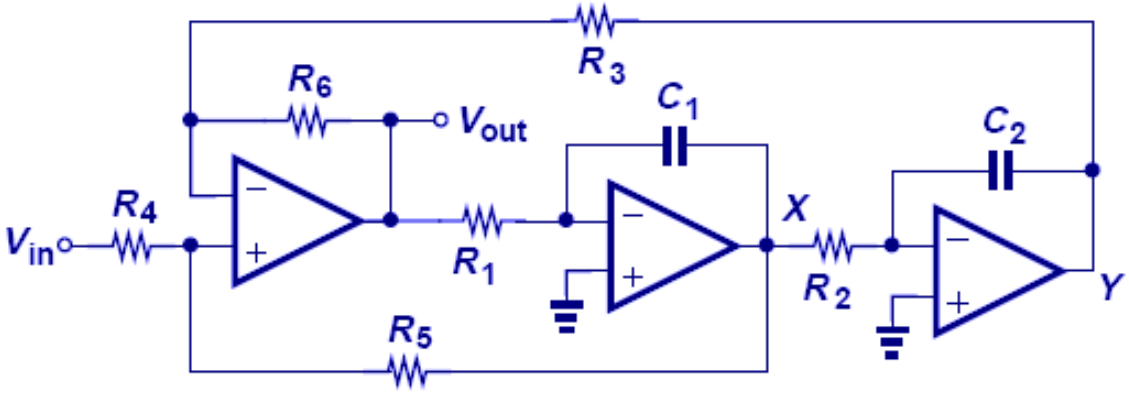
$$V_{out}(s) = \alpha V_{in}(s) - \frac{\omega_n}{Q} \cdot \frac{1}{s} V_{out}(s) - \frac{\omega_n^2}{s^2} V_{out}(s)$$

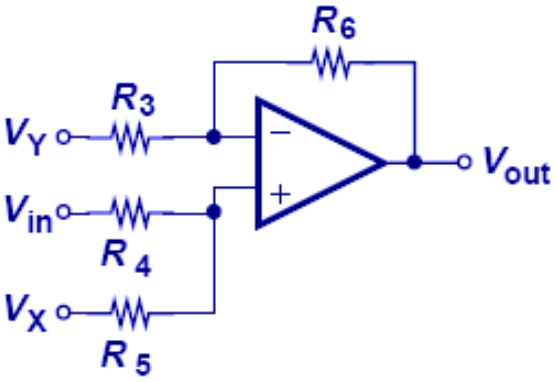
$$\alpha = \frac{R_5}{R_4 + R_5}\left(1 + \frac{R_6}{R_3}\right)$$

$$\frac{\omega_n}{Q} = \frac{R_4}{R_4 + R_5} \cdot \frac{1}{R_1 C_1}$$

$$\omega_n^2 = \frac{R_6}{R_3} \cdot \frac{1}{R_1 R_2 C_1 C_2}$$

Versatility of KHN Biquads





High-Pass

$$\frac{V_{out}}{V_{in}}(s) = \frac{\alpha s^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2}$$

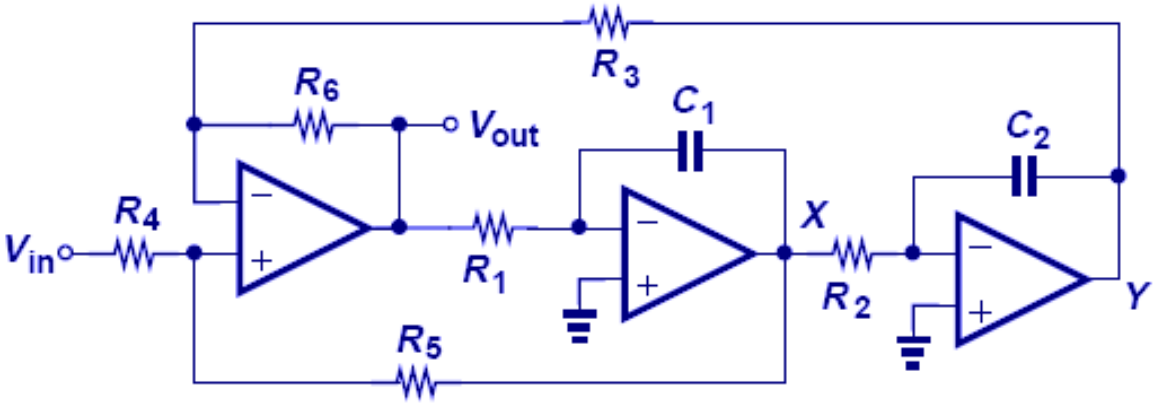
Band-Pass

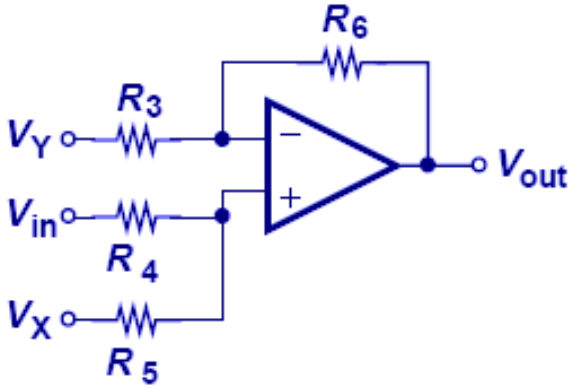
$$\frac{V_X}{V_{in}}(s) = \frac{\alpha s^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \cdot \frac{-1}{R_1 C_1 s}$$

Low-Pass

$$\frac{V_Y}{V_{in}}(s) = \frac{\alpha s^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \cdot \frac{1}{R_1 R_2 C_1 C_2 s^2}$$

Sensitivity in KHN Biquads





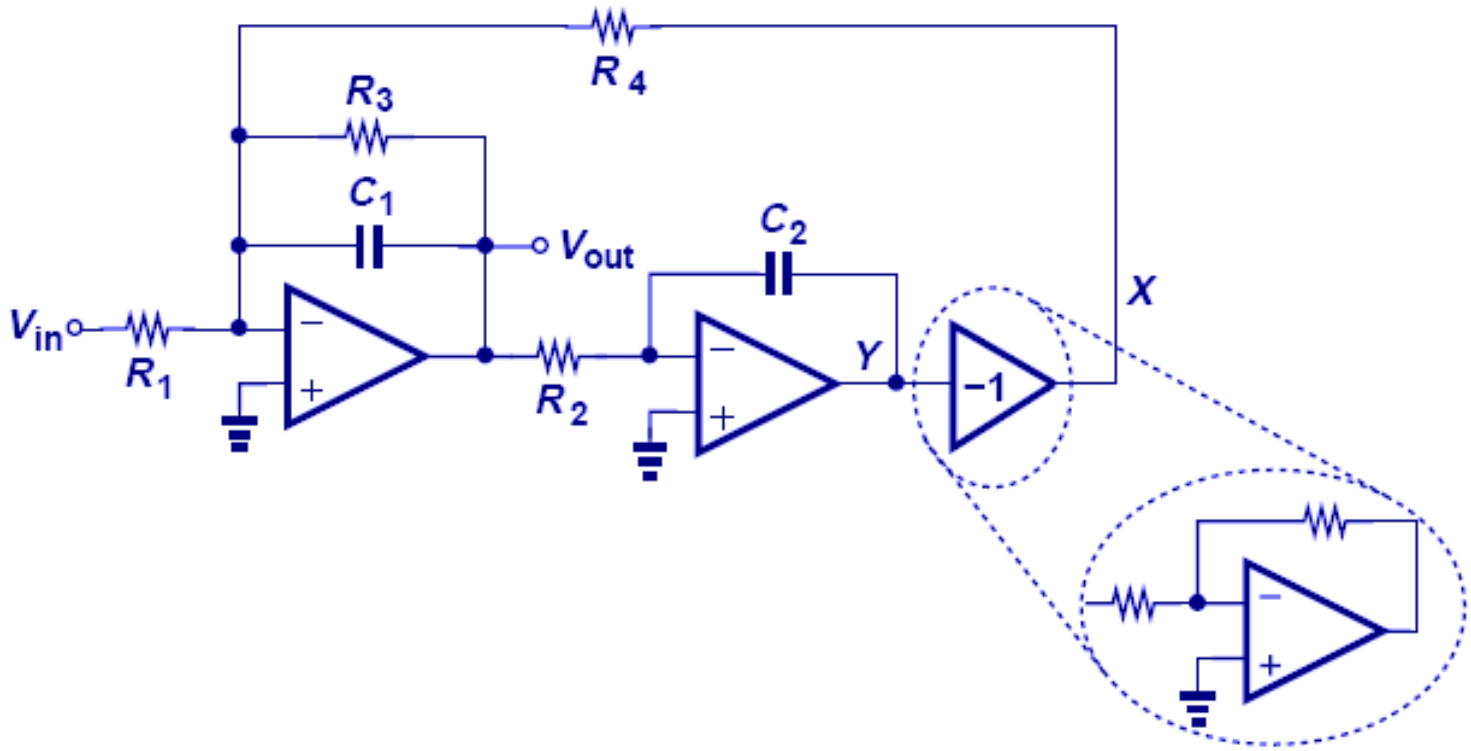
$$\left|S^{\omega_n}_{R_1,R_2,C_1,C_2,R_4,R_5,R_3,R_6}\right| = 0.5$$

$$\left|S^{Q}_{R_1,R_2,C_1,C_2}\right| = 0.5$$

$$\left|S^{Q}_{R_3,R_6}\right| = \frac{Q}{2}\frac{|R_3 - R_6|}{1+\dfrac{R_5}{R_4}}\sqrt{\frac{R_2C_2}{R_3R_6R_1C_1}}$$

$$\left|S^{Q}_{R_4,R_5}\right| = \frac{R_5}{R_4+R_5} < 1$$

Tow-Thomas Biquad



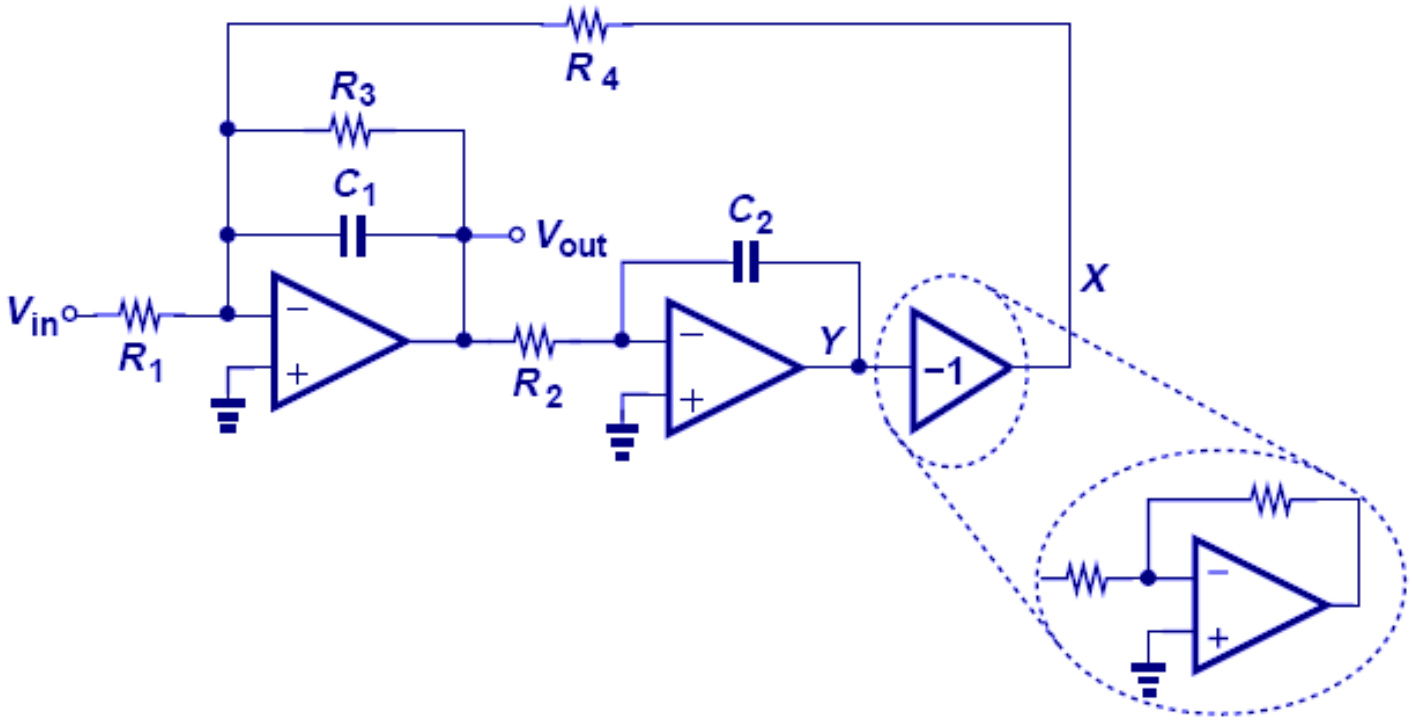
$$\frac{V_{out}}{V_{in}} = -\frac{R_2 R_3 R_4}{R_1} \cdot \frac{C_2 s}{R_2 R_3 R_4 C_1 C_2 s^2 + R_2 R_4 C_2 s + R_3}$$

Band-Pass

$$\frac{V_Y}{V_{in}} = \frac{R_3 R_4}{R_1} \cdot \frac{1}{R_2 R_3 R_4 C_1 C_2 s^2 + R_2 R_4 C_2 s + R_3}$$

Low-Pass

Example: Tow-Thomas Biquad



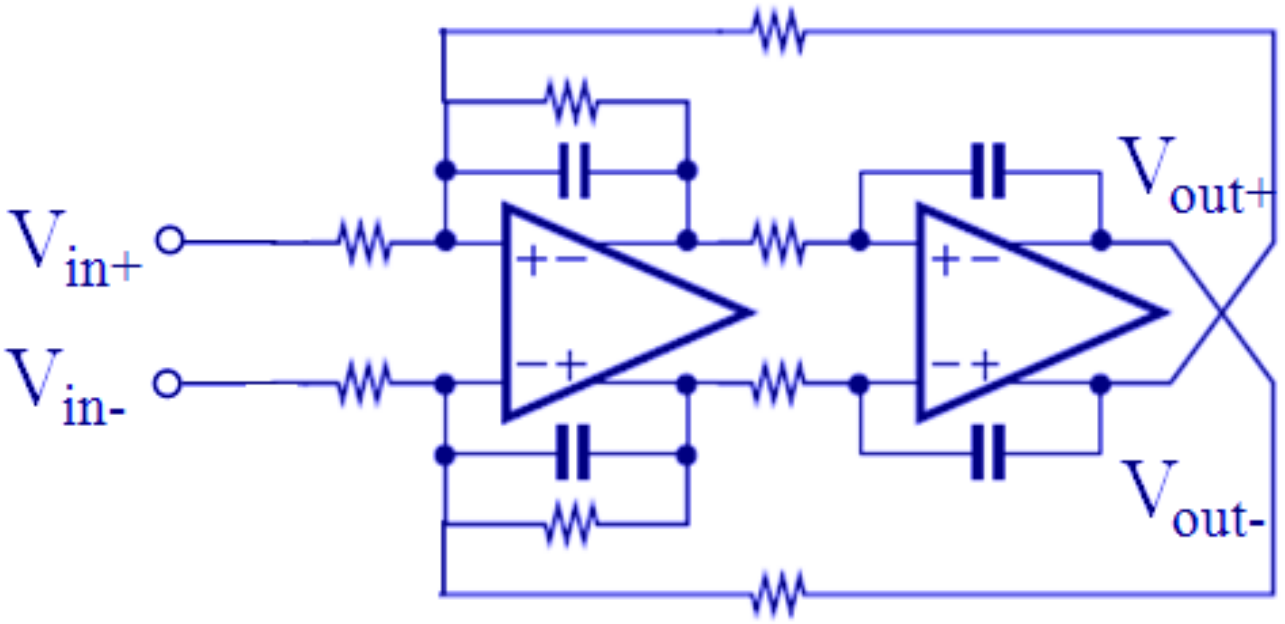
$$\omega_n = \frac{1}{\sqrt{R_2 R_4 C_1 C_2}}$$

Adjusted by R_2 or R_4

$$Q = \frac{1}{R_3}\sqrt{\frac{R_2 R_4 C_2}{C_1}}$$

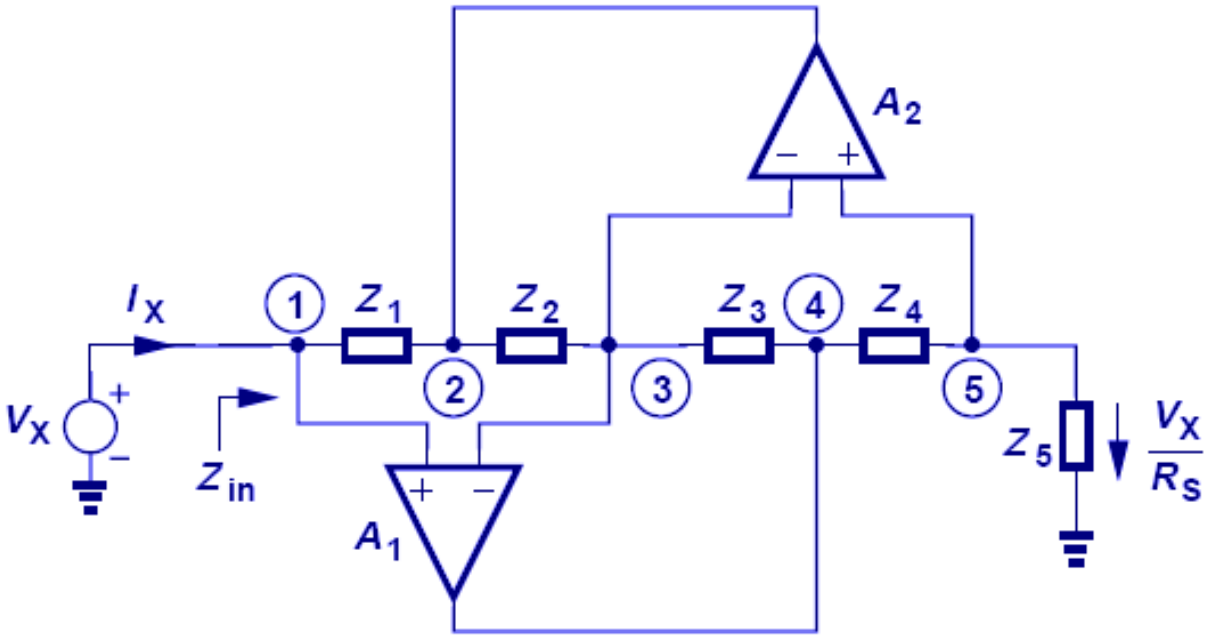
Adjusted by R_3

Differential Tow-Thomas Biquads



- **By using differential integrators, the inverting stage is eliminated.**

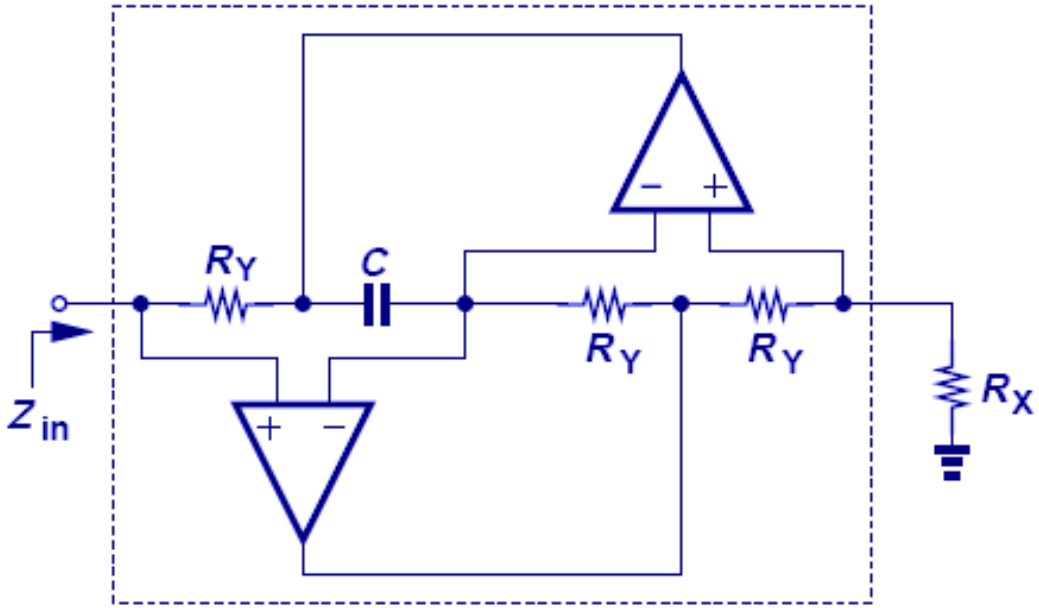
Simulated Inductor (SI)



$$Z_{in} = \frac{Z_1 Z_3}{Z_2 Z_4} Z_5$$

- **It is possible to simulate the behavior of an inductor by using active circuits in feedback with properly chosen passive elements.**

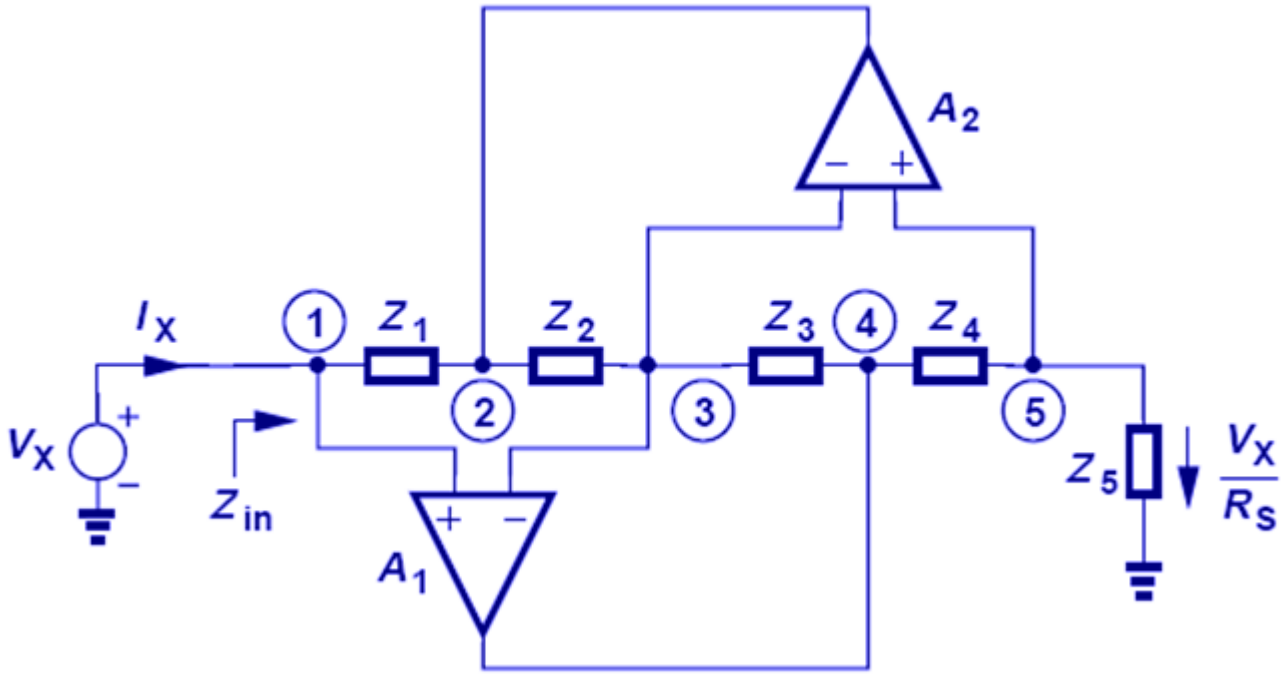
Example: Simulated Inductor I



$$Z_{in} = R_X R_Y^2 Cs$$

- By proper choices of Z_1-Z_4, Z_{in} has become an impedance that increases with frequency, simulating inductive effect.

Example: Simulated Inductor II

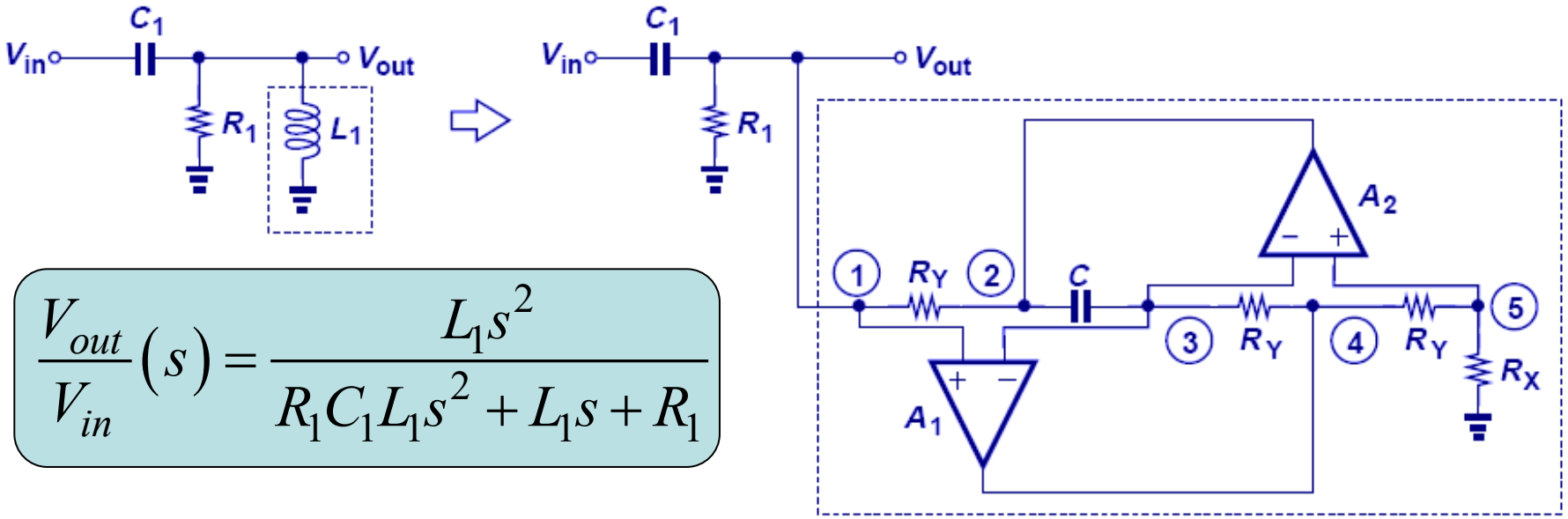


$$Z_1 = Z_2 = Z_3 = R_Y$$

$$Z_4 = \frac{1}{Cs}$$

$$Z_{in} = R_X R_Y^2 Cs$$

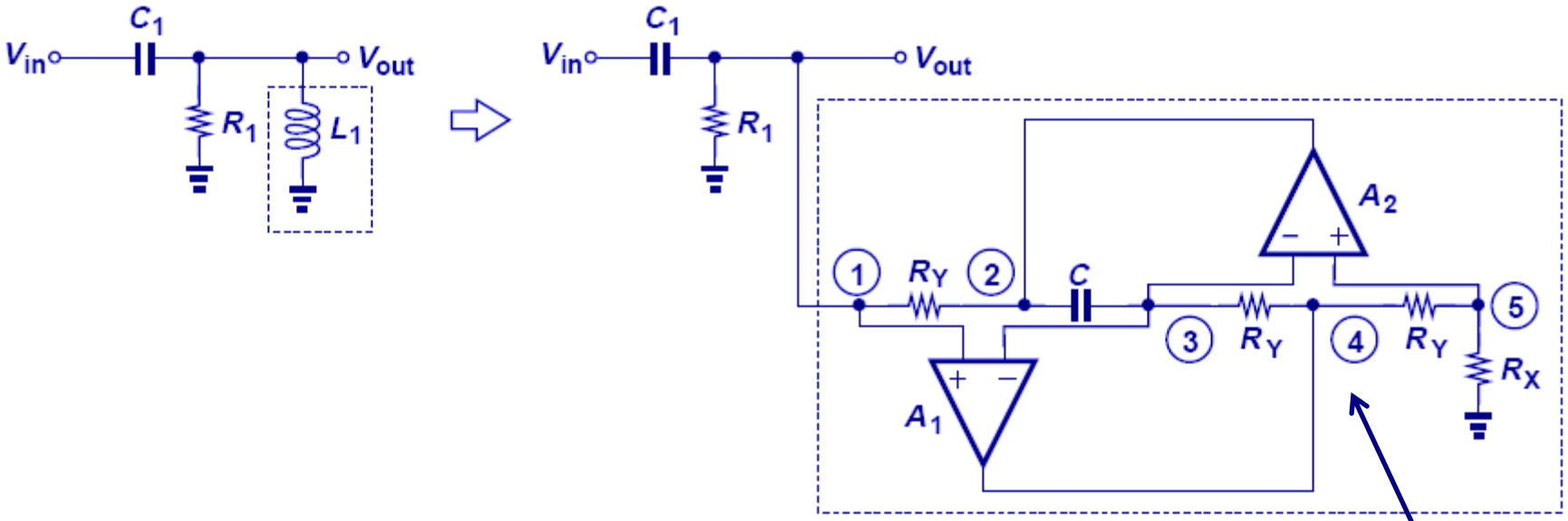
High-Pass Filter with SI



$$\frac{V_{out}}{V_{in}}(s) = \frac{L_1 s^2}{R_1 C_1 L_1 s^2 + L_1 s + R_1}$$

- **With the inductor simulated at the output, the transfer function resembles a second-order high-pass filter.**

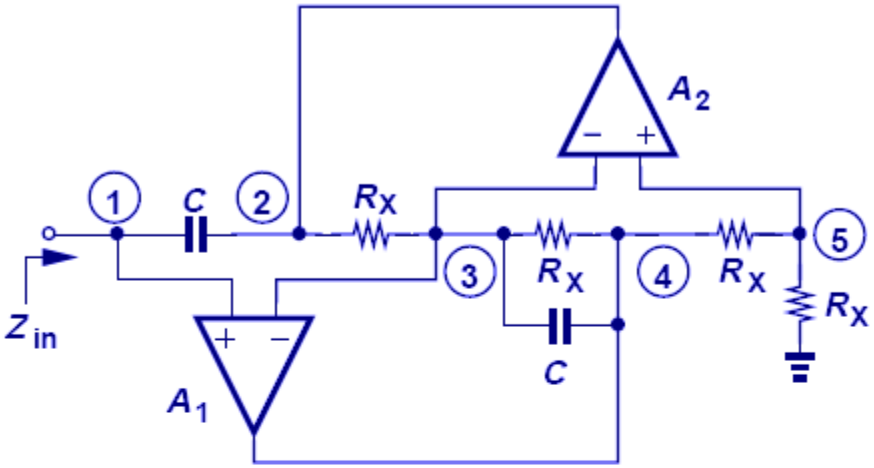
Example: High-Pass Filter with SI



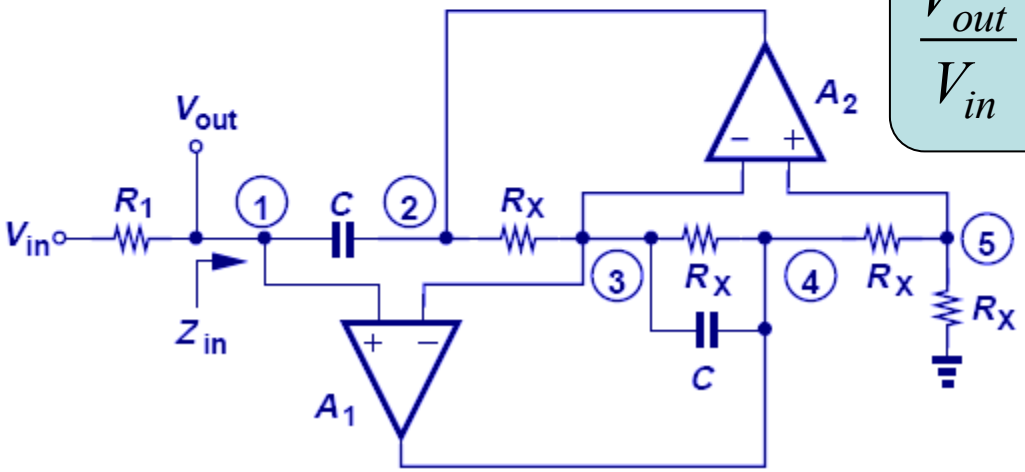
Node 4 is also an output node

$$V_4 = V_{out}\left(1+\frac{R_Y}{R_X}\right)$$

Low-Pass Filter with Super Capacitor



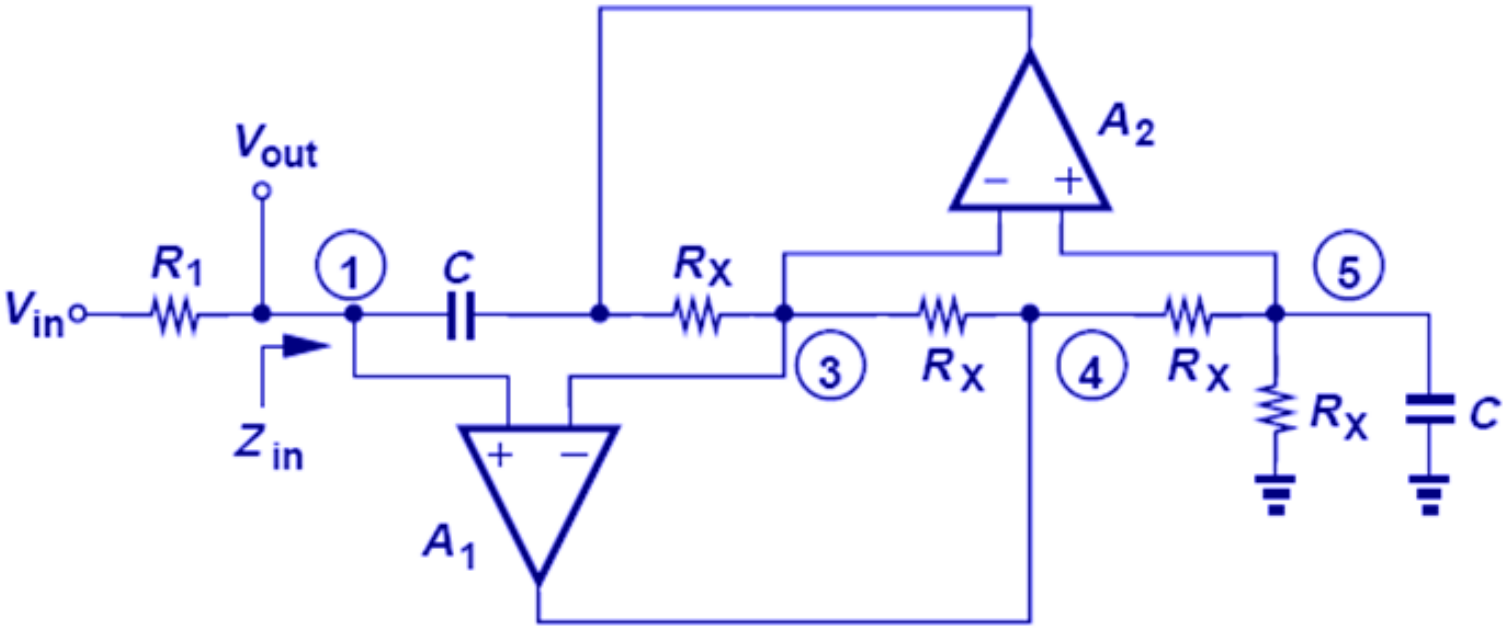
$$Z_{in} = \frac{1}{Cs\left(R_X Cs + 1\right)}$$



$$\frac{V_{out}}{V_{in}} = \frac{Z_{in}}{Z_{in} + R_1} = \frac{1}{R_1 R_X C^2 s^2 + R_1 Cs + 1}$$

Low-Pass

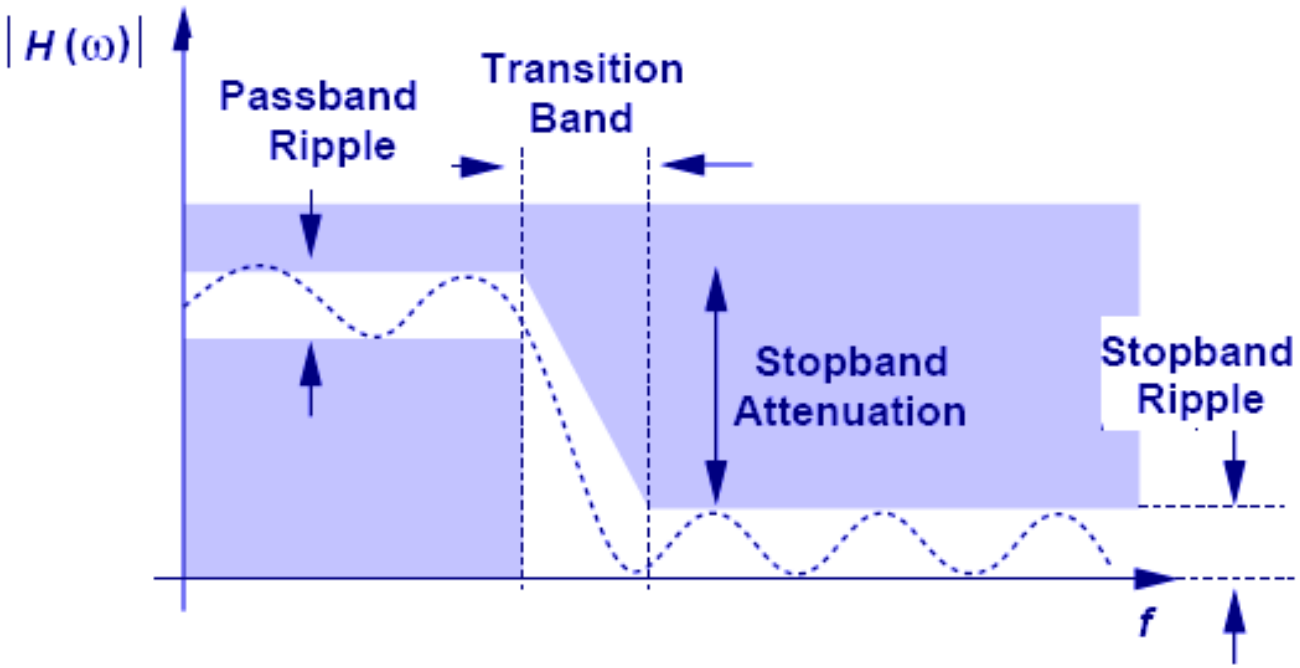
Example: Poor Low Pass Filter



$$V_4 = V_{out}\left(2 + R_X C s\right)$$

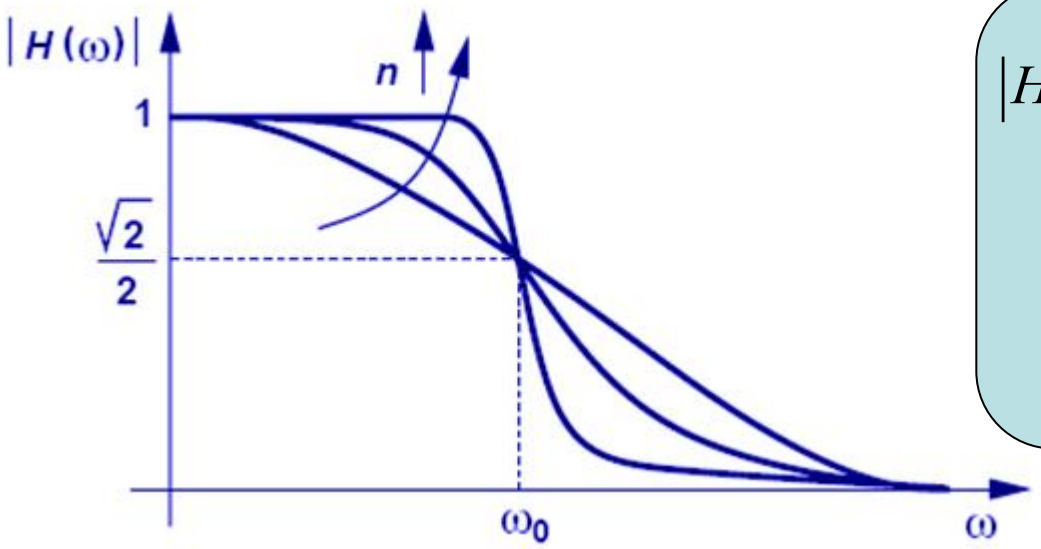
- **Node 4 is no longer a scaled version of the V_{out}. Therefore the output can only be sensed at node 1, suffering from a high impedance.**

Frequency Response Template



- **With all the specifications on pass/stop band ripples and transition band slope, one can create a filter template that will lend itself to transfer function approximation.**

Butterworth Response



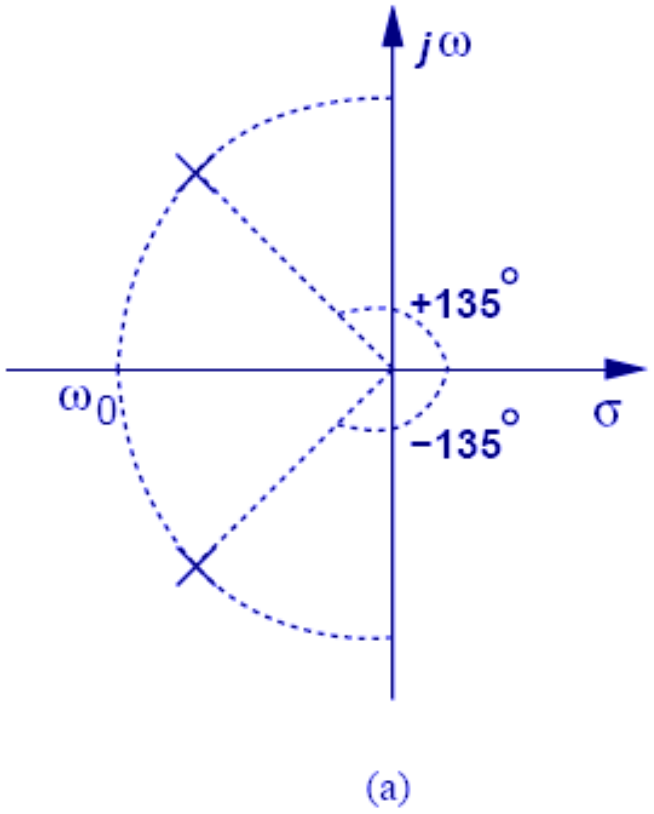
$$\left|H(j\omega)\right| = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_0}\right)^{2n}}}$$

$\omega_{-3dB}=\omega_0$, for all n

- The Butterworth response completely avoids ripples in the pass/stop bands at the expense of the transition band slope.

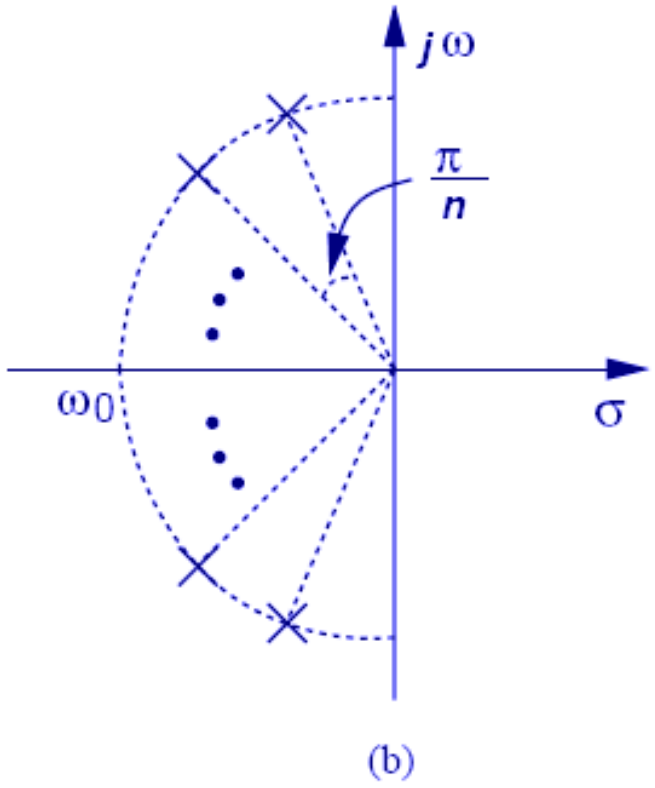
Poles of the Butterworth Response

$$p_k = \omega_0 \exp\frac{j\pi}{2}\exp\left(j\frac{2k-1}{2n}\pi\right), k = 1,2,\mathrm{L}\ ,n$$



(a)

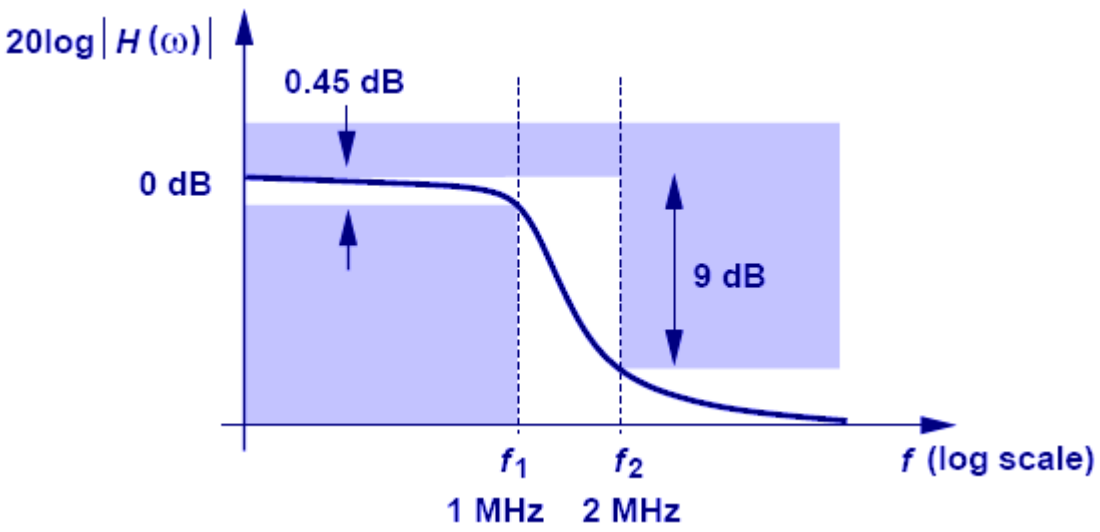
2nd-Order



(b)

nth-Order

Example: Butterworth Order



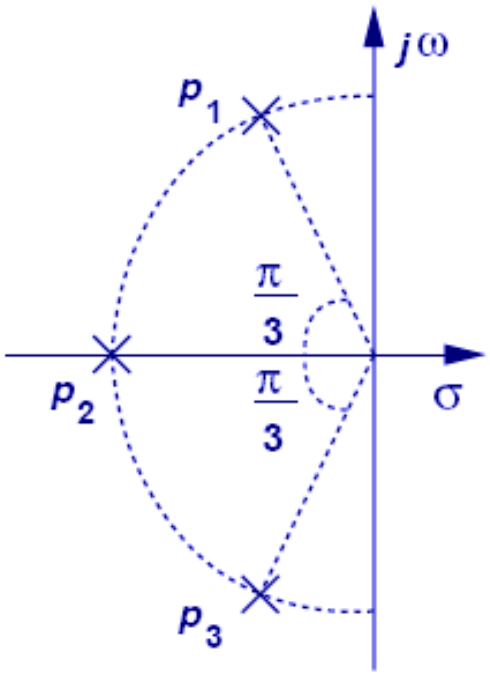
$$\left(\frac{f_2}{f_1}\right)^{2n} = 64.2$$

$$f_2 = 2f_1$$

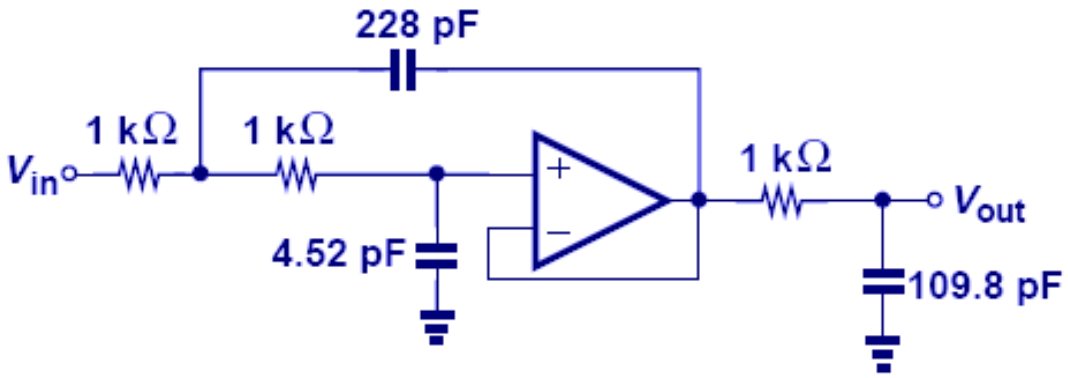
n=3

- **The Butterworth order of three is needed to satisfy the filter response on the left.**

Example: Butterworth Response



(a)



(b)

$$p_1 = 2\pi * (1.45MHz) * \left(\cos\frac{2\pi}{3} + j\sin\frac{2\pi}{3} \right)$$

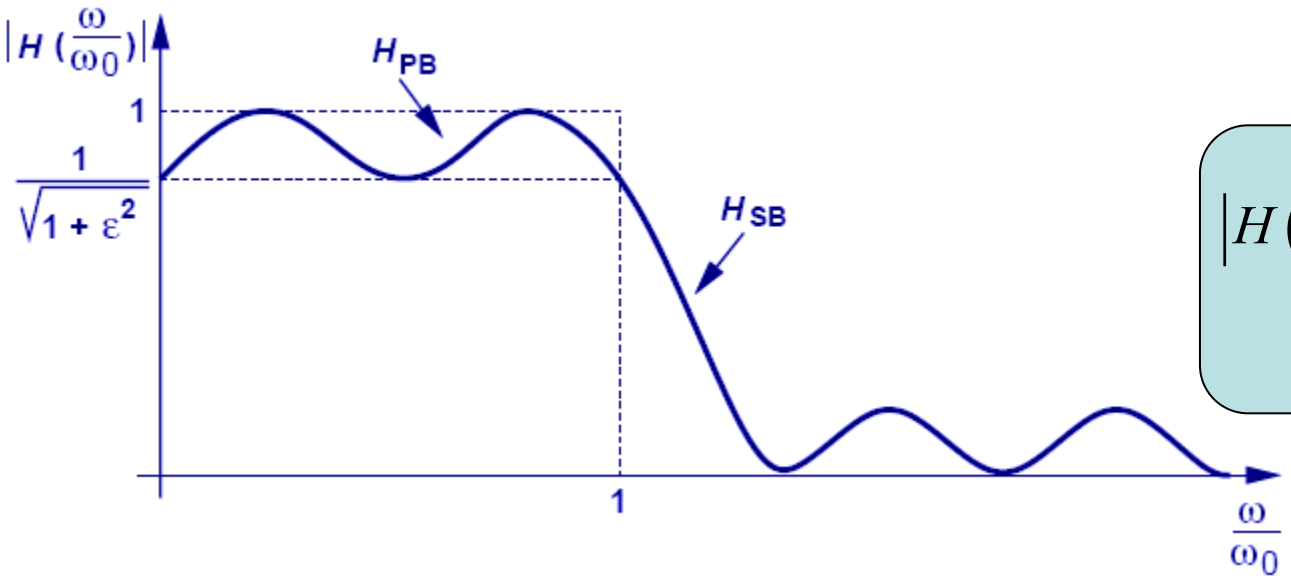
$$p_3 = 2\pi * (1.45MHz) * \left(\cos\frac{2\pi}{3} - j\sin\frac{2\pi}{3} \right)$$

2nd-Order SK

RC section

$$p_2 = 2\pi * (1.45MHz)$$

Chebyshev Response

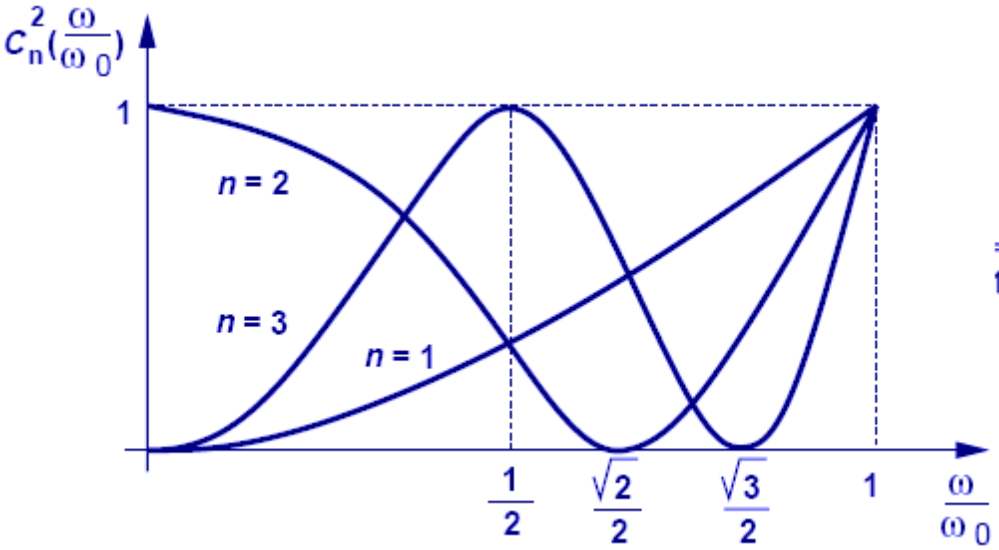


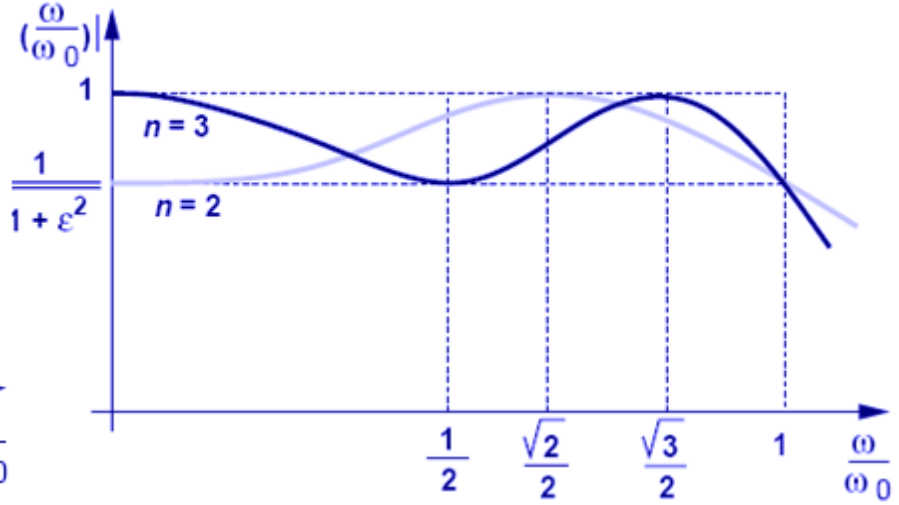
$$|H(j\omega)| = \frac{1}{\sqrt{1+\varepsilon^2 C_n^2\left(\frac{\omega}{\omega_0}\right)}}$$

Chebyshev Polynomial

- **The Chebyshev response provides an "equiripple" pass/stop band response.**

Chebyshev Polynomial





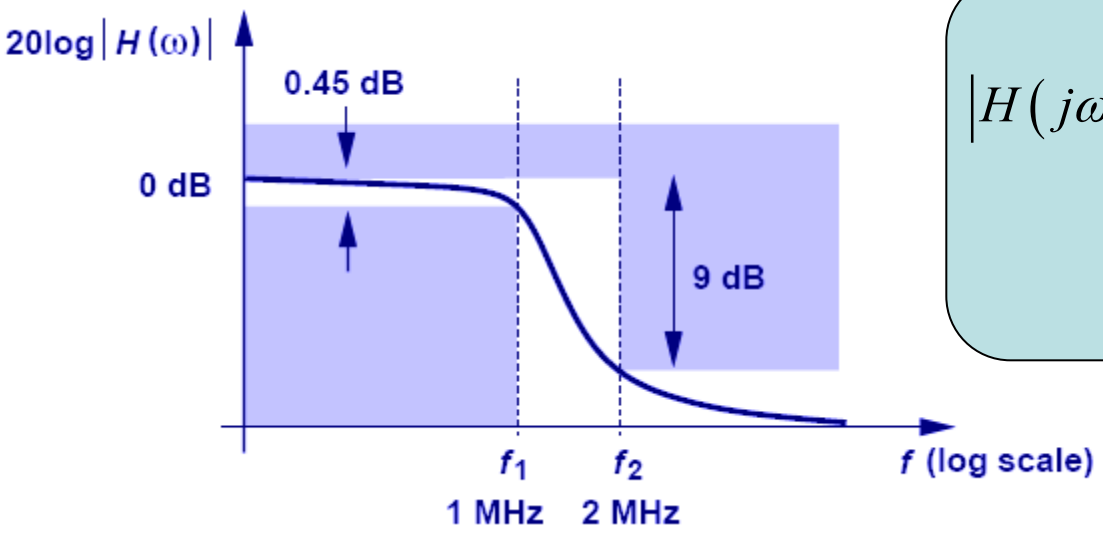
Chebyshev Polynomial for n=1,2,3

Resulting Transfer function for n=2,3

$$C_n\left(\frac{\omega}{\omega_0}\right) = \cos\left(n\cos^{-1}\frac{\omega}{\omega_0}\right), \omega < \omega_0$$

$$= \cosh\left(n\cosh^{-1}\frac{\omega}{\omega_0}\right), \omega > \omega_0$$

Example: Chebyshev Attenuation



$$|H(j\omega)| = \frac{1}{\sqrt{1+0.329^2\left[4\left(\frac{\omega}{\omega_0}\right)^3 - 3\frac{\omega}{\omega_0}\right]^2}}$$

$\omega 0 = 2\pi$ X (2MHz)

- **A third-order Chebyshev response provides an attenuation of -18.7 dB a 2MHz.**

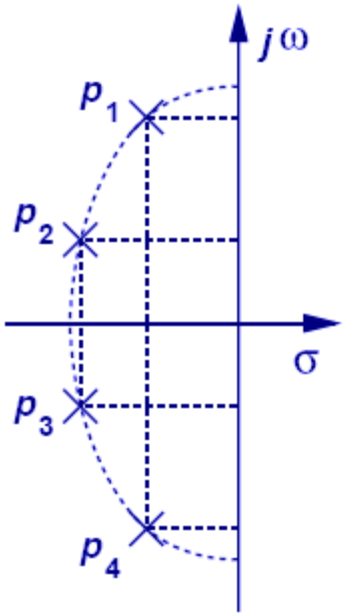
Example: Chebyshev Order

- Passband Ripple: 1 dB
- Bandwidth: 5 MHz
- Attenuation at 10 MHz: 30 dB
- What's the order?

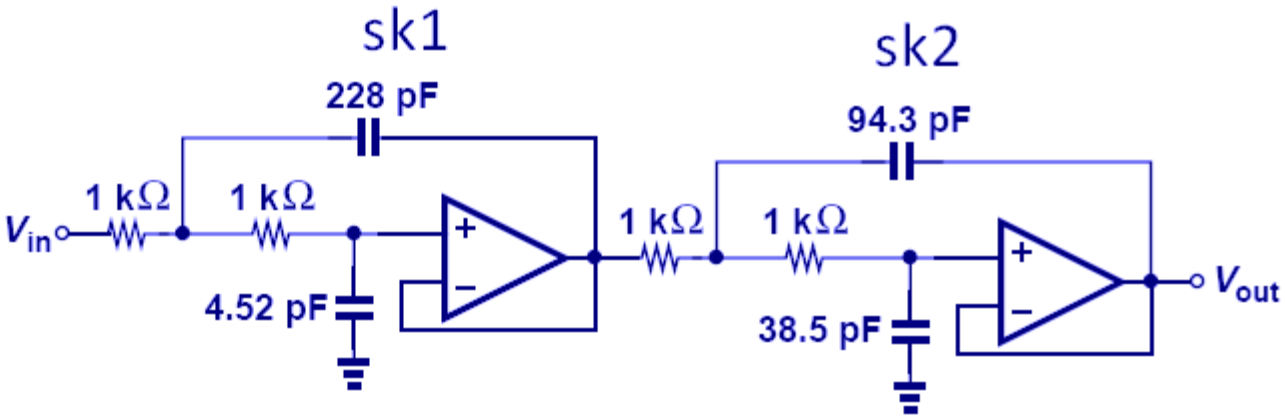
$$\frac{1}{\sqrt{1+0.509^2\cosh^2\left(n\cosh^{-1}2\right)}}=0.0316$$

n>3.66

Example: Chebyshev Response



(a)



(b)

$$p_k = -\omega_0 \sin\frac{(2k-1)\pi}{2n}\sinh\left(\frac{1}{n}\sinh^{-1}\frac{1}{\varepsilon}\right) + j\omega_0 \cos\frac{(2k-1)\pi}{2n}\cosh\left(\frac{1}{n}\sinh^{-1}\frac{1}{\varepsilon}\right)$$

K=1,2,3,4

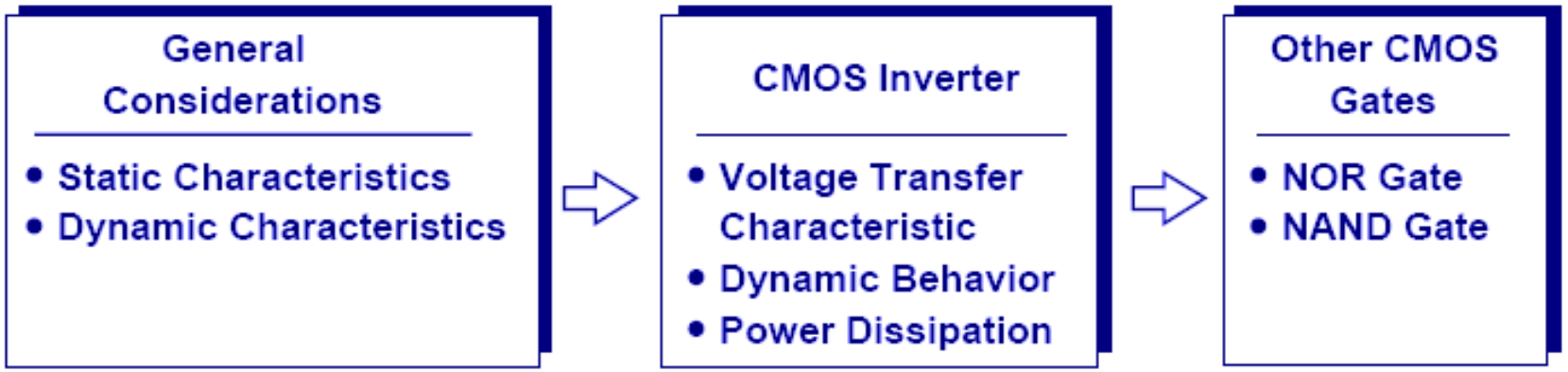
$p_{1,4} = -0.140\omega_0 \pm 0.983 j\omega_0$ **SK1**

$p_{2,3} = -0.337\omega_0 \pm 0.407 j\omega_0$ **SK2**

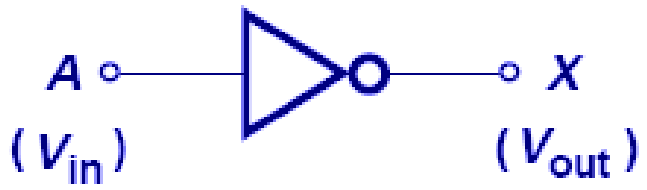
Chapter 15 Digital CMOS Circuits

- 15.1 General Considerations
- 15.2 CMOS Inverter
- 15.3 CMOS NOR and NAND Gates

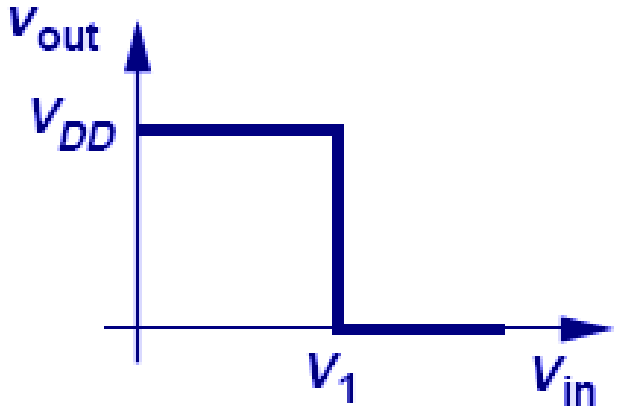
Chapter Outline



Inverter Characteristic



(a)

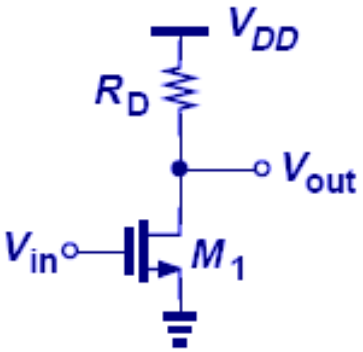


(b)

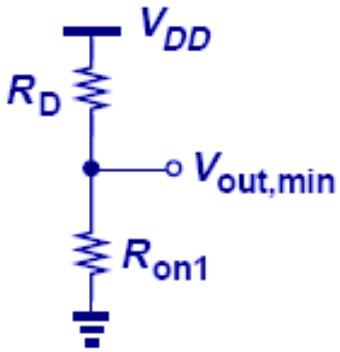
$$X = \bar{A}$$

- **An inverter outputs a logical "1" when the input is a logical "0" and vice versa.**

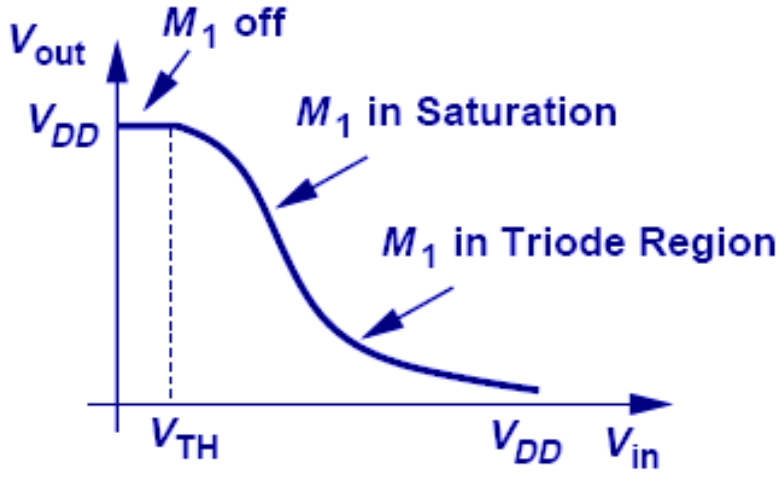
NMOS Inverter



(a)



(b)

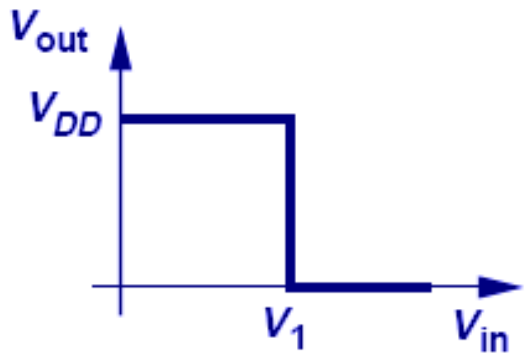


(c)

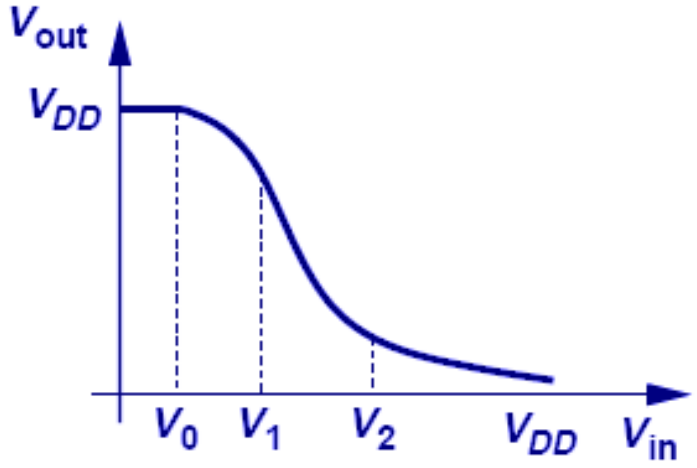
$$R_{on1} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TH})}$$

- **The CS stage resembles a voltage divider between R_D and R_{on1} when M_1 is in deep triode region. It produces V_{DD} when M_1 is off.**

Transition Region Gain



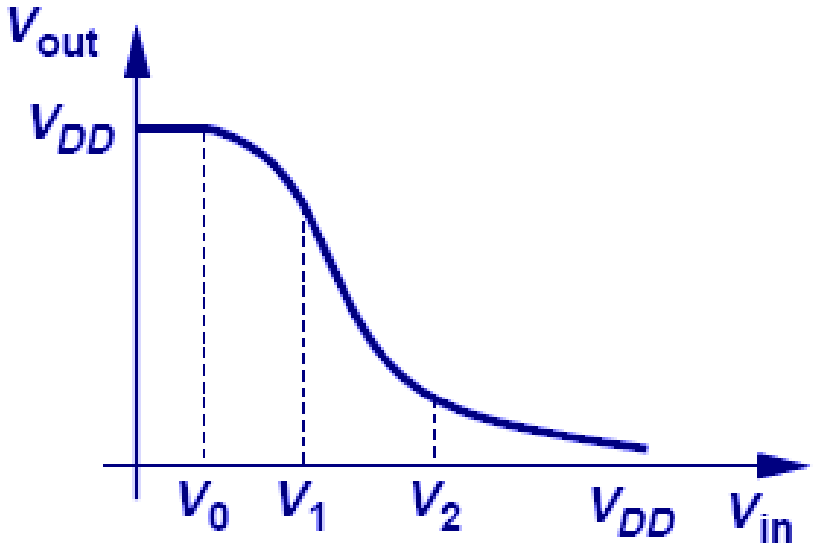
Infinite Transition Region Gain



Finite Transition Region Gain

- **Ideally, the VTC of an inverter has infinite transition region gain. However, practically the gain is finite.**

Example: Transition Gain

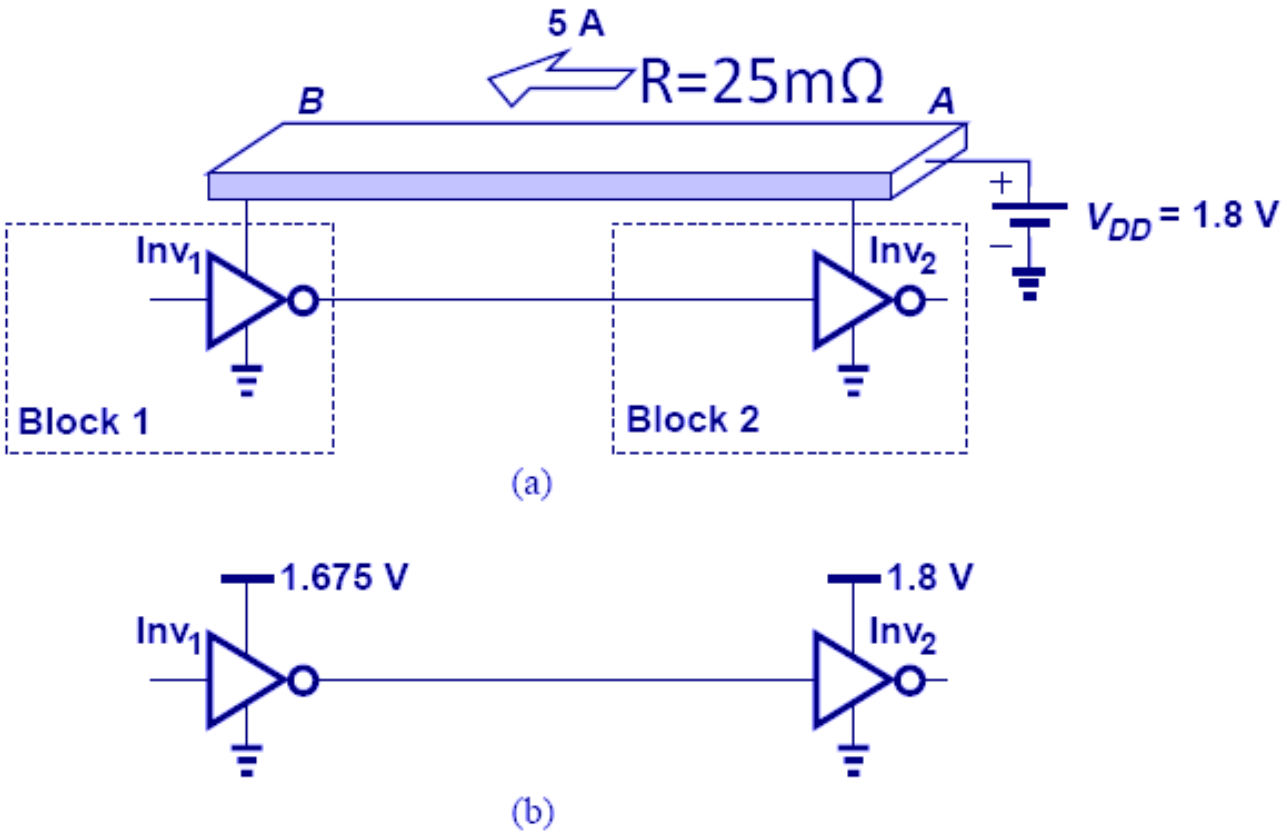


- Transition Region: 50 mV
- Supply voltage: 1.8V

$V_0 - V_2$: Transition Region

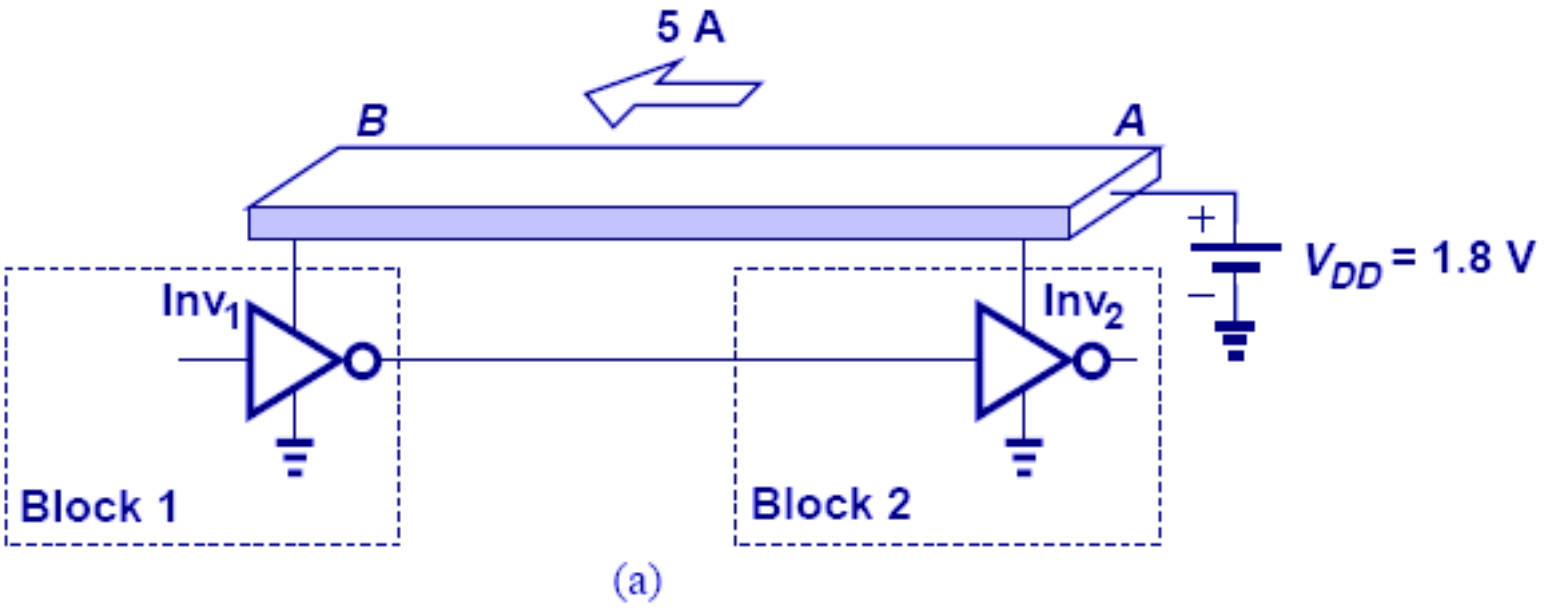
$$A_v = \frac{1.8}{0.05} = 36$$

Logical Level Degradation



- **Since real power buses have losses, the power supply levels at two different locations will be different. This will result in logical level degradation.**

Example: Logic Level Degradation



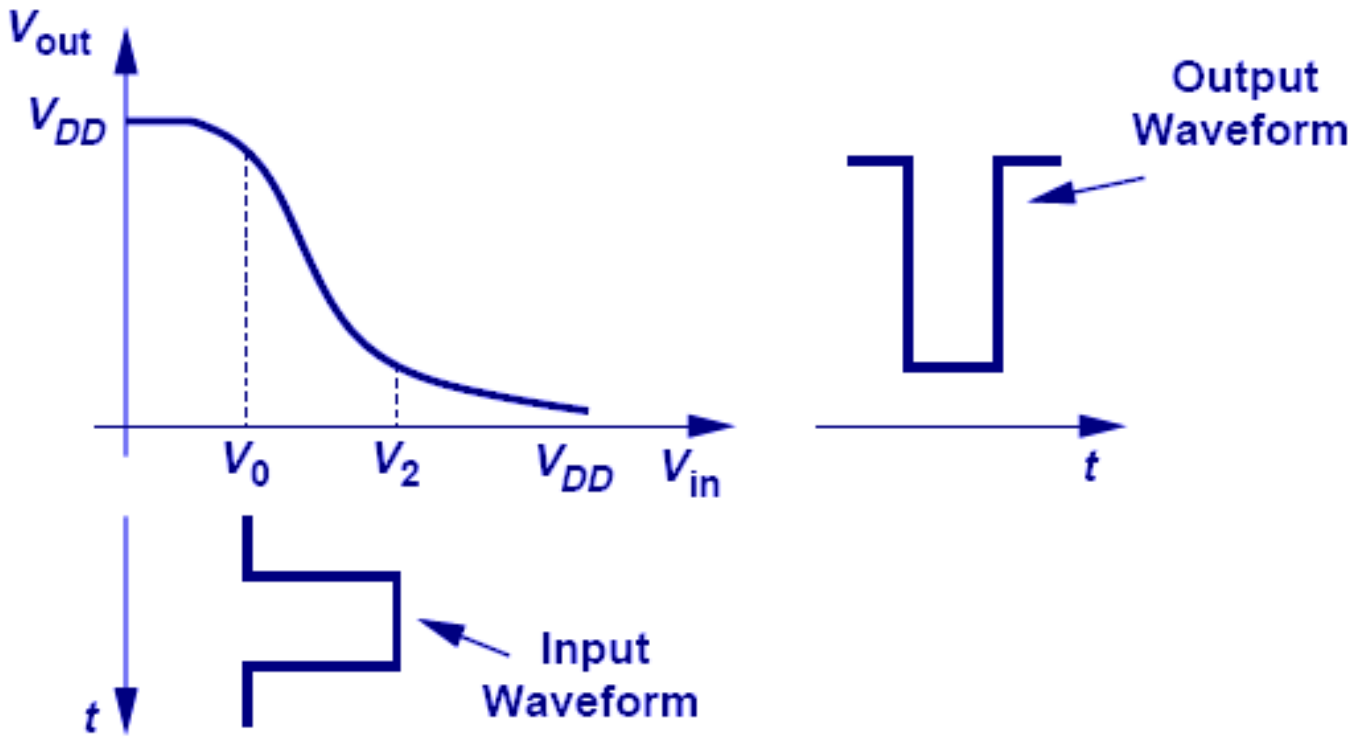
(a)

Supply B=1.675V

Supply A=1.8V

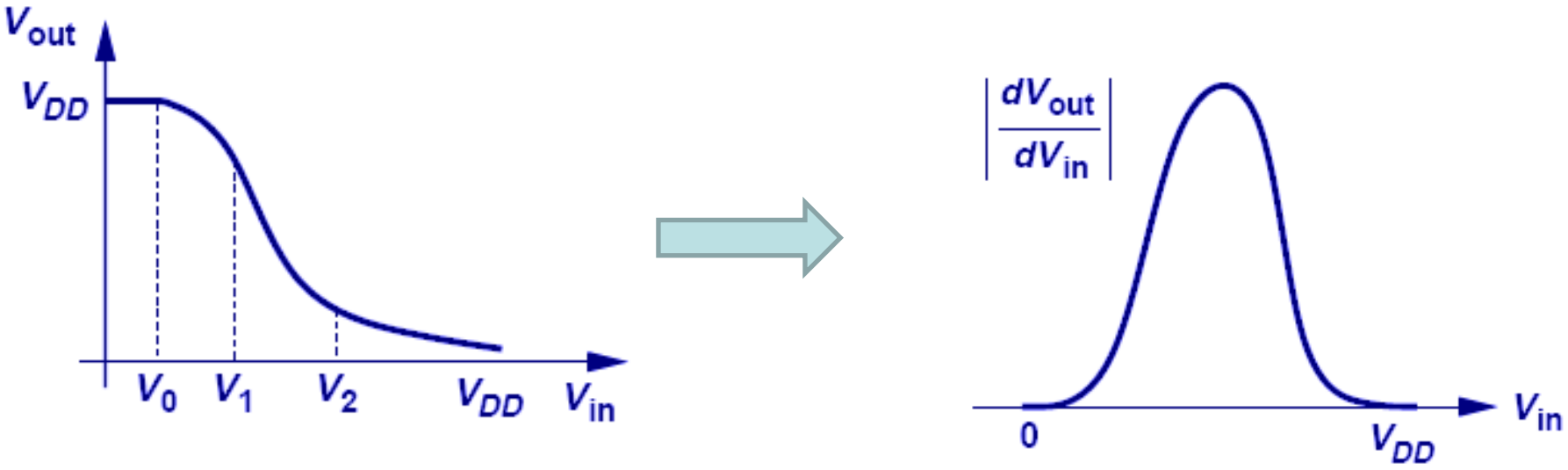
$$\Delta V = 5A \times 25m\Omega = 125mV$$

The Effects of Level Degradation and Finite Gain



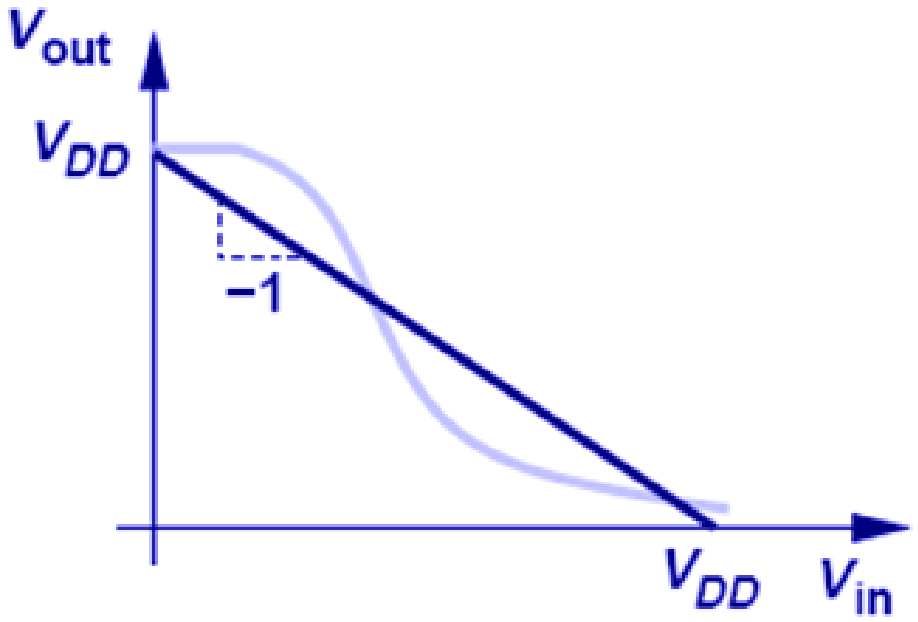
- **In conjunction with finite transition gain, logical level degradation in succeeding gates will reduce the output swings of gates.**

Small-Signal Gain Variation of NMOS Inverter



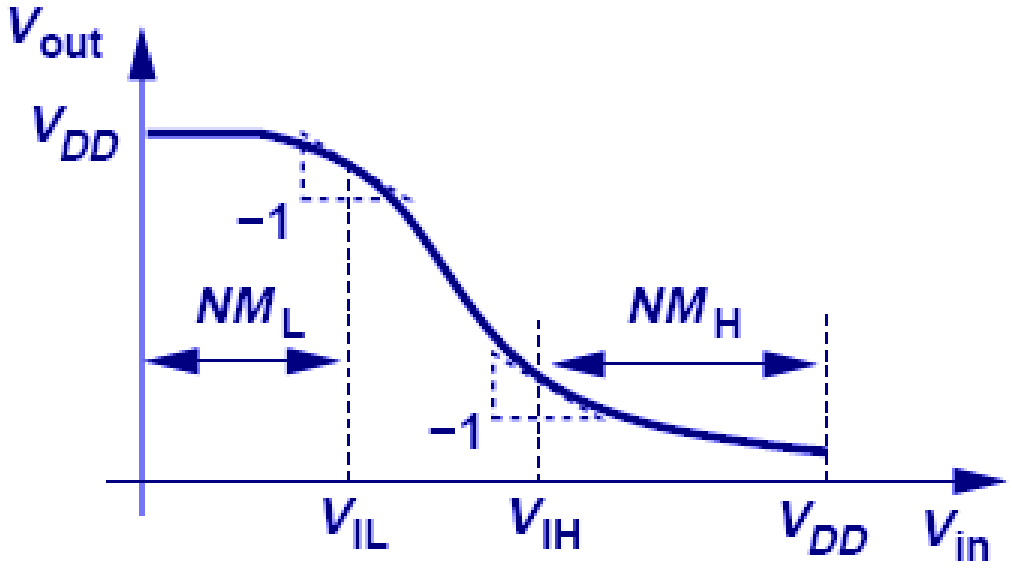
- **As it can be seen, the small-signal gain is the largest in the transition region.**

Above Unity Small-Signal Gain



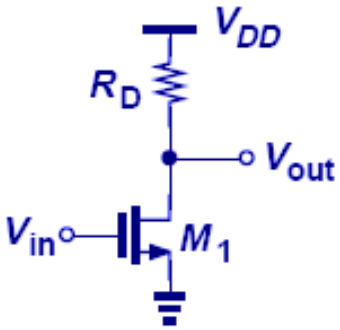
- **The magnitude of the small-signal gain in the transition region can be above 1.**

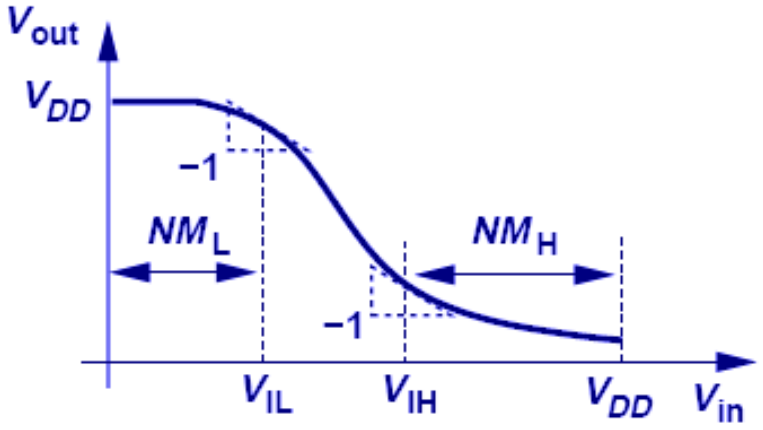
Noise Margin



- **Noise margin is the amount of input logic level degradation that a gate can handle before the small-signal gain becomes -1.**

Example: NMOS Inverter Noise Margin





$$\mathbf{1}: NM_L = V_{IL} = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_D} + V_{TH}$$

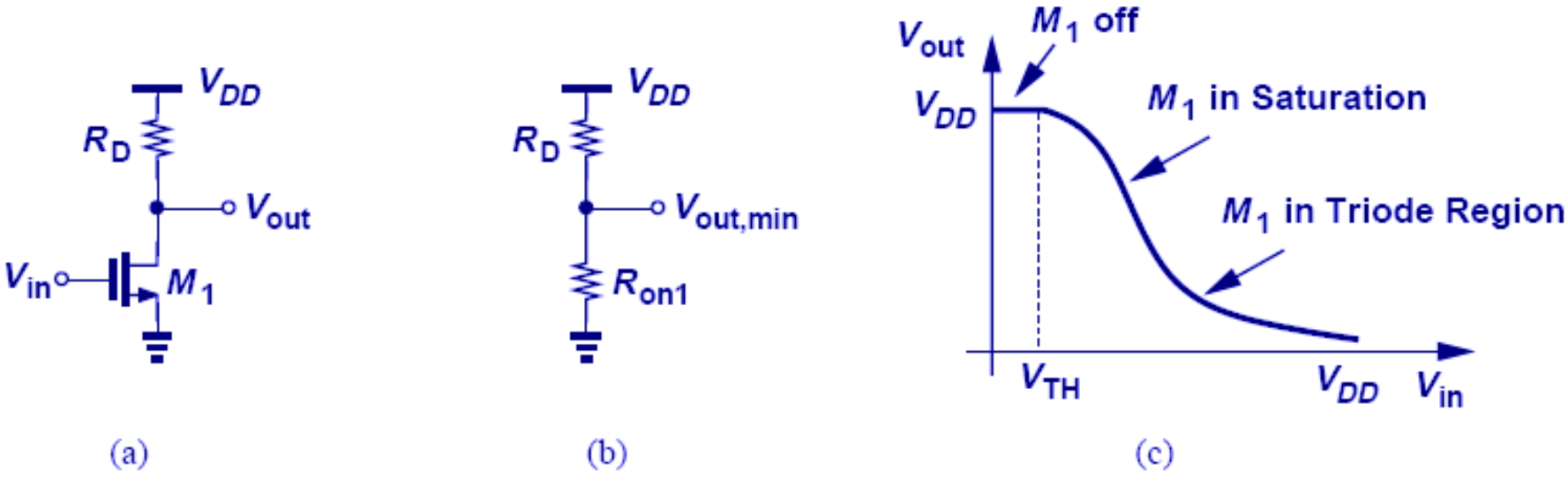
$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox} \frac{W}{L} R_D \left[2\left(V_{in} - V_{TH}\right) V_{out} - V_{out}^2 \right]$$

$$V_{out} = \frac{1}{2\mu_n C_{ox} \frac{W}{L} R_D} + \frac{V_{in} - V_{TH}}{2}$$

$\mathbf{V_{in}=V_{IH}}$

$$\mathbf{2}: NM_H = V_{DD} - V_{IH}$$

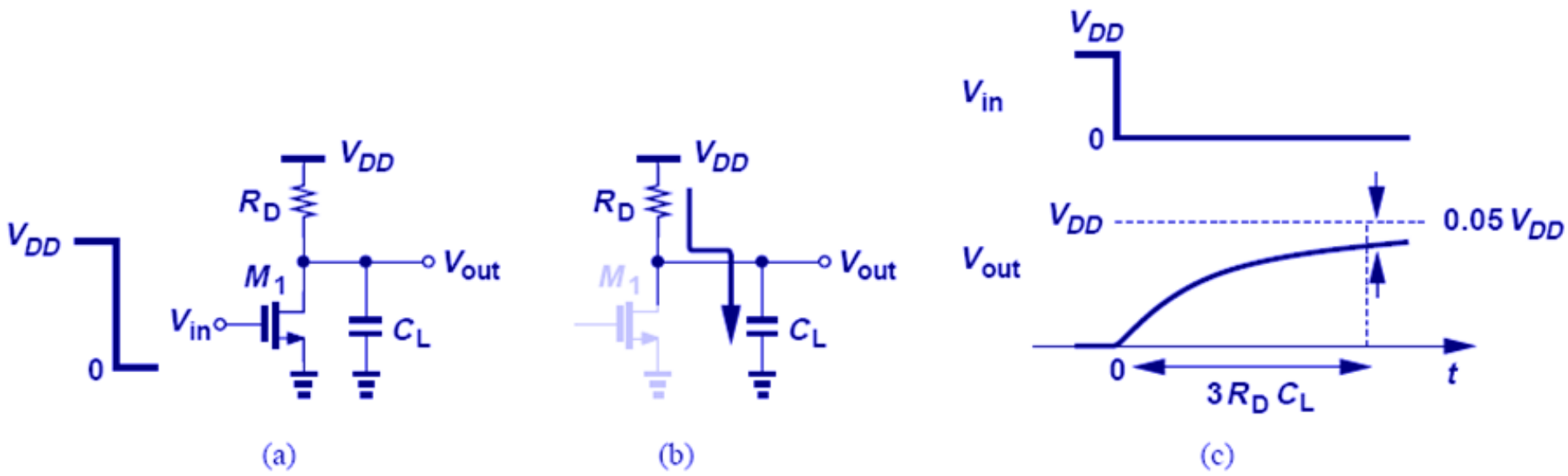
Example: Minimum V_{out}



$$R_D = \frac{19}{\mu_n C_{ox} \frac{W}{L}\left(V_{DD} - V_{TH}\right)}$$

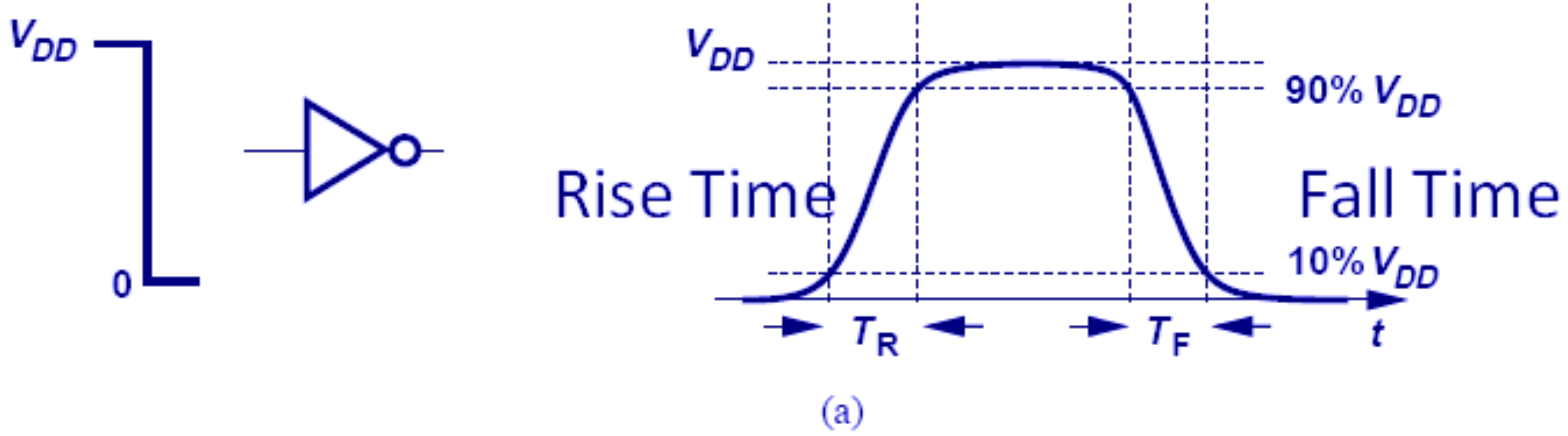
- **To guarantee an output low level that is below $0.05V_{DD}$, R_D is chosen above.**

Dynamic Behavior of NMOS Inverter Gates

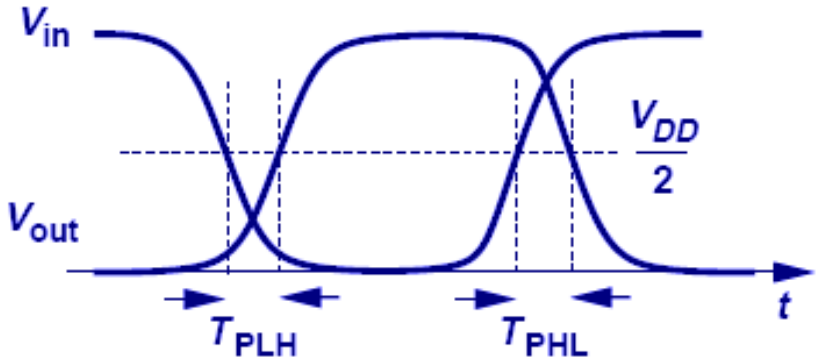


- **Since digital circuits operate with large signals and experience nonlinearity, the concept of transfer function is no longer meaningful. Therefore, we must resort to time-domain analysis to evaluate the speed of a gate.**
- **It usually takes 3 time constants for the output to transition.**

Rise/Fall Time and Delay



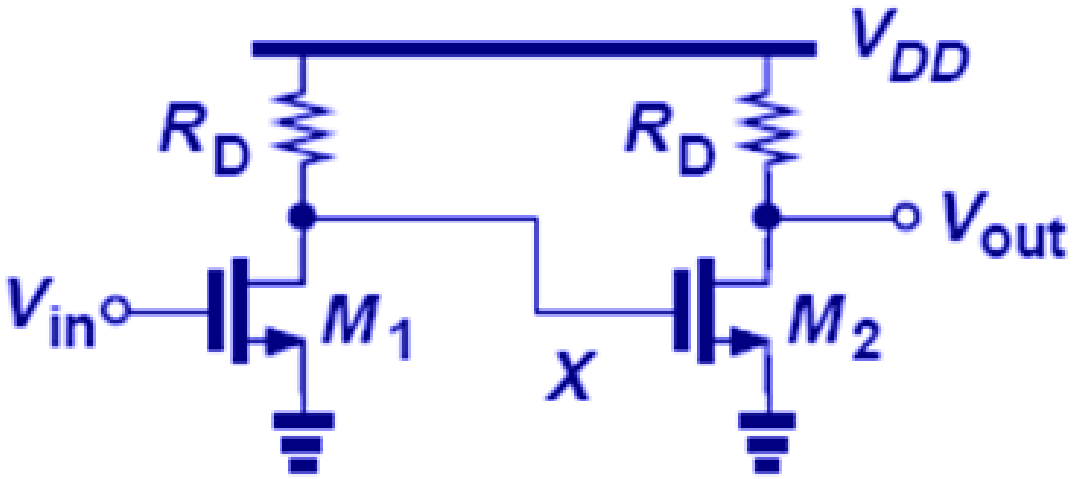
(a)



(b)

Delay

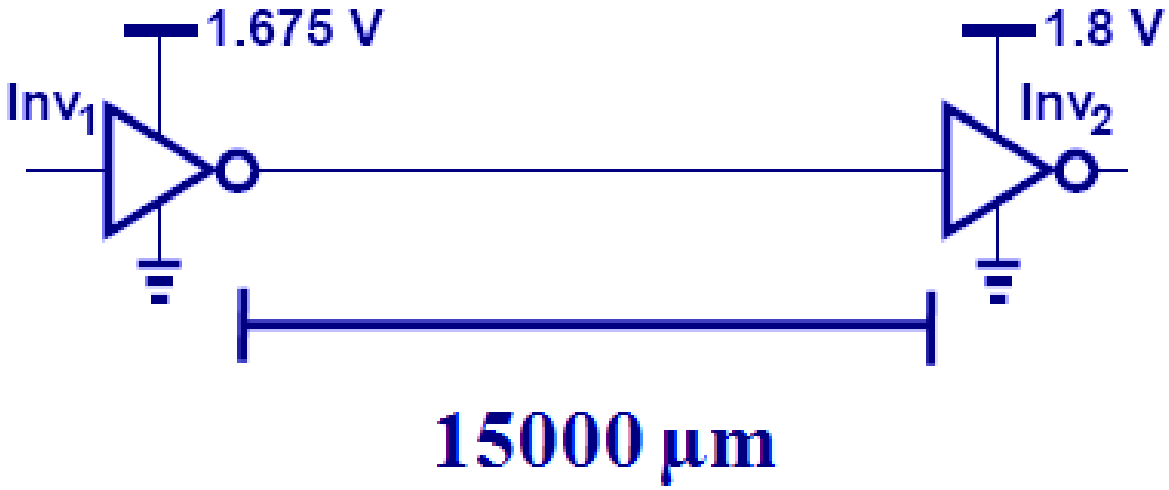
Example: Time Constant



$$\tau = R_D C_X = \frac{19L^2}{\mu_n \left(V_{DD} - V_{TH} \right)}$$

- **Assuming a 5% degradation in output low level, the time constant at node X is shown above.**

Example: Interconnect Capacitance

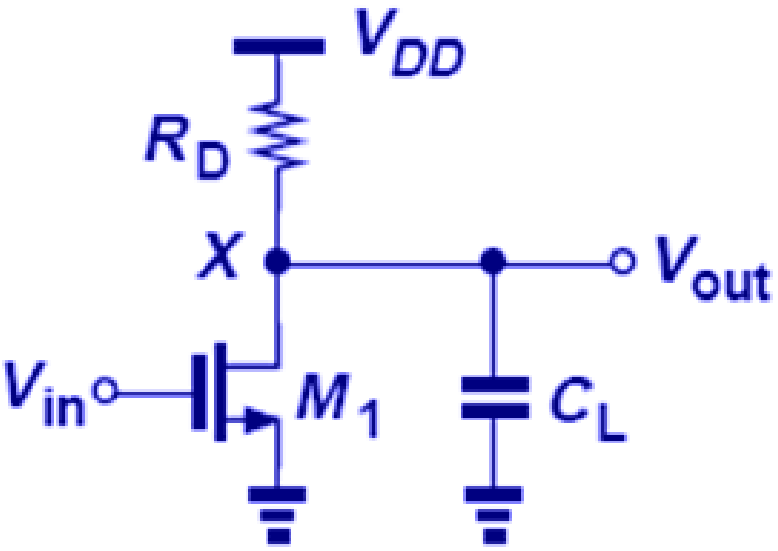


Wire Capacitance per Mircon: 50×10^{-18} F/µm

Total Interconnect Capacitance: $15000 \times 50 \times 10^{-18} = 750$ fF

Equivalent to 640 MOS FETs with W=0.5µm, L=0.18µm, $C_{ox} = 13.5$fF/µm^2

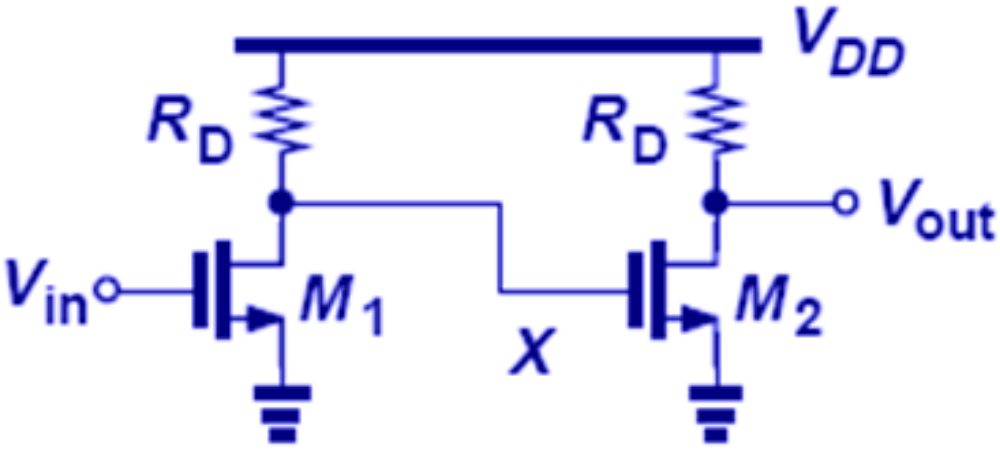
Power-Delay Product



$$PDP \approx V_{DD}^2 C_X$$

- **The power delay product of an NMOS Inverter can be loosely thought of as the amount of energy the gate uses in each switching event.**

Example: Power-Delay Product

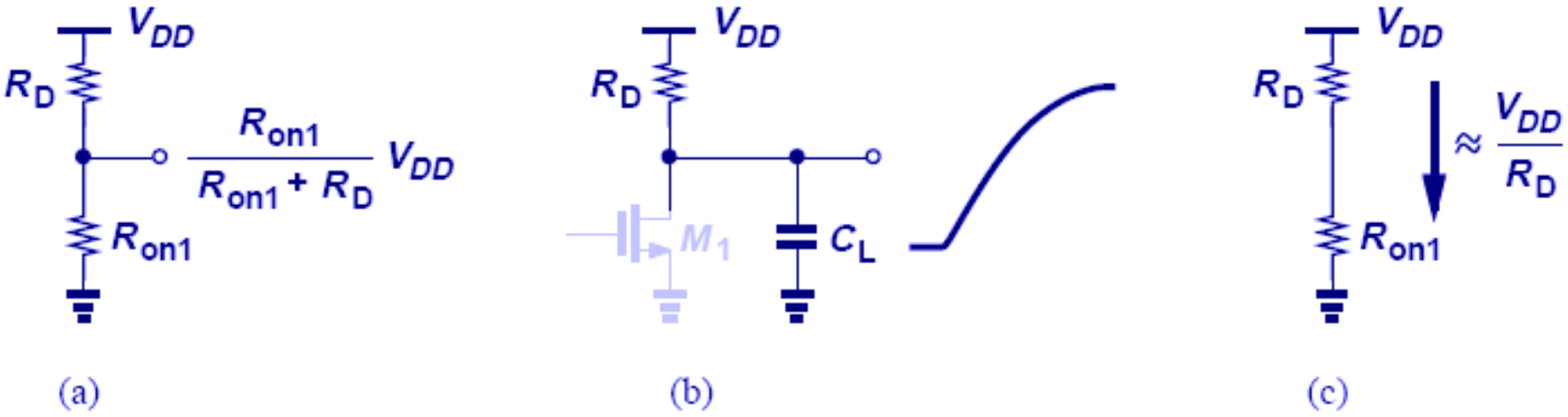


$$T_{PLH} \approx 3R_D C_X$$

$$PDP = \left(I_{DD} V_{DD}\right)\left(3R_D C_X\right)$$

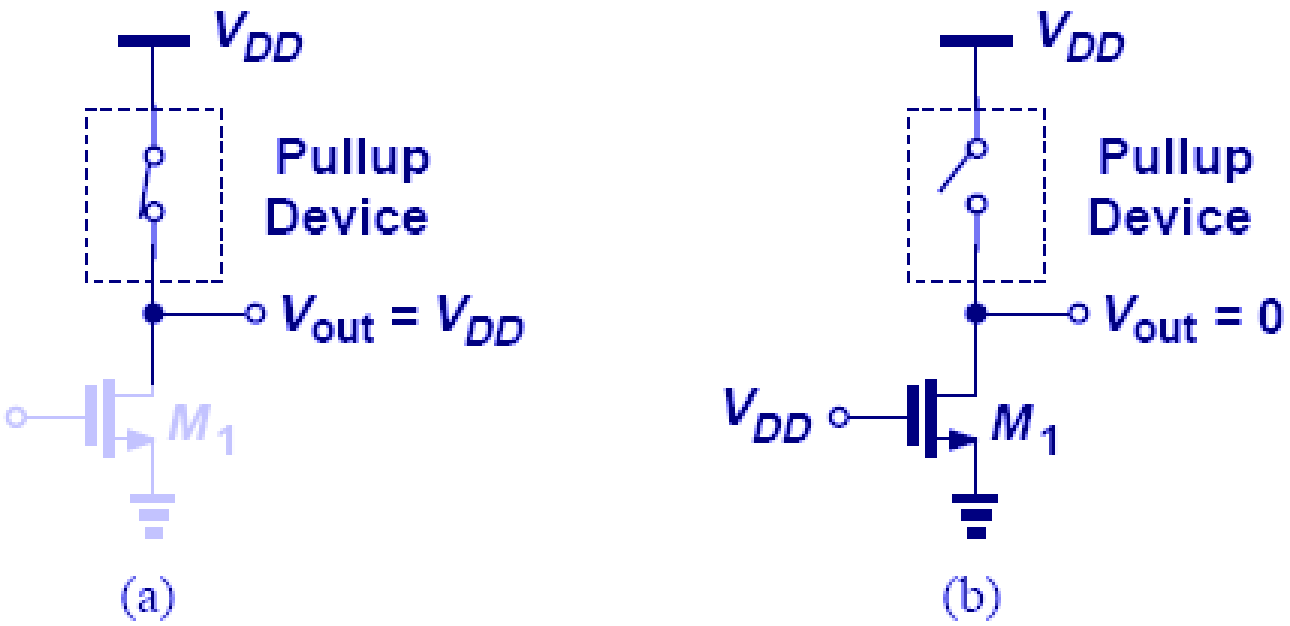
$$PDP = 3V_{DD}^2 WLC_{ox}$$

Drawbacks of the NMOS Inverter



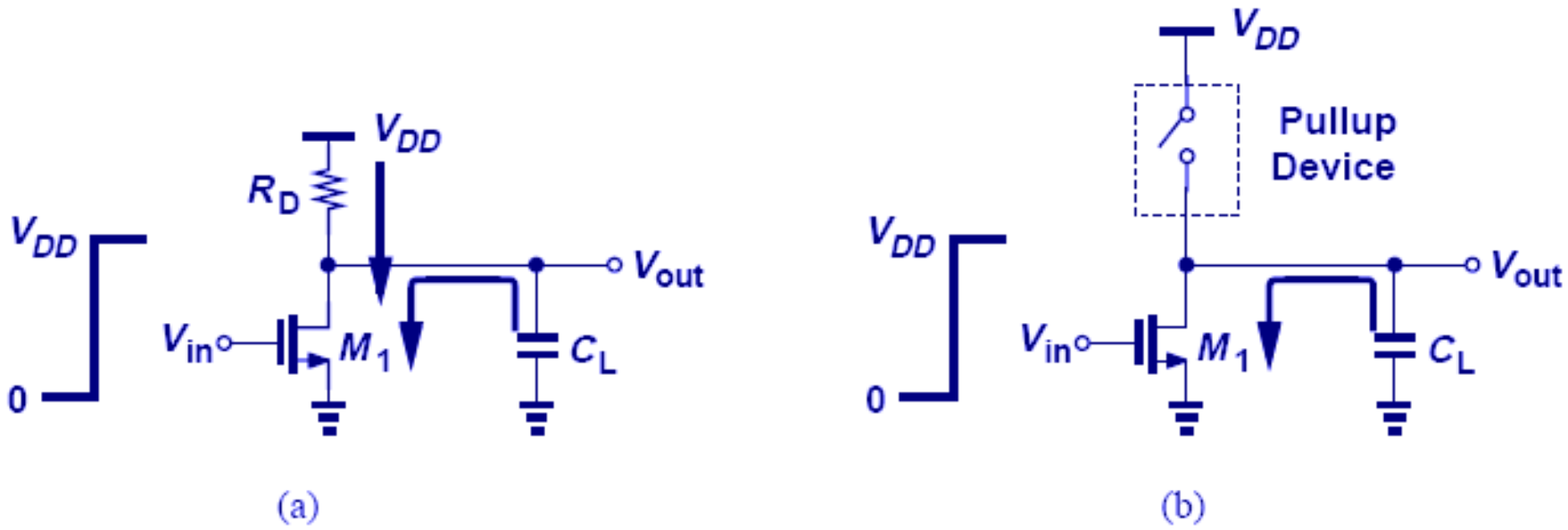
- Because of constant R_D, NMOS inverter consumes static power even when there is no switching.
- R_D presents a tradeoff between speed and power dissipation.

Improved Inverter Topology



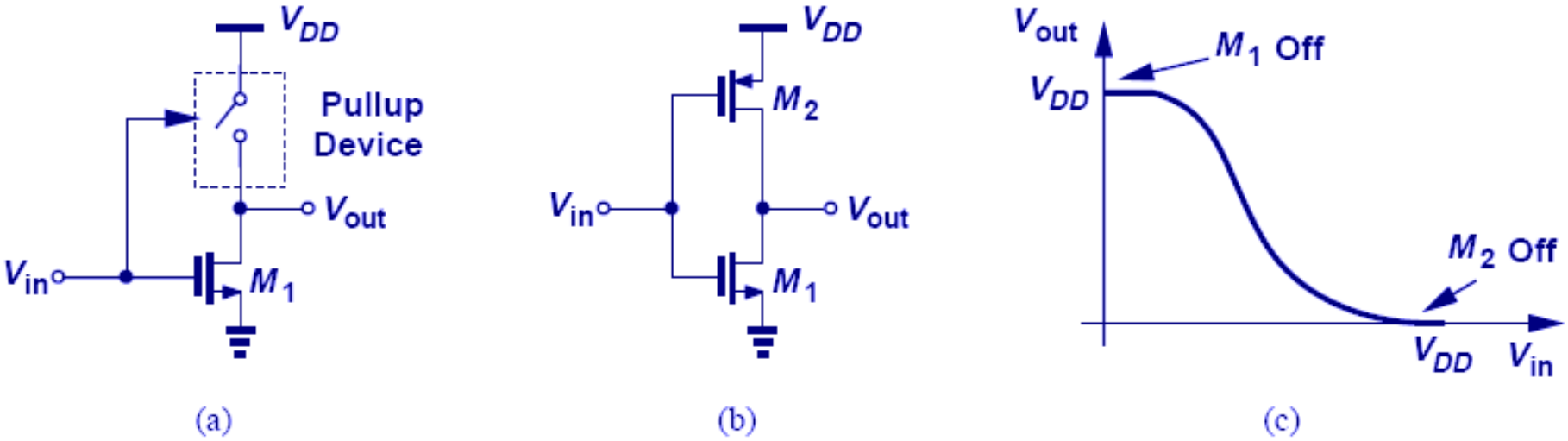
- **A better alternative would probably have been an "intelligent" pullup device that turns on when M_1 is off and vice versa.**

Improved Falltime



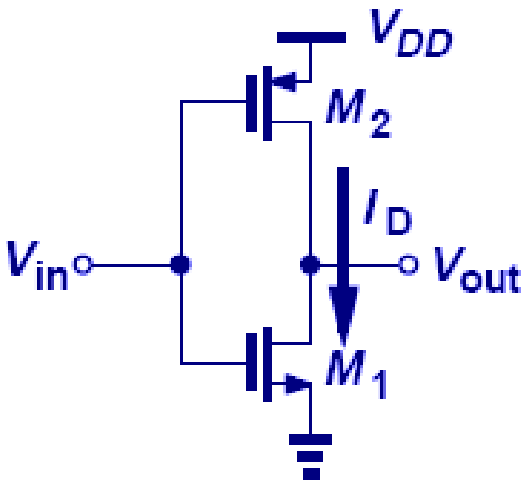
- **This improved inverter topology decreases falltime since all of the current from M_1 is available to discharge the capacitor.**

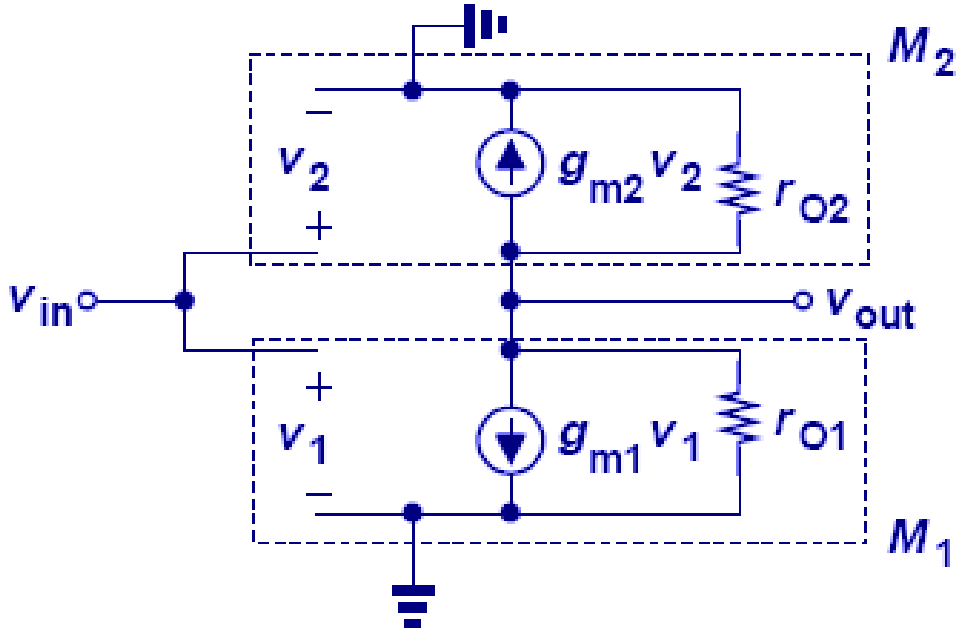
CMOS Inverter



- **A circuit realization of this improved inverter topology is the CMOS inverter shown above.**
- **The NMOS/PMOS pair complement each other to produce the desired effects.**

CMOS Inverter Small-Signal Model

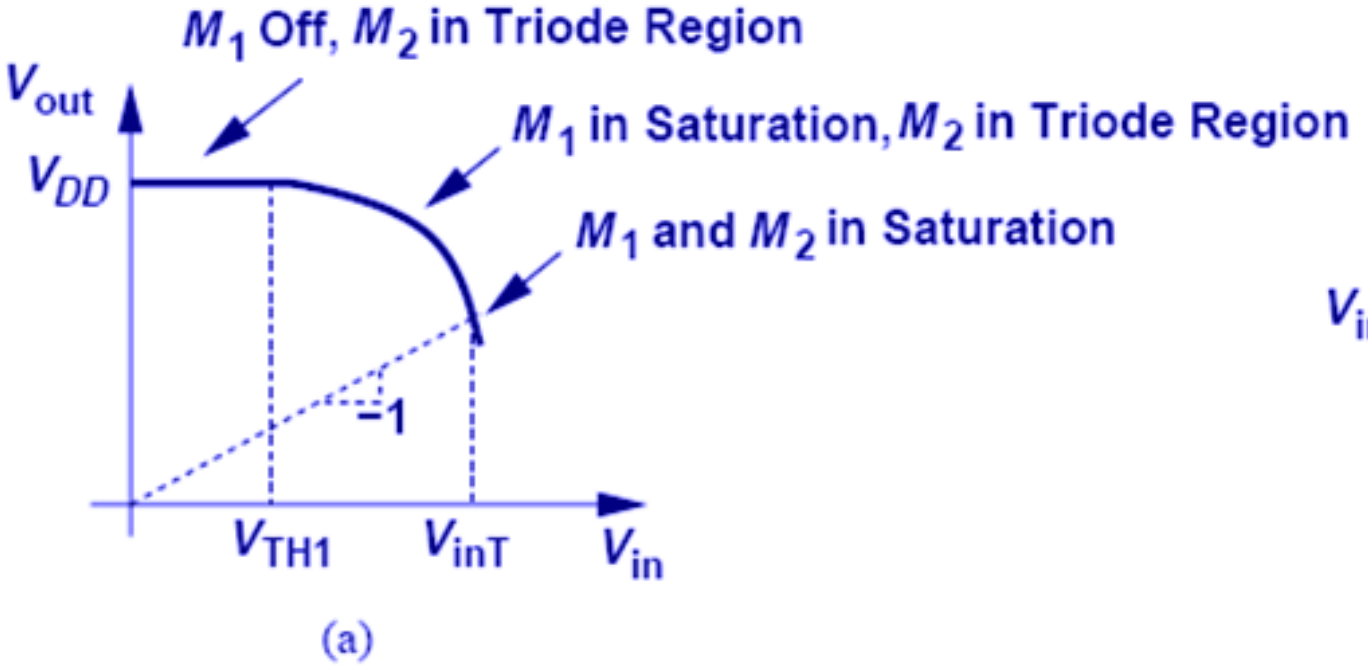


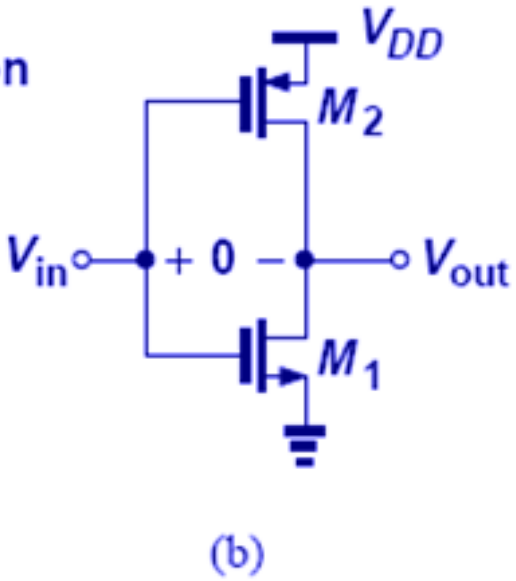


$$\frac{v_{out}}{v_{in}} = -\left(g_{m1} + g_{m2}\right)\left(r_{O1} \parallel r_{O2}\right)$$

- **When both M_1 and M_2 are in saturation, the small-signal gain is shown above.**

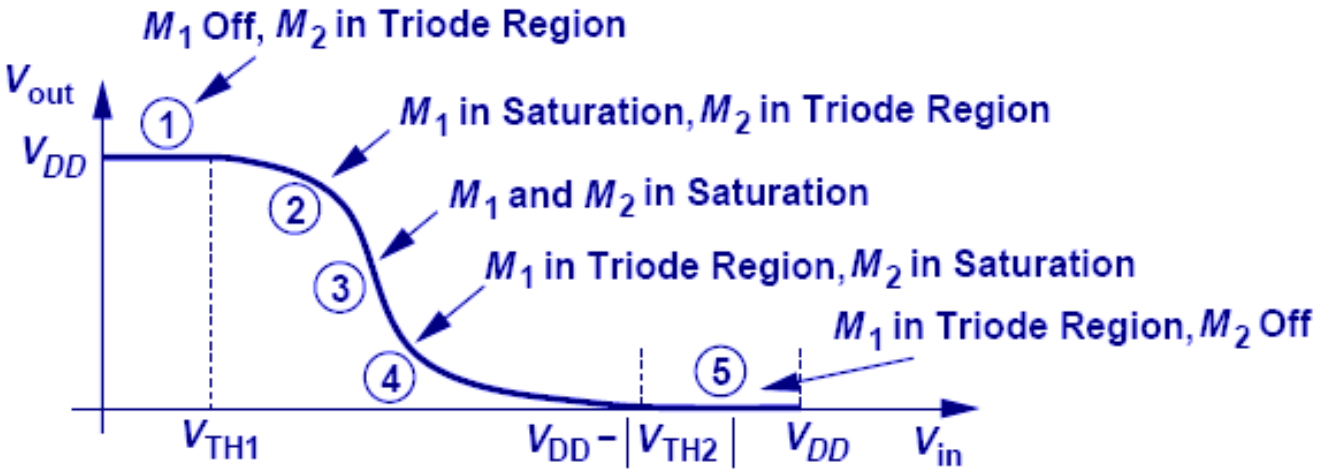
Switching Threshold

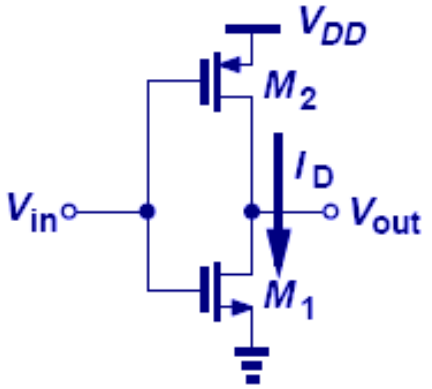




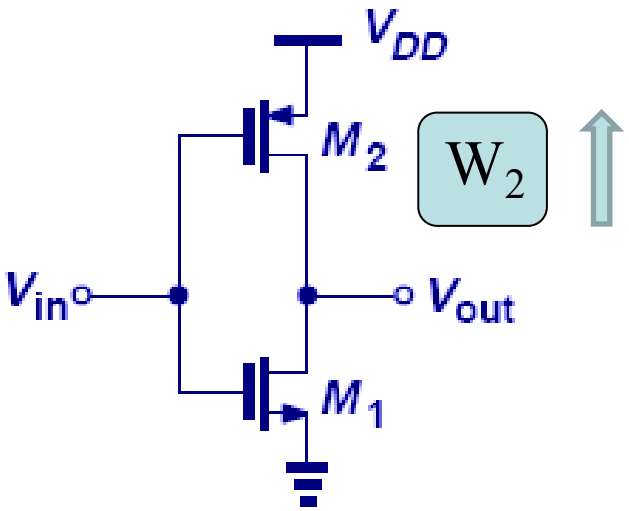
- The switching threshold (V_{inT}) or the "trip point" of the inverter is when V_{out} equals V_{in}.
- If $V_{inT} = V_{dd}/2$, then $W_2/W_1 = \mu_n/\mu_p$

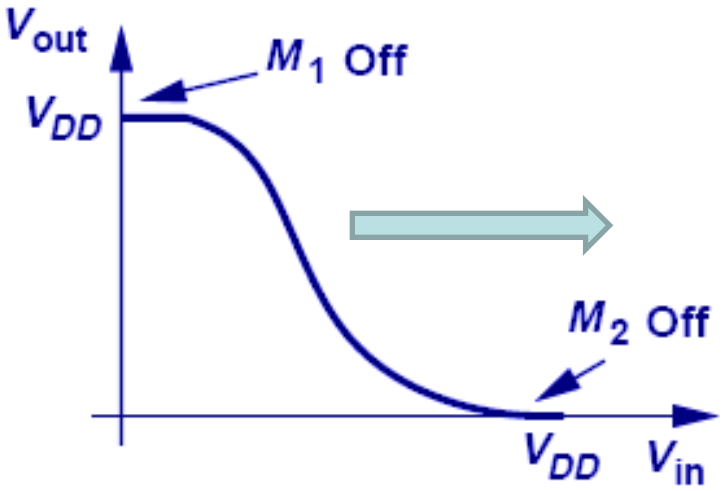
CMOS Inverter VTC





Example: VTC





- **As the PMOS device is made stronger, the VTC is shifted to the right.**

Noise Margins

$$NM_L = V_{IL}$$

$$NM_H = V_{dd} - V_{IH}$$

$$V_{IL} = \frac{2\sqrt{a}\left(V_{dd} - V_{TH1} - |V_{TH2}|\right)}{(a-1)\sqrt{a+3}} - \frac{V_{dd} - aV_{TH1} - |V_{TH2}|}{a-1}$$

V_{IL} is the low-level input voltage at which ($\delta V_{out}/\delta V_{in}$)=-1

$$V_{IH} = \frac{2a\left(V_{dd} - V_{TH1} - |V_{TH2}|\right)}{(a-1)\sqrt{1+3a}} - \frac{V_{dd} - aV_{TH1} - |V_{TH2}|}{a-1}$$

V_{IH} is the high-level input voltage at which ($\delta V_{out}/\delta V_{in}$)=-1

$$a = \frac{\mu_n \left(\frac{W}{L}\right)_1}{\mu_p \left(\frac{W}{L}\right)_2}$$

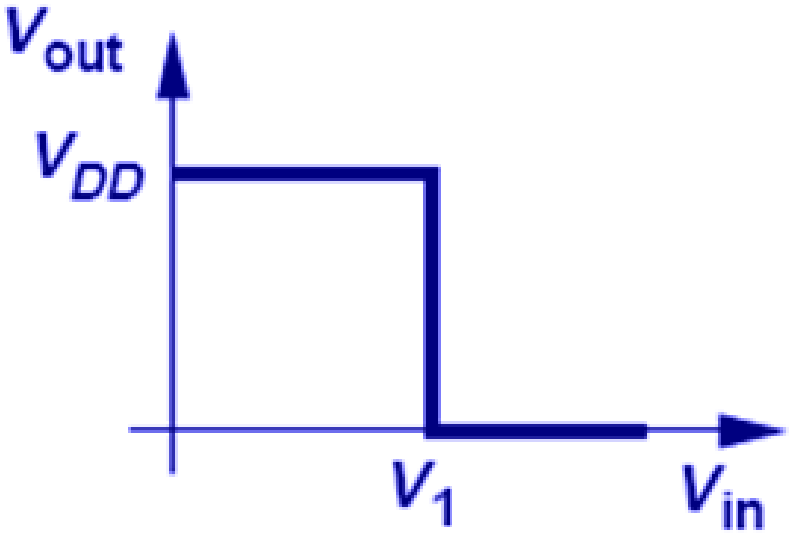
V_{IL} of a Symmetric VTC

$$V_{IL} = \frac{2\sqrt{a}\left(V_{DD} - 2V_{TH1}\right) - \sqrt{a+3}\left[V_{DD} - (a+1)V_{TH1}\right]}{(a-1)\sqrt{a+3}}$$

Symmetric VTC: a=1

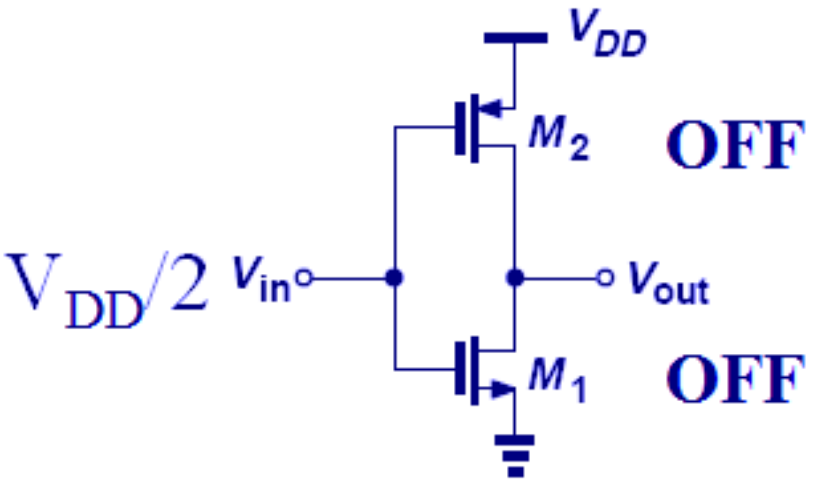
$$V_{IL} = \frac{3}{8}V_{DD} + \frac{1}{4}V_{TH1}$$

Noise Margins of an Ideal Symmetric VTC



$$NM_{H,ideal} = NM_{L,ideal} = \frac{V_{DD}}{2}$$

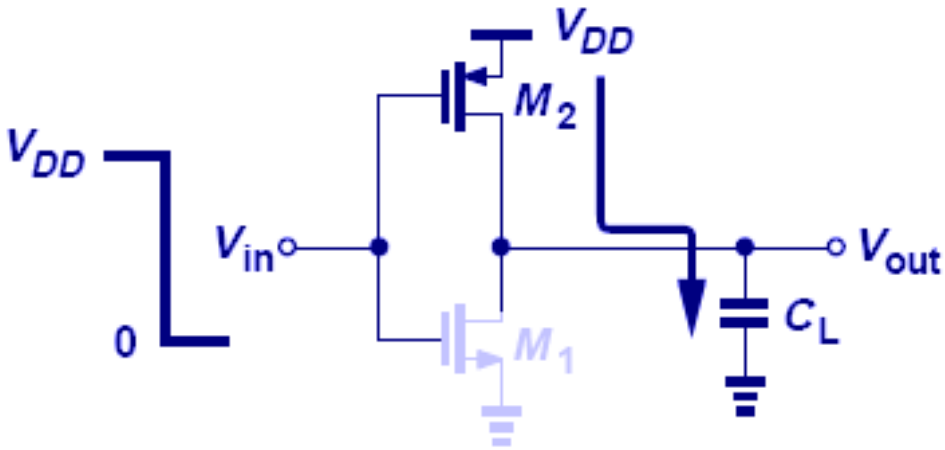
Floating Output



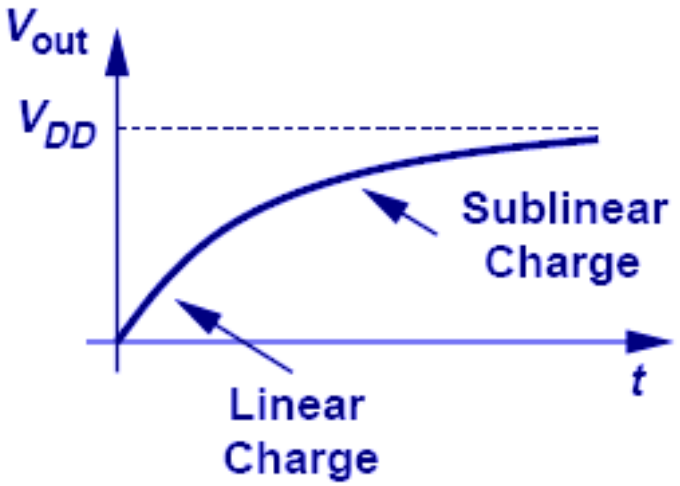
$$V_{TH1} > V_{DD}/2$$
$$|V_{TH2}| > V_{DD}/2$$

- When $V_{in}=V_{DD}/2$, M_2 and M_1 will both be off and the output floats.

Charging Dynamics of CMOS Inverter



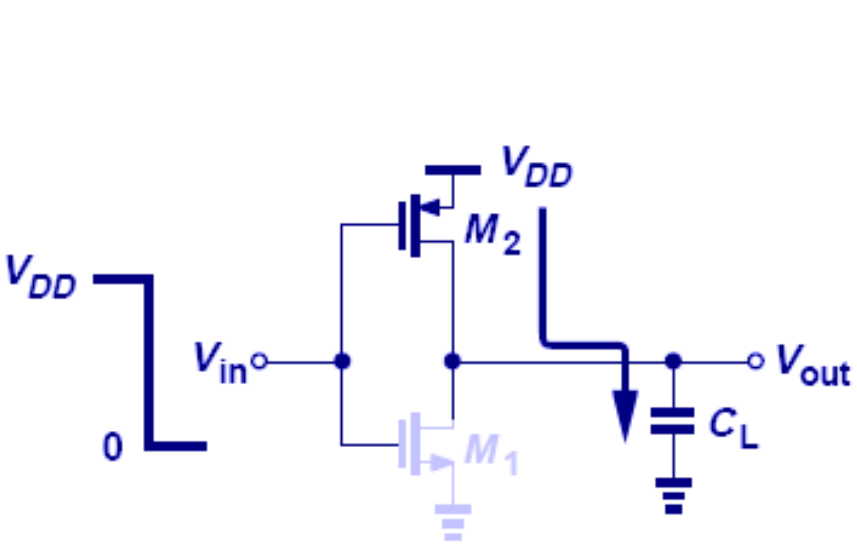
(a)

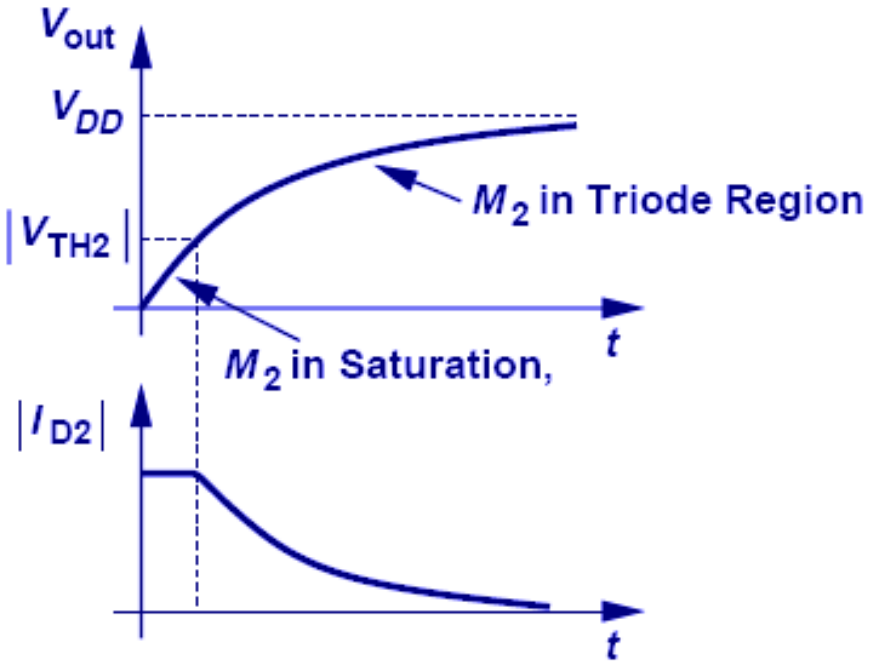


(b)

- As V_{out} is initially charged high, the charging is linear since M_2 is in saturation. However, as M_2 enters triode region the charge rate becomes sublinear.

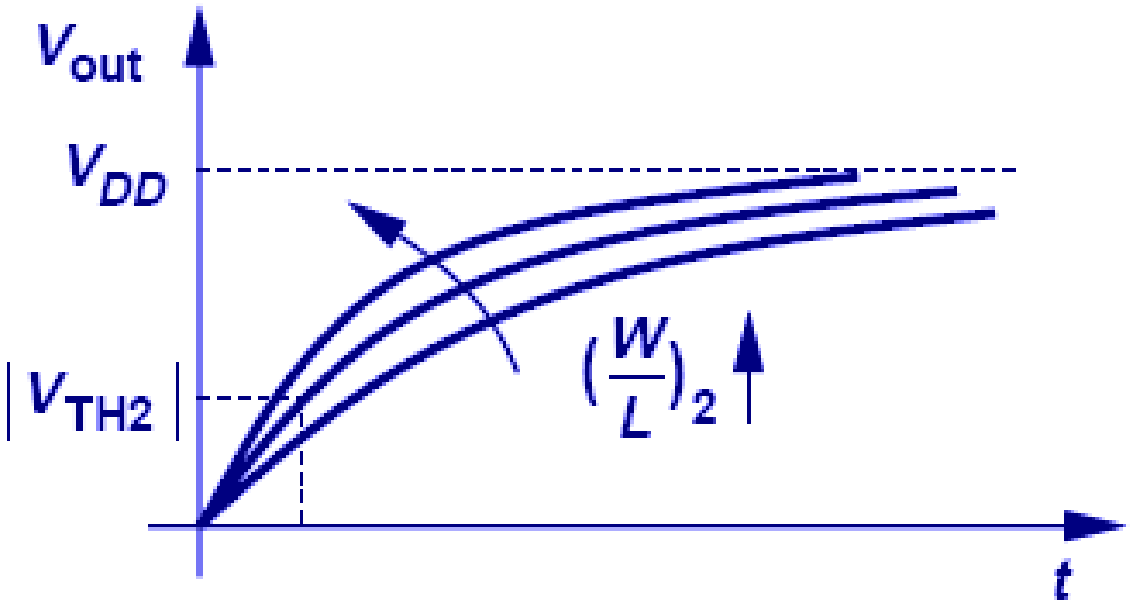
Charging Current Variation with Time





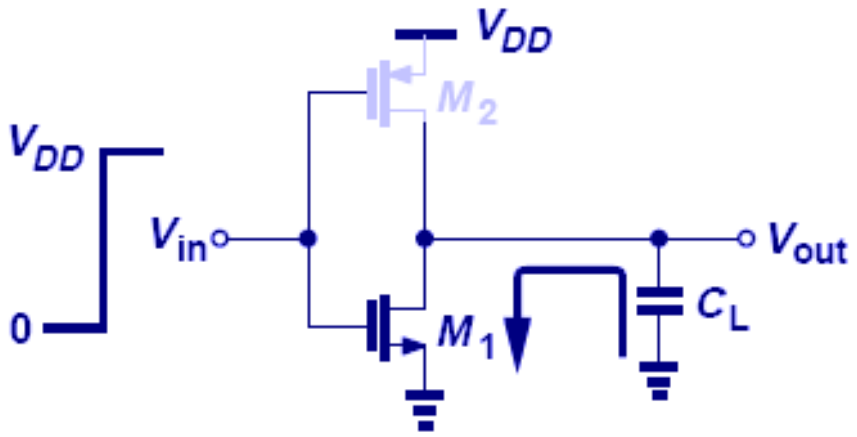
- The current of M_2 is initially constant as M_2 is in saturation. However as M_2 enters triode, its current decreases.

Size Variation Effect to Output Transition

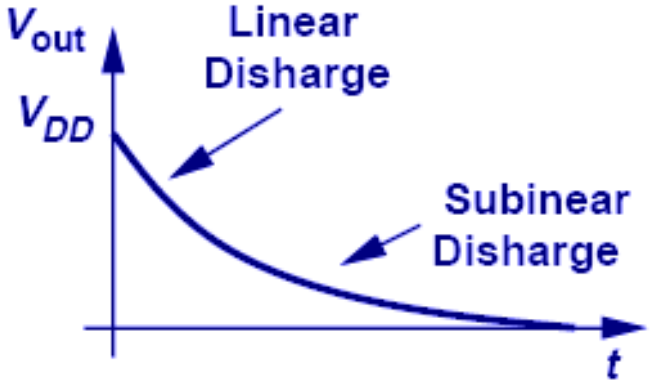


- **As the PMOS size is increased, the output exhibits a faster transition.**

Discharging Dynamics of CMOS Inverter



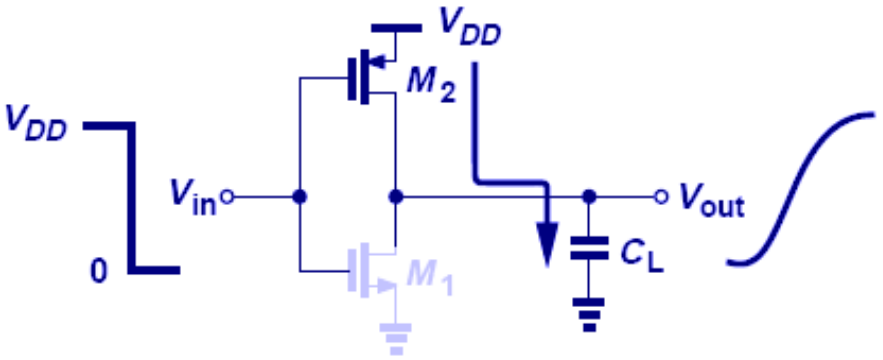
(a)



(b)

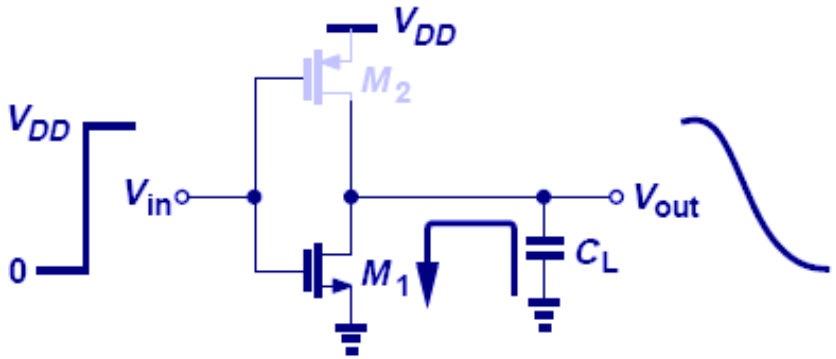
- **Similar to the charging dynamics, the discharge is linear when M_1 is in saturation and becomes sublinear as M_1 enters triode region.**

Rise/Fall Time Delay



Rise Time Delay

$$T_{PLH} = \frac{C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2\left[V_{DD} - |V_{TH2}|\right]}\left[\frac{2|V_{TH2}|}{V_{DD} - V_{TH2}} + \ln\left(3 - 4\frac{V_{TH2}}{V_{DD}}\right)\right]$$



Fall Time Delay

$$T_{PHL} = \frac{C_L}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[V_{DD} - |V_{TH1}|\right]}\left[\frac{2|V_{TH1}|}{V_{DD} - V_{TH1}} + \ln\left(3 - 4\frac{V_{TH1}}{V_{DD}}\right)\right]$$

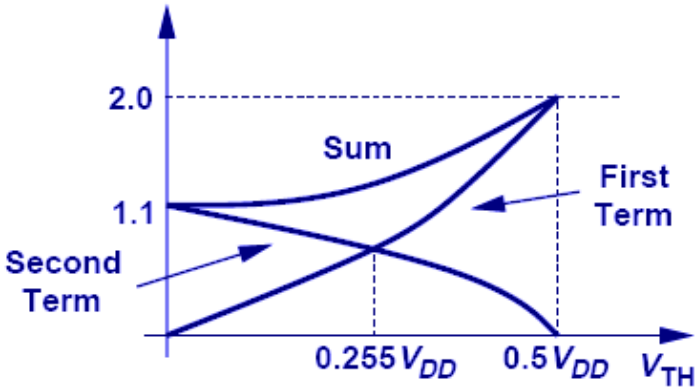
Example: Averaged Rise Time Delay

$$I_{AVG} = \frac{1}{4}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{DD} - |V_{TH2}|\right)^2$$

$$T_{PLH2} = \frac{C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{DD} - |V_{TH2}|\right)} \cdot \frac{V_{DD}/2 - \left(V_{DD} - |V_{TH2}|\right)}{V_{DD} - |V_{TH2}|}$$

$$T_{PLH2} \approx \frac{4}{3} R_{on2} C_L$$

Low Threshold Improves Speed



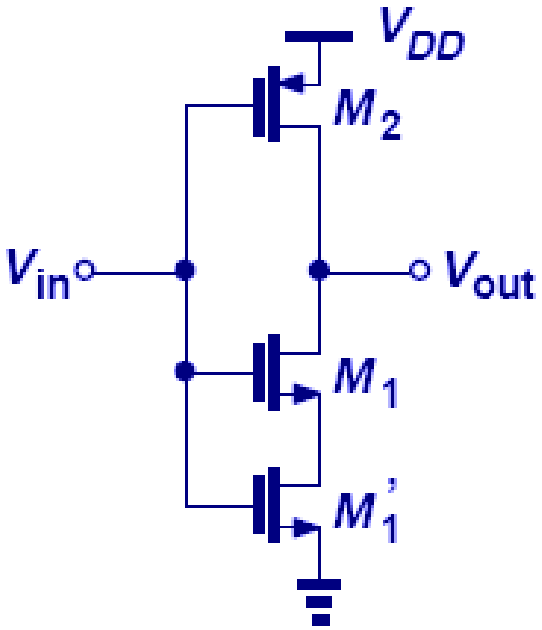
1st Term

$$T_{PLH/HL} = \frac{C_L}{\mu_{p/n} C_{ox} \left(\frac{W}{L}\right)_{2/1} \left[V_{DD} - |V_{TH2/1}|\right]} \left[\frac{2|V_{TH2/1}|}{V_{DD} - V_{TH2/1}} + \ln\left(3 - 4\frac{V_{TH2/1}}{V_{DD}}\right)\right]$$

2nd Term

- The sum of the 1st and 2nd terms of the bracket is the smallest when V_{TH} is the smallest, hence low V_{TH} improves speed.

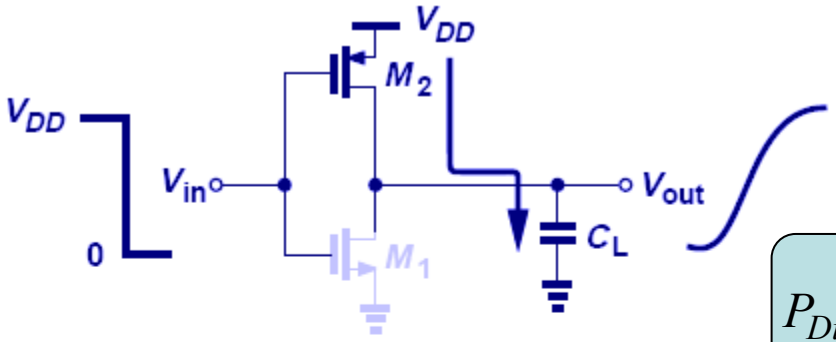
Example: Increased Fall Time Due to Manufacturing Error



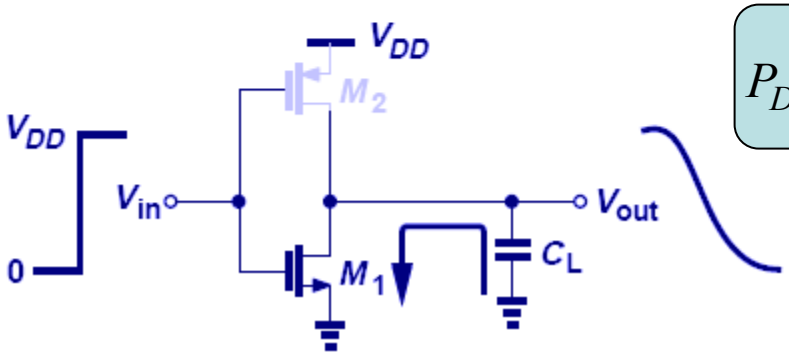
$$R_{on1} \parallel R'_{on1} = \frac{1}{\mu_n C_{ox}\left(\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)'_1\right](V_{DD} - V_{TH1})\right)} = 2R_{ON1}$$

- **Since pull-down resistance is doubled, the fall time is also doubled.**

Power Dissipation of the CMOS Inverter



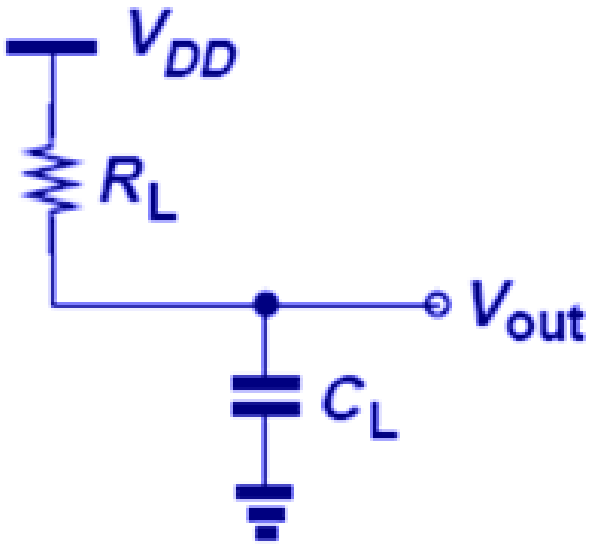
$$P_{Dissipation\_PMOS} = \frac{1}{2} C_L V_{DD}^2 f_{in}$$



$$P_{Dissipation\_NMOS} = \frac{1}{2} C_L V_{DD}^2 f_{in}$$

$$P_{supply} = C_L V_{DD}^2 f_{in}$$

Example: Energy Calculation

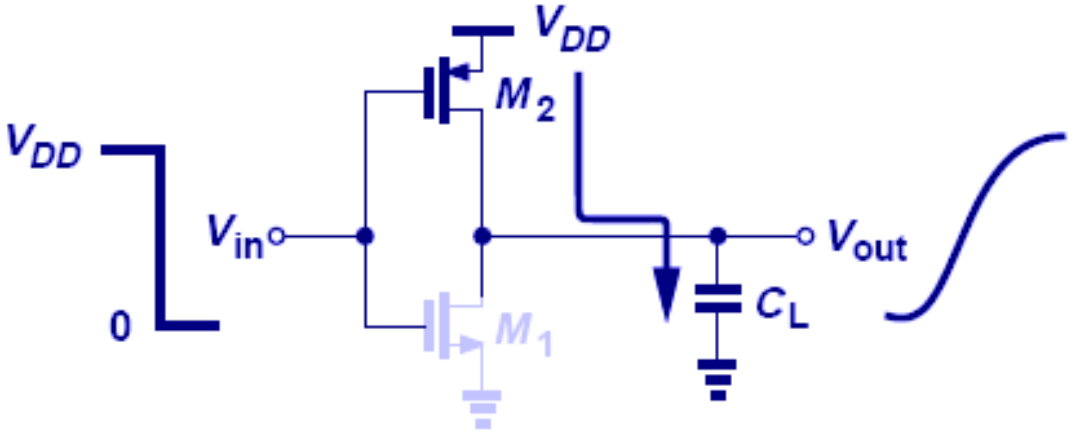


$$E_{stored} = \frac{1}{2} C_L V_{DD}^2$$

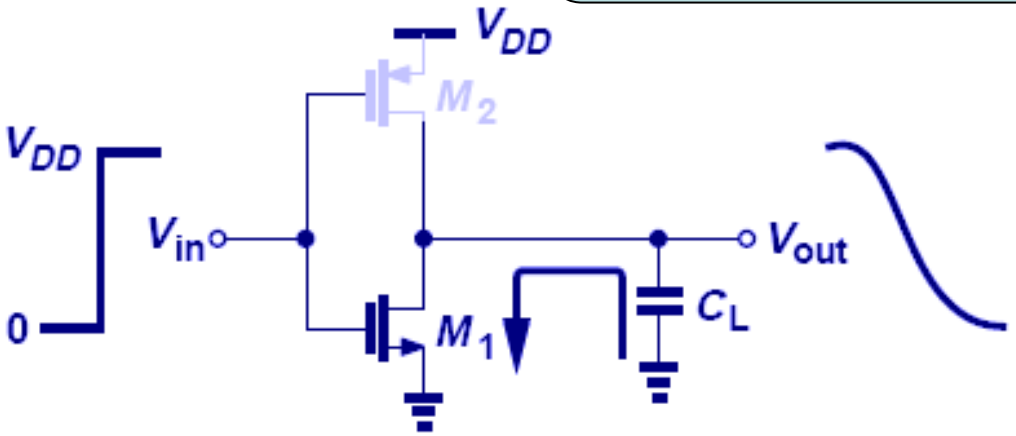
$$E_{dissipated} = \frac{1}{2} C_L V_{DD}^2$$

$$E_{drawn} = C_L V_{DD}^2$$

Power Delay Product

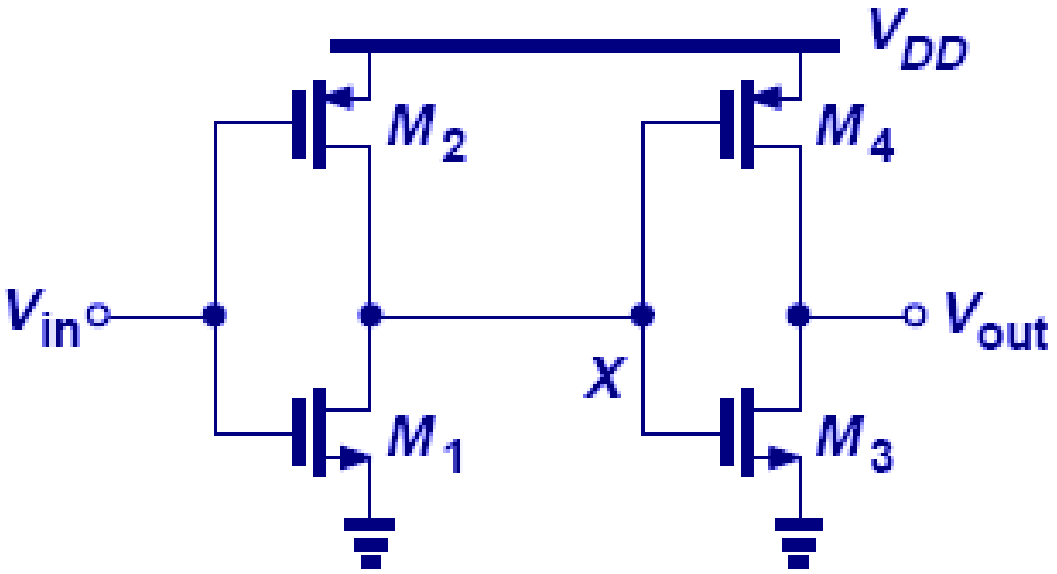


$$PDP = \frac{f_{in} C_L^2 V_{DD}^2}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1 \left[V_{DD} - |V_{TH1}|\right]} \left[\frac{2|V_{TH1}|}{V_{DD} - V_{TH1}} + \ln\left(3 - 4\frac{V_{TH1}}{V_{DD}}\right)\right]$$



$\mathbf{R_{on1}=R_{on2}}$

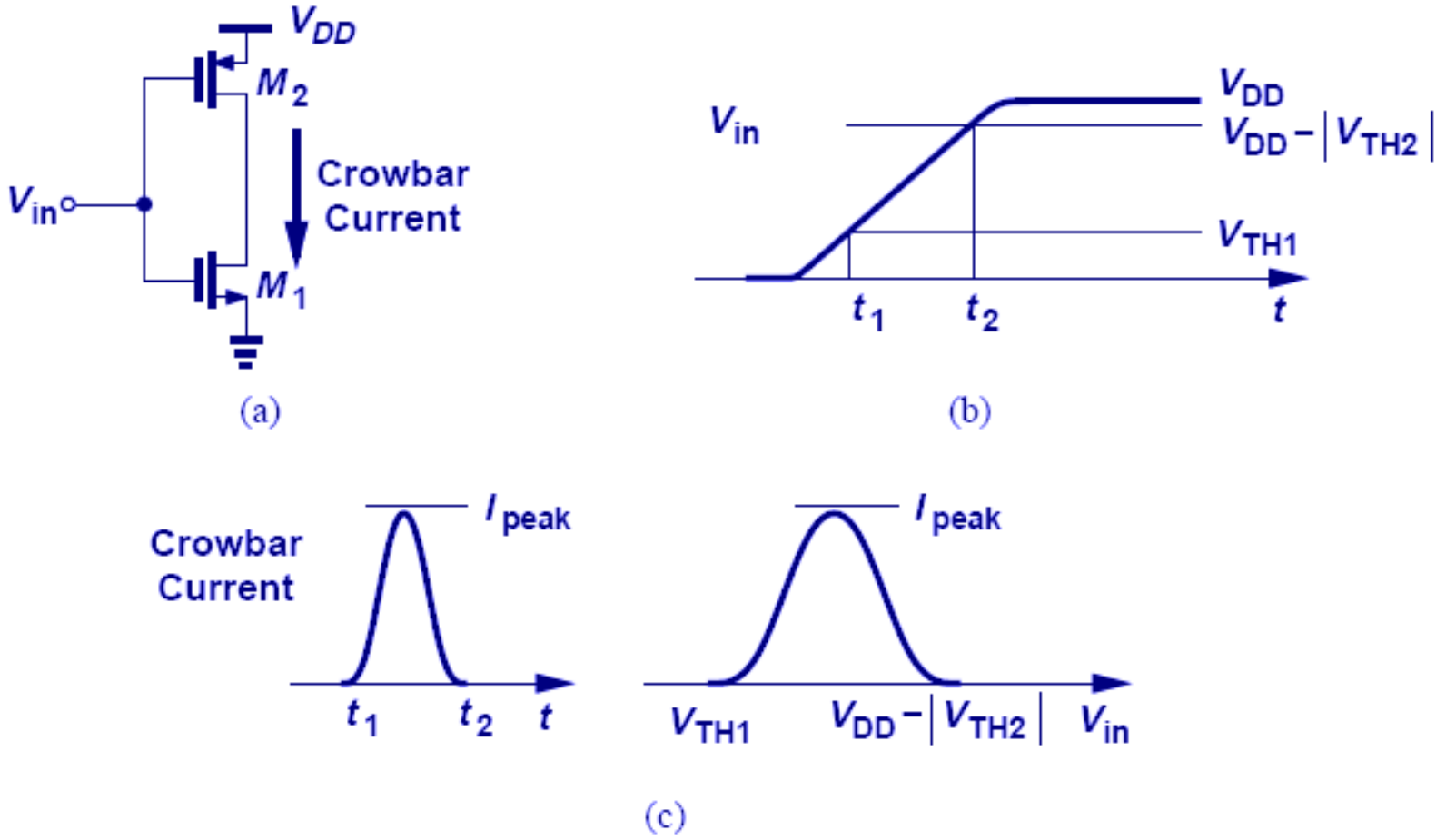
Example: PDP



$$R_{on} \approx \frac{4}{3} \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) V_{DD}}$$

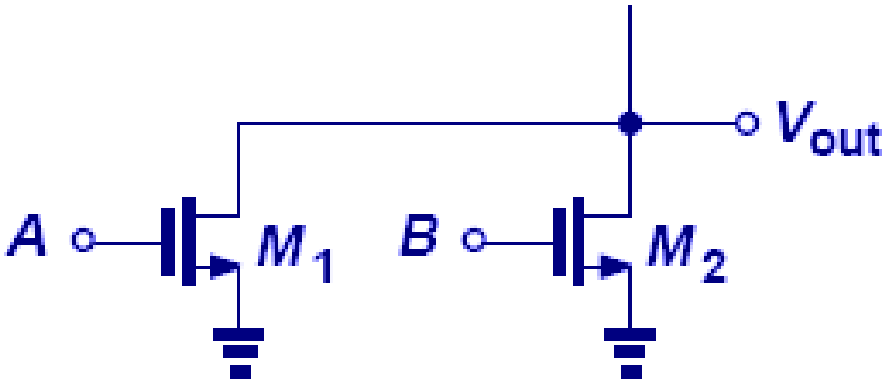
$$PDP = \frac{7.25 W L^2 C_{ox} f_{in} V_{DD}^2}{\mu_n}$$

Crowbar Current



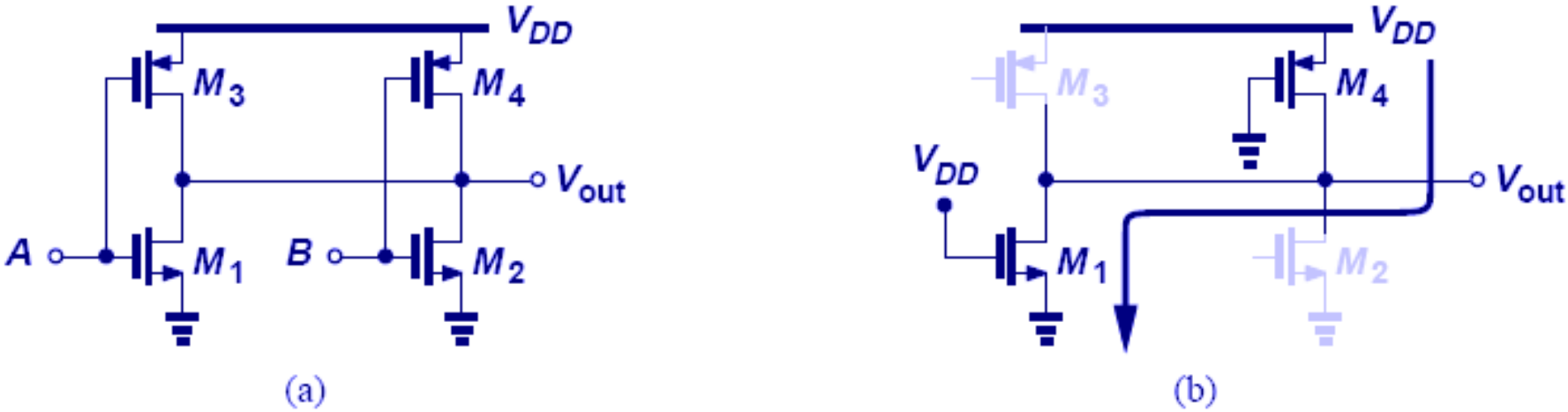
- When V_{in} is between V_{TH1} and V_{DD}-$|V_{TH2}|$, both M_1 and M_2 are on and there will be a current flowing from supply to ground.

NMOS Section of NOR



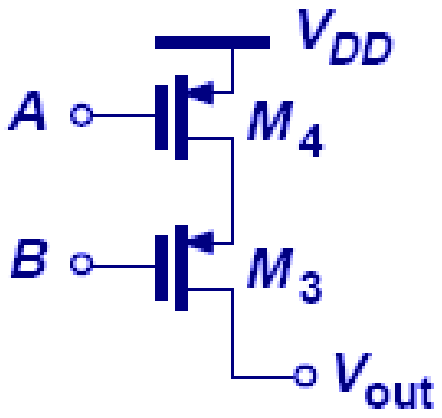
- **When either A or B is high or if both A and B are high, the output will be low. Transistors operate as pull-down devices.**

Example: Poor NOR



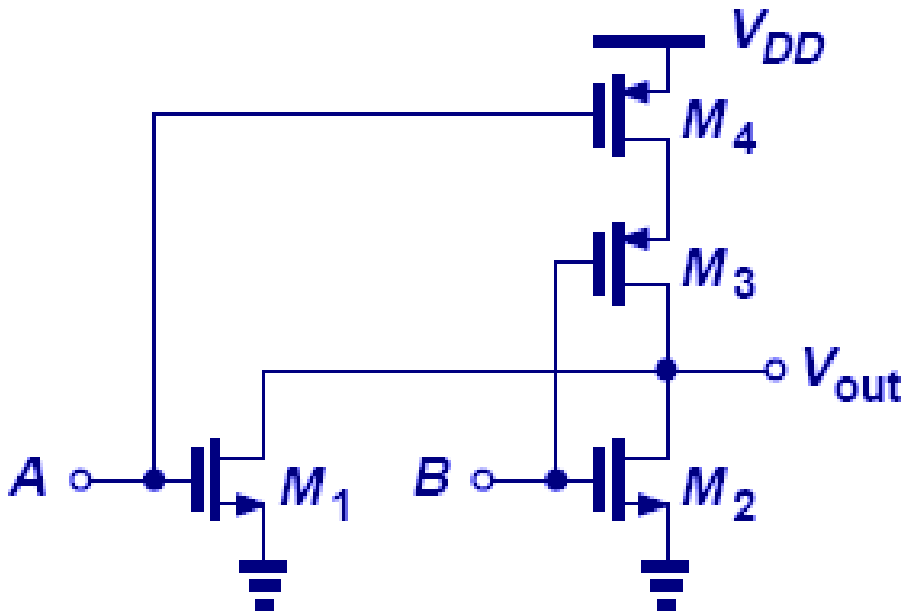
- **The above circuit fails to act as a NOR because when A is high and B is low, both M_4 and M_1 are on and produces an ill-defined low.**

PMOS Section of NOR



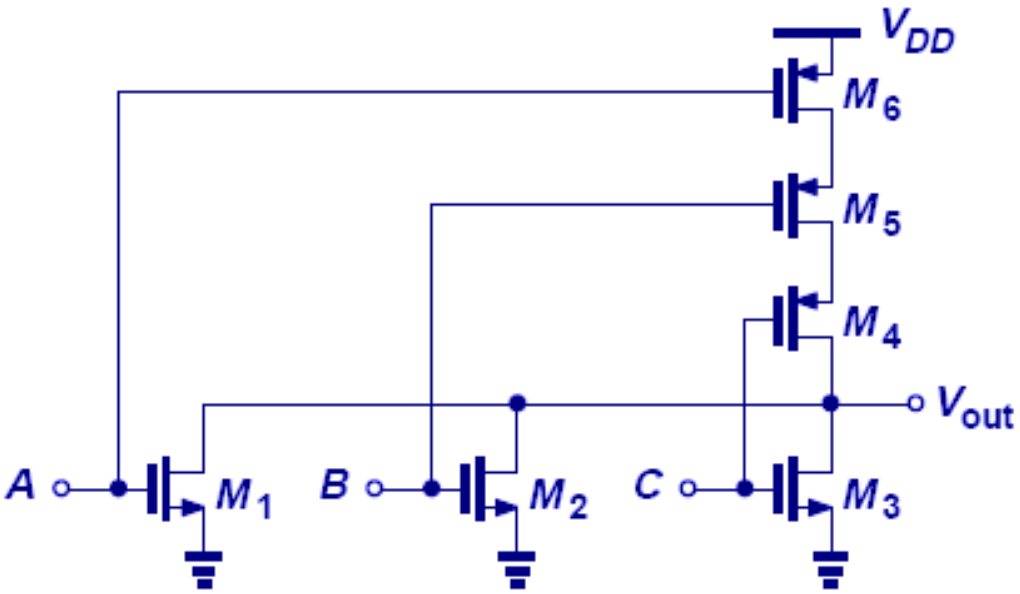
- **When both A and B are low, the output is high. Transistors operate as pull-up devices.**

CMOS NOR



- **Combing the NMOS and PMOS NOR sections, we have the CMOS NOR.**

Example: Three-Input NOR



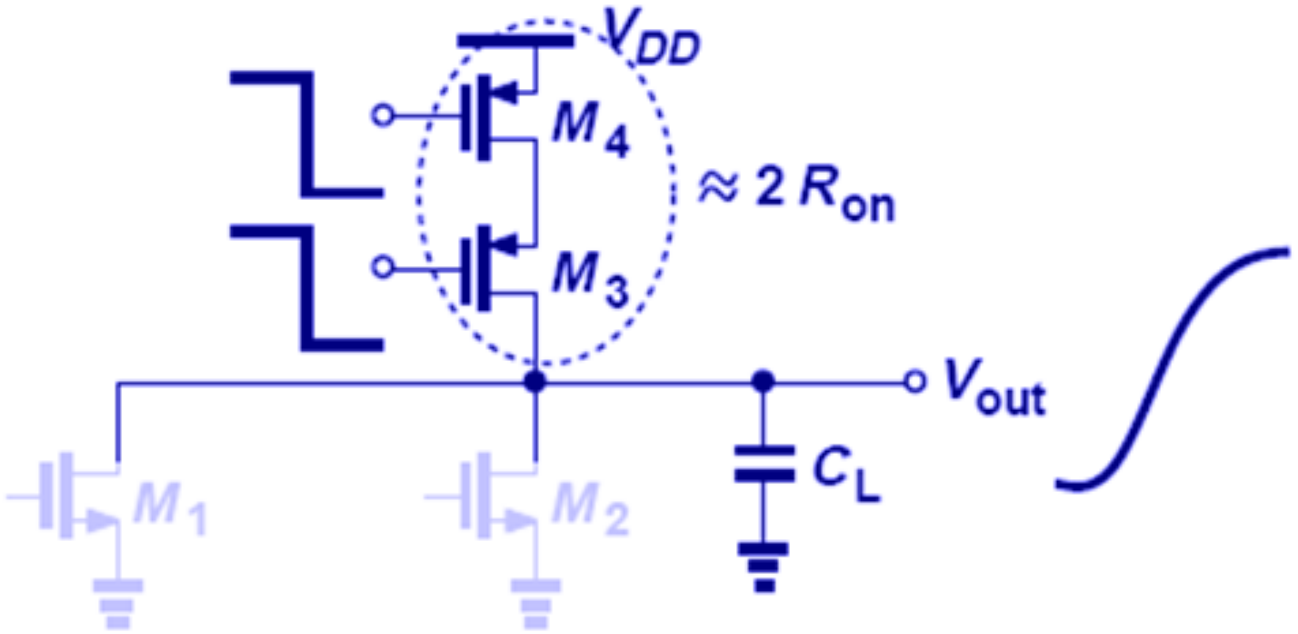
$$V_{out} = \left(A + B + C \right)'$$

Equal Rise & Fall ($\mu_n \approx 2\mu_p$)

$W_1=W_2=W_3=W$

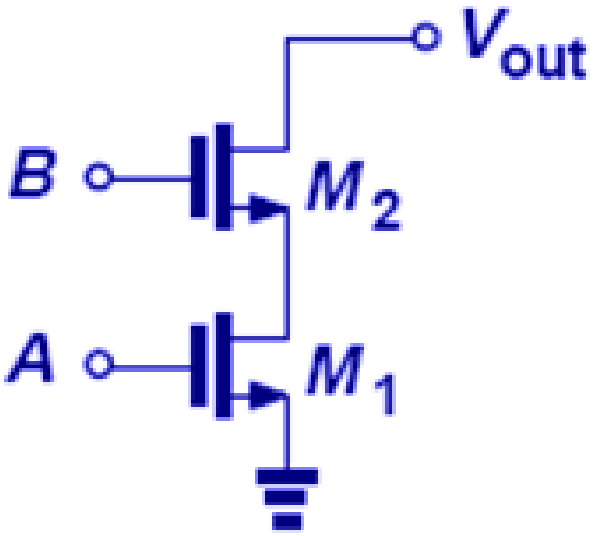
$W_4=W_5=W_6=6W$

Drawback of CMOS NOR



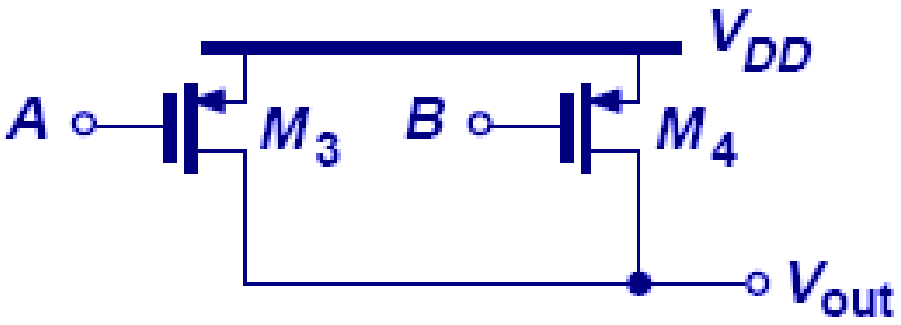
- Due to low PMOS mobility, series combination of M_3 and M_4 suffers from a high resistance, producing a long delay.
- The widths of the PMOS transistors can be increased to counter the high resistance, however this would load the preceding stage and the overall delay of the system may not improve.

NMOS NAND Section



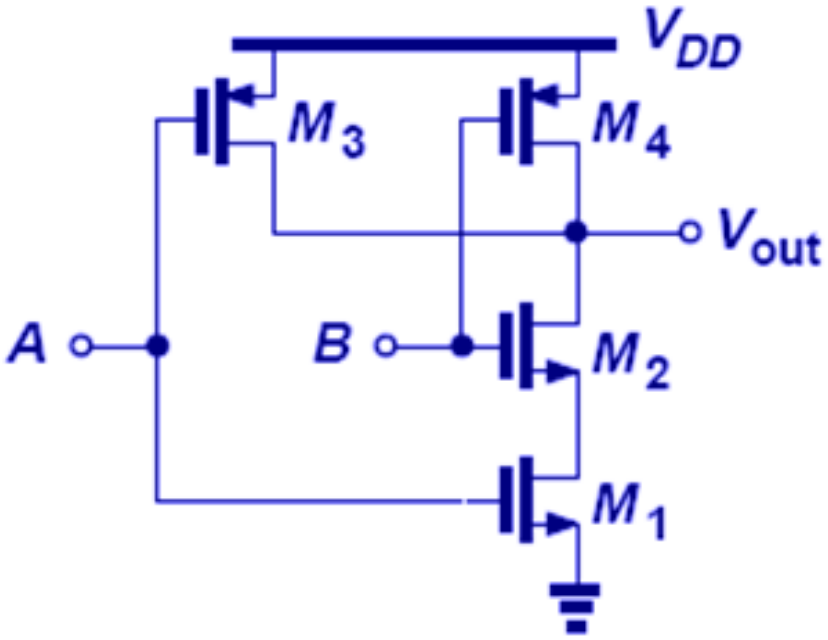
- **When both A and B are high, the output is low.**

PMOS NOR Section



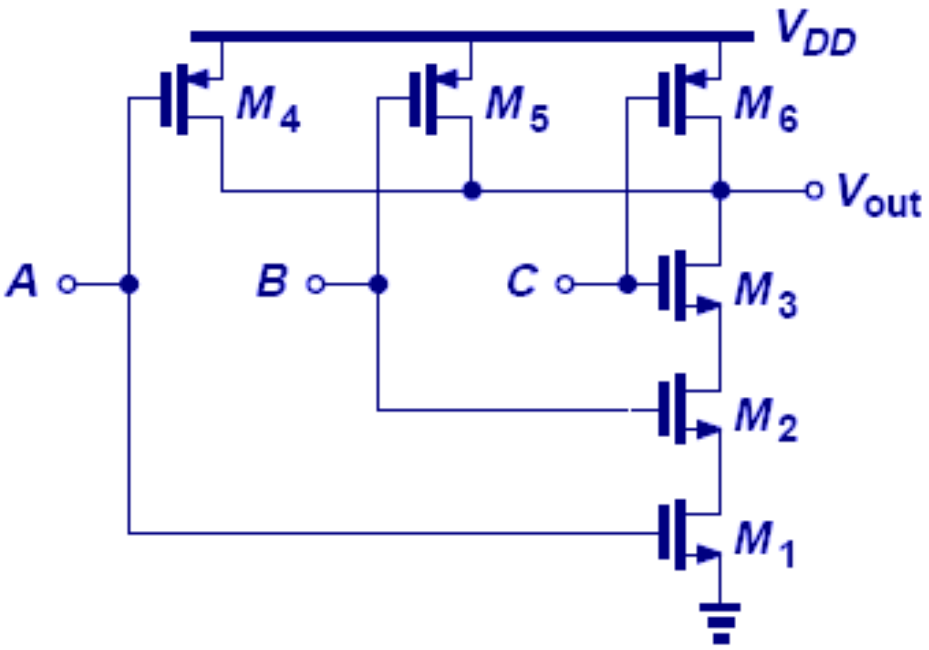
- **When either A or B is low or if both A and B are low, the output is high.**

CMOS NAND



- **Just like the CMOS NOR, the CMOS NAND can be implemented by combining its respective NMOS and PMOS sections, however it has better performance because its PMOS transistors are not in series.**

Example: Three-Input NAND

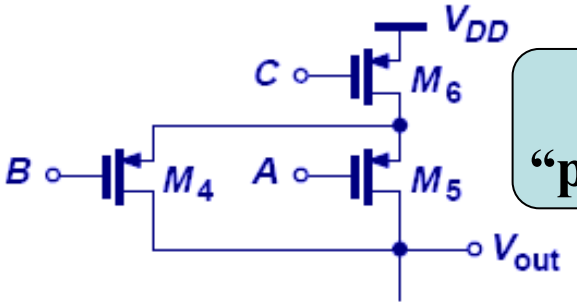


$$V_{out} = (ABC)'$$

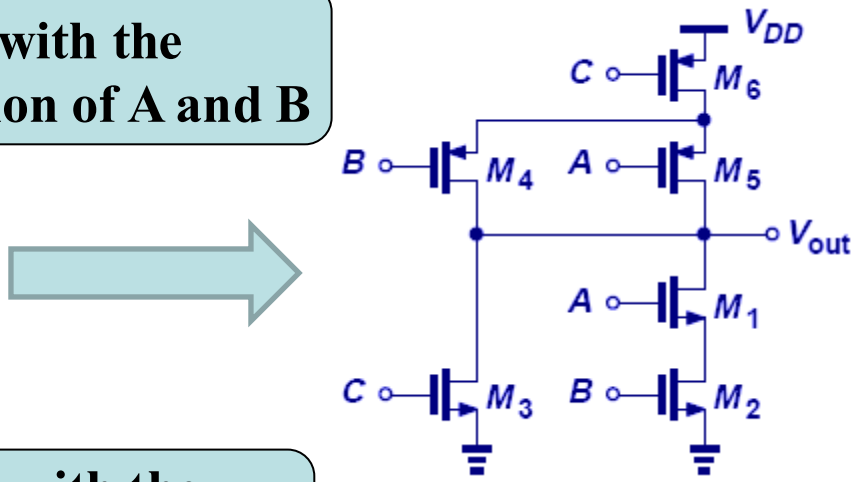
Equal Rise & Fall ($\mu_n \approx 2\mu_p$)

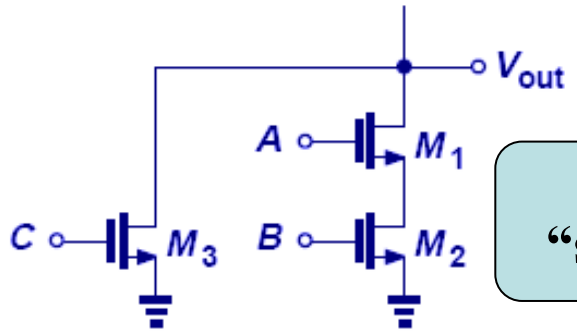
$W_1=W_2=W_3=3W$
$W_4=W_5=W_6=2W$

NMOS and PMOS Duality



C is in "series" with the "parallel" combination of A and B





C is in "parallel" with the "series" combination of A and B

- **In the CMOS philosophy, the PMOS section can be obtained from the NMOS section by converting series combinations to the parallel combinations and vice versa.**