THE UNIVERSITY OF DANANG
UNIVERSITY OF SCIENCE AND TECHNOLOGY
Faculty of Advanced Science and Technology

LABORATORY REPORT

Mixed-Signal Circuit Design

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Class : 21ECE

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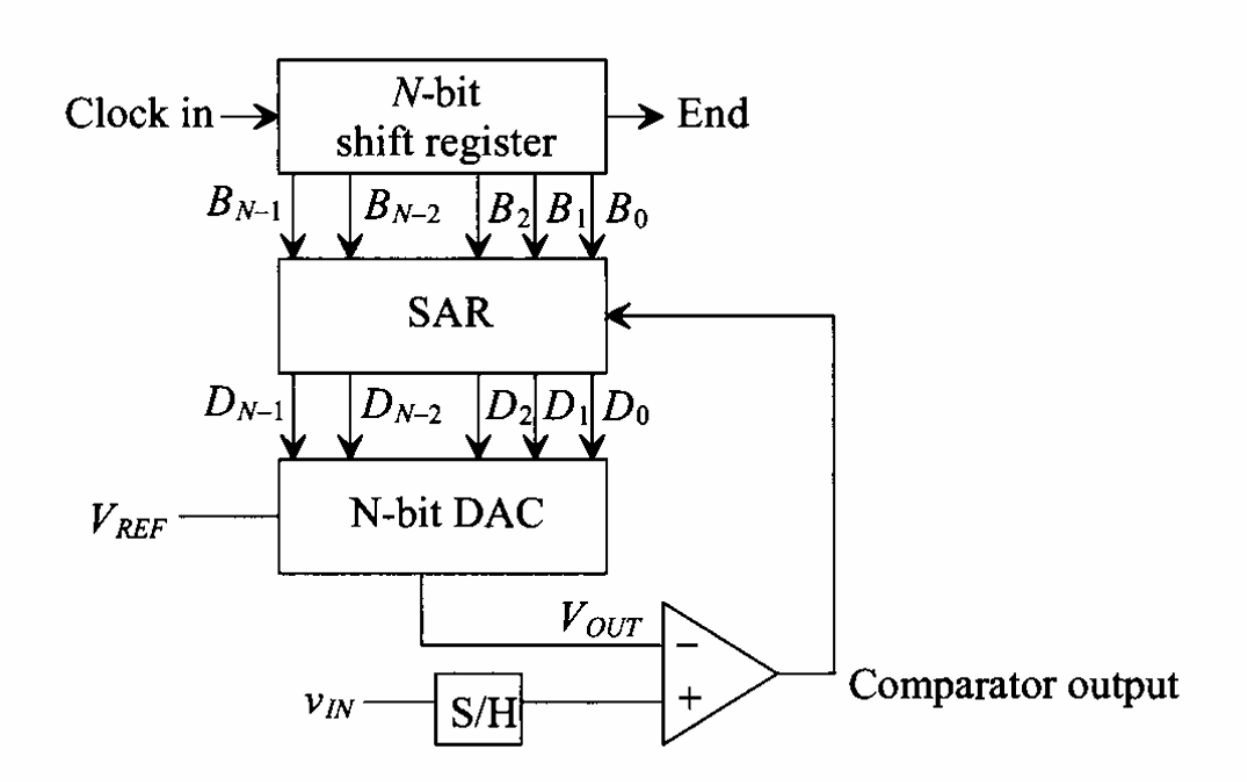
The Successive Approximation ADC

A successive approximation ADC determines the digital output by performing a binary search through all possible quantization levels until it reaches the final value. The converter uses an N-bit register, synchronized by a clock, to control the conversion process. The sampled input voltage $v_{IN}$is compared with the output of a DAC, and the comparator directs the SAR (Successive Approximation Register) to adjust the trial code.



The conversion procedure is as follows:

1. A logic 1 is loaded into the highest bit position of the shift register. For the first comparison, $B_{N-1} = 1$and all lower bits $B_k = 0$.
2. The MSB of the SAR, D_{N-1}, is initially set to 1, with all remaining SAR bits set to 0. Under this condition, the DAC produces an output equal to $\frac{V_{REF}}{2}$.
3. The input $v_{IN}$is compared to $\frac{V_{REF}}{2}$:
    - If $v_{IN} < \frac{V_{REF}}{2}$, the comparator output resets $D_{N-1} = 0$.
    - If $v_{IN} \geq \frac{V_{REF}}{2}$, D_{N-1}remains set to 1.
      This value becomes the MSB of the final digital result.

4. The original 1 in the shift register is shifted one position to the right so that $B_{N-2} = 1$, with all lower bits still at 0.

5. $D_{N-2}$is set to 1, while D_{N-3}through D_0remain 0, and D_{N-1}keeps the value determined from the previous step. The DAC now outputs either:

   - $\frac{V_{REF}}{4}$if $D_{N-1} = 0$, or
   - $\frac{3V_{REF}}{4}$if $D_{N-1} = 1$.

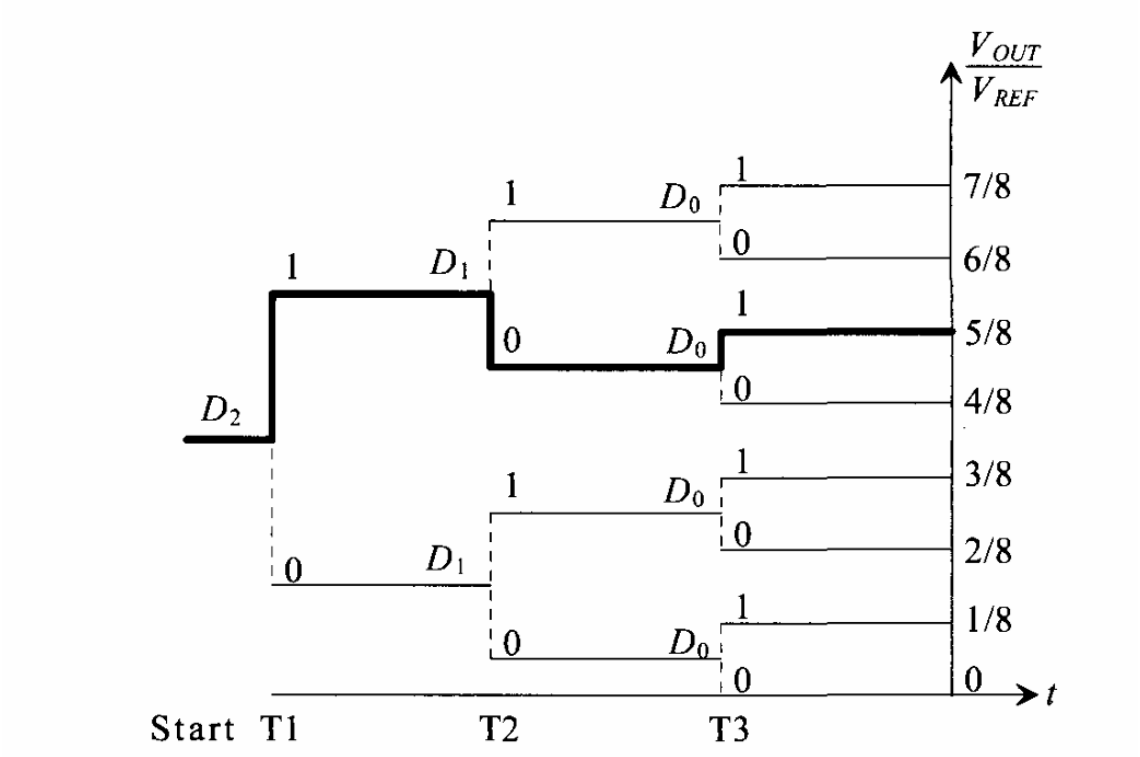
6. The comparator compares $v_{IN}$with this new DAC output:

   - If the DAC output is greater than v_{IN}, $D_{N-2}$is set to 0.
   - If the DAC output is less than or equal to v_{IN}, D_{N-2}remains 1.

7. This procedure continues bit by bit. Each comparison refines the digital value by determining whether the trial DAC output is above or below v_{IN}.

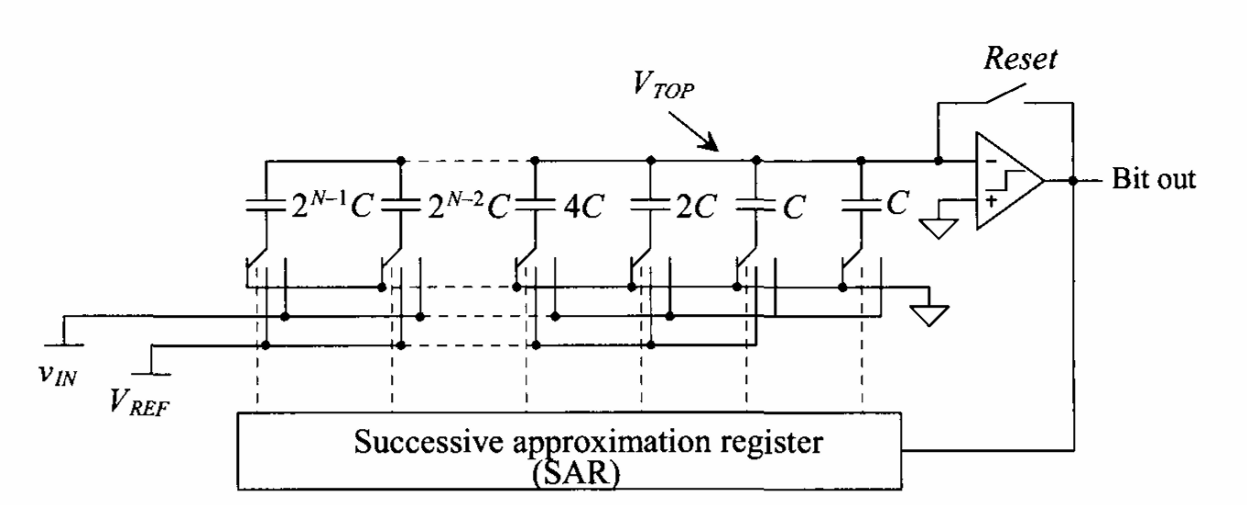
8. After all N bits have been tested, the DAC output converges to the value of v_{IN}within the resolution of the ADC, and the SAR holds the final digital code.

Here is the binary search performed by a 3-bit successive approximation ADC for D=101.



The Charge-Redistribution Successive Approximation ADC

One of the most popular types of successive approximation architectures uses the binary weighted capacitor array called a charge-redistribution successive-approximation ADC, this converter samples the input signal and then performs the binary search based on the amount of charge on each of the DAC capacitors. Figure shows N-bit architecture. A comparator has replaced the unity gain buffer used in the DAC architecture. The binary-weighted capacitor array also samples the input voltage, so no external sample-and-hold is needed.



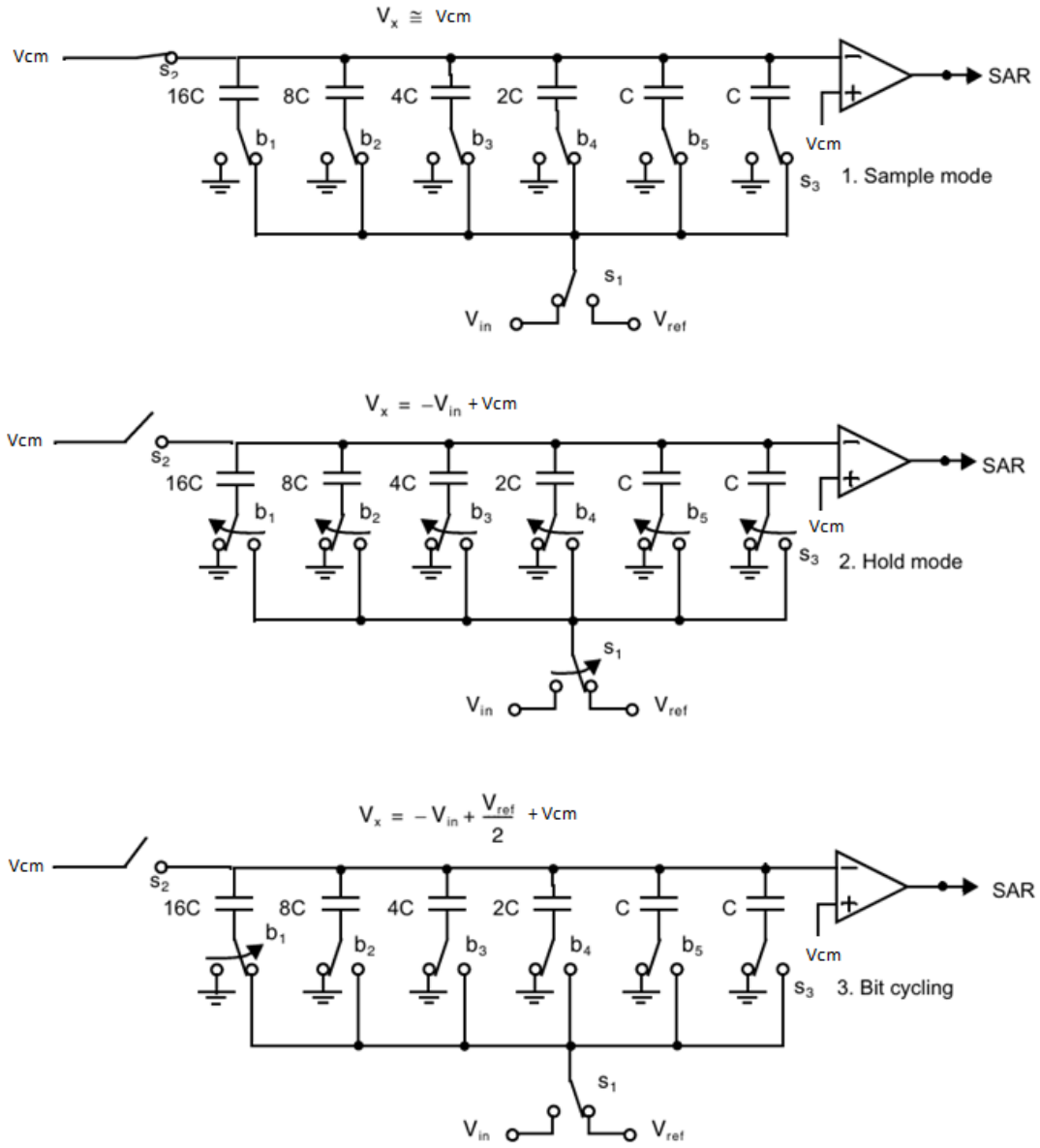
SAR ADC Algorithm

The straightforward approach of using a separate D/A converter and setting it equal to the input voltage (within one LSB) can be modified to the flow graph shown. Here, the error signal equals the difference between the input signal, , and the D/A output, . As a result, is always compared to common voltage (Vcm), as seen at the top of the flow graph, and the goal is to set this error difference within one LSB of zero. One of the first switched-capacitor analog systems using this approach is a charge-redistribution MOS A/D converter. With such a converter, the sample and hold, D/A converter, and the difference portion of the comparator are all combined into a single circuit. The unipolar case is shown and operates as follows:

1. Sample mode: In the first step, all the capacitors are charged to while the comparator is being reset to its threshold voltage through , In this step, note that the capacitor array is performing the sample-and hold operation.

2. Hold mode: Next, the comparator is taken out of reset by opening , and then all the capacitors are switched to ground. This causes , which was originally zero, to change to , thereby holding the input signal, , on the capacitor array. (This step is sometimes merged with the first bit time during bit cycling.) Finally, is switched so that can be applied to the capacitor array during bit cycling.

3. Bit cycling: Next, the largest capacitor (i.e., the capacitor in this example) is switched to . now goes to . If is negative, then is greater than , and the MSB capacitor is left connected to . Also is considered to be a 1. Otherwise, the MSB capacitor is reconnected to ground and is taken to be 0. This process is repeated times, with a smaller capacitor being switched each time, until the conversion is finished. To get an exact division by two, note that an additional unit capacitor of size has been added so that the total capacitance is rather than . Also, the capacitor bottom plates should be connected to the side, not to the comparator side, to minimize the parasitic capacitance at node . Although parasitic capacitance at does not cause any conver sion errors with an ideal comparator, it does attenuate the voltage . A signed A/D conversion can be realized by adding a input. If is less than zero at the first step, then proceed as in the unipolar case using . Otherwise, if is greater than zero, use and test for greater than zero when deciding whether to leave the capacitors connected to or not at each bit cycling.



After sampling, the switch connected to the input opens, and the bottom plates of all capacitors in the array are driven to ground. This causes the voltage at the top plate to become $V_{cm} - V_{IN}$.

The conversion starts by switching the bottom plate of the MSB capacitor to V_{REF}. If the comparator output is high, the MSB capacitor stays connected to V_{REF}. If the comparator output is low, the MSB capacitor is reconnected to ground. The comparator output at this step is the MSB, D_{N-1}.

The resulting top-plate voltage after the MSB decision is

$$V_X = V_{CM} - v_{IN} + D_{N-1} \cdot \frac{V_{REF}}{2}$$

The next largest capacitor is processed in the same way. After switching the second capacitor, the new top-plate voltage becomes

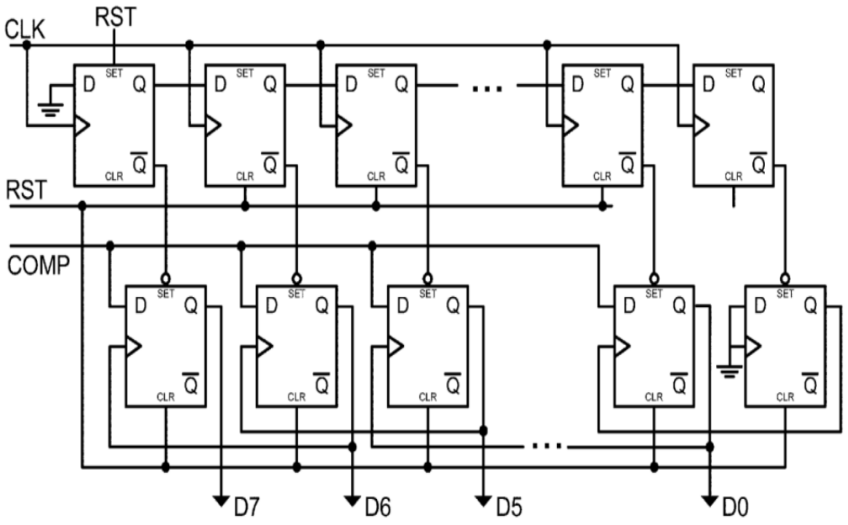
$$V_X = V_{CM} - v_{IN} + D_{N-1} \cdot \frac{V_{REF}}{2} + D_{N-2} \cdot \frac{V_{REF}}{4}$$

The conversion process continues with the remaining capacitors so that the voltage on the top plate of the array, Vx, converges to the value of the ground (within the resolution of the converter)

$$V_X = V_{CM} - v_{IN} + D_{N-1} \cdot \frac{V_{REF}}{2} + D_{N-2} \cdot \frac{V_{REF}}{4} + \cdots + D_0 \cdot \frac{V_{REF}}{2^N} \approx V_{CM}$$

SAR Control Logic

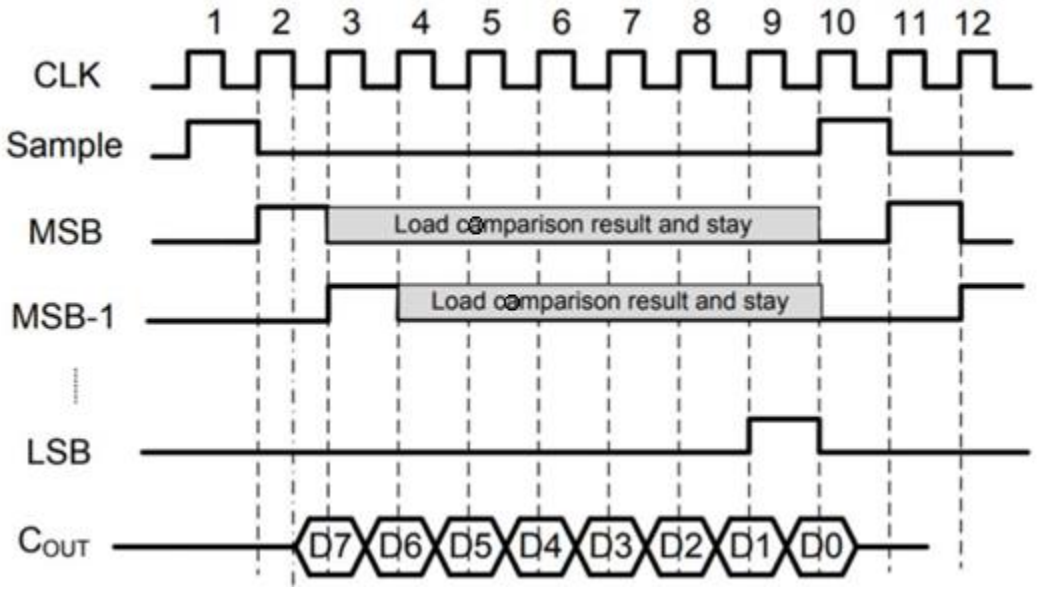
The simple direct realization of the SAR logic control, using 2(N + 1) D-flipflops Where N is the ADC resolution. All the D-flipflops input connected to ’0’ and its SET port to the RST signal while the RESET port is unconnected. The Lower flipflops SET ports are connected to the complementary outputs of the Upper flipflops after inversion with the clock port of each of them connected to the output of the next stage. The initial state all the outputs and the digital control bits is ’0’.



With the RST signal arriving all the D-flipflops are still in the reset phase with output ’0’, except for the first D-flipflop where the RST signal is connected to its SET port. The output Q of the first D-flipflop is set then to ’1’ and its complementary output is set to ’0’ setting the first lower D-FlipFlop output D0 to ’1’ not caring for the comparator output, this is the operation of connecting the largest DAC capacitor to *Vref*. At the next clock, RST signal returns low, the First upper D-flipflop changes output to ’0’ and the ’1’ spreads to the output of the second upper D-flipflop setting the second lower flipflop and D1 to ’1’ (next largest capacitor is connected to *Vref*.

	DAC outputs								C
0	0	0	0	0	0	0	0	0	X
1	1	0	0	0	0	0	0	0	a8
2	a8	1	0	0	0	0	0	0	a7
3	a8	a7	1	0	0	0	0	0	a6
4	a8	a7	a6	1	0	0	0	0	a5
5	a8	a7	a6	a5	1	0	0	0	a4
6	a8	a7	a6	a5	a4	1	0	0	a3
7	a8	a7	a6	a5	a4	a3	1	0	a2
8	a8	a7	a6	a5	a4	a3	a2	1	a1

At this step the first lower flipflop has ended the SET phase and the first comparison also has ended. The action of setting D1 to '1' will trigger the first Lower flipflop to check the comparator output connected to its D terminal. According to the comparator output, D0 is kept '1' if the comparator output is '1' or changes to '0' if the comparator output is '0'. No more change will happen to D0 till end of conversion since its only triggered by the rising edge on D1. The operation then continues till all digits are ready and at the next RST signal, the digital output is read and stored and all D-flipflops are reset again.



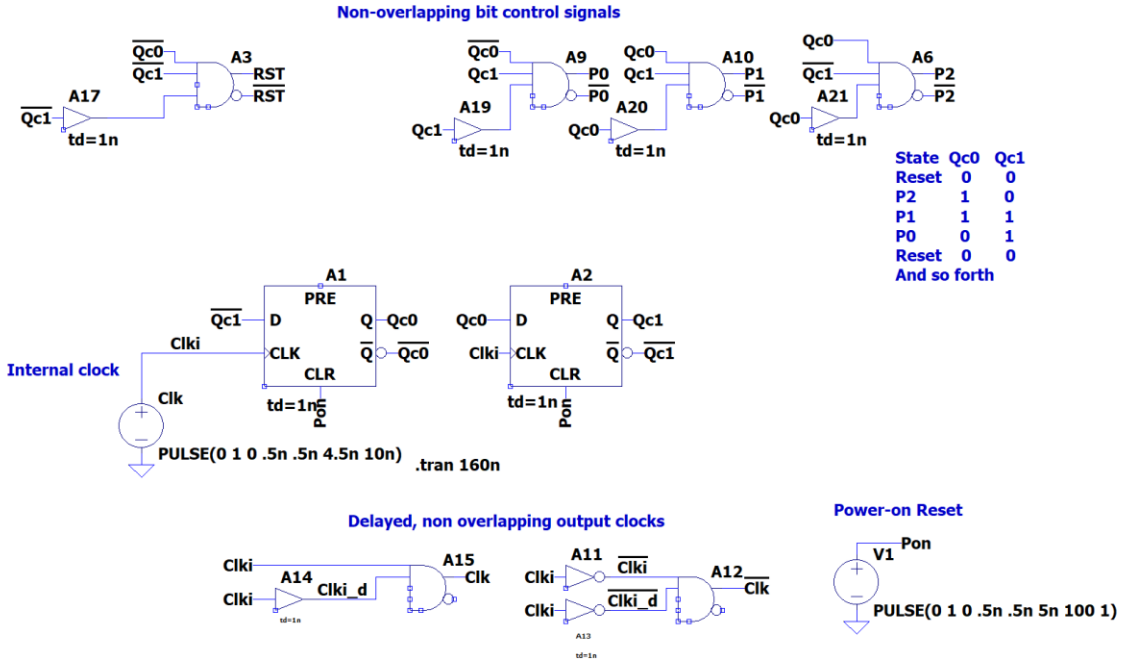
Simulation Results and Analysis

The primary objective of this laboratory is to design and simulate a 3-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). This project involves implementing the core components, including a binary-weighted capacitor array, a comparator, and the SAR control logic. The simulation aims to verify the "bit cycling" conversion process and analyze the final ADC transfer curve to confirm correct 3-bit quantization.

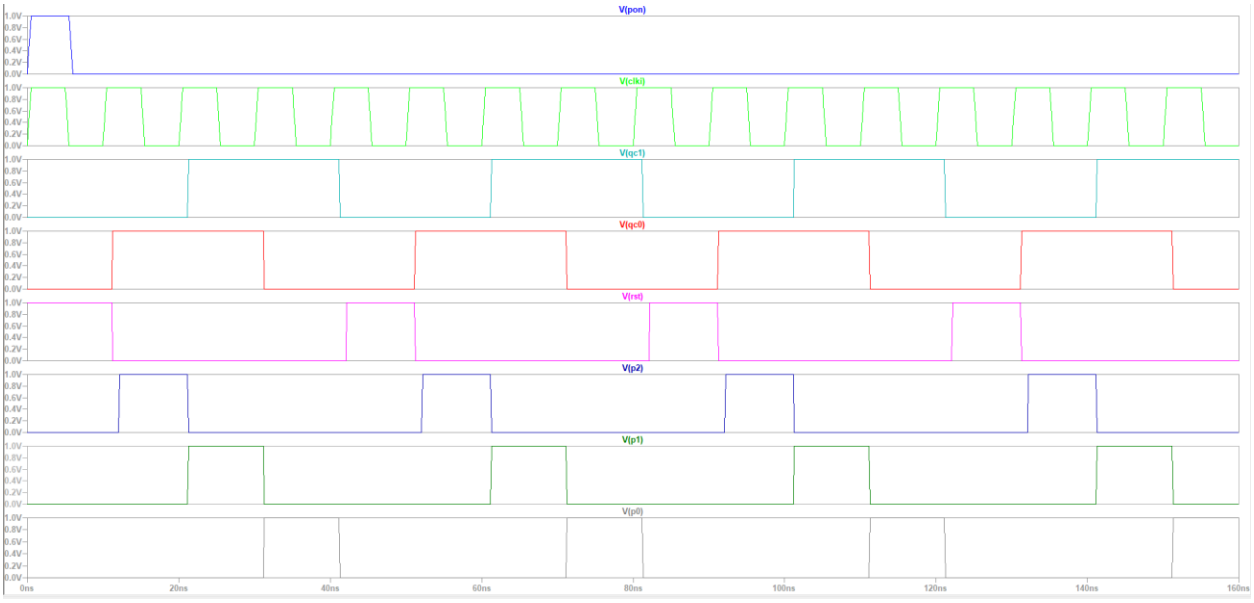
The 3-bit SAR ADC and its control logic were simulated to verify correct operation. The results are presented below.

1. SAR Control Logic and Timing

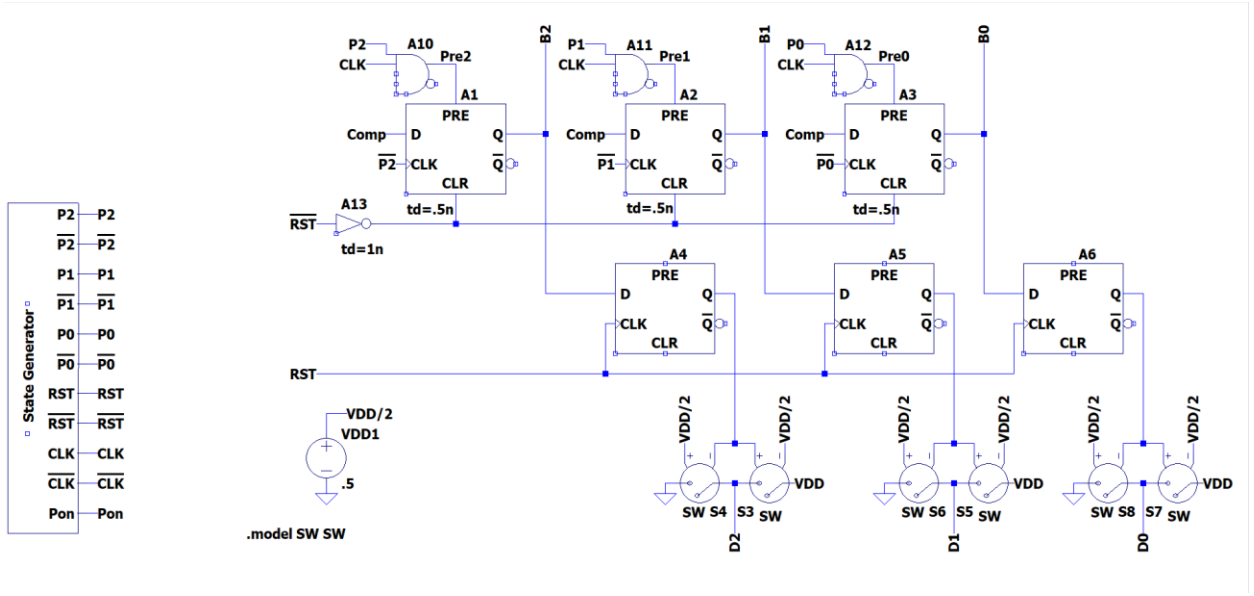
The SAR control logic is responsible for generating the non-overlapping clock signals that manage the three phases of operation: Sample, Hold, and Bit Cycling. The simulation results for the state generator are shown in the plot.



The "Internal clock" (V(clki)) drives a series of D-flipflops to generate delayed, non-overlapping outputs V(p0), V(p1), and V(p2). These signals correspond to the different states required for conversion, as outlined in the timing diagram. The V(rst) signal is used to initialize the conversion cycle. This simulation confirms the logic is functioning as required to step through the conversion process.



2. Internal Conversion Waveforms

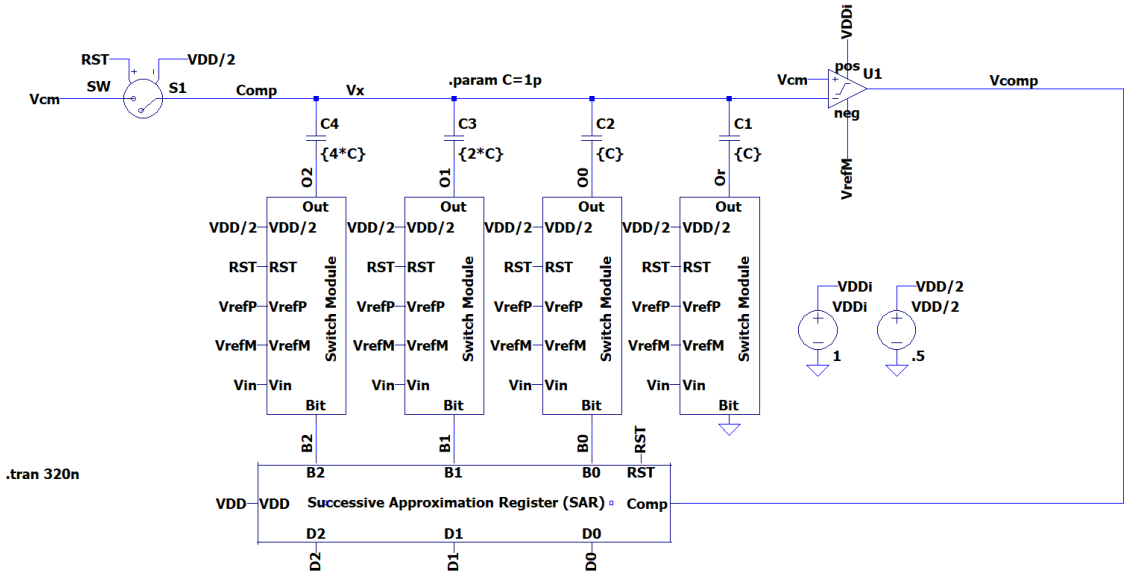


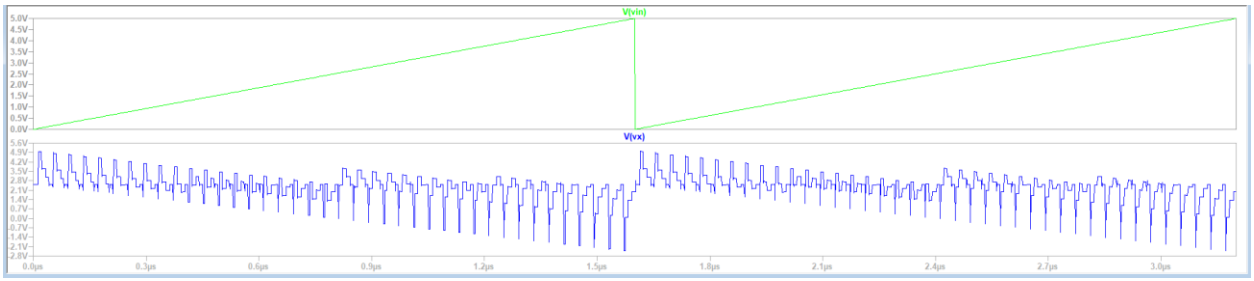
The plot shows the key internal voltages during several conversion cycles for a given input V(in).

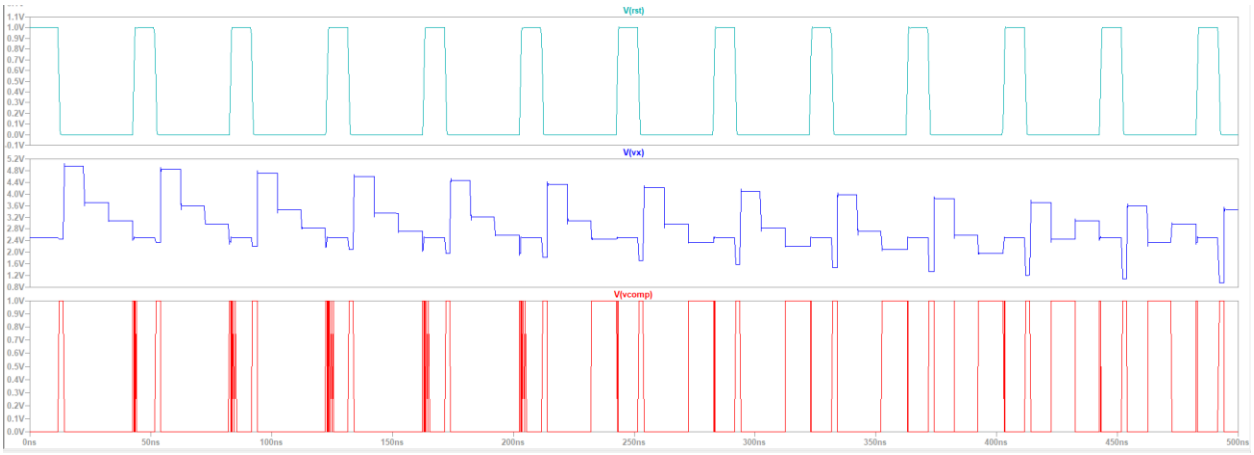
- **V(vx):** This is the voltage at the top plate of the capacitor array. As described in the theory, this voltage starts at Vin during the hold phase and then converges towards 0V (ground) with each successive bit test. The "staircase" shape of V(vx) clearly shows the charge redistribution as the DAC output is refined.
- **V(comp):** This is the output of the comparator. At each bit-cycling step, the comparator output goes high or low, determining the value of that bit (D2, D1, or D0).

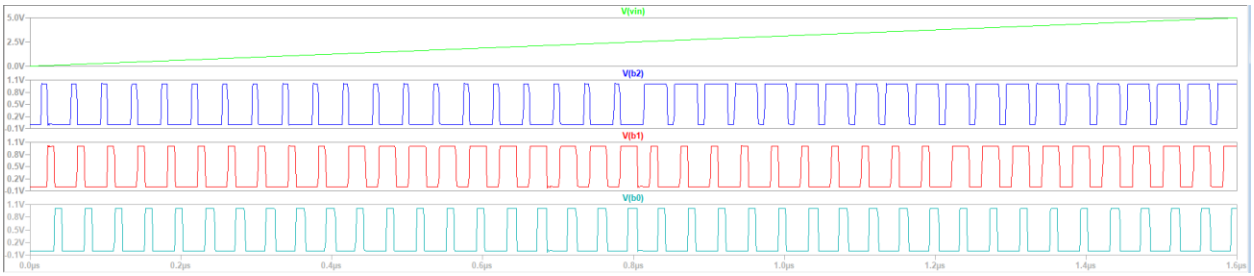
- **V(d2), V(d1), V(d0):** These are the digital outputs from the SAR logic. Their final values are set by the comparator output at the end of each bit test.

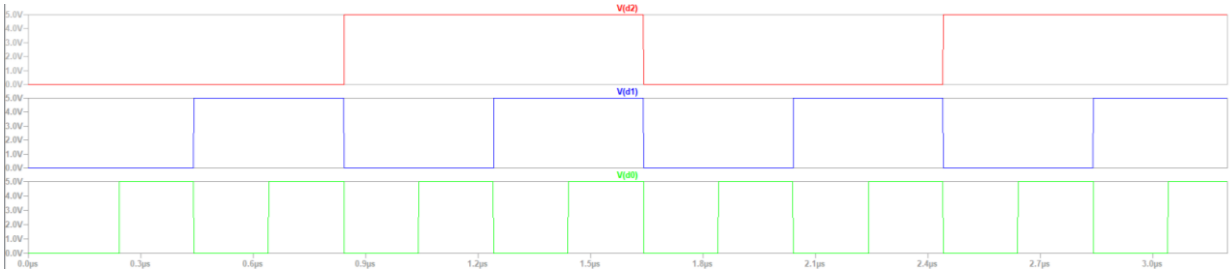
This plot successfully demonstrates the binary search algorithm in action. The V(vx) voltage is successively refined until it is approximately zero, at which point the SAR holds the correct digital code.











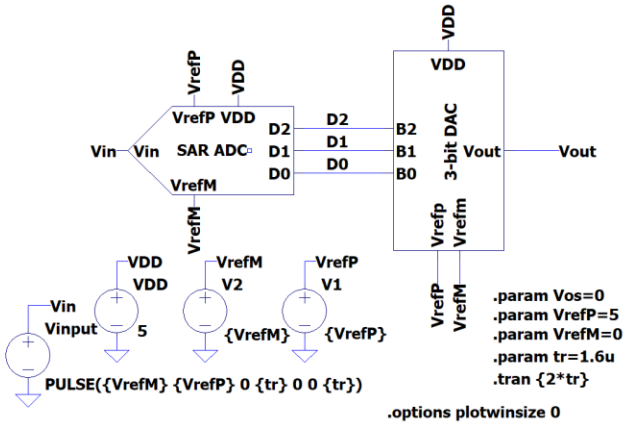
3. ADC Transfer Curve

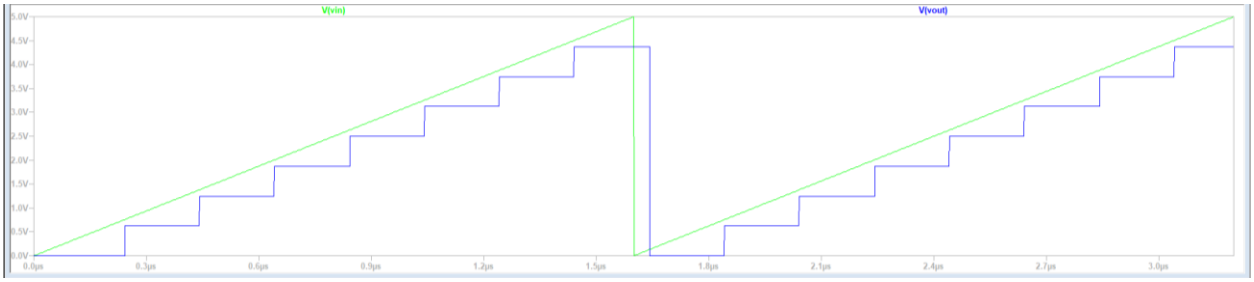
The final simulation tests the complete 3-bit SAR ADC by applying a slow-ramping analog input voltage (V(vin), green) and observing the output of an ideal 3-bit DAC (V(vout), blue) that is fed by the ADC's digital output.

The resulting plot shows the characteristic "staircase" transfer curve of an ADC.

- The **ramp** is the analog input, sweeping from 0V to 5V.
- The **output** is quantized.

As expected for a 3-bit converter, there are 2^3 = 8 distinct output levels. The output V(vout) holds its value as the input V(vin) ramps up, until V(vin) crosses the threshold for the next quantization level. This plot confirms the ADC is successfully converting the analog input into the correct 3-bit digital representation.





Conclusion

A 3-bit charge-redistribution Successive Approximation Register (SAR) ADC was successfully designed and simulated. The design was based on a binary-weighted capacitor array and D-flipflop-based control logic.

The simulation results verified all key aspects of the ADC's operation.

1. The SAR control logic correctly generated the non-overlapping clock signals required for the sample, hold, and bit-cycling phases.
2. Analysis of the internal node voltages confirmed the charge-redistribution binary search algorithm, showing the top-plate voltage V(vx) successfully converging to Vcm as each bit was determined.
3. The final ADC transfer curve demonstrated the correct 3-bit quantization of a ramp input, clearly showing the 8 distinct output levels.