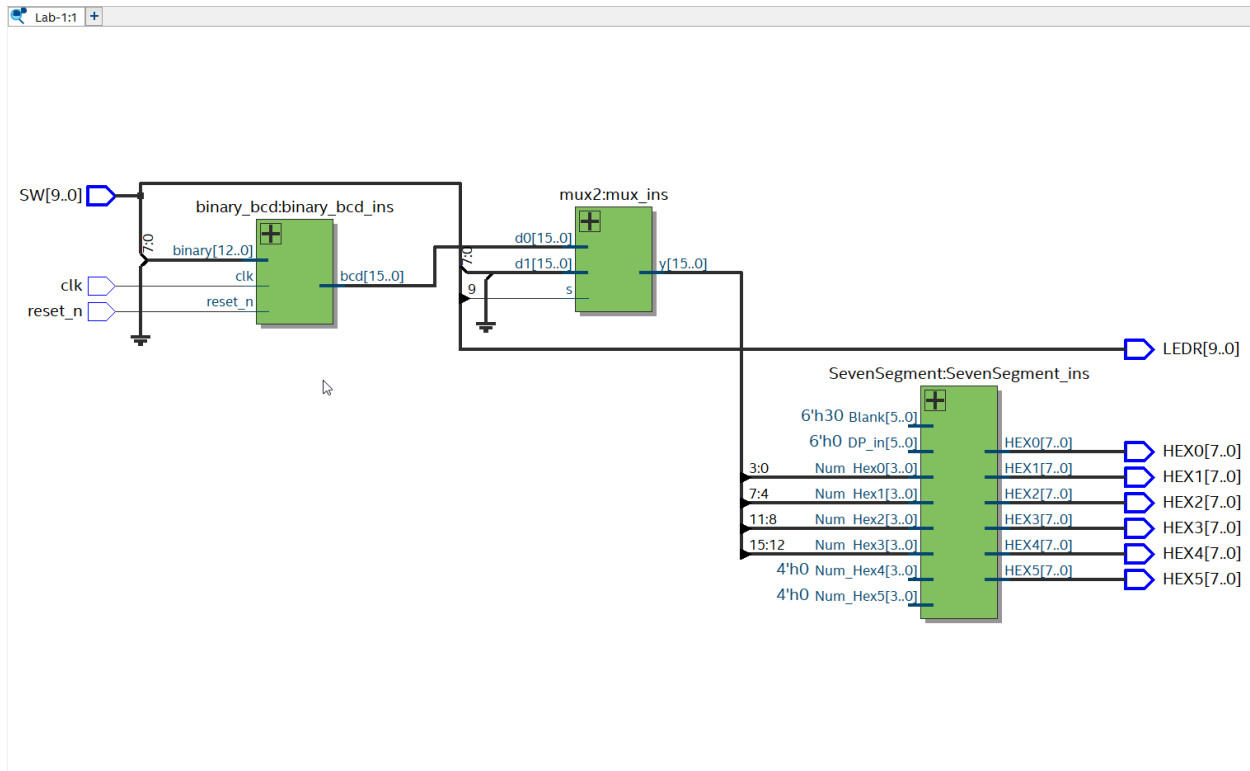


Group 48 Design Record

Ahmed Elmalawany, Andrew Glenwright, Jordan Lonneberg

October 10, 2020

RTL Schematic



Reports

No critical warnings or error messages were generated.

Type	ID	Message
Warning	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value.
Warning	13024	Output pins are stuck at VCC or GND.
Warning	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value.
Warning	292013	Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
Warning	15714	Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details.
Warning	332174	Ignored filter at Lab-1.sdc(9): ADC_CLK_10 could not be matched with a port.
Warning	332049	Ignored create_clock at Lab-1.sdc(9): Argument <targets> is an empty collection.
Warning	332174	Ignored filter at Lab-1.sdc(11): MAX10_CLK2_50 could not be matched with a port.
Warning	332049	Ignored create_clock at Lab-1.sdc(11): Argument <targets> is an empty collection.
Warning	15705	Ignored locations or region assignments to the following nodes:
Warning	171167	Found invalid Fitter assignments. See the Ignored Assignments panel in the Fitter Compilation Report for more information.
Warning	169177	12 pins must meet Intel FPGA requirements for 3.3-, 3.0-, and 2.5-V interfaces. For more information, refer to AN 447: Interfacing MAX 10 Devices with 3.3/3.0/2.5-V LVTT.
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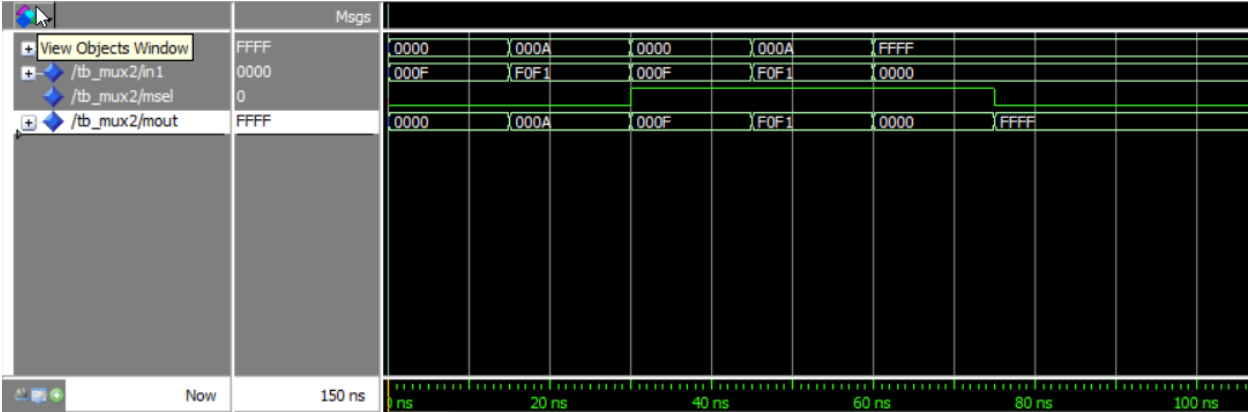
Slow 1200 mV Model Fmax

Slow 1200mV 85C Model Fmax Summary				
<<Filter>>				
	Fmax	Restricted Fmax	Clock Name	Note
1	126.33 MHz	126.33 MHz	clk	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges

Test Bench Results

tb_mux2 Test Bench Results



tb_top_level Test Bench Results

