Group 48 Design Record

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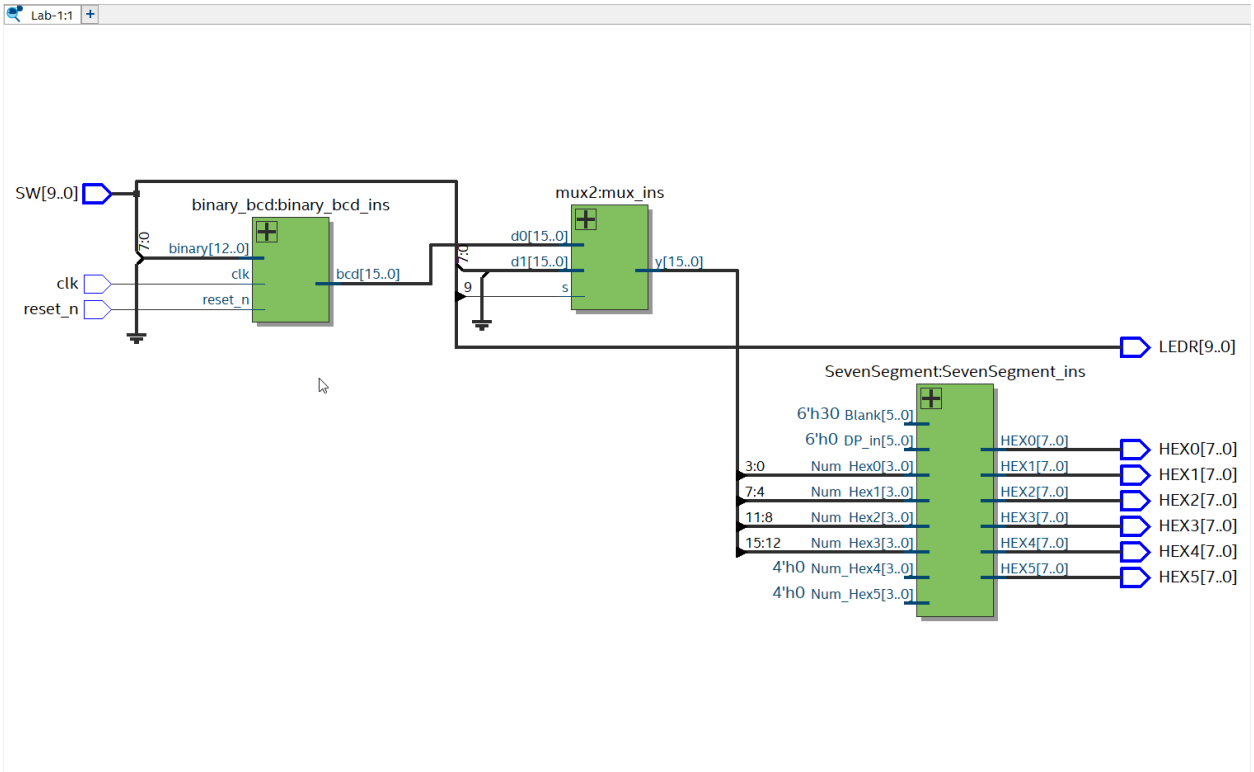
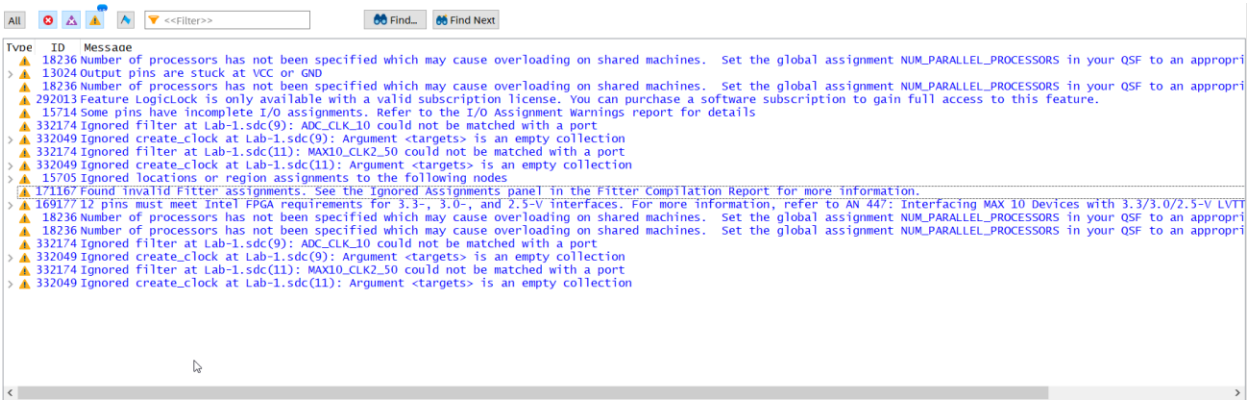
RTL Schematic



Reports

No critical warnings or error messages were generated.



Slow 1200 mV Model Fmax

Slow 1200mV 85C Model Fmax Summary

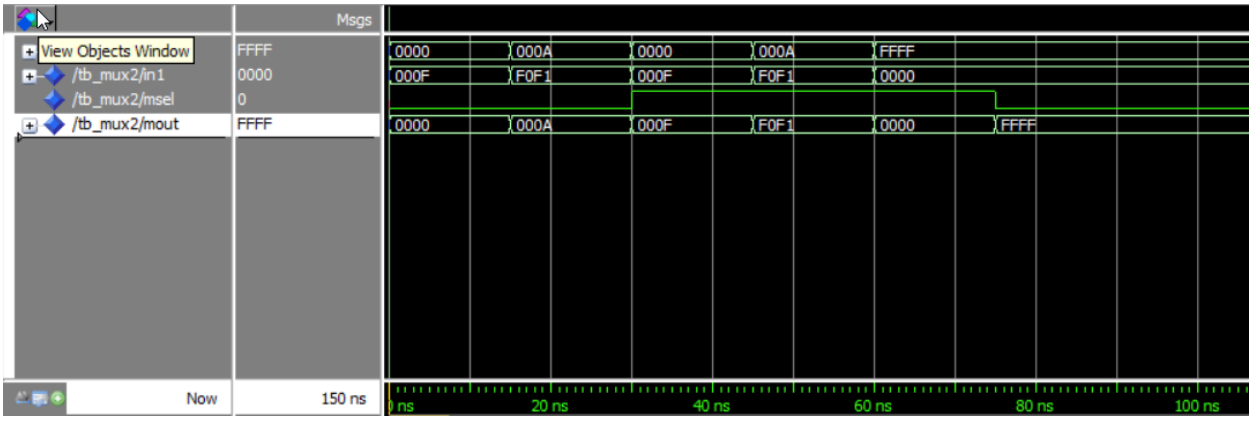
<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	126.33 MHz	126.33 MHz	clk	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges

Test Bench Results

tb_mux2 Test Bench Results



tb_top_level Test Bench Results