Harrison Doll

Madison, WI | hmrdo@protonmail.com | 262 490 9956 | github.com/hmrdo | linkedin.com/in/hmrdoll

Education

University of Wisconsin–Madison Sept 2021 – May 2025

Bachelor of Science-Computer Engineering

Major: Computer Engineering **Major:** Computer Science

Activities and Societies: Dean's List, Badger Powerlifting, and Engineering Expo Volunteer

Skills

Languages: Bash, C, C++, C#, Java, JavaScript, Python, Verilog, SystemVerilog, SQL, SQLite, HTML, CSS, React

Tools: ModelSim, Intel Quartus/Questa, VSCode, Visual Studio, Git, Gitlab, Jupyter, PowerShell, Linux, UNIX, Matlab, Altium, Docker, Kubernetes, Agile, RESTful APIs, PyTorch, Azure, GCC/GDB, RTOS, Shell, FPGAs, PCBs

Interpersonal Skills: Leadership/positive influence for team environments, collaborative, conflict resolution

Internship Experience

Information Systems Engineer, PAR Systems – Shoreview, MN June 2024 – Jan 2025

- Developed a PowerShell script to automate Windows OS installation and application deployment on new machines, as a fix for competing priorities between device provisioning and ticket management, boosting provisioning throughput by over 10× as well as freeing the team to focus on critical support tickets
- Maintained Azure, Active Directory, Barracuda, and SolarWinds environments under DoD security requirements, and created new user education, resulting in improved uptime, fewer incident reports, and faster resolution times
- Built a Python wrapper to run PowerShell commands for bulk deleting, creating, and modifying user accounts, for correcting out of date or incorrect Active Directory data, which reduced server storage usage and kept our directory's company information current

Projects

Air Defense System hmrdo.github.io/air-defense-project.github.io/

- Designed a real-time object detection pipeline and servo-controlled laser tracking system on an FPGA development board using Verilog, as part of a five-person senior design project, earning the Capstone Design Excellence Award exclusive to our class
- Collaborated with a teammate to optimize the camera logic pipeline over I2C due to slow frame-rate, ghosting, and artifacts, boosting frame throughput 4× to 60 FPS, eliminating the ghosting and quadrupling the speed of object detection
- Used ModelSim to simulate Verilog code on test-benches before assimilating into a synthesizable hierarchy where SignalTap was used in Quartus to debug and fix synthesized code on the FPGA, improving troubleshooting time and accelerating project delivery ahead of timeline
- Adhering to project specifications, developed a website in React to showcase the project timeline, architecture reviews, and a demo, resulting in a concise, modern, and well-understood representation of the project
- Collaborated with teammates, other teams, professors to develop and implement comprehensive project timelines, scope, and responsibilities, resulting in a well-structured and easy-to-follow plan of action

Five-Stage Pipelined Processor github.com/hmrdo/5-Stage-Pipelined-Processor

- Designed a processor with a five-stage (fetch-decode-execute-memory-writeback) pipeline for the WISC-ISA, tested with instructions written in assembly, creating a 100% accurate simulation of the ISA
- Optimized the processor with branch-prediction, data-forwarding from write-back, memory, and execute stages, and a 2-way-set-associative cache for data and instructions, to compete with classmates, providing an average 4× IPC improvement in all instructions

Two-Player Game on Microprocessor 2024

- Programmed a micro-controller using C to interface with another micro-controller over SPI, UART, and I2C communication protocols, locally with joysticks, buttons, and a screen, as well as manipulating interrupts and timers within the RTOS, to create a two-player memory game called Matching Pairs