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ARTICLE

Tunable *n*-Type Doping of Carbon Nanotubes through Engineered Atomic Layer Deposition HfO_X Films

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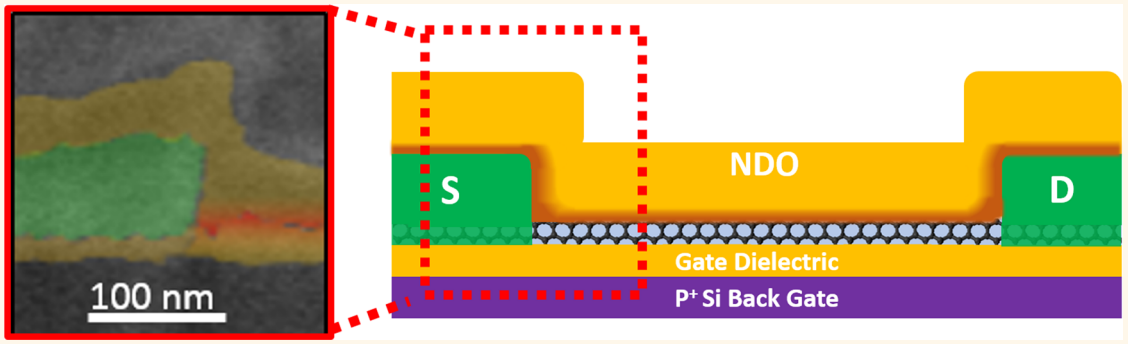
Supporting Information



ABSTRACT: **Although digital systems fabricated from carbon-nanotube-based field-effect transistors (CNFETs) promise significant energy efficiency benefits, realizing these benefits requires a complementary CNFET technology, *i.e.*, CNFET CMOS, comprising both PMOS and NMOS CNFETs. Furthermore, this CNFET CMOS process must be robust (*e.g.*, air-stable), tunable (*e.g.*, ability to control CNFET threshold voltages), and silicon CMOS compatible (to integrate within existing manufacturing facilities and process flows). Despite many efforts, such a silicon CMOS compatible CNT doping strategy for forming NMOS CNFETs does not exist. Techniques today are either not air-stable (using reactive low work function metals), not solid-state or silicon CMOS compatible (employing soluble molecular dopants in ionic solutions), or have not demonstrated precise control over the amount of doping (for setting threshold voltage, V_T). Here, we demonstrate an electrostatic doping technique that meets all of these requirements. The key to our technique is leveraging atomic layer deposition (ALD) to encapsulate CNTs with nonstoichiometric oxides. We show that ALD allows for precise control of oxide stoichiometry, which translates to direct control of the amount of CNT doping. We experimentally demonstrate the ability to modulate the strength of the *p*-type conduction branch by >2500× (measured as the change in current at fixed bias), realize NMOS CNFETs with *n*-type conduction ∼500× stronger than *p*-type conduction (also measured by the relative current at fixed biases), and tune V_T over a ∼1.5 V range. Moreover, our technique is compatible with other doping schemes; as an illustration, we combine electrostatic doping and low work function contact engineering to achieve CNFET CMOS with symmetric NMOS and PMOS (*i.e.*, CNFET ON-current for NMOS and PMOS is within 6% of each other). Thus, this work realizes a solid-state, air-table, very large scale integration and silicon CMOS compatible doping strategy, enabling integration of CNFET CMOS within standard fabrication processes today.**

KEYWORDS: *doping, CMOS, carbon nanotubes, transistors, digital logic*

As performance benefits with silicon-based computing systems are suffering from diminishing returns, alternative technologies are being pursued. Carbon nanotubes (CNTs) are an attractive emerging nanotechnology to build digital very large scale integration (VLSI) circuits, owing to their superior carrier transport with simultaneously ultrathin body (∼1 nm diameter).[1] Carbon nanotube field-effect transistors (CNFETs) are projected to improve energy efficiency of digital VLSI circuits by an order of magnitude *versus* that of silicon CMOS (quantified by EDP, energy-delay product),[2] while simultaneously enabling further opportunities for energy efficiency benefits (*e.g.*, for system architectures such as monolithic three-dimensional integrated systems[3−5]). Over the past decade, significant progress with CNT technology has transformed them from a scientifically interesting material to a

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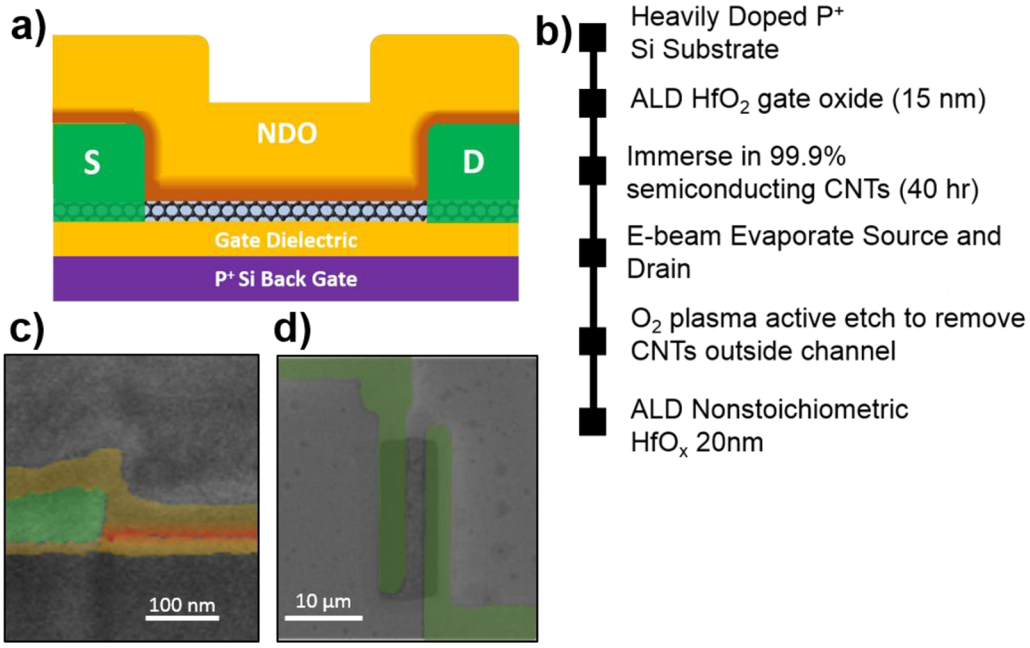

Figure 1. CNFET structure. (a) Schematic of NMOS CNFET encapsulated by nonstoichiometric doping oxide (NDO). The region shaded in red underneath the NDO represents the hafnium-rich oxide at the CNT−NDO interface. (b) Process flow for CNFETs. (c) Cross-sectional and (d) top-view scanning electron microscopy (SEM) images of a fabricated global back-gate CNFET encapsulated in NDO.

potential supplement to silicon CMOS for next-generation high-performance digital systems: high-performance PMOS CNFETs competitive with silicon FETs,[6−10] controlled CNT placement,[8,11,12] and complete digital systems (fabricated entirely with PMOS CNFETs)[3,13−15] have all been experimentally demonstrated.

Despite this progress, a major remaining obstacle facing CNFETs is the ability to dope CNTs to realize CNFET CMOS circuits (integrating PMOS and NMOS CNFETs). Specifically, it remains a challenge to dope CNTs to reliably form NMOS CNFETs. Whereas a range of previous efforts have fabricated NMOS CNFETs, no prior work satisfies all of the following requirements for a CNFET CMOS technology:

(1) tunable doping: simply realizing NMOS and PMOS CNFETs is insufficient; digital systems require a range of doping values to precisely set device parameters, such as threshold voltage (V_T)
(2) silicon CMOS compatible: solid-state and silicon CMOS compatible materials are required for ease of integration in current commercial fabrication facilities
(3) air-stable: the process should be air-stable (both during and postprocessing) to avoid changing device performance and/or increased variability
(4) uniform and robust: to yield digital VLSI systems, potentially comprising billions of CNFETs, any doping must be highly reproducible and uniform across devices on the same sample and devices across multiple samples.

For instance, many existing techniques for realizing NMOS CNFETs rely on low work function metal source/drain contacts (such as scandium, erbium, lanthanum, or calcium).[16−18] These materials are extremely air-reactive are not silicon CMOS compatible and, due to their reactivity, are also not uniform or robust (*e.g.*, they either significantly increase device variability compared to PMOS CNFET variability[18] or do not always successfully realize NMOS CNFETs). Alternative doping strategies leveraging reactive molecular dopants[19−21] similarly rely on materials not used in conventional silicon CMOS processing and contain contaminants (*e.g.*, ionic salts) that are prohibited from commercial fabrication facilities, are often not air-stable, and are not solid-state. NMOS CNFETs have also been realized by encapsulating CNTs with dielectrics,[26−29] but such methods have not simultaneously demonstrated both tunable and robust *n*-type doping (for instance, refs 26 and 27 rely on 20 Å electron-beam-evaporated aluminum or 50 Å of ytttrium over the CNTs, which is then allowed to oxidize in ambient environment; this lacks the control and uniformity afforded by atomic layer deposition).

Here, we demonstrate an electrostatic CNT doping technique that meets all of the requirements for realizing a CNFET CMOS technology (Figure 1). Specifically, this work demonstrates that precise engineering of the stoichiometry of dielectrics (referred to as the "nonstoichiometric doping oxide", NDO, in this instance HfO_X) deposited over exposed CNTs in the channel of CNFETs results in tunable and robust CNT doping. To accomplish this, we experimentally show that atomic layer deposition (ALD) allows for precise engineering of the stoichiometry of the NDO (*e.g.*, modifying the Hf content at the HfO_X−CNT interface), which in turn results in fine-grained control over the amount of *n*-type doping, the relative strengths of the *p*-type and *n*-type conduction, and the threshold voltage. We also present a model that directly relates the stoichiometry of the HfO_X NDO to an effective Schottky barrier height (Φ^*_{SB}), enabling designers to engineer a given NDO stoichiometry to achieve a precise quantity of CNT doping.

Moreover, we experimentally demonstrate the following key attributes: (1) our technique can be combined with other doping schemes. As an illustration, we combine NDO electrostatic doping with low work function contact engineering to achieve CNFET CMOS with NMOS and PMOS that achieve similar ON-current, OFF-current, and threshold

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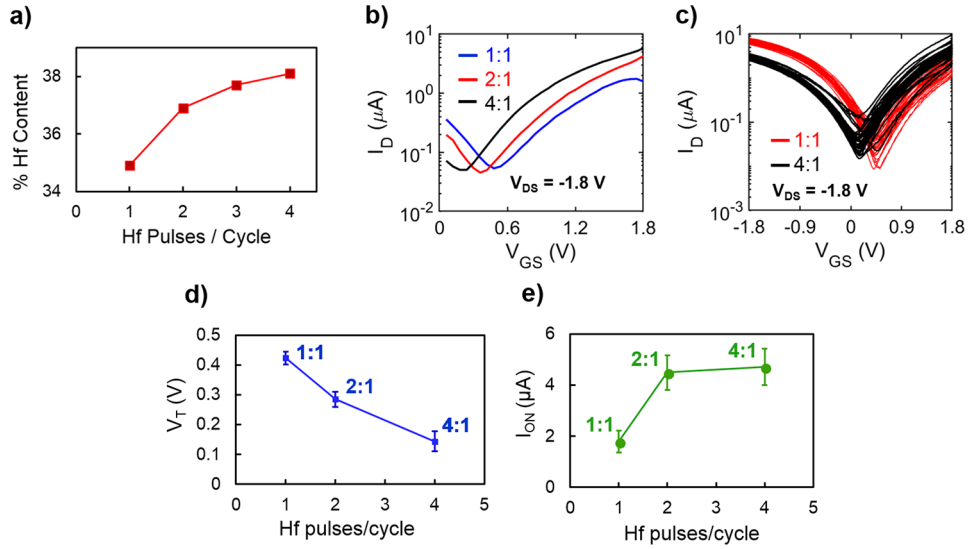

Figure 2. Controlling HfO_X stoichiometry for tunable doping. (a) Hf content with increasing Hf precursor/H_2O pulse ratio. (b) I_D–V_{GS} characteristics for CNFETs doped with Hf precursor/H_2O ratios of 1:1, 2:1, and 4:1 (measured with V_{DS} = −1.8 V). (c) Comparison of two sets of 35 CNFETs doped with 4:1 and 1:1 Hf/H_2O ratios. (d) Corresponding average V_T shift and (e) average *n*-branch ON-current (I_{ON}) for each type of NMOS CNFET with error bars indicating 99% confidence interval (sample size: 105 CNFETs). ON-current is extracted as the drain current at $|V_{GS}| = |V_{DS}| = |V_{DD}|$.

voltage magnitudes (referred to as "symmetric" NMOS and PMOS CNFETs). Due to the combined doping strategy, the contact metal does not need to have extremely low work function (<4 eV, such as scandium), but rather can have a work function >4 eV, such as titanium (a silicon CMOS compatible metal) while still realizing symmetric NMOS and PMOS. (2) The NDO electrostatic doping does not degrade performance (*e.g.*, V_T variations, inverse subthreshold slope, I_{ON}/I_{OFF}, and gate leakage are statistically similar to PMOS CNFETs). (3) We demonstrate CNFET static CMOS digital logic gates with rail-to-rail swing (>99% of supply voltage) and high gain (>15). (Gain is defined as the maximum absolute value of change in the output voltage with respect to the input voltage, $\Delta V_{OUT}/\Delta V_{IN}$.) Thus, this work provides a path for integrating CNFET CMOS within standard fabrication processes today by realizing a solid-state, air-stable, VLSI, and silicon CMOS compatible doping strategy.

RESULTS AND DISCUSSION

Doping Technique: ALD-Engineered NDO. Figure 1a–d shows the schematic, fabrication flow, and scanning electron microscope (SEM) images of a typical CNFET. Multiple CNTs comprise the channel with lithographically defined source, drain, and gate contacts. The gate metal and high-*k* gate dielectric (different oxide from the NDO, which is physically located on the other side of the channel compared to the high-*k* gate dielectric) is fabricated beneath the CNT channel, forming a back-gate device structure. Following the initial CNFET fabrication, an ALD-deposited HfO_X is deposited over the CNTs (*i.e.*, the NDO). The HfO_X dopes the CNT through electrochemical reduction (redox) of the CNTs in contact with hafnium,[27] as well as through field-effect doping, owing to the fixed charges in the HfO_X.[28,29] By controlling the stoichiometry of the first atomic layers of the NDO as well as the stoichiometry of the bulk NDO, we can precisely control both the amount of redox reaction at the HfO_X–CNT interface and the fixed charge, respectively.

ALD is key for engineering the stoichiometry of each atomic layer within the NDO. ALD HfO_X is deposited by alternating pulses of the precursor (tetrakis(dimethylamido)hafnium(IV)) and H_2O into a process chamber. The duration of the pulses, time between pulses, as well as the ratio of the Hf precursor/H_2O pulses change the amount and time the wafer is exposed to the Hf precursor,[30] resulting in fine-grained control over the HfO_X stoichiometry. Moreover, ALD is an industry-standard capability, and HfO_X dielectrics are already used in front-end-of-line silicon CMOS fabrication. To demonstrate the ability to fine-tune the stoichiometry of the NDO, we vary the pulse ratio of Hf/H_2O during the HfO_X deposition. As shown in Figure 2a, as the pulse ratio of Hf/H_2O increases from 1:1, 2:1, 3:1, and 4:1, the bulk Hf concentration increases from 34.9% to 36.9, 37.7, and 38.1% (measured by X-ray photoelectron spectroscopy, XPS). Importantly, the ability to vary NDO stoichiometry results in the ability to fine-tune CNT doping (resulting in varying relative strengths of the *p*-type and *n*-type branches in CNFET current–voltage characteristics, as well as control of the threshold voltage). We deposit each of the different NDO stoichiometries over back-gated CNFETs. Figure 2b–e illustrates how the slight increase in Hf concentration results in increasingly strong *n*-type doping of CNTs. As the Hf concentration increases, the strength of the *n*-type conduction branch increases, as evident by increasing drive current (average drive current (I_{ON}) of 1.8, 4.5, and 4.7 μA), as well as a reduction in the *p*-type conduction branch, which manifests as an increasingly negative shift in the V_T (average V_T of 0.40, 0.22, and 0.12 V). Moreover, this doping scheme is robust due to the high reproducibility and tight process control afforded by ALD: Supporting Information Figure S1 shows how two different wafers with the same NDO result in statistically similar doping (average V_T for the two wafers are 0.32 and 0.35 V).

To drastically increase the amount of *n*-type doping and realize unipolar NMOS CNFETs, the first several atomic layers (at the HfO_X–CNT interface) can be engineered with significantly higher Hf concentration. This is another key

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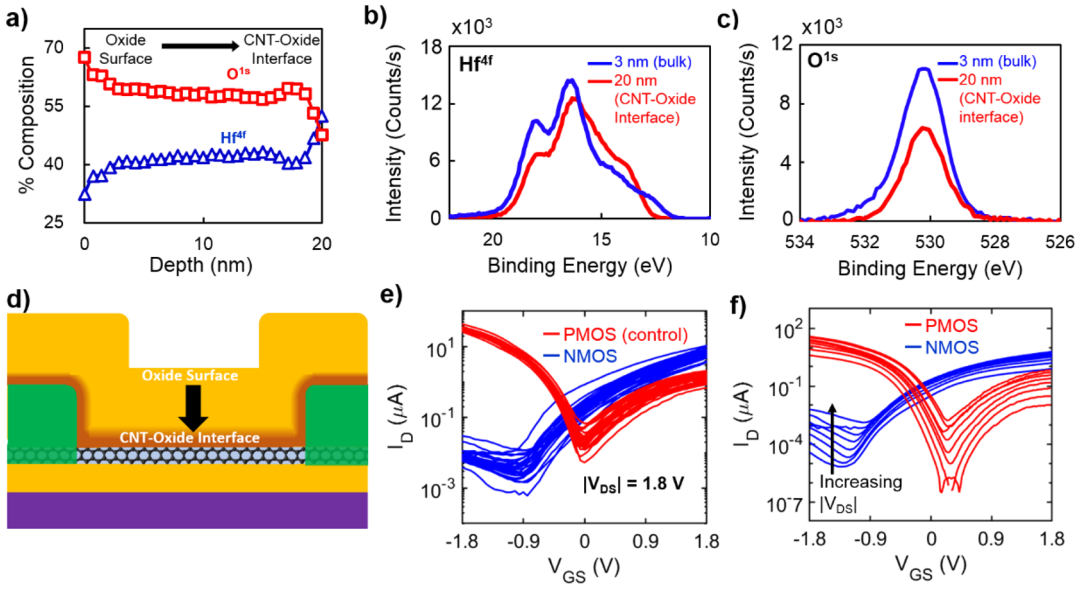

Figure 3. Material and electrical characterization of CNFETs with engineered Hf-rich HfO_X−CNT interface. (a) XPS depth profile of HfO_X film from surface to HfO_X−CNT interface. To increase Hf concentration in the first atomic layers, the wafer is pretreated with 50 pulses of Hf precursor (no H_2O), followed by 20 nm 3:1 HfO_X deposition. XPS confirms that the first few atomic layers reach >52% Hf, whereas the bulk has ∼38% Hf. (b) Hf^{4f} and (c) O^{1s} peaks at 3 nm depth (bulk HfO_2 film) and 20 nm depth (CNT−HfO_2 interface). (d) Schematic of CNFET identifying the NDO oxide surface and CNT−oxide interface. (e) I_D−V_{GS} curves of 35 CNFETs before and after *n*-type doping with Hf-rich CNT−oxide interface measured at V_{DS} = −1.8 V and V_{DS} = 1.8 V, respectively. The difference in ON-current between the PMOS and NMOS CNFETs is caused by all of these CNFETs using platinum metal source and drain contacts (see Figure 4 for additional details). (f) I_D−V_{GS} curves with V_{DS} swept from −0.2 to −1.8 V in −0.2 V steps for the PMOS and 0.2 to 1.8 V in 0.2 V steps for the NMOS CNFETs.

benefit of leveraging ALD, as the stoichiometry of each atomic layer can be independently controlled. The wafer is pretreated with 50 repeated pulses of Hf precursor (without H_2O pulses), followed by HfO_X deposition. As shown in Figure 3a−d, XPS confirms that the first few atomic layers at the CNT−oxide interface reach >52% Hf, while the bulk has ∼38% Hf. Electrical characterization of the back-gate CNFETs encapsulated with this NDO (*e.g.*, 50 repeated pulses of Hf precursor) in Figure 3e,f shows strongly unipolar NMOS CNFETs, increasing the *n*-type conduction branch by ∼500× while decreasing the *p*-type conduction branch by >2500× compared to the as-fabricated initial PMOS CNFETs (prior to NDO deposition). A key advantage of this doping scheme is that while such a Hf-rich atomic layer is a strong reducer (resulting in the strong *n*-type doping), it is encapsulated *in situ* within the low-pressure ALD chamber during the subsequent HfO_X deposition and is thus air-stable. Figure S2 shows CNFETs measured after 4, 12, and 30 days exposed to air; there is negligible change in the CNFET electrical characteristics. Moreover, Figure S3 shows this nonstoichiometric oxide does not increase gate leakage.

Having demonstrated how NDO encapsulation enables tunable doping of CNTs, we present a method for quantifying the degree of *n*-type doping resulting from an NDO-encapsulated CNFET. Quantifying the amount of CNT doping is critical for circuit design, as the amount of doping determines key parameters such as V_T. To quantify the amount of CNT doping, we define an effective Schottky barrier height (Φ_{SB}^{*}) between the CNT and the source/drain metal contacts (energy band diagram shown in Supporting Information, Figure S4c). We use an effective Schottky barrier height as the *p*-type and *n*-type conduction in CNFETs is largely determined by the Schottky barrier height at the interface between the CNT and source/drain metal contacts.[31] In the band diagram drawn in Supporting Information Figure S4c, Φ_{SB}^{*} is the height of the potential barrier inhibiting electron transport from the source metal to semiconducting CNT channel. Higher values of Φ_{SB}^{*} result in a greater tunneling barrier for conduction electrons, reducing *n*-branch current. By calibrating our experimental I_D−V_{GS} data to a Schottky barrier transport model,[32] we calibrate each fabricated CNFET to an associated value for Φ_{SB}^{*}, determining a relationship between NDO stoichiometry and the Φ_{SB}^{*}. The Landauer formulation was used to define the transport equations, and the Wentzel−Kramer−Brillouin approximation (see Supporting Information, Figure S4a,b) was used to solve the tunneling probability across the Schottky barrier of height Φ_{SB}^{*}. As shown in Supporting Information Figure S4d, increasing the hafnium content in the NDO layer lowers Φ_{SB}^{*} from 0.3 to 0.15 eV, thereby bolstering *n*-type conduction in CNFETs. Therefore, analogous to how the degree of doping in silicon is quantified by the dopant concentration (interstitial dopants per cm^3), we likewise can quantify (and modulate) the degree of CNFET doping by tuning the NDO stoichiometry (by calculating the corresponding effective Schottky barrier height).

Symmetric CNFET CMOS Characterization. To achieve NMOS and PMOS CNFETs with similar I_{ON}, I_{OFF}, and V_T, previous works have relied on extremely low work function metals (such as scandium and erbium) to reduce the Schottky barrier for electron injection into the CNT channel.[16−18] However, as discussed previously, the high reactivity of these materials precludes their integration into a silicon CMOS compatible fabrication process. Unfortunately, prior works attempting to use the lowest work function metals readily available in standard silicon CMOS processing—such as titanium—report significantly degraded *n*-type CNFET conduction[33] (as titanium's work function (4.33 eV) is lower than typical contact metals used for PMOS CNFETs such as

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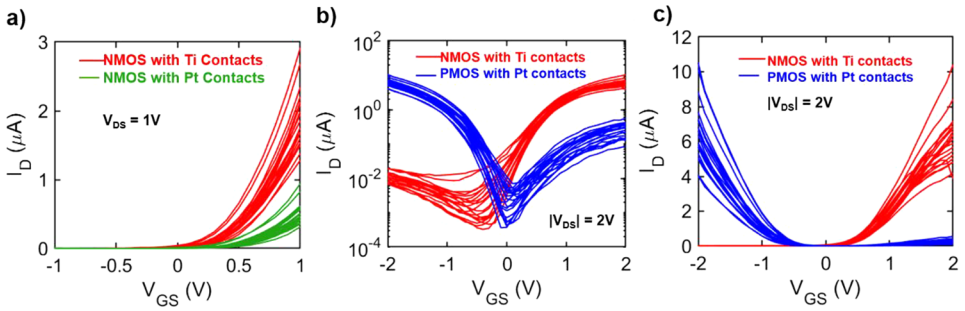

Figure 4. Combining NDO encapsulation with low work function contacts to achieve symmetric NMOS/PMOS CNFETs with similar I_{ON}, I_{OFF}, and V_T magnitude. (a) I_D−V_{GS} (linear scale) for NDO-encapsulated NMOS CNFETs with titanium contacts (red) and platinum contacts (green). (b,c) I_D−V_{GS} curves comparing 20 NDO-encapsulated NMOS CNFETs with titanium contacts (red) and 20 PMOS CNFETs with platinum contacts (blue).

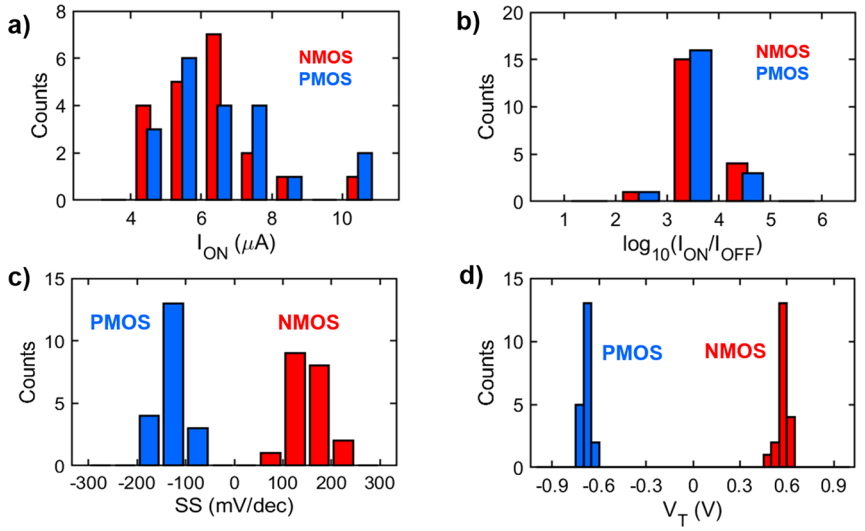

Figure 5. Summary statistics for 20 NMOS and 20 PMOS CNFETs measured with V_{DS} = 2 V (for NMOS) and V_{DS} = −2 V (for PMOS) and V_{GS} swept from 2 to −2 V for both NMOS and PMOS. (a) ON-current distribution for NMOS CNFETs, measured with V_{DS} = V_{GS} = 2 V (average, $\mu_{ION,N}$ = 6.24 μA; standard deviation, $\sigma_{ION,N}$ = 1.42 μA) and PMOS CNFETs, measured with V_{DS} = V_{GS} = −2 V (average, $\mu_{ION,P}$ = 6.60 μA; standard deviation, $\sigma_{ION,P}$ = 1.74 μA). (b) Distribution of $\log_{10}(I_{ON}/I_{OFF})$ for NMOS CNFETs (average, 3.63; standard deviation, 0.42) and PMOS CNFETs (average, 3.58; standard deviation, 0.35). (c) Distribution of maximum subthreshold slope for NMOS (mean, μ_n = 153.7 mV/decade; standard deviation, σ_n = 38.1 mV/decade) and PMOS (mean, μ_p = 125.4 mV/decade; standard deviation, σ_p = 24.5 mV/decade) CNFETs. (d) Threshold voltage distribution for NMOS CNFETs (mean, $\mu_{VT,N}$ = 0.57 V and $\sigma_{VT,N}$ = 0.03 V) and PMOS CNFETs (mean, $\mu_{VT,P}$ = −0.68 V; standard deviation, $\sigma_{VT,P}$ = 0.03 V). The threshold voltage of each CNFET was calculated using the extrapolation in linear region method, where the I_D−V_{GS} characteristic is linearly extrapolated at its point of highest slope and intersects the gate voltage axis at the threshold voltage.

palladium (5.22−5.64 eV), gold (5.31−5.47 eV), or platinum (5.12−5.93 eV), but still higher than scandium (3.5 eV), erbium (3.0 eV), *etc.*).

We show that, when combined with NDO encapsulation, NMOS CNFETs employing titanium contacts show symmetric performance as PMOS CNFETs fabricated with platinum contacts (a conventional source and drain metal for PMOS CNFETs[3,10,13,34,35]). Figure 4a shows the *IV* characteristics of a set of NMOS CNFETs with titanium contacts and a set of NMOS CNFETs with platinum contacts, all of which have been encapsulated with the same NDO. The NMOS CNFETS with titanium contacts achieve a 3× improvement in *n*-type conduction ON-current compared to NMOS CNFETs with platinum contacts (*e.g.*, the average I_{ON} increases by 3×). This enhanced *n*-type conduction allows us to fabricate, in a silicon CMOS compatible fashion, PMOS and NMOS CNFETs with symmetric *IV* characteristics (I_D−V_{GS} curves in Figure 4b,c).

Importantly, in contrast to previously reported doping methods, our combined doping technique neither degrades key device characteristics nor introduces significant device variability. Figure 5 shows distributions for a set of NMOS and PMOS CNFETs to demonstrate how key device characteristics such as I_{ON}, I_{ON}/I_{OFF}, inverse subthreshold slope, and $|V_T|$ are unchanged after *n*-type doping. As seen in Figure 5a,b, both the NMOS and PMOS devices exhibit nearly identical drive current and I_{ON}/I_{OFF} distributions (average I_{ON} and $\log_{10}(I_{ON}/I_{OFF})$ differ by <6% and <2%, respectively). The NMOS and PMOS CNFETs also exhibit similar inverse subthreshold slope and threshold voltage distributions (quantified by the mean and standard deviation; see Figure 5c,d), while having a minimal effect on device-to-device variations. Whereas previously reported doping techniques that used unstable and air-reactive materials introduce large variations in *IV* characteristics,[18,27] this combined doping technique avoids these variations by using only air-stable

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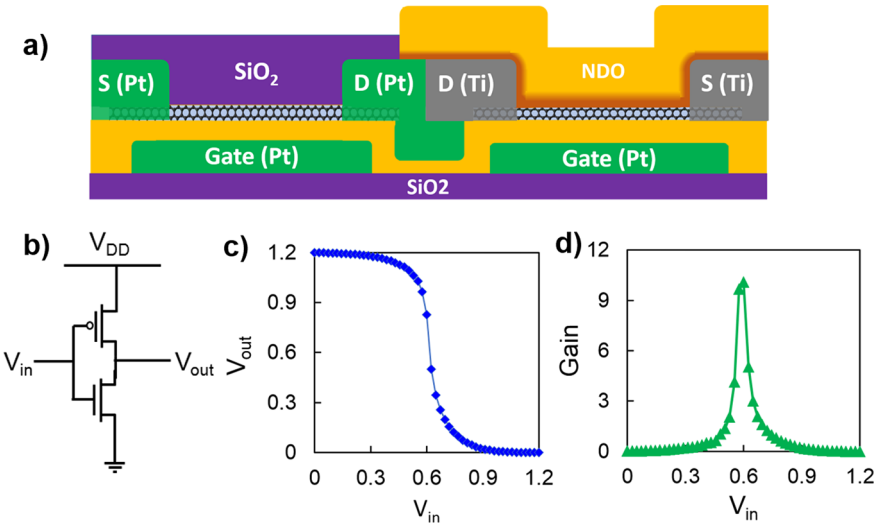

Figure 6. Static CMOS inverter fabricated by combing NDO encapsulation with lower work function contact engineering. (a) Cross-sectional schematic of local back-gate PMOS and NMOS CNFETs fabricated on the same die. (b) Circuit schematic for CMOS inverter. (c) Voltage transfer curve for fabricated CNFET inverter operating at a V_{DD} of 1.2 V. When V_{in} = 0 V, V_{out} reaches 99.92% of V_{DD} and when V_{in} = V_{DD}, V_{out} reaches 0.03% of V_{DD}. (d) Plot of inverter gain (change in V_{OUT} over change in V_{IN}) *versus* V_{in}, where the gain reaches a maximum of 10.

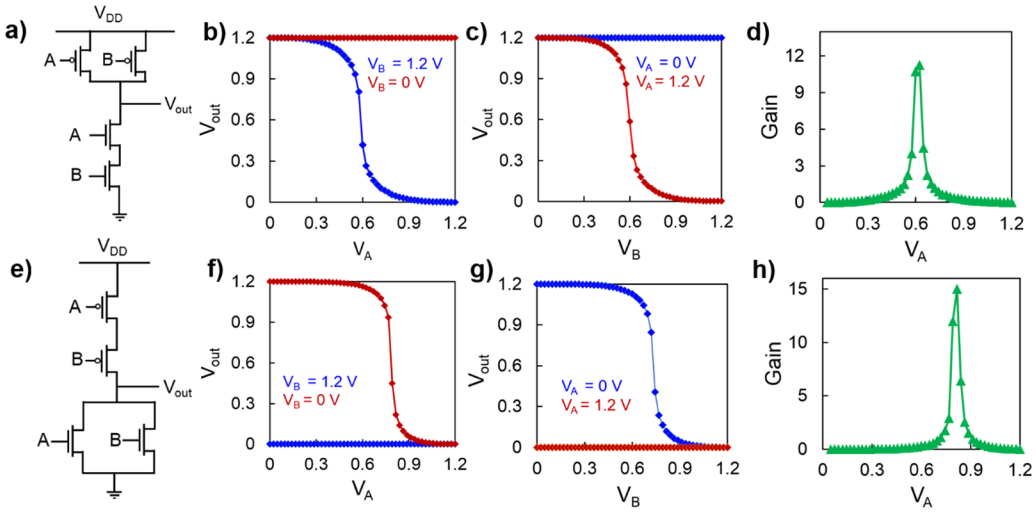

Figure 7. Two-input logic gates fabricated by combing NDO encapsulation with lower work function contact engineering. (a) Circuit diagram for static CMOS "not-and" (NAND2) logic gate. Voltage transfer curve for a NAND2 gate (b) when input V_A is swept from 0 to 1.2 V and (c) when input V_B is swept from 0 to 1.2 V. (d) Plot of NAND2 gate gain *versus* V_A (with V_B = V_{DD}), where a maximum gain of 11 is achieved. (e) Circuit diagram for CMOS NOR2 logic gate. Voltage transfer curve for a NOR2 gate (f) when the input V_A is swept from 0 to 1.2 V and (g) when the input V_B is swept from 0 to 1.2 V. (h) Plot of NOR2 gate gain *versus* V_A, where a maximum gain of 15 is achieved.

materials (HfO_2 and Ti) that are already integrated within standard silicon-based fabrication processes.

CNFET CMOS Logic. As a demonstration, we integrate local back-gate NMOS and PMOS CNFETs on the same substrate and demonstrate static CMOS logic gates: inverters, 2-input "not-or" (NOR2), and 2-input "not-and" (NAND2) logic gates with rail-to-rail swing and high gain. Figure 6 shows the voltage transfer curve of a fabricated CMOS inverter. It achieves near-rail-to-rail swing (the output voltage swing is >99% of V_{DD}), with a maximum gain of >10 (Figure 6c,d). Figure 7 shows fabricated two-input CMOS logic gates: CMOS NAND2 and CMOS NOR2 logic gates (circuit schematics in Figure 7a,e). In Figure 7b–d,f–h) both the NAND2 and NOR2 gates achieve near-rail-to-rail swing (the output voltage swing is >99% of V_{DD}), with a maximum gain of >11 and >15, respectively. Importantly, all of these logic gates are measured at a scaled supply voltage of 1.2 V_{DD}, without any external biasing.

CONCLUSION

We demonstrate a CNT doping technique that meets all of the requirements for realizing a future CNFET CMOS technology. The key to our technique is leveraging atomic layer deposition to encapsulate CNTs with nonstoichiometric oxides, which can be seamlessly combined with additional techniques (such as work function engineering). Using this approach, we demonstrate symmetric NMOS and PMOS CNFETs, as well as CMOS logic gates that achieve rail-to-rail output voltage swings of >99.9% and gains of >10 at a supply voltage of 1.2 V_{DD}. Moreover, the results from this work are applicable to a

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wide range of emerging one-dimensional and two-dimensional nanomaterials (as electrostatic doping is applicable to many ultrathin body materials[22−25]). Therefore, this work realizes a solid-state, air-stable, VLSI, and silicon CMOS compatible doping strategy, enabling integration of CNFET CMOS within standard fabrication processes today.

METHODS

Global Back-Gate CNFET Fabrication. For global back-gate CNFETs, a highly *p*-doped silicon substrate is used as the back-gate for all CNFETs. Fifteen nanometers of HfO_X is deposited using ALD for the gate dielectric. Importantly, all local back-gate CNFETs (PMOS or NMOS) are fabricated with the same gate stack: platinum metal for the back-gate followed by 15 nm of HfO_X as the gate dielectric. The wafer is then immersed in >99.9% semiconducting CNT solution (modified Nanointegris IsoSol-S100) for 48 h. The average CNT density is ∼15 CNTs/ μm. The channel length of the CNFETs is smaller than the average length of the CNTs. Therefore, the CNFETs comprise both direct transport from CNTs bridging the entire channel as well as percolation transport from network-based CNTs. Lithography was used to define the source and drain electrodes (channel length ∼2.5 μm and channel width = 20 μm, doping results are similar to channel length = 1 μm). Titanium and/or platinum were then deposited using electron-beam evaporation followed by lift-off. To dope the NMOS CNFETS, 20 nm of NDO is deposited using ALD. A chlorine reactive ion etch removes the NDO covering the probing pads.

CMOS Logic Gate Fabrication. Local metal back-gates are defined on top of a 800 nm SiO_2 wafer using photolithography. The rest of the fabrication up through CNT deposition follows the above. After CNT deposition, 1 nm titanium and 40 nm platinum are deposited for the PMOS source and drain electrodes, and 40 nm titanium is deposited for the NMOS source and drain electrodes by electron-beam evaporation followed by lift-off. CNTs outside the channel were selectively removed using an oxygen plasma etch. The 40 nm SiO_2 was then deposited over the PMOS CNFETs using electron-beam evaporation to protect the CNTs from the subsequent NDO deposition, while the NMOS CNFETs are left exposed. To dope the NMOS CNFETS, 20 nm of NDO is deposited over the substrate, followed by removing the NDO above the PMOS CNFETs using a chlorine reactive ion etch (the PMOS CNFETs are protected during this etch by the previously deposited SiO_2). Final metal routing can then be patterned and defined.

XPS Material Characterization. X-ray photoelectron spectroscopy data were obtained using a PHI VersaProbe II XPS. The Hf^{4f} and O^{1s} spectra were measured for ALD-deposited NDO films. Measurements of hafnium and oxygen content in bulk NDO films were made by obtaining Hf^{4f} and O^{1s} spectra after using 6 min of Ar sputtering (∼5 Å/min) to remove the first 3 nm from the NDO surface. A depth profile of NDO films was obtained by measuring the Hf^{4f} and O^{1s} spectra after each minute of Ar sputtering (40 min total).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b04208.

Additional information on air stability, gate leakage, hysteresis, wafer-to-wafer reproducibility, and modeling the effective Schottky barrier height (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Appenzeller, J. Carbon Nanotubes for High-Performance Electronics—Progress and Prospect. *Proc. IEEE* **2008**, *96*, 201−211.

(2) Kuhn, K. J.; Avci, U.; Cappellani, A.; Giles, M. D.; Haverty, M.; Kim, S.; Kotlyar, R.; Manipatruni, S.; Nikonov, D.; Pawashe, C. .; Radosavljevic, M.; Rios, R.; Shankar, S.; Vedula, R.; Chau, R.; Young, I. The Ultimate CMOS Device and Beyond. *IEEE Int. Electron Devices Meet* **2012**, *8*, 8.1.1−8.1.4.

(3) Shulaker, M. M.; Hills, G.; Park, R. S.; Howe, R. T.; Saraswat, K.; Wong, H.-S. P.; Mitra, S. Three-Dimensional Integration of Nanotechnologies for Computing and Data Storage on a Single Chip. *Nature* **2017**, *547*, 74−78.

(4) Shulaker, M. M.; Wu, T. F.; Pal, A.; Zhao, L.; Nishi, Y.; Saraswat, K.; Wong, H.-S. P.; Mitra, S. Monolithic 3D Integration of Logic and Memory: Carbon Nanotube FETs, Resistive RAM, and Silicon FETs. *2014 IEEE International Electron Devices Meeting* **2014**, *27*, 27.4.1−27.4.4.

(5) Sabry Aly, M. M.; Gao, M.; Hills, G.; Lee, C.-S.; Pitner, G.; Shulaker, M. M.; Wu, T. F.; Asheghi, M.; Bokor, J.; Franchetti, F.; Goodson, K.; Kozyrakis, C.; Markov, I.; Olukotun, K.; Pileggi, L.; Pop, E.; Rabaey, J.; Ré, C.; Wong, H.-S. P.; Mitra, S. Energy-Efficient Abundant-Data Computing: The N3XT 1,000x. *Computer (Long. Beach. Calif)* **2015**, *48*, 24−33.

(6) Cao, Q.; Tersoff, J.; Farmer, D. B.; Zhu, Y.; Han, S.-J. Carbon Nanotube Transistors Scaled to a 40-Nanometer Footprint. *Science* **2017**, *356*, 1369−1372.

(7) Qiu, C.; Zhang, Z.; Xiao, M.; Yang, Y.; Zhong, D.; Peng, L.-M. Scaling Carbon Nanotube Complementary Transistors to 5-Nm Gate Lengths. *Science* **2017**, *355*, 271−276.

(8) Brady, G. J.; Way, A. J.; Safron, N. S.; Evensen, H. T.; Gopalan, P.; Arnold, M. S. Quasi-Ballistic Carbon Nanotube Array Transistors with Current Density Exceeding Si and GaAs. *Sci. Adv.* **2016**, *2*, e1601240−e1601240.

(9) Zhong, D.; Xiao, M.; Zhang, Z.; Peng, L.-M. Solution-Processed Carbon Nanotubes Based Transistors with Current Density of 1.7 MA/Mm and Peak Transconductance of 0.8 MS/Mm. *2017 IEEE International Electron Devices Meeting (IEDM)* **2017**, 5.6.1−5.6.4.

(10) Shulaker, M. M.; Pitner, G.; Hills, G.; Giachino, M.; Wong, H.-S. P.; Mitra, S. High-Performance Carbon Nanotube Field-Effect Transistors. *2014 IEEE International Electron Devices Meeting* **2014**, *33*, 33.6.1−33.6.4.

(11) Cao, Q.; Han, S.; Tulevski, G. S.; Zhu, Y.; Lu, D. D.; Haensch, W. Arrays of Single-Walled Carbon Nanotubes with Full Surface Coverage for High-Performance Electronics. *Nat. Nanotechnol.* **2013**, *8*, 180−186.

(12) Joo, Y.; Brady, G. J.; Arnold, M. S.; Gopalan, P. Dose-Controlled, Floating Evaporative Self-Assembly and Alignment of Semiconducting Carbon Nanotubes from Organic Solvents. *Langmuir* **2014**, *30*, 3460−3466.

(13) Shulaker, M. M.; Hills, G.; Patil, N.; Wei, H.; Chen, H.-Y.; Wong, H.-S. P.; Mitra, S. Carbon Nanotube Computer. *Nature* **2013**, *501*, 526−530.

(14) Shulaker, M.; Van Rethy, J.; Hills, G.; Chen, H.; Gielen, G.; Wong, H. P.; Mitra, S. Experimental Demonstration of a Fully Digital Capacitive Sensor Interface Built Entirely Using Carbon-Nanotube FETs. *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers* **2013**, 112−113.

DOI: 10.1021/acsnano.8b04208
ACS Nano 2018, 12, 10924−10931

(15) Liu, Y.; Wang, S.; Liu, H.; Peng, L.-M. Carbon Nanotube-Based Three-Dimensional Monolithic Optoelectronic Integrated System. *Nat. Commun.* **2017**, *8*, 15649.
(16) Shahrjerdi, D.; Franklin, A. D.; Oida, S.; Ott, J. A.; Tulevski, G. S.; Haensch, W. High-Performance Air-Stable *n*-Type Carbon Nanotube Transistors with Erbium Contacts. *ACS Nano* **2013**, *7*, 8303−8308.
(17) Ding, L.; Wang, S.; Zhang, Z.; Zeng, Q.; Wang, Z.; Pei, T.; Yang, L.; Liang, X.; Shen, J.; Chen, Q.; Cui, R.; Li, Y.; Peng, L.-M. Y-Contacted High-Performance *n*-Type Single-Walled Carbon Nanotube Field-Effect Transistors: Scaling and Comparison with Sc-Contacted Devices. *Nano Lett.* **2009**, *9*, 4209−4214.
(18) Yang, Y.; Ding, L.; Han, J.; Zhang, Z.; Peng, L.-M. High-Performance Complementary Transistors and Medium-Scale Integrated Circuits Based on Carbon Nanotube Thin Films. *ACS Nano* **2017**, *11*, 4124−4132.
(19) Geier, M. L.; Prabhumirashi, P. L.; McMorrow, J. J.; Xu, W.; Seo, J.-W. T.; Everaerts, K.; Kim, C. H.; Marks, T. J.; Hersam, M. C. Subnanowatt Carbon Nanotube Complementary Logic Enabled by Threshold Voltage Control. *Nano Lett.* **2013**, *13*, 4810−4814.
(20) Geier, M. L.; Moudgil, K.; Barlow, S.; Marder, S. R.; Hersam, M. C. Controlled *n*-Type Doping of Carbon Nanotube Transistors by an Organorhodium Dimer. *Nano Lett.* **2016**, *16*, 4329−4334.
(21) Xu, J.-L.; Dai, R.-X.; Xin, Y.; Sun, Y.-L.; Li, X.; Yu, Y.-X.; Xiang, L.; Xie, D.; Wang, S.-D.; Ren, T.-L. Efficient and Reversible Electron Doping of Semiconductor-Enriched Single-Walled Carbon Nanotubes by Using Decamethylcobaltocene. *Sci. Rep.* **2017**, *7*, 6751.
(22) Rai, A.; Valsaraj, A.; Movva, H. C. P.; Roy, A.; Ghosh, R.; Sonde, S.; Kang, S.; Chang, J.; Trivedi, T.; Dey, R.; Guchhait, S.; Larentis, S.; Register, L.; Tutuc, E.; Banerjee, S. Air Stable Doping and Intrinsic Mobility Enhancement in Monolayer Molybdenum Disulfide by Amorphous Titanium Suboxide Encapsulation. *Nano Lett.* **2015**, *15*, 4329−4336.
(23) Valsaraj, A.; Chang, J.; Rai, A.; Register, L. F.; Banerjee, S. K. Theoretical and Experimental Investigation of Vacancy-Based Doping of Monolayer MoS_2 on Oxide. *2D Mater.* **2015**, *2*, 045009.
(24) Rai, A.; Valsaraj, A.; Movva, H. C. P.; Roy, A.; Tutuc, E.; Register, L. F.; Banerjee, S. K. Interfacial-Oxygen-Vacancy Mediated Doping of MoS_2 by high-k dielectrics. *2015 73rd Annual Device Research Conference (DRC)* **2015**, 189−190.
(25) McClellan, C. J.; Yalon, E.; Smithe, K. K. H.; Suryavanshi, S. V.; Pop, E. Effective *n*-Type Doping of Monolayer MoS_2 by AlO_x. *2017 75th Annual Device Research Conference (DRC)* **2017**, 1−2.
(26) Tang, J.; Cao, Q.; Tulevski, G.; Jenkins, K. A.; Nela, L.; Farmer, D. B.; Han, S.-J. Flexible CMOS Integrated Circuits Based on Carbon Nanotubes with Sub-10 ns Stage Delays. *Nat. Electron.* **2018**, *1*, 191−196.
(27) Suriyasena Liyanage, L.; Xu, X.; Pitner, G.; Bao, Z.; Wong, H.-S. P. VLSI-Compatible Carbon Nanotube Doping Technique with Low Work-Function Metal Oxides. *Nano Lett.* **2014**, *14*, 1884−1890.
(28) Zhang, J.; Wang, C.; Fu, Y.; Che, Y.; Zhou, C. Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from *p*-Type to *n*-Type Using Atomic Layer Deposition of High-κ Oxide and Its Application in CMOS Logic Circuits. *ACS Nano* **2011**, *5*, 3284−3292.
(29) Ha, T.-J.; Chen, K.; Chuang, S.; Yu, K. M.; Kiriya, D.; Javey, A. Highly Uniform and Stable *n*-Type Carbon Nanotube Transistors by Using Positively Charged Silicon Nitride Thin Films. *Nano Lett.* **2015**, *15*, 392−397.
(30) Aria, A. I.; Nakanishi, K.; Xiao, L.; Braeuninger-Weimer, P.; Sagade, A. A.; Alexander-Webber, J. A.; Hofmann, S. Parameter Space of Atomic Layer Deposition of Ultrathin Oxides on Graphene. *ACS Appl. Mater. Interfaces* **2016**, *8*, 30564−30575.
(31) Heinze, S.; Tersoff, J.; Martel, R.; Derycke, V.; Appenzeller, J.; Avouris, P. Carbon Nanotubes as Schottky Barrier Transistors. *Phys. Rev. Lett.* **2002**, *89*, 106801.
(32) Prakash, A.; Ilatikhameneh, H.; Wu, P.; Appenzeller, J. Understanding Contact Gating in Schottky Barrier Transistors from 2D Channels. *Sci. Rep.* **2017**, *7*, 12596.
(33) Chen, Z.; Appenzeller, J.; Knoch, J.; Lin, Y.-M.; Avouris, P. The Role of Metal−Nanotube Contact in the Performance of Carbon Nanotube Field-Effect Transistors. *Nano Lett.* **2005**, *5*, 1497−1502.
(34) Shulaker, M. M.; Wei, H.; Patil, N.; Provine, J.; Chen, H.-Y.; Wong, H.-S. P.; Mitra, S. Linear Increases in Carbon Nanotube Density Through Multiple Transfer Technique. *Nano Lett.* **2011**, *11*, 1881−1886.
(35) Shulaker, M. M.; Van Rethy, J.; Wu, T. F.; Suriyasena Liyanage, L.; Wei, H.; Li, Z.; Pop, E.; Gielen, G.; Wong, H.-S. P.; Mitra, S. Carbon Nanotube Circuit Integration up to Sub-20 Nm Channel Lengths. *ACS Nano* **2014**, *8*, 3434−3443.

DOI: 10.1021/acsnano.8b04208
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