OAI 33 (Static)

Group Number: 14

INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Group Members

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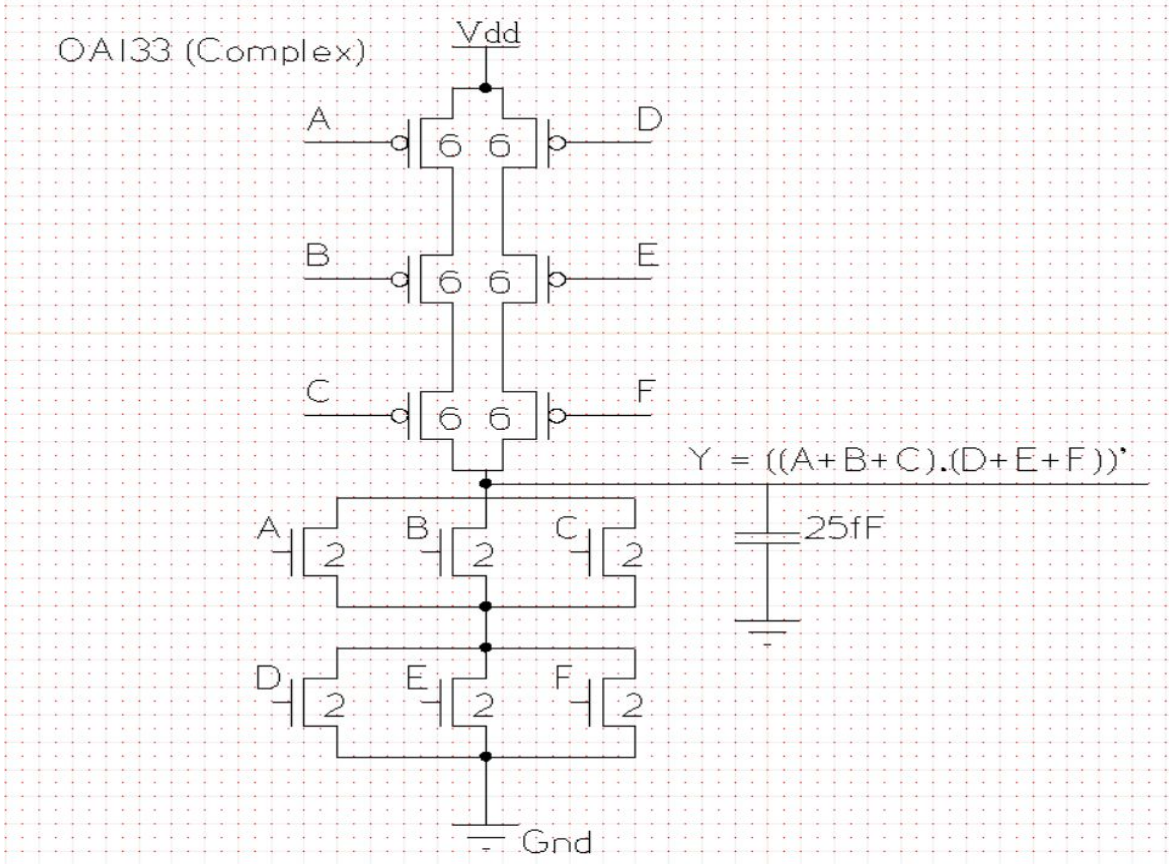
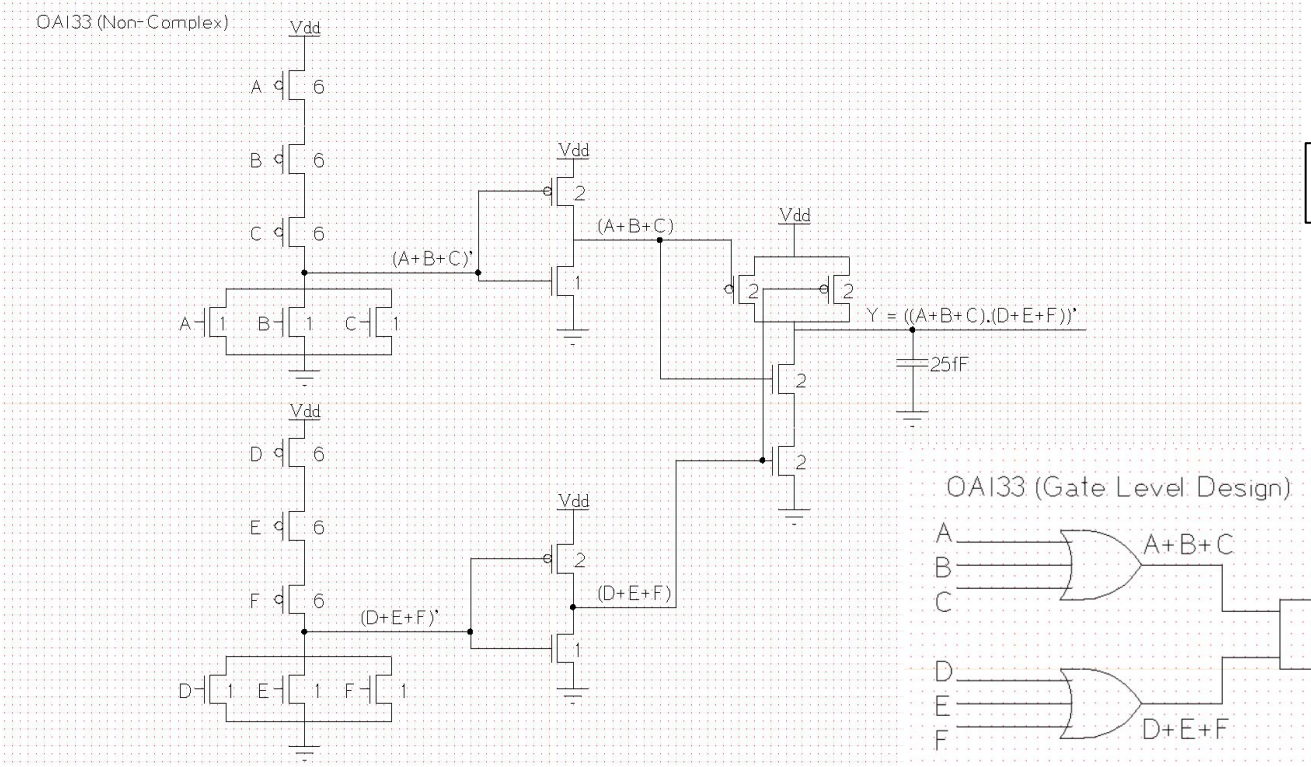
Schematic + Sizing (Complex) (1/2)



1u = 0.135µm
Size of PMOS = 0.81 um
Size of NMOS = 0.27 um

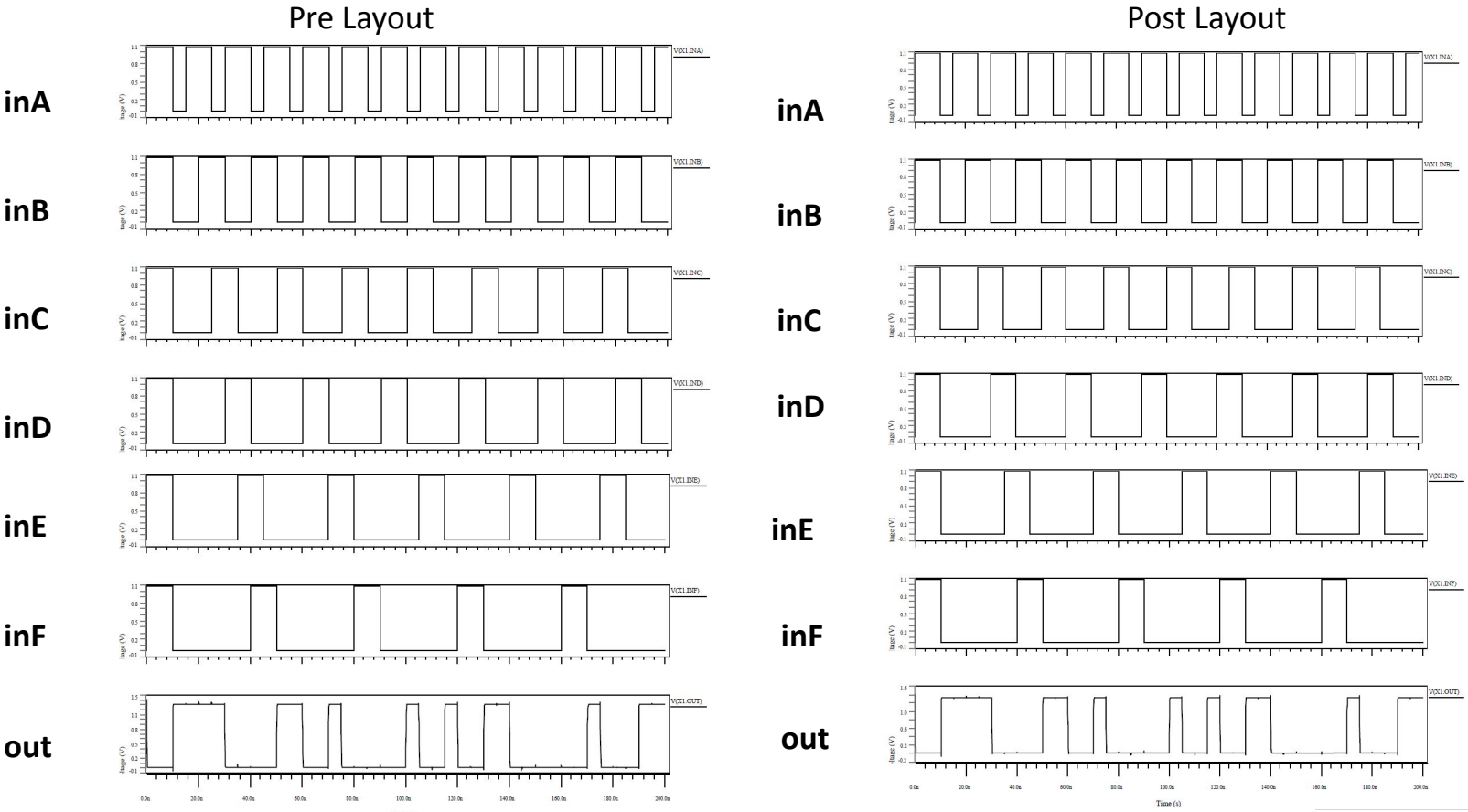
Schematic + Sizing (Non-Complex) (2/2)



1u = 0.135µm

Waveforms for Complex (1/2)

Y = ((A+B+C).(D+E+F))'

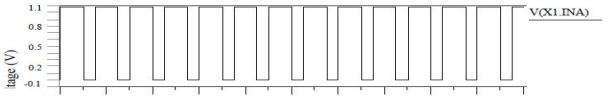


Waveforms for Non-Complex (2/2)

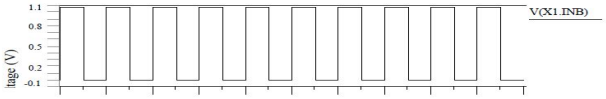
Y = ((A+B+C).(D+E+F))'

Pre Layout

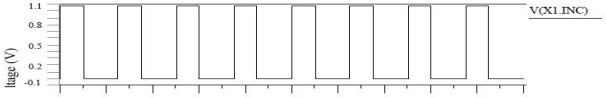
inA



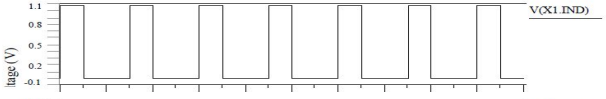
inB



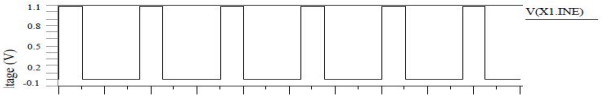
inC



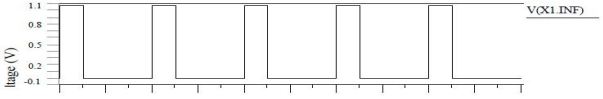
inD



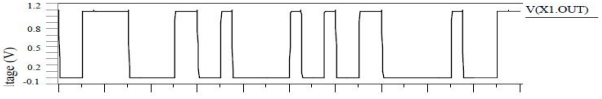
inE



inF

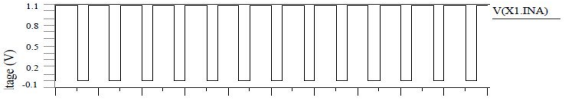


out

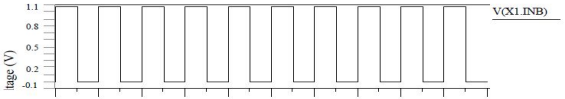


Post Layout

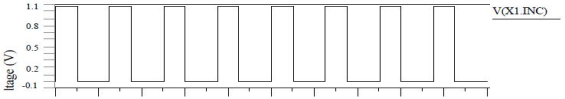
inA



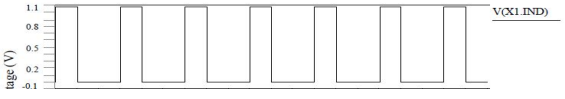
inB



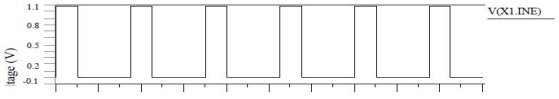
inC



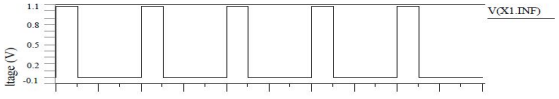
inD



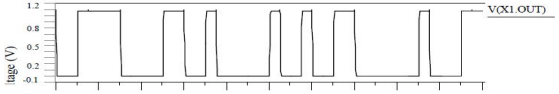
inE



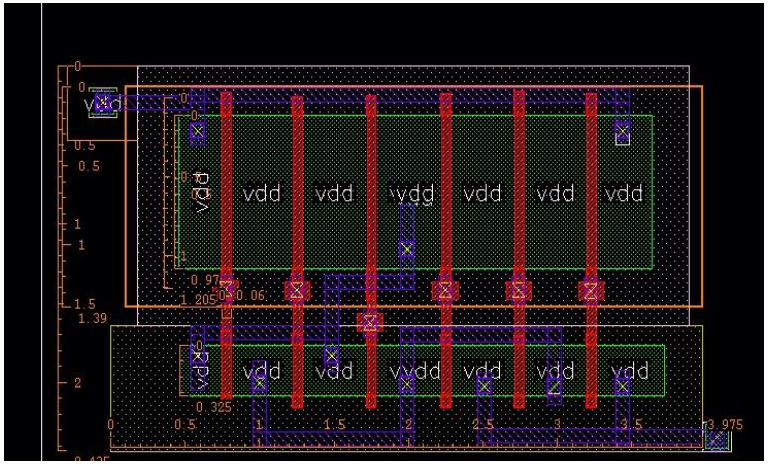
inF

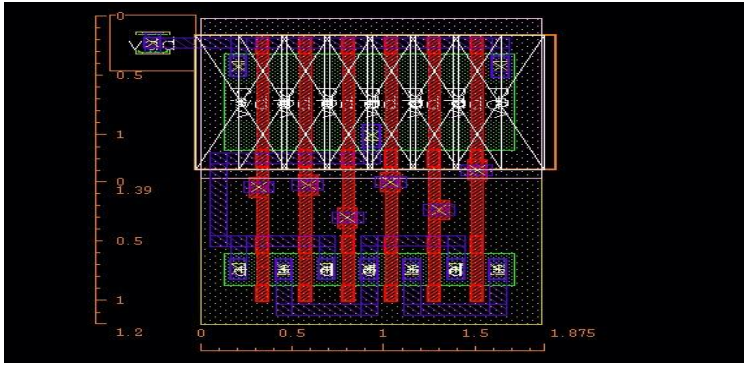


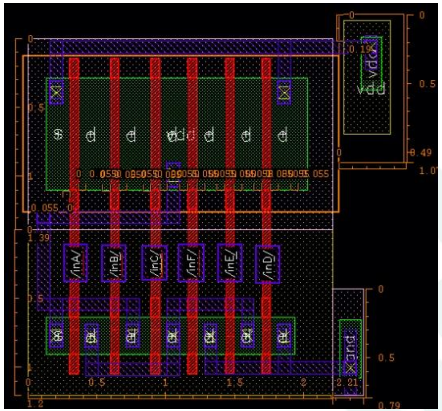
out



Challenges while Designing Layout (1/3)



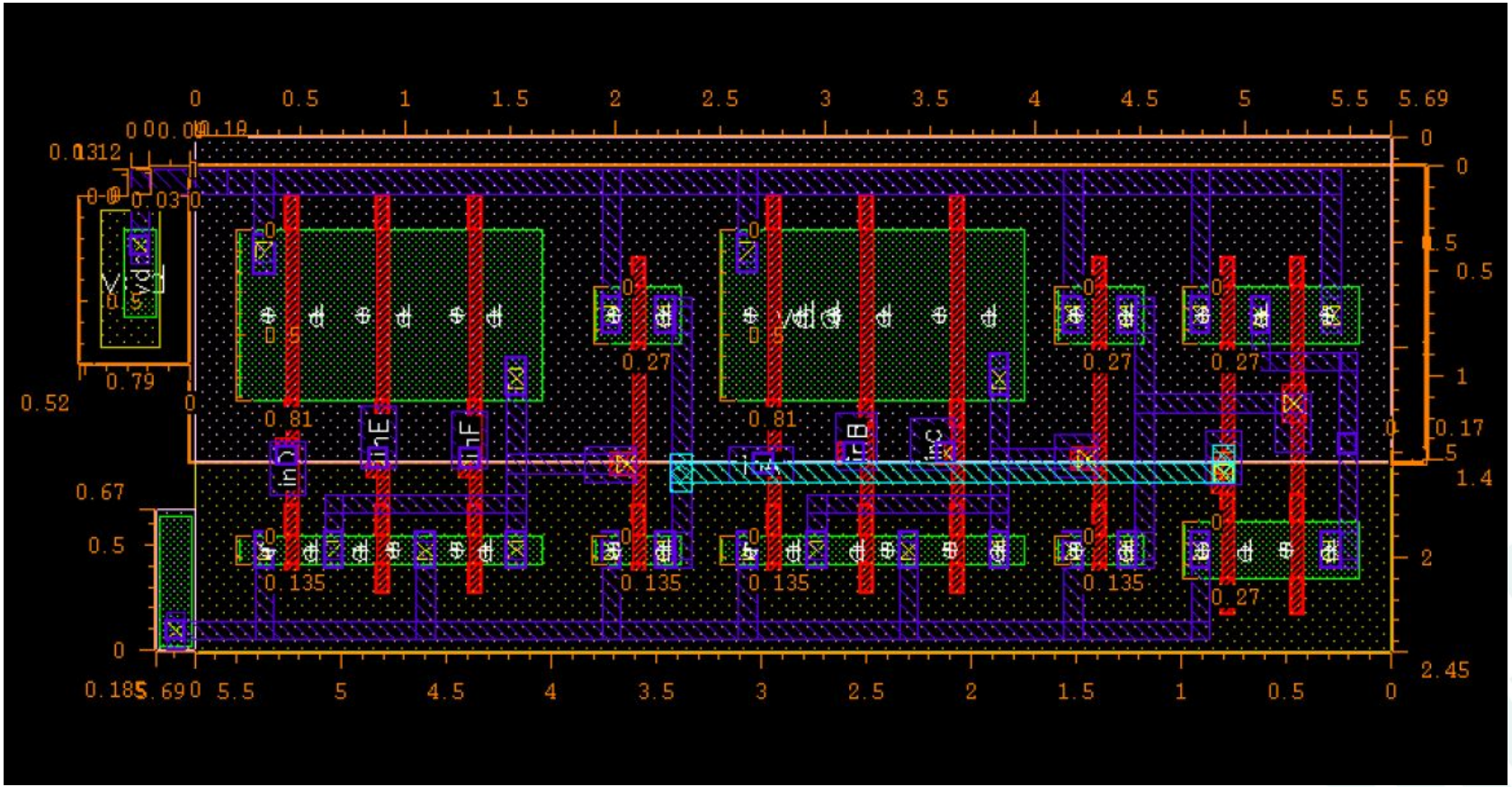




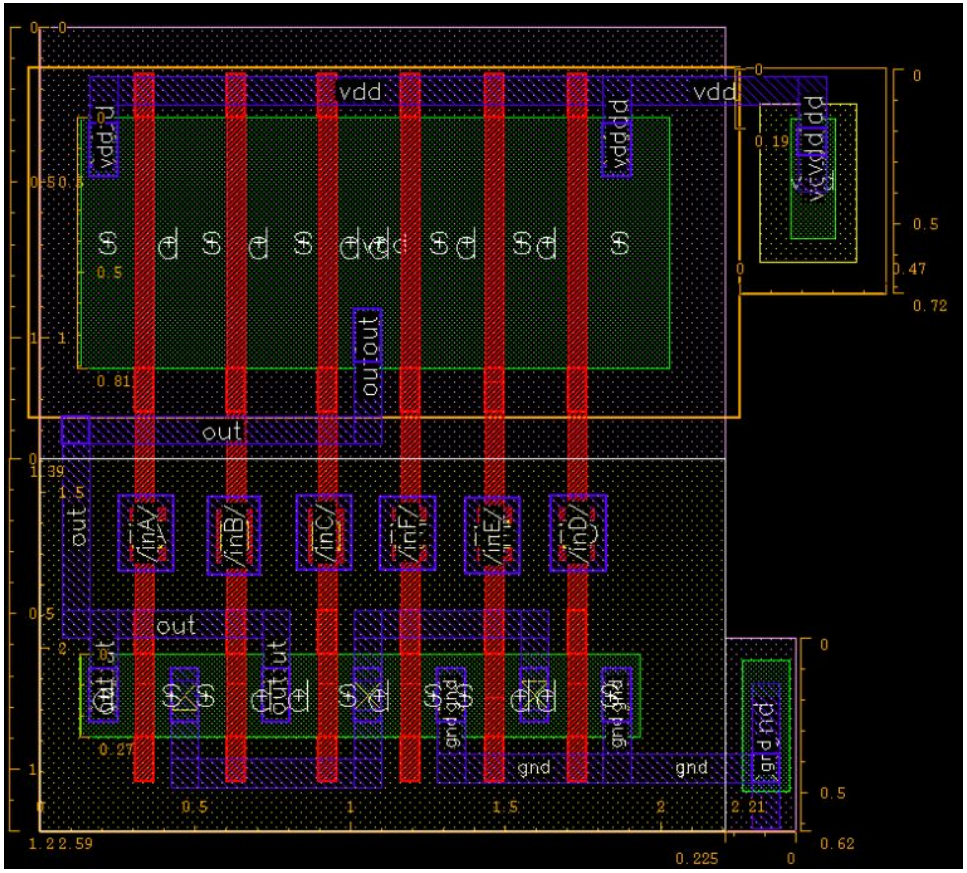
Our Learnings:

1. Each Source and drain should have a different OD layer and one common OD layer for all the PMOS/NMOS if shared together.
2. Making a custom layout helps us reduce Area and get minimum DRC errors.
3. The area occupied by input Vias(M1-PO) should be taken care of while creating the layout to avoid workload in future.
4. Dont use ChatGPT for Layout, it can increase the workload, asking Faculty, TAs and Seniors helps the most when you are stuck.

Layout (Non-Complex) (2/3)



Layout (Complex) (3/3)



Complex

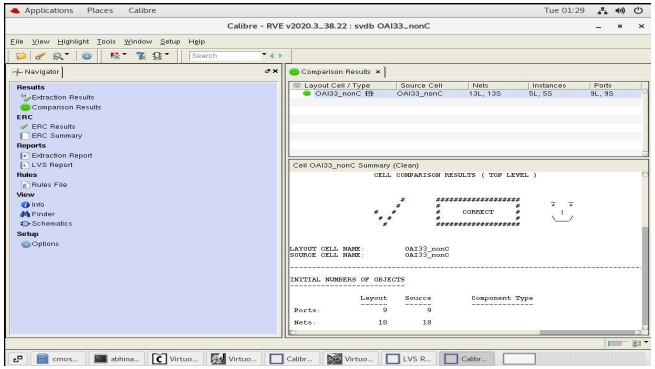
Area = 5.7239 µm^2 (excluding Vdd & Gnd Vias)
Total Area = 6.2018 µm^2

Non-Complex

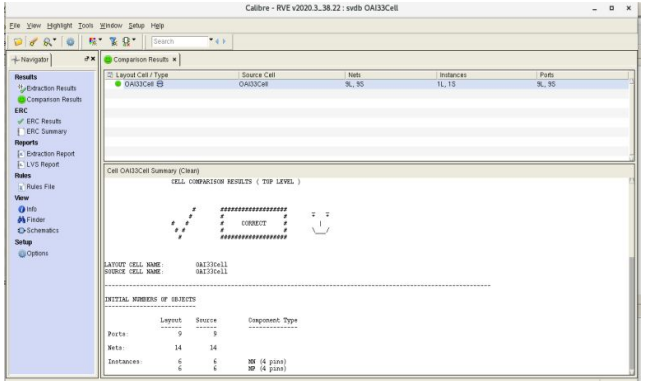
Area = 14.2365 µm^2 (excluding Vdd & Gnd Vias)
Total Area = 14.77018 µm^2

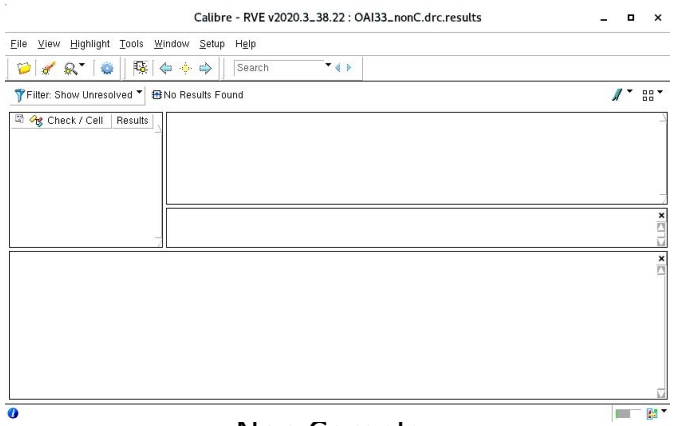
	Complex	Non Complex
Number of Transistors	12	20
Area	6.2018 µm^2	14.7712 µm^2
Height	13 tracks	13 tracks
Width	14 tracks	32 tracks

DRC, ERC and LVS Reports

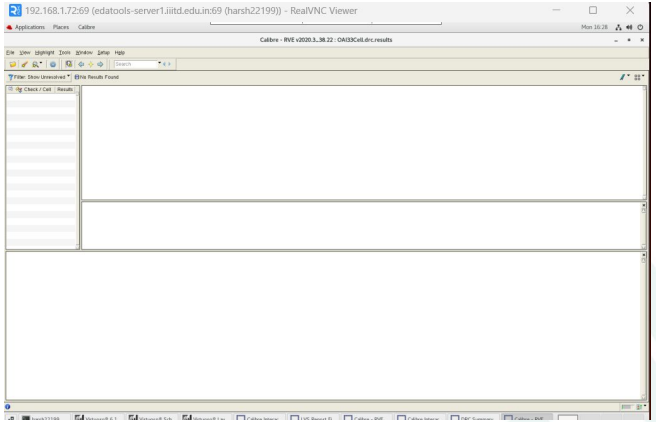


LVS & ERC Clean





DRC Clean



Non Complex

Complex

Verification Results (for all PVTs) tpd,tcd & power (1/2)

Pre Layout Simulations

PVT	tpd(ns)	tcd(ns)	Power(µW)
FF, 1.32V, -40C	0.049	0.021	1.99
FF, 1.32V, 125C	0.063	0.028	3.18
SS, 1.08V, 125C	0.111	0.051	1.43
SS, 1.08V, -40C	0.086	0.039	1.34

Complex

Post Layout Simulations

PVT	tpd(ns)	tcd(ns)	Power(µW)
FF, 1.32V, -40C	0.050	0.023	2.02
FF, 1.32V, 125C	0.066	0.029	3.22
SS, 1.08V, 125C	0.116	0.055	1.45
SS, 1.08V, -40C	0.090	0.042	1.37

PVT	tpd(ns)	tcd(ns)	Power (µW)
FF, 1.32V, -40C	0.079	0.044	2.28
FF, 1.32V, 125C	0.100	0.056	4.05
SS, 1.08V, 125C	0.213	0.123	1.63
SS, 1.08V, -40C	0.171	0.099	1.53

Non Complex

PVT	tpd(ns)	tcd(ns)	Power(µW)
FF, 1.32V, -40C	0.080	0.044	2.30
FF, 1.32V, 125C	0.101	0.056	4.07
SS, 1.08V, 125C	0.214	0.124	1.65
SS, 1.08V, -40C	0.172	0.100	1.55

Verification Results (for all PVTs) tfall & trise (2/2)

Pre Layout Simulations

PVT	tfall(ns)	trise(ns)
FF, 1.32V, -40C	0.059	0.065
FF, 1.32V, 125C	0.074	0.082
SS, 1.08V, 125C	0.117	0.16
SS, 1.08V, -40C	0.076	0.1399

Post Layout Simulations

PVT	tfall(ns)	trise(ns)
FF, 1.32V, -40C	0.0613	0.067
FF, 1.32V, 125C	0.074	0.085
SS, 1.08V, 125C	0.12	0.17
SS, 1.08V, -40C	0.077	0.14

Complex

PVT	tfall(ns)	trise(ns)
FF, 1.32V, -40C	0.095	0.061
FF, 1.32V, 125C	0.137	0.073
SS, 1.08V, 125C	0.309	0.120
SS, 1.08V, -40C	0.230	0.106

Non Complex

PVT	tfall(ns)	trise(ns)
FF, 1.32V, -40C	0.095	0.062
FF, 1.32V, 125C	0.138	0.074
SS, 1.08V, 125C	0.313	0.123
SS, 1.08V, -40C	0.235	0.106

Analysis

	PVTs
Best Case (TCD)	FF, 1.32V, -40C
Worst Case (TPD)	SS, 1.08V, 125C
Worst Power	FF, 1.32V, 125C

	Complex	Non Complex
Number of Transistors	**12**	**20**
Area	**6.2018 μm^2**	**14.7712 μm^2 (2.3x Complex)**
Power	**Less**	**More (1.2x for FF,125,1.32)**
Delays	**Less**	**More**

Work Distribution

Present Work Distribution (after mid sem presentation)

Complex Layout - Abhinav Kumar Saxena, Harsh Nangia
Non Complex Layout - Abhinav Kumar Saxena, Akanksh Semar, Harsh Nangia, Kunal
Simulations Complex Post Layout - Abhinav Kumar Saxena, Akanksh Semar, Harsh Nangia, Kunal
Simulations Non Complex Post Layout - Abhinav Kumar Saxena, Harsh Nangia, Kunal

Previous Work Distribution (Midsem Presentation)

Schematics + Sizing for Complex - Cumulative Efforts
Schematics + Sizing for Non Complex - Cumulative Efforts
Stick Diagram for Complex - Abhinav Kumar Saxena, Akanksh Semar, Kunal
Stick Diagram for Non Complex - Kunal, Harsh Nangia, Akanksh Semar
Simulations Complex PreLayout - Abhinav Kumar Saxena, Harsh Nangia, Kunal
Simulations Non Complex PreLayout - Abhinav Kumar Saxena, Akanksh Semar, Harsh Nangia, Kunal