

Power

hnaderi.dev

Sheet: /Power/

File: power.kicad_sch

Title: HNaderi's PLL SSTC

Size: A4

Date:

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Rev: 2

Id: 2/5



The layout of this circuit is of crucial importance!
It must have very low inductance in order to reduce
high voltage transients due to parasitic
oscillations.
Prefer wide overlapping planes for high current
traces over thin wires.

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Sheet: /Inverter/
File: inverter.kicad_sch

Title: HNaderi's PLL SSTC

Size: A4
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Date:

Rev: 2

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Sheet: /Interrupter/

File: interrupter.kicad_sch

Title: HNaderi's PLL SSTC

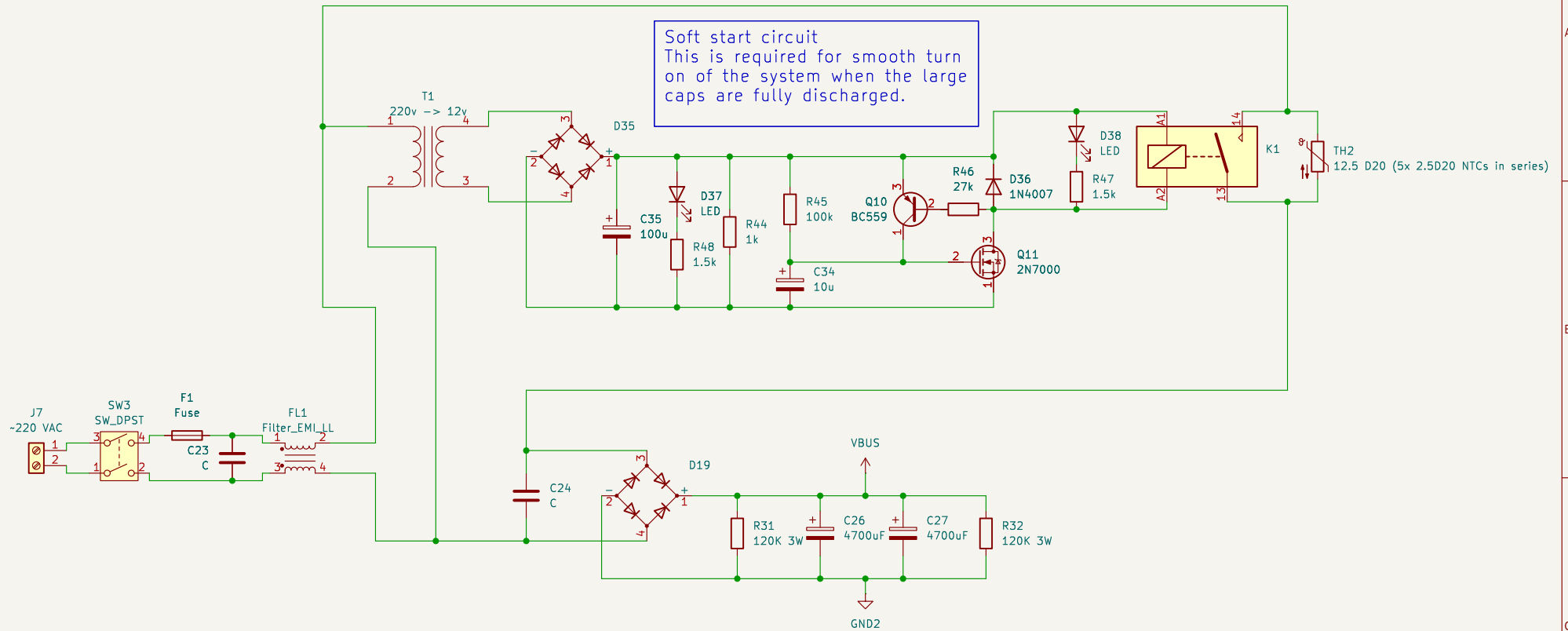
Size: A4

Date:

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Sheet: /Rectifier/

File: rectifier.kicad_sch

Title: HNaderi's PLL SSTC

Size: A4

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Rev: 2

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