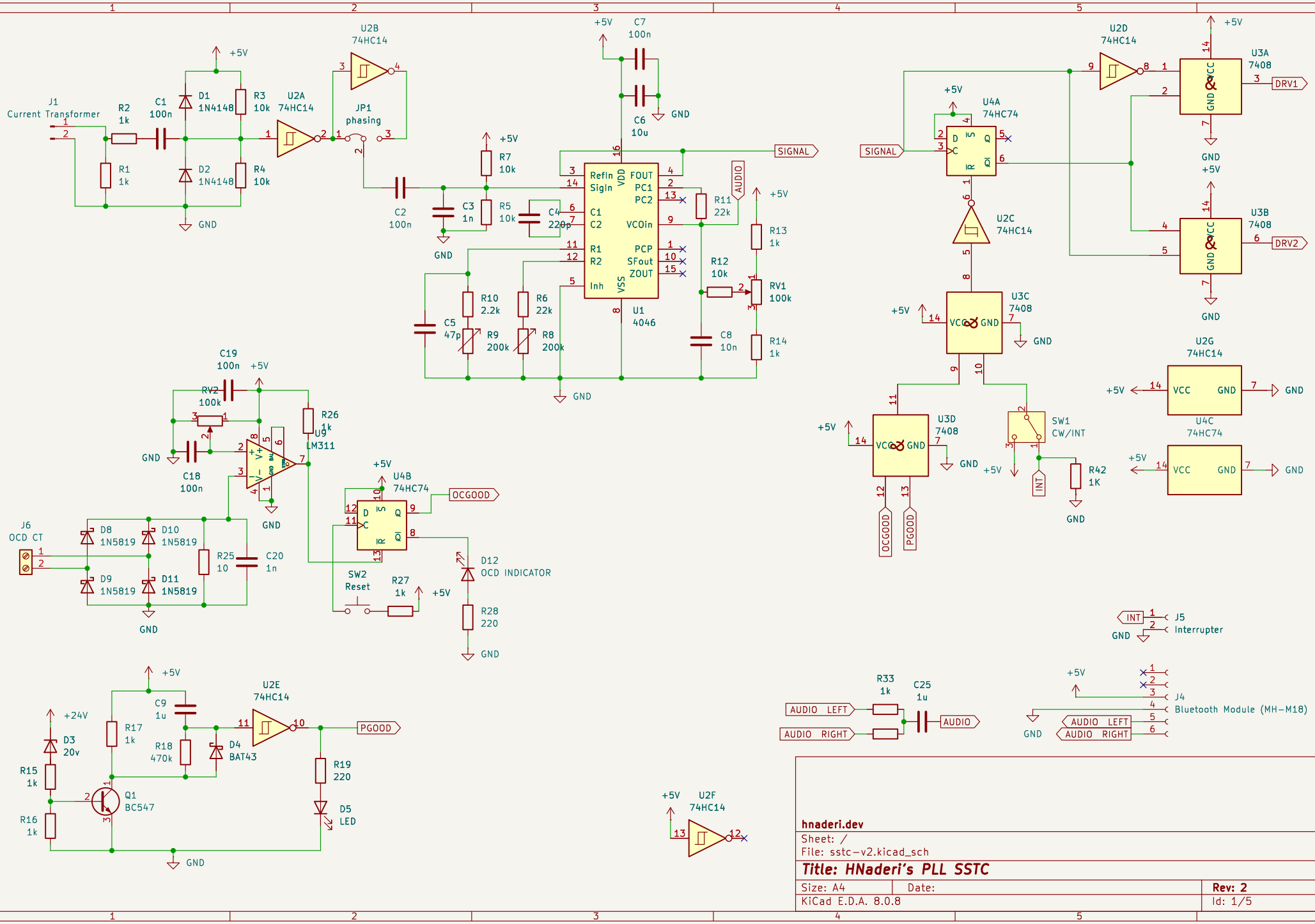
J1
Current Transformer
R2
1k
C1
100n
D1
1N4148
D2
1N4148
R3
10k
R4
10k
R1
1k
U2A
74HC14
U2B
74HC14
JP1
phasing
C2
100n
+5V
GND
C7
100n
C6
10u
SIGNAL
R7
10k
C3
1n
R5
10k
C4
220p
RefIn
SigIn
VDD
FOUT
PC1
PC2
C1
C2
VCOin
R1
R2
PCP
SFout
ZOUT
Inh
VSS
U1
4046
AUDIO
R11
22k
R12
10k
RV1
100k
R13
1k
R14
1k
R10
2.2k
R6
22k
C5
47p
R9
200k
R8
200k
C8
10n
U2D
74HC14
U4A
74HC74
U2C
74HC14
U3A
7408
U3B
7408
U3C
7408
DRV1
DRV2
U3D
7408
SW1
CW/INT
R42
1K
INT
OCGOOD
PGOOD
U2G
74HC14
U4C
74HC74
VCC
GND
C19
100n
RV2
100k
C18
100n
R26
1k
U9
LM311
J6
OCD CT
D8
1N5819
D10
1N5819
D9
1N5819
D11
1N5819
R25
10
C20
1n
U4B
74HC74
OCGOOD
SW2
Reset
R27
1k
D12
OCD INDICATOR
R28
220
J5
Interrupter
R33
1k
C25
1u
AUDIO LEFT
AUDIO RIGHT
AUDIO
J4
Bluetooth Module (MH-M18)
+24V
D3
20v
R15
1k
R16
1k
R17
1k
C9
1u
R18
470k
D4
BAT43
Q1
BC547
U2E
74HC14
PGOOD
R19
220
D5
LED
U2F
74HC14
hnaderi.dev
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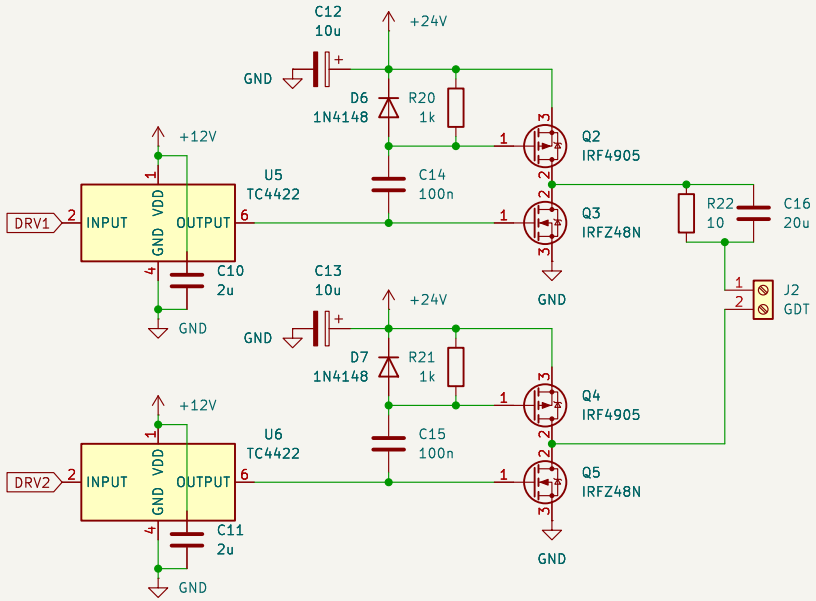
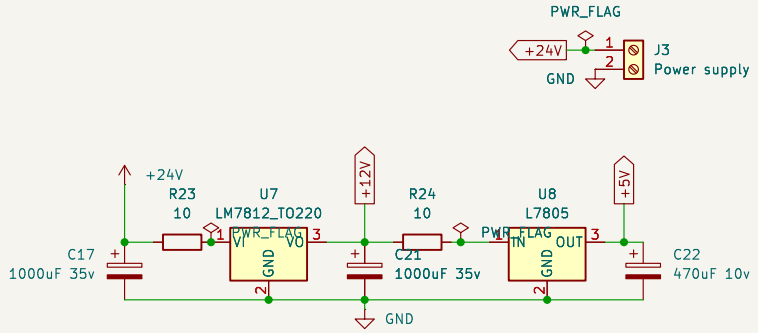
Size: A4
Date:
Rev: 2
KiCad E.D.A. 8.0.8
Id: 1/5





Power
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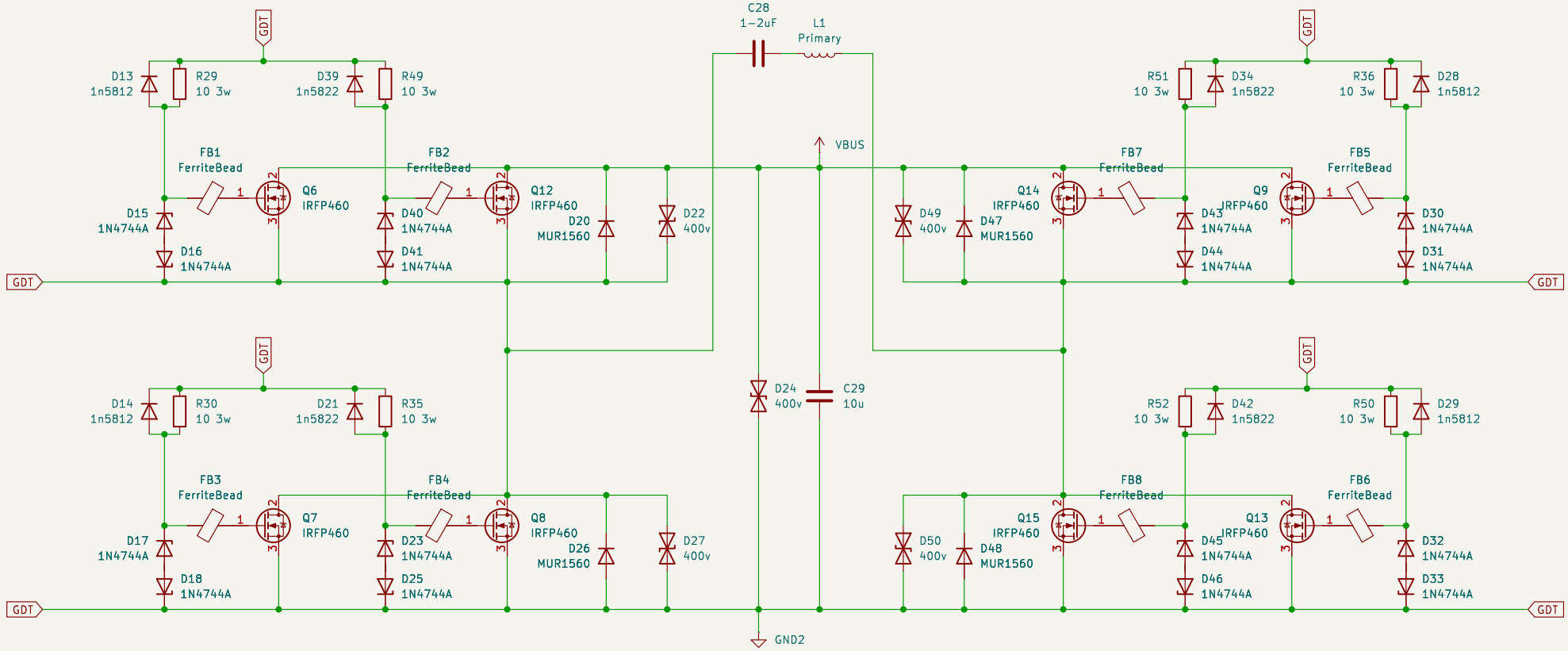
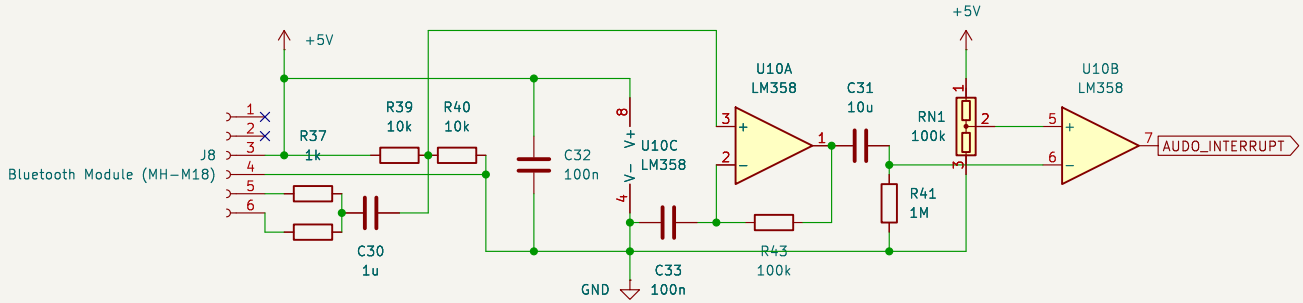
Title: HNaderi's PLL SSTC

Size: A4	Date:	**Rev: 2**
KiCad E.D.A. 8.0.8		Id: 2/5



The layout of this circuit is of crucial importance!
It must have very low inductance in order to reduce high voltage transients due to parasitic oscillatiions.
Prefer wide overlapping planes for high current traces over thin wires.

hnaderi.dev		
Sheet: /Inverter/		
File: inverter.kicad_sch		
Title: HNaderi's PLL SSTC		
Size: A4	Date:	**Rev: 2**
KiCad E.D.A. 8.0.8		Id: 3/5



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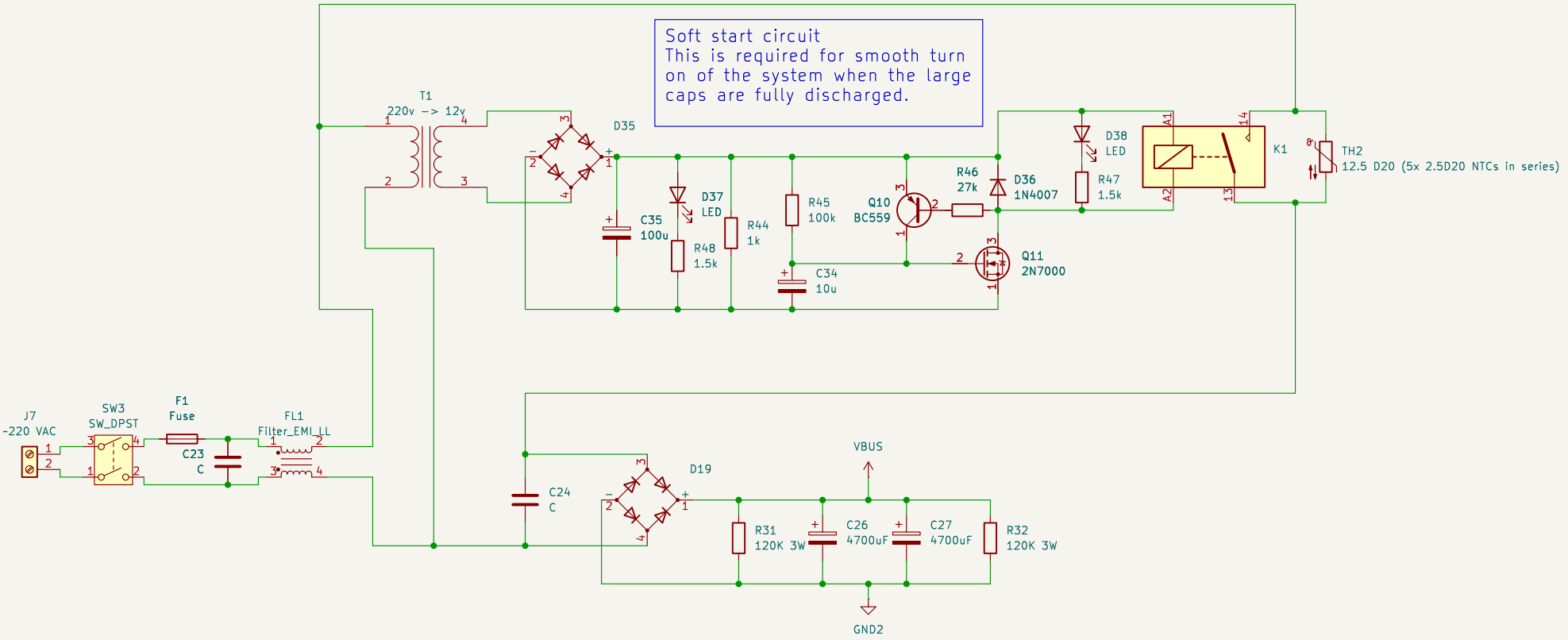
Size: A4	Date:	**Rev: 2**
KiCad E.D.A. 8.0.8		Id: 4/5



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Size: A4	Date:	**Rev: 2**
KiCad E.D.A. 8.0.8		Id: 5/5