A tailor-made checker for specific DV challenges

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SNUG Taiwan

Agenda

Interface Signals

Ultra/Flush Signal Pair

Verification difficulties

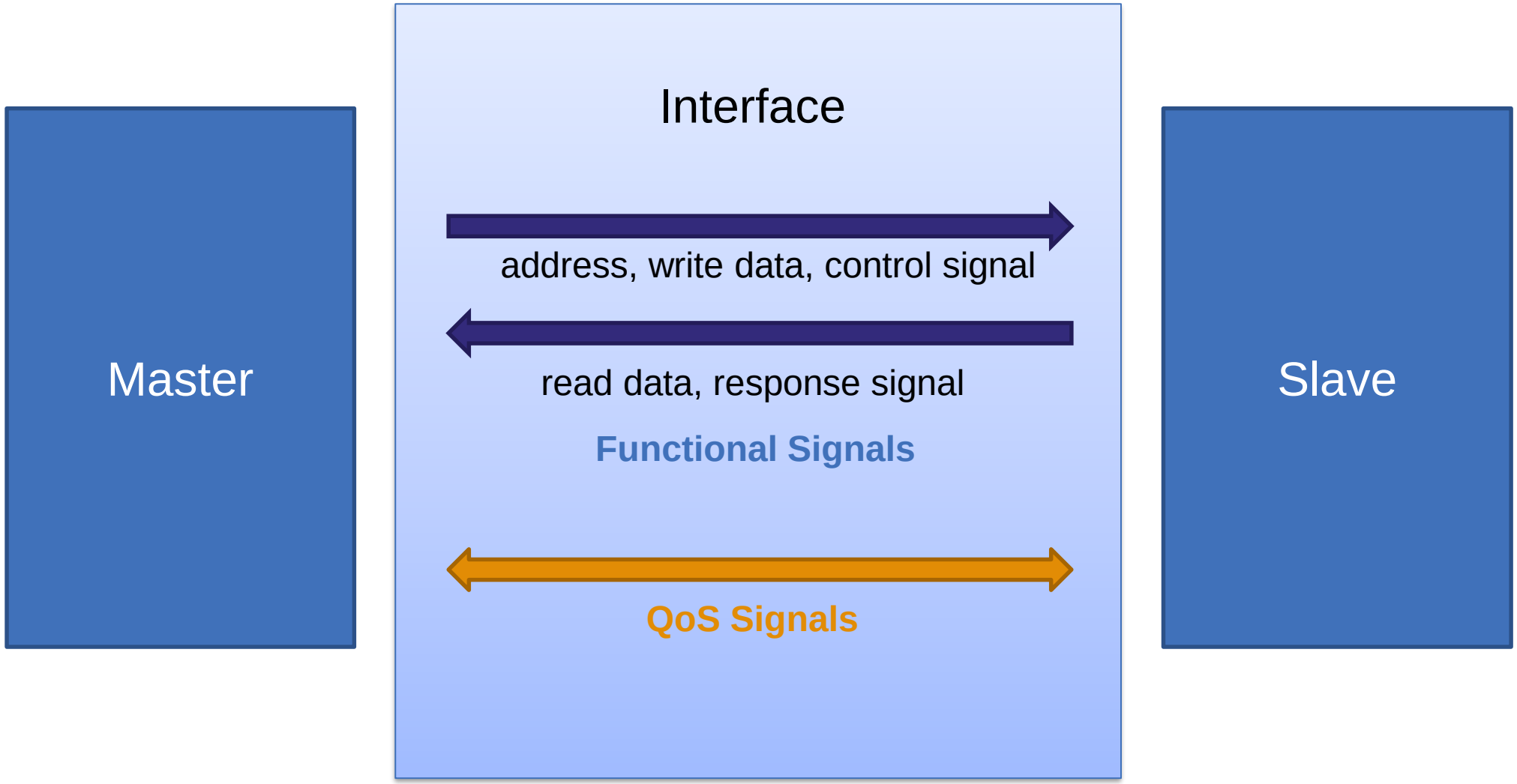
VC App Solution

Experiment Result

Conclusion

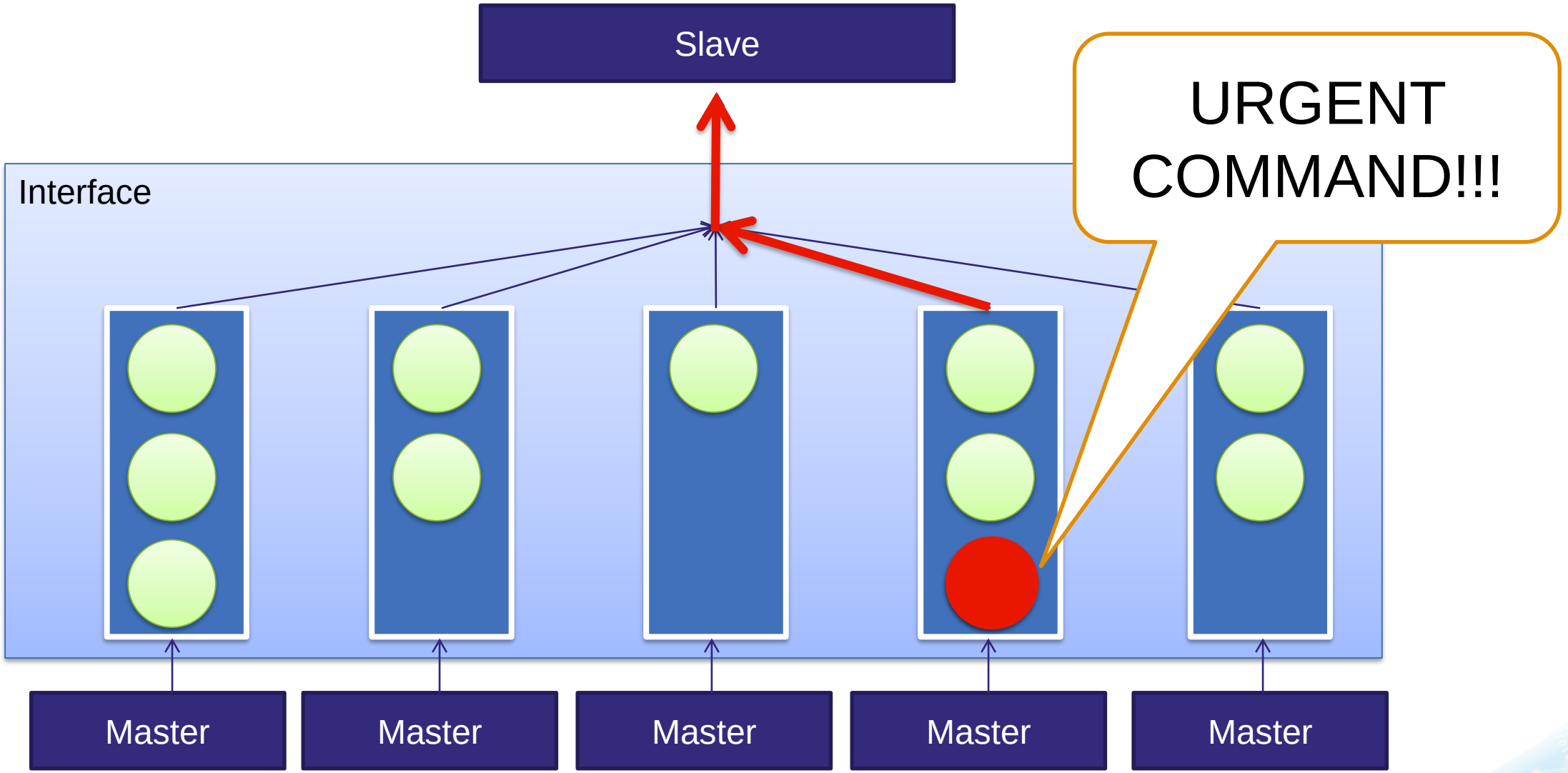
Future Work

Interface signals

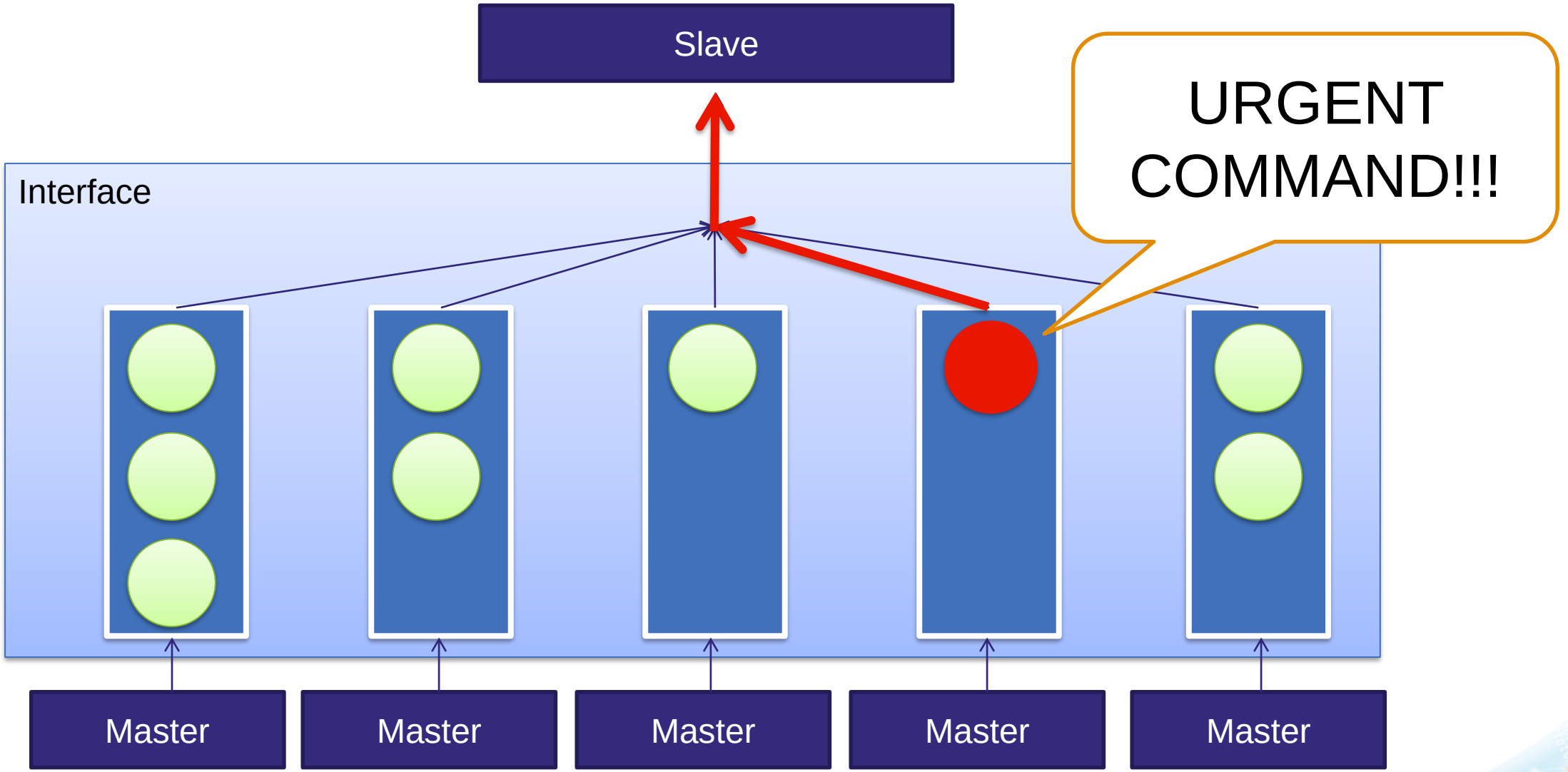


Ultra/Flush Signal Pair

Ultra/Flush Signal Pair



Ultra/Flush Signal Pair



Ultra/Flush Signal Pair

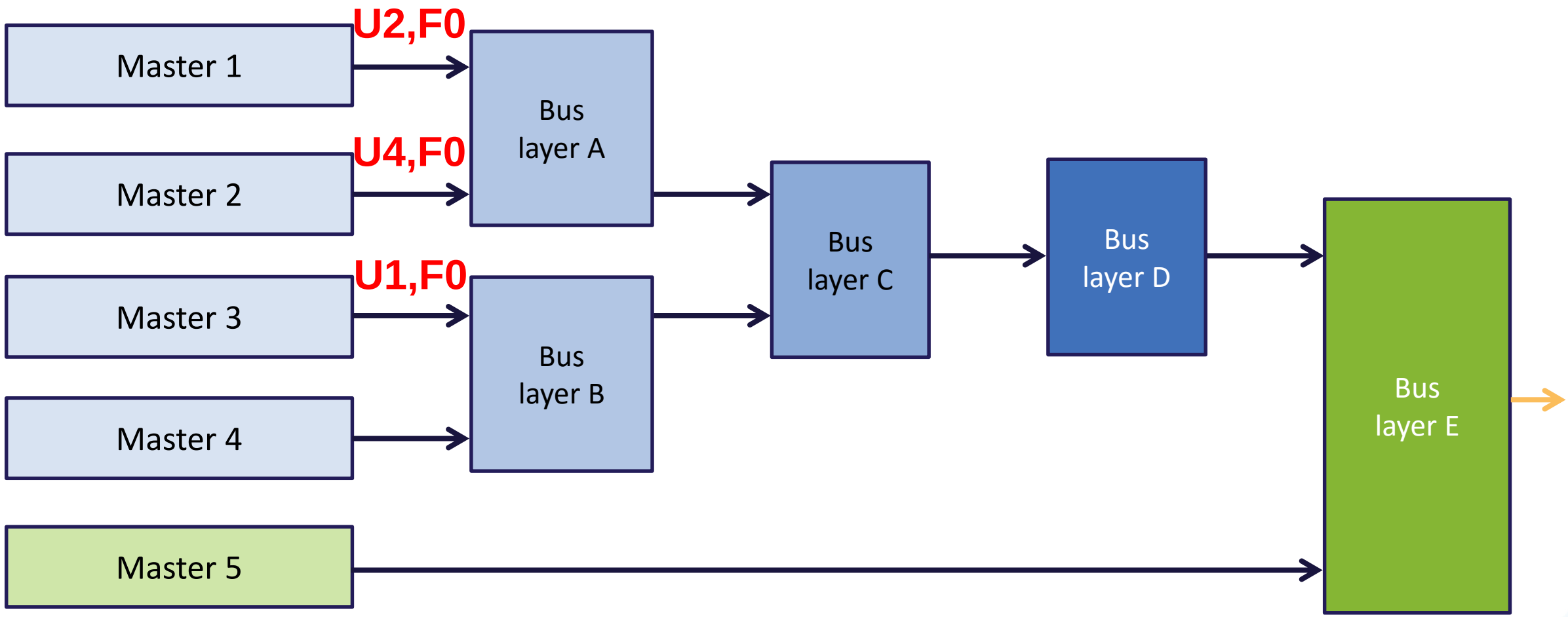
- ultra
  - Generated by Master
  - Priority indicator
- flush
  - Generate by Queue/Arbiter
  - Indicate preceding low priority command block following high priority command
- One-hot signaling

ultra[3:0]
- 1xxx = U8; 01xx = U4; 001x = U2; 0001= U1;
- Priority: U8 > U4 > U2 > U1

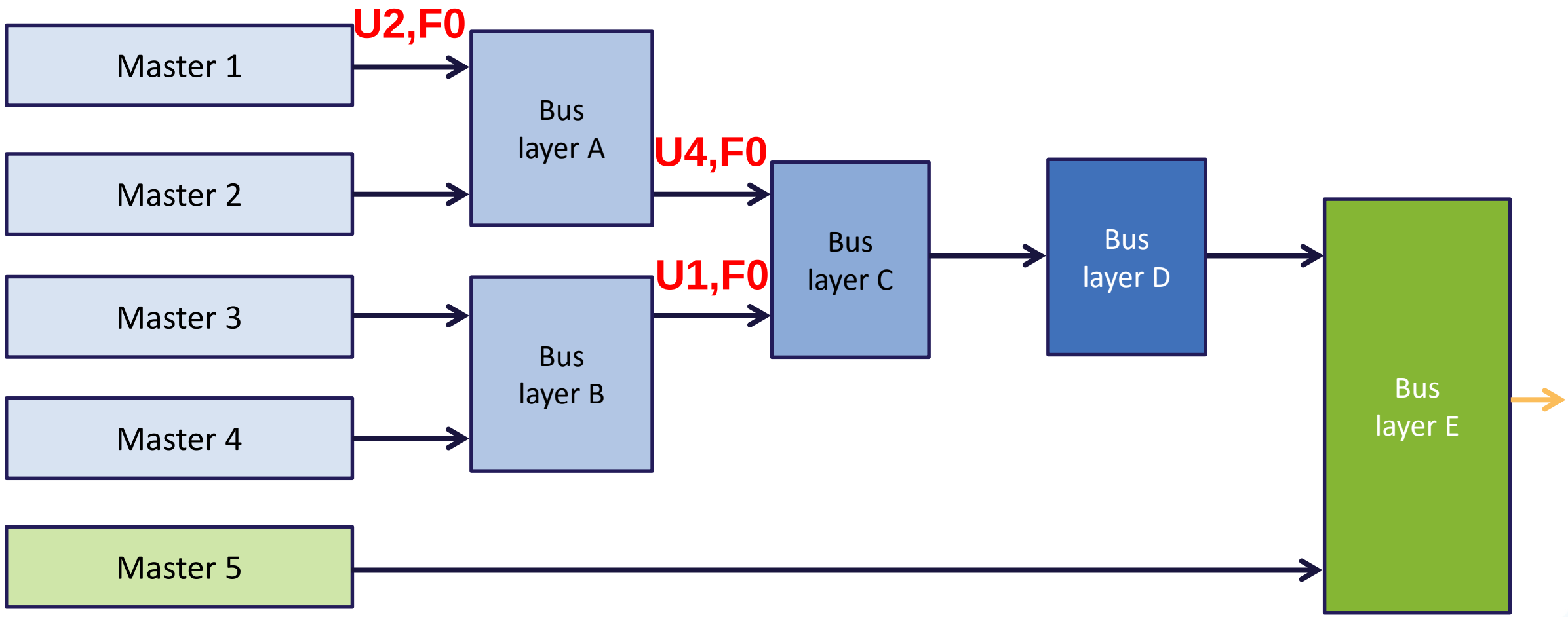
flush[3:0]
- 1xxx = F8; 01xx = F4; 001x = F2; 0001= F1;
- Priority: F8 > F4 > F2 > F1

ultra[3:0] ⇔ flush[3:0]
- U8 = F8, U4 = F4, U2 = F2, U1 = F1

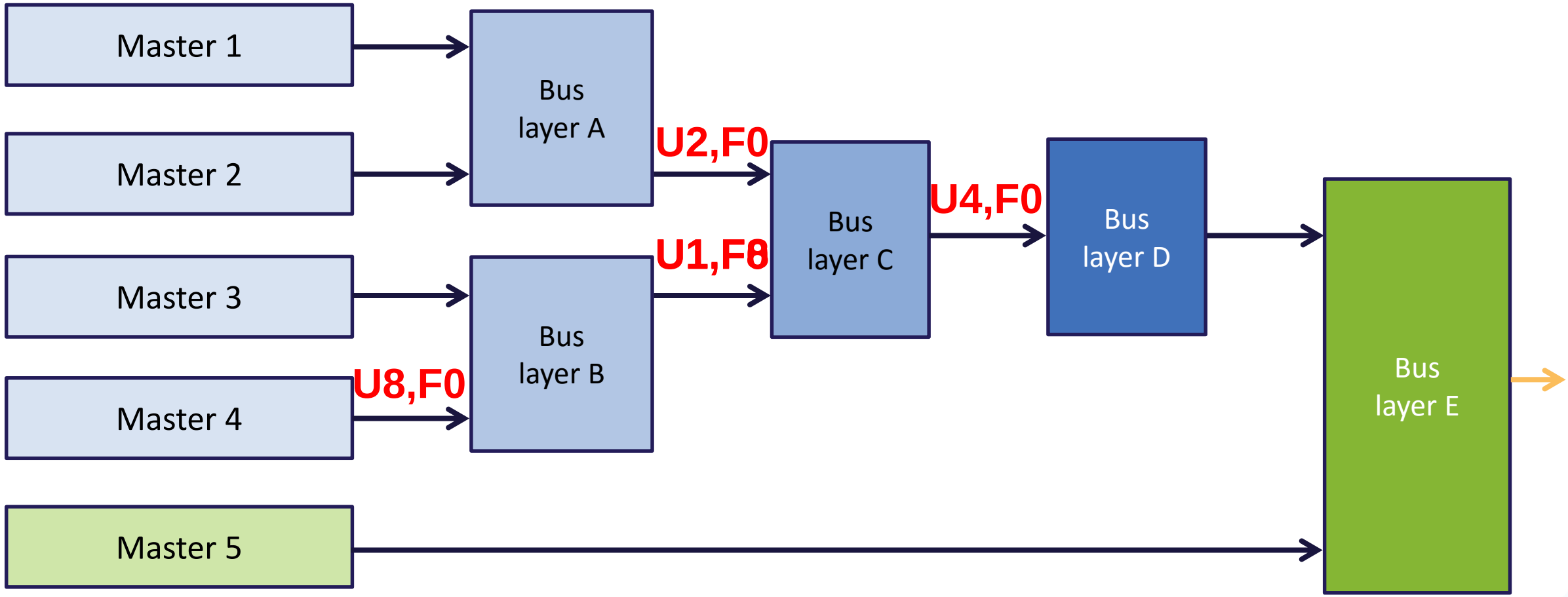
Ultra/Flush Example



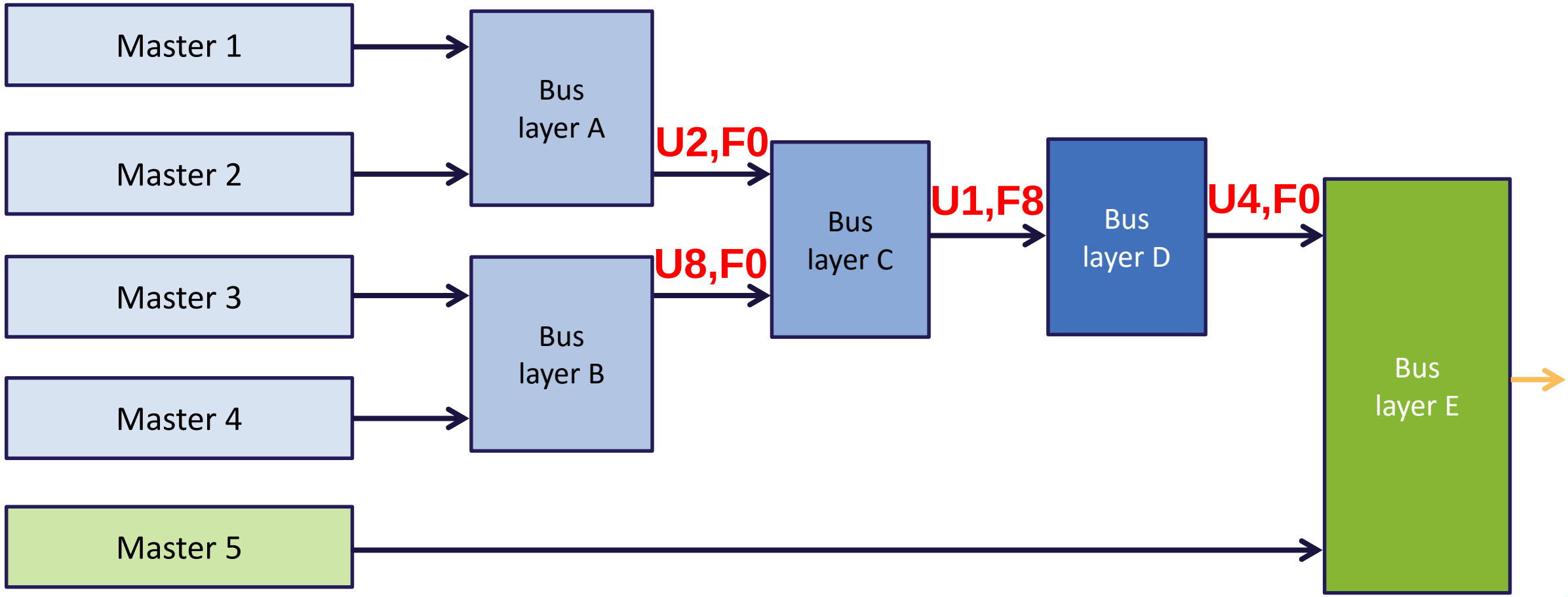
Ultra/Flush Example



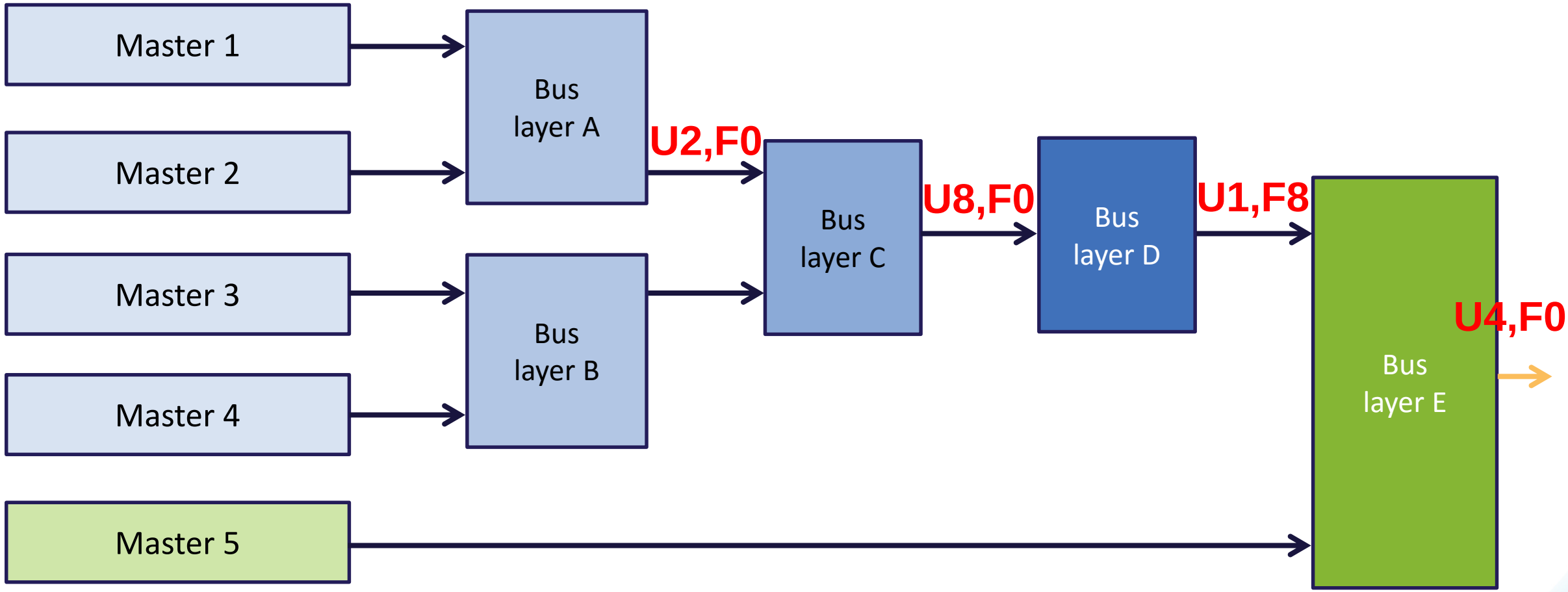
Ultra/Flush Example



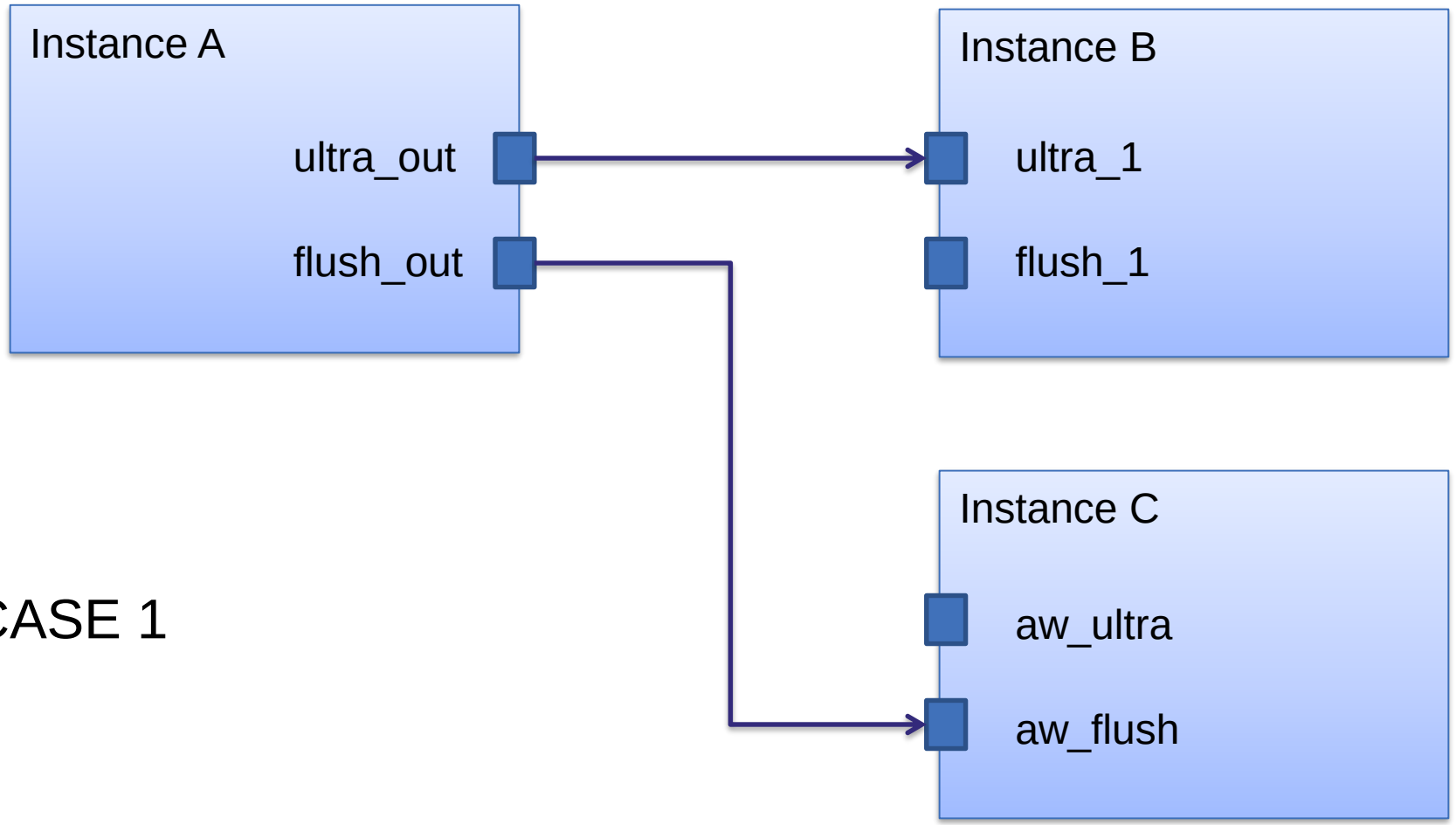
Ultra/Flush Example



Ultra/Flush Example

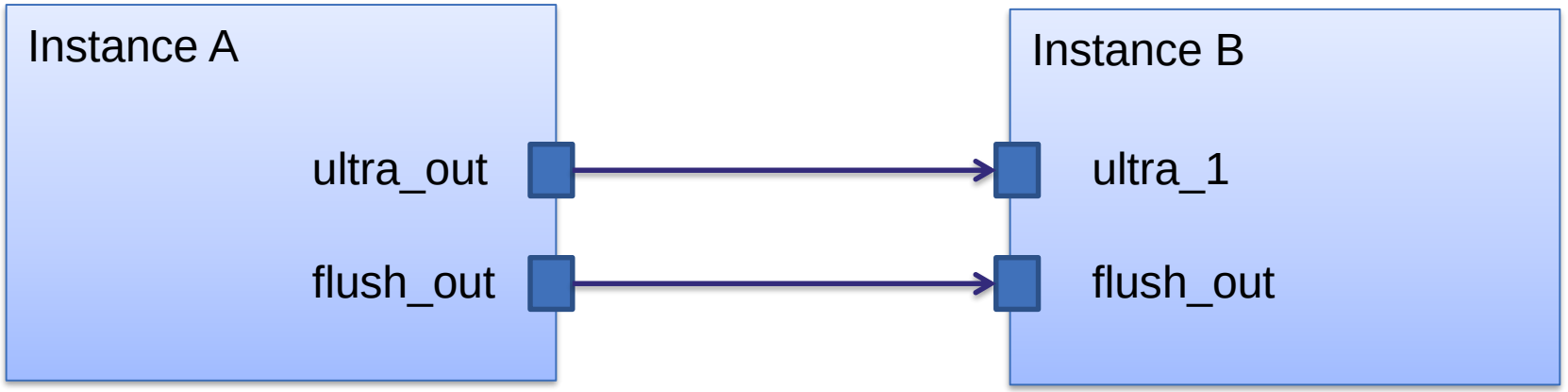


Existing Threats

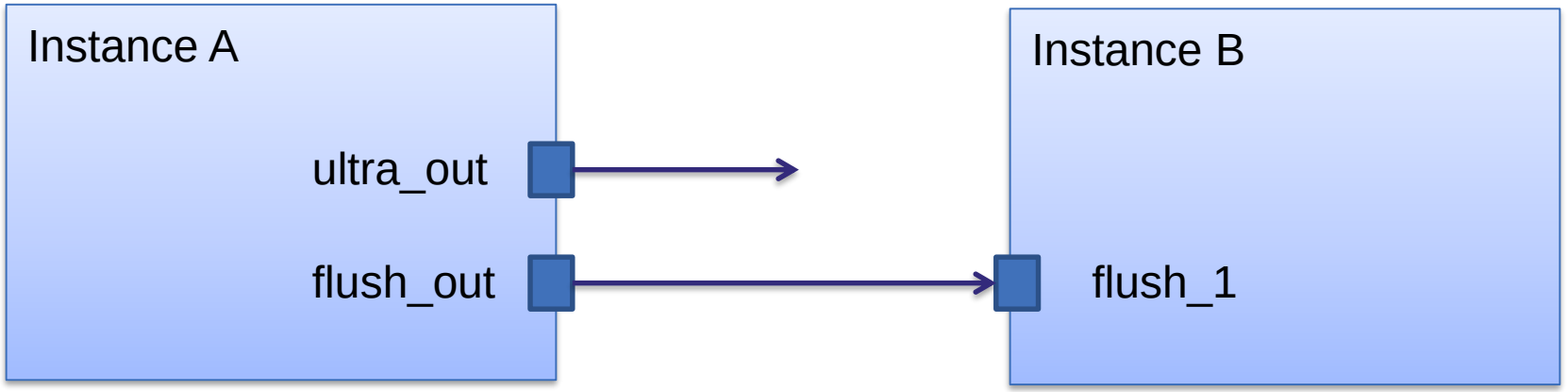


Existing Threats

CASE 2



CASE 3



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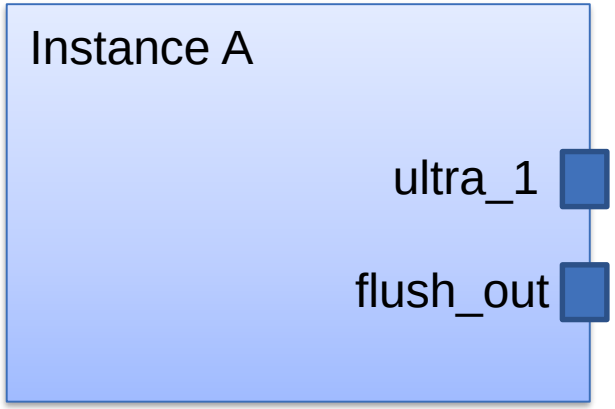
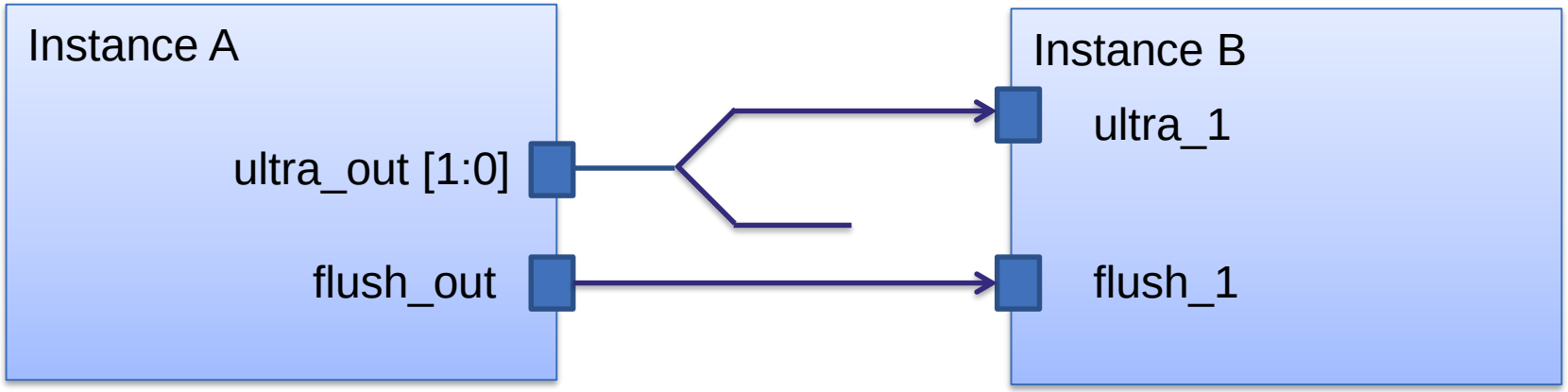
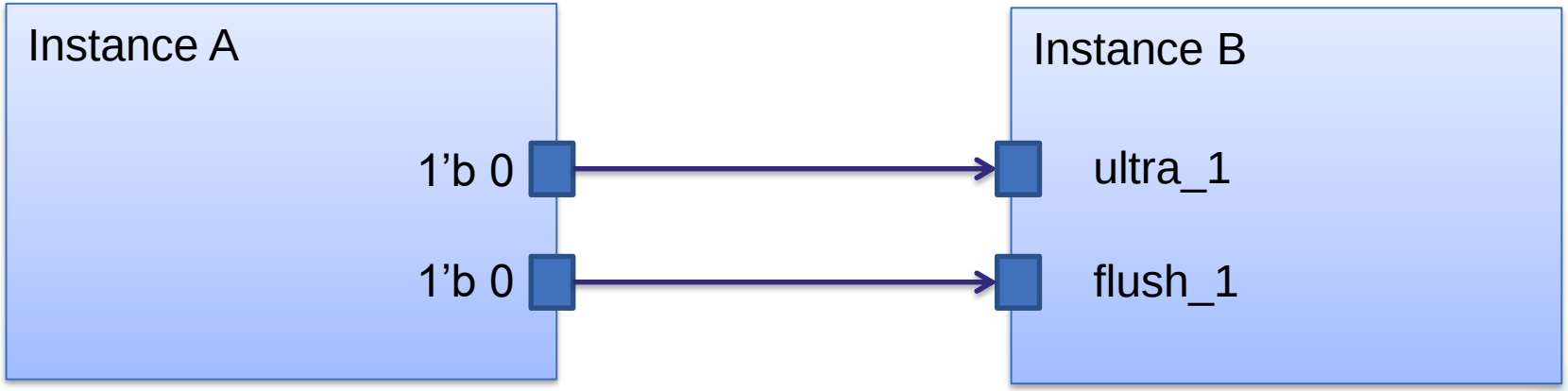


CASE 4



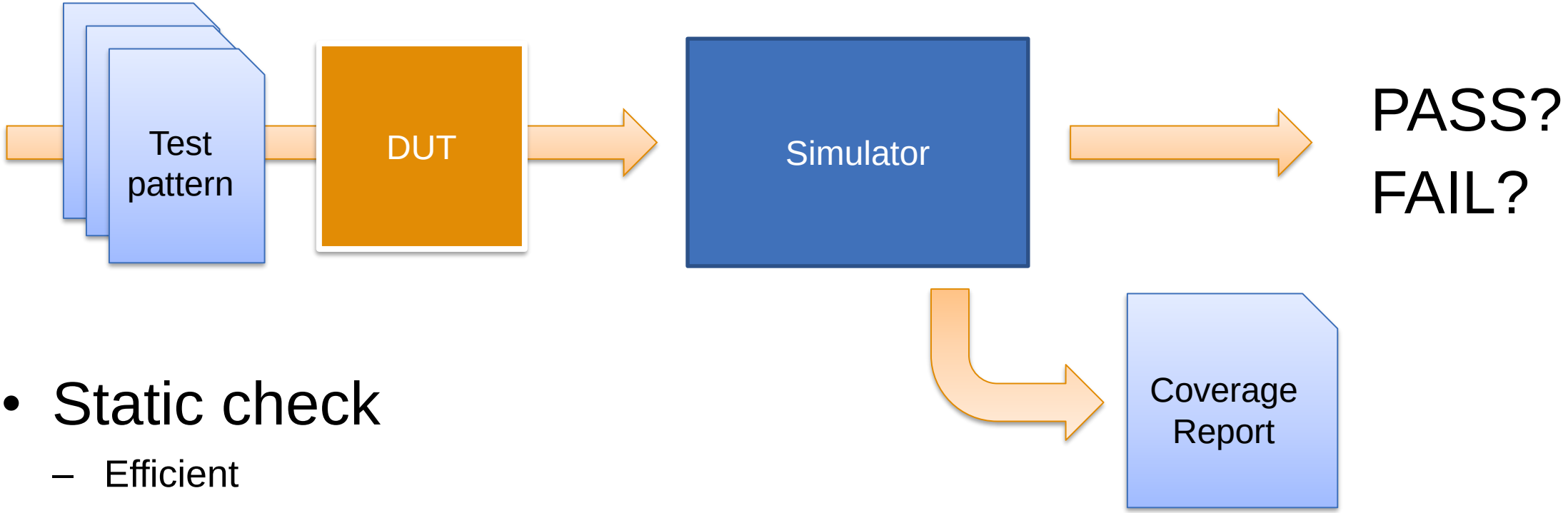
CASE 5



CASE 6

Verification difficulties

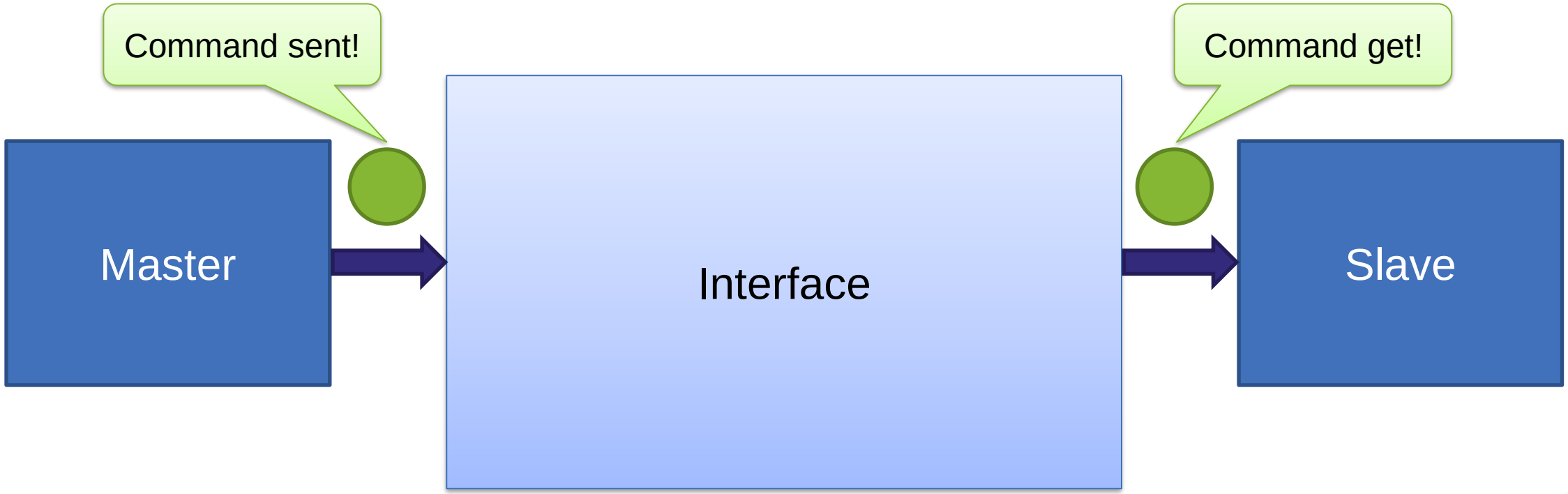
- When simulation based verification is not good enough …



- Static check
  - Efficient
  - Reliable

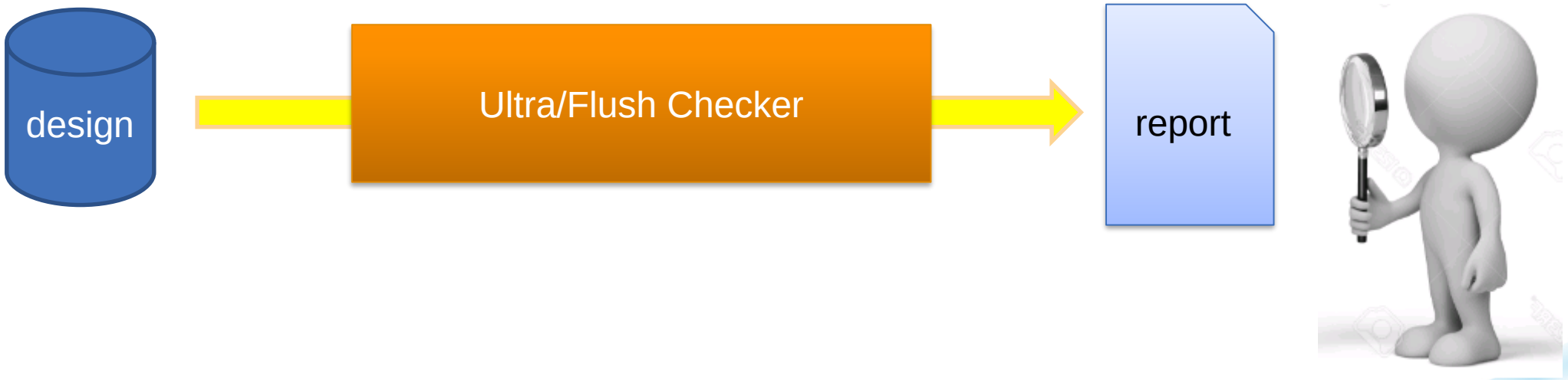
Verification difficulties

- Verification difficulties
  - QoS signals don’t affect simulation outcome
  - Flush signal values are generated by interface depending on the bus traffic



VC App Solution

- Static Connectivity Check
- Treat Ultra as golden
- Verification goals
  - Ultra and Flush must connect to the same destination
  - Ultra and Flush must be pairs
  - Tied constant scenarios must be reviewed



Step-by-Step

Ultra/Flush Checker

Finding target modules

Signal pair identification

Connectivity Checking

Report generation

Step-by-Step

- Finding Target Modules
  - Search for all the modules that contain ultra signals
  - Exclude modules from the exclude file for efficiency

- Identifying Ultra/Flush signal pairs

prefix**ultra**suffix [input [WIDTH-1:0]] => prefix**flush**suffix [input [WIDTH-1:0]]

h**ultra**_m [input [3:0]] => h**flush**_m [input [3:0]]

ultra_s [output [1:0]] => **flush**_s [output [1:0]]

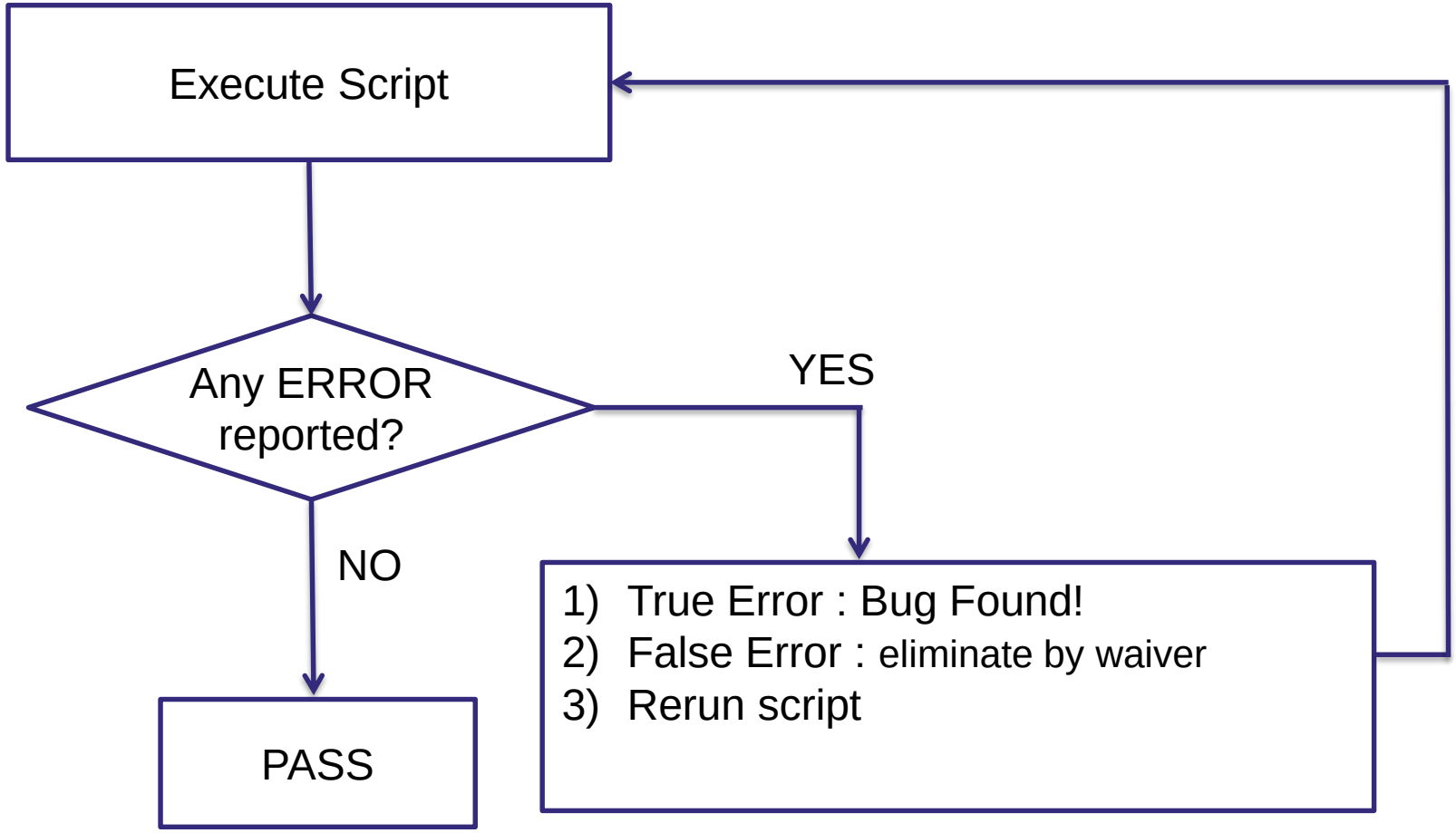
m1_aw**ultra** [input [3:0]] => m1_aw**flush** [input [3:0]]

Step-by-Step

- Connectivity check
  - We treat Ultra signals as golden
  - Use VC App functions to trace the destination of a Ultra signal, then check its corresponding flush signal must connect the same

- Report Generation
  - Gives separate reports for error and warning messages
  - Designer can review the reports and fix the design, or modify the exclusion file
  - Keep track of the total error/warning numbers

Use model for end user



Experiment Result

Severity	Scenario	Case 1 Error Found	Case 2 Error Found
Error	UFE1 – Ultra/Flush destination mismatch	774	4060
	UFE2 – Ultra/Flush naming mismatch	324	5182
	UFE3 – Ultra floating but Flush not	2	24
Warning	UFW1 – Ultra not having corresponding Flush	5238	9624
	UFW2 – Ultra/Flush range mismatch	4	0
	UFW3 – Ultra tied constant	50	121

Experiment Results

- Error & Warning Reports

```
*******************************************
* VC App: Ultra/Flush Check
* Report : ultra_flush_check_0822.log
* Date   : 2017-08-22 11:54:45
*******************************************

[Error]-UFE1. ultra port "chip_tmdl.u_chip.u_mdsys_top_wrap.md2ap_GALS_M2S_ultra_m_lat_a0[1]" connects to instance "chip_t
mdl.u_chip.u_infra_peri_par_wrap.u_infra_top_par_wrap.u_infra_top_pwr_wrap.infra_top.u_infra_md_par_wrap.mdsys_intf_pwr_wr
ap.mdsys_intf.u_md2ap_ahb_GALS_SLV.ultra_m_lat_M2S_GALS_BUF[1].dtc_ultra_m_lat_M2S_GALS_BUF", yet flush port "chip_tmdl.u_
chip.u_mdsys_top_wrap.md2ap_GALS_M2S_flush_m_lat_a0[1]" does not connect the same.
[Error]-UFE1. ultra port "chip_tmdl.u_chip.u_mdsys_top_wrap.md2ap_GALS_M2S_ultra_m_lat_a0[1]" connects to instance "chip_t
mdl.u_chip.u_infra_peri_par_wrap.u_infra_top_par_wrap.u_infra_top_pwr_wrap.infra_top.u_infra_md_par_wrap.mdsys_intf_pwr_wr
ap.mdsys_intf.u_m
ip_tmdl.u_chip.u_
[Error]-UFE1. ult
mdl.u_chip.u_infr
ap.mdsys_intf.u_m
chip.u_mdsys_top_
[Error]-UFE1. ult
mdl.u_chip.u_infr
ap.mdsys_intf.u_m
ip_tmdl.u_chip.u_
[Warning]-UFW1. Module instance "chip_tmdl.u_chip.u_mdsys_top_wrap.u_mdsys_top.u_modeml1sys_wrap.u_dfe0_par
_wrap.dfesys0_pwr_wrap.u_dfesys0.dfe_bus_intf.u_dfe_2x1_intc_cabgen.u_dfe_masif_2x1.u_dfe_masif_2x1_aw_mux"
 contains ultra port "m0_awultra", yet no corresponding flush port.
[Warning]-UFW1. Module instance "chip_tmdl.u_chip.u_mdsys_top_wrap.u_mdsys_top.u_modeml1sys_wrap.u_dfe0_par
_wrap.dfesys0_pwr_wrap.u_dfesys0.dfe_bus_intf.u_dfe_2x1_intc_cabgen.u_dfe_masif_2x1.u_dfe_masif_2x1_aw_mux"
 contains ultra port "m1_awultra", yet no corresponding flush port.
[Warning]-UFW1. Module instance "chip_tmdl.u_chip.u_mdsys_top_wrap.u_mdsys_top.u_modeml1sys_wrap.u_dfe0_par
_wrap.dfesys0_pwr_wrap.u_dfesys0.dfe_bus_intf.u_dfe_2x1_intc_cabgen.u_dfe_masif_2x1.u_dfe_masif_2x1_aw_mux"
 contains ultra port "s_awultra", yet no corresponding flush port.
[Warning]-UFW1. Module instance "chip_tmdl.u_chip.u_mdsys_top_wrap.u_mdsys_top.u_modeml1sys_wrap.u_dfe0_par
_wrap.dfesys0_pwr_wrap.u_dfesys0.dfe_bus_intf.u_dfe_2x1_intc_cabgen.u_dfe_masif_2x1.u_dfe_masif_2x1_ar_mux"
 contains ultra port "m0_arultra", yet no corresponding flush port.
```

Conclusion

- We utilized static tool to achieve verification goals that can not be accomplished by simulation
- We showed a practical solution to generate clear reports for efficient review
- This solution is adopted to verify our CBIP designs and is capable of finding real bugs

Future Work

- There are other scenarios where simulation can’t provide suitable verification. It doesn’t have to be “Ultra/Flush” signals.
- Our Future work is to deploy this methodology to other connectivity checking needs. Expand the possibilities to the fullest.

MEDIATEK

snug
Synopsys Users Group
Taiwan

Thank You