Test IP: Bringing the Tools and Methodology from Pre-Silicon Verification to Post-Silicon Validation

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Test Evolution

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SNUG Boston

Agenda

Post Silicon Validation Problems

Our Solution

Implementation with Synopsys

Application & Results

Conclusions & Future Work

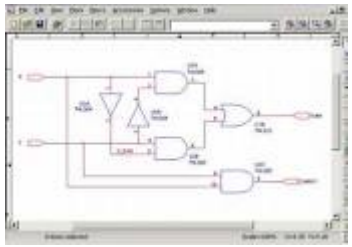
Current Post Silicon Validation

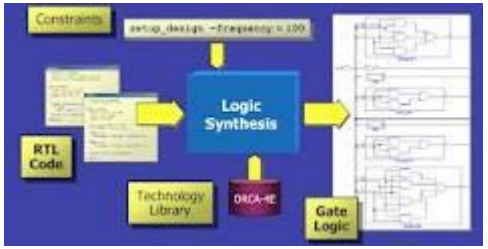
- Protocol boxes from multiple vendors generally do not work together well.
  - All have their own driver software and programming model
  - All have their own debugging tools
  - Functional testing is limited
- Tool flows from pre-silicon to post-silicon to production and back are nonexistent.
  - This makes writing tests challenging
    - and thus generally limited in robustness.
  - Debugging suspected problems is difficult across more than one interface.
  - Issues in production? Good luck …

Functional Testing Issues

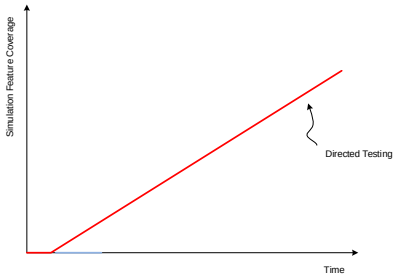
Post Silicon Validation	Production Testing
Can’t simulate everything.	SCAN is not covering all defects.
Power distribution network and power domain testing.	50% Non-Detected Faults.
Fringe functionality.	No correlation to bugs in post silicon.
Performance validation.	Has always been done in some form, but is difficult and limited on ATE.
Use case testing	

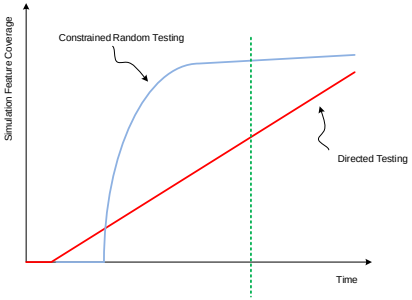
About Time For a Change



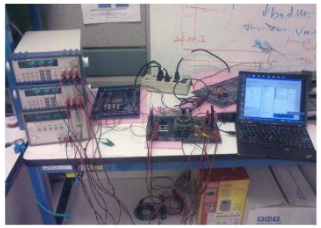


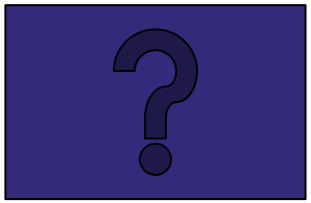
Large design productivity jump!

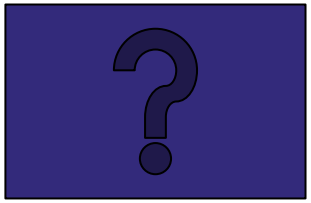


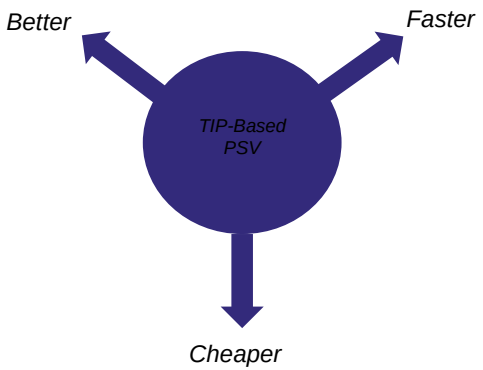


Large verification productivity jump!









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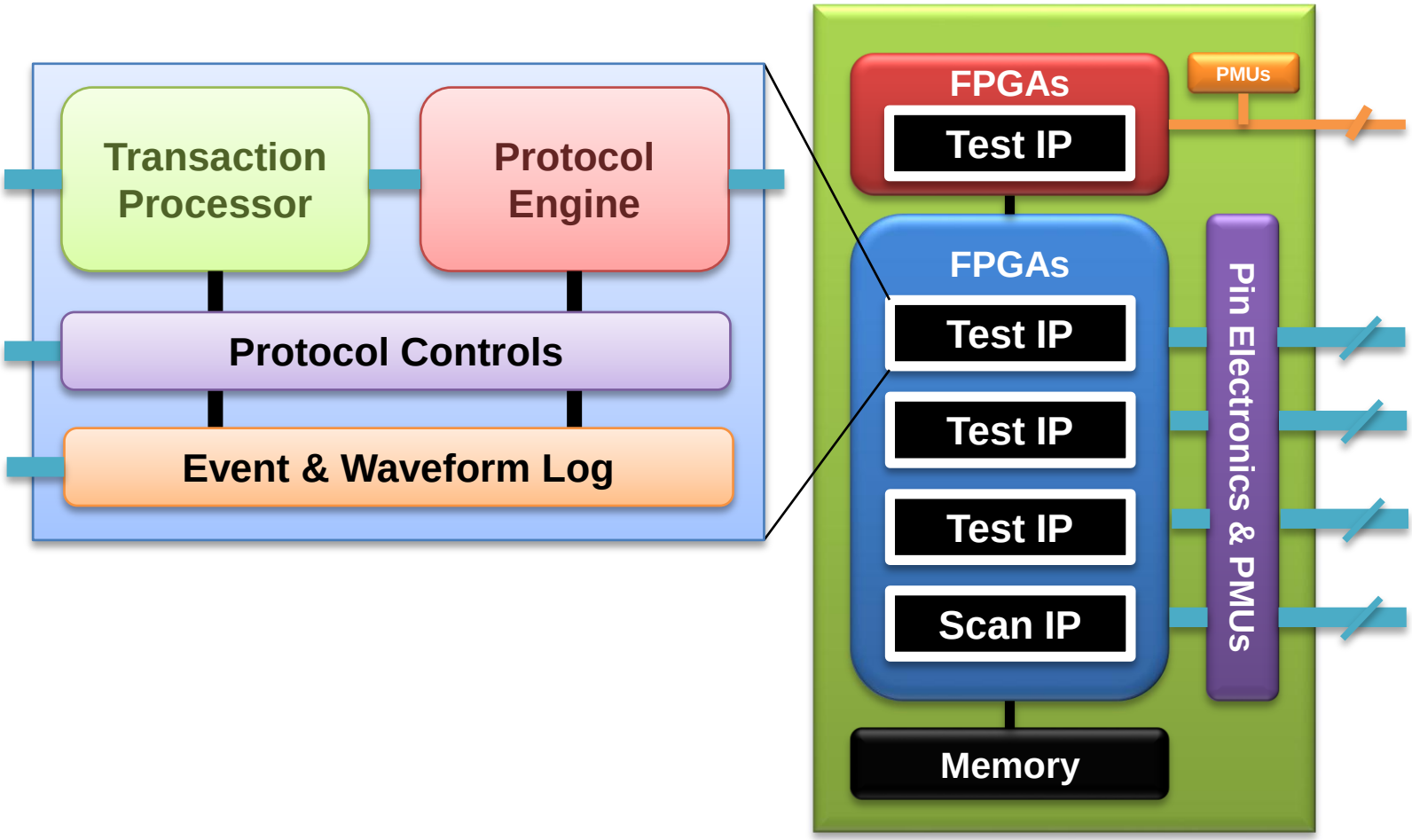
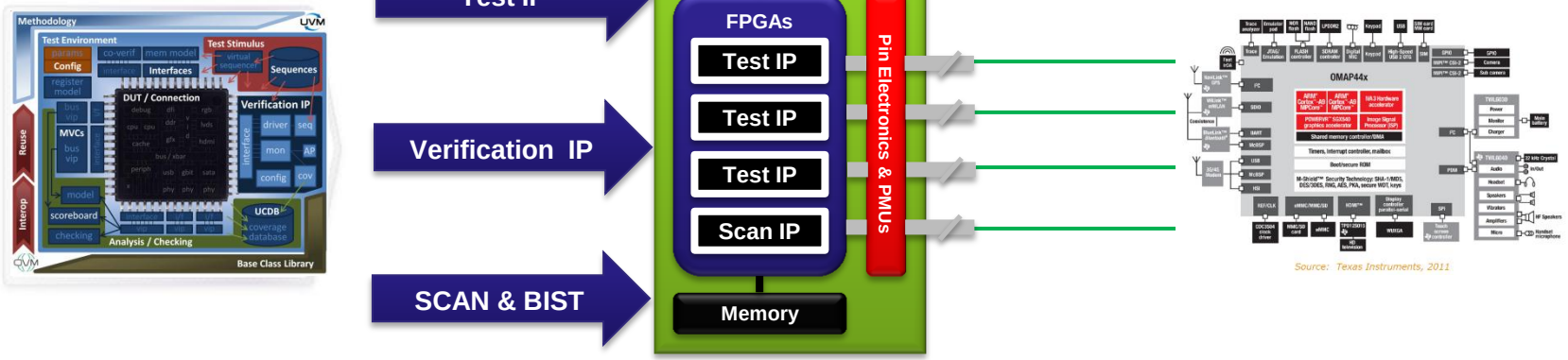
Test IP Architecture



Connecting to a DUT



PSV Requirements Alignment

PSV Testing Requirement	TIP-Based PSV System Feature
Pre-to Post-Silicon Leverage	• Same methodology & tools as pre-silicon • Use models allow Pre-Si <->Post-Si leverage
Deterministic Operation & Repeatable Test Cases	• TIP synchronization methods analogous to pre-silicon • Seed-based algorithmic stimulus
Self-checking Tests	• Scoreboard methodology • Algorithmic response checking • Pre-loaded expect data with self-checking
Debug Hooks	• View stimulus and response from DUT via Protocol Analyzer tools across all interfaces • Time-stamped scoreboard data • Recreate in pre-silicon DV environment for internal DUT debug visibility
Error Injection	• Scenario-based callbacks in transaction processing flow for each TIP type • Pre-defined error injection mechanisms

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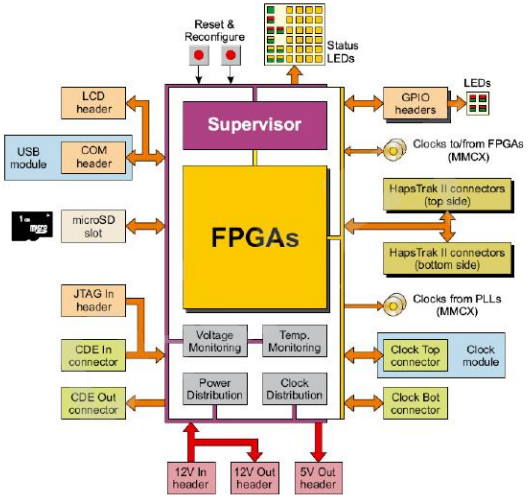
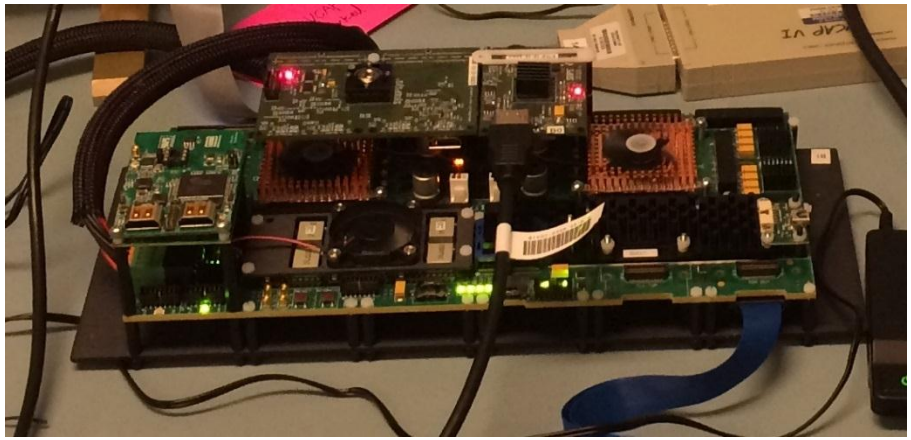
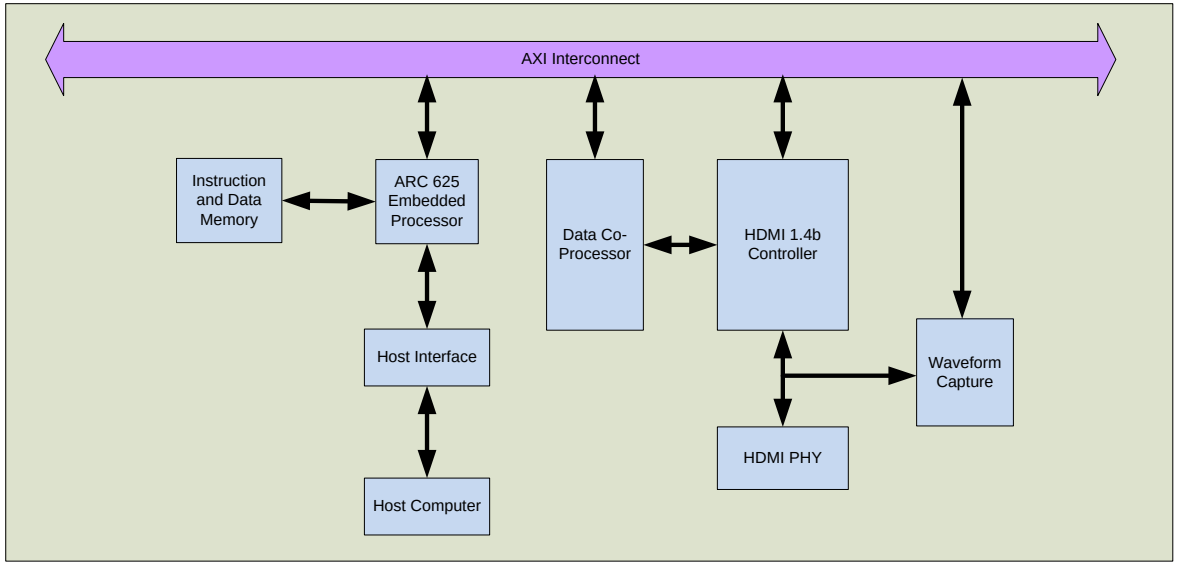
HDMI TIP in HAPS





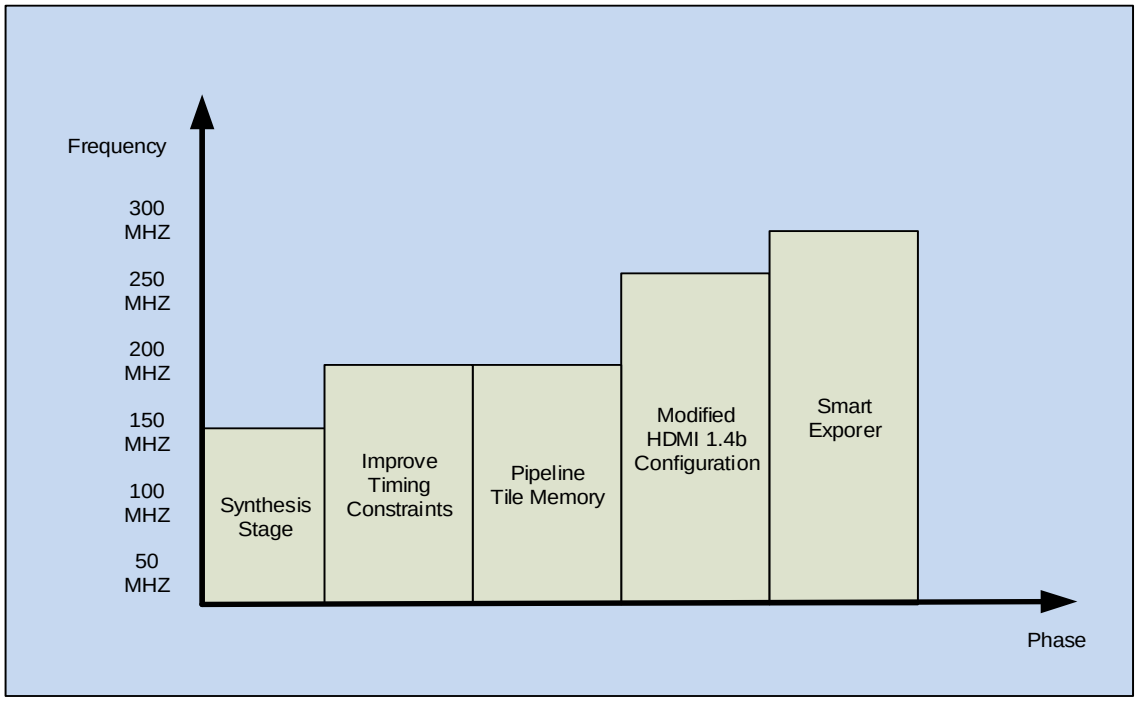
- Large FPGAs
  - No issues with fitting - enough logic, memory, and IO resources
- HDMI PHYs on HAPS daughter cards
  - Easy prototyping for protocols
  - Other modules, like DVI to ease debugging
- Clock resources
  - 27 MHz to 297 MHz with multiple frequencies in between
- UMR Bus for communication via PCIe

TIP Internals



- ARCitect2
  - ARC625 soft core, 50-75MHz
- CoreConsultant
  - Generate source
- CoreAssembler
  - Generate AXI4 & other DesignWare
  - Wire everything together

Timing Closure



- Synplify Premier
  - Synthesis
- Xilinx ISE
  - Implementation
- Xilinx SmartExplorer
  - Timing closure

- Difficult to close timing with HDMI 1.4b in 4K mode
  - Issues in IP core
    - Removed some features not needed for testing
  - Issues in transaction processor logic
    - Synthesis and implementation optimizations

Embedded SW

- uC core used for flexibility and implementation speed

  Empirical data suggests the following rule: for complex systems, RTL implementation takes 5x more time/resources than embedded SW implementation, and embedded software takes 5x more time/resources than non-embedded SW

- Goals:
  - Shift as much as possible (traffic generation, pre- and post-processing) to the embedded SW
  - Perform the rest in the RTL
- MetaWare
  - Development toolkit for ARC SW development
- MQX RTOS
  - Interrupt handling for HDMI events

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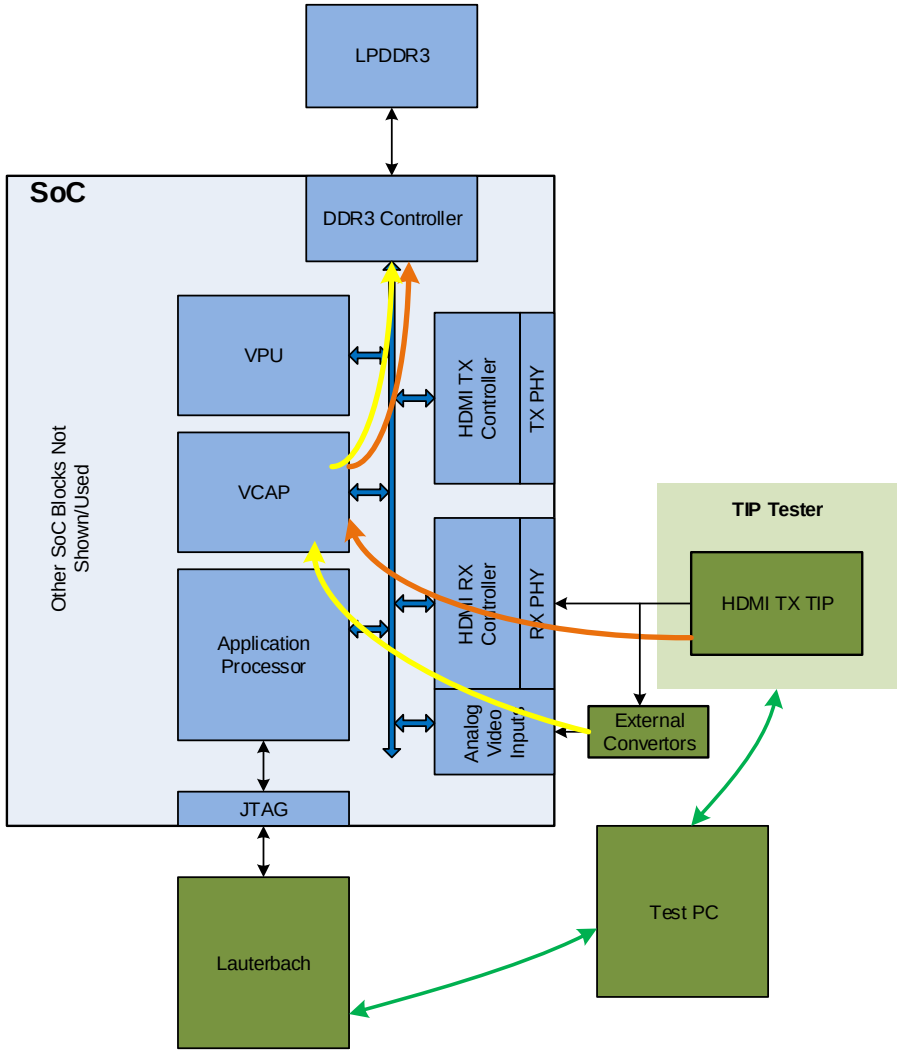
Set Top Box / Smart TV IC

- Integrated TIP HW, SW, and Lauterbach in a Visual Studio
  - Custom PSV board for push-button testing.
- Configured TIP system to drive HDMI into IC and converters for the AFE,
  - Self-checking test code for pixel-level comparisons.
  - Useful as an early silicon production system.
- Found 15 overall issues, from low to high priority, that required investigation.
- Ran focused nightly regressions that were difficult to do with existing test equipment, and found issues.
- Quickly confirmed existing issue with VGA noise, and characterized.

PSV Setup



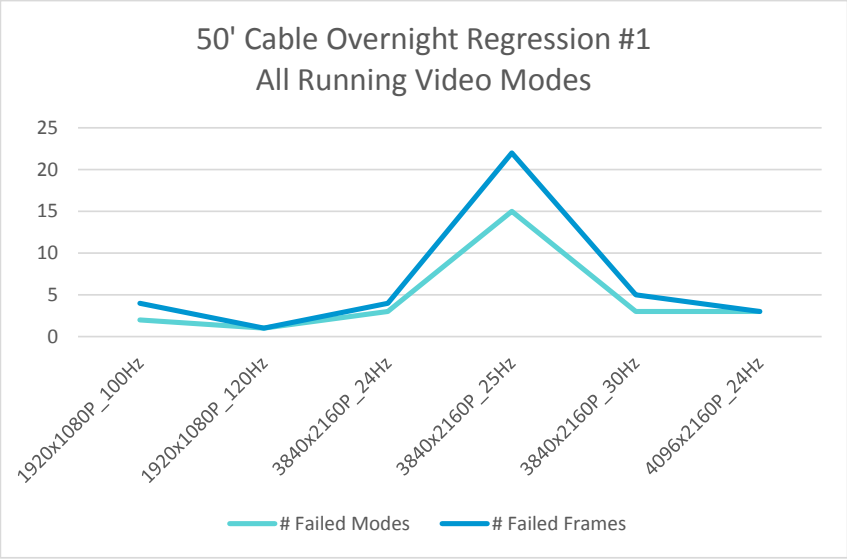
- Use HDMI TX TIP to drive frames
  - Ran all required modes, plus additional 4K/60Hz/4:2:0 mode
  - Run for hours & days and recorded errors
- Used DDR for Video Capture
  - Both HDMI and AFE, concurrent testing, stressing logic & DDR
  - Pixel compare in test with error checking and reporting
  - Push-button testing, nightly & weekend regressions
- Test PC coordinated HDMI TX and Lauterbach with debug system
  - All in Visual Studio
  - Easy to craft tests
    - Stress design & characterize issues
    - Collect statistics

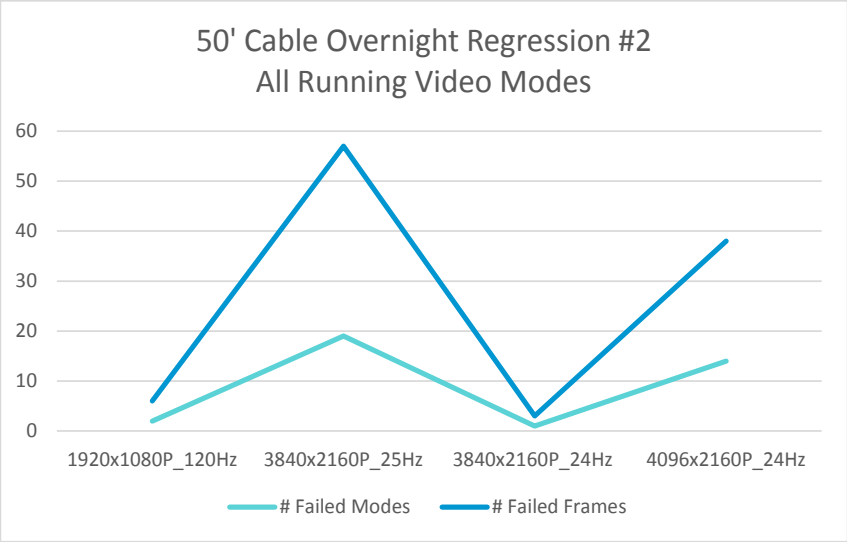
Issues Found

#	Type of Issue	Status
7	Potential SW Driver problem	Some are definitely SW driver issues. Others need further investigation.
2	Test site setup	AFE related. Impacts automatic testing.
1	PHY	Two runs were done. Both indicating silicon issues at 297MHz pixel rates.
1	PSV Board	This is a known issue found independently. TIP system was used for more characterization of noise, showing ~25%.
4	Unknown	These are related to mode switching and dual-channel throughput into and out of DDR.

- 15 Issues found
  - Thru 4 days of work, with overnight stress testing
- PHY issue and 4 unknown issues are very interesting
  - TIP system allowed for building repeatable and interesting tests quickly
  - PHY issues were deemed silicon problems!

Silicon Issues: PHY

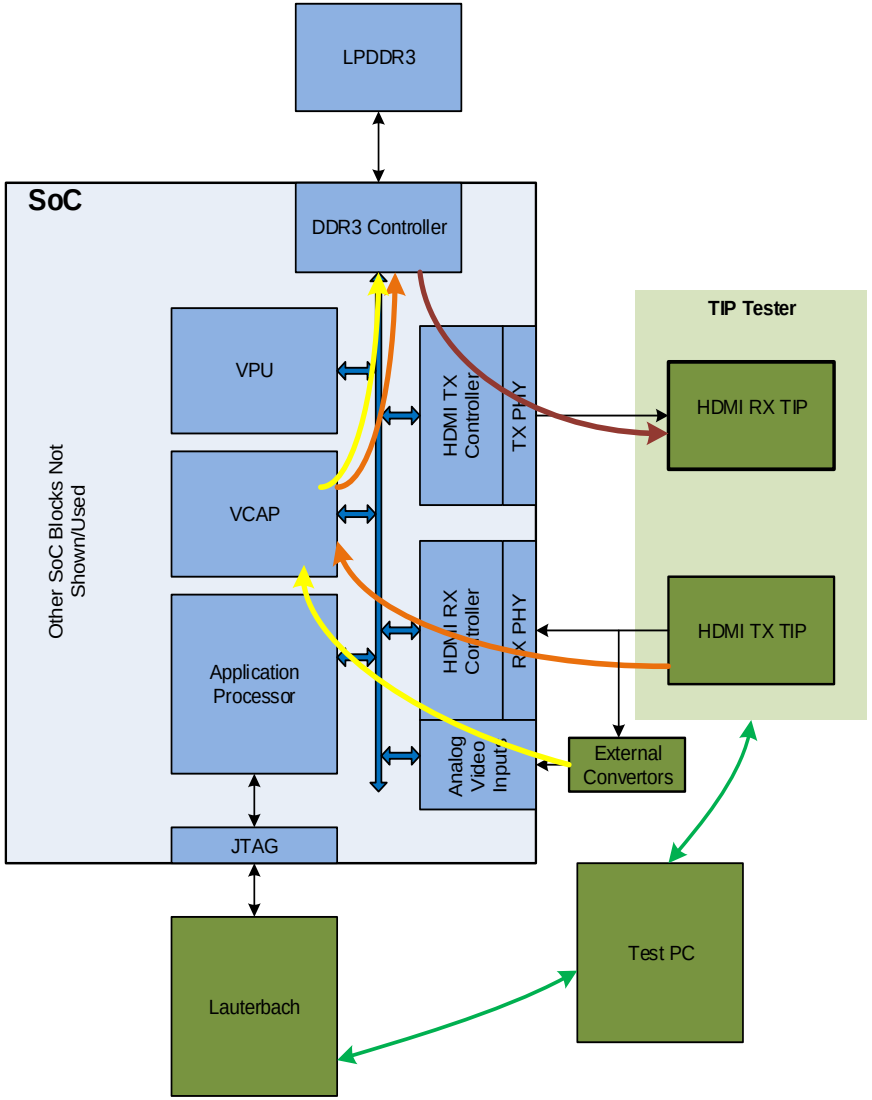




- Found using 50’ cables and overnight regressions
- Showed a statistically significant number of pixel errors across various video modes
  - Required a 297MHz pixel clock rate into the HDMI receiver PHY
- The failures were randomly distributed over 14 hours of testing.
  - Regression #1 run with typical silicon
  - Regression #2 run with slow silicon
  - More errors with slow silicon
- Difficult to find using existing PSV solutions
  - Requires full functional, at-speed, self checking testing using random data over many hours!

End to End Testing

Proof of Concept



- Expanded the testing to the Multimedia subsystem
  - HDMI TX & RX TIP @ 1080p
    - Only end to end mode supported
  - Concurrent AFE Video Stream
  - Pixel-by-Pixel Compare in RX TIP in real-time
  - Random Data
- Why Important?
  - Test Time
    - ~2-3 minutes
    - 20-30x faster than ~40-60 minutes with DDR-based compare method
  - Functional Coverage
    - Closed loop, exercising logic & DDR
  - More efficient
    - Push-button, self checking, at speed
    - Basis for future work

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Summary

Applying the TIP-based PSV methodology on the HAPS platform, both for pre-silicon PHY characterization and PSV of the VCAP and MMS, demonstrated the following:

- HAPS allows straightforward prototyping and allowed us to run real-time protocol-based PSV across multiple protocols.
- The ability to easily create robust tests that are repeatable and self-checking.
- The ability to craft tests to find issues quickly.
- The ability to run tests overnight or over a week, with end to end self-checking and error history.
- Quick discovery & characterization of silicon issues that would be difficult to find with existing test equipment, like protocol analyzers.
- Extending the PSV work to concurrent testing with Android would be straightforward.

And, most importantly …

The Ability to Find Silicon Bugs!

Moving Forward

- Will scale across multiple TIP instances
  - MIPI DSI, MIPI CSI-2, USB 2/3x, UFS
  - Native support for synchronizing TIP instances
  - Debugging the DUT across protocol interfaces
- Can be used across PSV groups, from
  - Interface to subsystem to full chip
  - Leveraging tests and methodology across groups.
- Will reduce the cost of PSV testing
  - Integrating functionality that is limited in existing test equipment,
  - Providing in one platform functionality that would require multiple pieces of existing test equipment integrated in an ad-hoc way.
- Extends to production testing


Thank You