I’m sorry that I’m currently working from home, so the internet speed when connecting to RAS server is slow.
Allow me to turn off video.

Good Afternoon, everyone.
Thank you so much Huong-san for introducing me and the organization.
Also thank you for giving me this presentation opportunity.

Let me start by saying just a few words about myself.
My name's Hoi from High Speed Interface Department.
From now on, I will take a new assignment on managing High-Speed I/F Section 3.
And I will have a new chance to work with Peripheral Circuit team.
So I'm looking forward to cooperating with you for more success. Thank you.

So now, get back to the topic at hand.

In today's presentation, I'd like to walk you through the PJ development status of 2H/2023, our major targets of 2024,
and also some operational policies that ensuring consistency and efficiency of PJ development

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Firstly, I will begin with Organization and Mission.
We have some members that got promoted to new positions this year.
By this chance, congratulations on your new roles.
And I hope that you continue developing yourself and contributing to our business.

Our organization includes two small sections: High-Speed I/F Section which is still managed by me & Peripheral and Communication Section which is managed by Khanh-san.
In each section, we have some small teams working on each specific IP function.
In HSIF IP, we have group working on Storage I/F, Connectivity, Image/Display IP
In Peripheral IP, we have group working on Analog Mixed Signal IP: ADC, DAC, or some communication IP: R-Switch, Ethernet, etc

Our mission is to:
My responsibility is to:

We will try to standardize and unify process, core methodology, EDA tool and apply it for projects from High-speed I/F IP to Peripheral I/F IP to improve productivity.

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And now, it’s time to look back on our project developments from 2H/2023.
Last year, we have been supporting verification for both original IPs which are developed by Renesas and also Purchased IP from Vendor.
Some original IP, for example:
xSPI-Dual: We completed verification for both Master/Slave function. DPO application
MIPI DSI/CSI
Type-C
Some Purchased IP in RCAR-X5H which has T.O middle of Jul. So we are in hurry to complete these IP verification.
UFS: Completed all verification items + DTL
USB3.2/USB2 and PCIe4 which are using same MP-MPHY: The remaining items is HP2 which is planned to complete by May/31
PCIe6.0 + CXL30: This PJ still has a high risk, we just completed the 1-path check + start some base verification. We try to accelerate debugging with JP team
For Analog & Mixed Signal, ADC
Communication R-switch3.0: We supported verification for COMA/TS module to achieve 100% functional coverage

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In addition to PJ development, we investigated and learned some new methodologies to improve our productivity.
DTL:
Many complex IP (e.g. USB, PCIe, UFS, etc) require very significant time on system boot-up and initialization sequence (link training)
This can lead to many wasted simulation cycles and engineer wait hours if:
+ The same start-up phases are executed repeatedly for every test while contributing little towards the coverage
+ If there is a failure during debugging, it’s needed to go through the entire initialization phase to debug that issue
That’s the idea behind DTL.

Benefits:

+ Reduce test development cycles/flows
+ Reduce debugging cycles/flows
+ Save hundreds of SIM hours and more importantly, engineer wait hours
+ Get to the more meaningful portion of the simulations faster

DPO:
Shorten the regression TAT. The benefit increases when the more regression iterations are performed

VCS DPO flow involves following 3 steps:
・Learn: performs analysis and store learnings/recommendations in the database.
・Merge: merges the learnings across the designs/tests.
・Apply: Learnings/Recommendations are fetched from the merged database and applied automatically.

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2024 Major Targets
For Purchased IP, we will continue verification for all these IP in RCAR-X5H by the due date.
For xSPI-Dual, this IP will enhance to support 16-bits data width
There are two new PJs: USB3 Device IP which enhances to support HS/LS Iso. IN/OUT and TypeC-PD

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Improve every aspect of the work by a slightest percentage that can make a bigger improvement.
If we could improve spec of CDV by just 1%
If we could improve constraint tunning of random verification by just 1%
If we could improve every little components for re-usuability & portability by just 1%
And everything like that, every 1%. There would be a tremendous improvement in the long run.

JG UNR:
Removes distracting coverage holes due to code that is unreachable because of unused configurations that allows engineers to focus verification efforts on the remaining actual coverage holes.

Cadence Smart Run w/ vManager:
Provide fastest TAT for a regression and improve verification throughput:
+ Learning the typical run durations for tests
+ Provide the ability to reshuffle and launch new regressions using the new queuing policies to improve TAT for regression