Verifying Microprocessor Debug-bus Connectivity Formally using VC Formal

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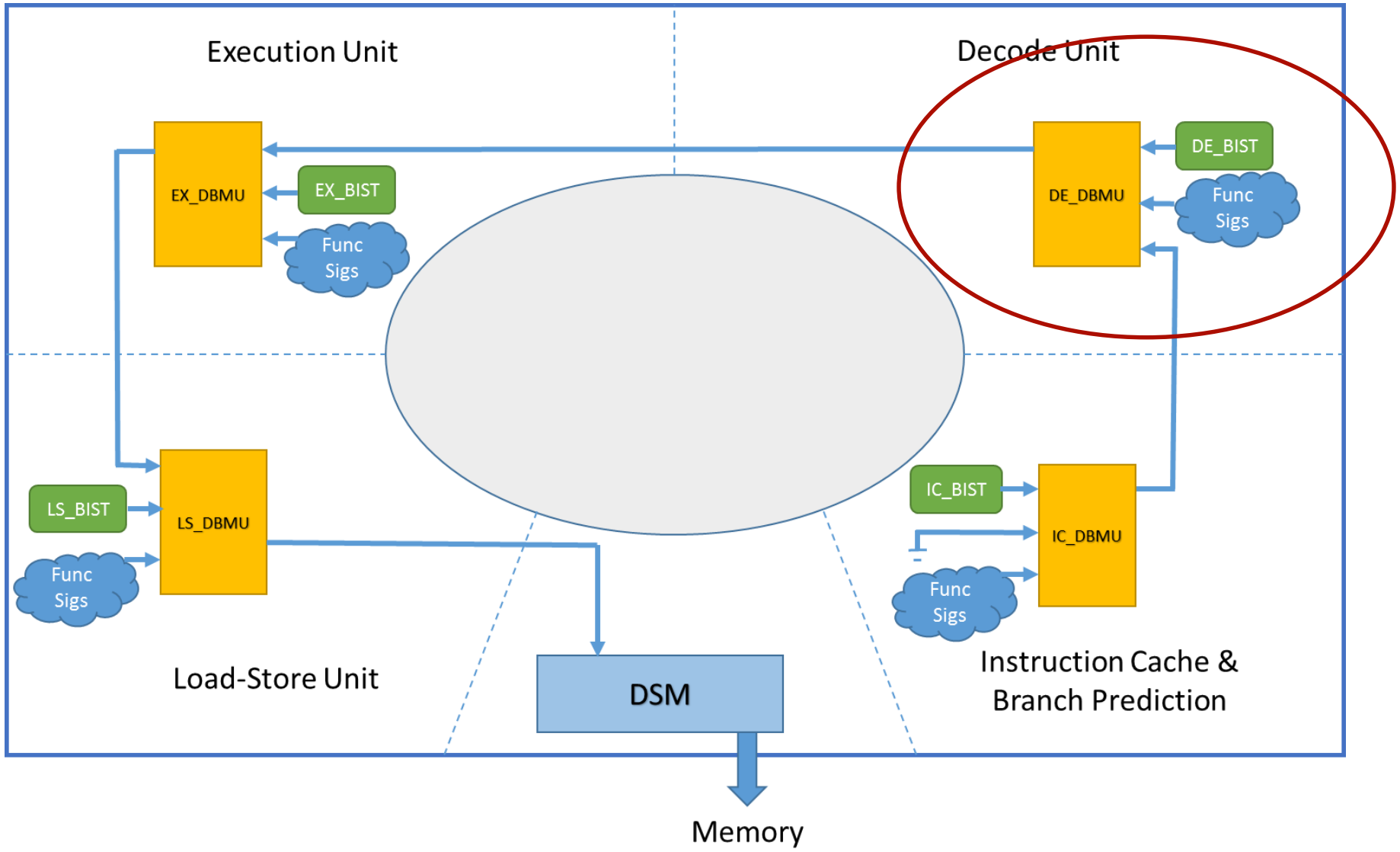
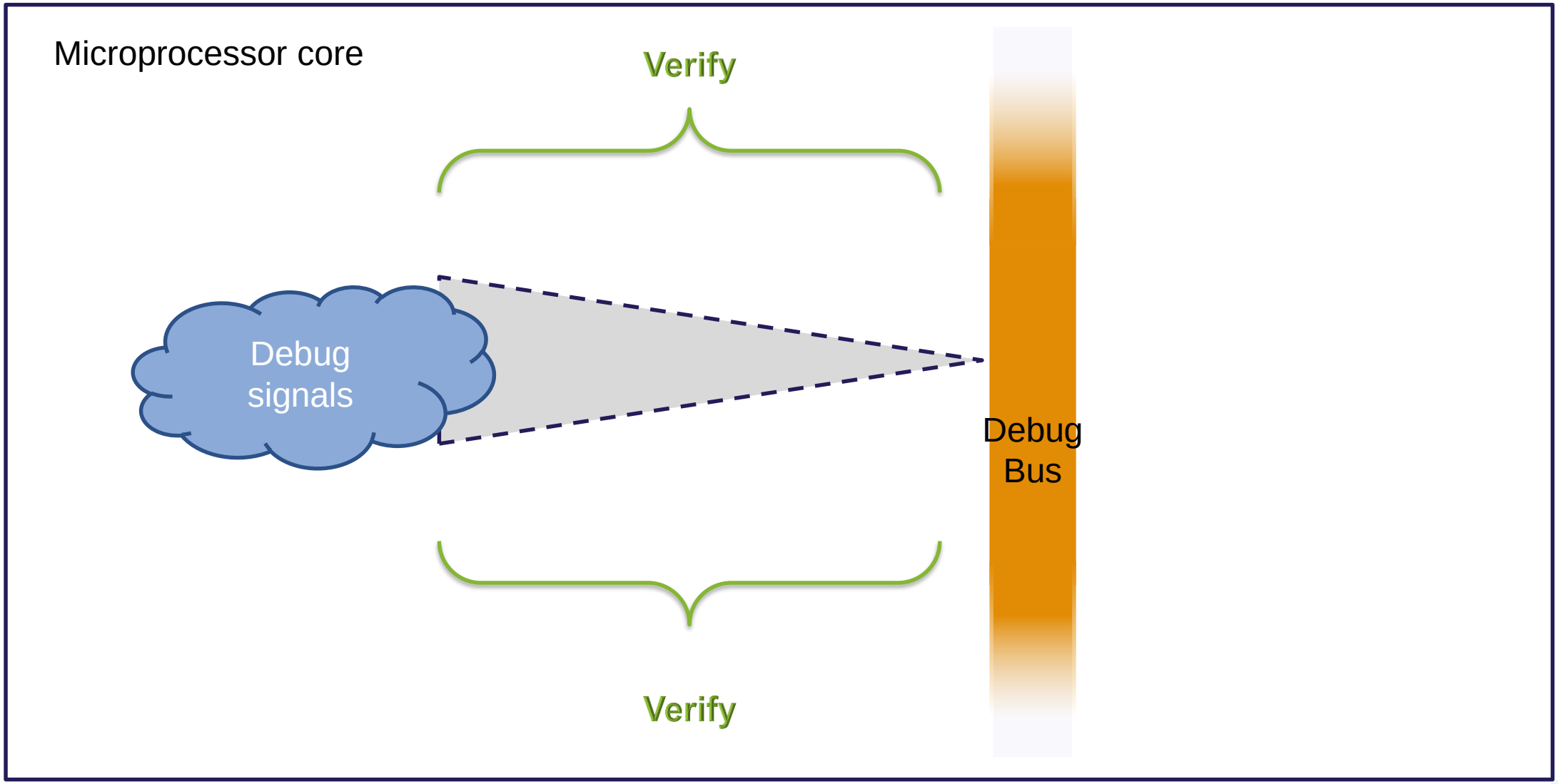
Agenda

- **What is debug-bus?**
- Traditional verification
- Why use formal?
- How to use formal
- Gotchas
- Issues identified
- Conclusion

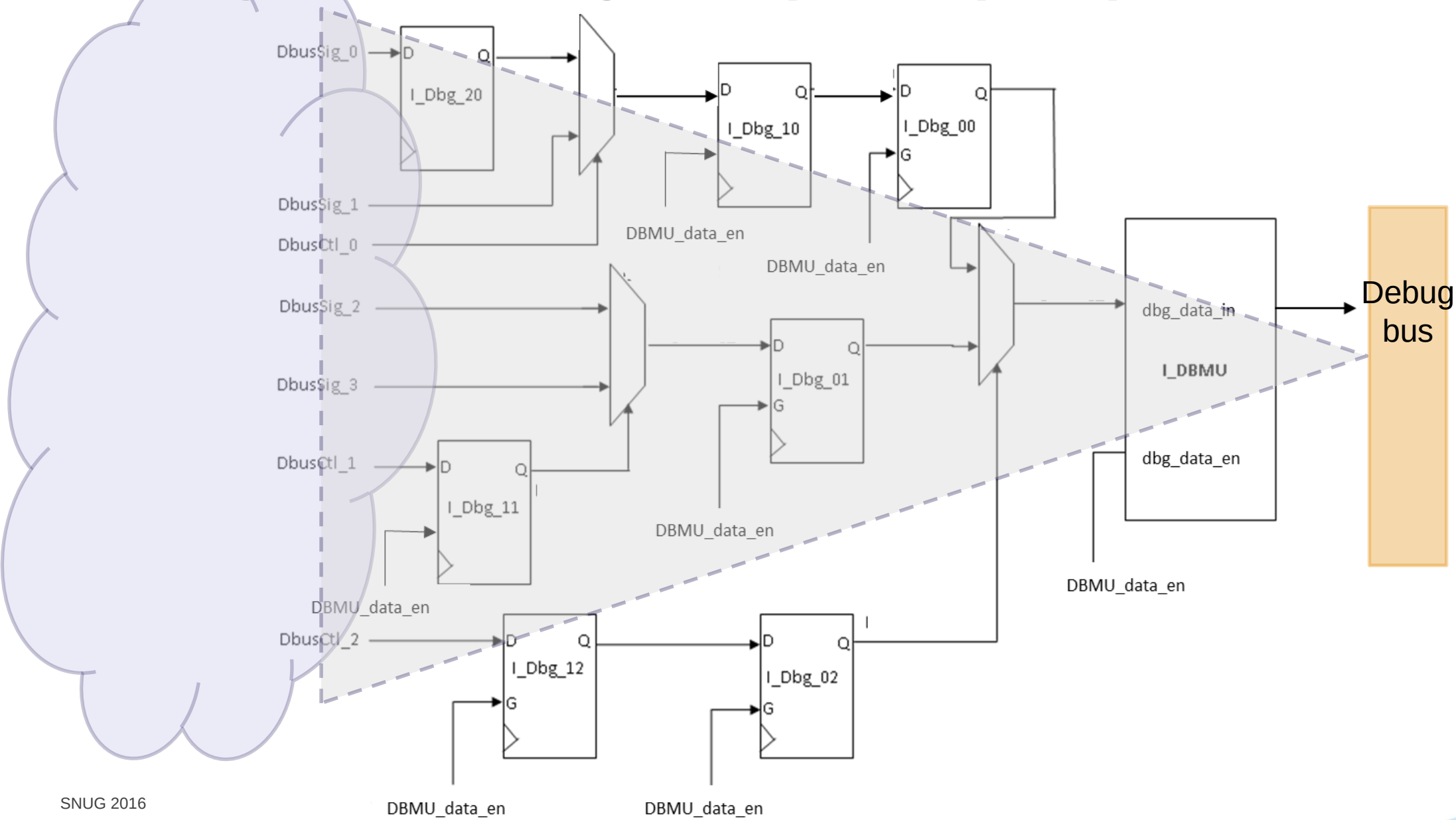
What is debug-bus?



Problem statement



Debug-Bus Muxing Unit (DBMU) stop



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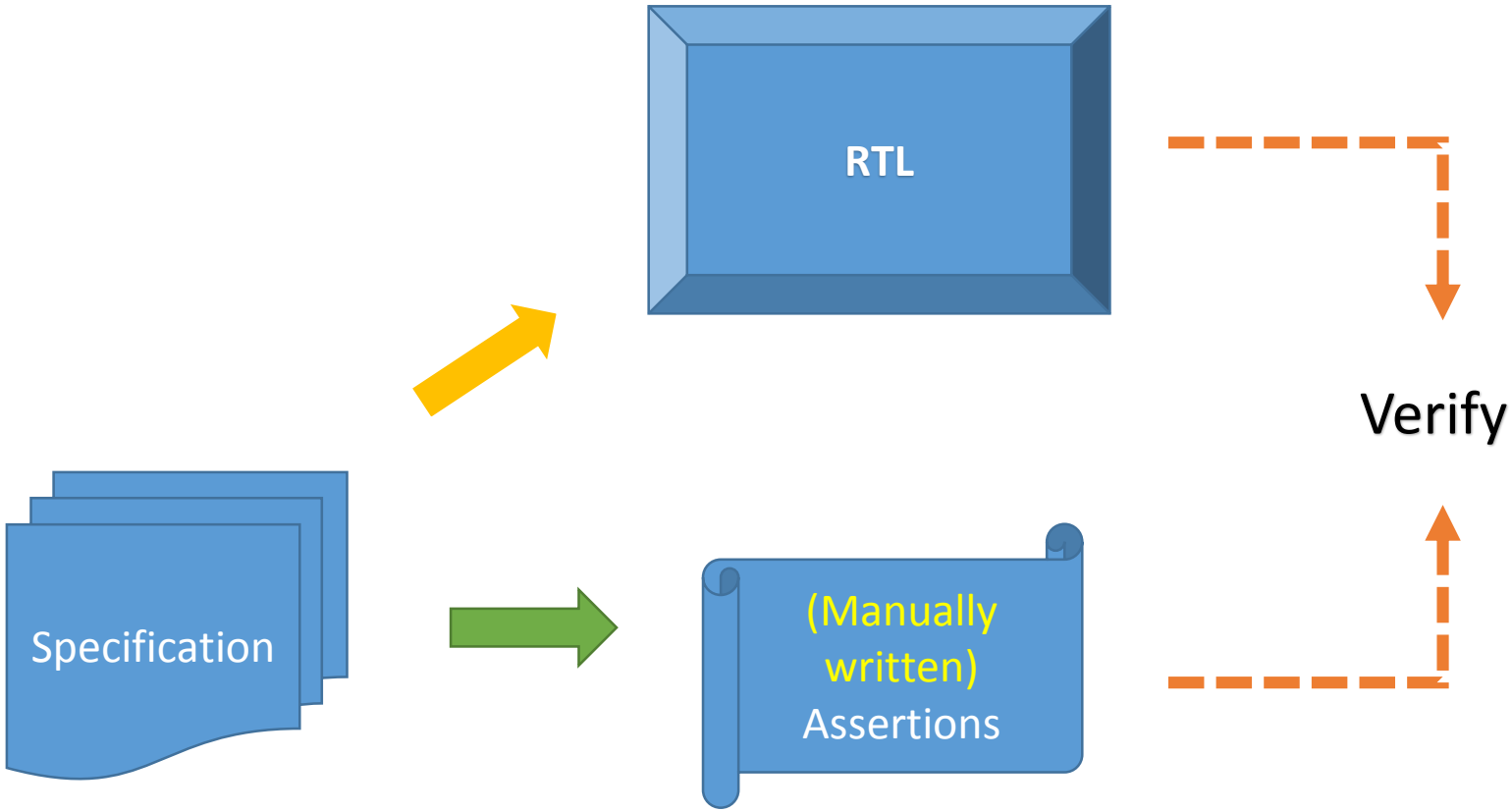
Simulation-based verification



Determining verification effort

- ▲ Critical piece of debug hardware
- ▲ Behaves like a hardware assertion

- ▼ No direct customer value
- ▼ Writing D-tests is monotonous and labor intensive
- ▼ Debug signals change constantly as design evolves

Drawbacks of traditional verification

Design

- Keeping assertions up-to-date is time-consuming
- Even simple RTL changes require assertion updates

Verification

- Lots of false positive fails
- Closing assertion coverage is cumbersome

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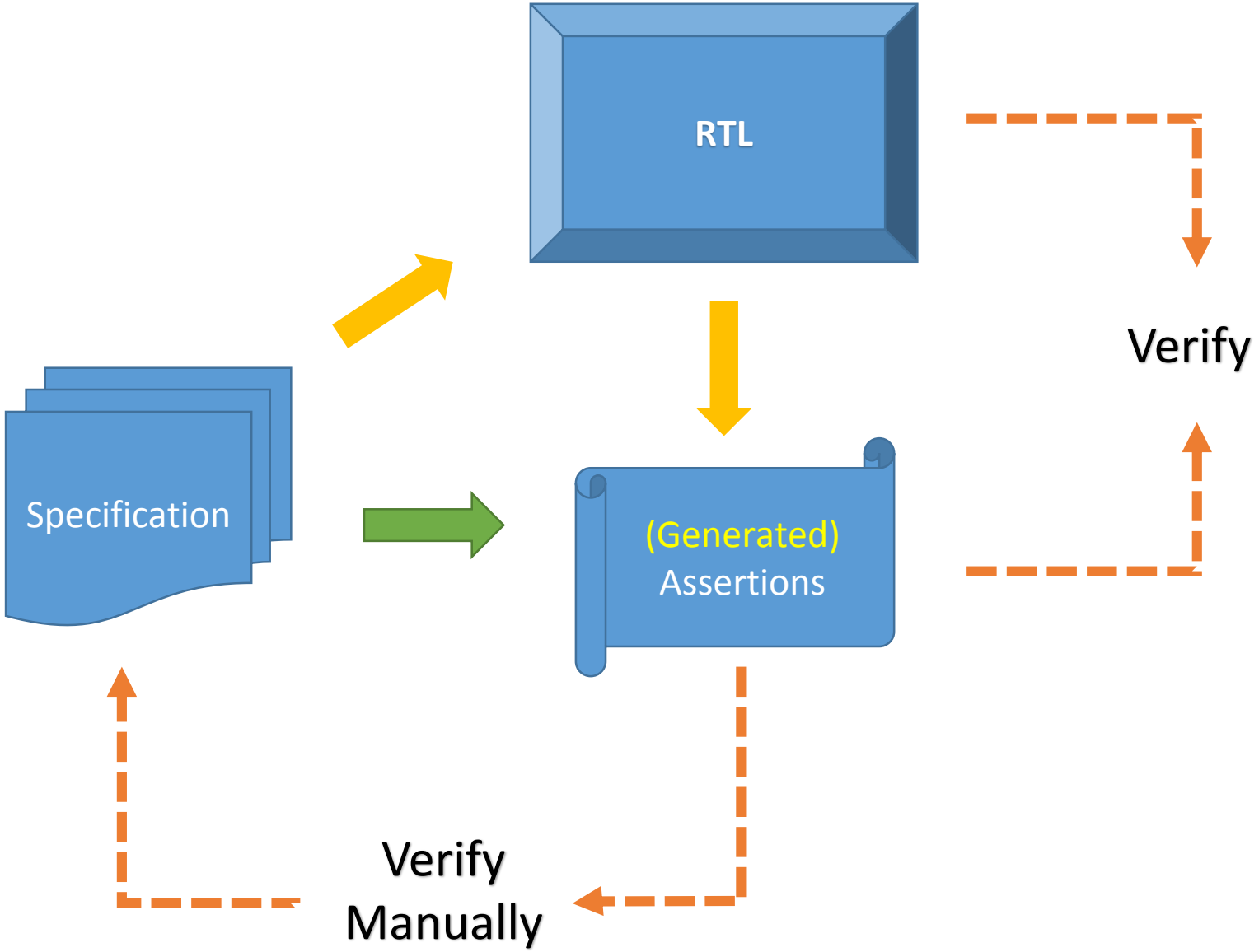
Formal verification



Pros and Cons of formal verification

- ▲ Can be setup as an automated flow
- ▲ Not having to write/update assertions
- ▲ Testing is exhaustive
- ▲ Turnaround time of 24 hours

- ▼ Learning formal verification
- ▼ Have to build test infrastructure from scratch
- ▼ Design has to be amenable

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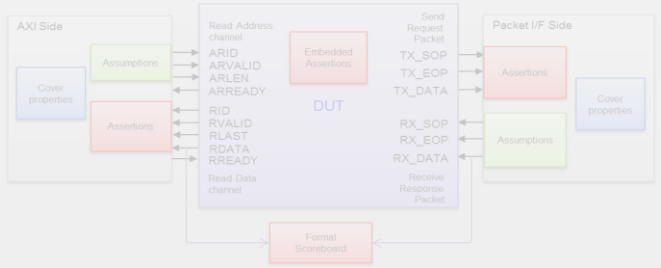
VC Formal

Property Verification

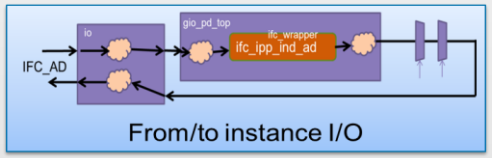
Verify property convergence



Connectivity Checking

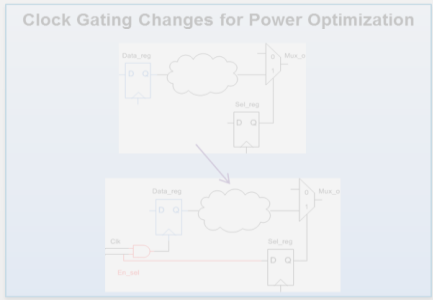
Verify connectivity correctness

to specification



Sequential Equivalence

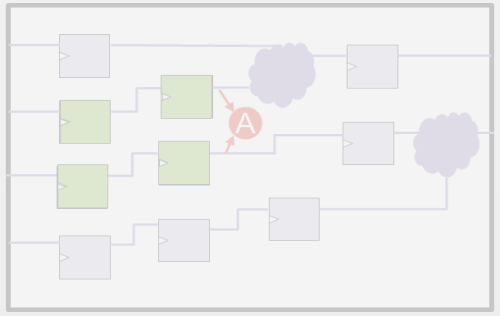
Catches bugs missed by other tools



Auto Checks

Formal aware structural design analysis

Easy setup and comprehensive checks



Formal Coverage Analyzer

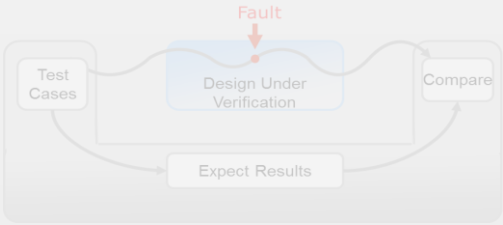
Native integration in VCS

Common coverage debug with Verdi

Formal Testbench Analyzer

Formal testbench completeness

High performance fault injection & analysis



Preparing for formal verification

1. Analyze design size and depth of logic

2. Follow a consistent signal naming convention

   Source: DbusSig*
   Sink: DBMU_LOCAL_DATA
   Control: DbusCtl*

3. Replace AND-OR logic with muxes using `defines

How it's done

Step 1: Assertion extraction

Initialize tool

Black-boxes unwanted modules

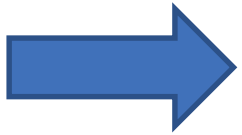
Setup clock and reset

Enable clock-gaters

Identify sources and destination

Identify control signals

Generate assertions



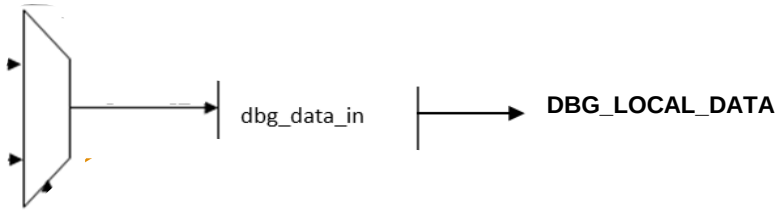
Step 2: Assertion proof

Define initial state

Prove assertions

(Debug and repeat)

Example of SV assertions



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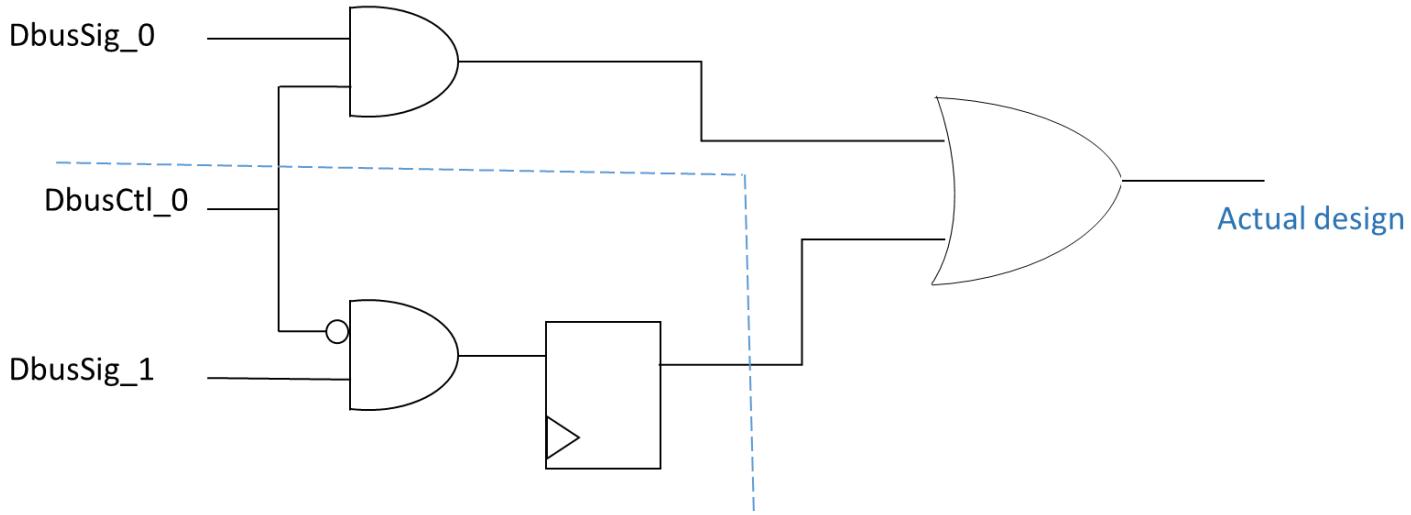
Combinational logic in datapath



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Debug-bus design issues identified

- No path from debug signal to DBMU output

- Naming convention violations

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Conclusion

- Used VC Formal to perform processor core debug-bus connectivity check
- Checks are exhaustive; no separate coverage closure effort required
- Flow is automated. 24 hours turnaround time.
- Required design modifications to work around tool limitations
- No debug-bus issues in silicon

AMD

snug
Synopsys Users Group
Austin

Thank You

- When can the generated assertions fail?
  - When design used for assertion generation != design used for assertion proof (AND-OR -> muxes)
  - Use assertions as golden to check functional ECOs. Will see fails is debug-bus connectivity is disrupted.

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