



Combining Emulation and Virtual Prototyping – The Whole Is Greater Than the Sum of Its Parts

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Agenda

Hybrid System Level Emulation – Platform Goals

Shift left with Pre-Silicon Platforms

Bringing the Platform to Life

Technical Challenges

Results

The Bigger Picture – Pre-Silicon Continuum

Hybrid System Level Emulation

Platform Goals

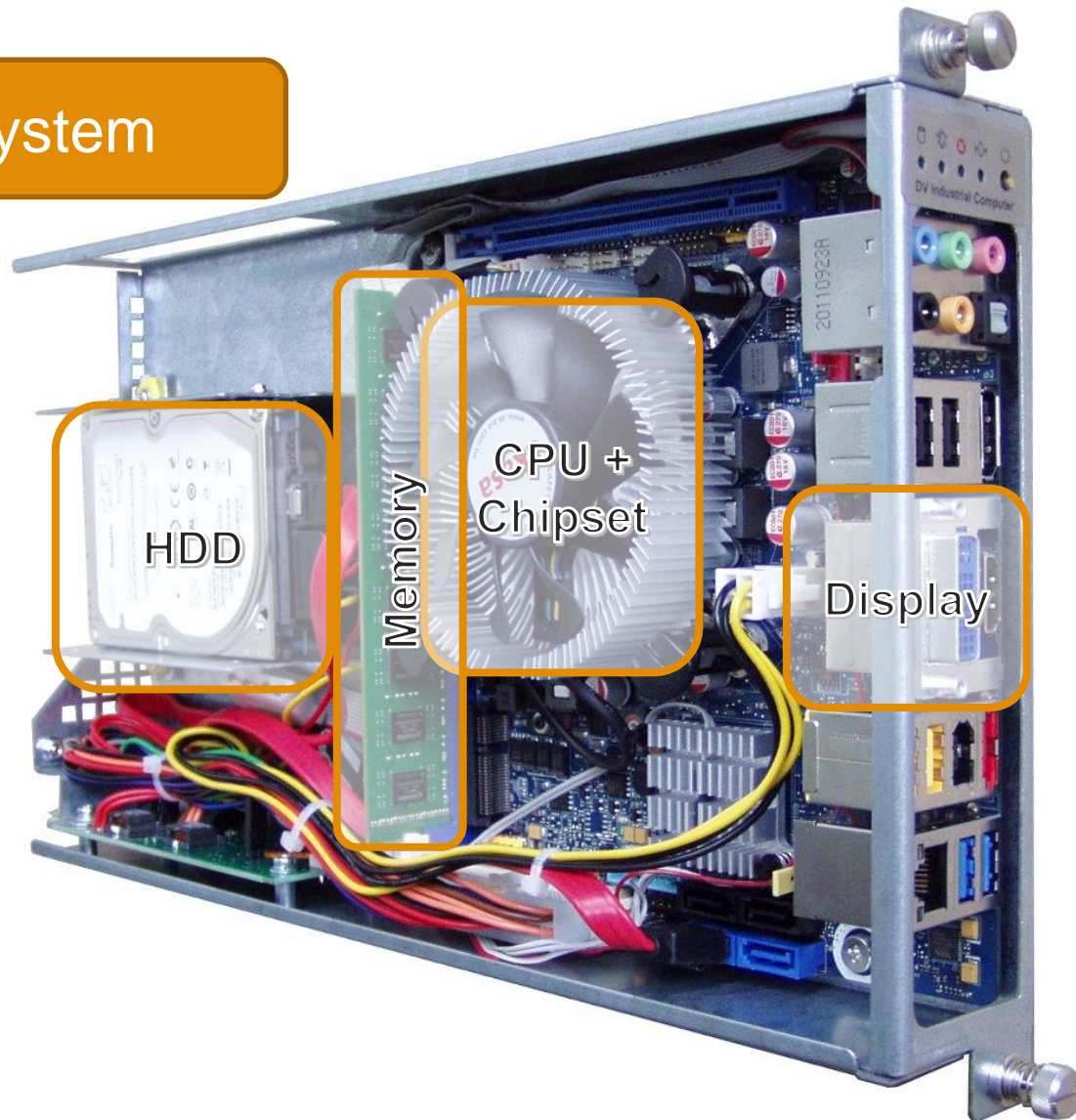
- Speedup effective performance
- Reduce emulation model size
- Meet system validation goals
 - Shift Left System Validation (SV)
 - HW/SW Co-validation

Enabling use cases not possible with system level emulation (SLE)

- Execute operating system (OS) based validation with production SW stack pre-silicon (Pre-Si)

Shift left with Pre-Silicon Platforms

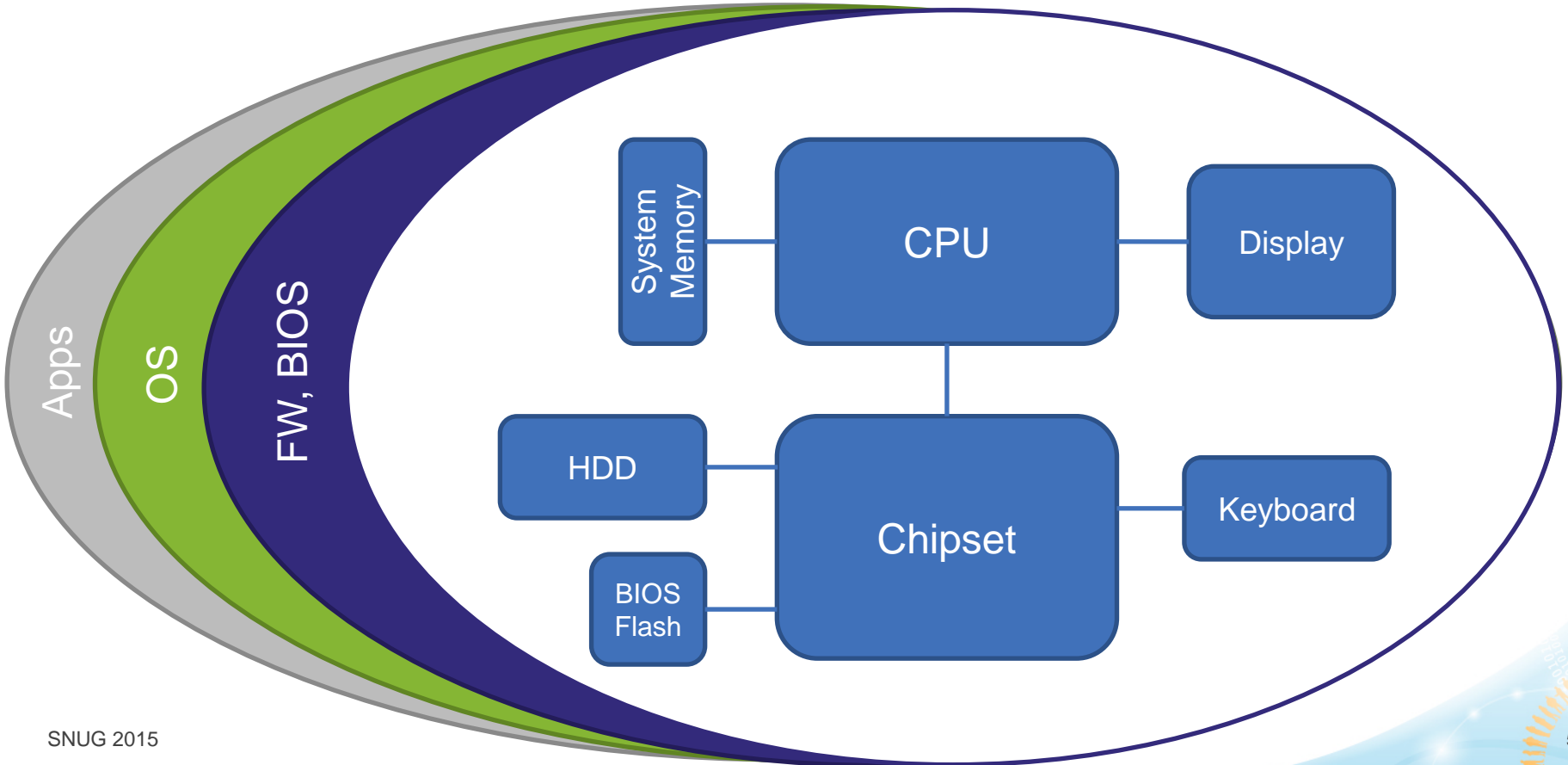
Think System




Shift left with Pre-Silicon Platforms

Think System

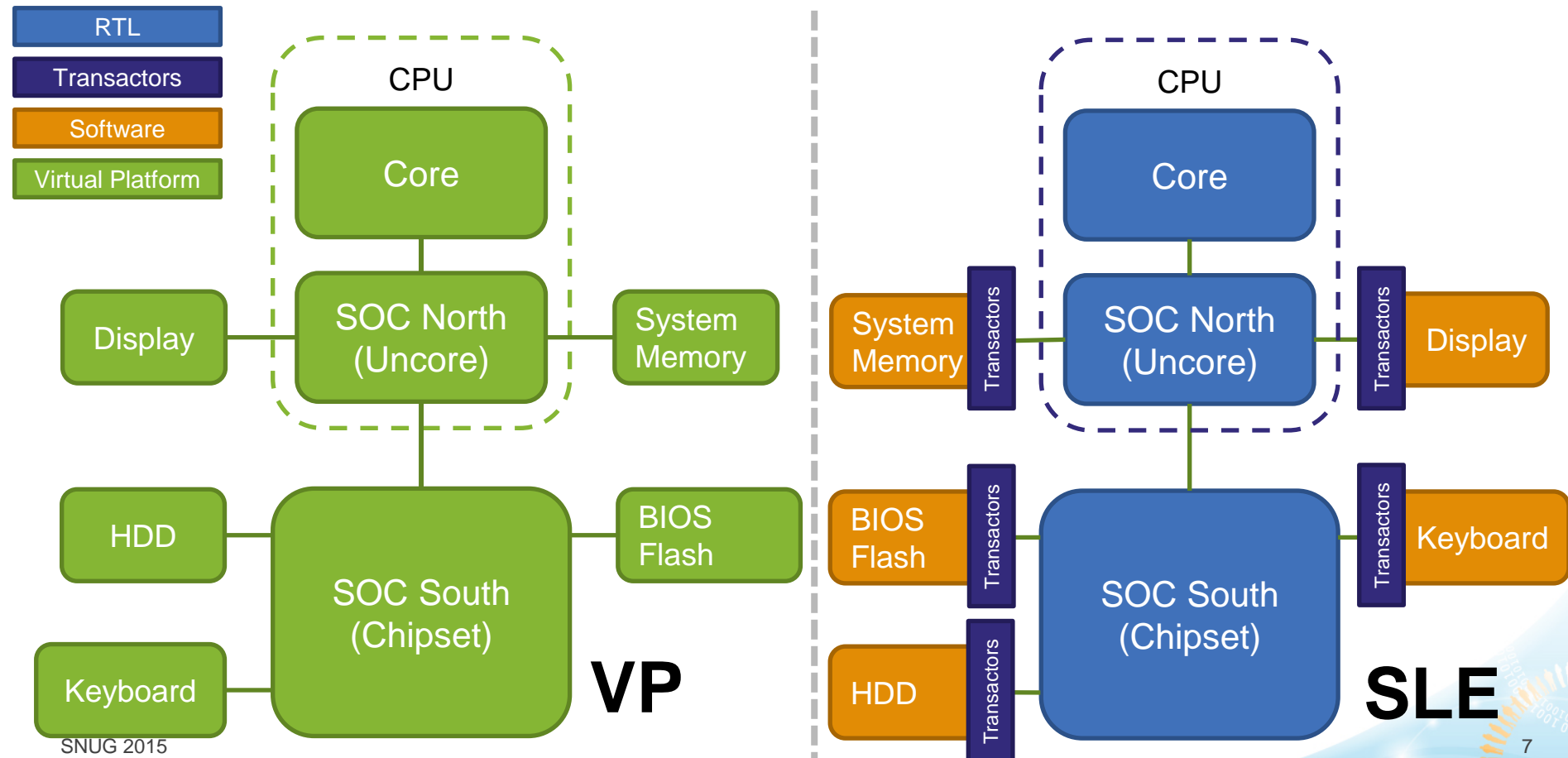
Think Platform



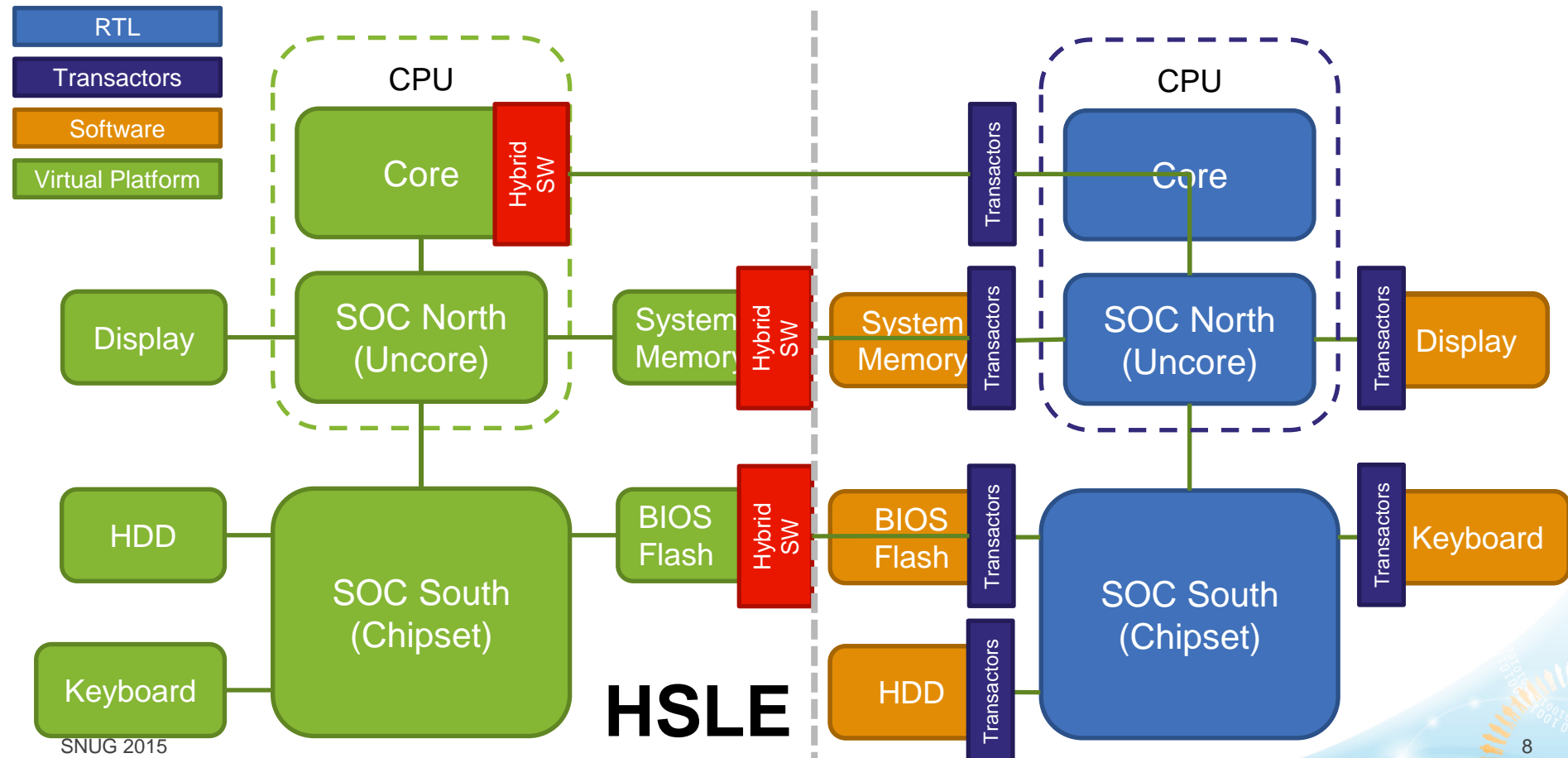
Pre-Si Platforms We Use

	Virtual Platform (VP)	Emulation (SLE)	Hybrid Emulation + VP (HSLE)
Properties	<ul style="list-style-type: none"> High speed functional simulator Good debug-ability Early availability 	<ul style="list-style-type: none"> RTL accuracy Good debug-ability Longer integration time 	<ul style="list-style-type: none"> RTL accuracy + functional accuracy Great debug-ability Less expensive by ~33% (#boards)
Drawbacks	Not the real HW	Low runtime speed vs. VP/FPGA Expensive (\$)	Single outstanding transaction from Core
Use Cases	<ul style="list-style-type: none"> Software and Firmware development 	<ul style="list-style-type: none"> RTL development and validation 	<ul style="list-style-type: none"> HW/SW Co-validation System use case validation
Time for OS Boot	Minutes	Weeks	

Bringing the Platform to Life

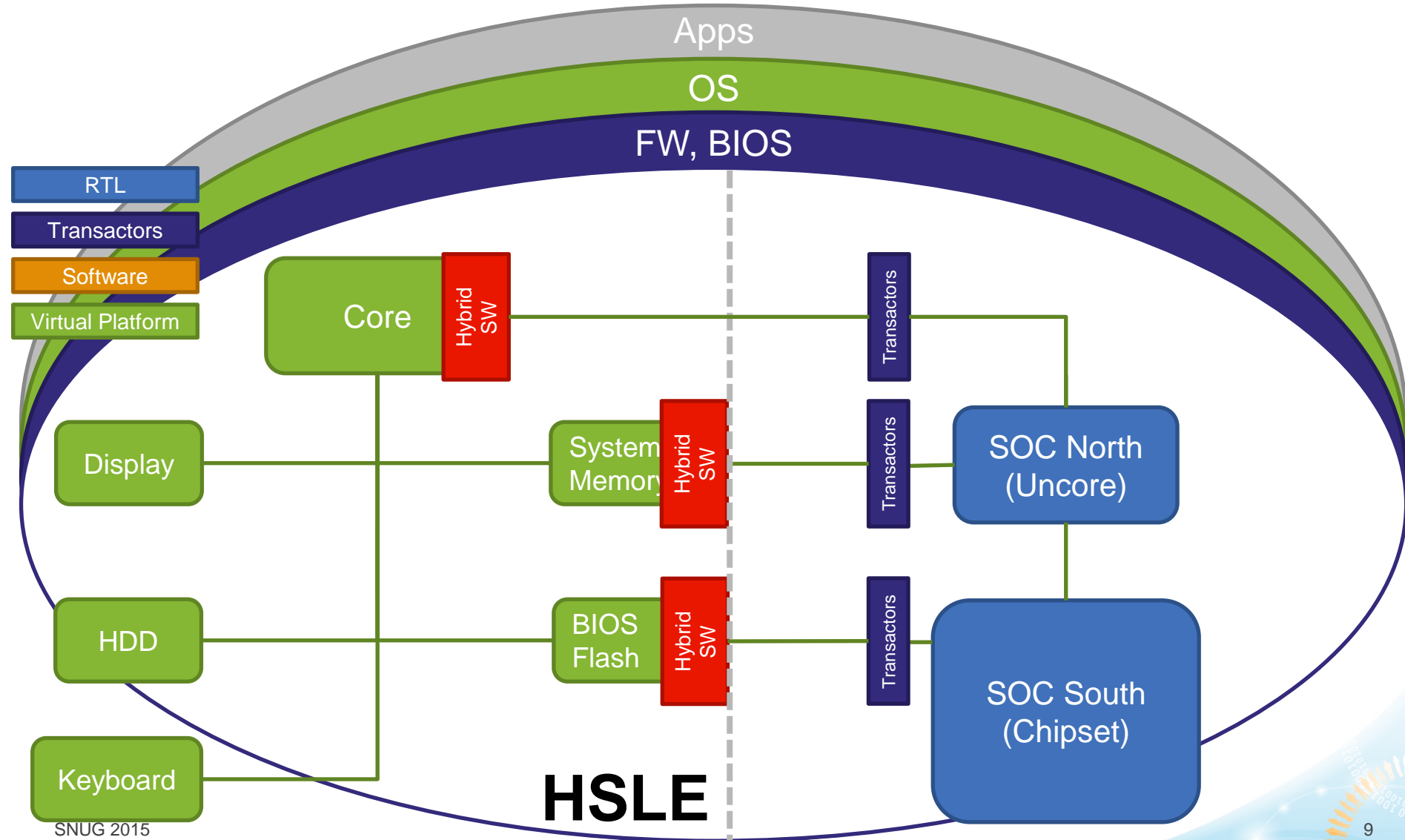


Bringing the Platform to Life



Bringing the Platform to Life

Enabling the use case: Execute OS based validation with production SW stack Pre-Si




Technical Challenges

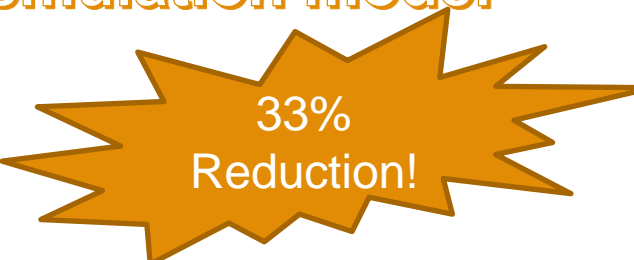
- The hybrid SW bridges the gap between levels of abstraction
 - Keeping both platforms “unaware” of the hybrid connection
 - SLE is RTL level accuracy
 - VP is architectural level simulator
- HSLE partitioning – Balance between emulation and VP
 - Balance validation coverage and runtime performance
 - Different configurations for different use cases
 - Execute code at VP speed boosts the effective performance
 - System memory and BIOS flash in VP
 - What about other devices? e.g. HDD, keyboard, display, etc.

Results

- The hybrid SLE partitioning significantly **increases effective performance**
 - Booting OS with production SW
 - Achieved speed of several hundreds KHz driver clock
 - Same as SLE
 - Dense and complex design fitted into ZSE1
- Removing the CPU core **reduces the emulation model size**
 - Better Utilization of Emulation Capacity



X350
Speedup!

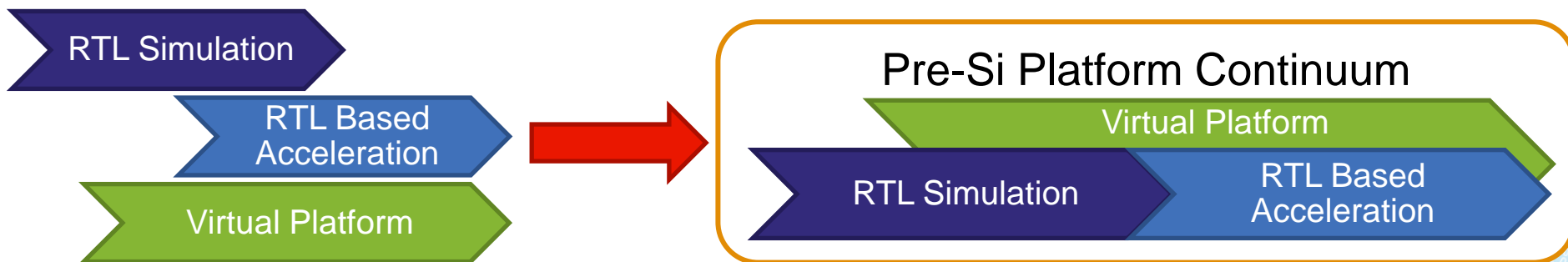


33%
Reduction!

Enabling use cases not possible with SLE

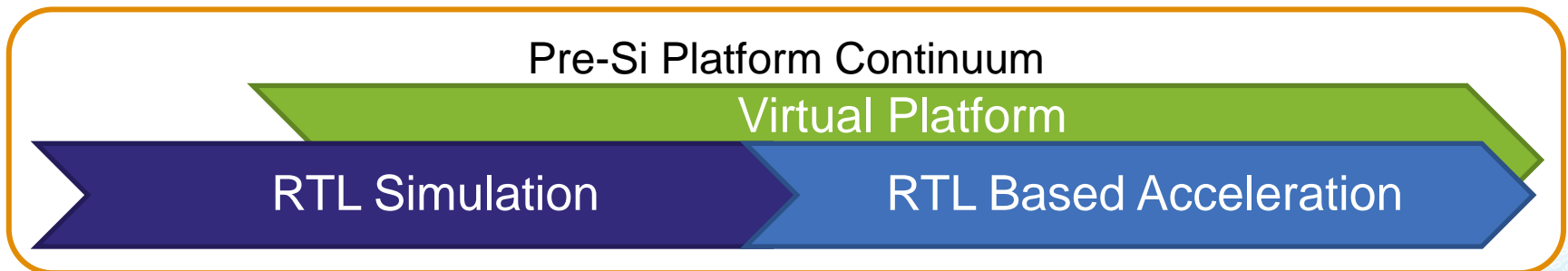
Result Retrospective

- We're taking advantage of a mature and stable VP and SLE
 - Intel is investing in development of a functional accurate VP
- Can we avoid effort duplication?
 - Share virtual device model between RTL simulation, SLE and VP
 - Share across products
 - IP vendors can provide virtual model and collaterals
 - EDA tools can enable reusing the same collateral across platforms



The Bigger Picture – Pre-Si Continuum

- The need for continuum across the product life cycle and seamlessly support reuse from platform to platform
 - Maximum reuse and minimal additional work per platform
- Easily reuse functional validation content across IP and integration
 - Reuse across different technologies and usage models
- → Develop software and firmware Pre-Si
- → Verify end product use cases Pre-Si



(*) Chris Lawless, Intel Corporation, EDPS 2014, California USA

(*) Bill Hodges, Intel Corporation, SNUG 2014, Texas USA

Summary

- Enabling SV use cases not possible with SLE
 - Booting OS with production SW executing SV applications
- Speedup effective performance → X350 speedup
 - Enabling Use Cases Not Possible With SLE
 - Some workloads are speed-up better (CPU centric workloads)
- Reduce emulation model size → ~33% reduction
 - Better Utilization of Emulation Capacity
- The need for continuum across the product life cycle and seamlessly support reuse from platform to platform
 - Need to shift our partners and vendors



Thank You

