Early Design decisions based on RTL Power Estimation

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ABSTRACT

Using RTL Power estimation, we can try to understand the direction of the design progression with respect to power consumption. We can also use RTL Power estimation to make early design decisions like choosing between different IPs that offer same functionality, but consume less power for the specific application.

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1. Introduction

In this modern era of chip design, there is a lot of emphasis on low power design. Low power design is the direction forward. With the emphasis on shorter time-to-market, there is a growing need to explore various techniques that can help in achieving this goal. In the current traditional design flows the power usage details are not available till the design reaches implementation phase. If the power numbers are too high, the possibility of decreasing the power consumption is only through efficient implementation and floor planning. If we want to decrease the power through efficient RTL, the time to market target may be very difficult to meet. With shorter and shorter time-to-market the need to get an indication on the power consumption early in the design cycle is paramount.

The use of tools like SpyGlass RTL Power Estimation can be very useful in this endeavor. The power consumption numbers at RTL level can indicate possible refinement of the RTL in a power context. Recently, a lot of companies are taking the re-usable IP approach. This approach provides us with a unique opportunity. With the availability of multiple IPs that can fit the need of a specific application, we have the option of picking the right IP that has low power consumption in the SoC and potentially help in reducing the power consumption drastically.

We started developing this idea and used a real time design that could be implemented using three different internal IPs. In this paper we present our results and possible next steps in refining the flow.

In the following sections we present the approach we took, results and conclusions.

2. Design

In the receiver design and implementation of wireless devices, phase to Cartesian conversion is commonly used in wireless communication protocols. Such conversion usually happens in the faster sample domains, coupled with high frequency system clocks.

The conventional approach for this conversion is to use a pre calculated cosine value Lookup Table (LUT), synthesized through logic gates to map the phase inputs to the Cartesian components.

Depending on the system requirement, the number of the entries varies. Using trigonometry logic manipulation, it is possible that instead of employing a full lookup table, designers commonly use a half table or even quadrature table in an attempt to reduce area occupied by the LUT itself.

However, while the true area benefit of using a partial LUT is debatable, as the clock rate increases, the speculation arises that the additional logic required to precondition the phase input in order to use the partial LUT has a tendency to consume more dynamic power.

In order to prove this speculation, a dynamic power estimate tool, which takes into account of technology library, accurate wire load model through reference design, clock rate, and very importantly, the activity profile is required to provide the data point on this.

In this test run, we experimented with all three implementations in Verilog RTL models, a full LUT, and a Half LUT and a quadrature LUT respectively. The activity profiles for each implementation are collected through RTL simulation with actually channel model and realistic input for the duration of receiving interval. All toggle activities are recorded in VCD format. The wire load model was collected through a reference design in the same technology.

3. Flow

In this paper we used SpyGlass RTL Power estimation tool box to analyze a top level design that has a Look Up Table (LUT) in it. Fig. 1 illustrates the inputs and outputs to the tool. The inputs and outputs remain the same irrespective of the tool used. The inputs provide a way for the tool to do a primitive synthesis of the design. The stimulus information will allow the tool to calculate the power consumption results.

By using this basic setup, we can run multiple scenarios. We can start to explore the change in results by changing any one or more of these inputs. For this paper, we focus mainly on the effects of changing the RTL.

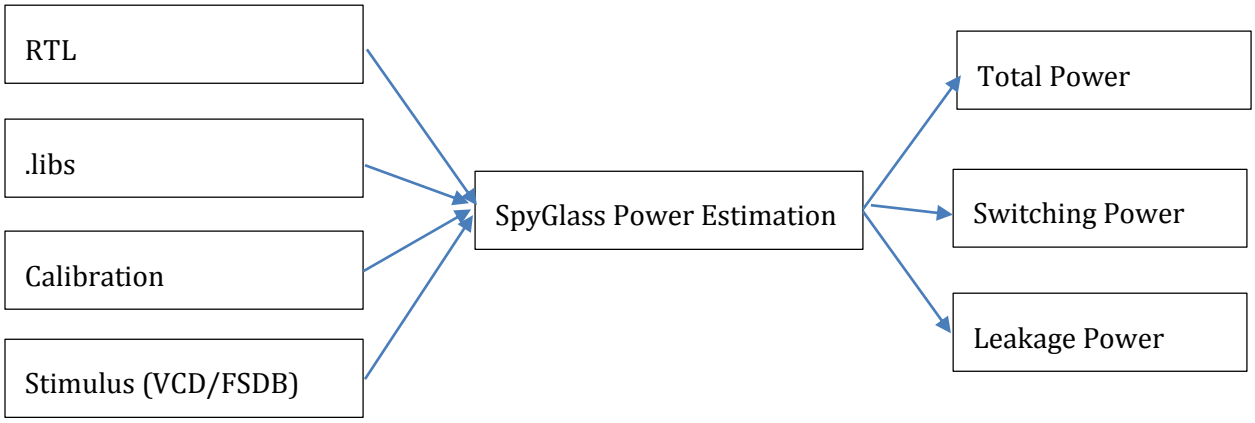

Figure 1: Inputs and Outputs

The results of the flow are categorized into total power, switching power and leakage power. The switching power pertains to the power consumed by the block during toggling phases. This information is very useful when identifying the high power consuming blocks in the design. These effects are explained in the next chapter.

3.1 Calibration

Calibration data is the information about the cell allocation data, VT mix percentage and defining the clock tree. This information is necessary to get useful results from the tool. This data is used by the tool when running power estimation along with wire load model to predict power consumption of the design. Accuracy of the results is highly dependent on supplying a well-constructed calibration data.

Obtaining this data is rather simple when you have a legacy design. Cases where legacy design in available, using SPEF and an associated gate level netlist, calibration information can be generated quickly.

However, for a new design the designer may have to come up with this data manually. Possible ways to get around this may be to use a similar design, that is functionally similar and uses the same technology node as the current design, that has a SPEF and netlist available to generate the data. The designer should verify all this information before using it.

We have observed that for any power estimation tool this data is extremely necessary to get accurate results.

3.2 Stimulus

Another important piece of the flow is a well-defined stimulus. A stimulus that covers wide range of scenarios can help pin point the high power operating conditions well before hand. This information can be used to identify potential modules ripe for optimization.

Running power estimation in vector less state cannot estimate switching power usage and these results are not useful to perform any type of optimization. To avoid this, in primitive design where availability of a well-structured stimulus is a problem, the designer can opt to use an estimate switching activity. This will generate moderately useful estimation numbers.

In our observations, using a well-defined stimulus is a lot more effective than using an estimate switching activity. The estimate switching activity will fail in identifying peak power and corresponding operating conditions.

4. Results

The design used for this paper operates at 32MHz and employs cmos090_lp9tm1tfs technology node. It has an internal block that performs a LUT function. Because of the flexible nature of this design, the LUT function can be performed in three different ways. By using a full, quad or half LUT. Since all three LUTs are standard IPs, their external interfaces are consistent which allows replacing one for the other with relatively low effort.

As established in the earlier sections, with the setup in place, it is relatively easy to run multiple scenarios with one LUT at a time. Fig 2 illustrates how the power consumption changes by using different LUT. The design power consumption is clearly lower when a full LUT is employed. These results can be used as a basis to make design decisions.

If the design does not permit swapping of IPs, these results can also provide an early insight into which IPs are consuming high power. This allows the designer to take a hard look at the high power IP and refine them as much as possible. SpyGlass also provides power reduction suggestion but it is beyond the scope of this paper. The confidence in using the results depends on the tool reliability and a well worked out setup.

Further analysis of the results identified that the design has a 60% clock gating efficiency. This information was used to improve the clock gating by inserting additional clock gates whenever possible. Note that adding clock gating will result in slight increase of power consumption, so it is benefitial to run another iteration to verify that adding additional clock gating is in fact having a positive affect on the design.

We have also identified high power consuming operating cycles and used the results to optimize peak power usage by adding additional switching controls. We have reduced the total power consumption by a factor of 28% even before implementing cell optimization techniques.

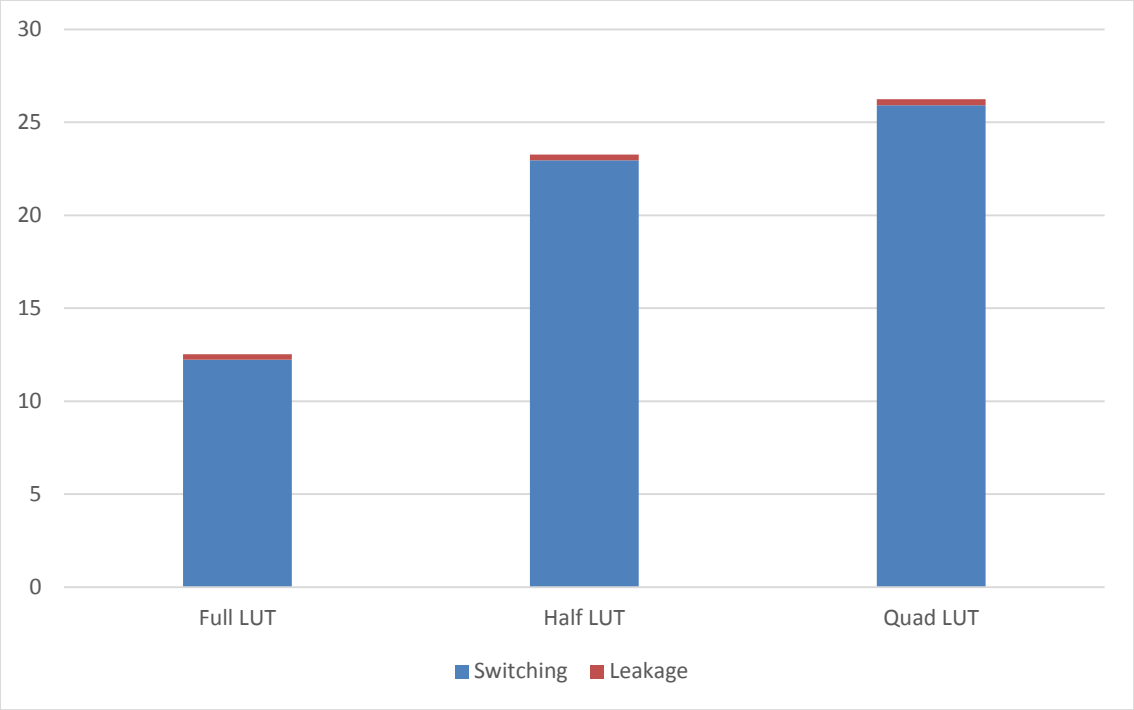

Figure 2: Power Consumption comparison

5. Conclusions

As the need for low power designs increase day by day, there is a growing need to explore various avenues to decrease power. The traditional flows do not provide with a power consumption results till implementation phase. By this time there is very little refinement that can be done to RTL because of time to market considerations.

With the increased reliability of the RTL Power Estimation tools, we can explore power savings very early in the design cycle. This early power information can be used to identify potential issues with the IPs well before the implementation stage. This helps the designers to take a hard look at the high power IPs and start to identify possible solutions.

The solutions we suggest in this paper are IP swapping whenever possible and RTL refinement. The focused results can pin point the blocks in the design that are ripe for refinement. With relatively easy setup, the designer can run multiple iterations and take advantage of the reduction suggestions from the tool.

6. References

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