



Exploring Protolink

Effective Debugging from Firmware to Hardware

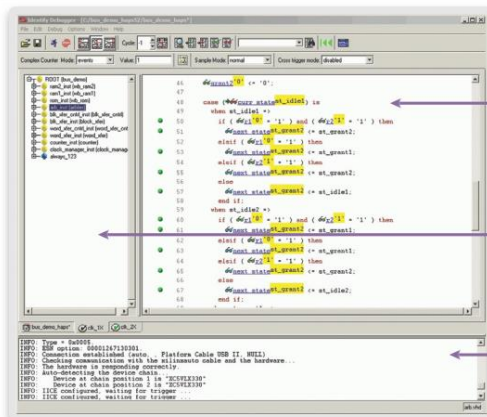
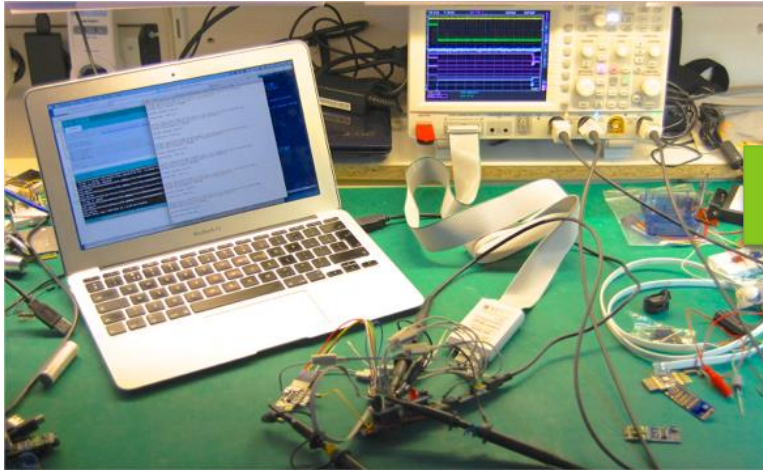
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“The World’s Smartest Debugging”

Debugging Scenario



RTL source view: Allows you to easily instrument and select the design parts on the RTL level that you would like to monitor and debug

Design hierarchy view: Allows selection of any level of the design for display of the RTL source code

Command line view: Provides access for using TCL commands and scripts, command history, and debug logic size estimates during instrumentation

Figure 1: The powerful Identify Debugger GUI allows you to quickly navigate through your design and to debug the RTL source code



Make the world a better place...

.....at least for our engineers

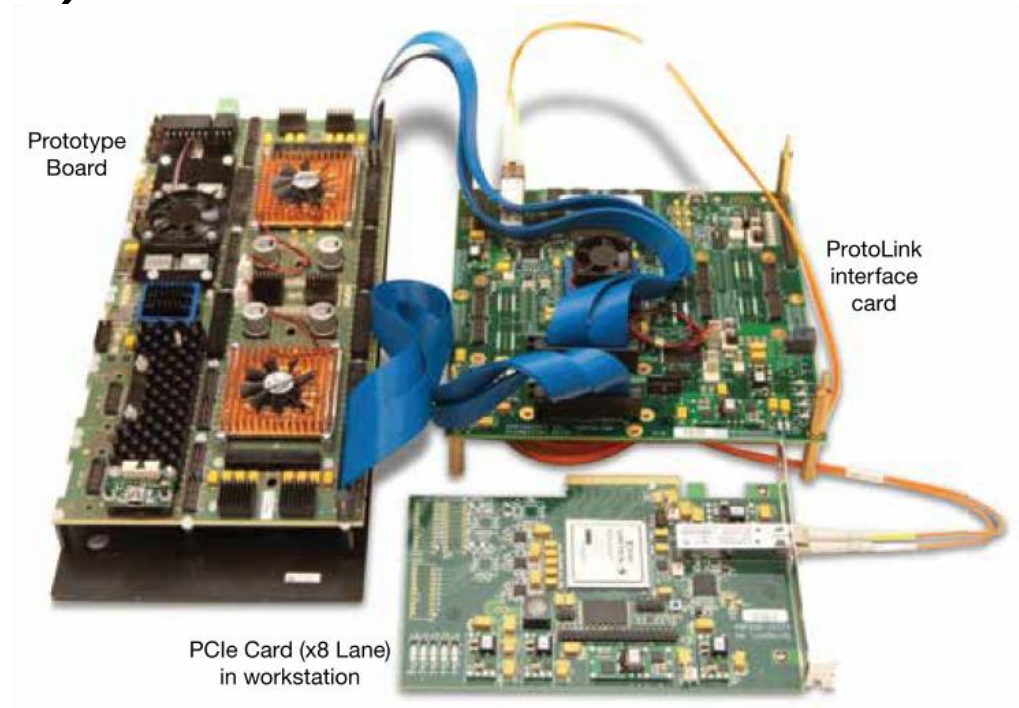
- **Imagine if you could...**

- Found bug easier
- Fix bug quicker
- Go home earlier
- Product will be stronger
- Revenue will look better
- Number on your pay slip will be bigger

Three Inspiring Stories for Free

-What is it? What can it do?

- ***Long capture length(<1s)***
- ***High speed (125MHz)***
- ***Easy connection***
- ***Easy to use***
- ***Fast eco***
- ***...***



Case Study

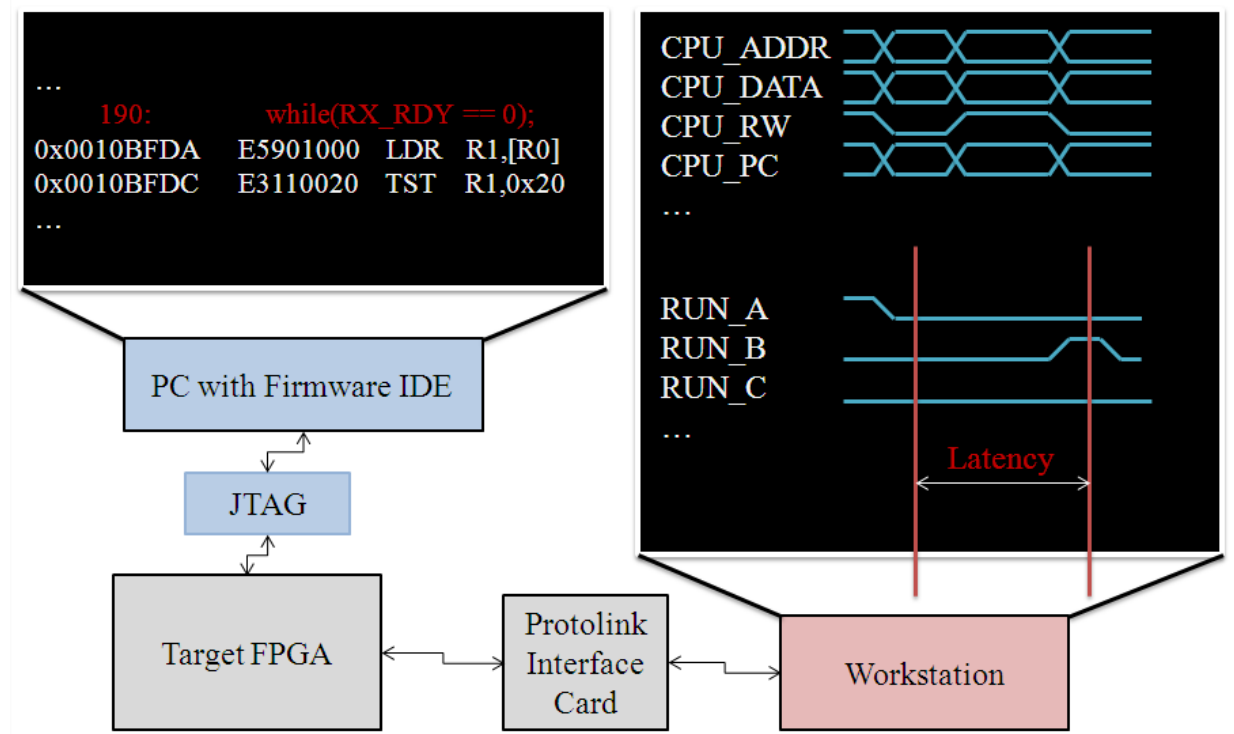
Firmware Flow Tracer

Firmware Flow Tracer

-Performance monitor

- Before
 - Output value to GPIO as check point, capturing by Logic Analyzer
 - No hardware latency information

NOW=> Performance measure by firmware check point, with the ability of analyzing Hardware Event at the same time

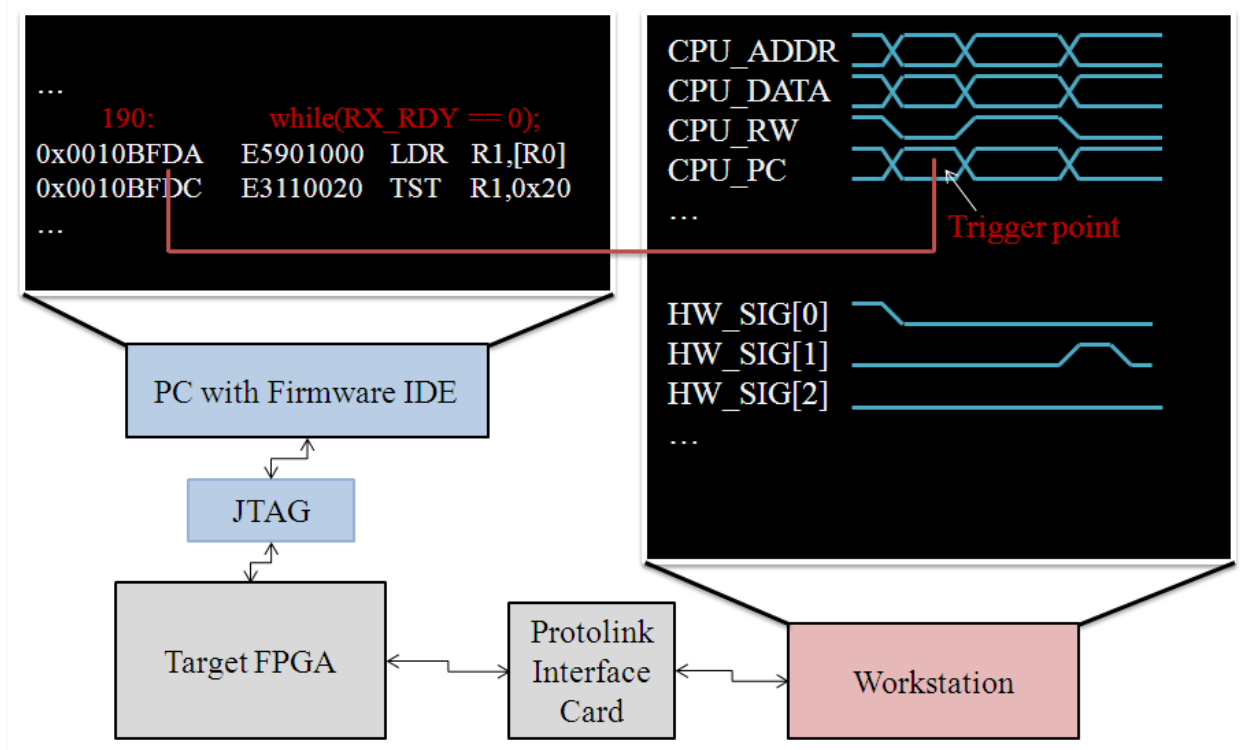


Firmware Flow Tracer

-Firmware execution and hardware status mapping

- Before
 - Error occurs while Firmware “Freerun”, often under RTOS
 - Firmware engineer debug purely by experience

NOW=> Further investigate into firmware flow by mapping machine code. Able to distinguish whether it is a firmware multi-task scheduling issue or an actual hardware bug

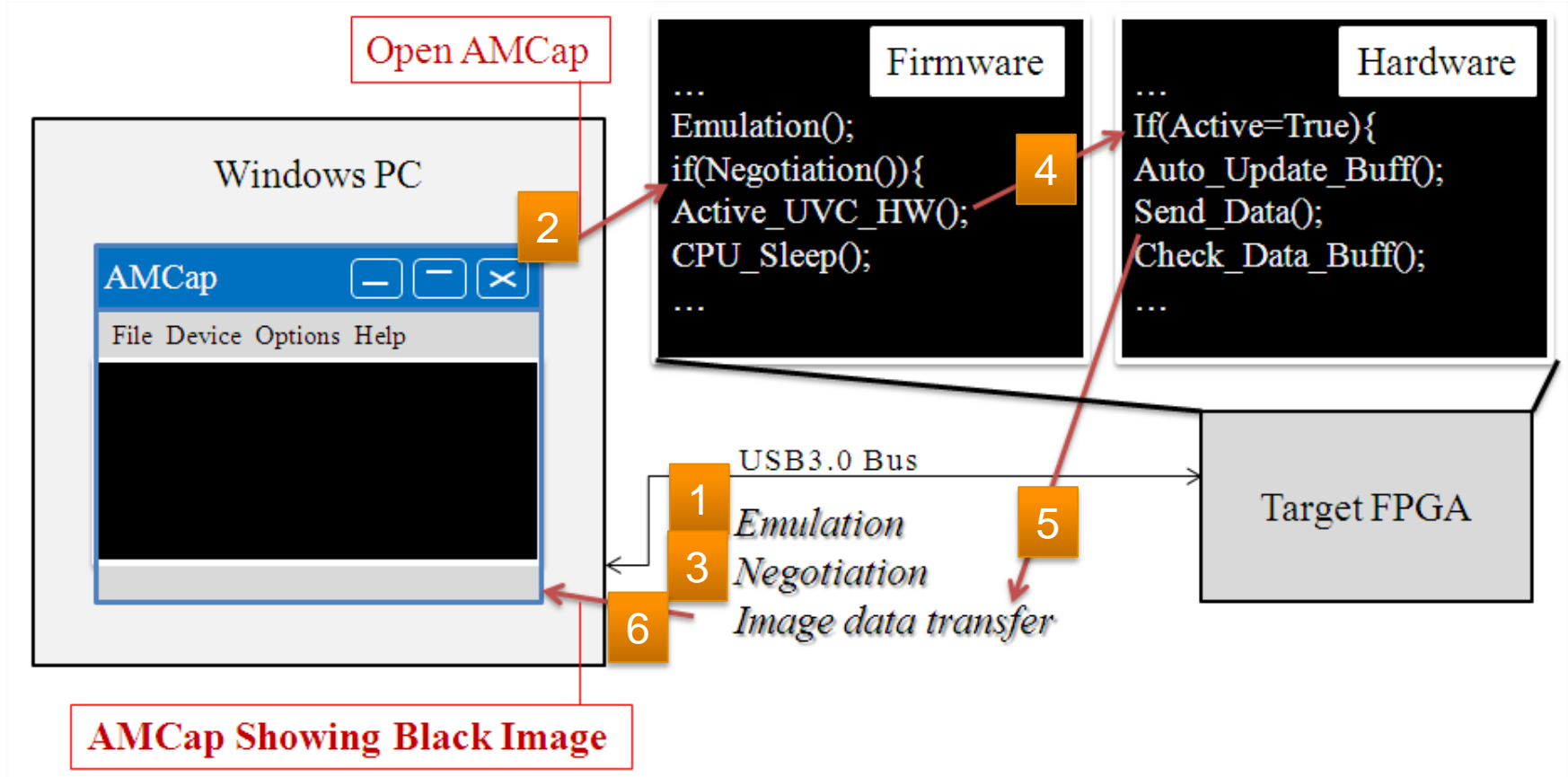


Case Study

Synchronize with 3rd Party Debug Tool

Problem: no Image shown on AMCap

-UVC Controller malfunction?



- AMCap will not display correct image unless it received correct data. (format, frame size...)

Found: Oversized Image Payload

-UVC Controller malfunction! But now what?

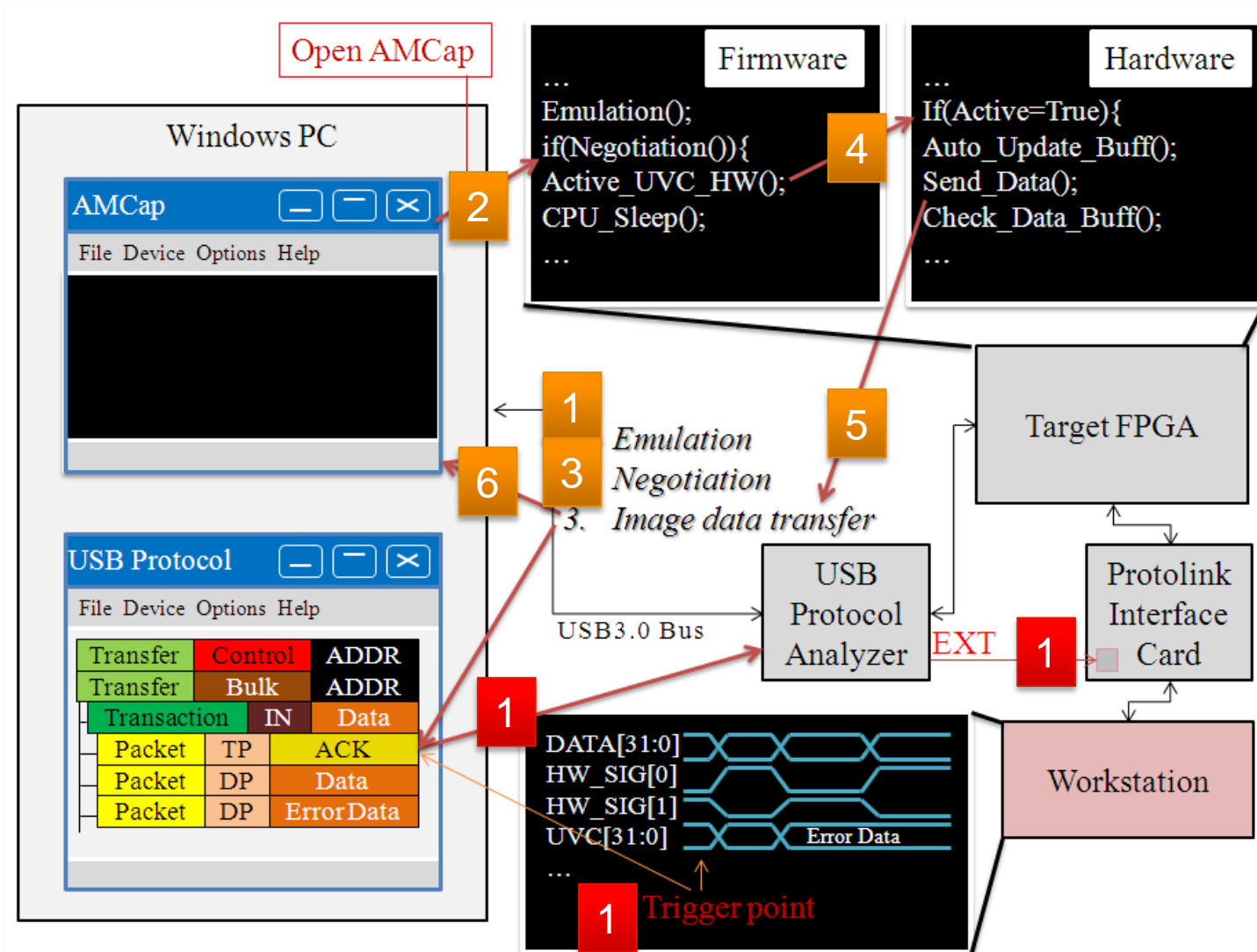
- Oversized Image Payload occurs randomly, so there will be no hardware trigger point
 - Identify relies on specific trigger point
- It takes 33ms to transfer entire data of one Image Frame
 - Duplicate in Simulation environment is impossible
 - Still no specific hardware trigger point

Before => No solution!

Solution: Sync with USB Analyzer

-Capture hardware signal for almost 1s!

**NOW=>
<2 Days**



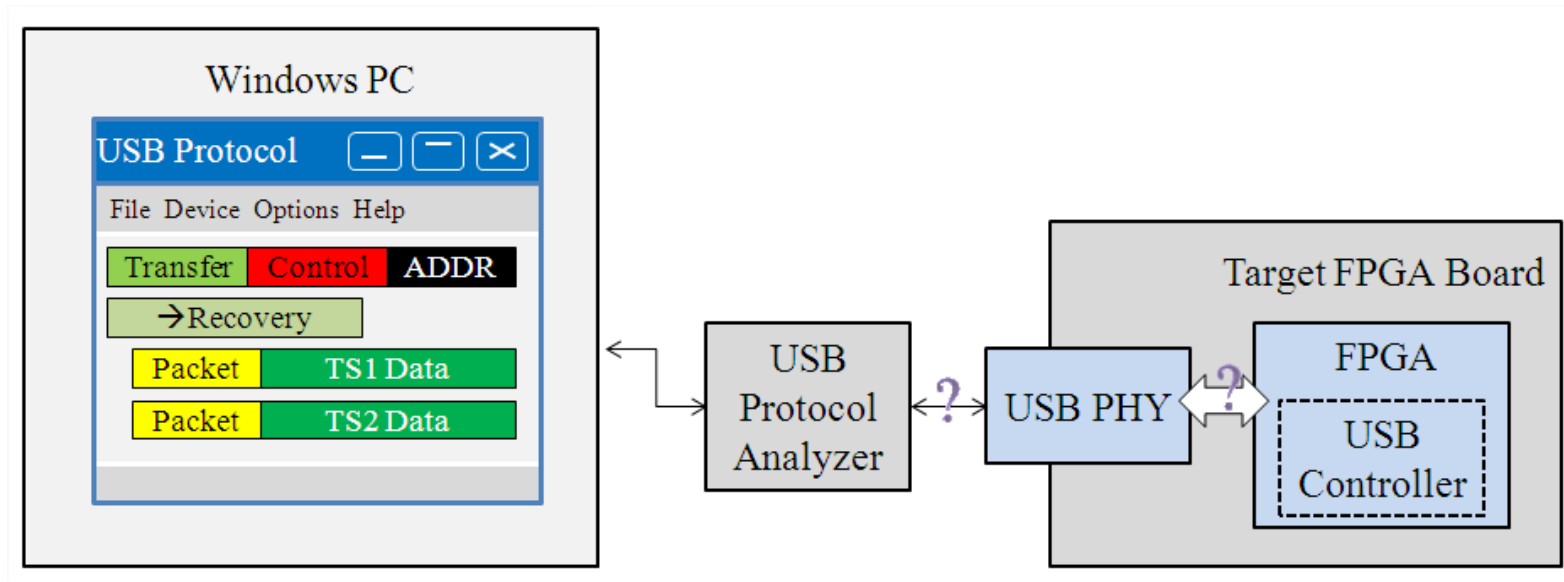
Case Study

125MHz USB3.0 Interface Debugging

Problem: Unexpected Recovery

-the source of incorrect link packet?

- Enter into Recovery mode randomly during “burn-in”
 - Performance drop
 - Potential design flaw

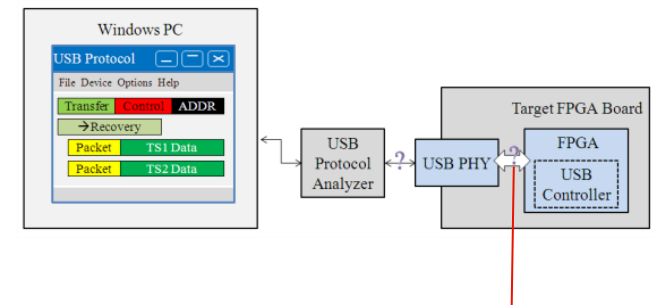


Who's to blame?

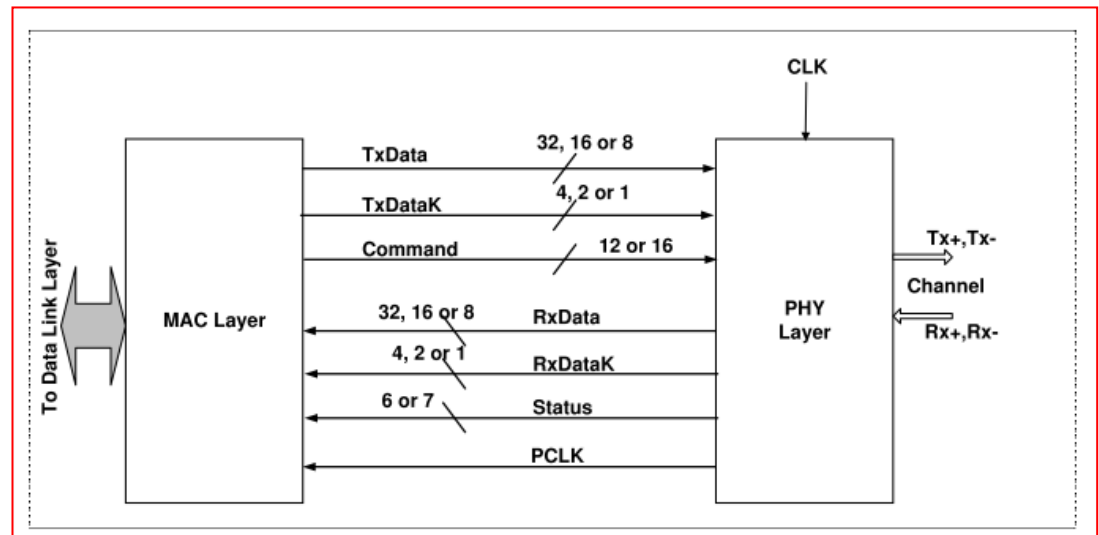
Solution: 125MHz Probe & Sync

-Easy to setup

- 125MHz PCLK as Protolink Synch Probe Clock
 - Max user clock (TDM=1)
- Synchronize with 3rd Debug Tool
 - Trigger “Recovery”



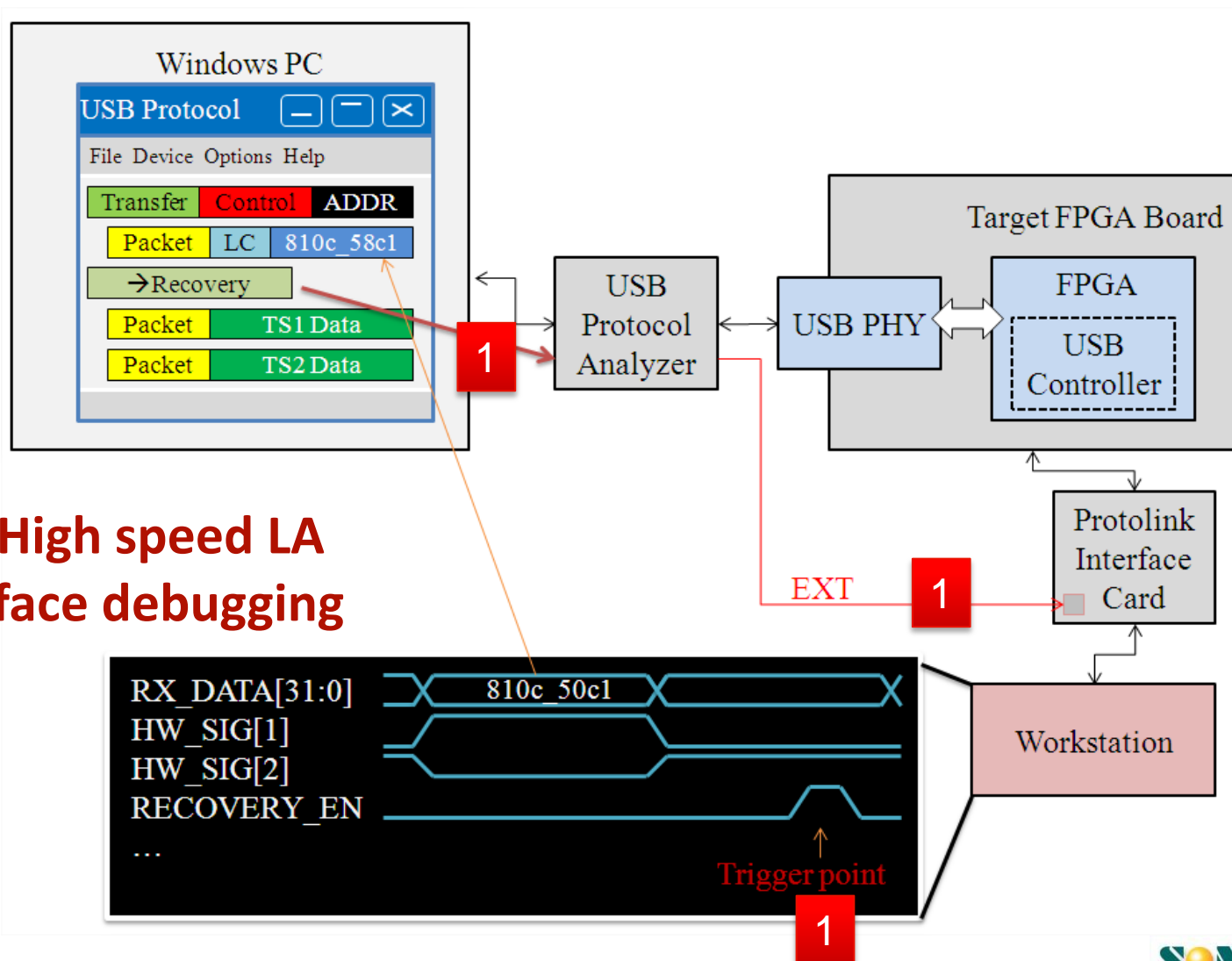
Note: Only 64*6 probe signals are allowed at 125MHz Synch Probe mode.



Result: Quick Clarification

-PHY or Board level issue

**NOW=> High speed LA
for interface debugging**



Summary

- Better co-working between firmware and hardware engineer
- Sync with other debug tool => Trigger point
- Feel safe
- Drawback: Feel terrible when going back to LA/Identify debugging!



Thank You