A Novel Waveform Generation Methodology for Power Estimation

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SNUG Taiwan

Agenda

Motivation

Basic Concept of Siloti

Proposed Methodology

Specification of FSDB Merge & Replay

Steps and Corresponding Inputs for FSDB Merge & Replay

Results

Conclusions and Future Works

Motivation

- Low power is one of key competitiveness of mobile devices
  - Famous power failure case: *Qualcomm 810 overheating issue!*
- To make sure no surprise after tapeout, estimating power accurately is very crucial
  - High accuracy is guaranteed by using post-layout sim. pattern with post-layout netlist
  - However, it is very time-consuming and too late
- Siloti (PowerReplay) can generate post-sim like pattern efficiently
  - Siloti can generate many patterns for power/IR tool
  - But power/IR tool **requires many runs** to get whole power/IR info. of subsystem or whole chip
- Single whole subsystem/chip post-sim like pattern can save efforts and runtime of successive power/IR tool

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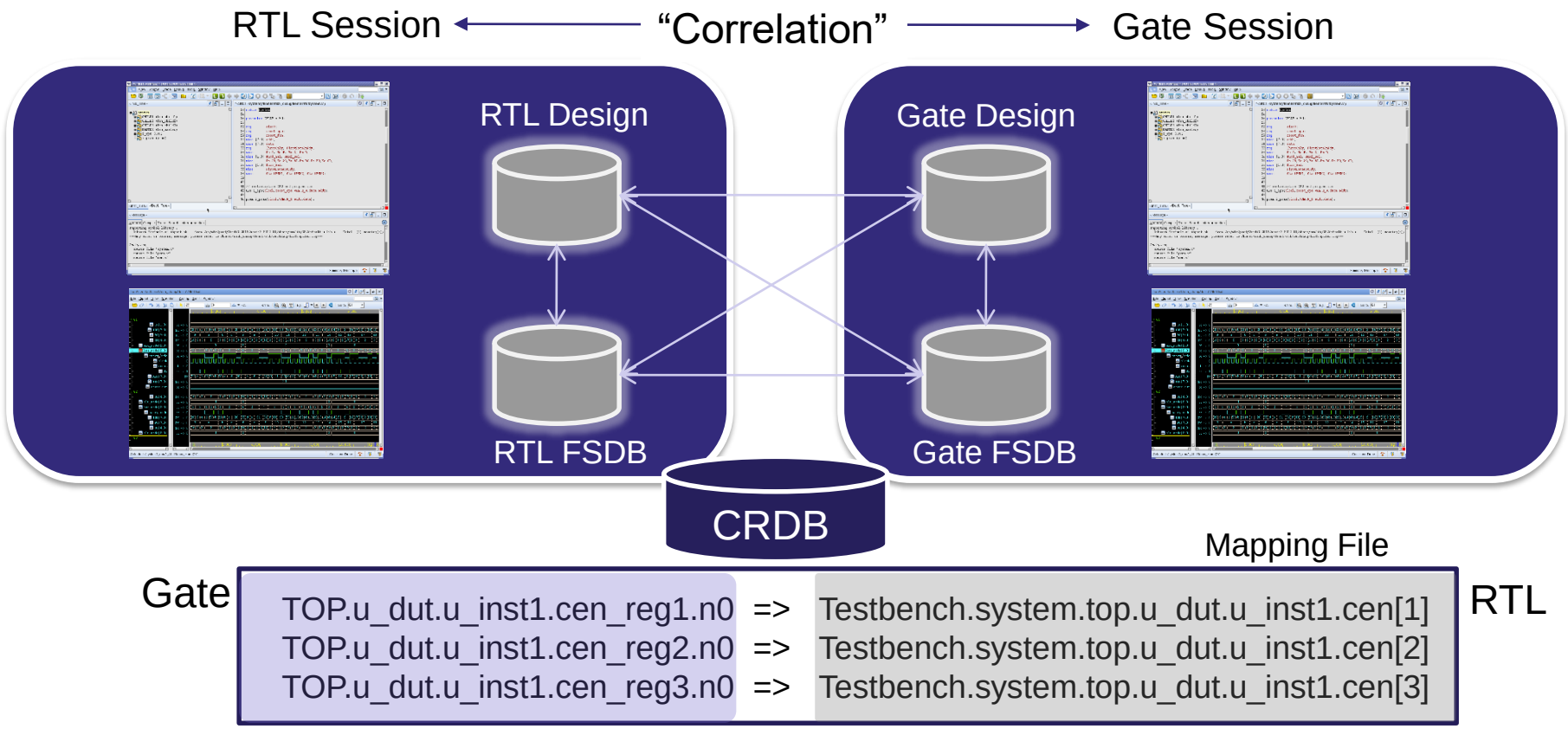
Siloti Correlation Technology

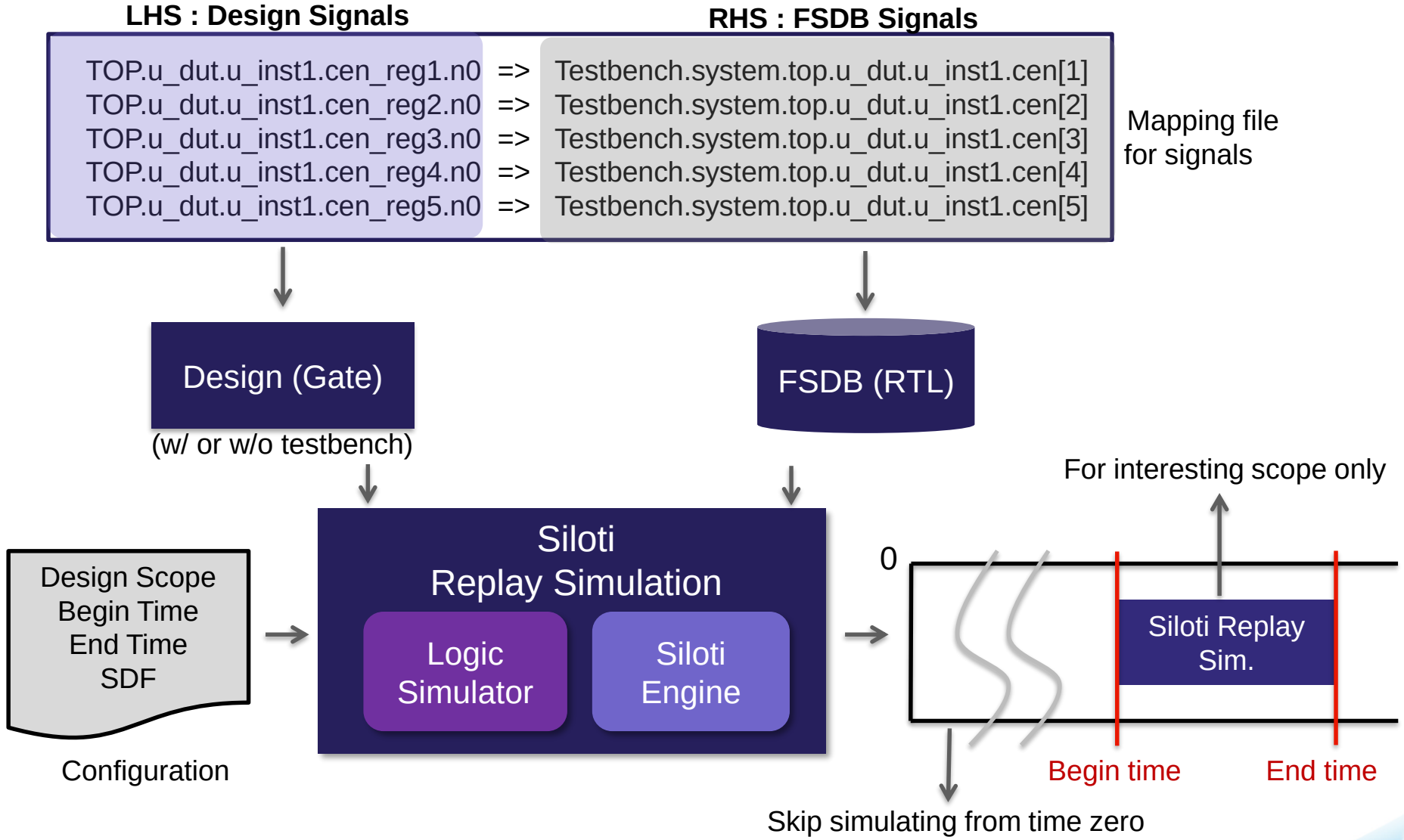
Cross-Abstraction Correlation and Debug



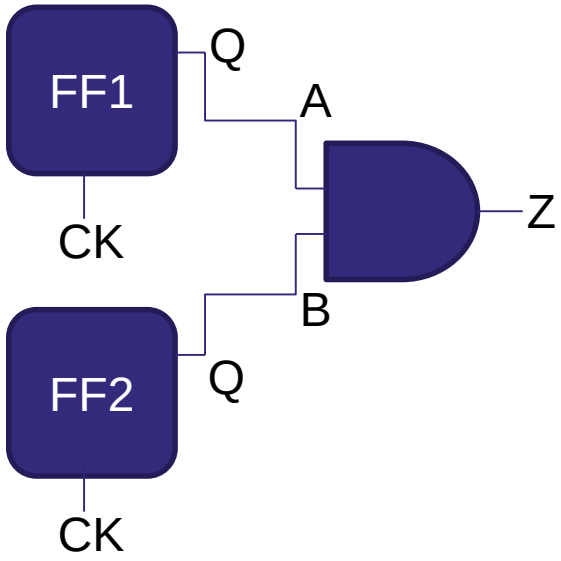
- Automatic mapping of signals between RTL and gate level design

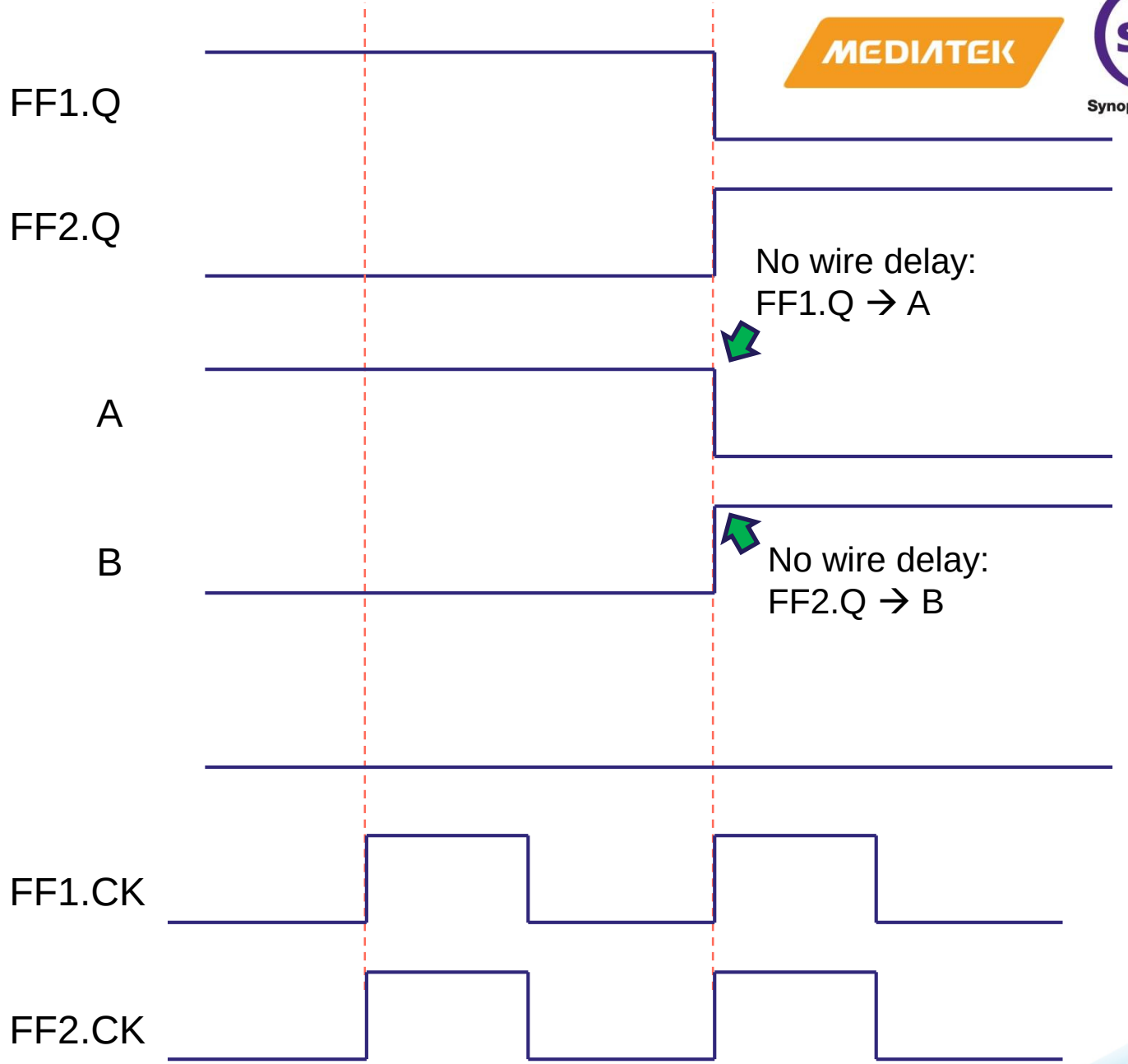
Siloti Replay Simulation Technology

Replay Gate Level Simulation with RTL Signal Inputs

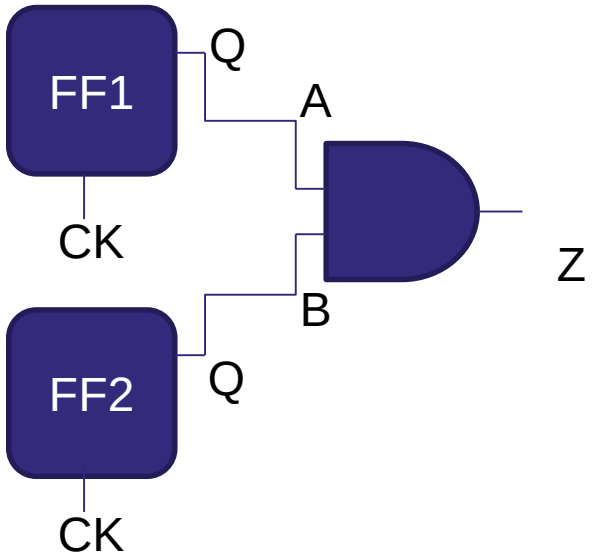


RTL Sim.

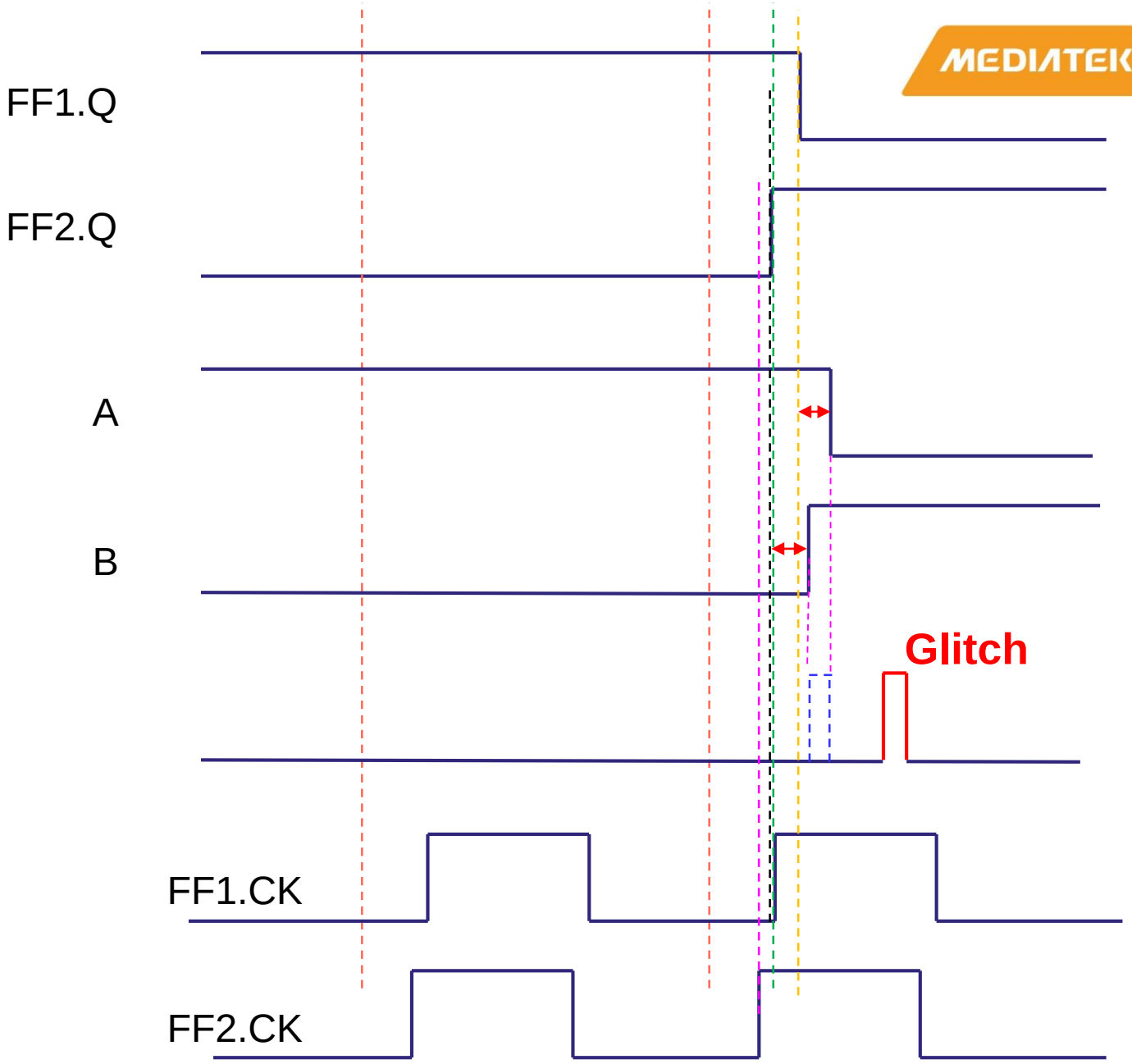

FF1
Q
A
Z
CK
B
FF2
Q
CK


FF1.Q
FF2.Q
No wire delay:
FF1.Q → A
A
B
No wire delay:
FF2.Q → B
FF1.CK
FF2.CK

Post Sim.

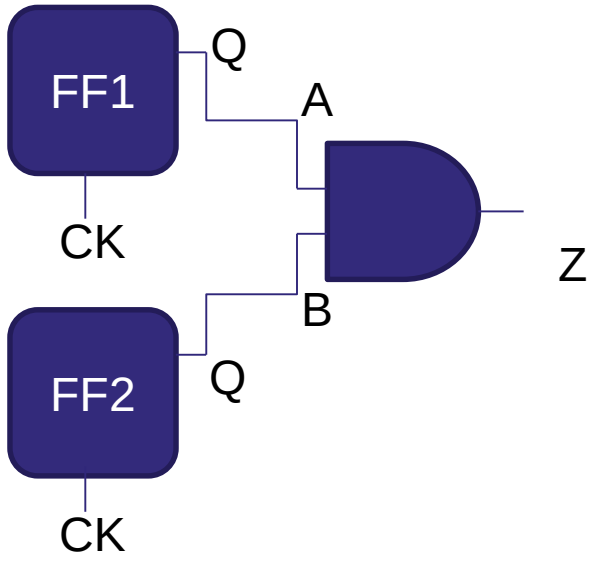


FF1.CK , FF2.CK arrival time of posedge delays

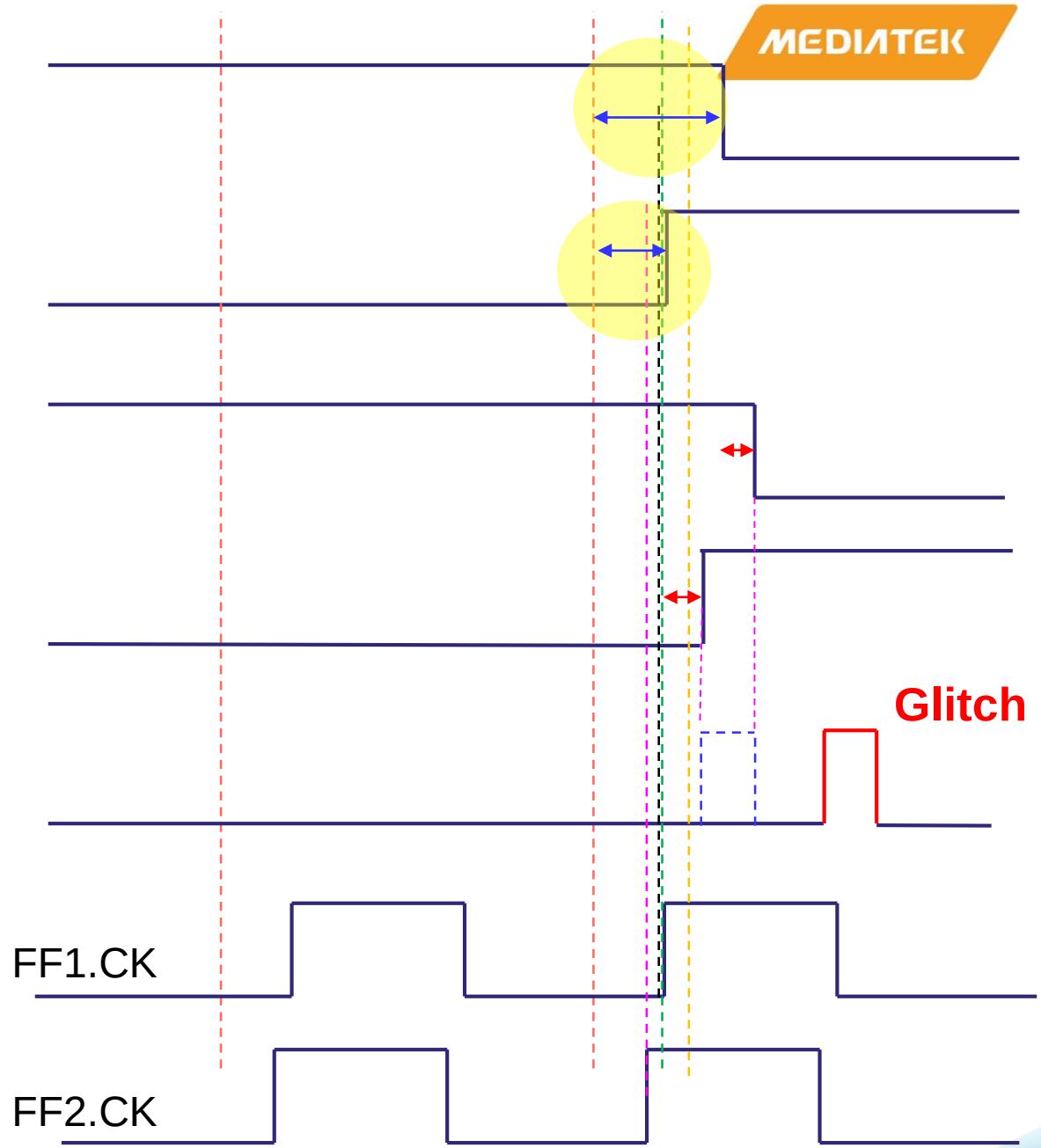


Siloti – Q-Delay

Q-Delay is extract from PrimeTime worst-case rise/fall delay



FF1.CK , FF2.CK arrival time of posedge delays



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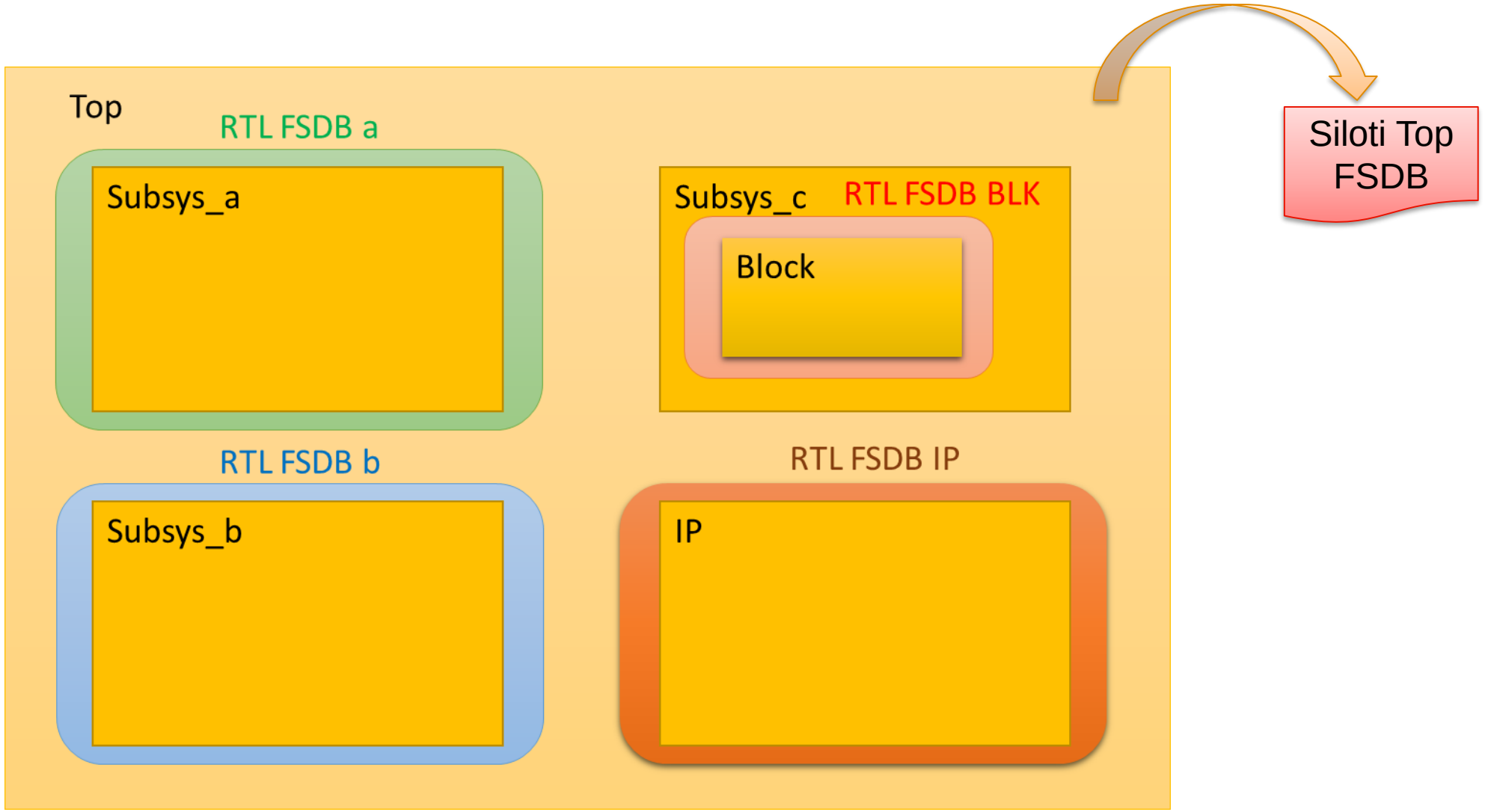
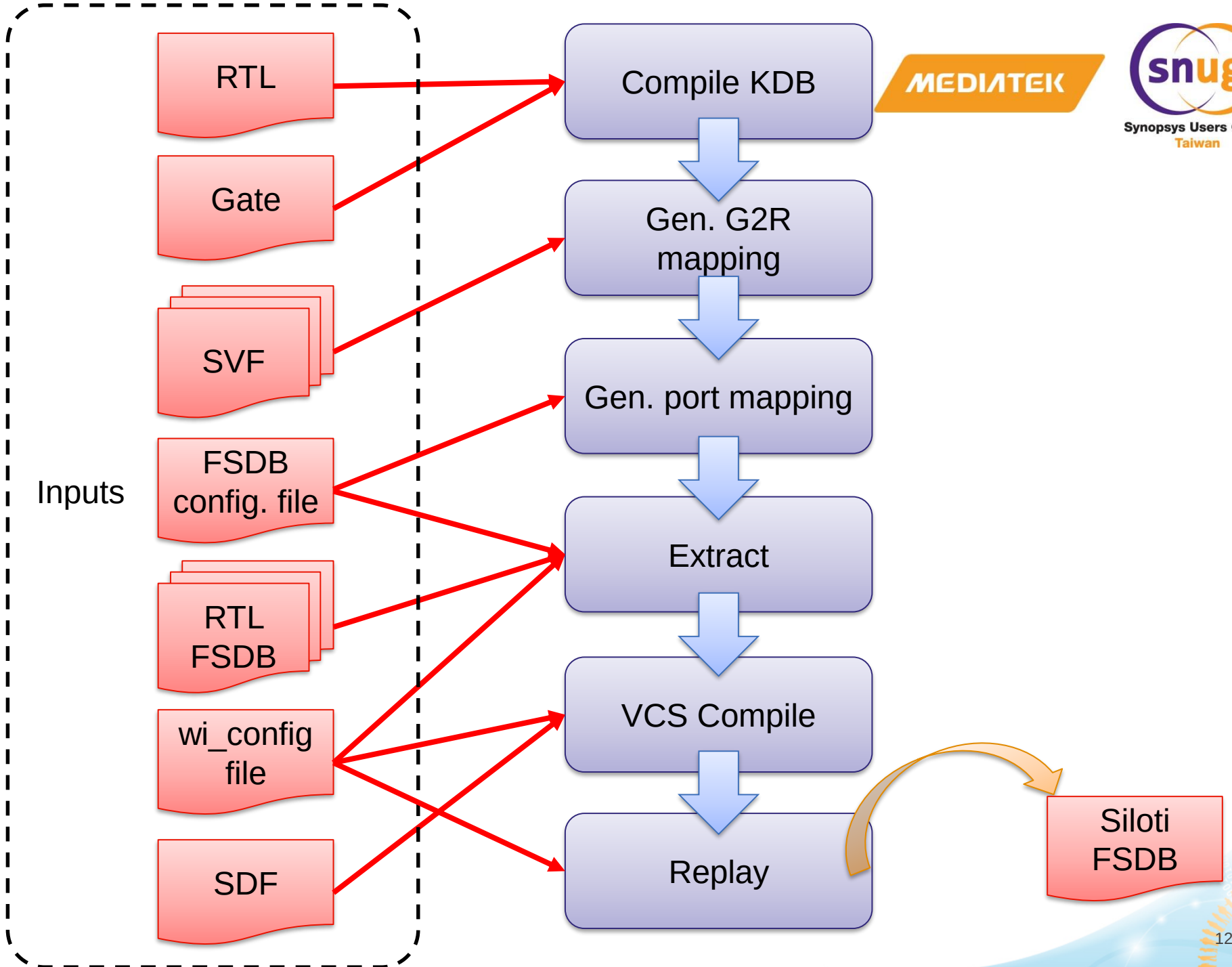
Concept: Concurrently Merging & Replaying RTL FSDBs



Proposed Siloti Merge & Replay Flow



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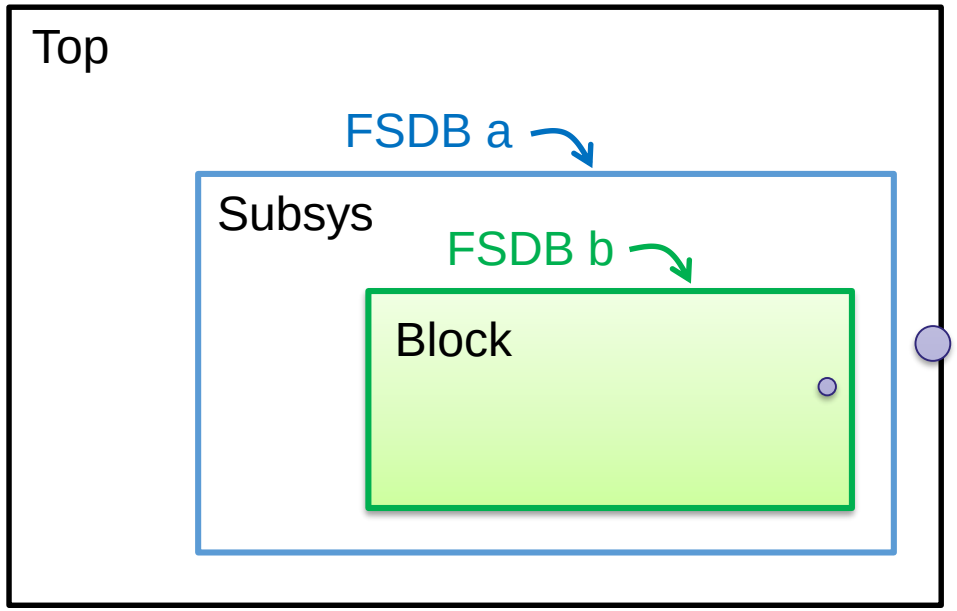
Specification of FSDB Merge & Replay

How to merge when replaying scopes have overlap?



Which FSDB should be replayed on “Block”?

Spec. “Last one win”

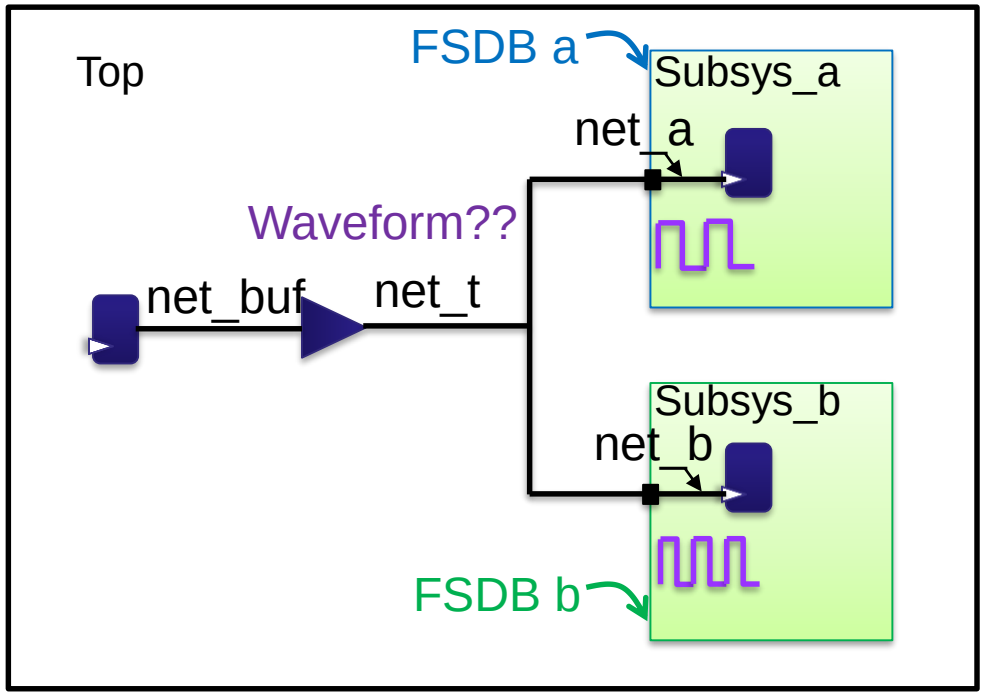
FSDB config. File:

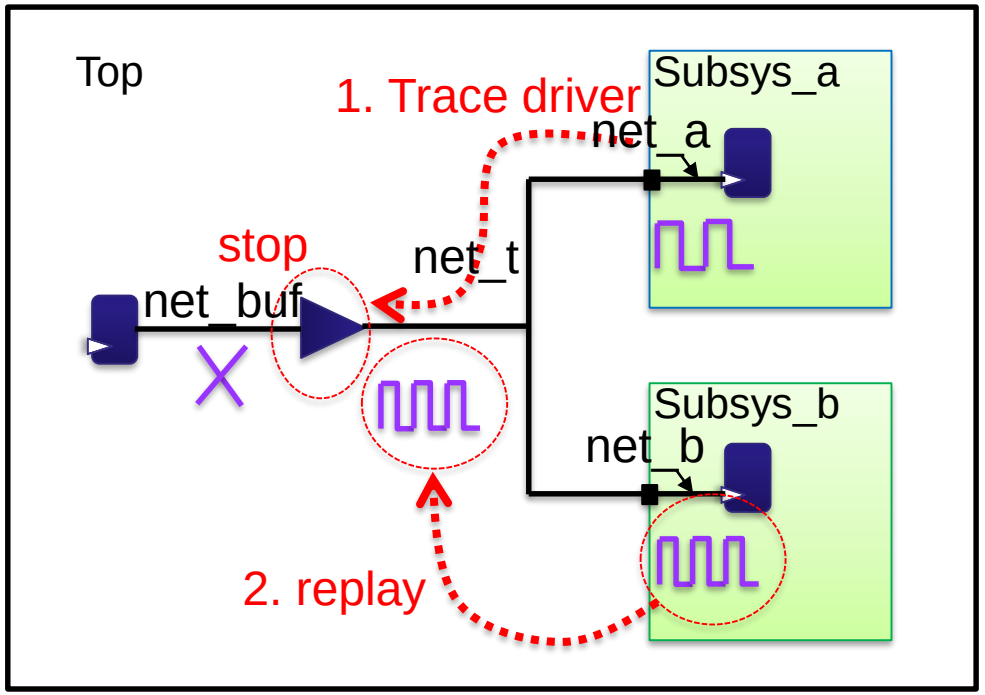
rtl_a.fsdb –begin_time 300ns –end_time 900ns –from_scope tb.Top.Subsys –to_scope Top.Subsys
rtl_b.fsdb –begin_time 5600ns –end_time 6200ns –from_scope tb.Top.Subsys.Block –to_scope Top.Subsys.Block

Specification of FSDB Merge & Replay (cont'd)

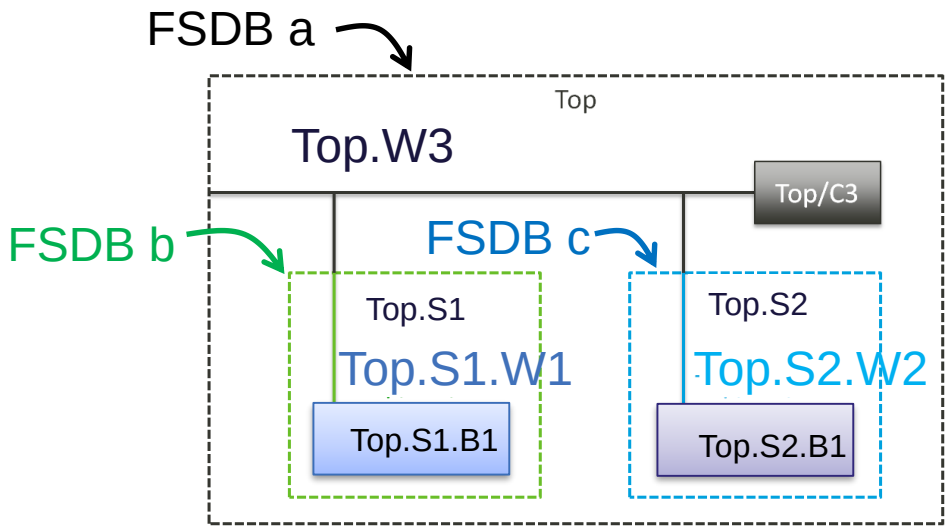
How to handle signal conflict?

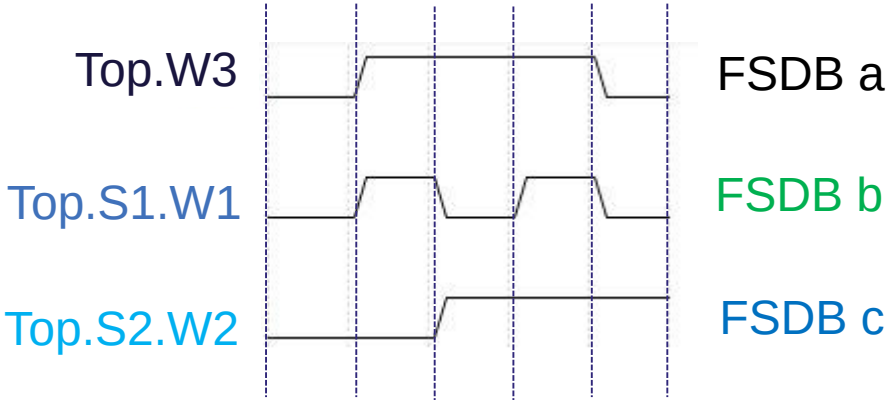
Spec. "Replay busiest one to source"





Convert Conflict FSDB to Average SAIF





Concept: "Resolve conflict signals by averaging their total toggles"

SAIF TC (Toggle Count) of "W3", "W2", and "W1": (2+4+1)/3 = 2.3

SAIF T0 (Total time at 0) of "W3", "W2", and "W1": (0.4+0.6+0.4)/3 = 0.47

SAIF T1 (Total time at 1) of "W3", "W2", and "W1": (0.6+0.4+0.6)/3 = 0.53

Note: SAIF is IEEE standard
=> converting to SAIF means 3rd party tool can use merged waveform as well

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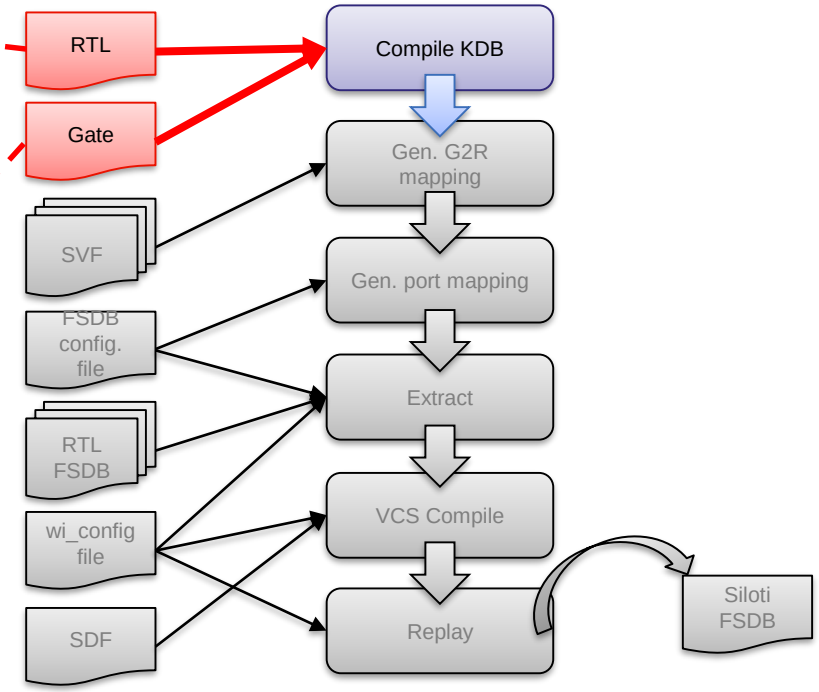
Step 1: Compile KDB

```
% vericom –sv –f rtl_file_list.f –lib kdb_rtl
% vericom –sv –f gate_file_list.f –lib kdb_gate
```

./kdb_rtl.lib++

./kdb_gate.lib++

Verdi Knowledge Data Base

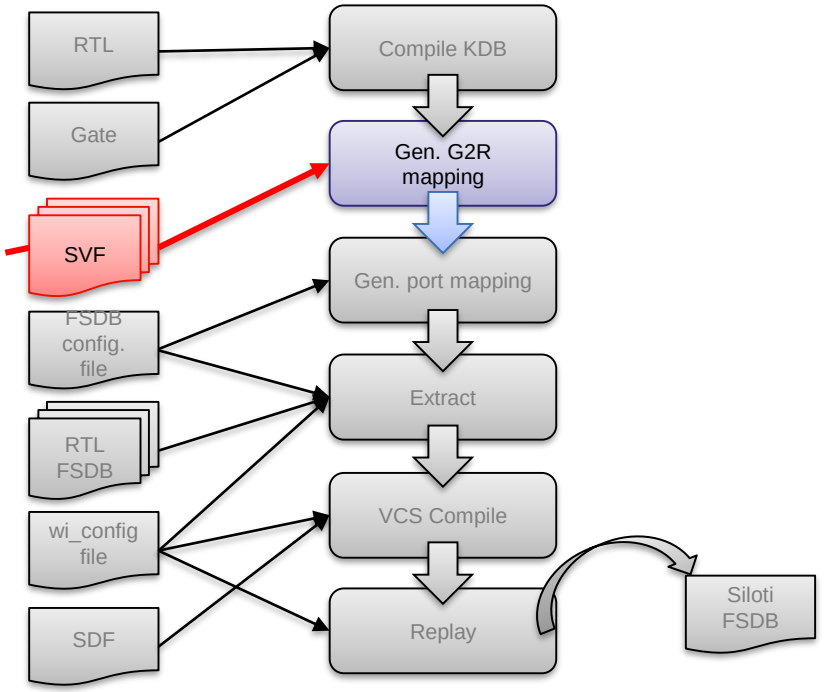


Step 2: Gen. G2R Mapping

./kdb_rtl.lib++

./kdb_gate.lib++

```
% crdb –RTL “-lib kdb_rtl –top Top” –GATE “-lib kdb_gate –top Top” \
-impSVF “Subsys_a.svf Subsys_b.svf Subsys_c.svf IP.svf” \
-target_scope “Top” –allreg –expGateUncor –top_inport \
-excludeModule vc_exclude_mod.list –expMap G2R.list.gz –crdb
G2R.crdb
```



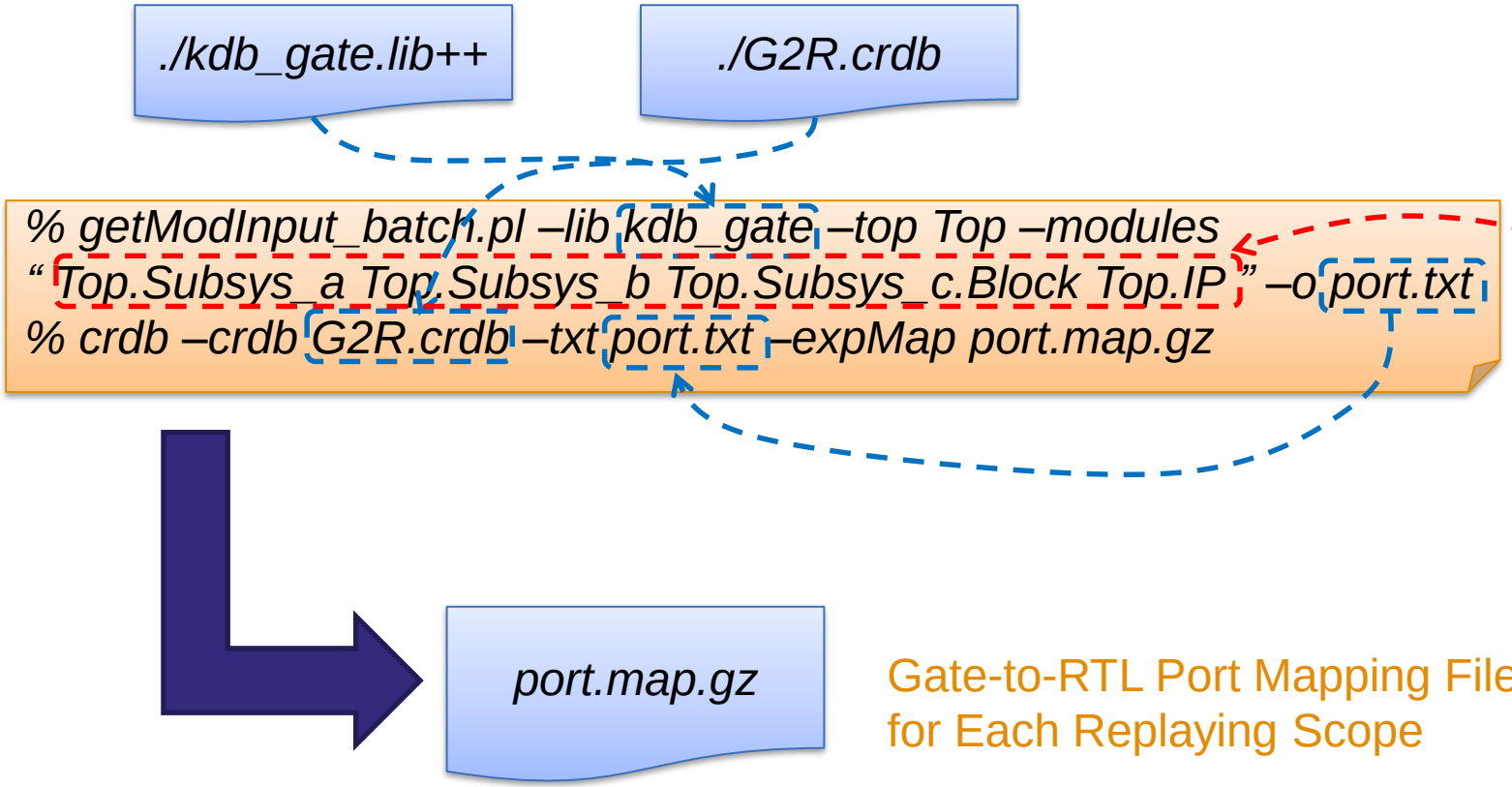
./G2R.crdb

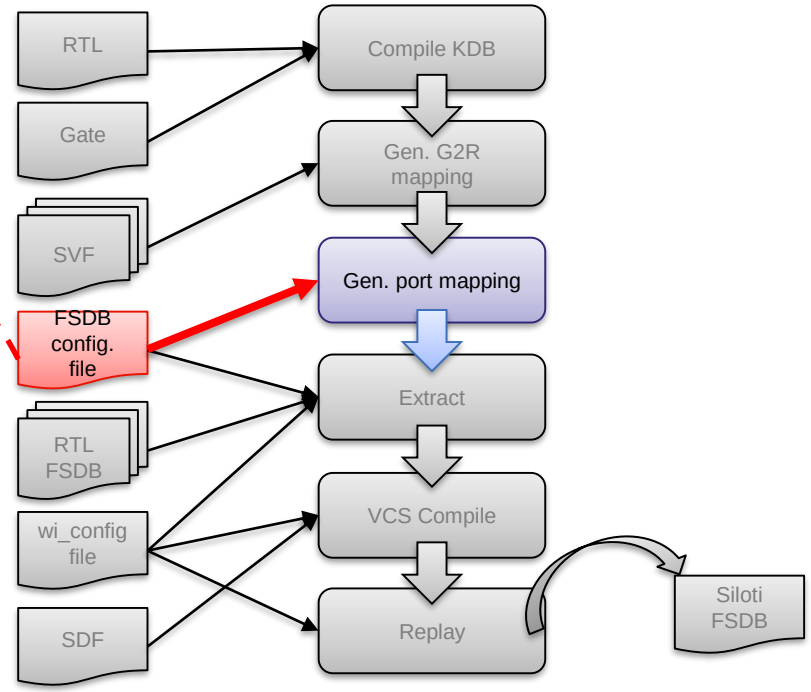
Mapping Data Base

G2R.list.gz

Gate-to-RTL Reg. Mapping File

Step 3: Gen. Port Mapping





Gate-to-RTL Port Mapping File
for Each Replaying Scope

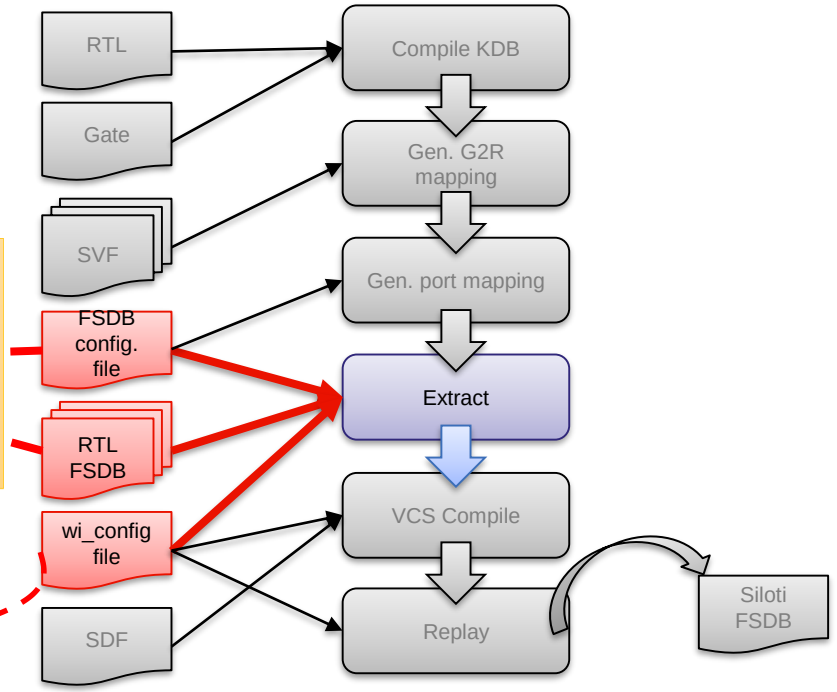
Step 4: Extract

```
set FSDB_list                    = fsdb_list
set Scope                        = Top
set Map                          = G2R.list.gz
set Map                          = port.map.gz
set simulation_compile_script    = wi_compile.rc
set simulation_run_script        = wi_run.rc
set Begin_time                   = 0
set End_time                     = 600000
```

```
rtl_a.fsdb –begin_time 300ns –end_time 900ns –from_scope tb.Top.Subsys_a –to_scope Top.Subsys_a
rtl_b.fsdb –begin_time 1200000ps –end_time 1800000ps –from_scope tb.Top.Subsys_b –to_scope Top.Subsys_b
rtl_blk.fsdb –begin_time 5600ns –end_time 6200ns –from_scope tb.Top.Subsys_c.Block –to_scope Top.Subsys_c.Block
rtl_ip.fsdb –begin_time 1770800ns –end_time 1771400ns –from_scope tb.Top.IP –to_scope Top.IP
```

./kdb_gate.lib++

```
% wisim –lib kdb_gate –top Top –target whatIf_Top –config wi_config –replay_extract
```



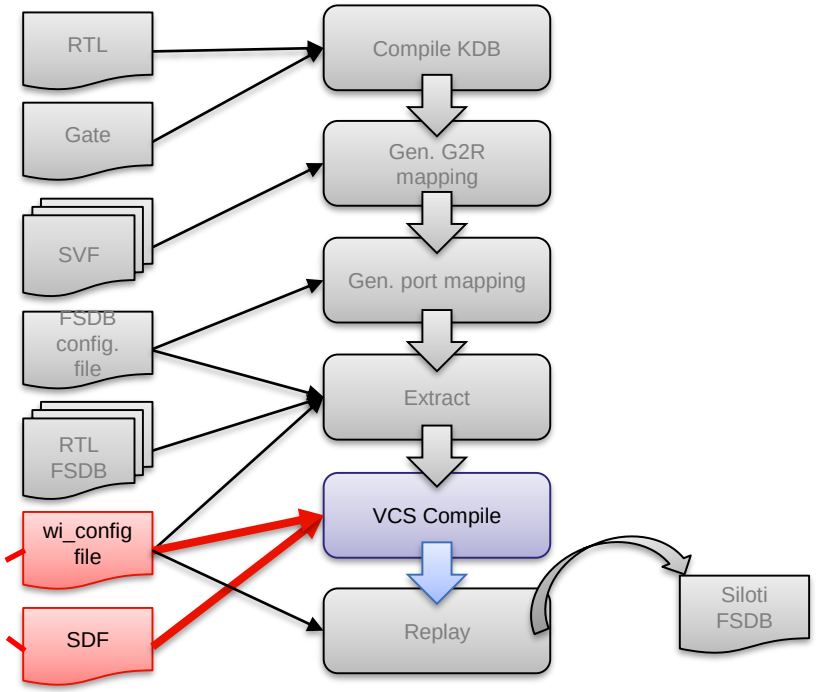
- wi_test.sv — Siloti TB
- wi_design.v — Instrumented Design
- wi_manip.fsdb — Merged RTL FSDB

Step 5: VCS Compile

```
set FSDB_list                  = fsdb_list
set Scope                      = Top
set Map                        = G2R.list.gz
set Map                        = port.map.gz
set simulation_compile_script  = wi_compile.rc
set simulation_run_script      = wi_run.rc
set Begin_time                 = 0
set End_time                   = 600000
set Time_Unit                  = ps
set Delay                      = delay_wrap
set SDF                        = "Top.sdf.gz" "Top" "" "" "MAXIMUM"
set ExcludeModule              = vc_exclude_mod.list
```

./kdb_gate.lib++

% wisim –lib kdb_gate –top Top –target whatIf_Top –config wi_config –replay_compile



./csrc

./simv.daidir

simv

VCS Data Base

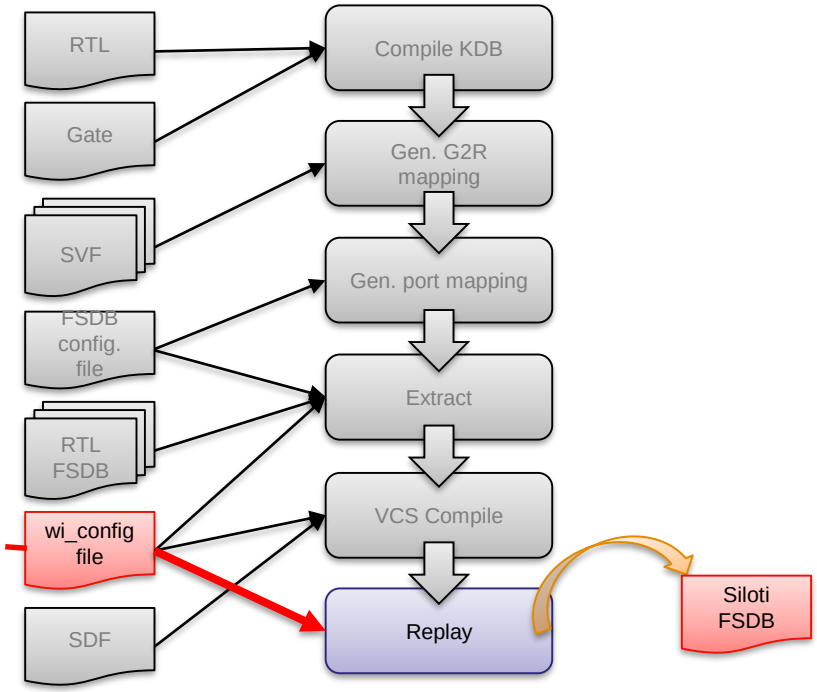
VCS Sim. Execution File

Step 6: Replay

./kdb_gate.lib++

% wisim –lib kdb_gate –top Top –target whatIf_Top –config wi_config –replay_sim

Siloti FSDB



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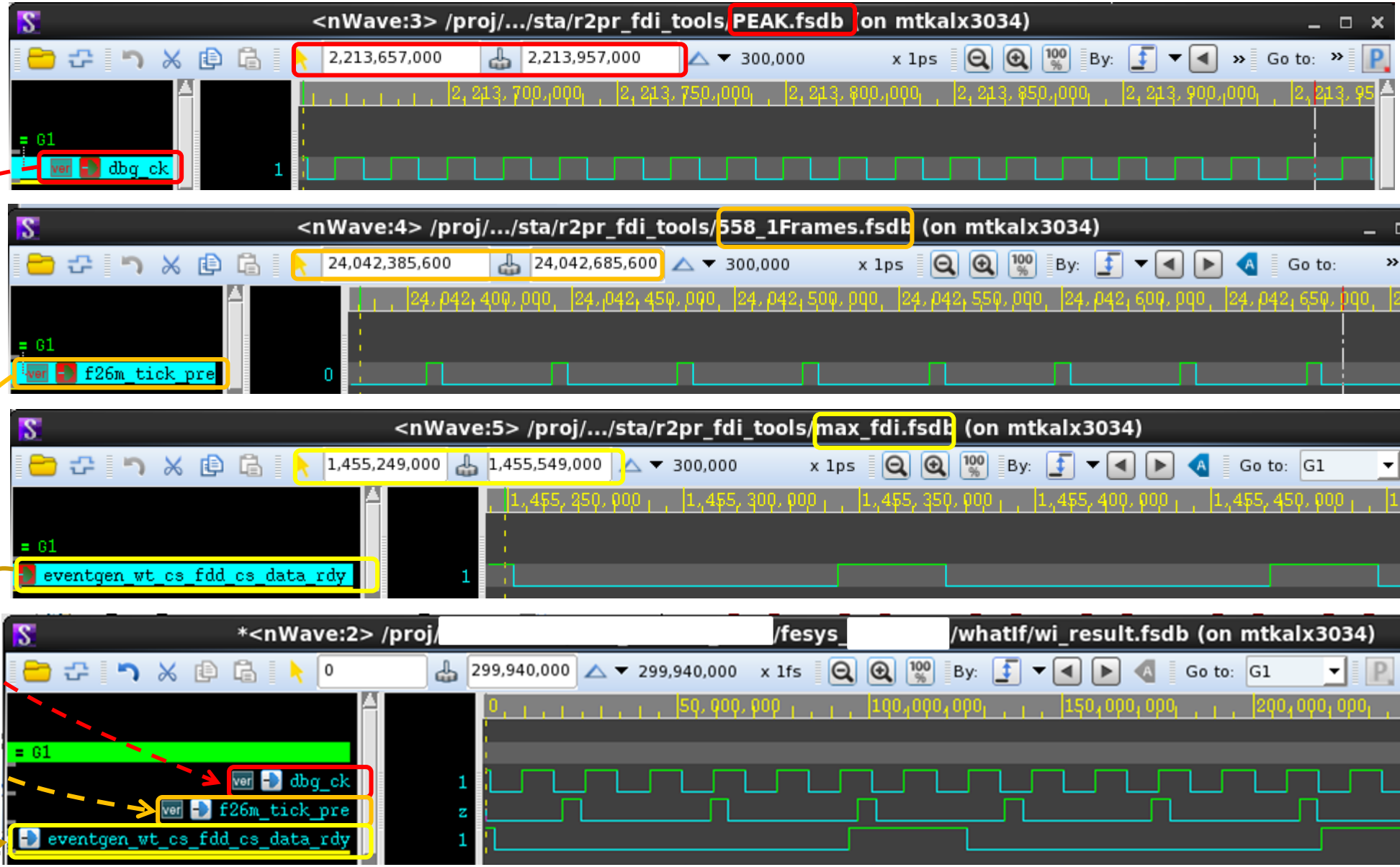
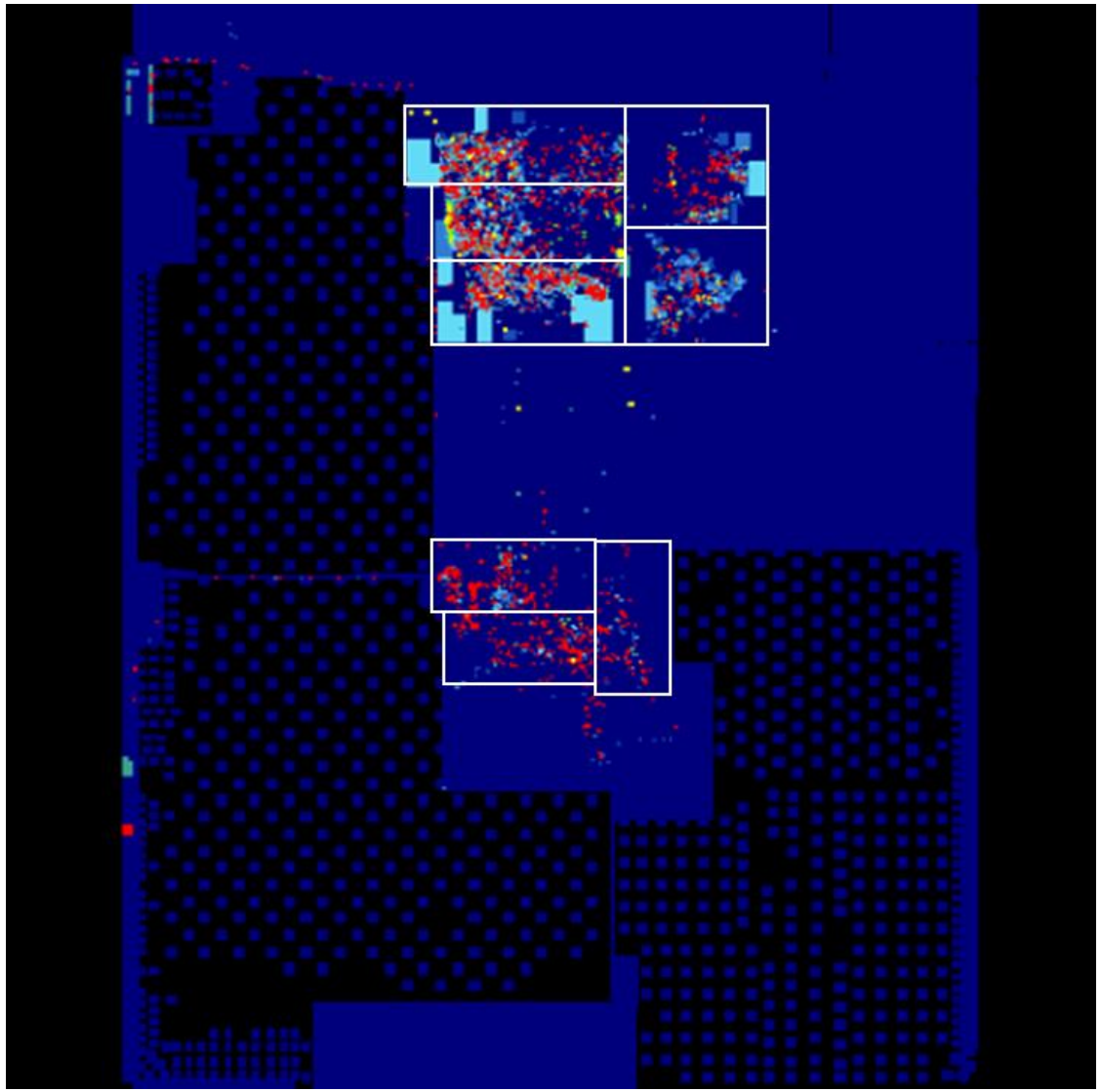

<nWave:3> /proj/.../sta/r2pr_fdi_tools/PEAK.fsdb (on mtkalx3034)
2,213,657,000
2,213,957,000
300,000
x 1ps
By:
Go to:
2,213,700,000
2,213,750,000
2,213,800,000
2,213,850,000
2,213,900,000
G1
dbg_ck
1
<nWave:4> /proj/.../sta/r2pr_fdi_tools/558_1Frames.fsdb (on mtkalx3034)
24,042,385,600
24,042,685,600
300,000
x 1ps
By:
Go to:
24,042,400,000
24,042,450,000
24,042,500,000
24,042,550,000
24,042,600,000
24,042,650,000
G1
f26m_tick_pre
0
<nWave:5> /proj/.../sta/r2pr_fdi_tools/max_fdi.fsdb (on mtkalx3034)
1,455,249,000
1,455,549,000
300,000
x 1ps
By:
Go to:
G1
1,455,250,000
1,455,300,000
1,455,350,000
1,455,400,000
1,455,450,000
1,455,500,000
G1
eventgen_wt_cs_fdd_cs_data_rdy
1
*<nWave:2> /proj/ /fesys_ /whatIf/wi_result.fsdb (on mtkalx3034)
0
299,940,000
299,940,000
x 1fs
By:
Go to:
G1
0
50,000,000
100,000,000
150,000,000
200,000,000
250,000,000
G1
dbg_ck
f26m_tick_pre
eventgen_wt_cs_fdd_cs_data_rdy
1
z
1

Results (Cont'd)

- Replay 8 RTL FSDBs for 8 different subsystems
- 40M instances
- Runtime 12+ hours



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- Novel waveform generation methodology is proposed for the power estimation, IR signoff, and power optimization
  - By enhancing Siloti for concurrently replaying multiple RTL waveforms to different gate design scopes
- SAIF solution is proposed for solving the signal conflict issues in merged FSDB
  - By averaging wires which have conflicts
- Results are also demonstrated in this paper for proving the effectiveness of the proposed methodology
- The future work contains:
  - Generate separate gate-to-RTL mapping rate report for each target replaying gate scope
  - Generate separate RTL FSDB mapping rate report for each target replaying gate scope
  - Develop solution for efficient debugging between RTL FSDBs and merged gate FSDB

MEDIATEK

snug
Synopsys Users Group
Taiwan

Thank You