The Challenges of Low Power Design: A System-on-Chip with 152 Power Domains

David Bean
Ericsson

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Agenda

Design Overview

Low Power Design & Implementation

Low Power Verification

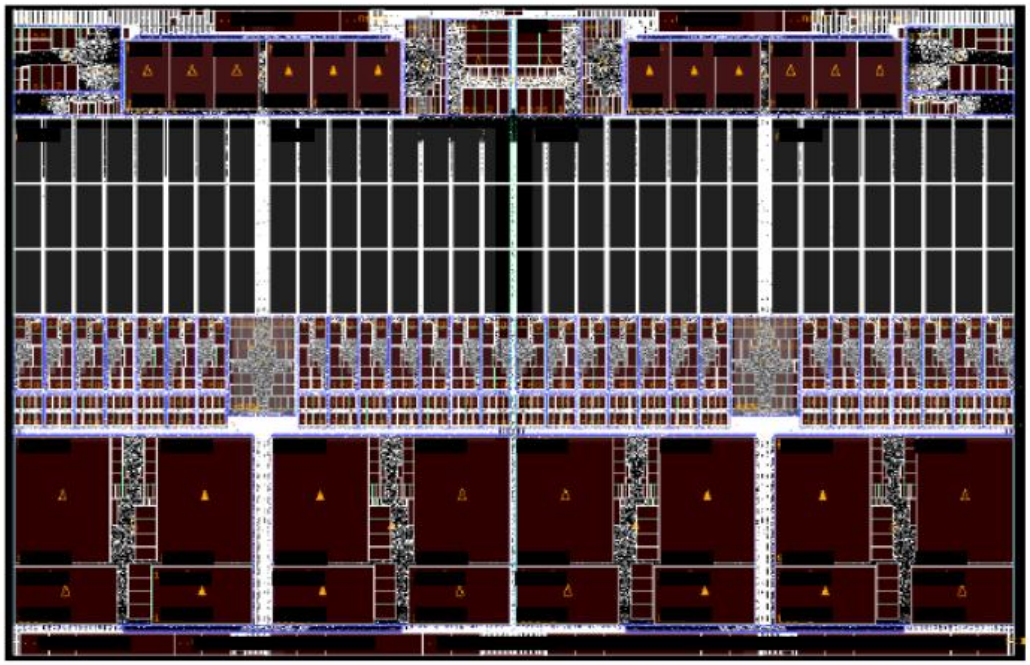
Conclusions

Q&A

Design Overview

The SoC and Why Low Power?

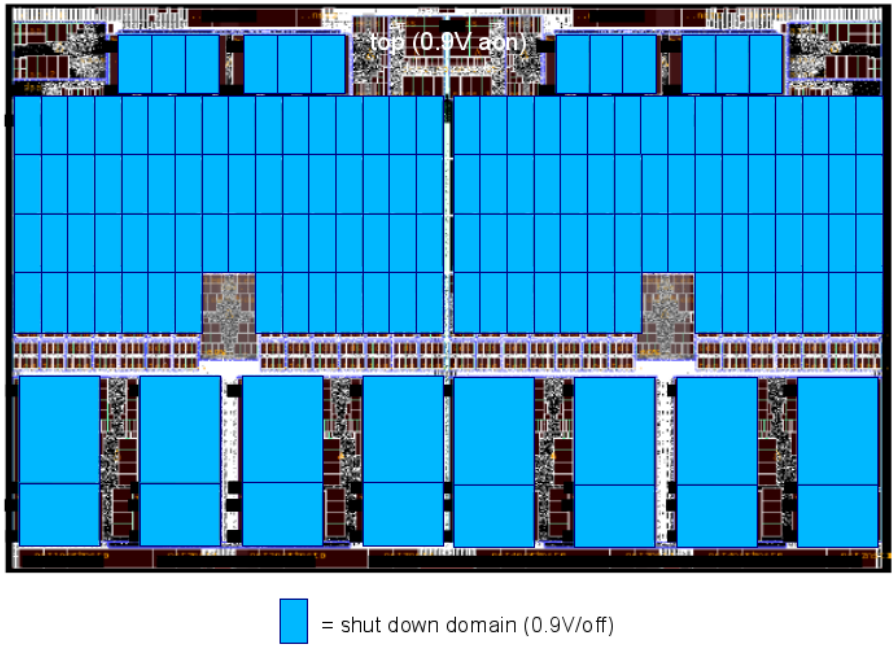
- Presentation describes SoC with 152 shut down domains
  - TSMC 28nm HPM
- Low power design critical for Ericsson
  - New applications require increasing computation
  - High leakage power of sub 90nm processes
  - Market pressure
- Low power flow
  - UPF
  - Synopsys low power verification tools



SoC layout plot

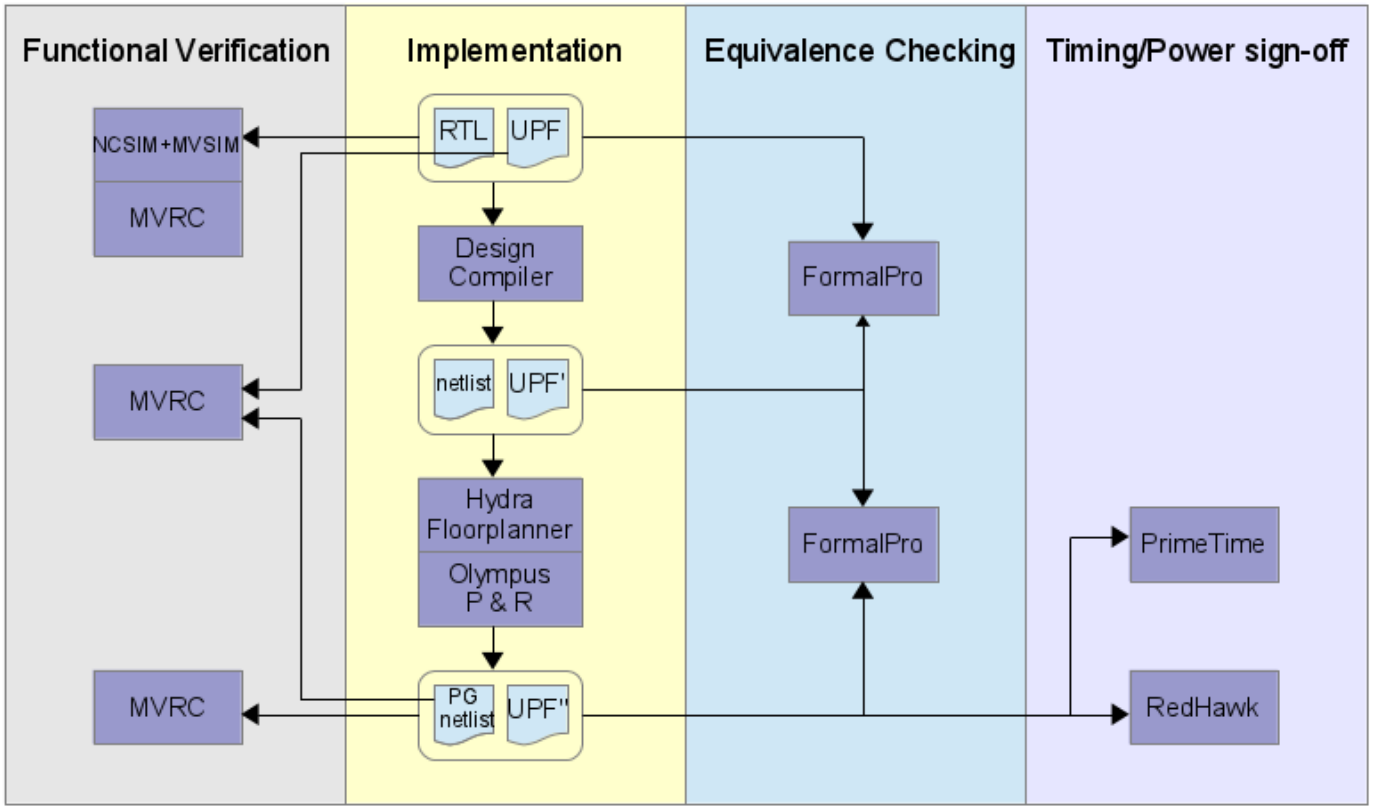
The Challenge of Low Power

- Overall Challenges
  - Pioneering the low power flow for our design group
  - The shut down domains are a large proportion of chip area
  - No previous experience with UPF or Synopsys low power verification tools
- Advanced low power design
  - Static multi supply design
    - Same voltage level for all design
  - 152 partitions can be shut down
  - RAM macros with shut down and deep sleep modes



SoC layout showing shut down domains

Low Power Tool Flow



- We used a mixed vendor tool flow
  - Can choose best-in-class for each flow step
  - But can give compatibility issues when sharing files
  - Responsibility for support can get blurred.

Low Power Design & Implementation

Low Power Design Coding

- RTL (Verilog)
  - Designed with UPF in mind
    - Power domains correspond to single modules
    - Wrappers around power domains for placing AON logic and isolation cells (`-location parent`)
    - Include power control nets and power management
  - Regular design reviews to keep team informed of low power issues
- UPF
  - Defines power domains
  - Defines power modes using power state table (PST)
  - Adds multi voltage cells
    - Power switches, isolation gates, level shifters
  - Must be supported by all tools in the flow

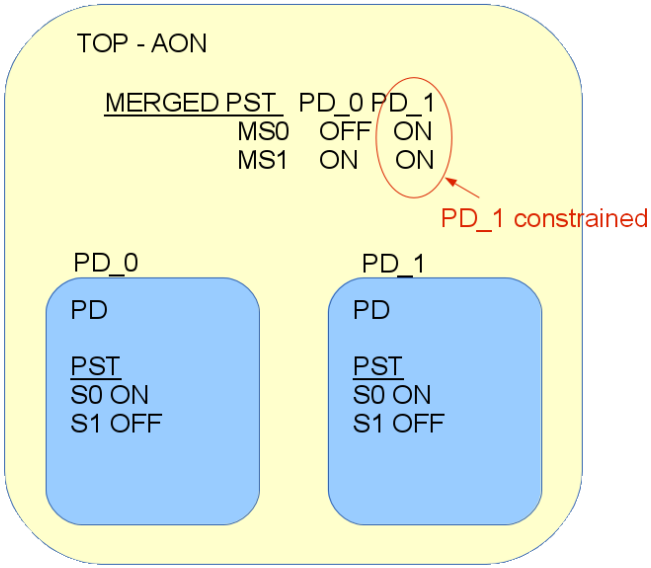
UPF Design Choices

- Power intent specification
  - Controlled document defining power intent
- UPF 1.0
  - To keep UPF methodology simple
  - Not confident that all tools/vendors would support UPF 2.0
- Hierarchical UPF
  - Modular design
  - 152 power domains but only 5 power domain modules
  - Which RTL modules require a UPF?
    - Each power domain or power domain wrapper
    - Each block in the physical hierarchy (P&R block)
    - Top level

Implementation Challenges

Power State Table (PST) reduction

- Impossible to verify 2^{152} power states!
- The architecture has some limitations which reduce this – but not many
- Used design modularity & hierarchy in UPF to reduce PST
  - Only expand power states once for duplicated modules by constraining expansion to high levels.



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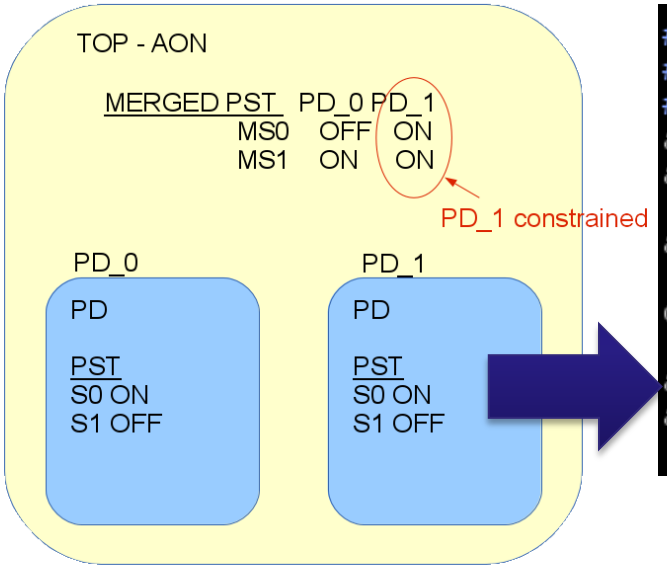


```
##################################################################
## PD Power State Table
##################################################################
add_port_state VDD  -state {ON 0.81}
add_port_state VSS  -state {GND 0.0}

add_port_state PSW/vout -state {ON 0.81} -state {OFF off}

create_pst TOP_pst -supplies {PSW/vout VDD VSS}

add_pst_state s0 -pst PD_pst -state {OFF ON GND}
add_pst_state s1 -pst PD_pst -state {ON  ON GND}
```

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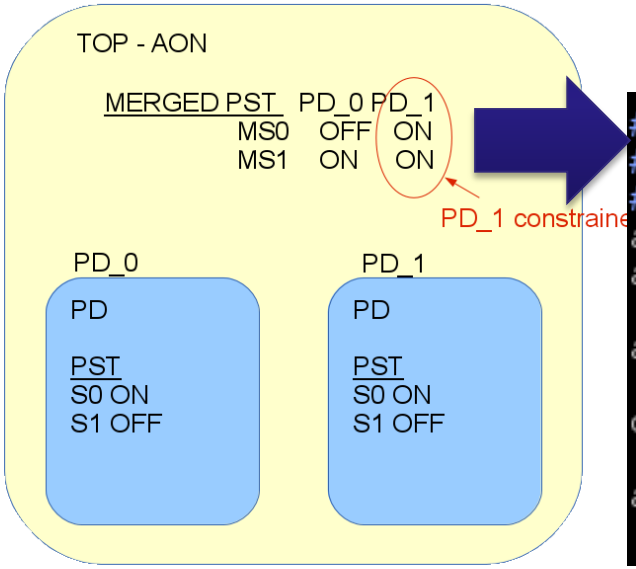
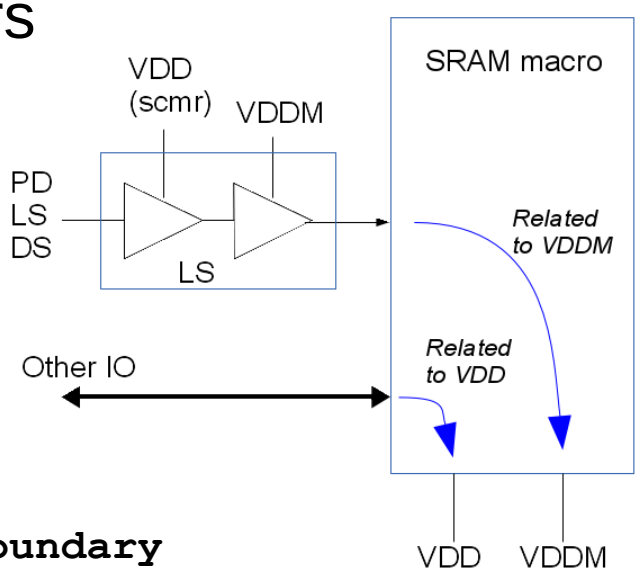



```
##################################################################
## PD Power State Table
##################################################################
##################################################################
## TOP Power State Table
##################################################################
add_port_state VDD -state {ON 0.81}
add_port_state VSS -state {GND 0.0}

add_port_state PD_1/PSW/vout -state {ON 0.81} -state {OFF off}

create_pst TOP_pst -supplies {PD_1/PSW/vout VDD VSS}

add_pst_state s0 -pst TOP_pst -state {ON ON GND}
```

Implementation Challenges

Handling RAM macros: Ensuring level shifters were placed correctly

- The RAM macros power control pins were driven by RAM core supply so needed level shifters

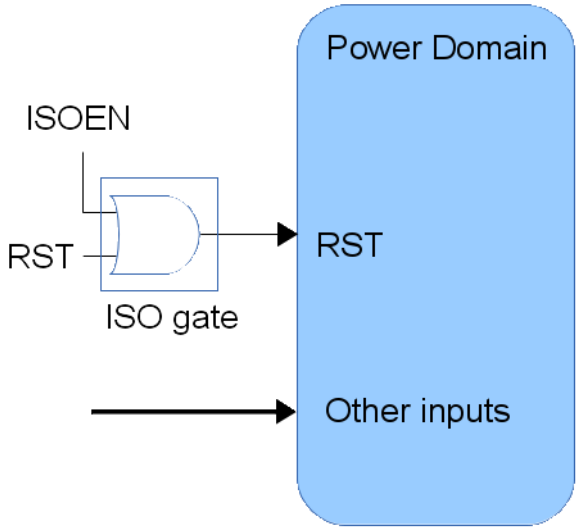


1. In UPF use **`connect_supply_net`** to specify connections for all these pins
2. In DC use **`mv_allow_ls_on_leaf_pin_boundary`**
3. Check the multi voltage library has required LS – attribute on VDD pin called “scmr” (std_cell_main_rail) so it can be placed in an AON area.

Implementation Challenges

Shut down domain reset policy

- Clamp resets to power domains active when isolated
  - Ensures all power domains have reset applied on power up and are initialised to a known state.
  - No retention registers in the power domains
  - Gives “ISO_DEVICE_REDUNDANT” warnings in MVRC which were waived.



Implementation Challenges

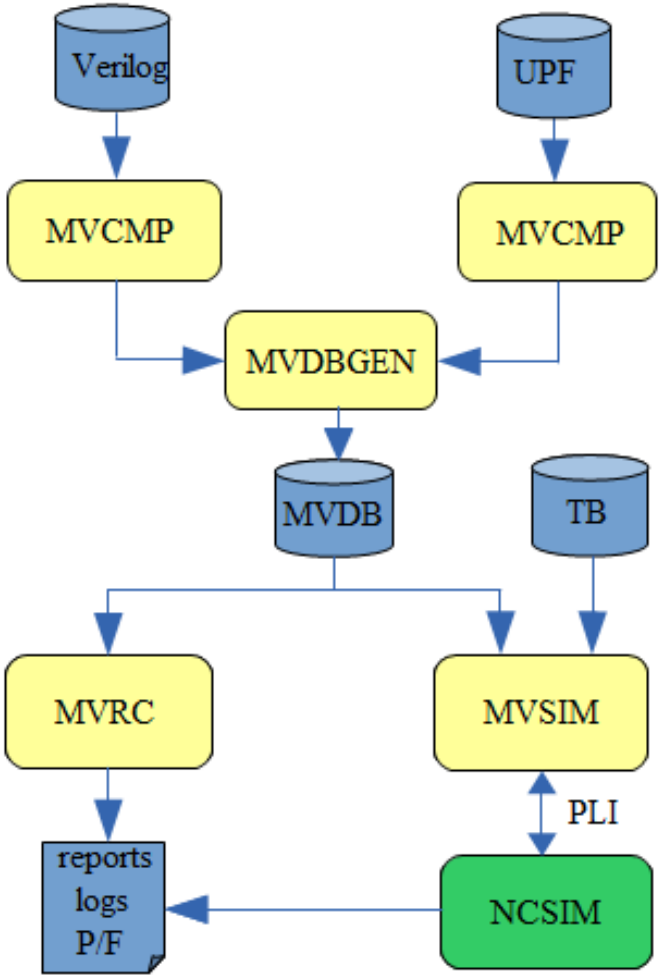
UPF changes required for back end tools

- Floorplanning tool required:
  - `load_upf` sub-block calls before defining supply nets
  - `create_supply_port` and `create_supply_net` can go before `load_upf` but any commands which refer to ports/nets from sub-blocks must go after
- Place & route tool required:
  - All IO supplies to be present in UPF top level
    - Ensure supplies in UPF match up with the physical IO groupings. Some voltage regions were physically split and this required duplicating supplies in the UPF
  - PST in every UPF file
    - Including UPFs for P&R blocks with no shut down domains

Low Power Verification

Low Power Verification Tool Flow

- Synopsys low power verification tools
  - MVCMP, MVDBGEN, MVSIM & MVRC
- Dynamic simulation
  - MVSIM + NCSIM using PLI
- Static rule checking
  - MVRC



Dynamic Simulation using MVSIM

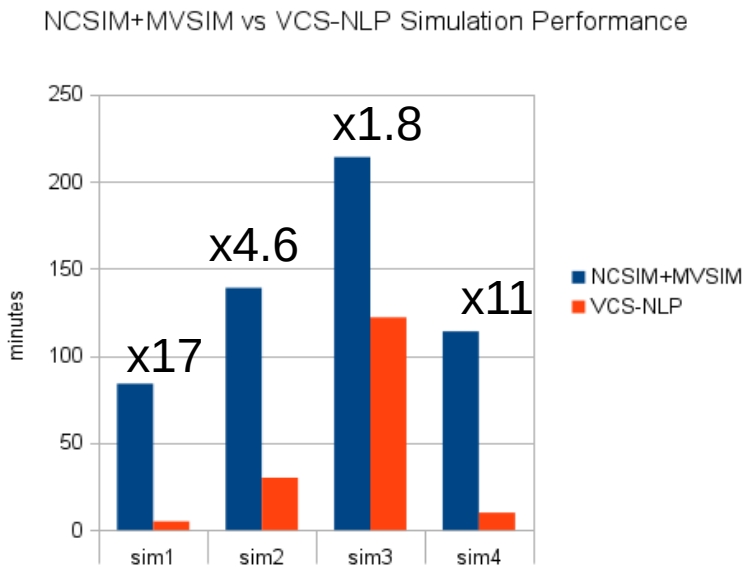
- Using RTL + UPF (golden)
- Test suite built to verify the following
  - Power Control
    - Power on/off sequences for each power domain
    - Power domains function correctly after power cycled
  - Power Intent
    - Blocks that share interfaces with a shut down domain
- Power states reduced by verifying all interfaces to shut down domains. Don't need to verify all 2^{152} power modes!

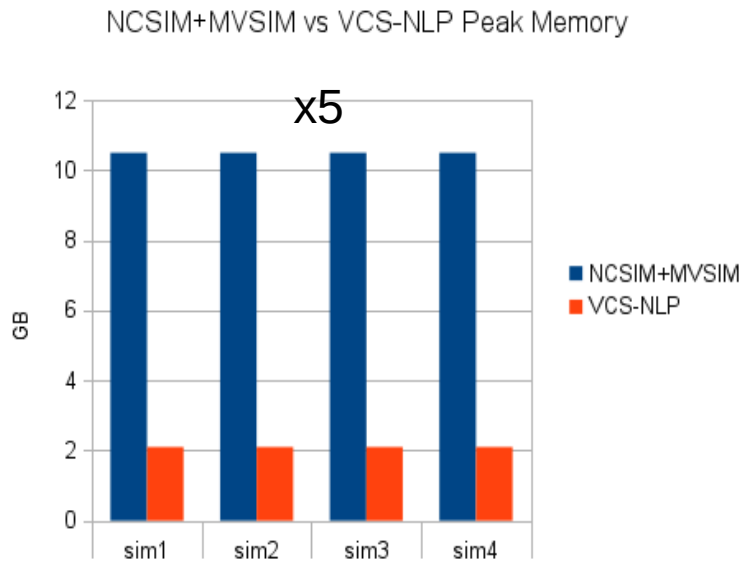
MVSIM Challenges

- Single MVSIM license
  - Could only run simulations sequentially
  - Test suite took 4 days to run!
  - We run standard sims on a multiprocessor grid but could not use this.
  - Require this for future project which would need low power capability with standard license.
- Coverage
  - Test suite covers all 152 power domains
  - But MVSIM coverage had limited capability (improved in VCS-NLP)
  - Assertions written to check power off/on sequence rules

Evaluation of VCS-NLP

- VCS-NLP vI_2014.03
  - Carried out after tape out on full low power test suite
  - No PLI overhead
  - Improved speed, capacity & coverage





Static Rule Checking using MVRC

- Vectorless detection of connectivity & architecture errors
  - Missing, illegal or redundant isolation/level shifters (uses PST)
  - Supply & power control connectivity
  - Clock, reset, enables & power control architectural checks
- Ran at multiple stages in flow (sign off underlined)
  - Final RTL + UPF (golden)
  - Gate level netlist + UPF' (UPF written by synthesis tool)
  - Power and ground (PG) netlist + UPF (golden)
  - PG netlist + UPF'' (UPF written by P&R tool)
- PG netlist checked continuously during back-end flow

MVRC Challenges

Mixed vendor flow

- Third party tool used for Place & Route
  - UPF" was not compatible with Synopsys tools
    - Some UPF commands interpreted differently
    - No **`connect_supply_net`** for multi voltage cells
  - MVRC sign off run with PG netlist + UPF (golden)
    - Using **`mvdbgen -verilog_pg_connections`** to extract supply connections from the netlist

MVRC Challenges

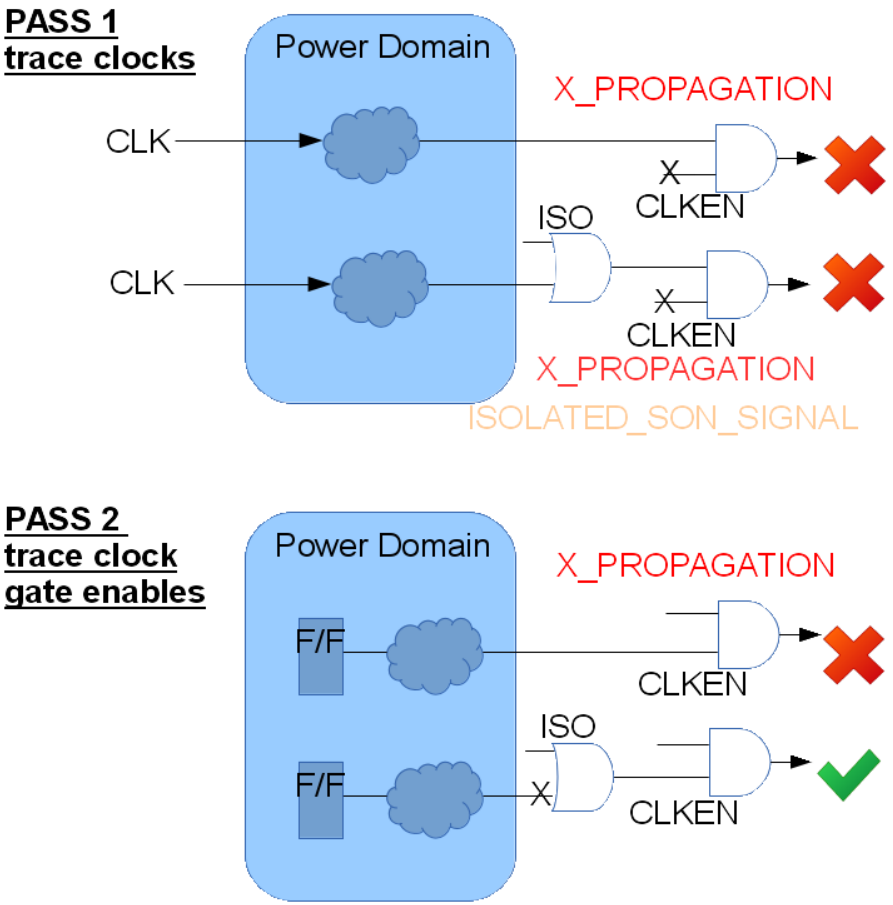
Architecture Checks

- Traces “special” signals (clocks, resets, iso/psw/scan enables) and checks for corruption
  - Use **`create_clock`** and **`create_reset`** to specify signals
  - Also use **`infer_sources`** to automatically infer special net sources
- Problem occurred when tracing back through clock gate enables (solution on next slide)
  - Thousands of X_PROPAGATION errors flagged for clock gate enable sources in shut down domains
    - These were protected by isolation gates so were okay but needed a method to clear these to ensure no real errors

MVRC Challenges

Architecture Checks

- Run checks twice
  - 1. Without tracing through clock gate enables and with `halt_at_isolation_data false` Flags errors relating to clock sources
  - 2. With tracing through clock gate enables and with `halt_at_isolation_data true` Flags errors on clock gate enables.



MVRC Challenges

Well Bias Checks

- In this design all nwell ties must be connected to the always on supply, VDD. For the power domains this requires a different tie cell so wanted to check that the correct cells were placed.

  – To check that all pg_pin's of type nwell are connected to VDD

    ```
    set_back_bias -domain <domainName> -type nwell -net VDD
    ```

  – To check that all pg_pin's of type pwell are connected to VSS

    ```
    set_back_bias -domain <domainName> -type pwell -net VSS
    ```

MVRC Challenges

Using Isolation gates as logic gates

- In some power domains power switch acknowledge signals were combined inside the domain. A 2-input AON gate did not exist in the multi-voltage library
  - Used an isolation gate to combine the signals
  - Used `set_var_ignore_logic_iso_cells` to identify these cells
  - Architecture checks still flagged “X_PROPAGATION” errors and “ISOLATED_AON_SIGNAL” warnings
  - These had to be manually checked and waived

MVRC Challenges

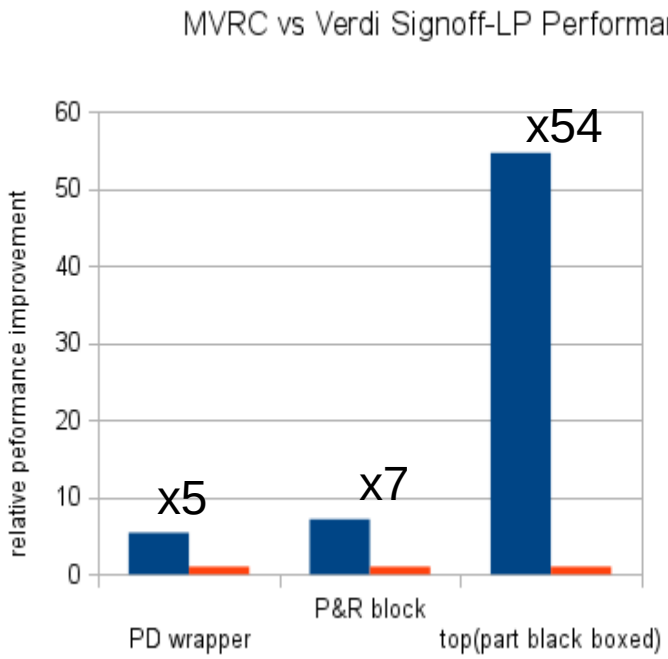
Capacity Issues

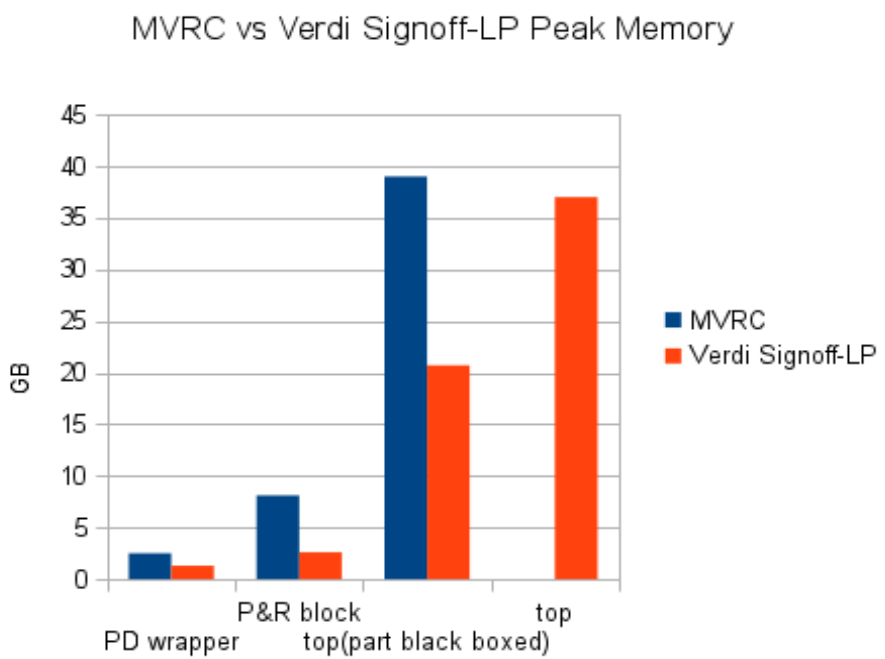
- MVRC did not have the capacity to run the top level PG netlist
- Solution was to run in two passes with different modules black boxed (in top level) for each run
- Compromised checks
- Only acceptable because there were no multi-voltage cells at the top level

Verdi Signoff-LP Evaluation

Results

- Synopsys Verdi Signoff-LP vH-2013.06
  - Ran all PG netlist blocks after tape out
  - Ran top level PG netlist in three hours using 37 GB of RAM!





Bugs Caught by MVRC

- Wrong supply connection to RAM Macros
- Wrong supply connection to LS
- Missing ISO cells
- Buffers placed between LS and RAM macro
- Redundant AON buffers in power domain
- Redundant LS before DDR phy pins

Conclusions

Lessons Learnt

- Write a power intent spec before starting coding
- Write RTL with consideration for low power flow
  - build wrappers around power domains
  - take care when adding power control blocks
- Build knowledge by attending Synopsys low power training courses & workshops
- Hold regular peer reviews
  - Keep design team involved in UPF flow
- Don’t hesitate to contact Synopsys support when problems arise
- Pipe clean flow to layout netlist ASAP to highlight issues

Recommendations for our next project

- Use a simulator with native low power capability
- Migrate from MVRC to Verdi Signoff-LP for static rule checking
  - improved capacity, performance & coverage tools
- If possible integrate low power into more simulation test benches
  - should not be a special case
  - Note that this requires a new licensing model

Thank You

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Presenter's Name
Spell Out Company Name

Month Day, Year (XXXX)
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Slide Title

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Transition Slide

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Two Column Layout

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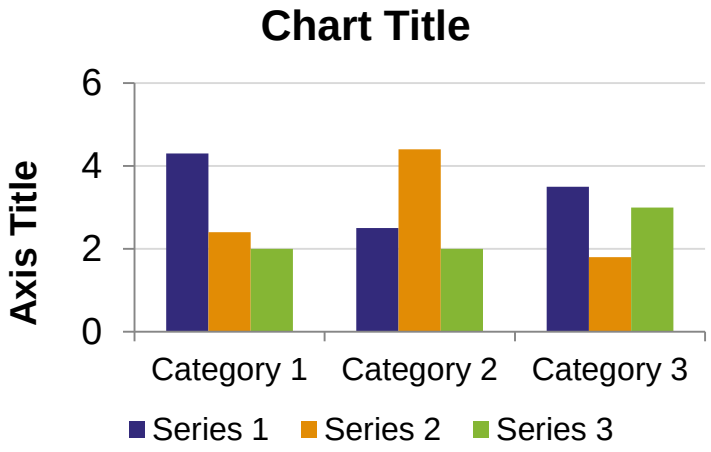

Two Column Layout

Column Title

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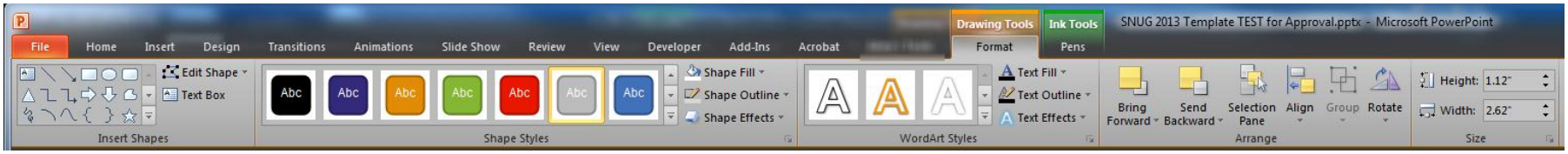
Shape Coloring and Format



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Title Slide

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