AMBA Interconnect Design Flow Automation

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September 24th, 2015
Boston, MA

AMBA Interconnect Design Flow

We found ourselves…

- Spending a great deal of time on things other than design or optimization related tasks
- Frustrated with tediousness in the flow
- Unable to leverage performance models as much as we'd like
- Creating an automated solution to help alleviate these problems

Agenda

AMBA Interconnect Design Challenges

Automation Goals

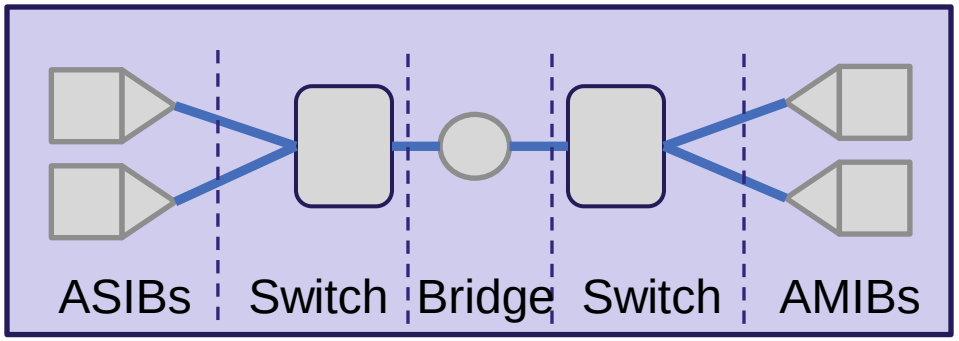
AMBA Designer Automation Flow

Performance Analysis and Model Integration

Conclusion

AMBA Interconnect Design Challenges

AMBA Designer Configuration



Per Node

- Time closure
  - 10 fields
- Buffer depths
  - Per channel
- Run-time Configuration
  - AQoS features: latency, rate, trans.
  - ASIB only
    - read_qos priority value
    - write_qos priority value
    - fd_bit – max-o limit

Per Connection

- Max Outstanding
  - Read
  - Write
  - Total

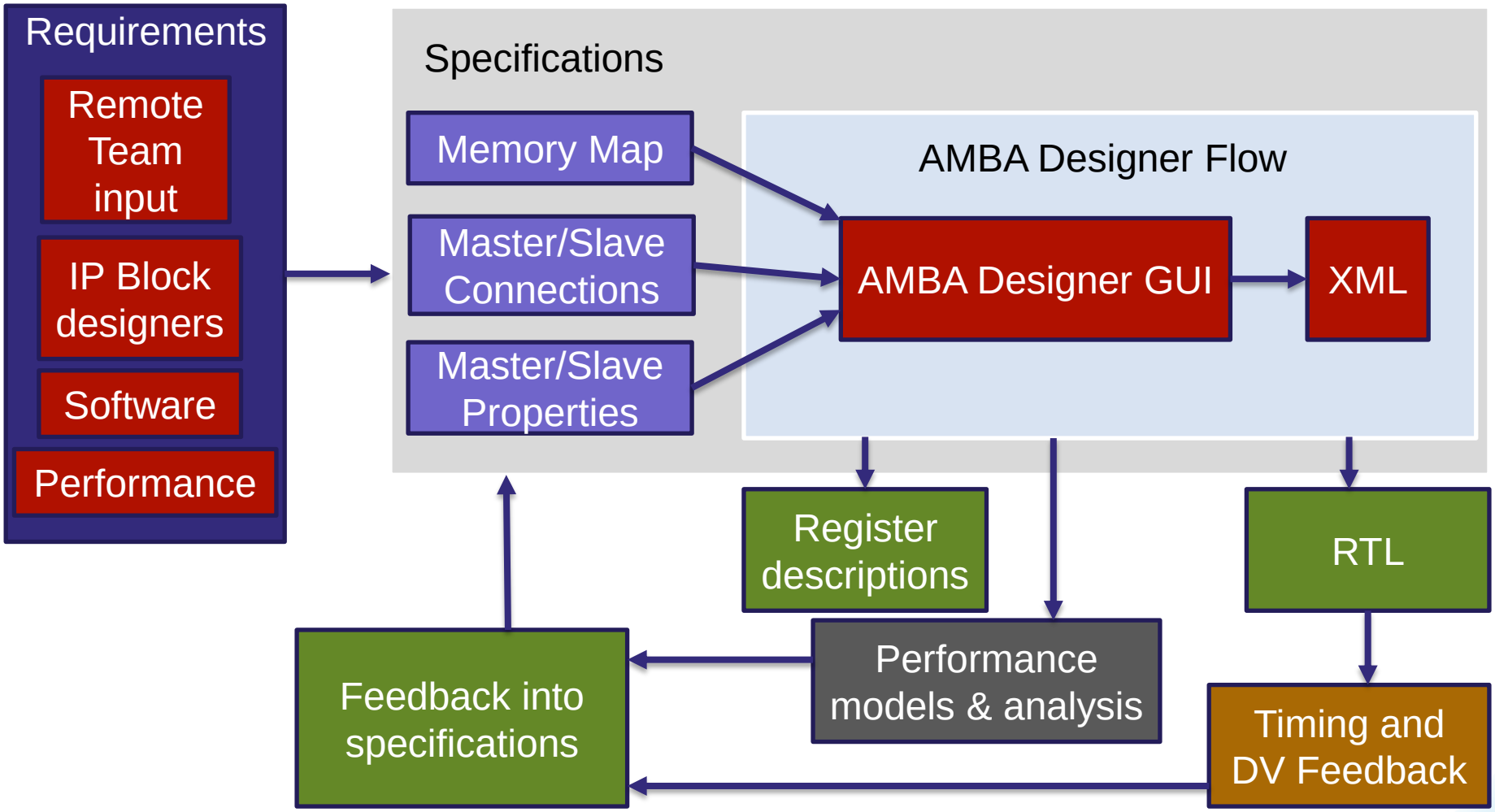
Overall Layout

- Per-switch mux
- Clock domain crossings
- Datawidth conversions

- Many combinations
- All parameters are interdependent
  - Can't be evaluated individually

AMBA SoC Design Flow

Has many moving parts



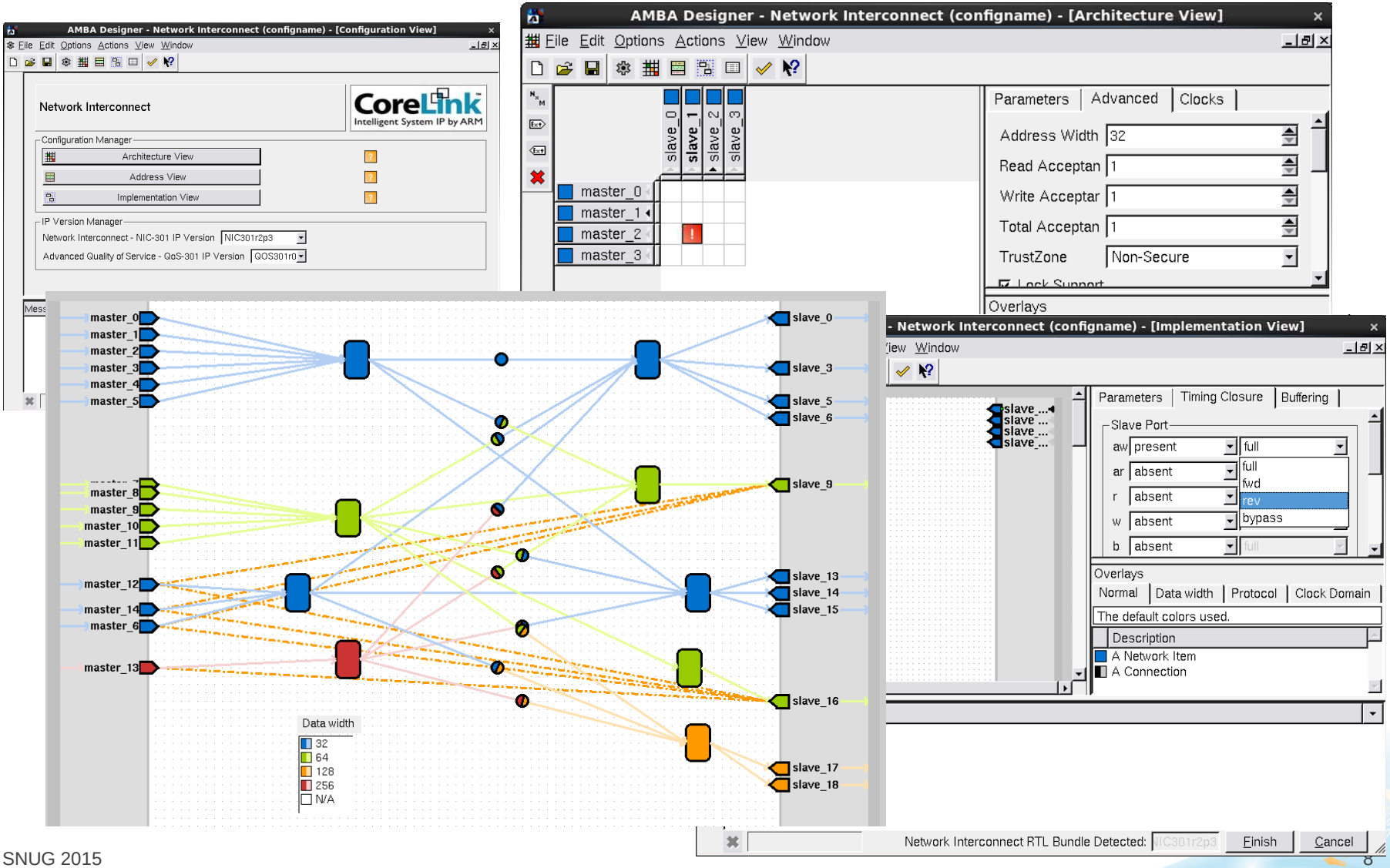
Maintaining coherency between all of these can be a full time job!

Problems with this workflow

- Lots of manual steps which are quite time consuming and tedious
  - Menus buried in the AMBA Designer GUI
  - Manual translation between specs and AMBA Designer
  - Manual translation to other formats
- These steps must be repeated over and over during a design
- Potential for human error, with costs extending to debug and DV
- We can do better!

AMBA Designer

Screenshot of Configurator GUI



Automation Goals

Our Goals

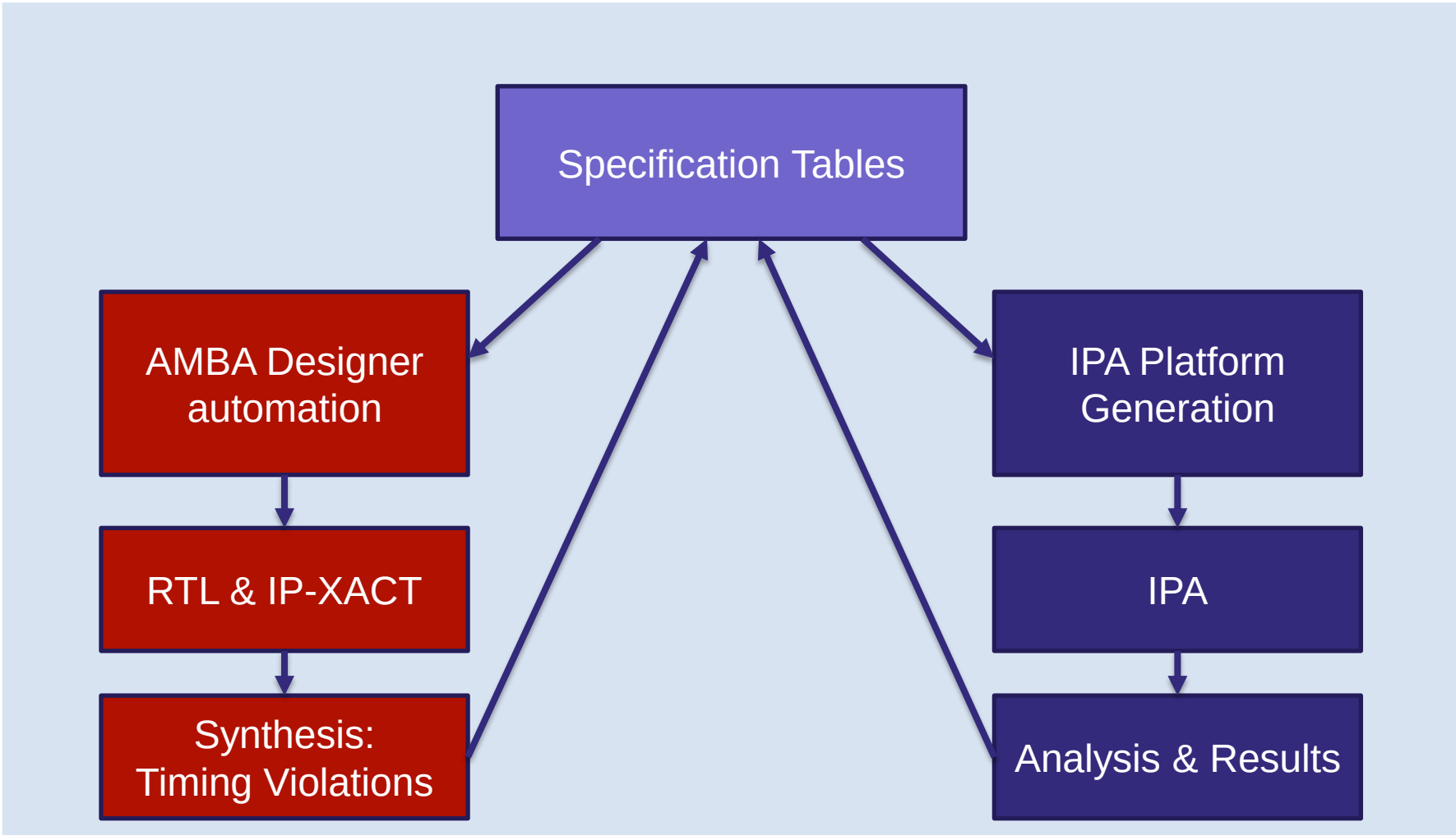
Saving time and money

- Saving time by avoiding lots of manual steps (resourcing)
- Reducing human error from manual efforts
  - Because human error costs time and resources for debug and DV!!
- All of this saves

Goals

- Single-source specifications – a single source of truth
- Automating translation between formats
- Performance models must be part of the automated flow
- Detailed and accurate methods for performance analysis of the interconnect

Overall Automation Goal



AMBA Designer Automation Flow

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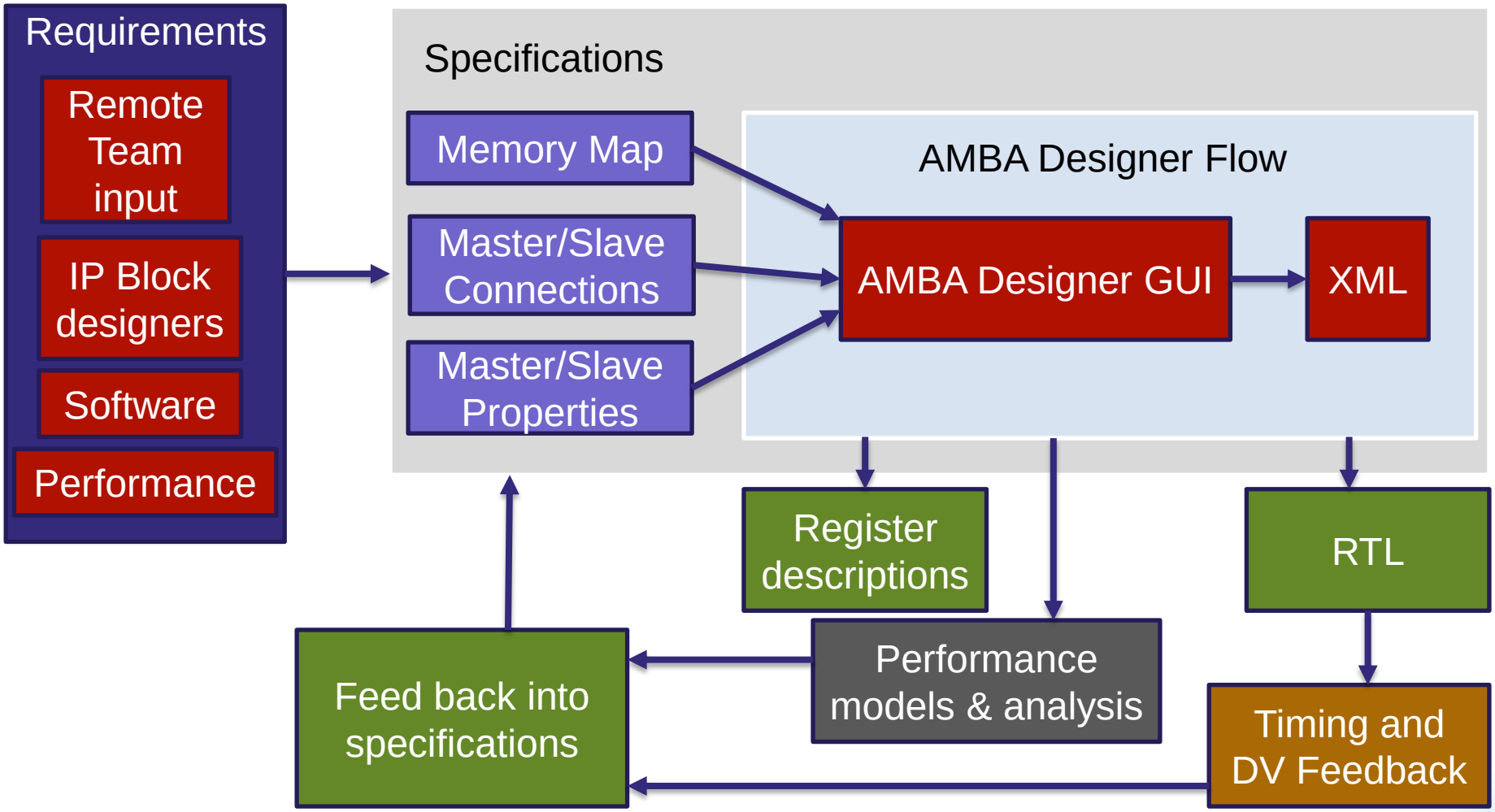
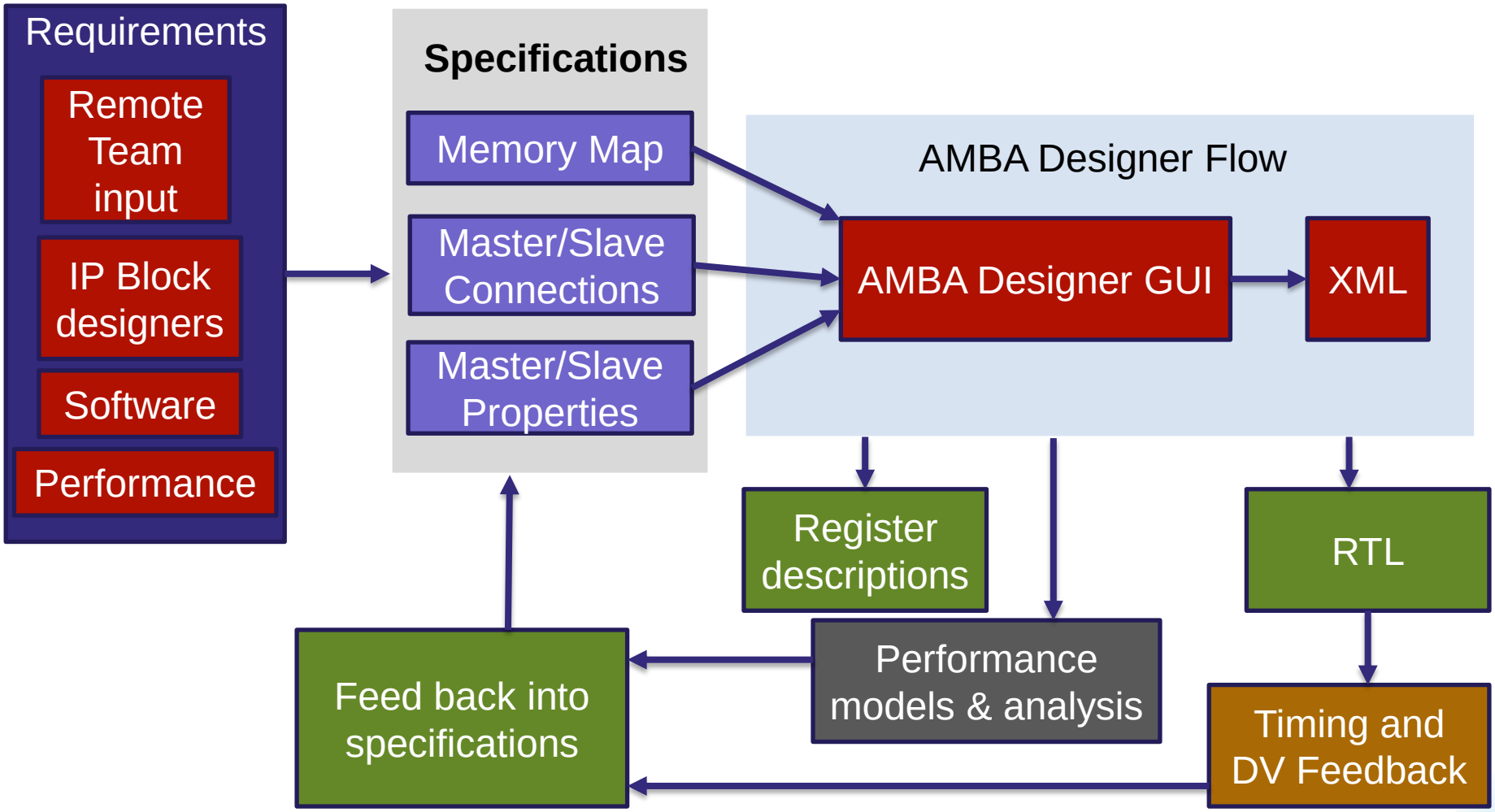
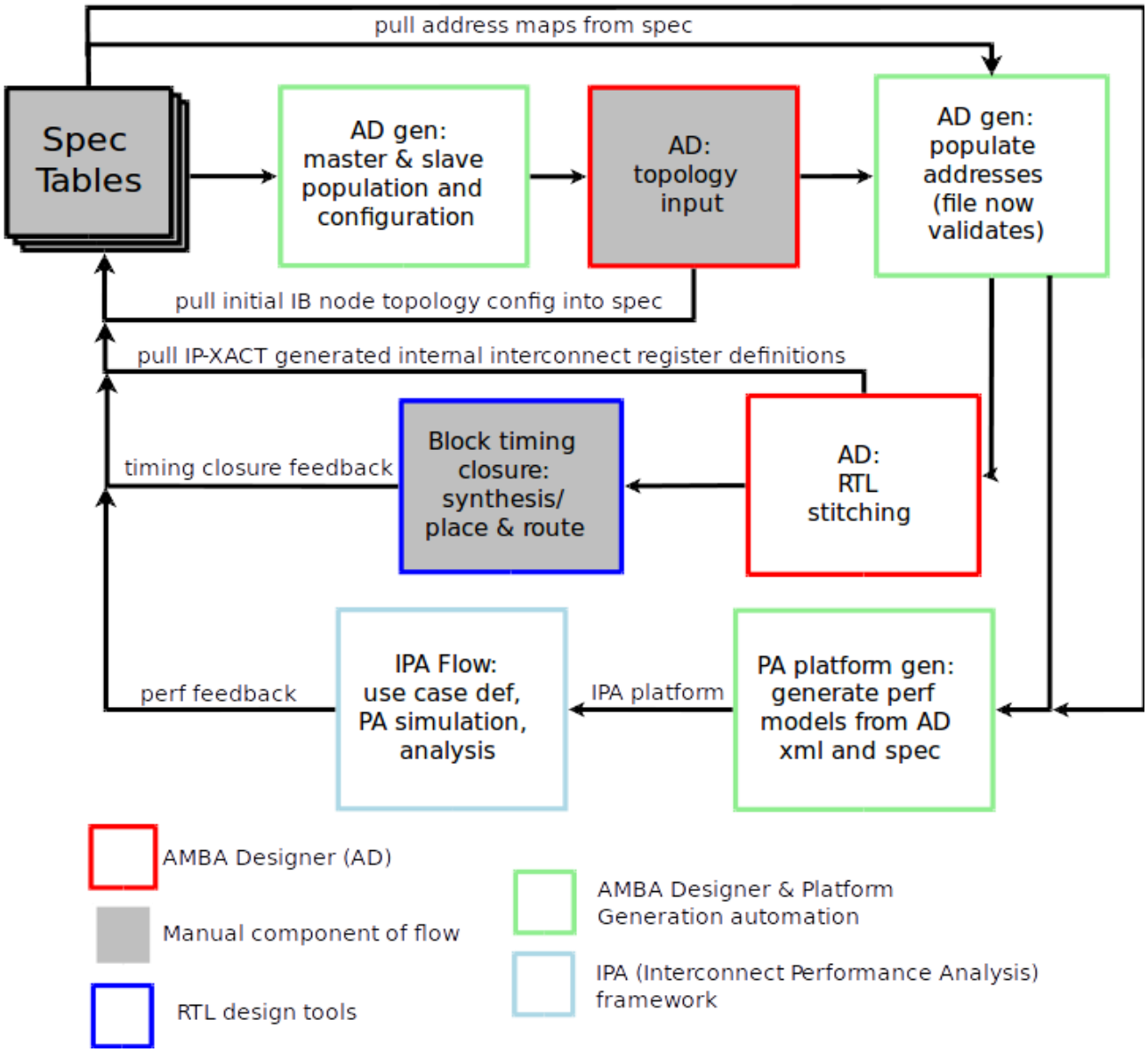
AMBA SoC Design Flow



AMBA SoC Design Flow



Automation Flow



Performance Analysis and Model Integration

Modeling interconnect performance; and how do we tie this to our automation?

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Different tools at different times

And varying levels of fidelity

- Pen and paper / spreadsheet analysis
- Performance models / simulation for dynamic interaction
- RTL simulation at block level
- RTL simulation at full chip level

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Synopsys' Platform Architect (PA)

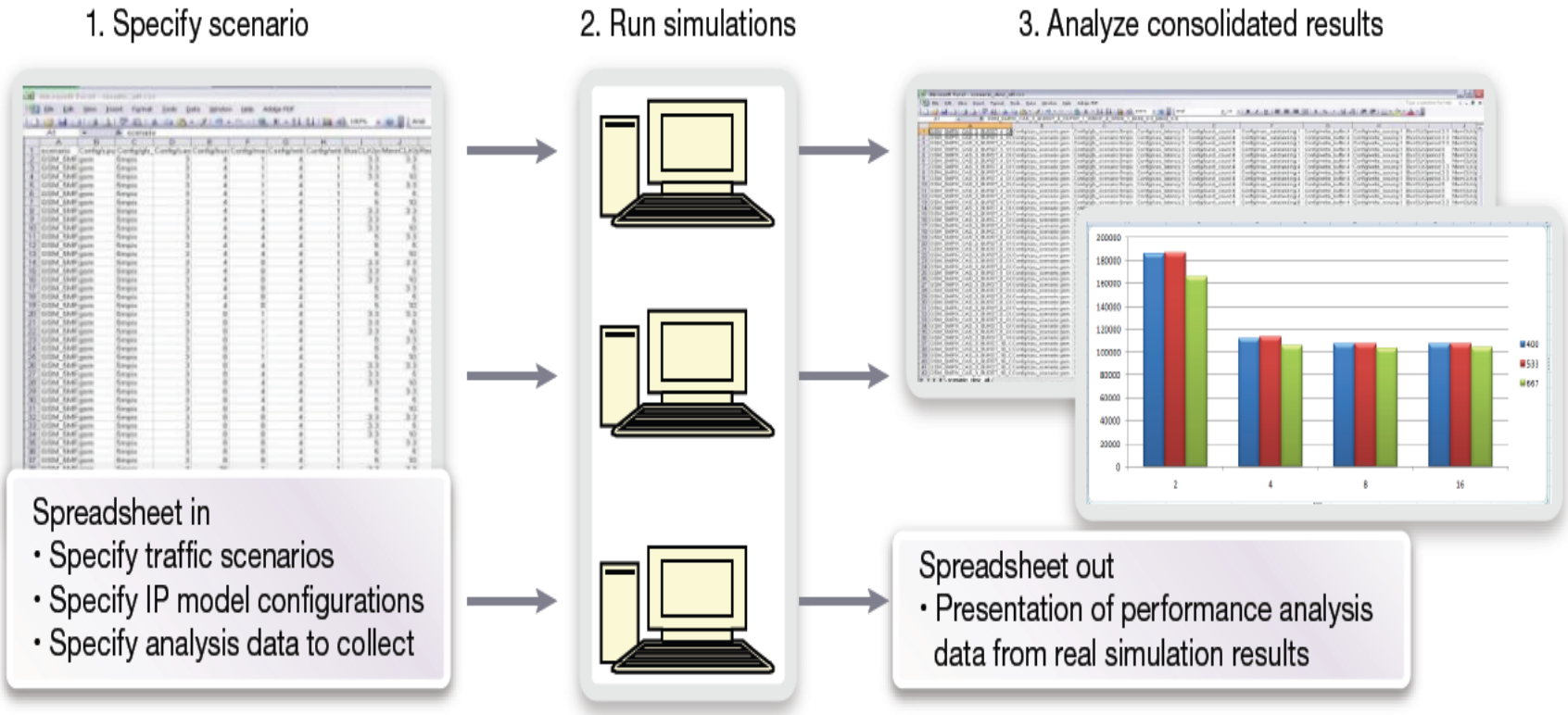
SystemC TLM 2.0 Environment (& much more)

For our needs, it provides:

- Cycle accurate AMBA bus models and monitors
  - NIC301 and NIC400 (& more)
- Supporting models for memories and initiators
- Ability to assemble representative SoC as a 'platform'

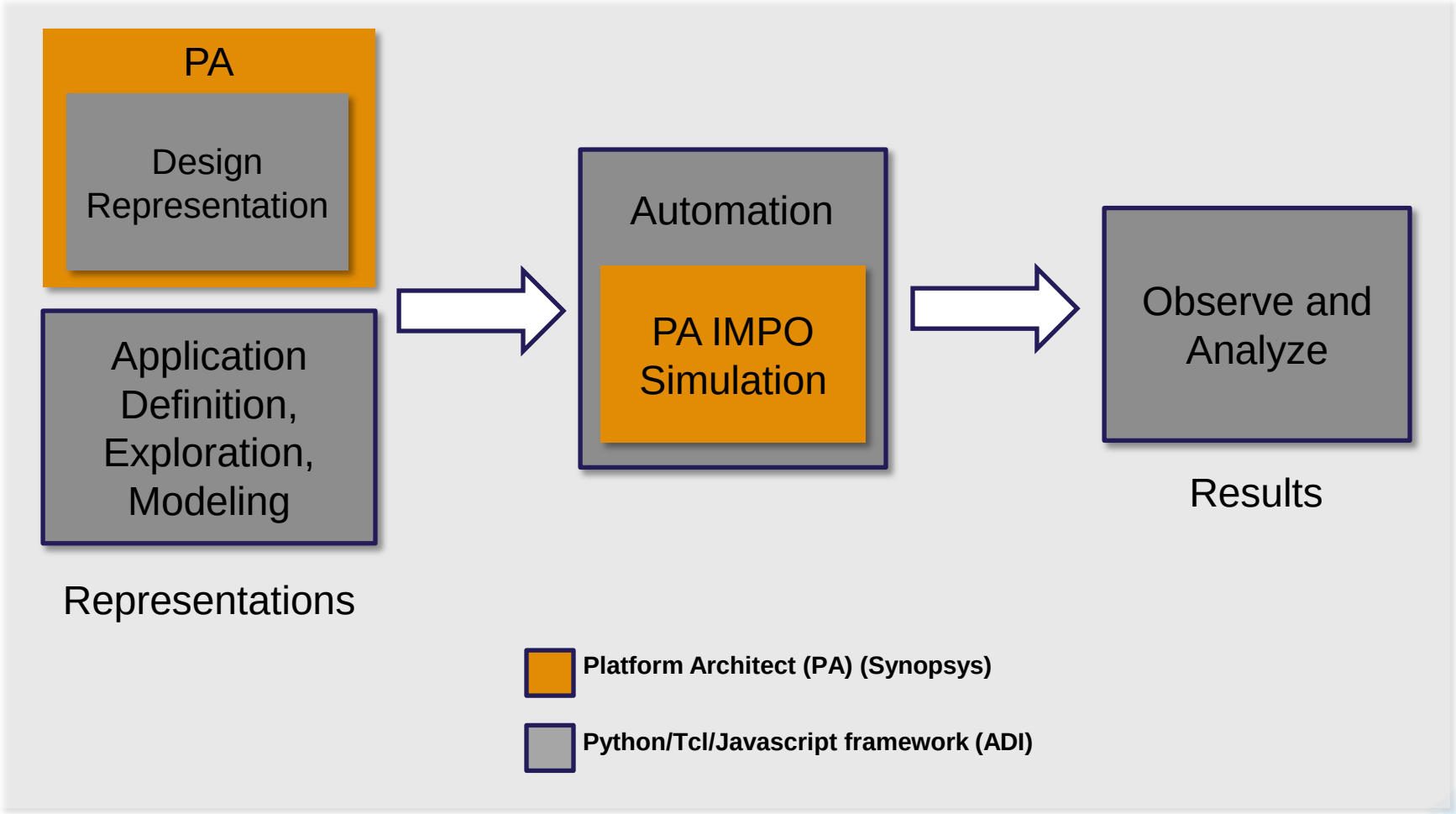
Platform Architect (PA) – IMPO

(Interconnect and memory performance optimization)



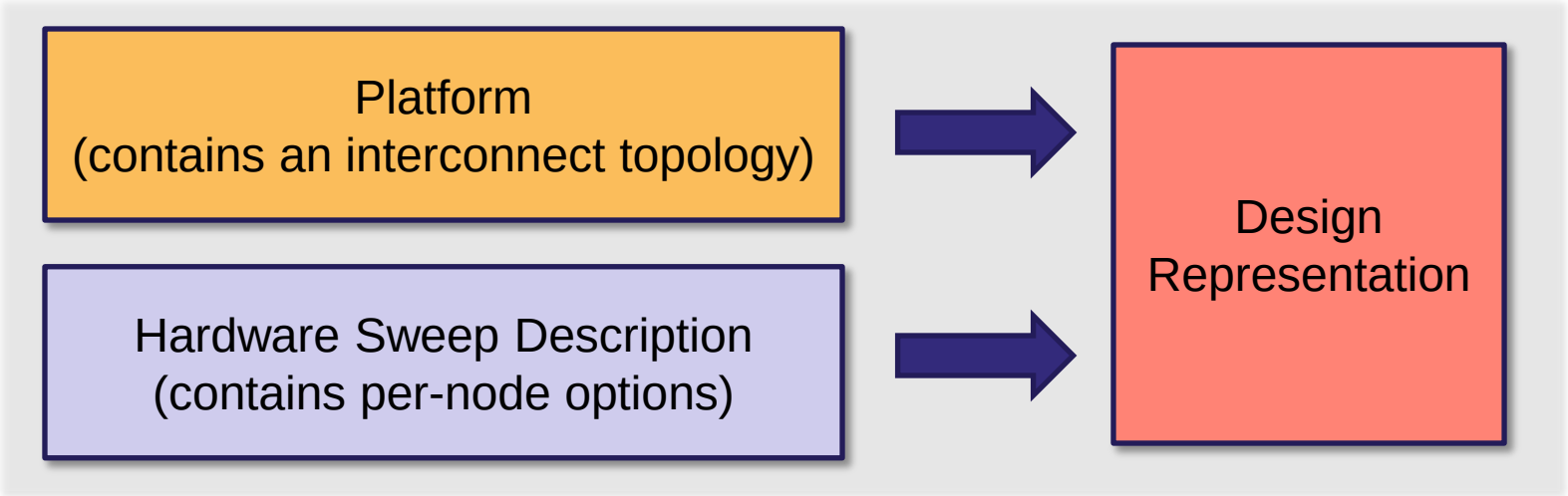
ADI IPA Methodology Overview

Interconnect Performance Analysis



IPA: The SoC Design

- We want to explore different:
  - Interconnect topologies
  - Per-node configuration options
- Need a way to describe these



Challenges with platform assembly

- Platform assembly in Platform Architect is time consuming
  - Especially for larger interconnect designs
- Limits the number of interconnect designs an architect can explore
  - Many manual steps to generate the performance models (IPA platform) when an AMBA Designer interconnect is created/updated
- Back to our goals…

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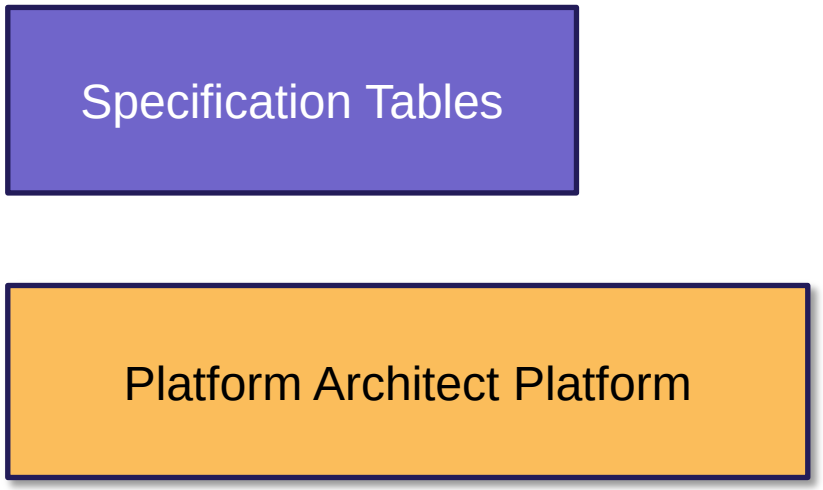
Platform generation from spec



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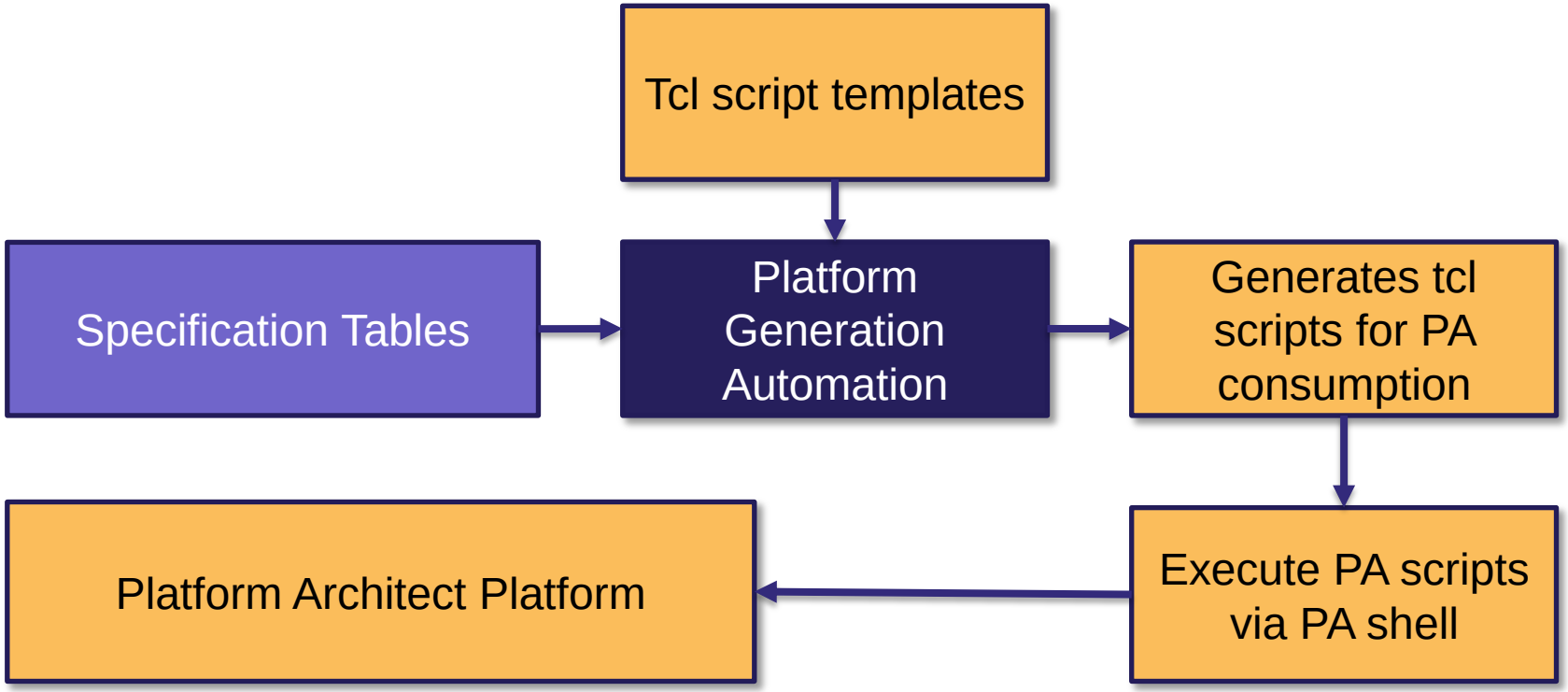
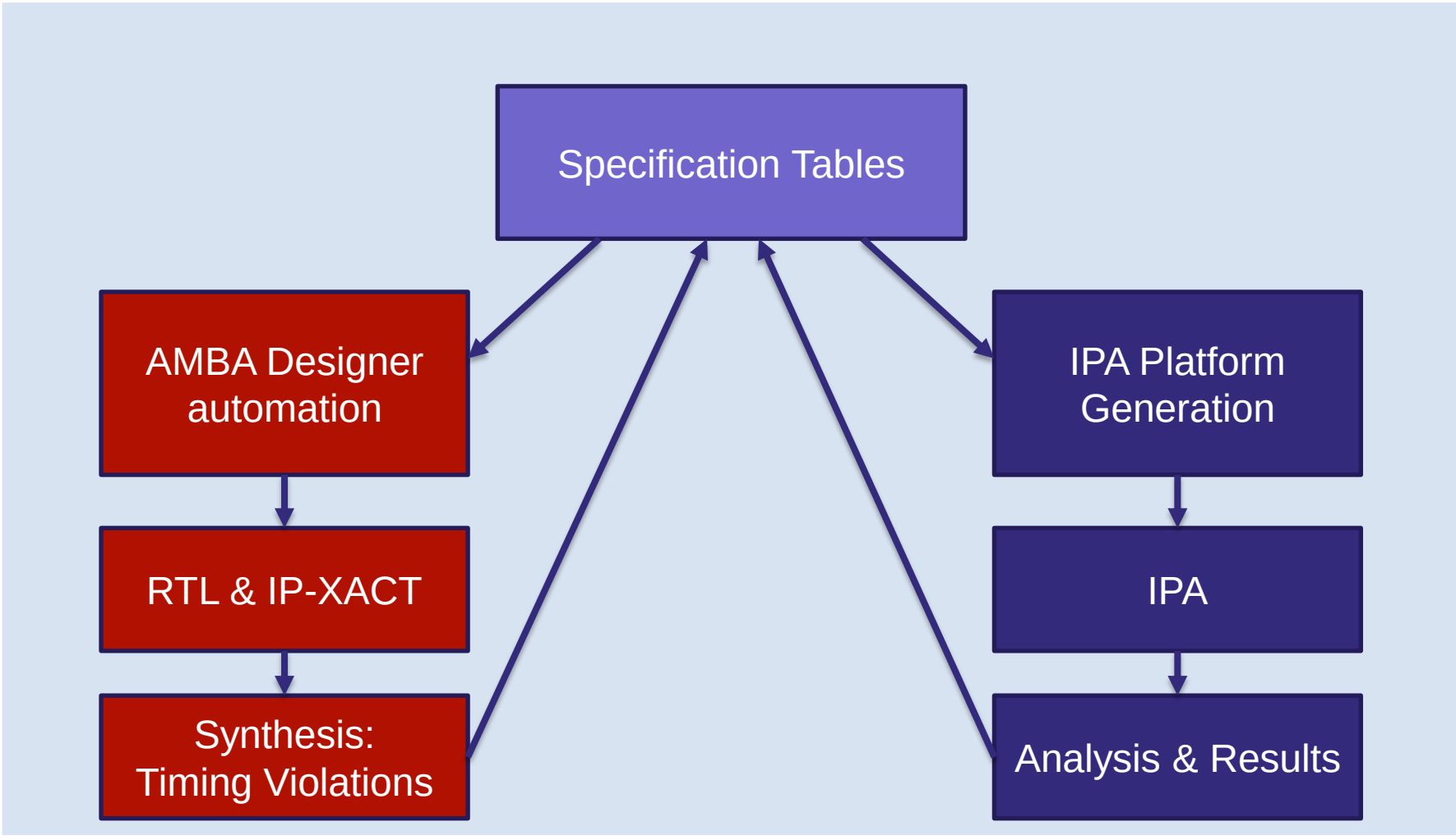


Conclusion

Overall Automation Flow



Q&A

ANALOG DEVICES

snug
Synopsys Users Group

Thank You