# Reset Testing Made Simple with UVM Phases

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#### **Agenda**

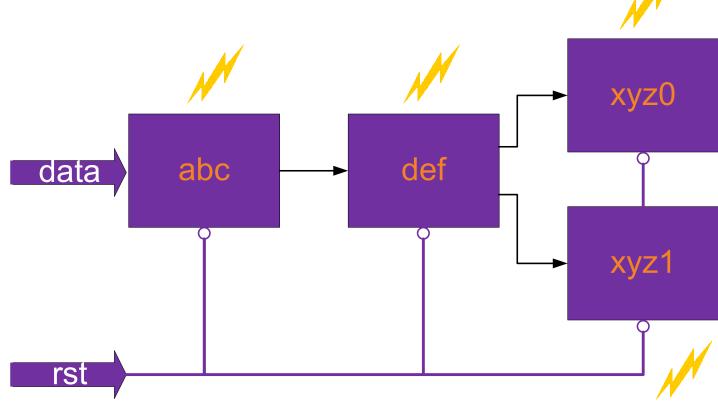


- Why Test Resets?
- Typical Challenges
- Solution
- Types of Reset Testing
- Resetting Components
- Multi-Domain Resets
- Re-Randomizing on Reset
- Conclusions
- Q&A





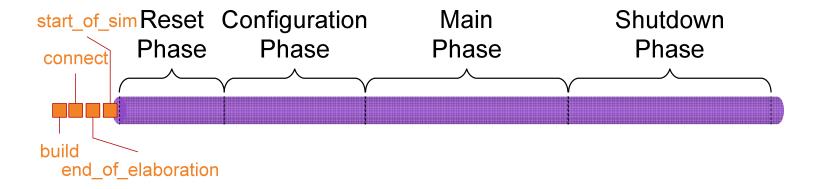
Power is gone, what's the problem?







We already do this in every simulation







We always reset our flops anyway

```
always @ (posedge clk or negedge rst_n) begin
   if(~rst_n) begin
       data_a0 <= 'b0;
       data_a1 <= 'b0;
       data_a2 <= 'b0;
   end else begin
       data_a0 <= data;</pre>
       data_a1 <= data_a0;</pre>
       data_a2 <= data_a1;</pre>
   end
end
                                                        nter
```



#### Why am I here listening to this guy?





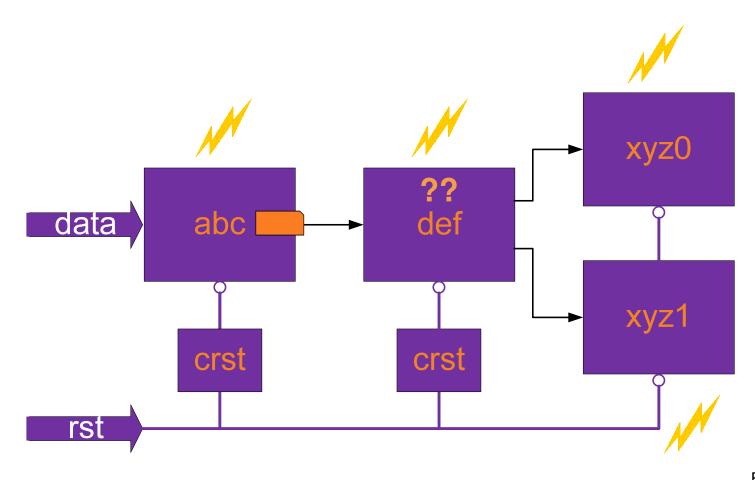


• But the times, they are a-changin'





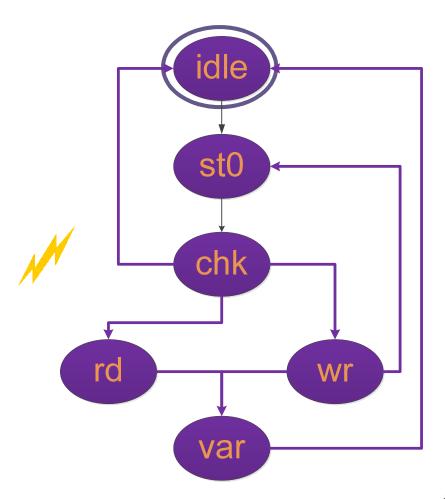








Are you idle?







How could that happen?

```
always @ (posedge clk or negedge rst_n) begin
   if(~rst_n) begin
       data_a0 <= 'b0;
       data_a1 <= 'b0;
       data_a2 <= 'b0;
   end else begin
       data_a0 <= data;</pre>
       data_a1 <= data_a0;</pre>
       data_a2 <= data_a1;</pre>
       data_a3 <= data_a2;</pre>
   end
end
```

unter





- Memories don't clear on reset
- FIFOs are not flushed
- Previous data leaks out
- Statistics are not zeroed
- Soft Resets
- Networking link down/up scenarios
- Multi-Domain Resets
- Your Scenario Goes Here



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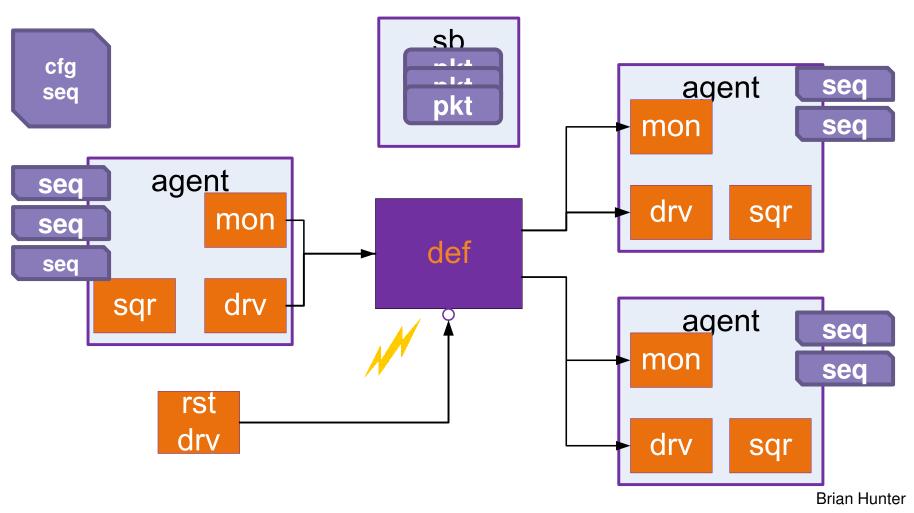


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## **Typical Challenges**







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- Global notification of reset
  - global variables are generally bad practice
  - tlm analysis ports would go all over the place
- Kill sequences
- Kill threads
- Work for VIP, too?





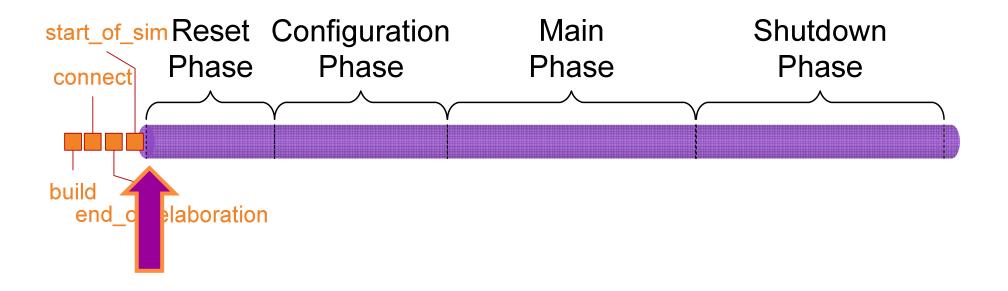
Phase Jumps to the Rescue!



#### Phase Jumps



Phases are a major piece of UVM

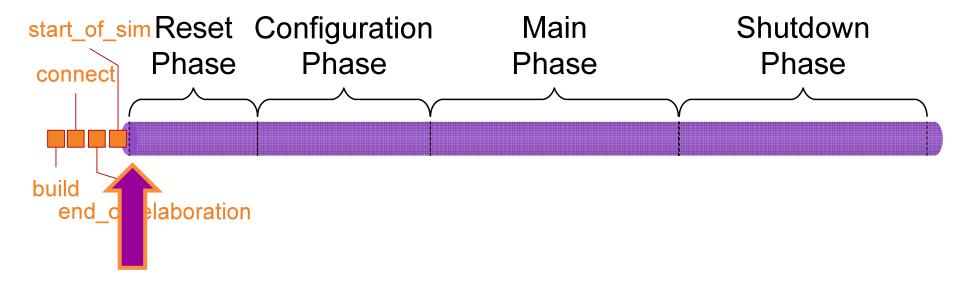




#### **Phase Jumps**



 UVM also has a lesser-known feature called phase jumping





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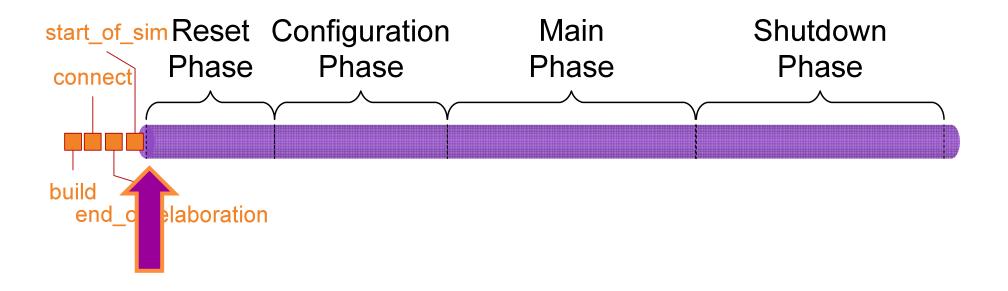


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Idle Reset Testing





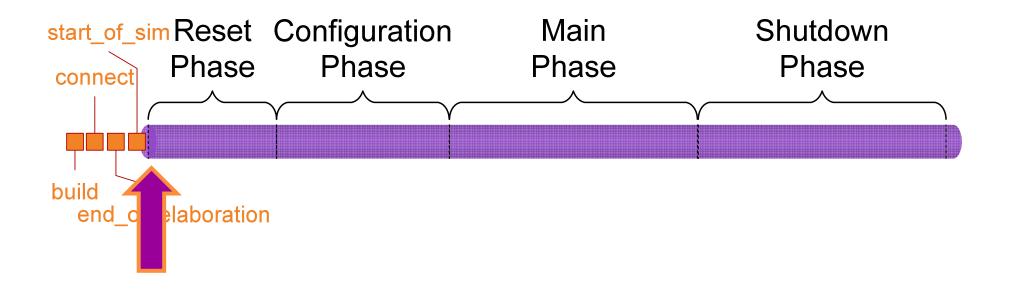


```
class idle reset test c extends basic test c;
   `uvm_component_utils(idle_reset_test_c)
   int run count; // The number of times the test should run
   function new(string name="idle reset",
                uvm_component parent=null);
      super.new(name, parent);
   endfunction : new
   virtual function void phase ready to end(uvm phase phase);
      super.phase_ready_to_end(phase);
      if(phase.get imp() == uvm shutdown phase::get()) begin
         if(run_count == 0) begin
            phase.jump(uvm pre reset phase::get());
            run count++;
         end
      end
   endfunction : phase ready to end
endclass : idle reset_test_c
```





Active Reset Testing





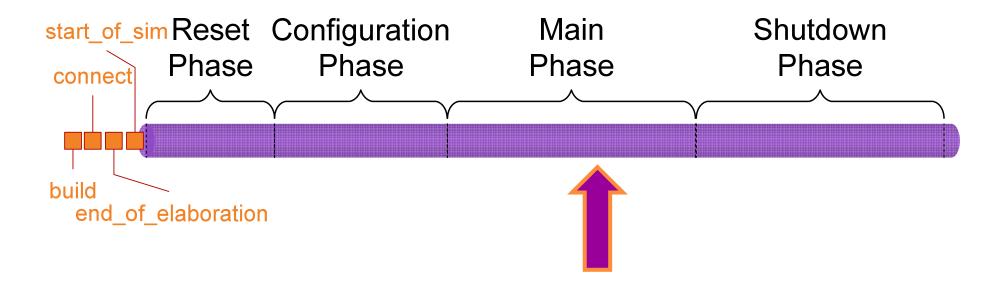


```
virtual task main phase(uvm phase phase);
   fork
      super.main_phase(phase);
   join none
   if(hit_reset) begin
      phase.raise objection(this);
      std::randomize(reset_delay_ns) with {
         reset delay ns inside {[1000:4000]};
      };
      #(reset delay ns * 1ns);
      phase.drop objection(this);
      phase.get_objection().set_report_severity_id_override(
         UVM WARNING, "OBJTN CLEAR", UVM INFO);
      phase.jump(uvm_pre_reset_phase::get());
      hit reset = 0;
   end
endtask : main_phase
```





Soft Reset Testing







• Link-Down, Link-Up





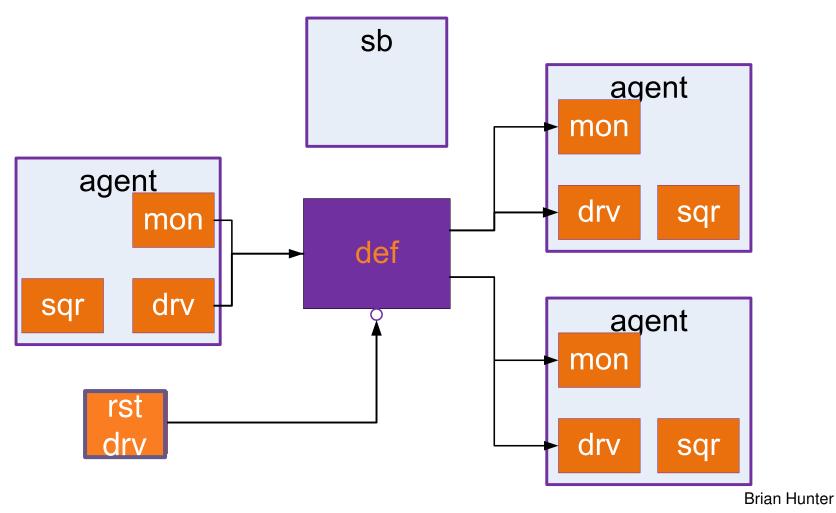
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```
class rst drv c extends uvm driver;
   `uvm component utils begin(rst drv c)
      `uvm field string(intf name, UVM DEFAULT)
      `uvm field int(reset time ps, UVM DEFAULT)
   `uvm component utils end
  // var: rst vi
  // Reset virtual interface
  virtual rst intf rst vi;
  // var: intf name
  string intf name = "rst i";
  virtual function void build phase (uvm phase phase);
      super.build phase(phase);
     // get the interface
     uvm resource db#(virtual rst intf)::read by name("rst intf",
                                          intf name, rst vi)
  endfunction : build_phase
```





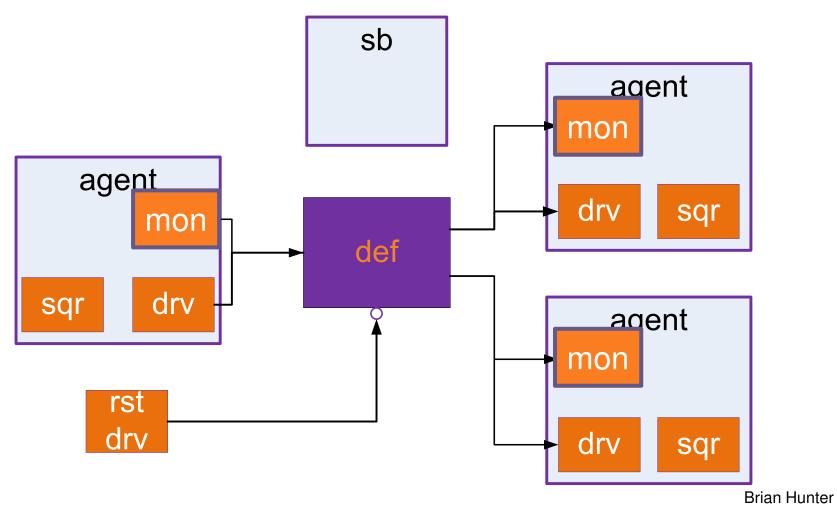
```
// var: reset_time_ps
// The length of time, in ps, that reset will stay active
rand int reset_time_ps;

// Base constraints
constraint rst_cnstr { reset_time_ps inside {[1:1000000]}; }

virtual task reset_phase(uvm_phase phase);
    phase.raise_objection(this);
    rst_vi.rst_n <= 0;
    #(reset_time_ps * 1ps);
    rst_vi.rst_n <= 1;
    phase.drop_objection(this);
endtask : reset_phase
endclass : rst_drv_c</pre>
```











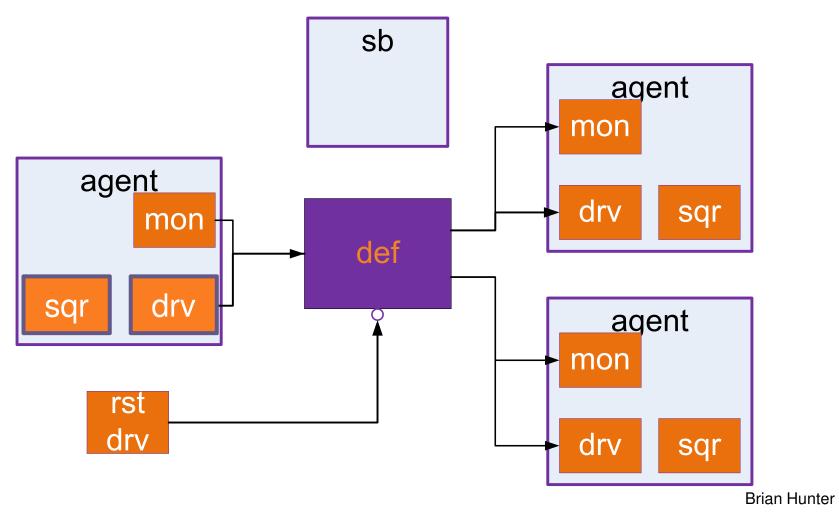
```
class mon c extends uvm monitor;
   `uvm_component_utils(mon_c)
   virtual task run_phase(uvm_phase phase);
      forever begin
         @ (posedge my_vi.rst_n);
         fork
            monitor items();
         join none
         @(negedge my_vi.rst_n);
         disable fork;
         cleanup();
      end
   endtask : run_phase
endclass : mon c
```





```
class drv c extends uvm driver;
   `uvm_component_utils(drv_c)
   event reset_driver;
   virtual task run_phase(uvm_phase phase);
      forever begin
         @(posedge my vi.rst n);
         fork
            drive items();
         join_none
         @(reset_driver);
         disable fork;
         cleanup();
      end
   endtask : run_phase
endclass : mon c
```









```
class agent_c extends uvm_agent;
  `uvm_component_utils(agent_c)
  sqr_c sqr;
  drvc drv;
  ...
  virtual task pre_reset_phase(uvm_phase phase);
    if(sqr && drv) begin
       sqr.stop_sequences();
      ->drv.reset_driver;
    end
  endtask : pre_reset_phase
endclass : agent_c
```





- Scoreboards and Predictors are also components
- Simply erase the contents of expected queues upon detecting resets

```
class sb_c extends uvm_scoreboard;
   `uvm_component_utils(sb_c)

// expected packets
   pkt_c exp_pkts[$];

// clear expected upon reset
   virtual task pre_reset_phase(uvm_phase phase);
        exp_pkts.delete();
   endtask : pre_reset_phase
endclass : sb_c
```

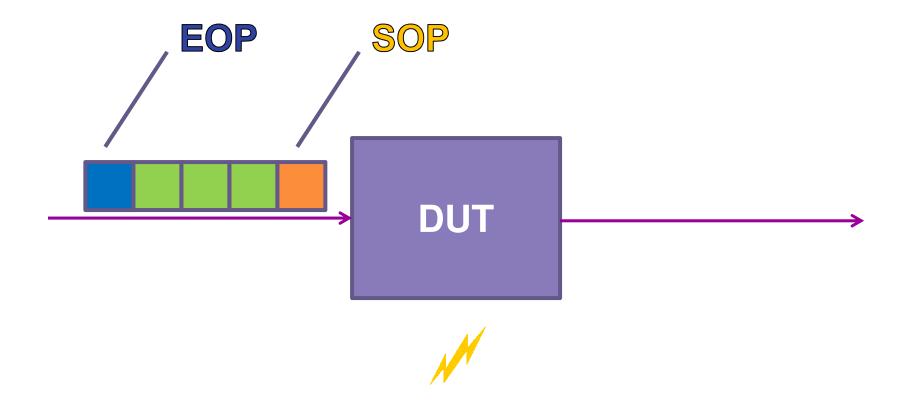




- Some predictions can be very difficult
  - In one simulation, no packets come out after resets
  - In another simulation, the first expected packet happens to come out on the same cycle as the pre\_reset phase
- All tests must be self-checking. All tests must pass.
- Try a ternary scoreboard
- Mark traffic as unpredictable









## **Resetting Components**



```
class sb c extends uvm scoreboard;
   `uvm component utils(sb c)
   uvm analysis imp rcvd pkt #(pkt c, sb c) rcvd pkt imp;
  pkt c exp pkts[$];
   // mark all outstanding packets as unpredictable
   virtual task pre_reset_phase(uvm_phase phase);
      foreach(exp pkts[num])
         exp_pkts[num].unpredictable = 1;
   endfunction : write_soft_reset
   function void write_rcvd_pkt(pkt_c _pkt);
     pkt c exp pkt = exp pkts.pop front();
      // unpredictable packets are ignored
      if(exp pkt.unpredictable)
         return:
      else if(exp_pkt.compare(_pkt) == 0)
            `uvm error(get full name(), "Packet Miscompare.")
   endfunction : write rcvd pkt
endclass : sb c
```

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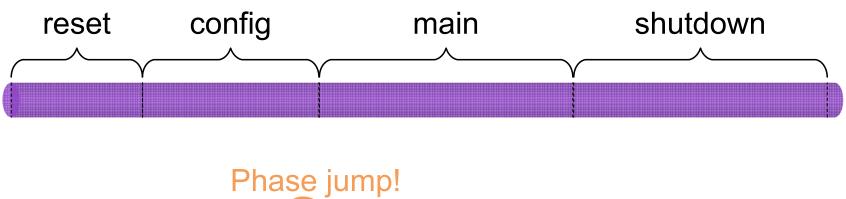


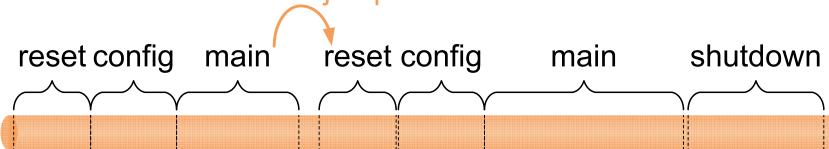


scoreboard DUT p\_agent b\_agent p\_domain **b\_domain** p\_rst\_drv b\_rst\_drv



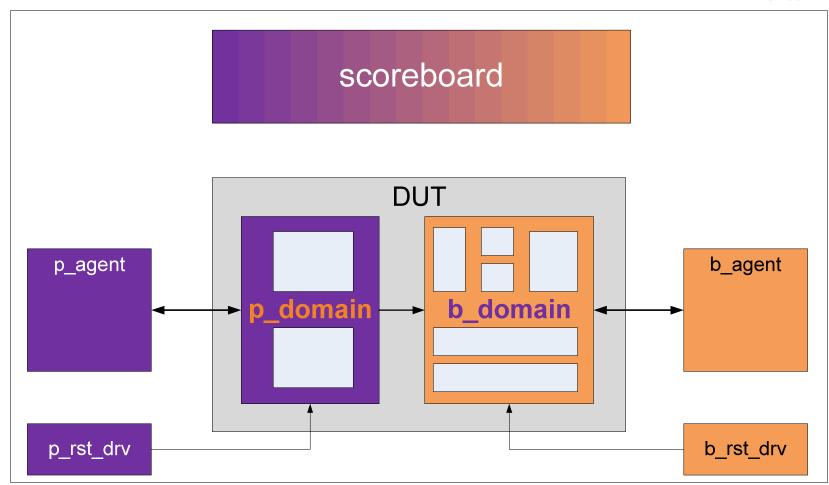
















```
uvm_domain p_domain;

virtual function void build_phase(uvm_phase phase);
    super.build_phase(phase);
    p_domain = uvm_domain::type_id::create("p_domain");
    p_agent.set_domain(p_domain, .hier(1));
endfunction : build_phase
```





```
virtual task main_phase(uvm_phase phase);
      fork
         super.main_phase(phase);
      join none
      if(run count == 0) begin
         phase.raise_objection(this);
         randomize();
         #(reset delay ns * 1ns);
         phase.drop_objection(this);
         p_domain.jump(uvm_pre_reset_phase::get());
         run count++;
         // tell scoreboard that a reset occurred
         -> scoreboard.p_domain_reset;
      end
   endtask : main_phase
```



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## Re-Randomizing on Reset



```
class cfg c extends uvm object;
  // The number of transactions to send
  rand int num trans;
  // All of the configuration space registers can be randomized
                                    device id = 0x14972048
  rand reg block c config space;
  // how fast is your clock?
                                   490
  rand int period ps;
  // Run in PCI, PCI/X, or PCI
                                 Structural Variable
  rand pci mode e pci mode;
  // The number of PCI agents
                                 Structural Variable
  rand num pci agents;
endclass : cfg c
```



## Re-Randomizing on Reset



```
class cfg c extends uvm object;
  // The number of transactions to send
   rand int num trans;
   // All of the configuration space registers can be randomized
   rand reg_block_c config_space;
     // Ensure that structural variables are only randomized once
     function void post_randomize();
        pci_mode.rand_mode(0);
        num_pci_agents.rand_mode(0);
     endfunction : post_randomize
   // The number of PCI agents to create
   rand num pci agents;
endclass : cfg c
```



## Re-Randomizing on Reset



```
class active reset test c extends base test c;
  rand cfq c cfq;
  virtual task pre_reset_phase(uvm_phase phase);
      randomize();
  endtask : pre_reset_phase
  virtual task main_phase(uvm_phase phase);
      fork
         super.main_phase(phase);
      join_none
      if(hit_reset) begin
         phase.raise objection(this);
         std::randomize(reset_delay_ns) with {
            reset delay ns inside {[1000:4000]};
         };
         #(reset_delay_ns * 1ns);
```



#### **Conclusions**



- Functional reset testing is getting more important
- Reset testing used to be very complicated
- UVMs phases and phase jumping make these tests easy-peasy
- Some *minor* component changes need to be made
- If you avoid the use of structural variables, you can re-randomize everything all in one simulation!

