Mixed-Signal Validation From a Full-Chip Perspective

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Agenda

Introduction

Methodology

Issues Encountered

Results

Future Improvements

Conclusion

Introduction

Introduction

Historically

- At SoC Level – Analog blocks were modelled using System-Verilog Behavioural Models

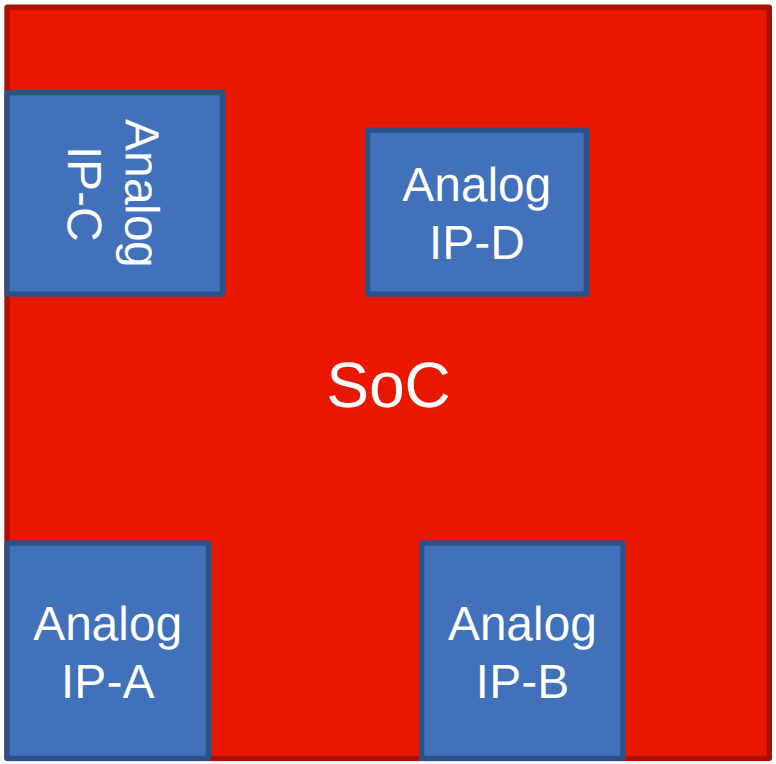
- For simplicity at SoC level – some models may have been disabled or reduced in functionality to decrease simulation time

- Issues found previously:
  - Incorrect State Machine Start-up Sequence
  - Incorrect Forces on PLL clocks
  - Glitches on PI Clocks
  - Floating nodes and inverted nodes

Introduction

Typical Design

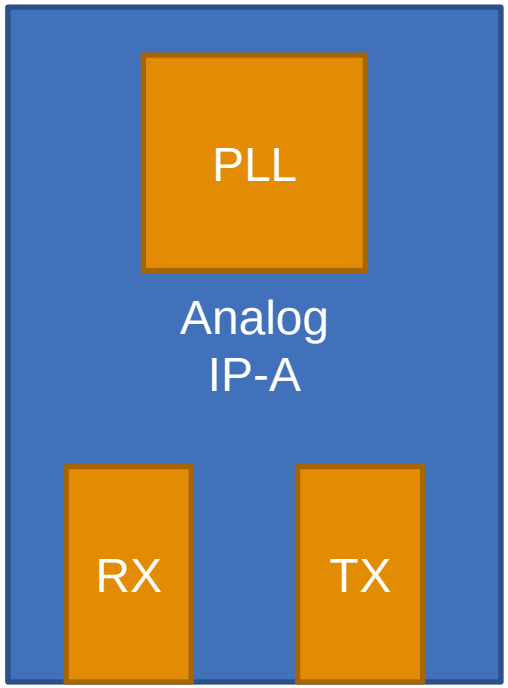
- Interface IO's –
  - GPIO's,
  - HSIO's
  - Etc.
- Internal Analog Blocks
  - PLL
  - Thermal Sensor
  - Voltage Regulators
  - Etc.



Introduction

High-Speed IO

- Multi Port HSIO
  - Multiple Lanes of TX and RX
- PLL Frequency at 10GHz
- Only concentrated on one TX and one RX Port



Introduction

Our Aim/Goal

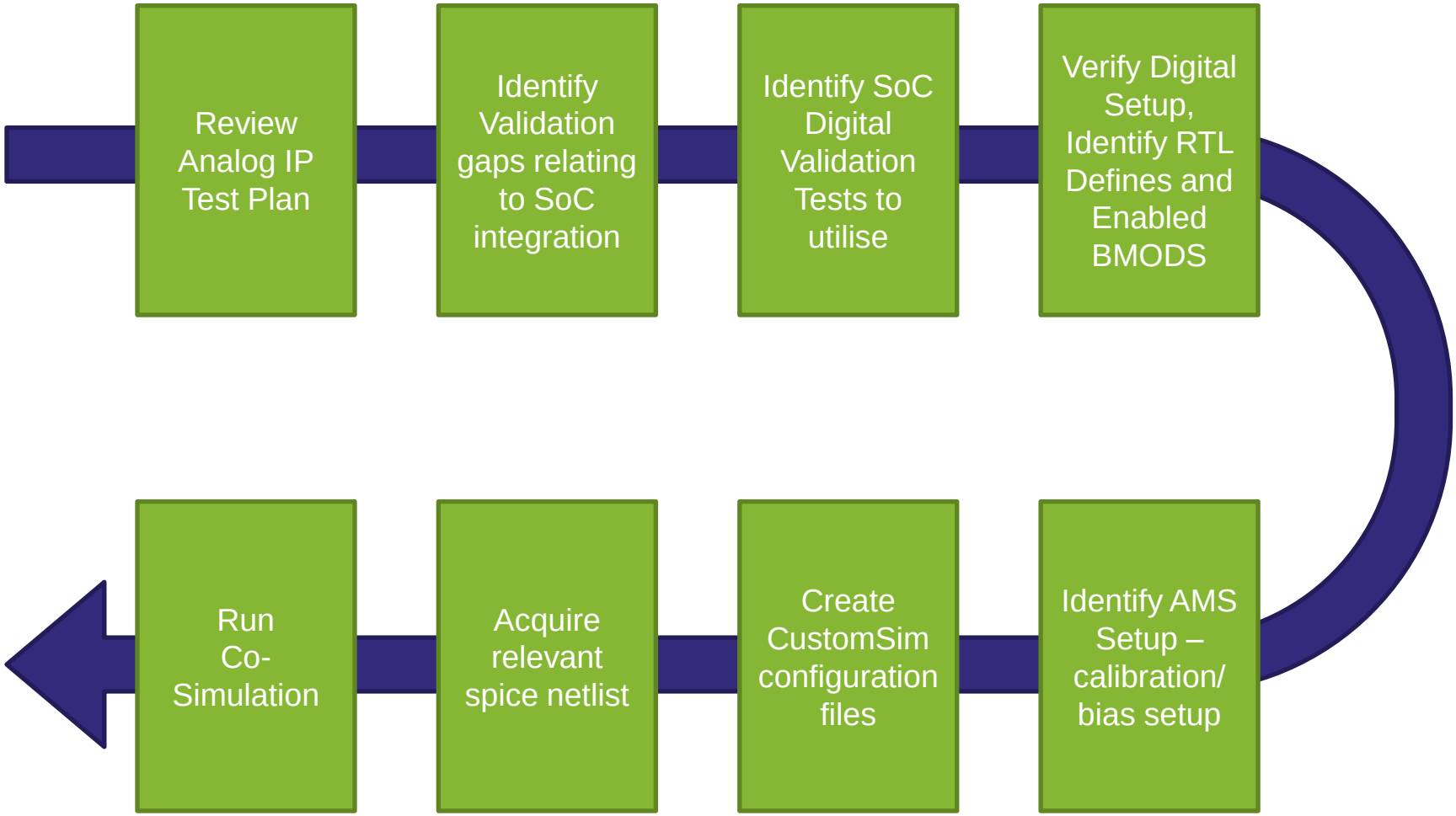
- Validate the interconnectivity and data flow between Analog Blocks and the SoC

- Not necessarily to verify internal components of the IP.

- Verify some crucial components within the IP such as
  - PLL Frequencies
  - Divided clock frequencies
  - Vp-p and Vcm of various components on data path of RX/TX
  - Power up sequence of state-machines

Methodology

Methodology



Issues Encountered

Issues Encountered

Interaction with IP teams

- Started off on a ‘Solo Run’ trying to determine the correct setup to use in the CustomSim Configuration files
- Incorrect bias setup, calibration setup
- Majority of cases, the final configuration files were same as IP team

Issues Encountered

SoC Environment

- Channel Models were not available in SoC environment
  - Required manual instantiation
- A Model of the TX FIR output, not present at the RX input in SoC level
  - Required manual instantiation
- IP release model vs Integrated SoC Model
  - SoC model typically does not immediately integrate the Analog IP
  - Some issues we were noticing were due to an older version of the IP being integrated into SoC environment

Issues Encountered

Test Availability

- Entirely dependant on Digital SoC team for our Tests
- Required tests not developed or still WIP
  - Reset test initially to pipe clean flow
- Random feature in digital tests did not suit our needs

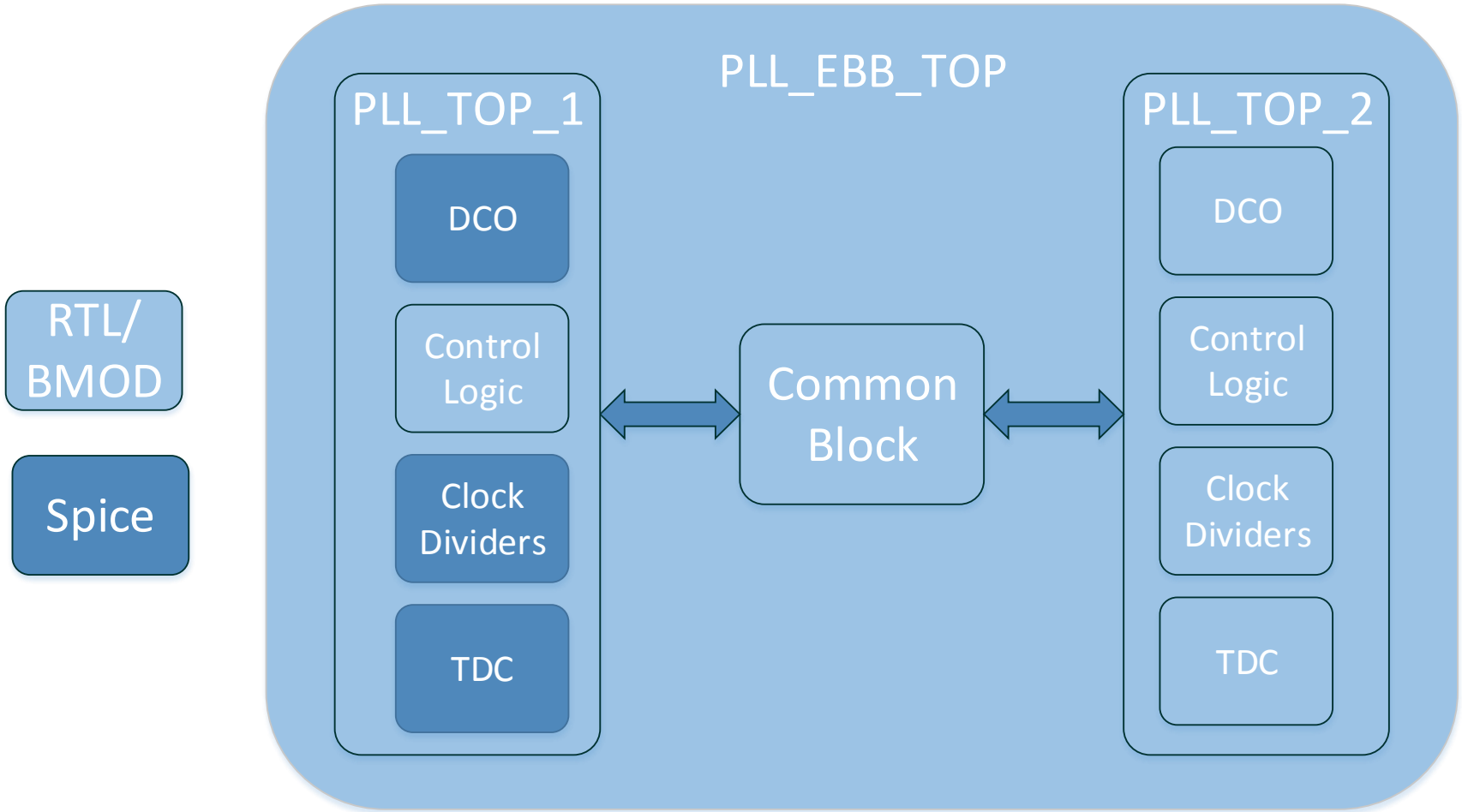
Issues Encountered

Port Direction

- Incorrect a2d/d2a thresholds implied on certain input/output ports
- Important to verify contents of *interface_element.rpt*
- Use port_dir command in .init file:
  - port_dir -cell invs1 (input a; output y);

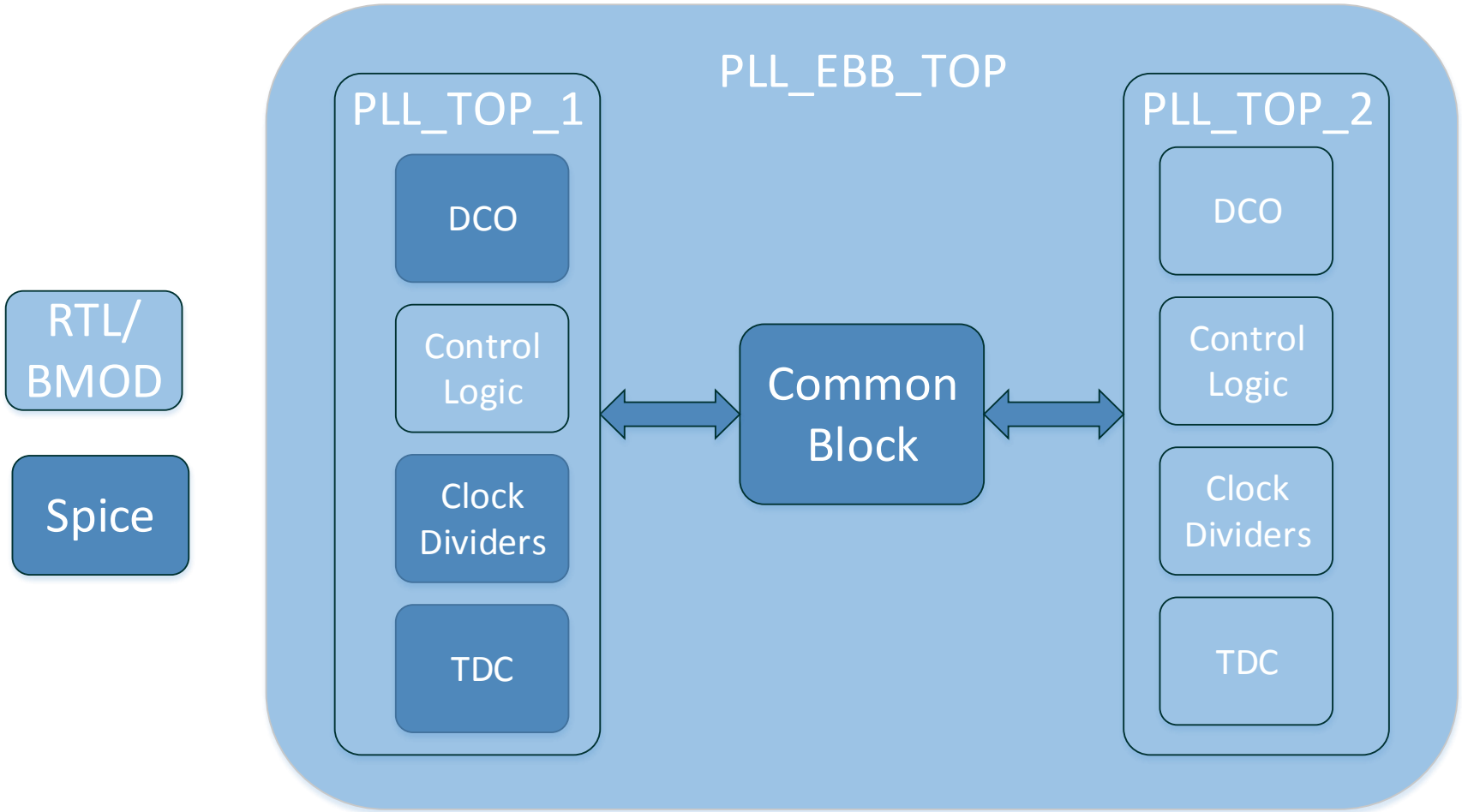
Issues Encountered

PLL Trial 1



Issues Encountered

PLL Trial 2

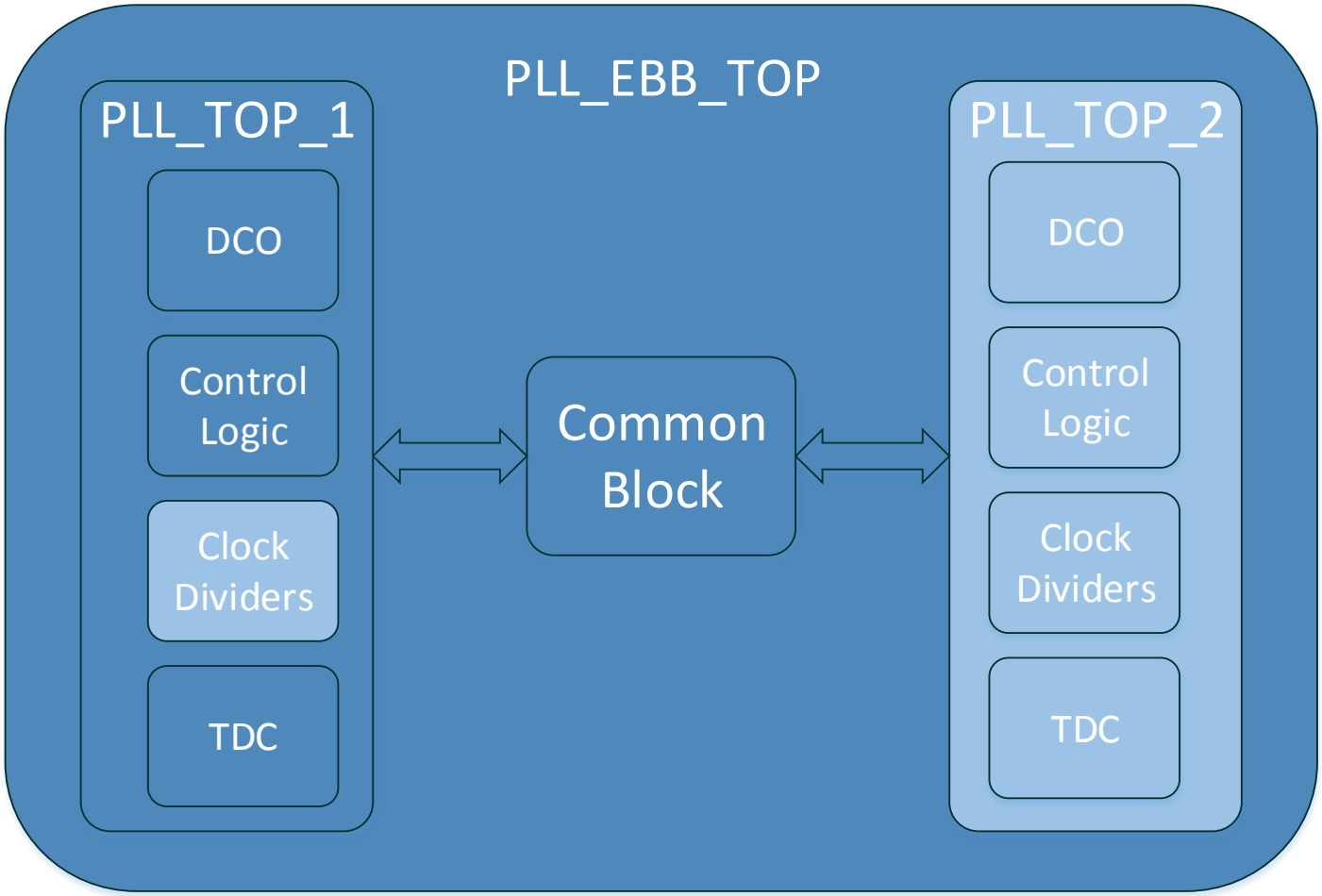


Issues Encountered

PLL Trial 3

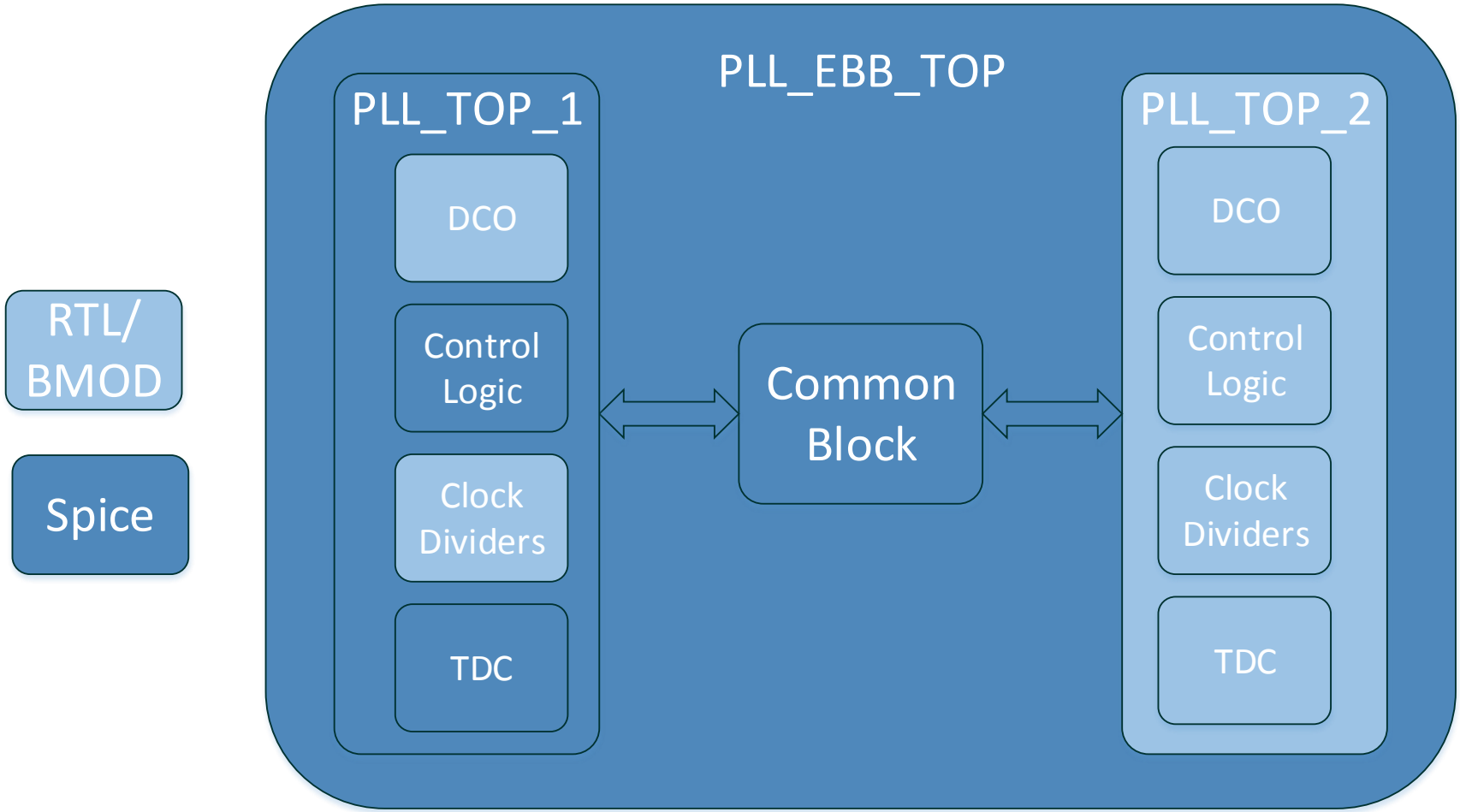
RTL/ BMOD

Spice



Issues Encountered

PLL Final Setup



Results

Results

Simulation Time

Run Type	Simulation Run Length	Netlist Element Count
(1) VCS – Ceratin BMODS disabled	15hrs	
(2) VCS – ALL BMODS enabled	31hrs	
(3) VCS-AMS – RX as spice	10days	700,000
(4) VCS-AMS – TX as spice	3.5days	700,000
(5) VCS-AMS – PLL_EBB_TOP as spice	2days	35,000

Results

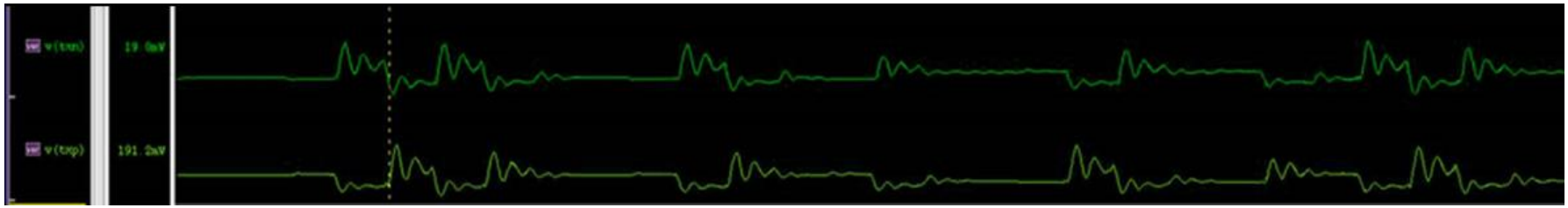
Results for HSIO - RX

- Initially certain Vp-p and Vcm specifications in RX component failed
- Some settings such as calibration, gain values and state machine timers were set for SoC team digital test which were not appropriate to our needs
- Once correct setup was attained we achieved an overall pass based on our test criteria

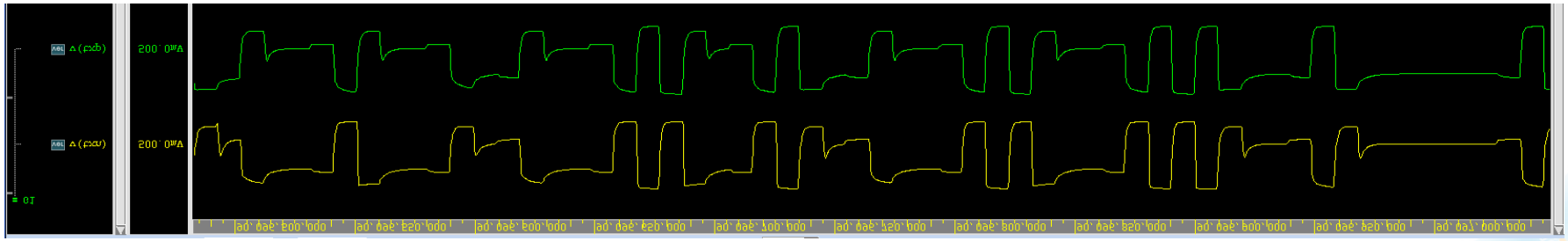
Results

Results for HSIO - TX

- TX results completed with a pass
- Low numbers of issues in setup and debug
- Inductors on TX pads caused ringing that was hard to set correct a2d thresholds
- With Inductors:



- Without Inductors:



Results

Results for HSIO - PLL

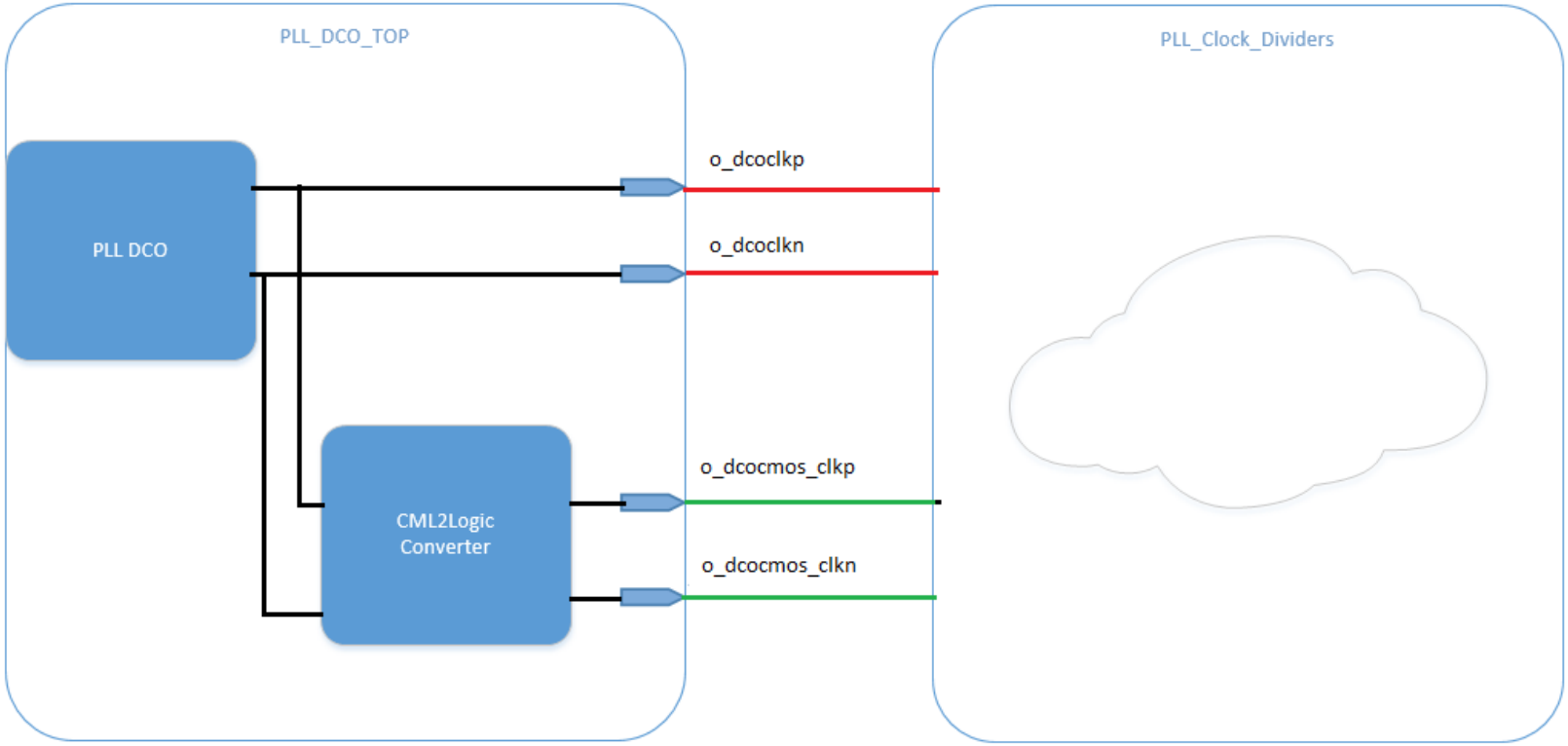
- Once initial trials were completed, we achieved an overall pass

- Due to high quality of unit level Mixed Signal Validation, we saw limited gain in pursuing our debug to get PLL DCO to lock as spice

Results

Other IP results

- Thermal sensor power up sequence bug found
- PLL and clock divider circuit had incorrect connections



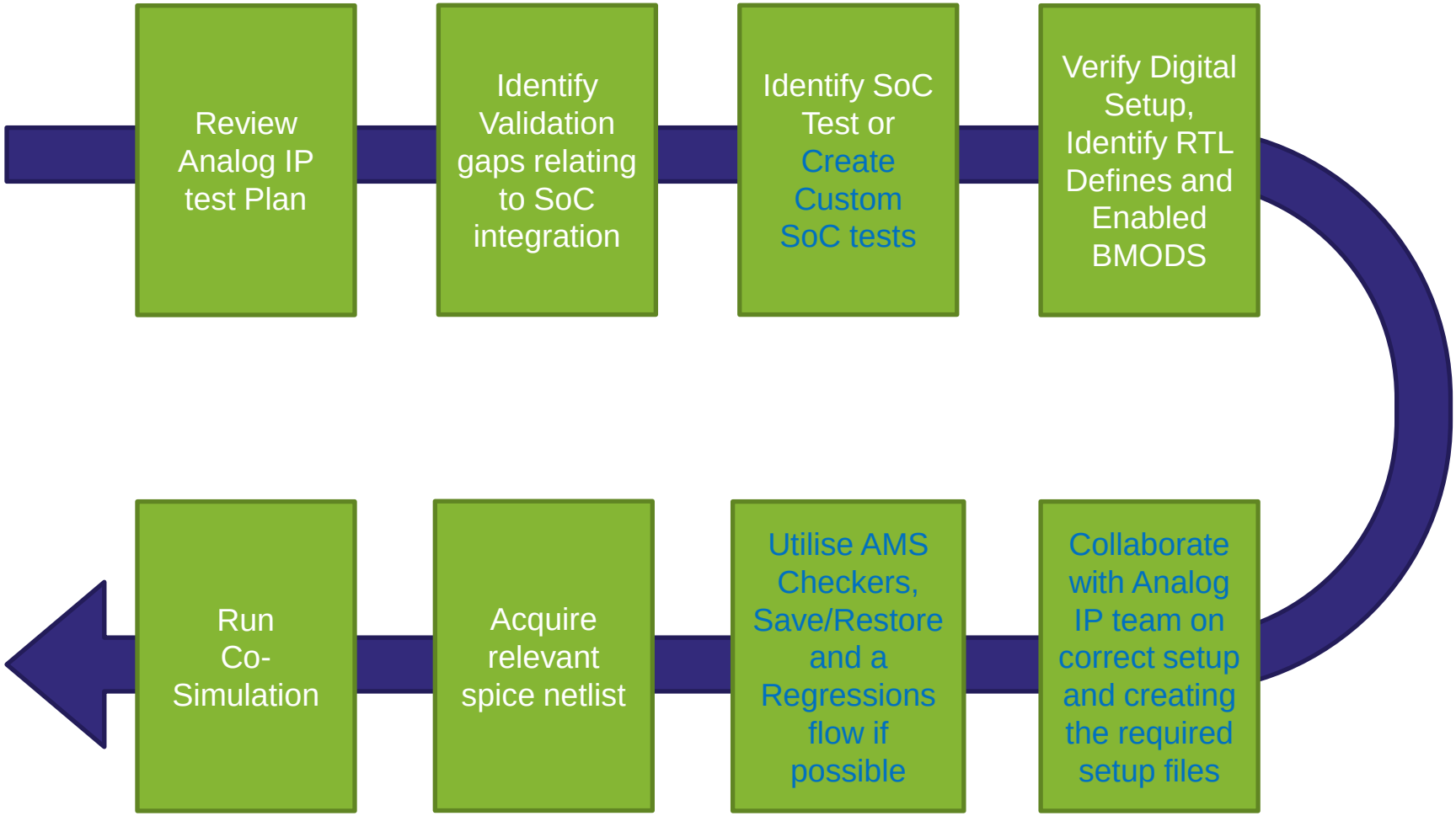
Future Improvements

Future Improvements

- AMS Checkers
- Regression Flow
- Save/Restore
- Early engagement with IP team
- Targeted SoC AMS Tests

Future Improvements

Updates to AMS Flow



Conclusion

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- MSV was easy to integrate into SoC environment
- Good working relationship required with Analog-IP team to avoid initial setup issues
- Setup files from Unit Level simulations can be easily ported to SoC level
- Should consider MSV at SoC Level for Analog-IP's with limited MSV at unit level
- Risk assessment on IP's with good MSV at unit level

Thank You