



# Verifying C++ Firmware Sequences In UVM Environment

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# Agenda

Introduction

**Testbench Updates** 

Firmware Vs RTL Verification

Scoreboard For Firmware

Conclusion

## Introduction

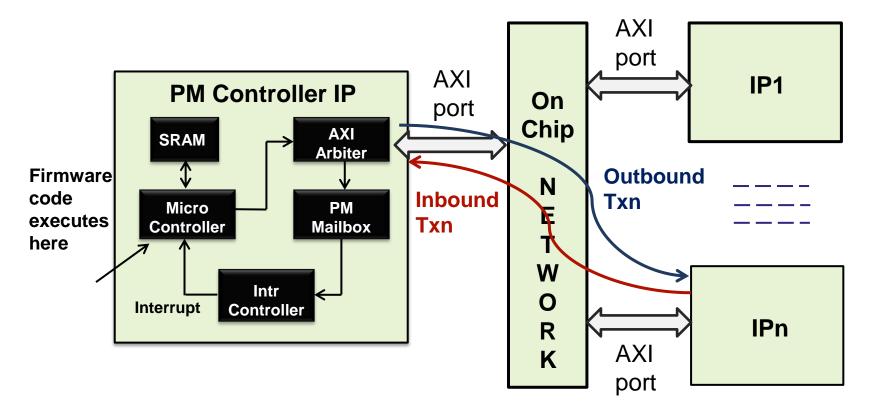


- What is firmware?
  - C++ code executing on microcontroller
- Power management firmware in AMD designs
  - Dynamically manages the power states in the entire design
- Need for VCS verification
  - Firmware is an AXI agent
  - Involves interactions with multiple components
  - Needs to be simulated in VCS with other agents/sub-blocks to verify datapath and connectivity in the system
  - Post Si bring-up times are increasing steadily due to unqualified firmware

## Introduction



Firmware as an AXI agent in the system



## Introduction



- Verification platforms for firmware
  - VCS
  - Instruction set simulator (simulation model for the micro-controller)
  - Post silicon bring-up

Platform	Cycle Accurate	Debug Turnaround	What is covered?
VCS/UVM testbench	Yes	Medium	Hardware interactions
Instruction Set Simulator	No	Fast	Mathematical computations
Post-Silicon bring- up	Yes	Medium	Real time scenarios

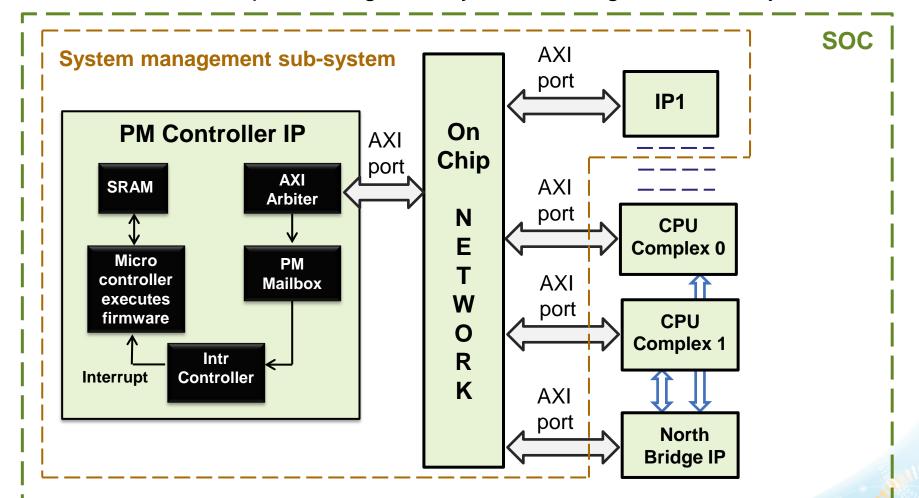




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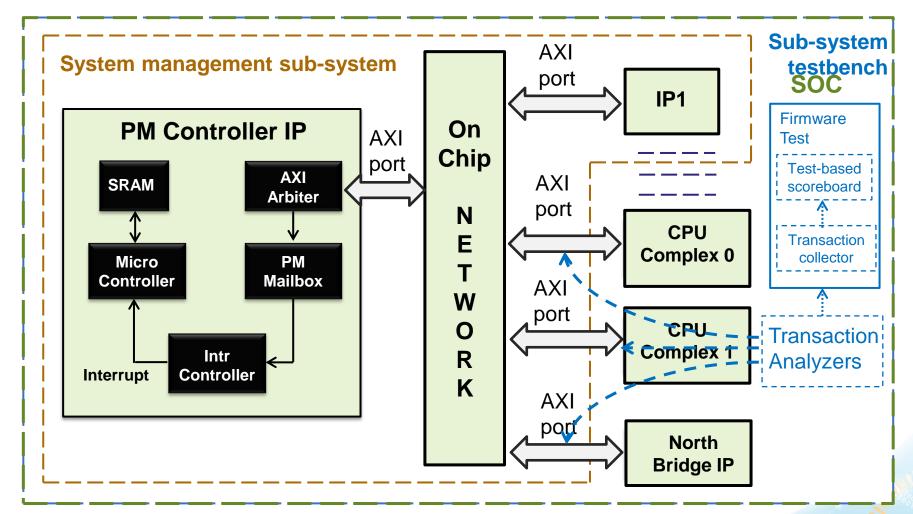
### **Verification Scope**

Firmware development begins in system management sub-system





## System management sub-system verification



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### Testbench components

#### AXI BFM

- Mimics the actions of an AXI agent on the network
- Can initiate read/write to an AXI agent and receive read/write from an AXI agent
- Pre-developed verification component
- Easy modelling of non-RTL components

### Transaction Analyzer

- Generic implementation using uvm\_subscriber class
- Used for detecting transactions at key AXI interfaces and qualifying firmware sequence
- Used for determining when to set up response registers in AXI BFMs (to mimic IP behavior)



### Transaction analyzer using uvm\_subscriber class

```
class core axi slv export \#(type\ T = axi\ write\ req\ txn,\ type
parent ptr = firmware top env) extends uvm subscriber;
parent ptr ptr;
                                                      Uniquely identify the
bit [`NUM CORE PER COMPLEX-1 : 0] core id;
                                                      subscriber component
bit [`NUM OF COMPLEXES-1 : 0] complex id; <
                                                      Populate component
                                                      variables in an
                                                      iterative structure from
                                                      the parent class
ptr.core prefill queue[complex id][core id].push back
                                                      (transaction);
endfunction
                                                Use in a forever loop in
endclass : core axi slv export
                                                base test to process
                                                transactions at key
                                                interfaces
```



## Firmware Vs RTL Verification



## Firmware Vs RTL Verification



#### Similarities

- Testbench infrastructure (firmware, an AXI agent is RTL)
- Stimulus in the tests
- Verification for datapath and connectivity

#### Differences

- Verification for correctness is the distinguishing factor
- Firmware qualification is a sequence check
- Cannot be covered with IP checkers





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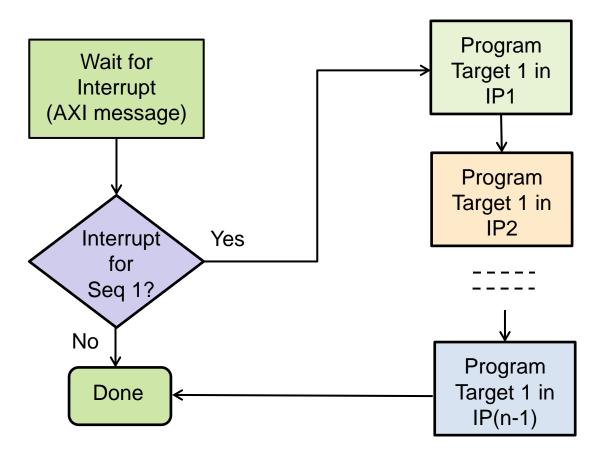
#### Overview

- Need for firmware scoreboard
  - Does the firmware execute a sequence correctly?
- Can we use standard UVM scoreboard?
  - UVM scoreboard is suitable for protocol checking
  - Knowledge of what firmware must execute is in the test, scoreboard must therefore be in the test
  - Sequence check in a multi-IP sub-system is complex with standard scoreboard
- What does firmware scoreboard involve?
  - Transaction collector using analysis ports
  - Test-based enumerated scoreboard



#### Test-based enumerated scoreboard

- Step by step procedure
  - 1. Read the firmware specification, identify key programming steps





#### Test-based enumerated scoreboard

2. Create an enumerated structure for the targets in the sequence

```
typedef enum {
          Target_1,
          ...
          Target_N,
} pm_event;
```

3. Create the scoreboard (SCBD) as a hash variable

Key – targets in the sequence; Value – TRUE or FALSE



#### Test-based enumerated scoreboard

4. Populate the expected SCBD hash at the start of the test

5. Mark the actual SCBD during transaction collection

```
if (txn.addr == <interesting addr 1>) begin
     pm_event_scbd [Target_1] = TRUE;
end
```

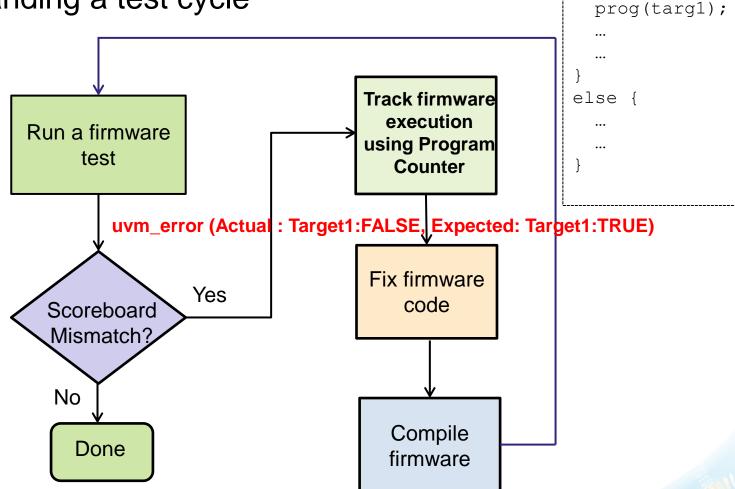
6. At the end of the test, compare expected and actual SCBD hashes

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if (cond1) {

### **Evaluating failures**

Understanding a test cycle





## Conclusion



## Conclusion



- Problem point
  - Simulate firmware C++ sequences
  - Verify firmware sequence for correctness
- What did it involve
  - Testbench updates
  - Test-based scoreboard
  - Regression cycle with firmware tests
- Outcome
  - Verify hardware interactions of firmware
  - Deliver clean code and help speed up to post-silicon bring up



Ashwini debugs the firmware bug with the help of test-based scoreboard!





# **Thank You**

