

# Sharing Generic Class Libraries in SystemVerilog Makes Coding Fun Again

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#### Look familiar?

```
`define min(x,y) ((x)<(y)?(x):(y))
function bit random_bool( int unsigned true_percentage );
  return $urandom_range(99) < true_percentage;
endfunction
               task watch_event( event e, time timeout );
                 fork // thread firewall
                   begin
                     fork
                      @e ;
                      #timeout $error( "timeout" );
                    join_any
                    disable fork;
                  end
                                           ... but no open
                join
             endtask
                                          library is available
```



# Why are these functions rarely shared?

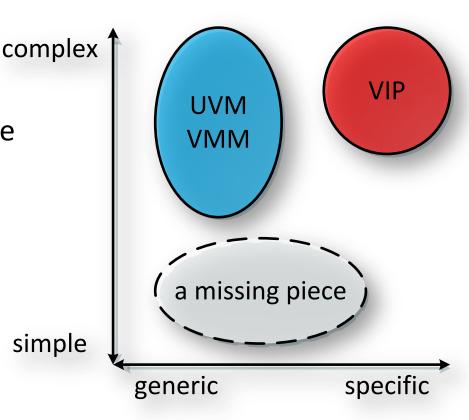
- Most people lack the time to develop them
  - Creating robust functions requires thorough verification
  - Defining consistent and configurable functions is not trivial
  - Writing API documents is a burden
- Some functions are relatively easy to develop
- Sharing them might be difficult, both technically and legally



### What does a shared library offer you?

- Sharing a library allows you to:
  - save time
  - write more readable code
  - focus on project-specific logic
  - avoid common mistakes
- A shared library can evolve and be fixed by peers

simple





# How did we create this library?

- Investigated nine verification projects from various domains:
  - Array processor
  - Image processor
  - SoC interconnects
  - Mobile peripherals
- Surveyed other programming languages
  - C++, Java, Python, Perl, Ruby, JavaScript



# What functions does the library provide?

- Text Processing
- Containers
- Strategy
- Verification-specific
- Domain-specific

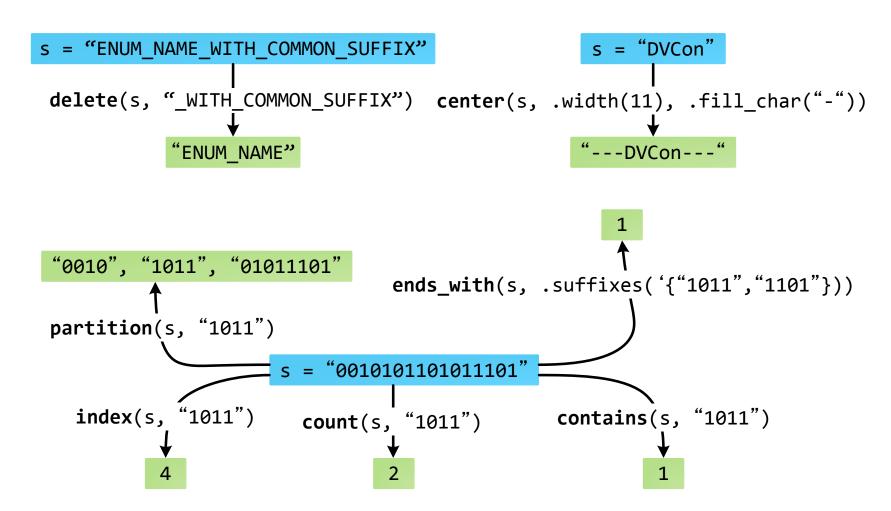
... about 360 methodology-independent low-level functions



#### **TEXT PROCESSING**

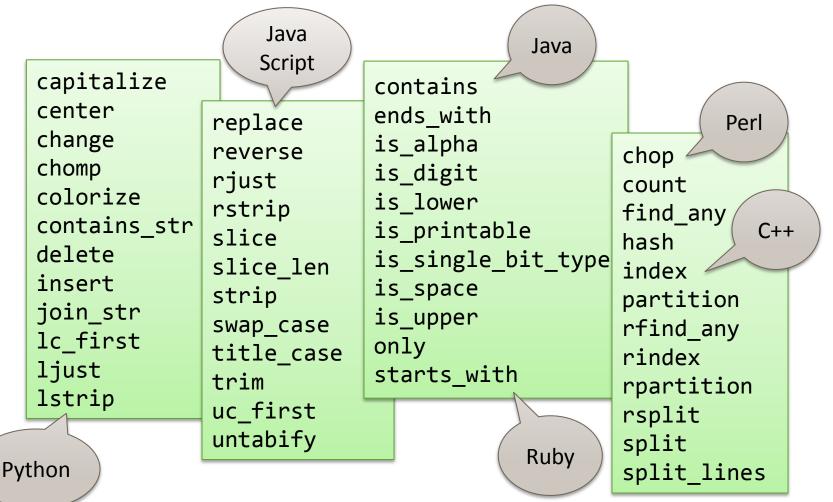


### What can you do with the text-processing library?





# What functions are in the text-processing class?





### How we implemented the text-processing class

All text functions are static

```
s = text::capitalize( "capitalize me" );
```

- Two implementations
  - SystemVerilog only
  - SystemVerilog with C++

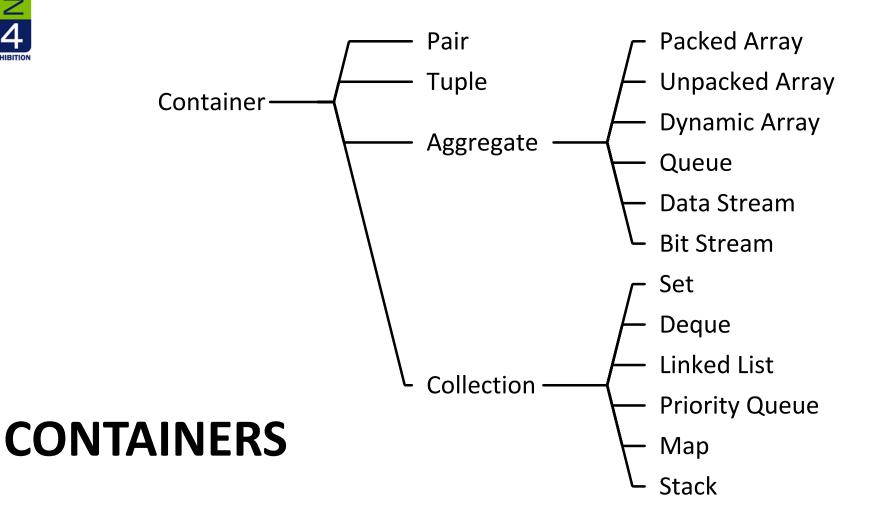


#### My favorite function: colorize

```
$display( text::colorize(
"message in green", ——
 FG GREEN) );
$display( text::colorize(
 "white on red",
 FG WHITE, BG RED) );
$display( text::colorize(
 "underlined boldface",
 .underline(1), .bold(1)) );
```

```
keisuke@d...thub/cluelib = = *
message in green
<u>whi</u>te on red
<u>underlined</u> boldface
```







### Container: A data structure that collects other objects

• Pair (■,□)

```
pair#(int, string) p;
p = new( 123, "message" );
return p; // as a single unit
```

- Tuple ( , , , , , , , , , , , , , )
- Aggregates
- Collections

All containers are parameterized classes.

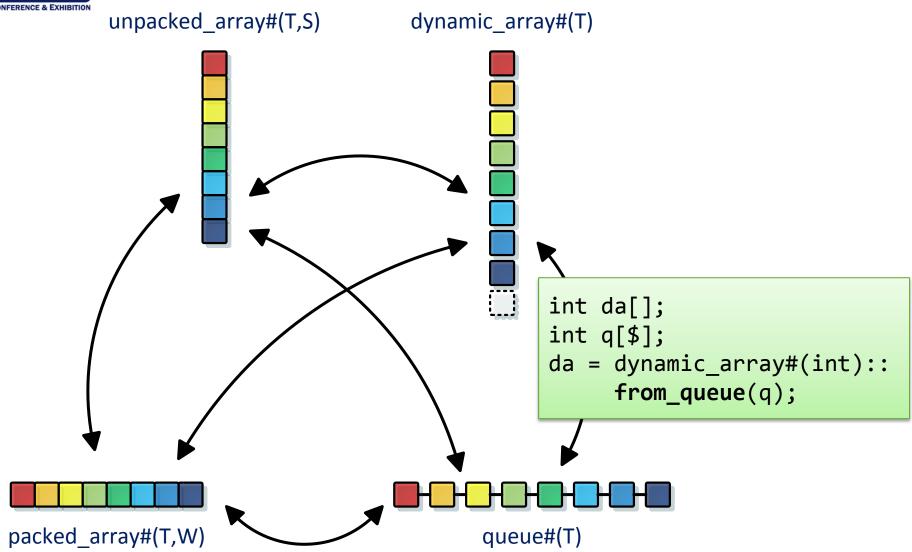


#### Aggregate classes

- Provides utility functions for:
  - Packed Array
  - Unpacked Array
  - Dynamic Array
  - Queue
  - Data Stream
  - Bit Stream



#### Array converters

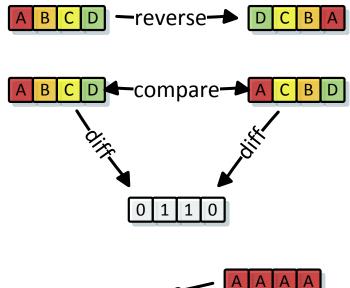


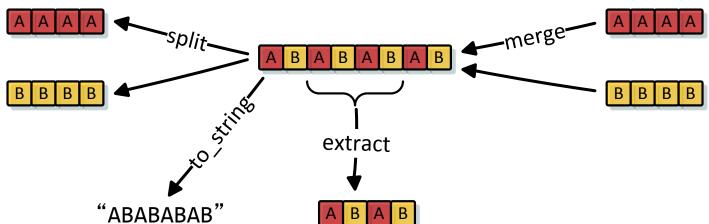


### What can you do with the array functions?

Most aggregate classes support these functions.









### My favorite functions: to\_string

```
bit[7:0] ds[]; // data stream
ds = new[16](
                                                                   33
  '{ 'h00, 'h11, 'h22, 'h33, 'h44, 'h55, 'h66, 'h77,
                                                                   44
     'h88, 'h99, 'hAA, 'hBB, 'hCC, 'hDD, 'hEE, 'hFF });
                                                                   55
$display( data_stream#(bit,8)::to_string(
  ds, .group(2), .num_head(4), .num_tail(6)));
                  :: - keisuke@devo: ~/Dropbox/dev/github/cluelib
                                                                   88
                                                                   99
                                                                   AA
                                                                   BB
   ... can
                    0011 2233 ... aabb ccdd eeff
 display a
part of the
data stream
```

ds[]

00

11

22

66

77

CC

DD

EE



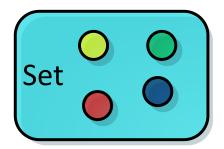
#### And to\_string\_with\_en

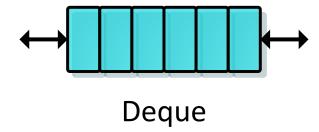
... displays enabled data only

```
de[]
ds[]
66
88
BB
```

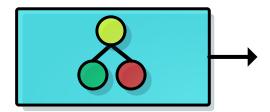


### Collections

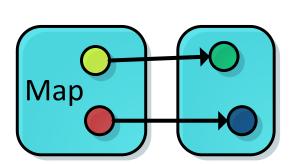


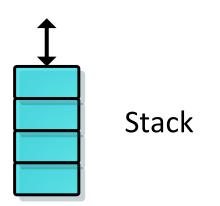






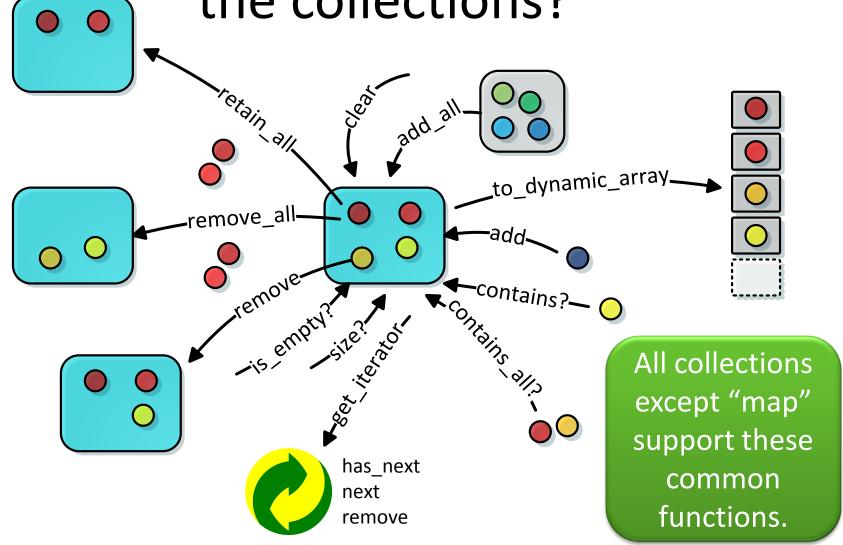
**Priority Queue** 







What can you do with the collections?





#### **STRATEGY**



# Strategy: A family of interchangeable algorithms

- Comparators
  - Example: pair\_comparator

```
class pair_comparator#(type T=pair) extends comparator#(T);
  virtual function bit eq( T x, T y );
   return x.first == y.first && x.second == y.second;
  endfunction
// ... other functions
  endclass
first
// /second
// ...
```

- Formatters
  - Converts an object to a string format



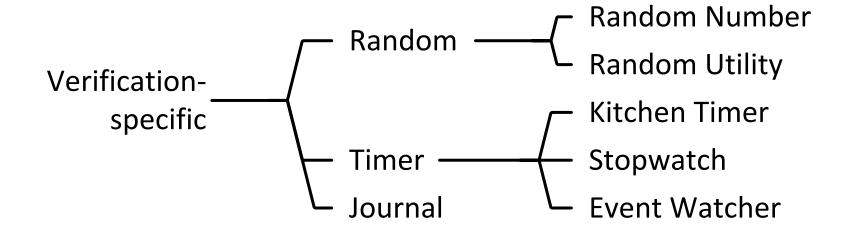
### My favorite class: comma\_formatter#(T)

```
comma_formatter#(longint) com_fmtr =
comma_formatter#(longint)::get_instance();

$display( com_fmtr.to_string( 123456789 ) );
```

... inserts commas as thousands separators





#### **VERIFICATION-SPECIFIC**



### What can you do with the random classes?

**Distribution Bin** 

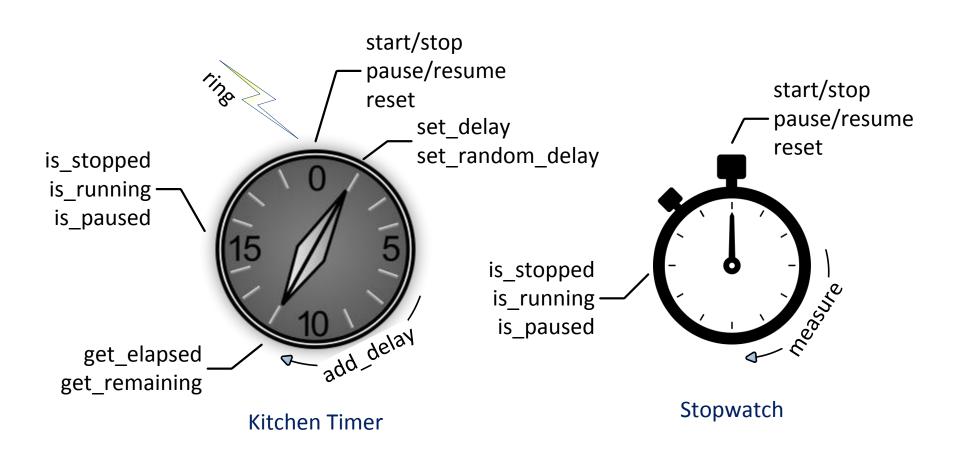
min	max	weight
100	200	1
300	400	2
500	600	3
700	800	4

Classes with 2, 4, 8, 16, and 32 distribution bins are defined.

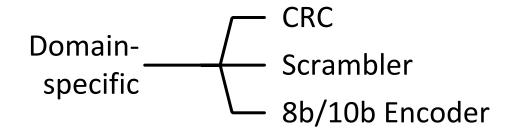
```
if ( random_util::random_bool(70) ) begin // 70% true
```



### What can do you with the timers?







#### **DOMAIN-SPECIFIC**



#### Domain-specific

- Offers utility functions to a specific target domain, which are generic enough to reuse
  - CRC
    - 42 commonly used CRC functions
  - Scramble
    - 18 commonly used scramblers
  - 8b/10b Encoder
  - (Color converters)
  - (Matrix functions)



#### Package and license

Using the package

```
import cl::*; // wildcard import
int i = choice#(int)::min(j,k);

// using the scope resolution operator
int i = cl::choice#(int)::min(j,k);
```

MIT License



#### API document

#### to\_queue

static Converts a dynamic array of type T to a queue of the same type.

#### **Arguments**

da A dynamic array to be converted.

reverse optional If 0, the element at the index 0 of da is positioned to the index 0 of the queue. If 1, the elements are positioned in the reverse order. The default is 0.

#### Returns

A queue converted from da.

#### **Examples**

```
bit da[] = new[8]( '{ 0, 0, 0, 1, 1, 0, 1, 1 } );
bit q[$];

q = dynamic_array#(bit)::to_queue( da );
assert( q == '{ 0, 0, 0, 1, 1, 0, 1, 1 } );

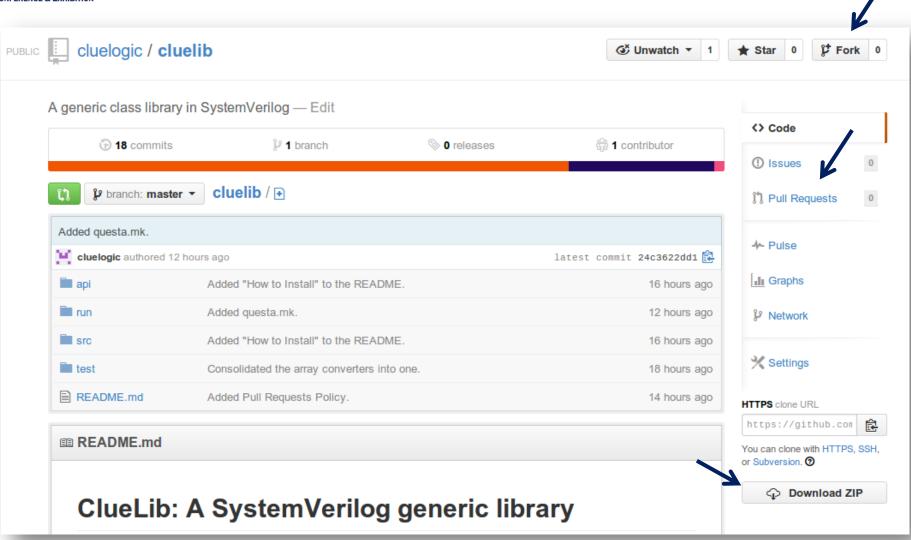
q = dynamic_array#(bit)::to_queue( da, .reverse( 1 ) );
assert( q == '{ 1, 1, 0, 1, 1, 0, 0, 0 } );
```

#### See Also

da\_to\_q



### Social coding with GitHub





#### **CASE STUDY**



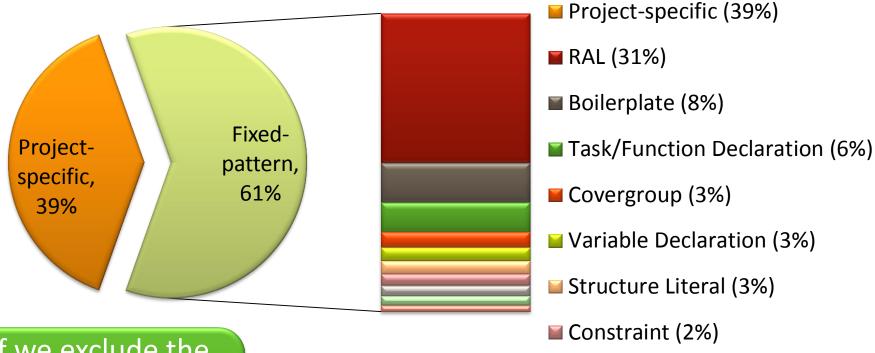
# How much code could be replaced by the library?

- Investigated nine projects
  - A total of 489,875 lines of class-based code (no module-based code or comments)
- About 2% of code could be replaced by the library

This result fell short of our expectations.



### What did the other 98% of the code consist of?



If we exclude the fixed-pattern code, the reduction rate rose to 5%.

- Compiler Directive (2%)
- Interface (2%)
- **■** Typedef (1%)



# Are there any limitations of the library?

- Some functions are probably infeasible to develop in SystemVerilog
  - regular-expressions, image processing, parsing JSON, etc.



# What are the disadvantages of an open-source project?

- "Most free software projects fail" [Fogel, '05]
  - New sets of complexities, such as deploying a web site, documentation, and managing contributors
- Verification libraries are usually developed using an employer's resources

 The copyright of such libraries belongs to the employer

To avoid potential lawsuits, we will not accept any "pull requests" from individual contributors.



#### What next?

- UVM-dependent library
  - Extension of uvm\_tlm\_generic\_payload
  - uvm\_event waiter
  - report\_phase that collects the simulation statistics

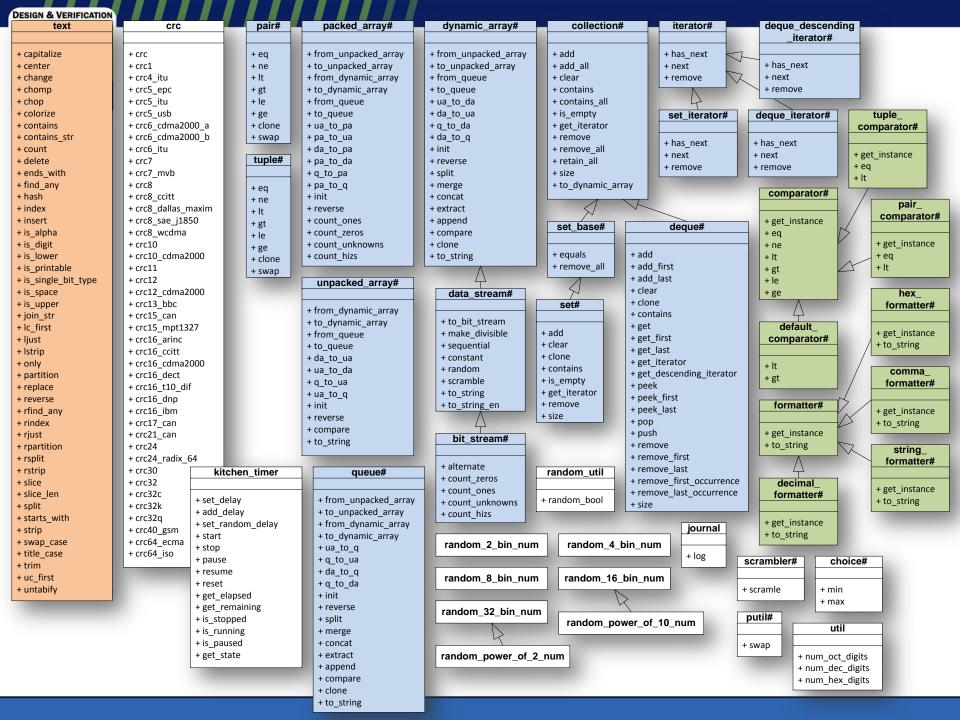


# Is coding in SystemVerilog fun again?

- Absolutely!
- "batteries included"
  - 360+ functions
- Fork me on GitHub
  - https://github.com/cluelogic/cluelib



#### **BACKUP SLIDES**





#### SystemVerilog only

... uses a for loop to find a match

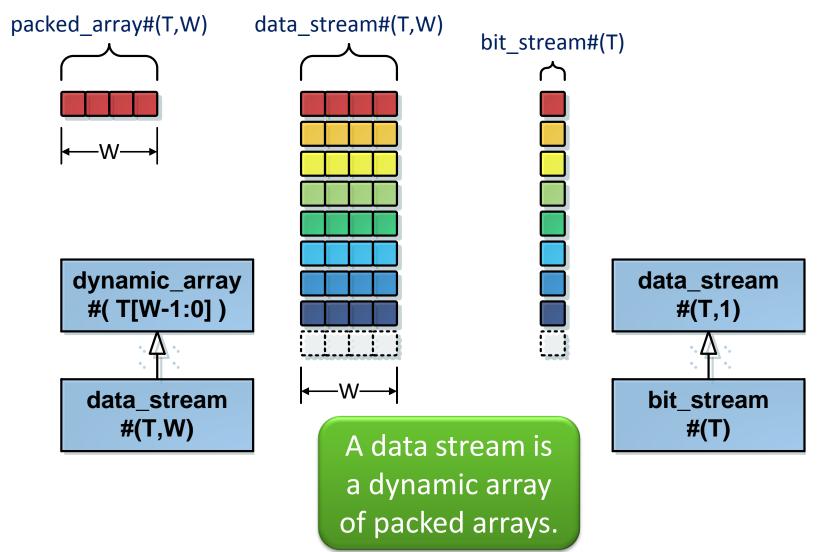


#### SystemVerilog with C++

... delegates the search to the "find" function of C++



#### Data stream and bit stream





### What can you do with the data stream?

