

Terrestrial Verification Methodology

A “Down-To-Earth” Approach to Developing UVM VIPs

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Canada



Agenda

- Patterns, Patterns... everywhere
- Façade Pattern
- Façade : 'Terrestrial' Verification Methodology (TVM)
- Future Work...
- Q&A

I'm a big fan of...



Design Patterns

Pattern	.. Huh?
Factory	Dynamically change classes instantiated
Callback	Add functionality via hooks
State	Finite State Machine (dynamic)
Chain of Responsibility	Handles sequence of transformations
Command	Dynamically change behaviour

This Year's Pattern *du Jour*?

Façade

Façade

Wikipedia Definition:

A **façade** ([/fə'sɑ:d/](#))^[1] is generally one exterior side of a building, usually, but not always, the front.

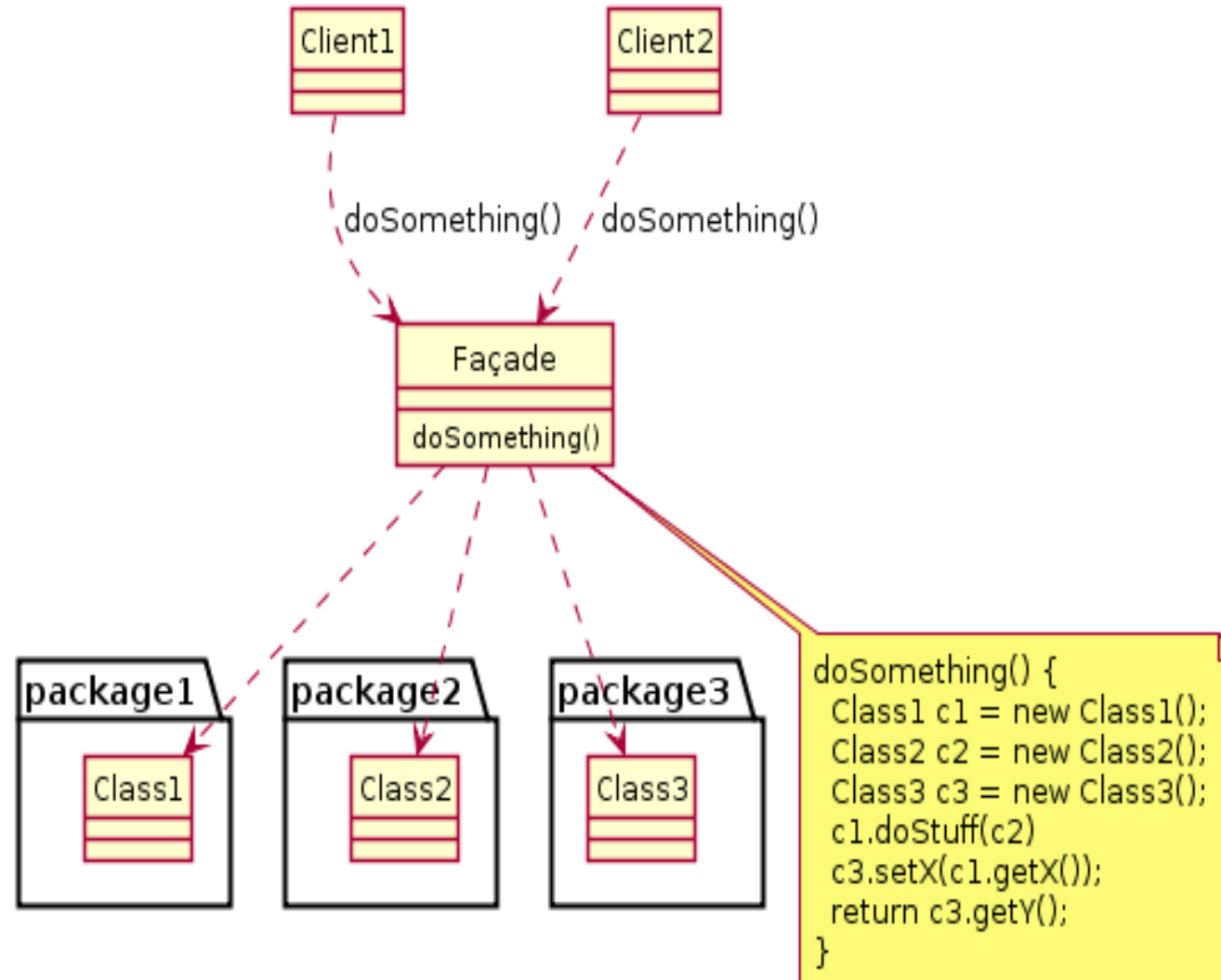
In architecture, the façade of a building is often the **most important aspect from a design standpoint**, as it sets the tone for the rest of the building

Façade Pattern

Goal:

Adds a simplifying front-end for multiple collaborating classes

Façade Pattern



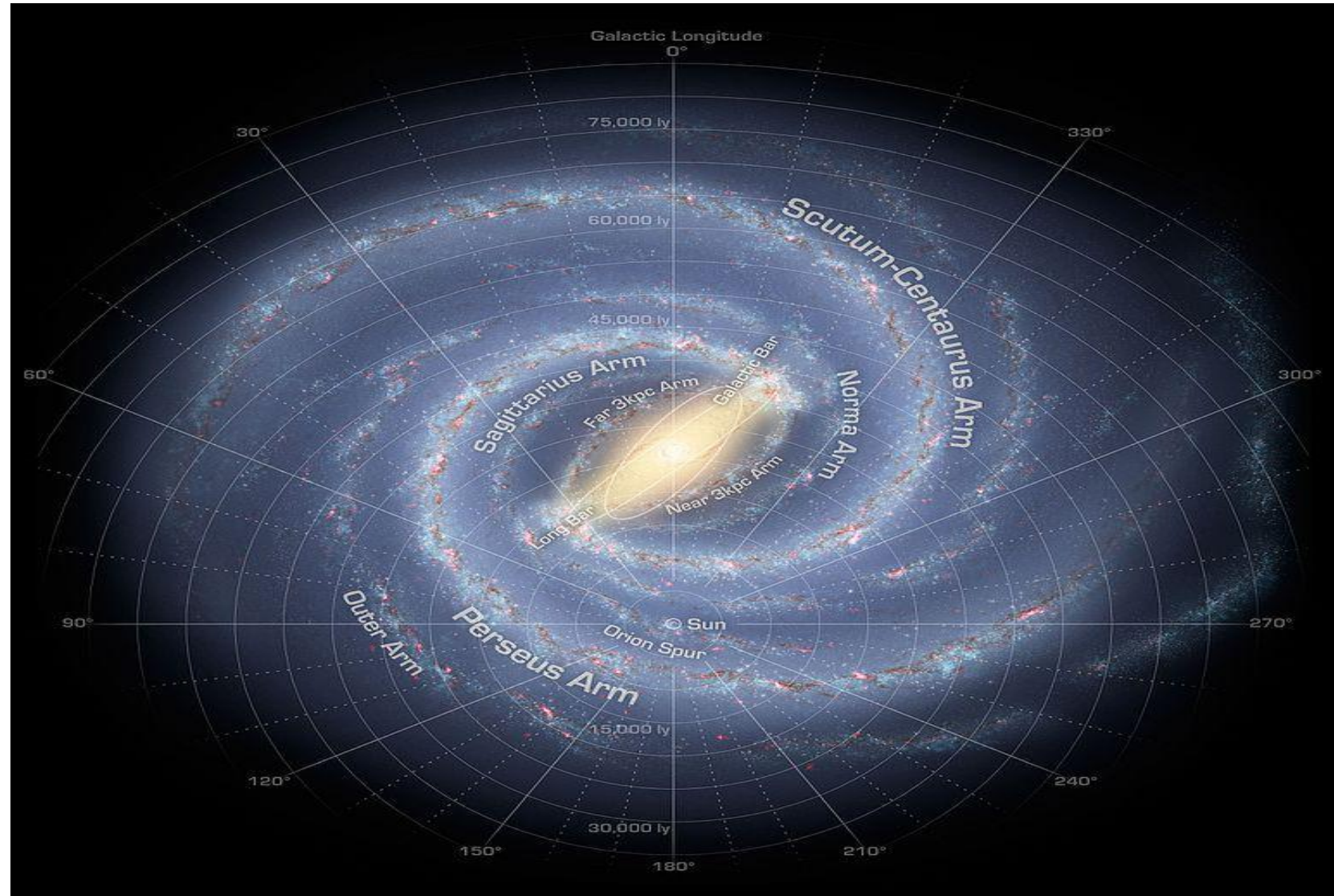
Terrestrial Verification Methodology

Application of Façade Pattern

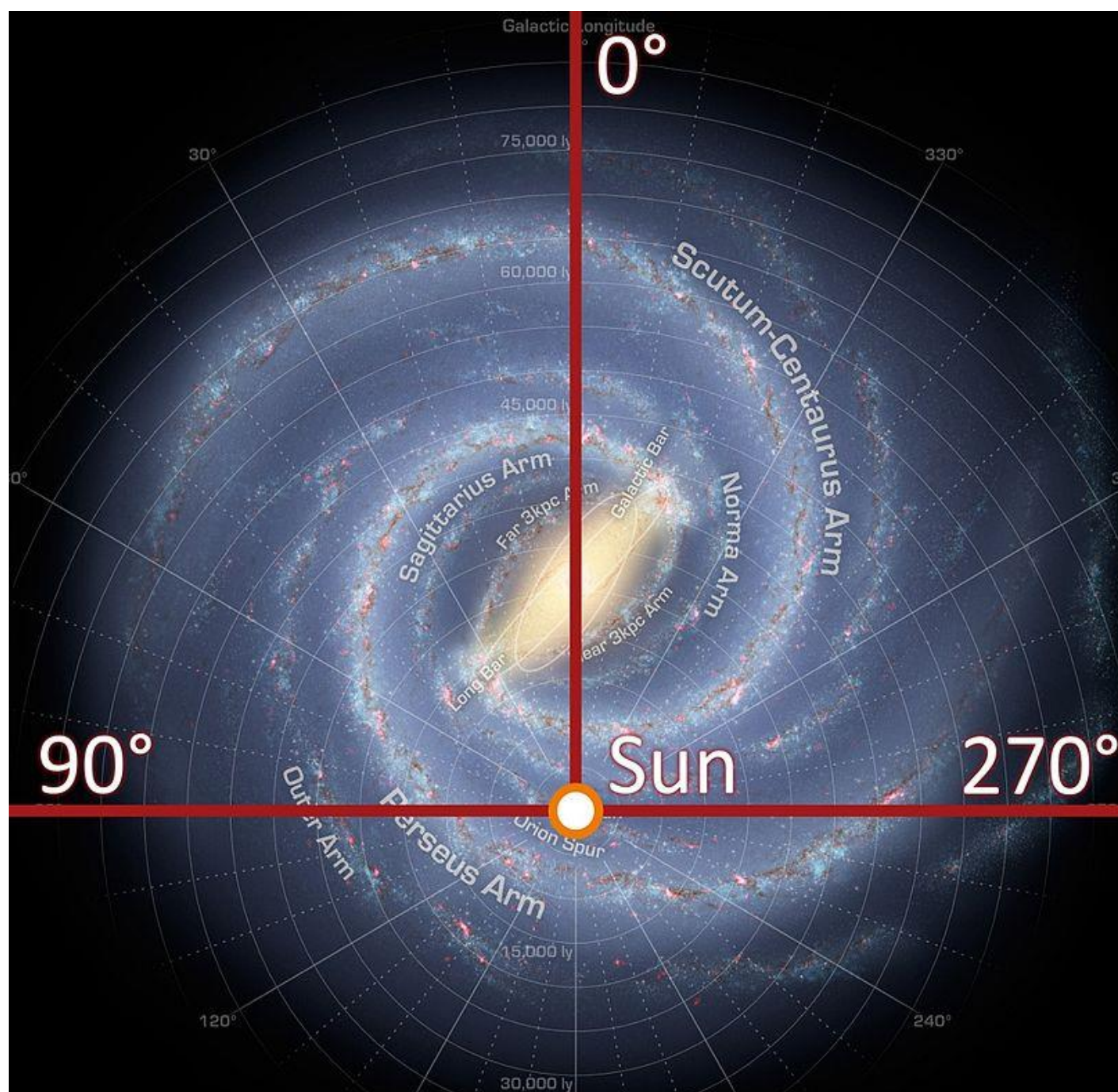
Universal

Verification Methodology

I've *never*
said that the
name was
pretentious...
nope, not me.



Now...



ciena.
Experience. Outcomes.

snug
Synopsis Users Group
Canada

Terrestrial

Verification Methodology



It's goals are
a little more
*down to
earth.*

Someone needs to...

What About UVM?

From a slide-deck
presentation on
PSS

■ The Bad

- Non DV & Designer Engineers are not familiar with System Verilog & UVM
- Overly complicated and hard to debug
- Need to be an expert in UVM to create a simple directed test

Someone needs to... look up the word:

What About UVM?

- Excellent for Block/IP Level Verification,
 - Does not scale to System Level Verification, Only Solves “Checking” Portability Problem

Someone needs to... look up the word:
“irony”

What About UVM?

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Engineering needs.



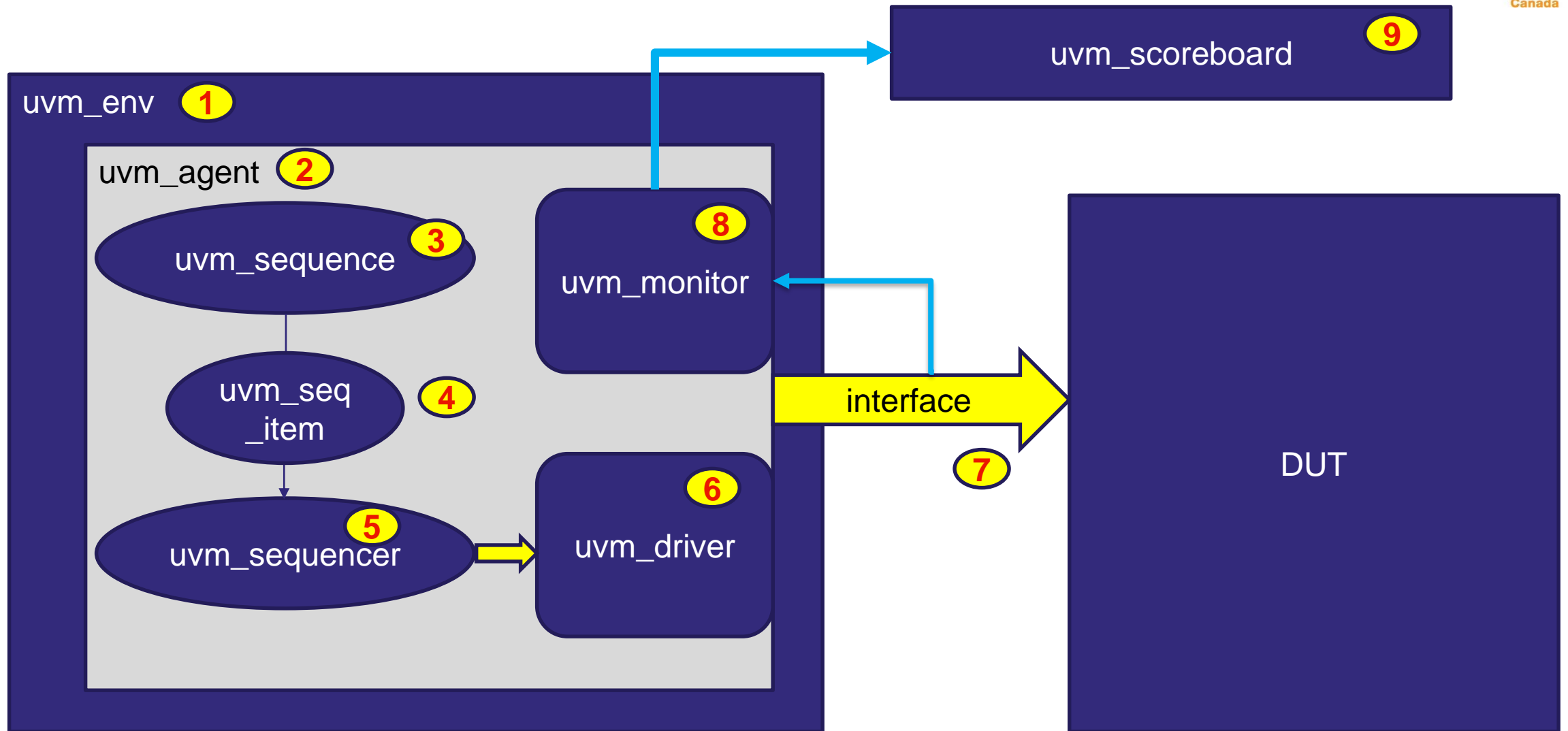
Terrestrial Verification Methodology (TVM)

Goal

Simplify the use-case for an agent's driver, monitor and scoreboard.

... intended for *simple* agents

Usual UVM Sequence Item Flow



Sorry...

... my head just exploded



Do we *really* need...

NINE collaborating classes???

Uh...well... *actually*....

YES.

Why? SOLID

- S Single Responsibility Principle
- O Open/Closed Principle
- L Liskov Substitution Principle
- I Interface Segregation Principle
- D Dependency Inversion Principle

Class should have
only a single

Open for extension; y

Replaceable with

Many specific
interfaces are better
than 1 general

Depend on
abstractions, not
concretions

UVM

Encourages adherence to the SOLID principles.

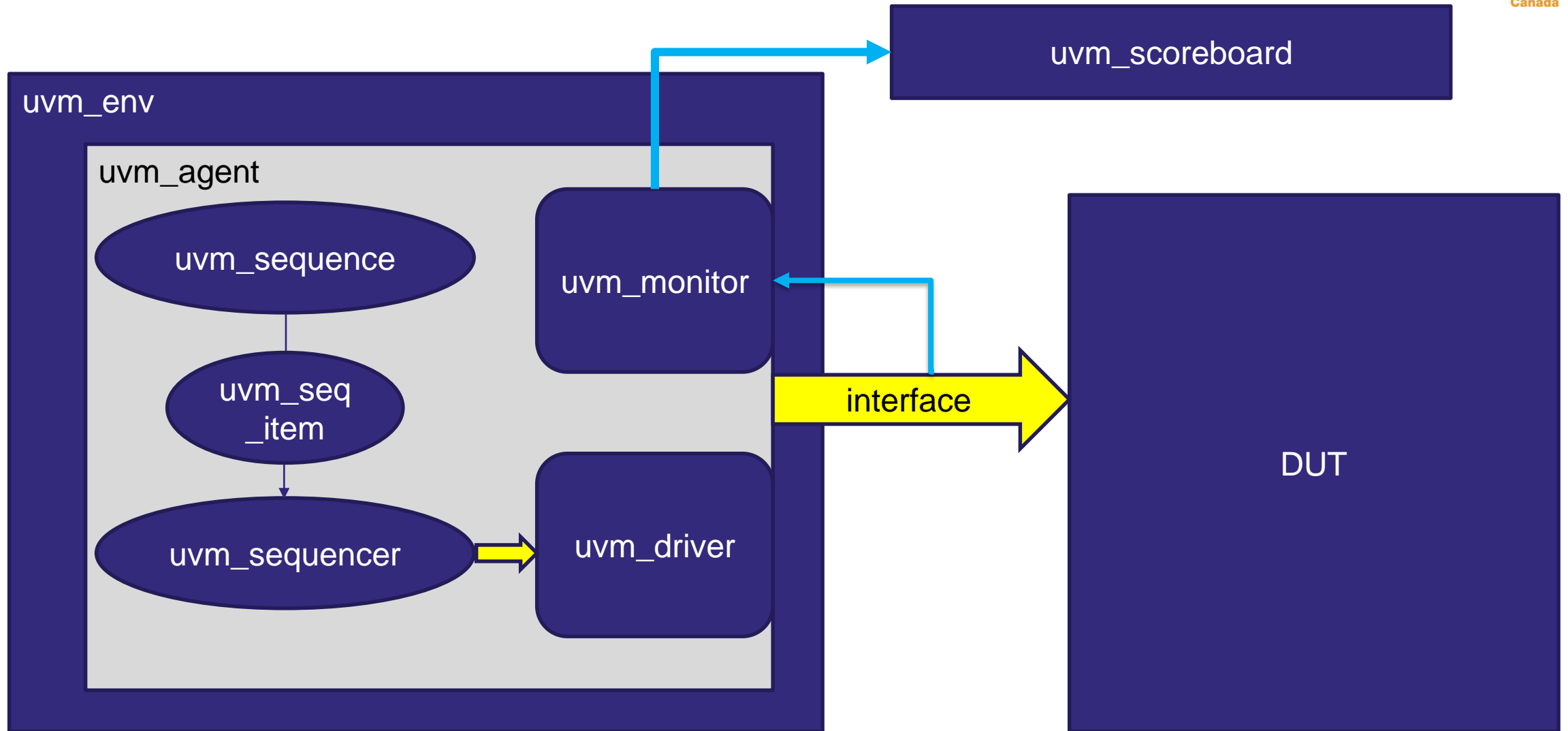
- S** each class is responsible for one thing
- O** inheritance
- L** Factory Pattern
- I** API in each is consistent
- D** encourages abstraction

But *sometimes* you just want it to be simpler...

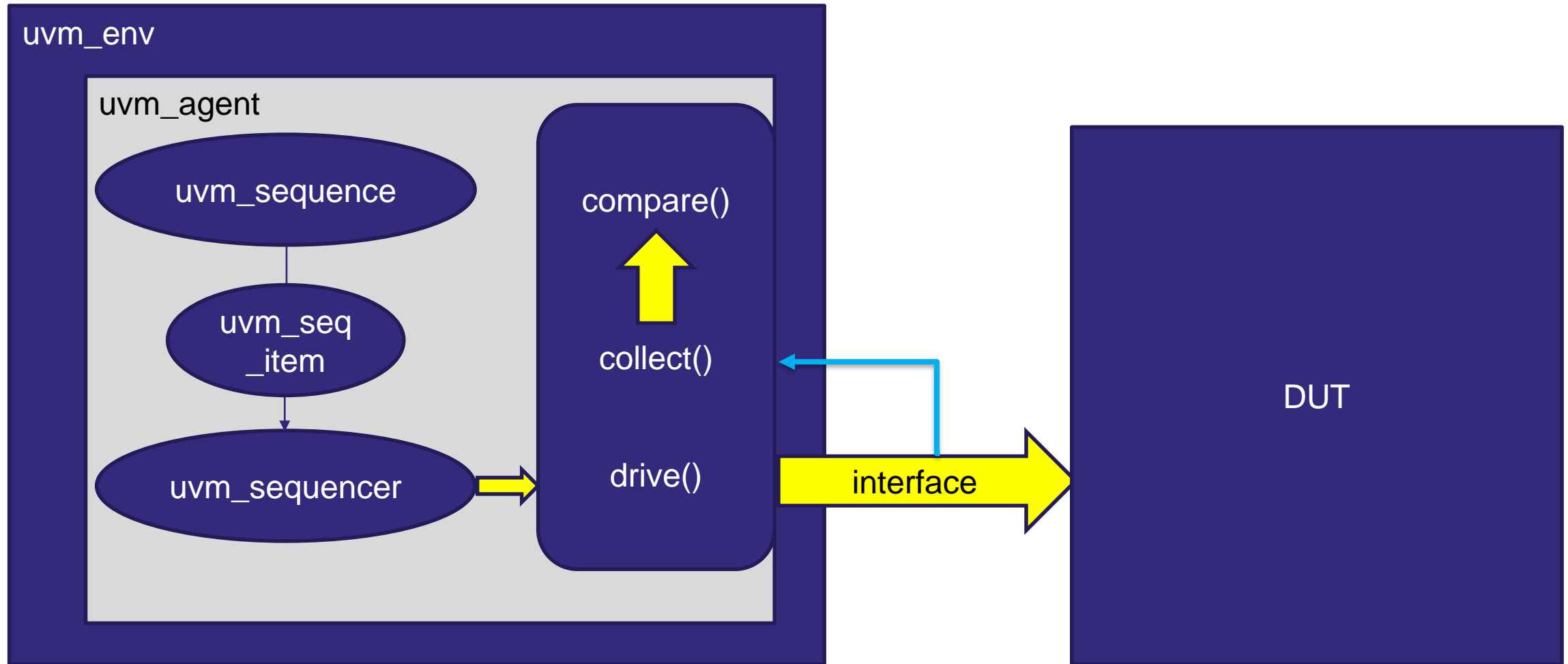
Use cases:

- Simple VIPs that will likely not change: proprietary serial interfaces
- Simple agent for RTL unit testing

Usual UVM Sequence Item *Flow*

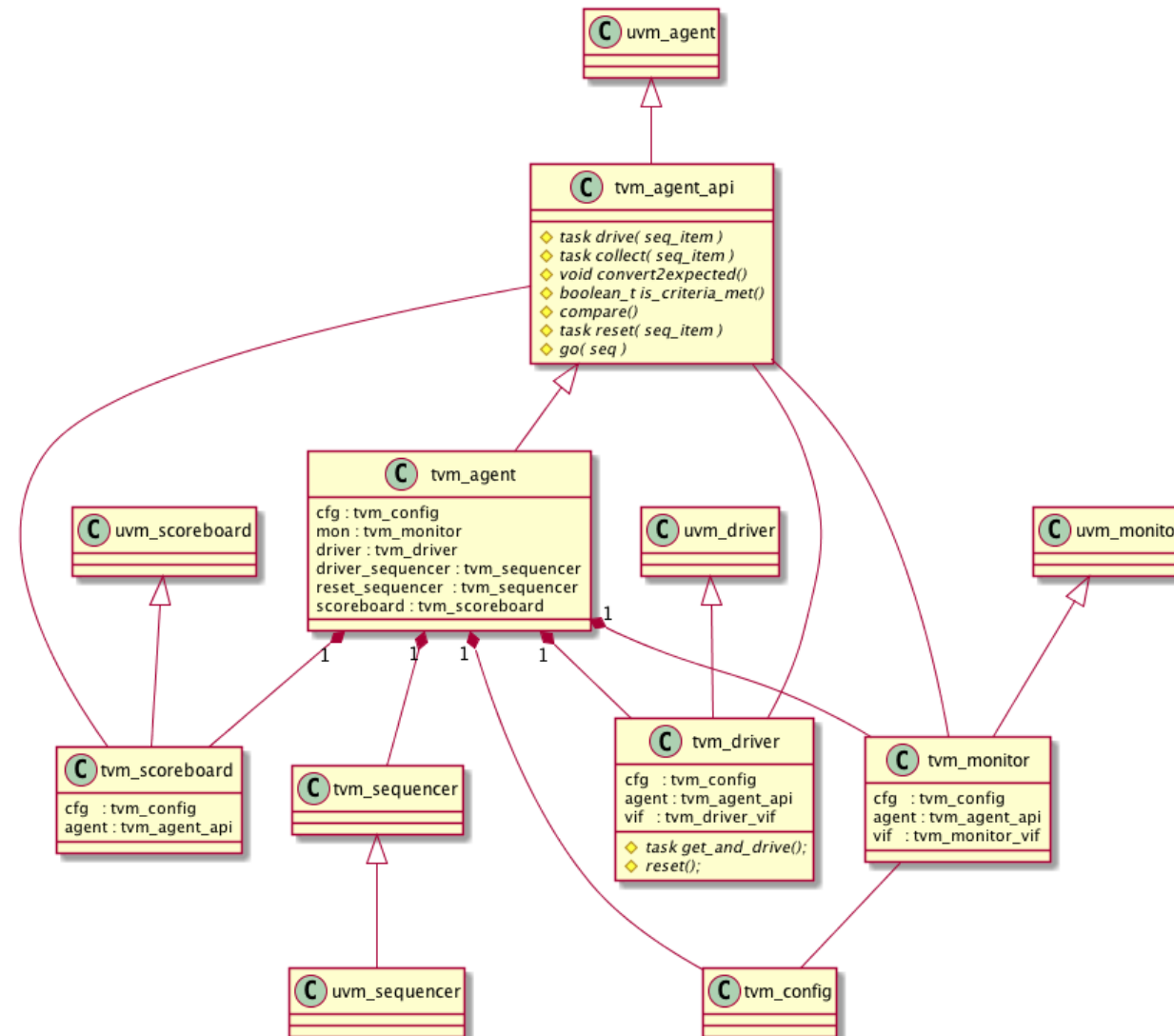


TVM: *Globbering* driving, monitoring & scoreboarding



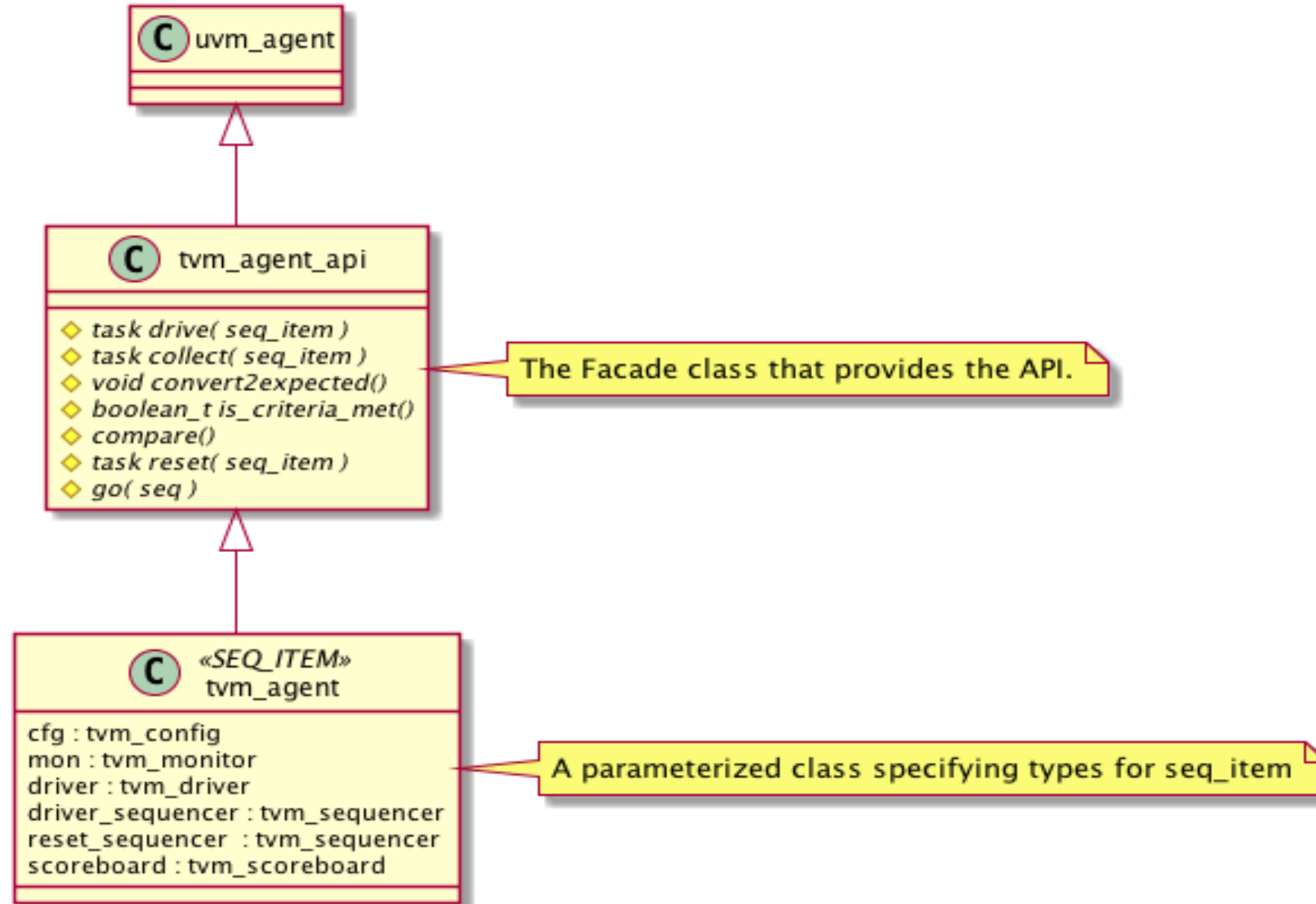
TVM : Entire Class UML Eye-Chart

Terrestrial Verification Methodology – Class Diagram



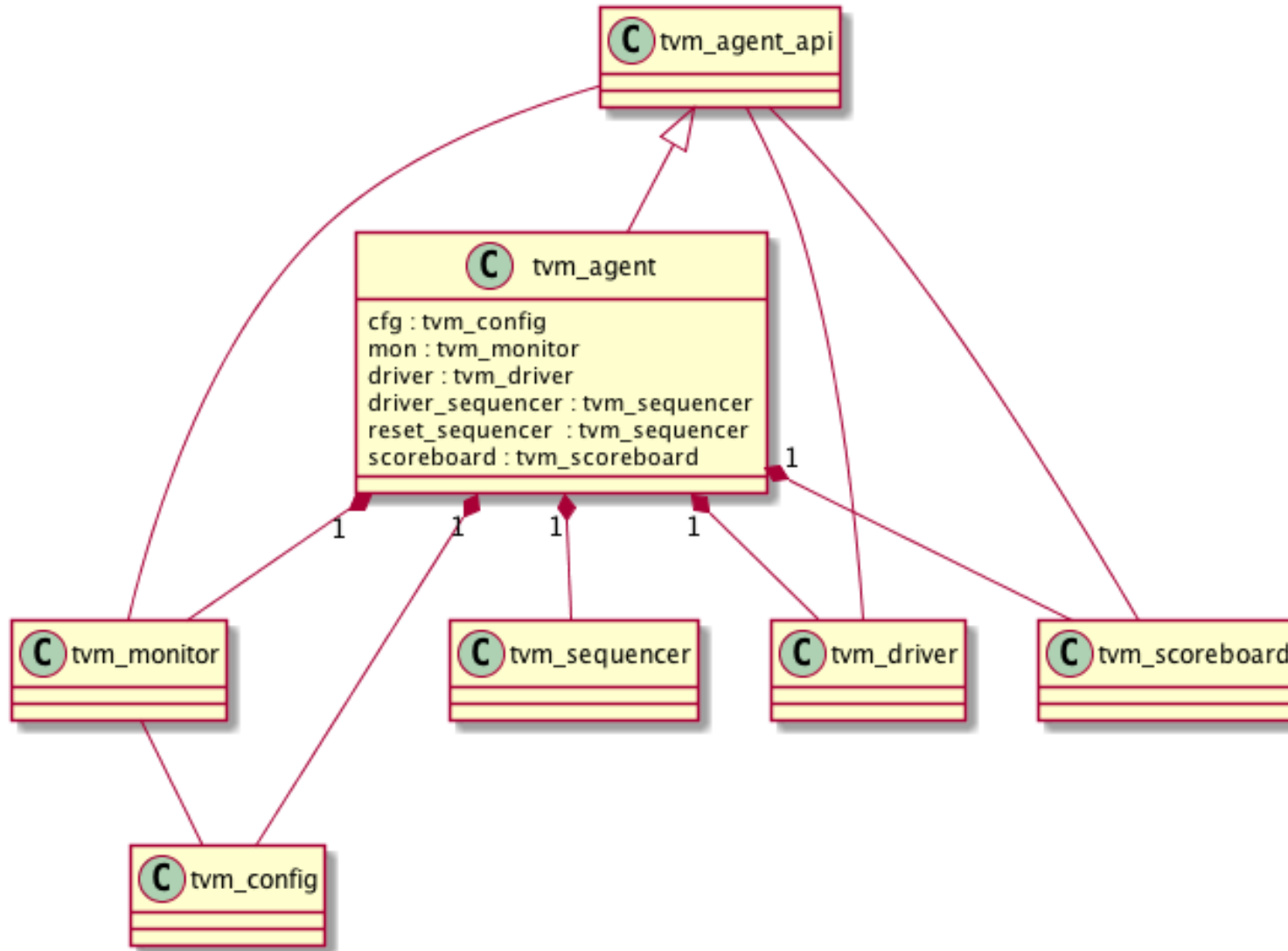
TVM : API – The Heart of It All

Terrestrial Verification Methodology – Class Diagram (Facade)



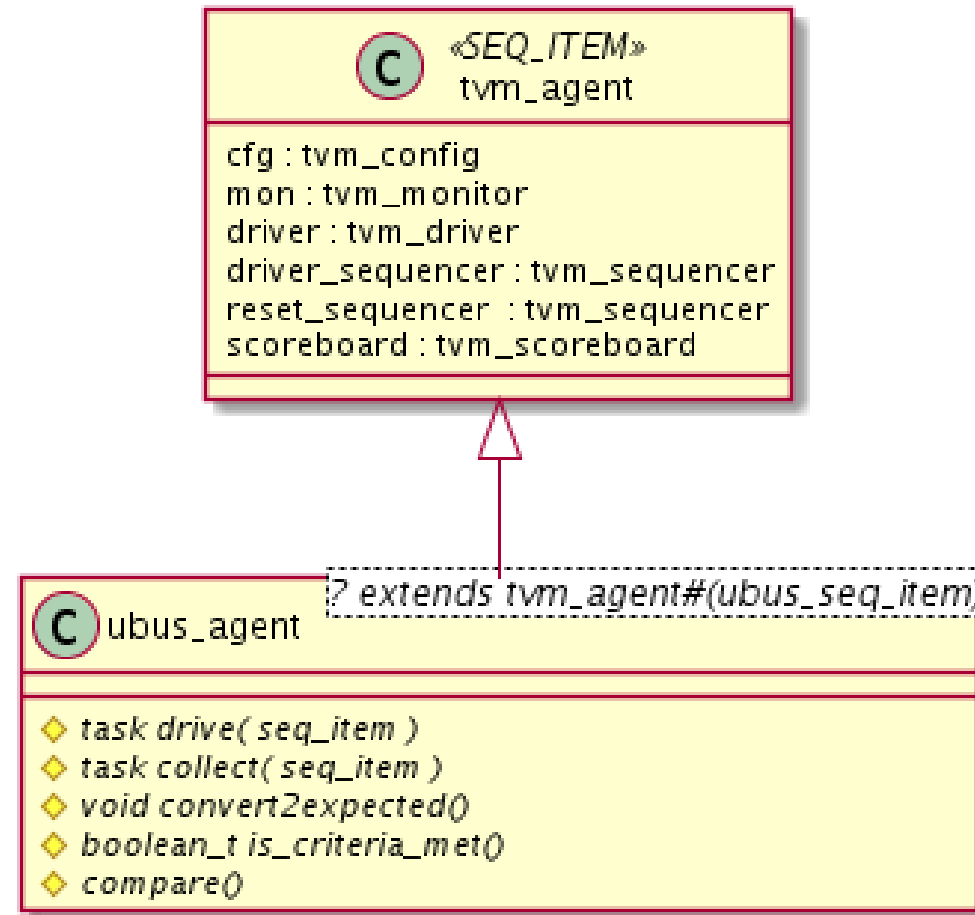
TVM Agent: If you build it they will come

Terrestrial Verification Methodology – tvm_agent Class Diagram



TVM Example: ubus_agent

Terrestrial Verification Methodology – ubus_agent Class Diagram



TVM Agent: Build and Connect

- Build phase:
 - Creates the underlying `tvm_driver`, `tvm_monitor`, `tvm_scoreboard`
- Connect phase:
 - Connects sequencer to driver
 - Connects monitor to scoreboard
 - etc.

TVM Agent: Incrementally Evolutionary



Evolutionary: Built on standard UVM classes

- Can use factory to swap in more complicated driver, monitor, scoreboard
- `tvm_scoreboard` has built-in in-order, HOL comparison
- Can derive `tvm_agent` (or any `tvm_*` class) from your company- or project-layer UVM class.

TVM Agent: Run Phase API

- Driver

drive

transfers a seq item (from your sequence) to pin wiggles

- Monitor

collect

collects pin wiggles and create a seq item, pushes it onto its analysis port

- Score board

convert2expected

aka predictor: accepts input seq item and converts to *expected* seq item

is_criteria_met

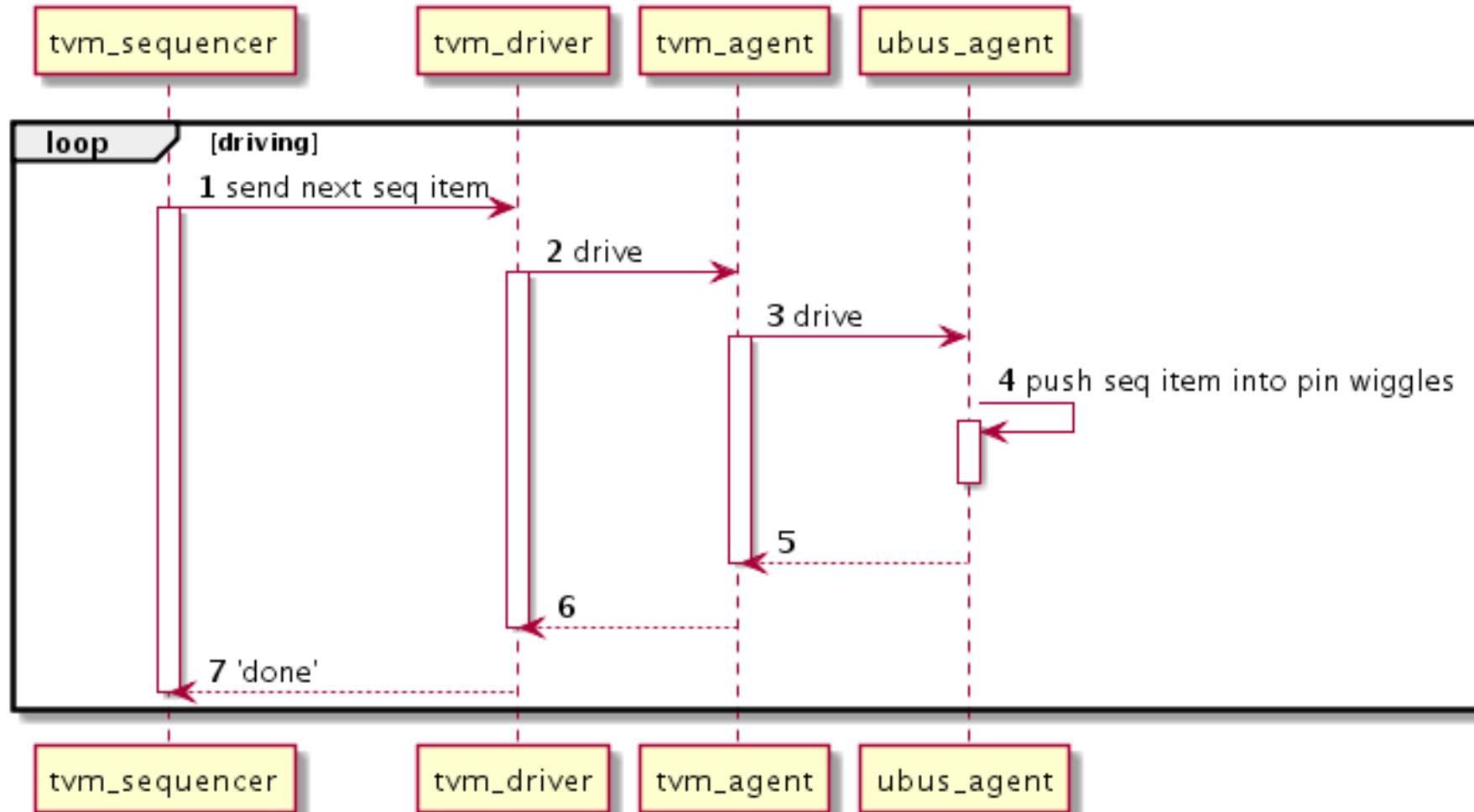
when *actual* seq item received, do you have everything you need to run the compare? e.g., Is there something in the *expected* q?

compare

does *actual* == *expected* (override if necessary)

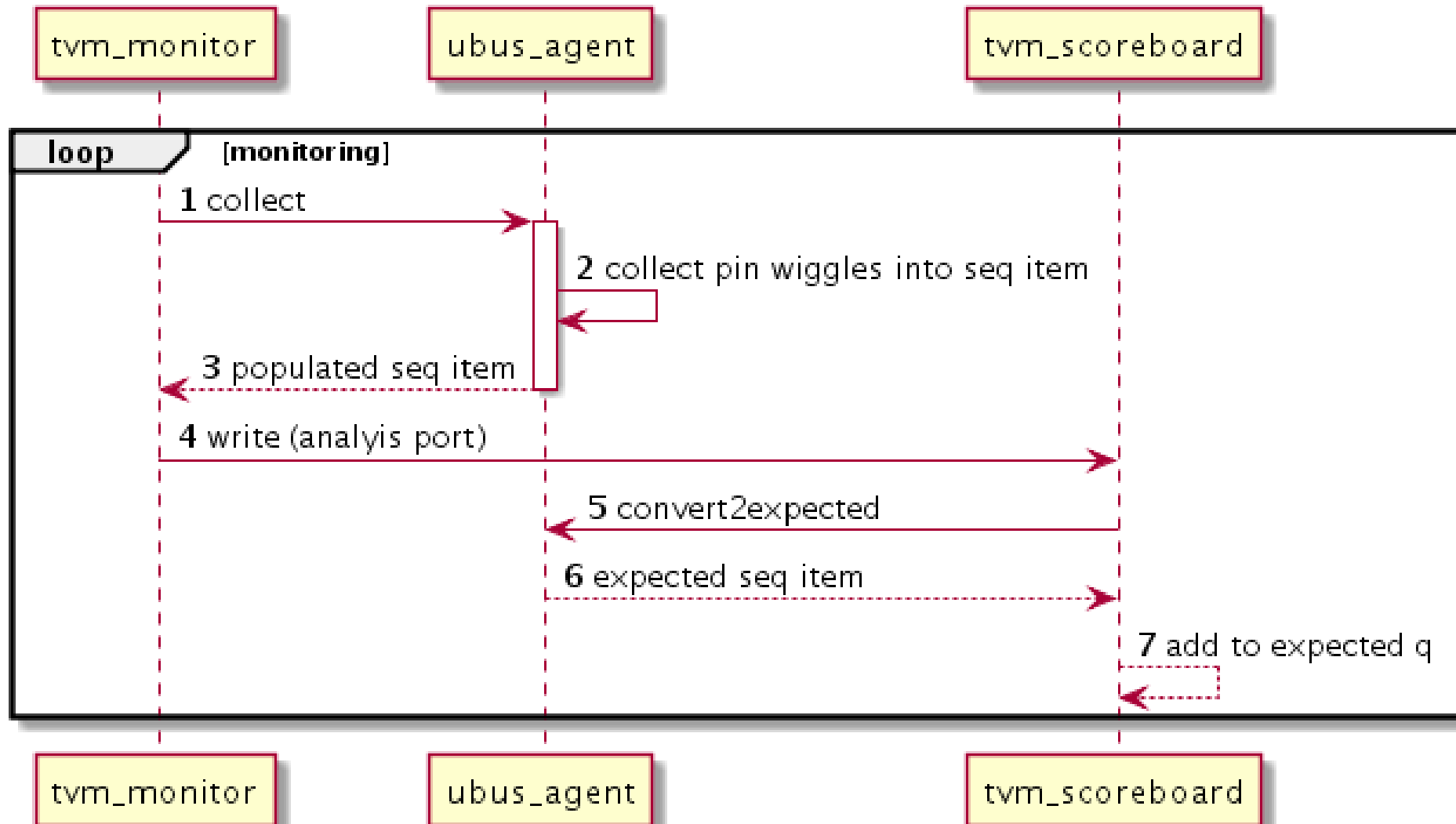
TVM : Driving

Terrestrial Verification Methodology – Sequence Diagram (Driving Phase)



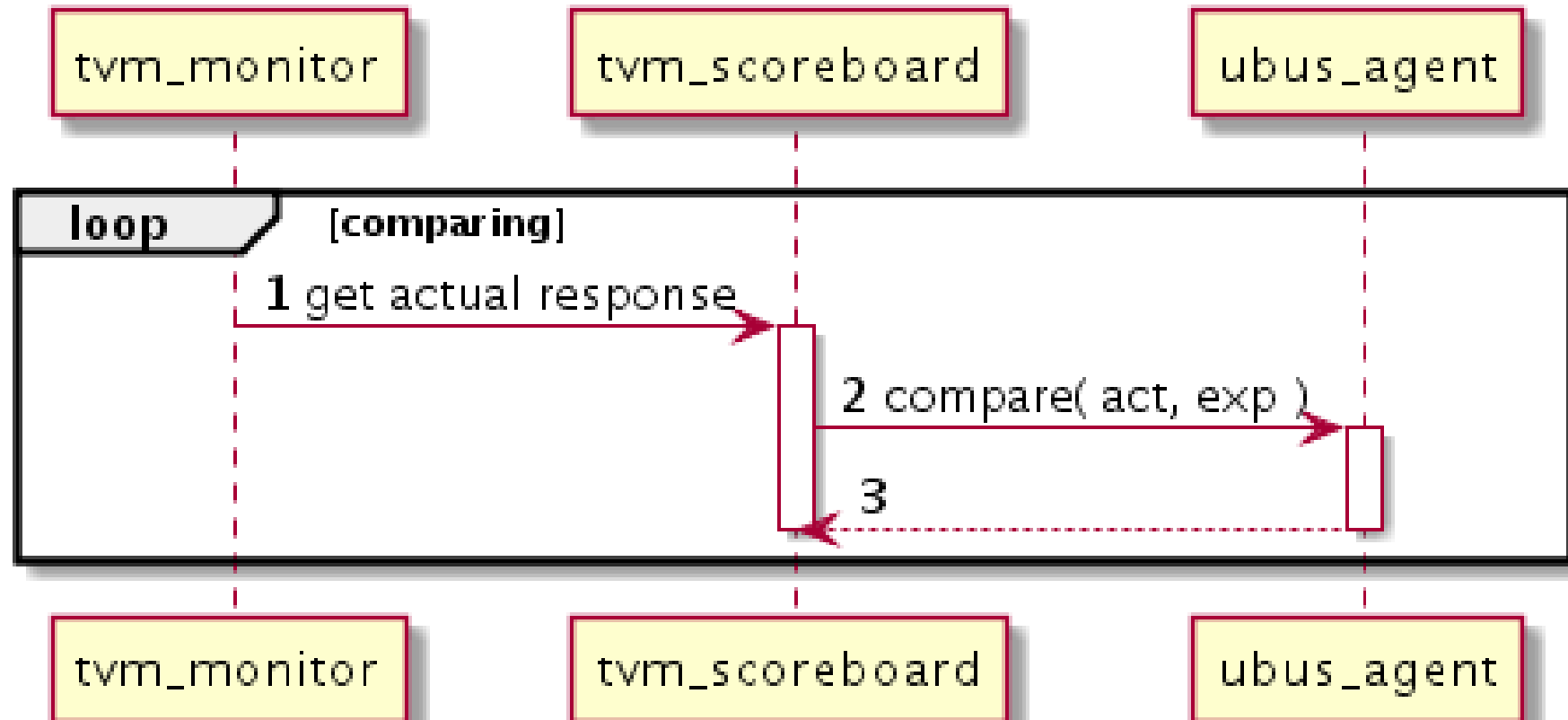
TVM : Monitoring

Terrestrial Verification Methodology - Sequence Diagram (Monitoring Phase)



TVM : Scoreboarding

Terrestrial Verification Methodology - Sequence Diagram (Comparing Phase)



Compare & Contrast: TVM vs UVM

UVM	TVM
Complicated (nine classes)	Less complicated (down to six...and counting)

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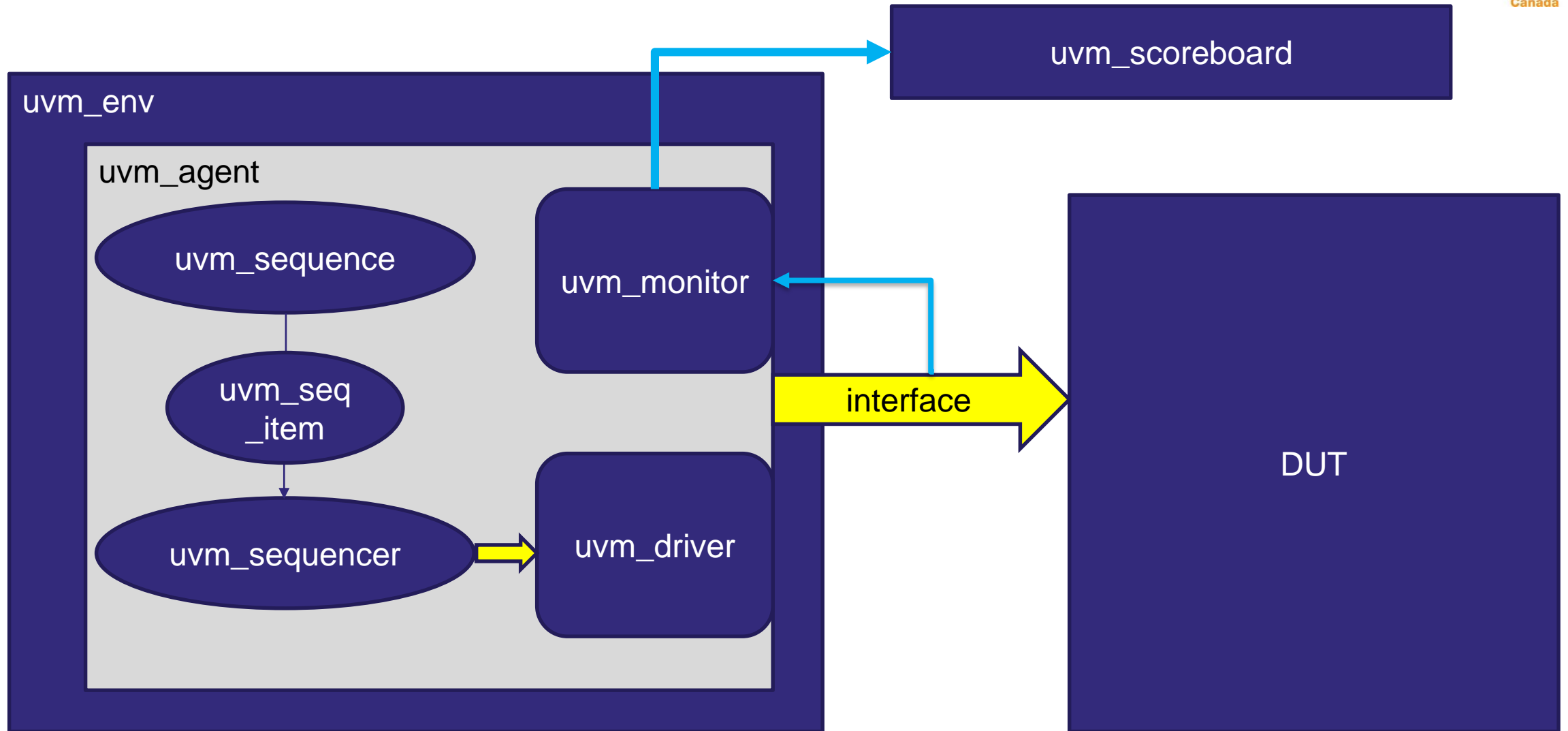
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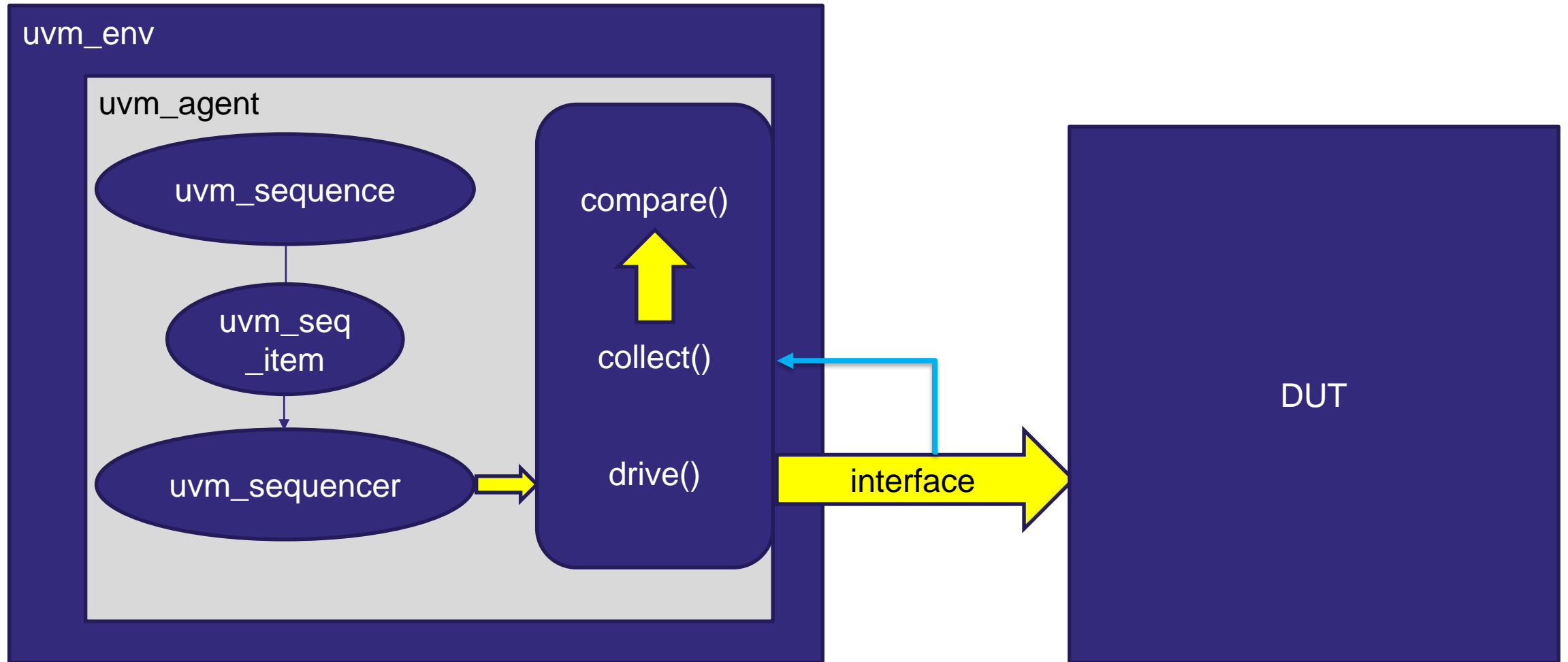
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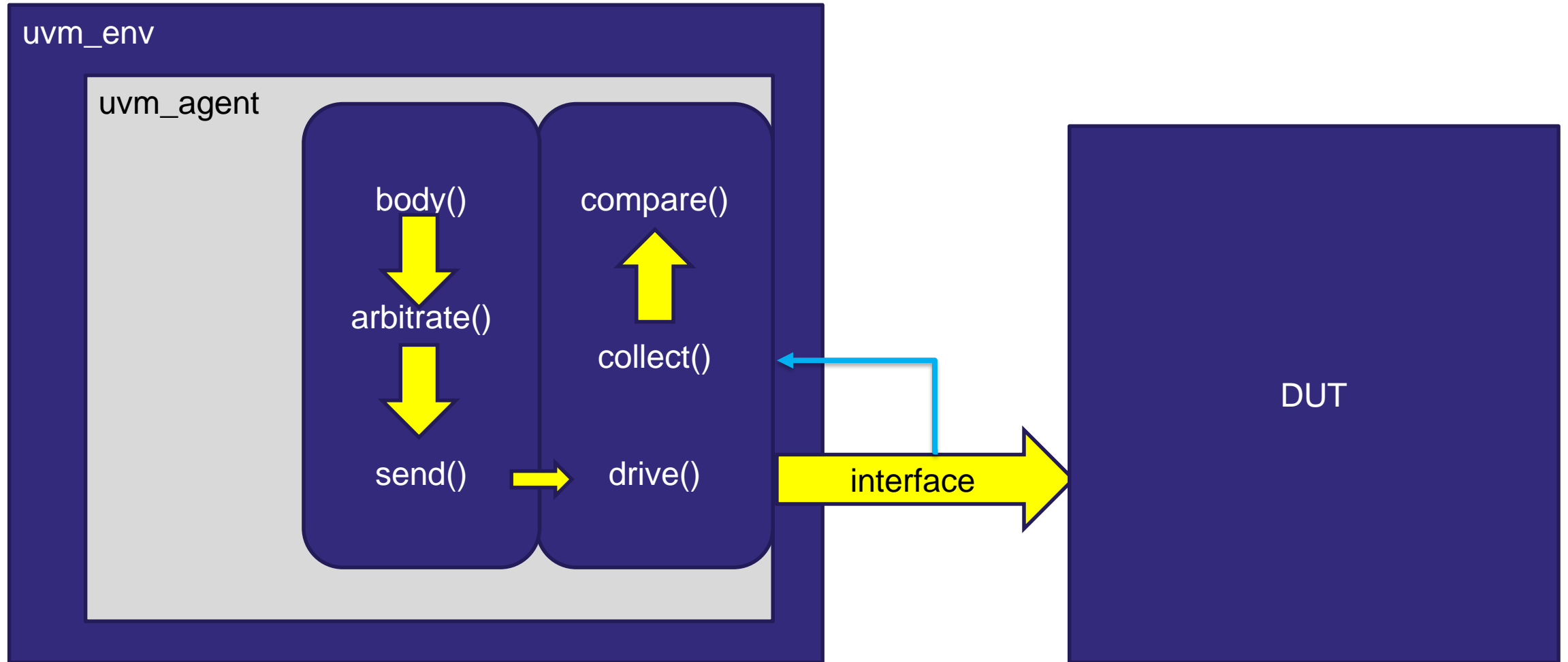
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Can be created from a company / project UVM layer	Yup. Ditto
Scale from Block to System.	It should... but if you probably want to create a complete UVM VIP at this point

UVM Now





TVM Future? *Globbing* seq_item gen



Conclusions

- Goal of the Presentation: describe Façade pattern
- Demonstrate Façade use-case with TVM
- TVM is at this point a “neat idea” (IMHO) that is still evolving

Thank You

.. and thanks to
Pierre Girodias and
Mike Thompson
for their help.



Q&A

We have time for nine questions.

