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Automated Integration of MathWorks® Simulink® Signal Flow Graph Models into Synopsys® Virtualizer™-based Virtual Prototypes

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Effektiv

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Agenda

The Application: Automotive Mixed-Signal ASICs

The Current Workflow and its Challenges

The Improved Workflow

Summary & Conclusion



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The Application

Automotive Mixed-Signal ASICs



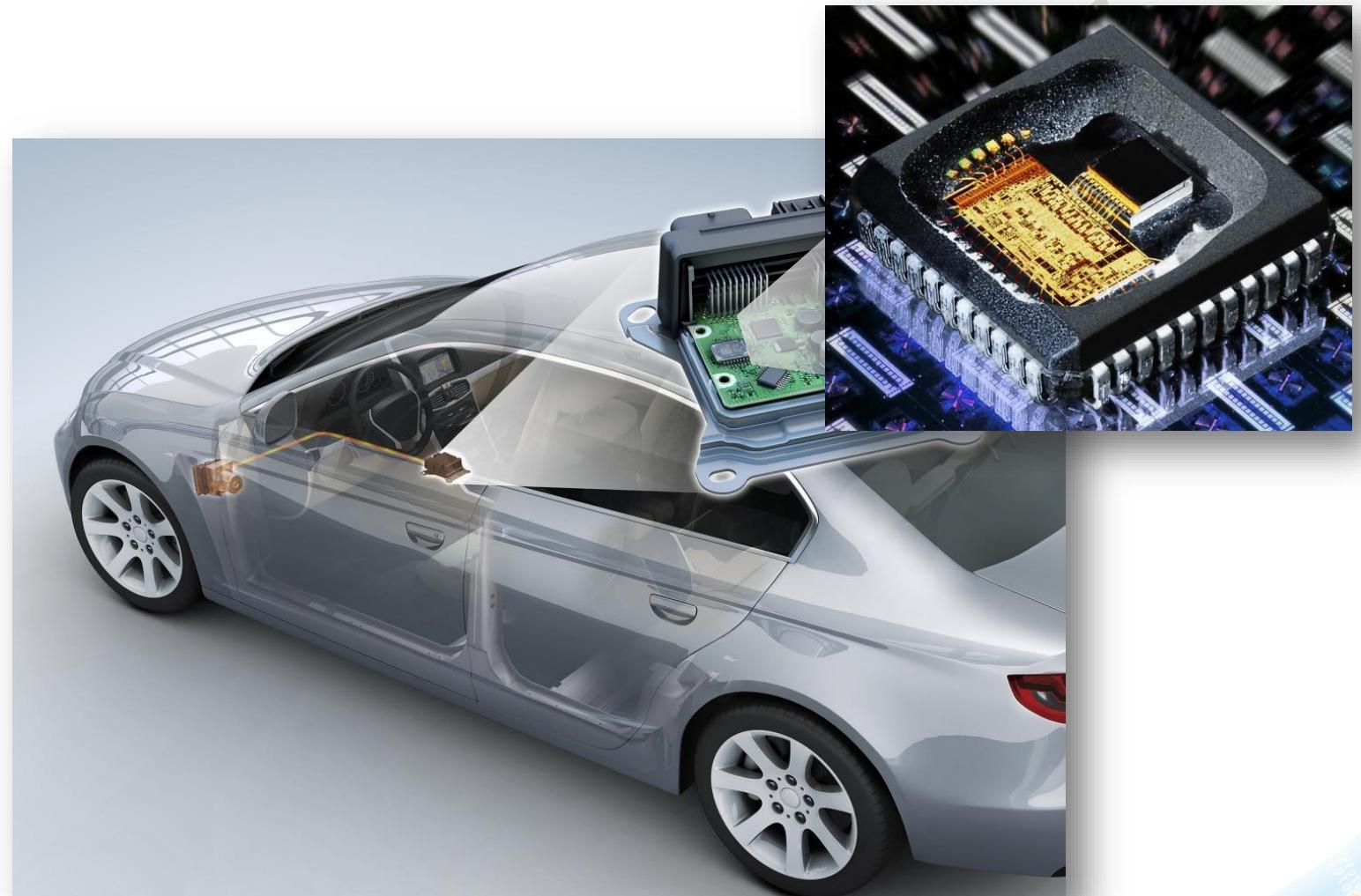
Automotive Mixed-Signal ASICs



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- Bosch accelerates progress of automotive technology with continued innovations like ESP or autonomous driving solutions
- Integral part for these solutions are automotive sensors
- Example: Inertial sensor system for ESP

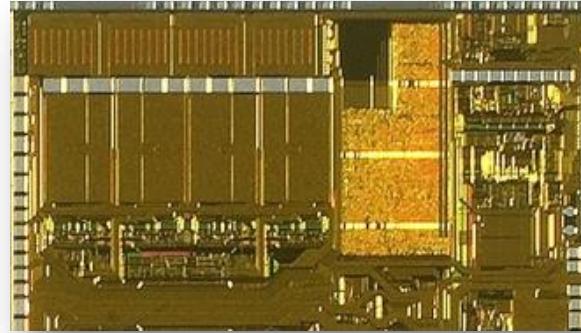


Automotive Mixed-Signal ASICs



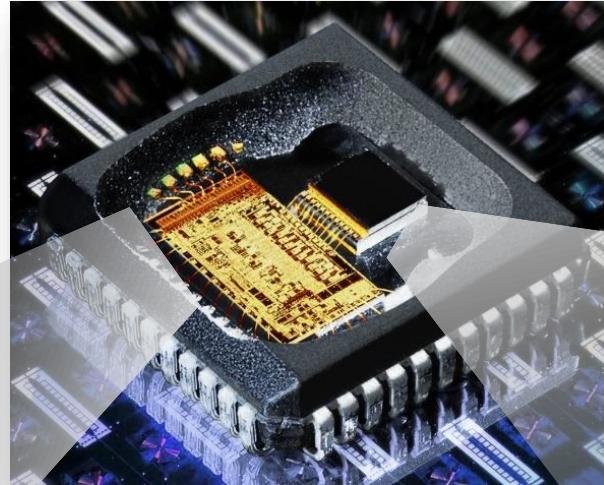
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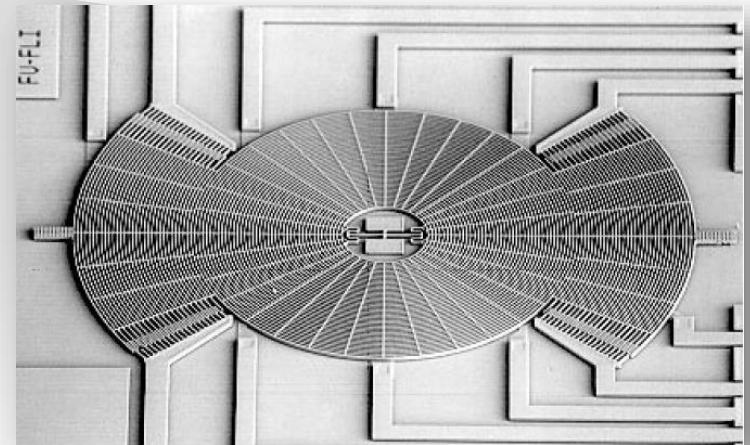


Heterogeneous SoC:

- Analog Hardware
- Digital Non-Programmable Hardware
- Processors



System-in-Package (SiP)



Sensor

Sensor ASIC

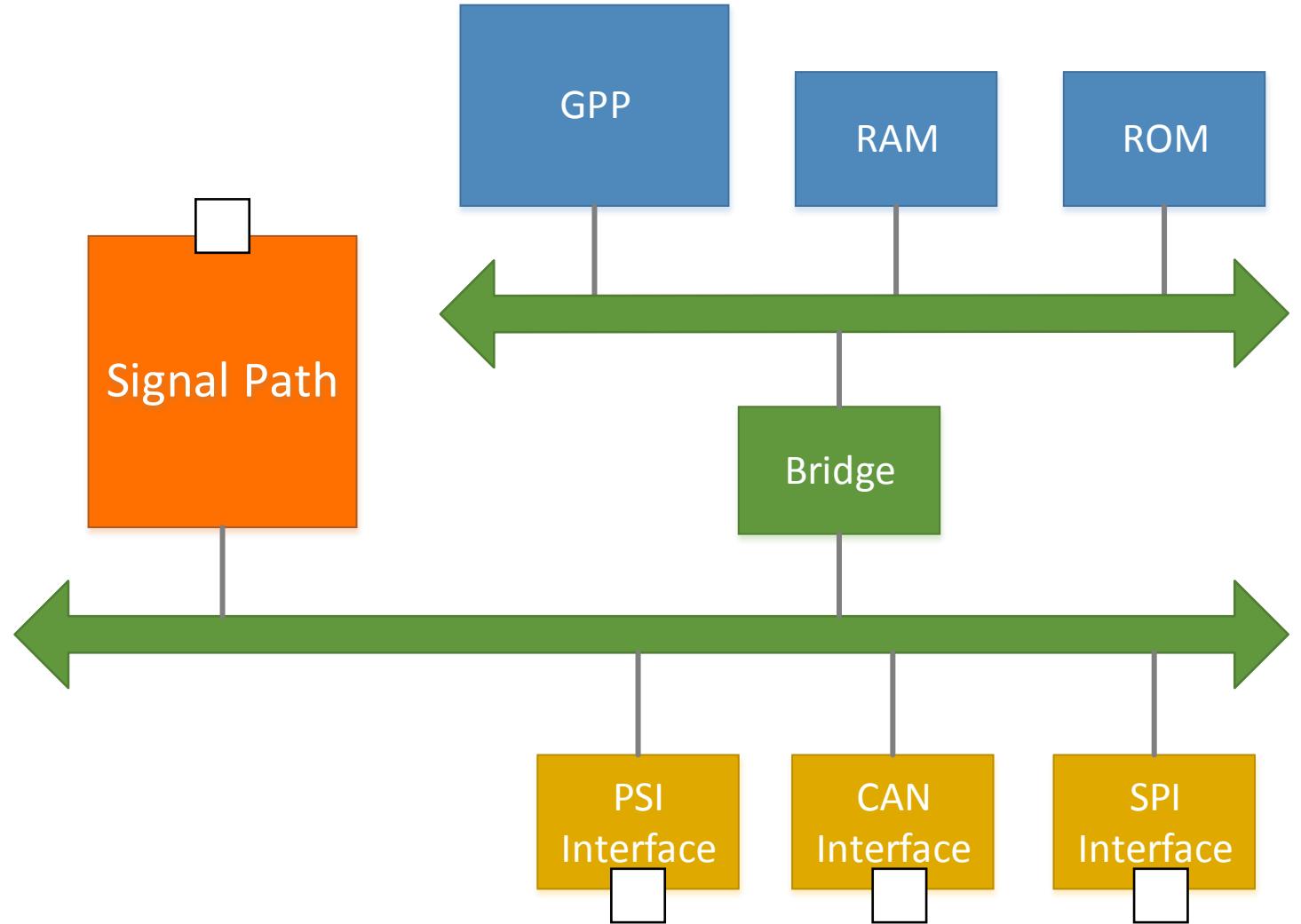
Architecture Example



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- Signal path for sensor signal processing
- General Purpose Processor (GPP) subsystem for
 - safety monitoring
 - communication protocols
 - etc.
- Several interfaces
- On-Chip-Architecture



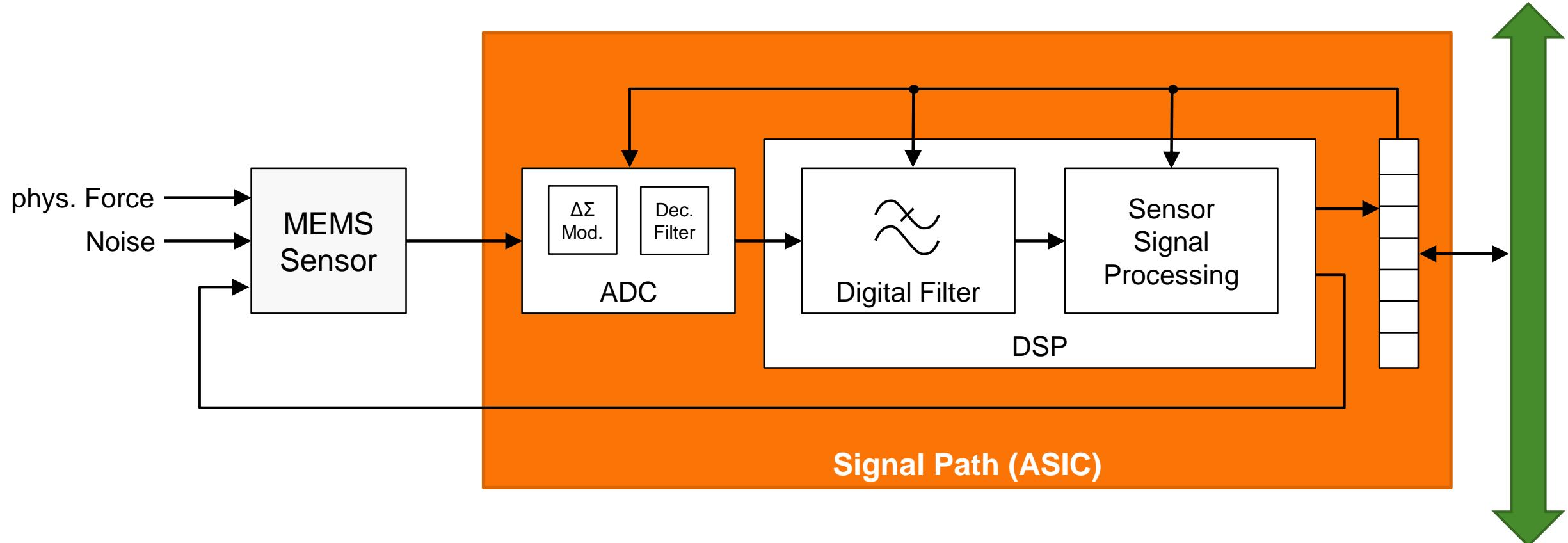
Sensor ASIC

Signal Path Example



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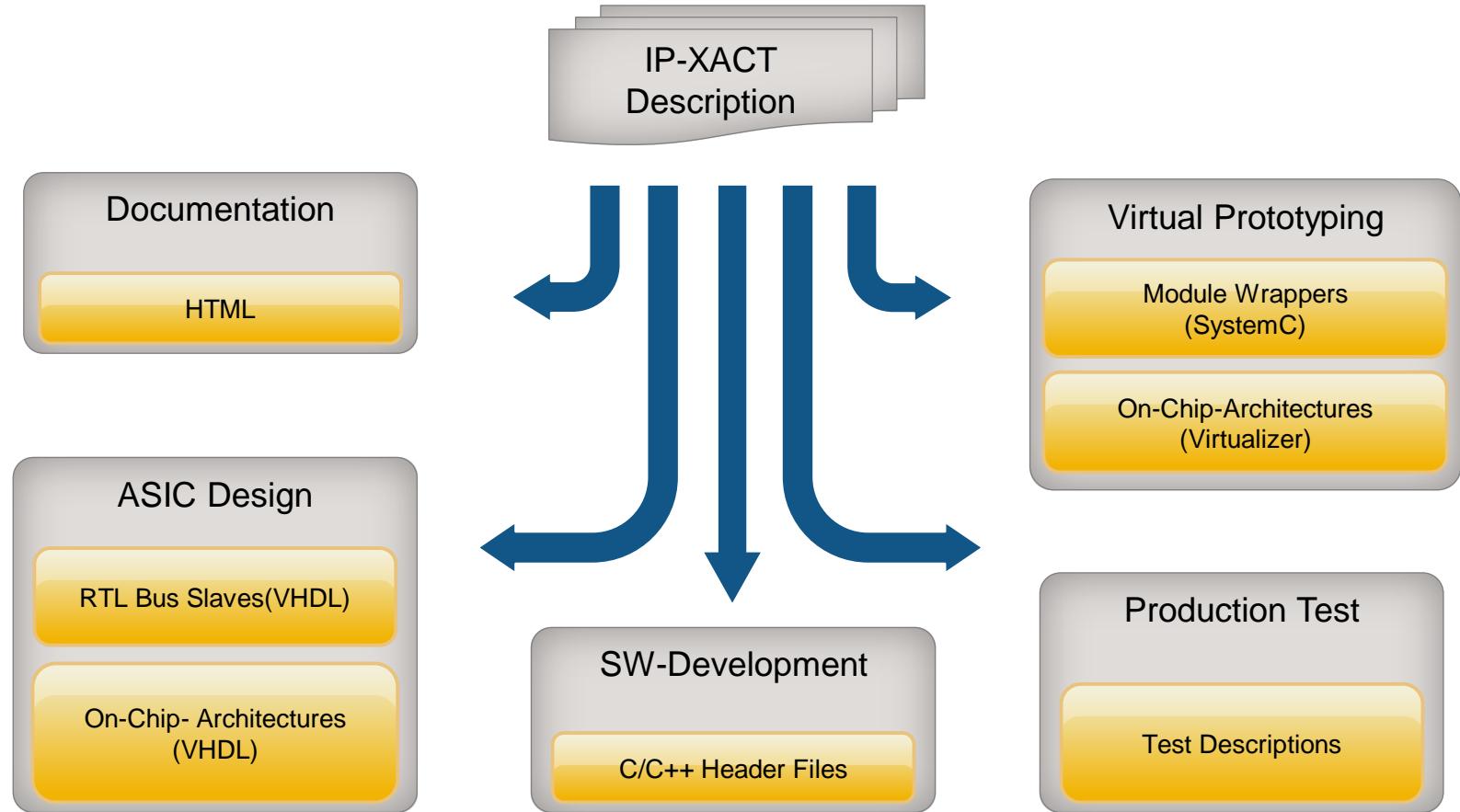
The Current Workflow and its Challenges



Current Workflow

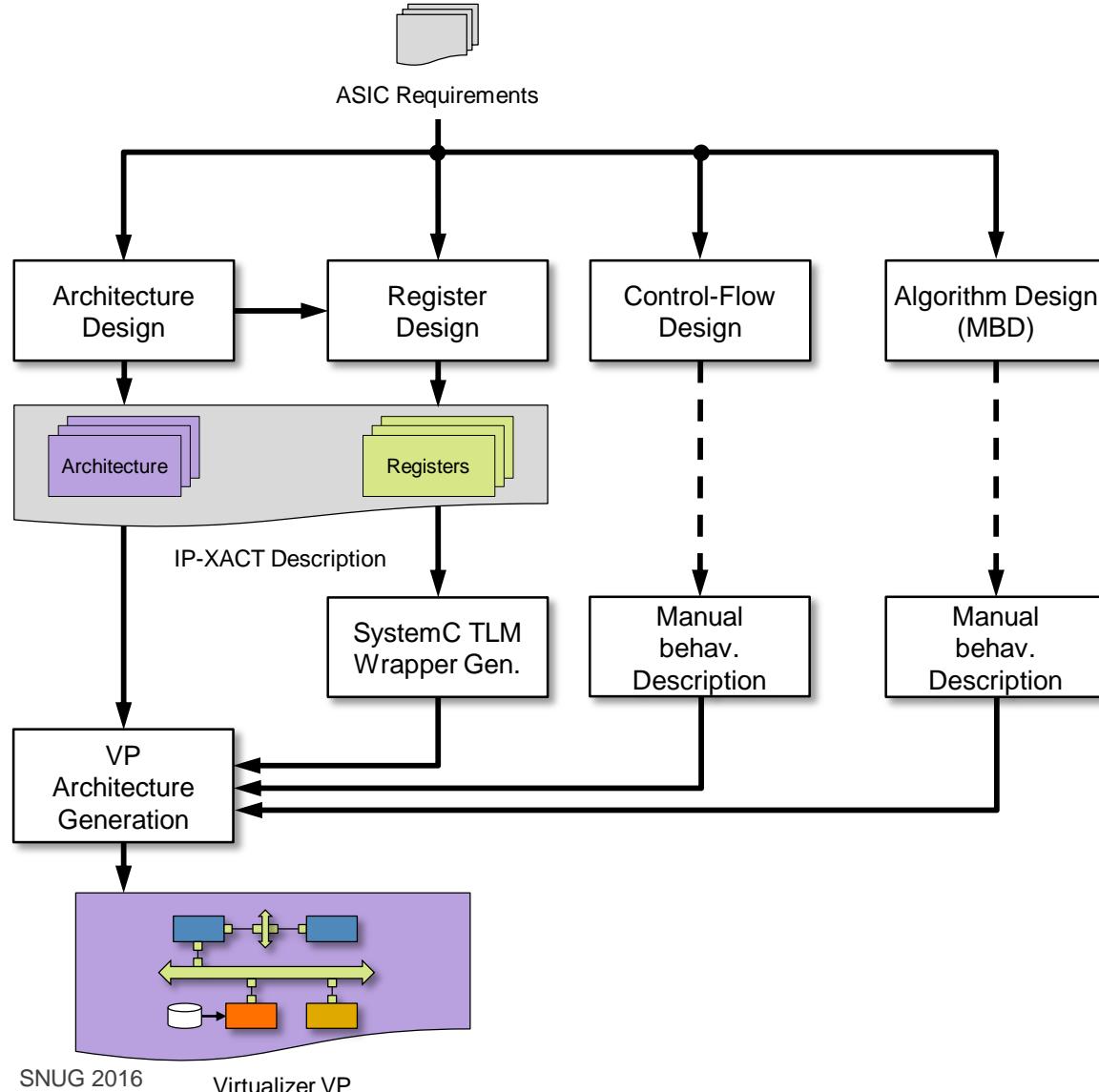
IP-XACT-Centric Tool Environment

- IP-XACT description as single source
- Generation of various design, test and documentation outputs
- Ensures consistency throughout the whole design flow



Current Workflow

IP-XACT-centric VP Generation



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- Automated generation of VP architectures and TLM register interfaces
- Signal processing algorithm design using Model-Based Design
- Manual behavioural description of control- and signal-flow oriented designs

Virtual Platform and Model-Based Design

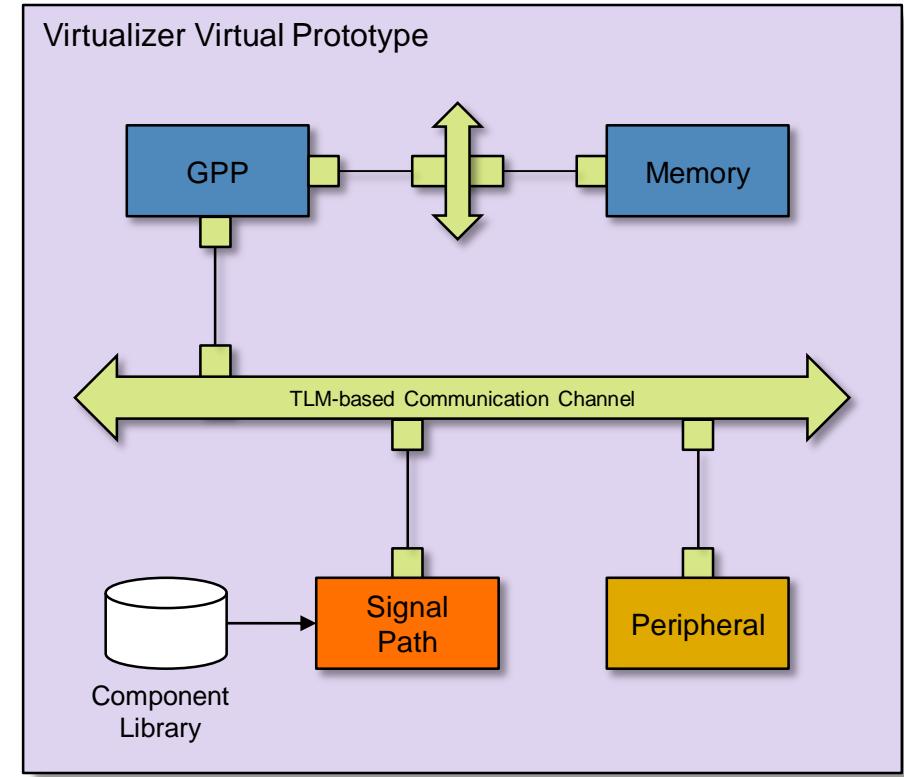


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Virtual Platforms (VP)

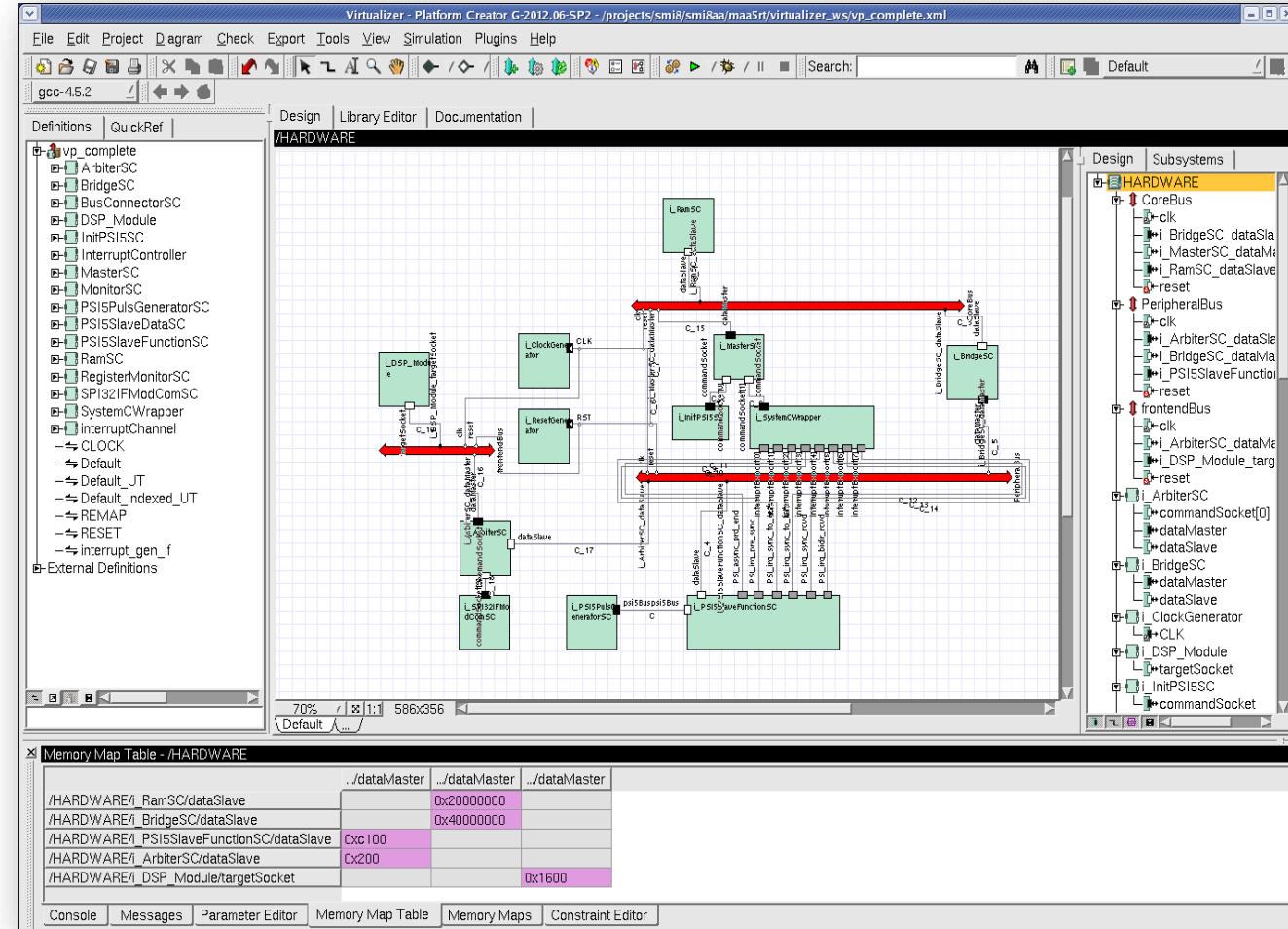
- SoC architecture centric
- High-speed pre-silicon development environment
- Abstracting communication interfaces through Transaction Level Modelling (TLM)
- Benefits
 - SoC concept validation and architectural exploration
 - Concurrent SW and HW development
 - Validation of HW/SW interfaces
 - Optimization of SW



VP for SoC Architecture Definition

System Simulation and SW Development in Synopsys Virtualizer

- Tool for construction and simulation of Virtual Prototypes
- Large module library
- Comprehensive debugging capabilities
- Export of development kits for SW development



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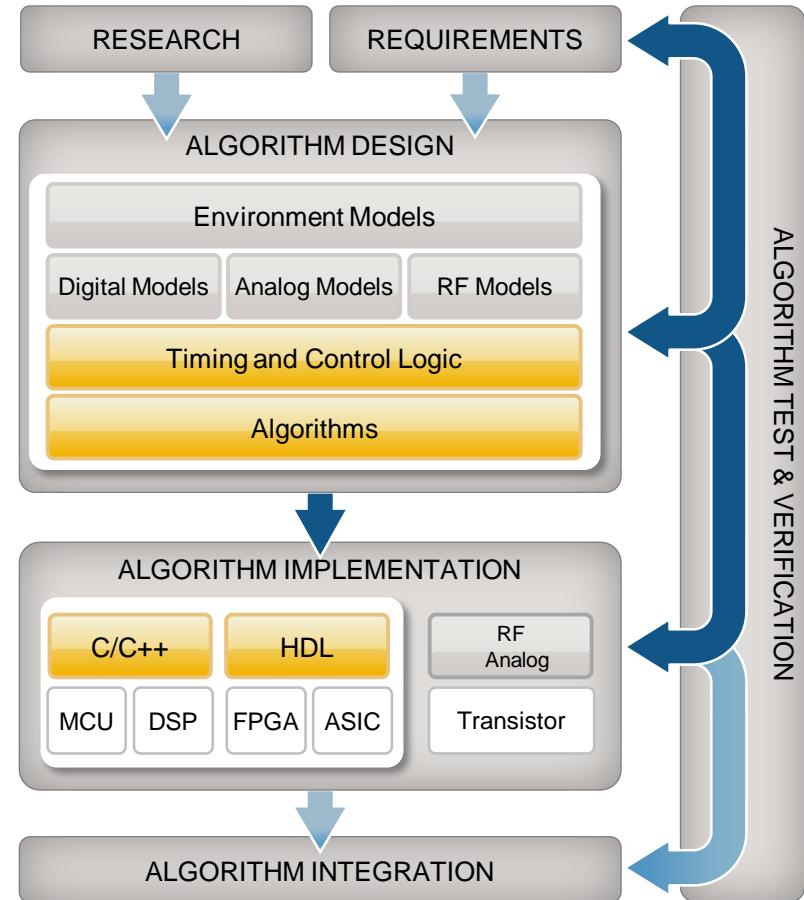
Virtual Platform and Model-Based Design

Model-Based Design (MBD)



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- Algorithm centric
- Signal-flow-oriented multi-domain simulation
 - Differential equation, transfer function, physical network level
 - Time-continuous, time-discrete
 - Value-continuous, value-discrete
- Benefits
 - Mathematical algorithm design
 - Early verification of its functional correctness and performance in its environment
 - Implementation through automatic code generation

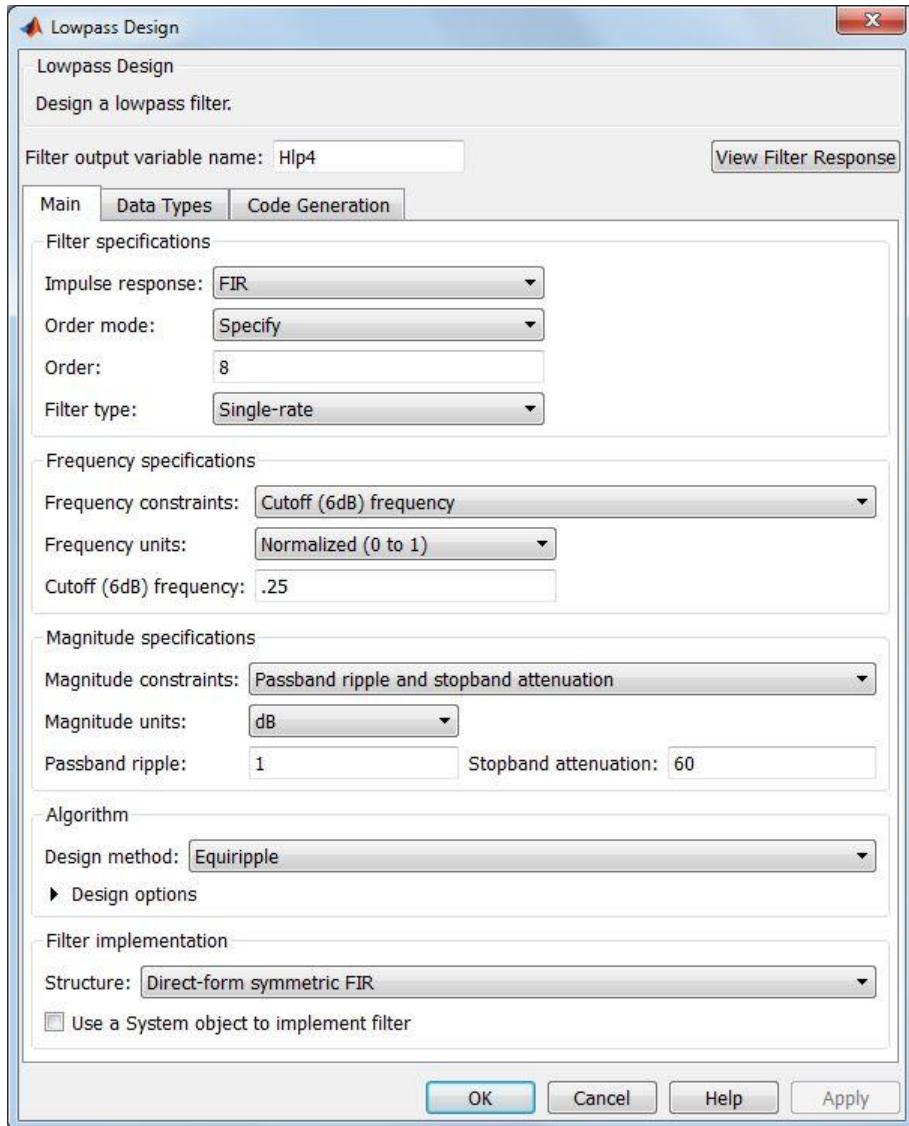
Algorithm Design w/ Model-Based Design

Example: Lowpass Filter



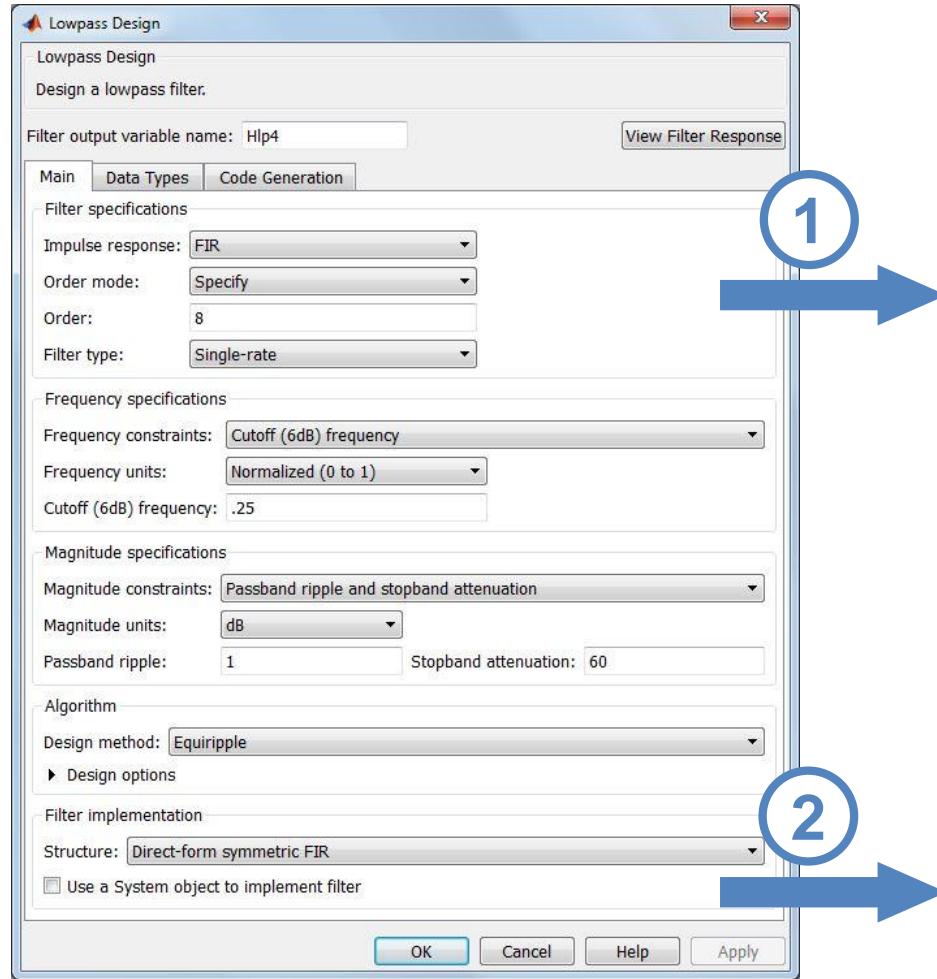
Specification:

- Filter response: FIR
- Design Method: Equiripple
- 6dB-cutoff frequency: 0.25
- Stopband attenuation: 60 dB
- Passband ripple: 1 dB

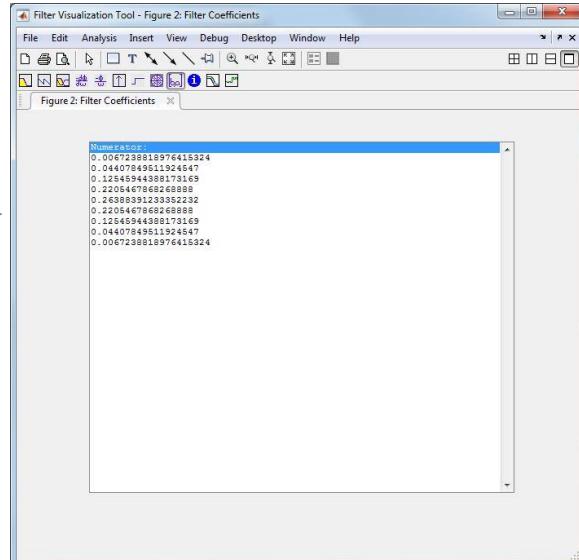


Algorithm Design w/ Model-Based Design

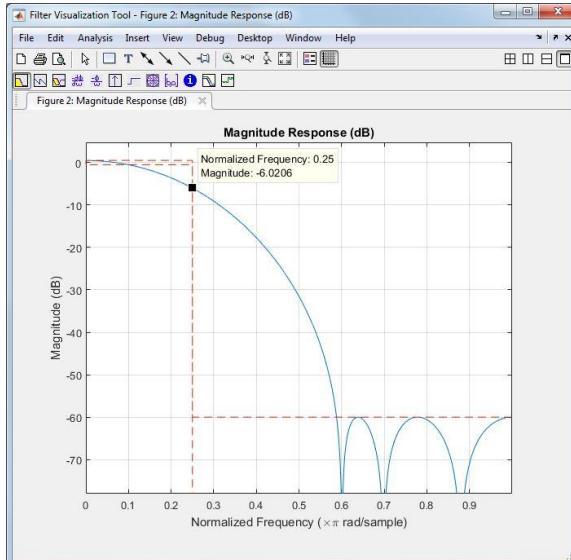
Step 1: Algorithm Design and Verification with MATLAB



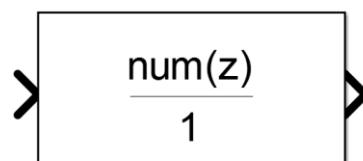
Filter Coefficients



Magnitude Response



Export from MATLAB to Simulink

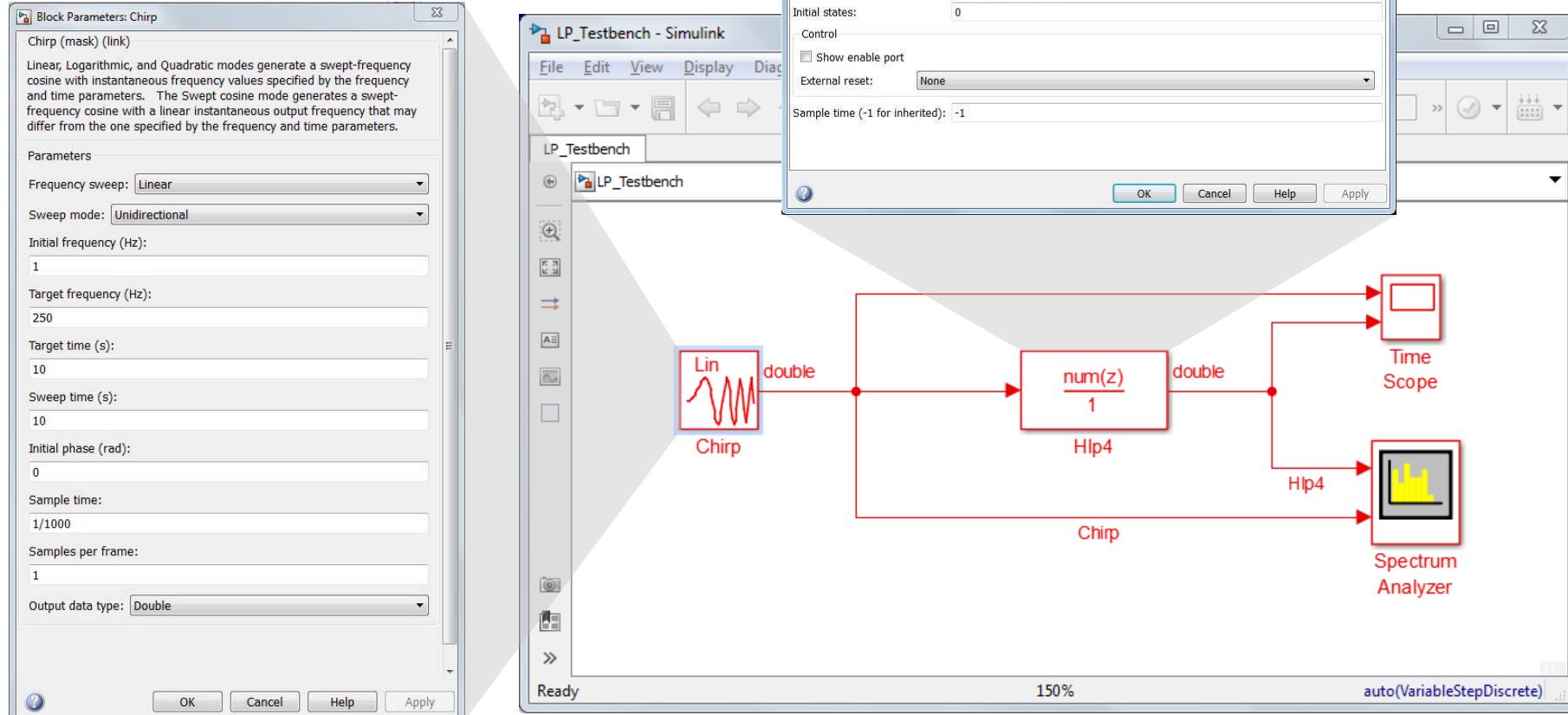


Algorithm Design w/ Model Based Design

Step 2: Signal Flow based Simulation with Simulink

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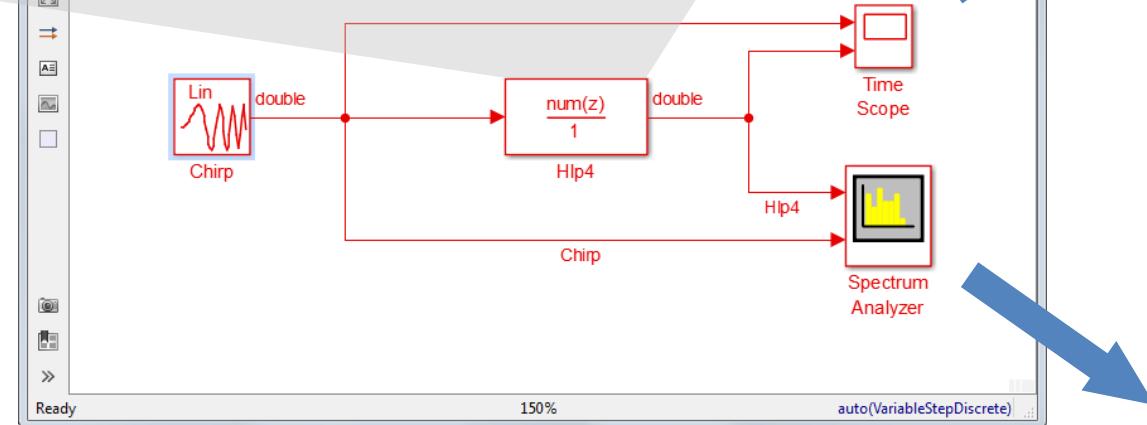
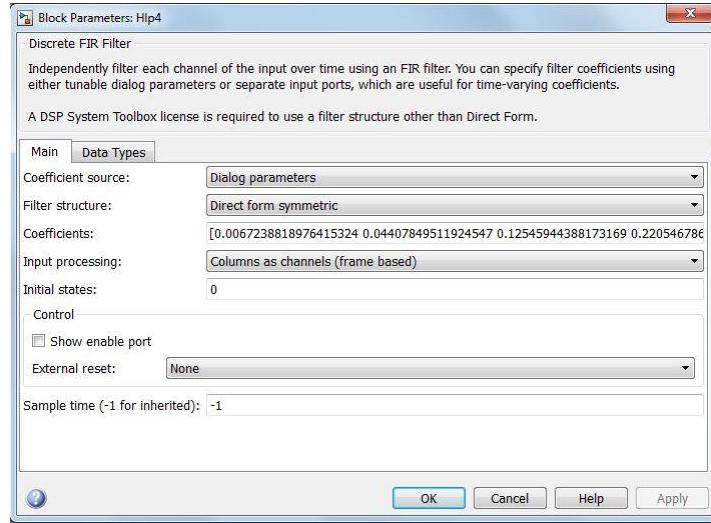


Algorithm Design w/ Model Based Design

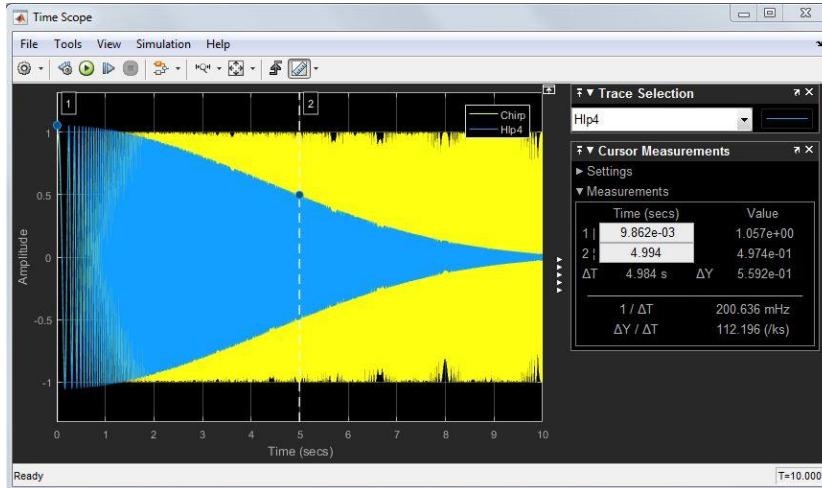
Signal-Flow-based Simulation with Simulink

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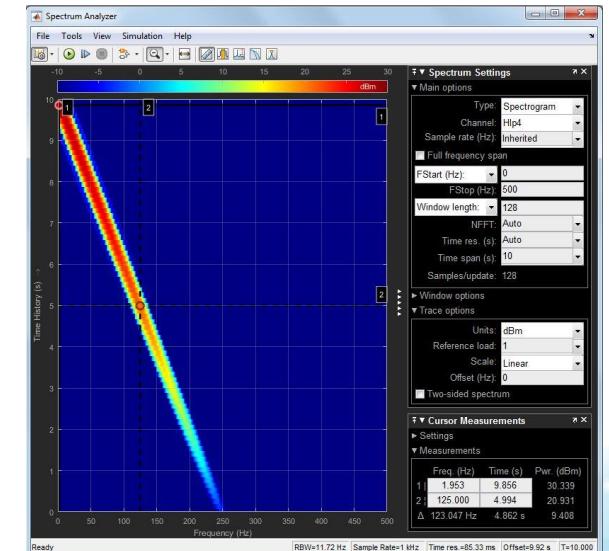
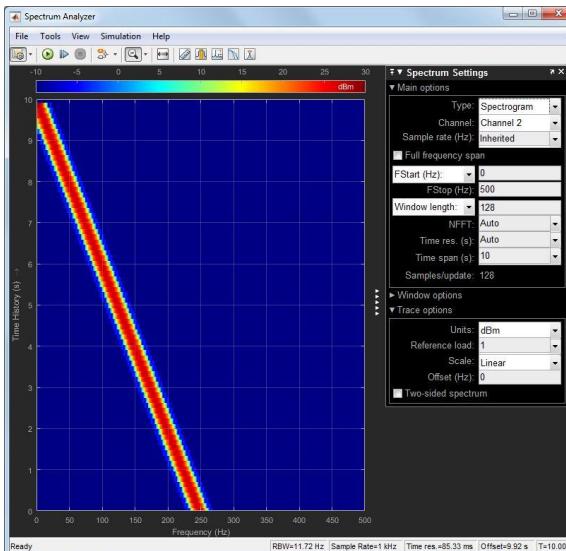
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Time domain:

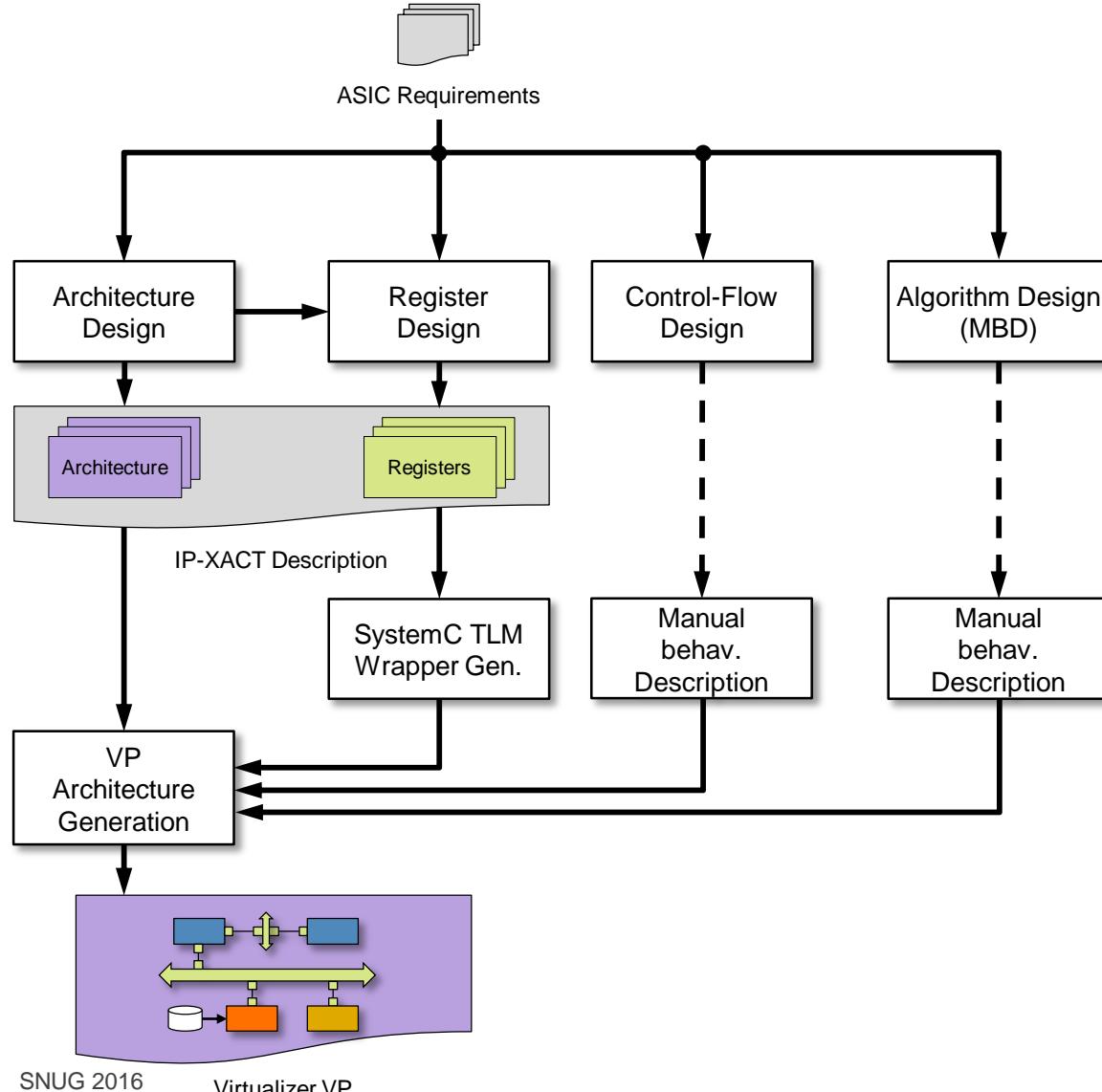


Frequency domain:



IP-XACT-centric VP Generation

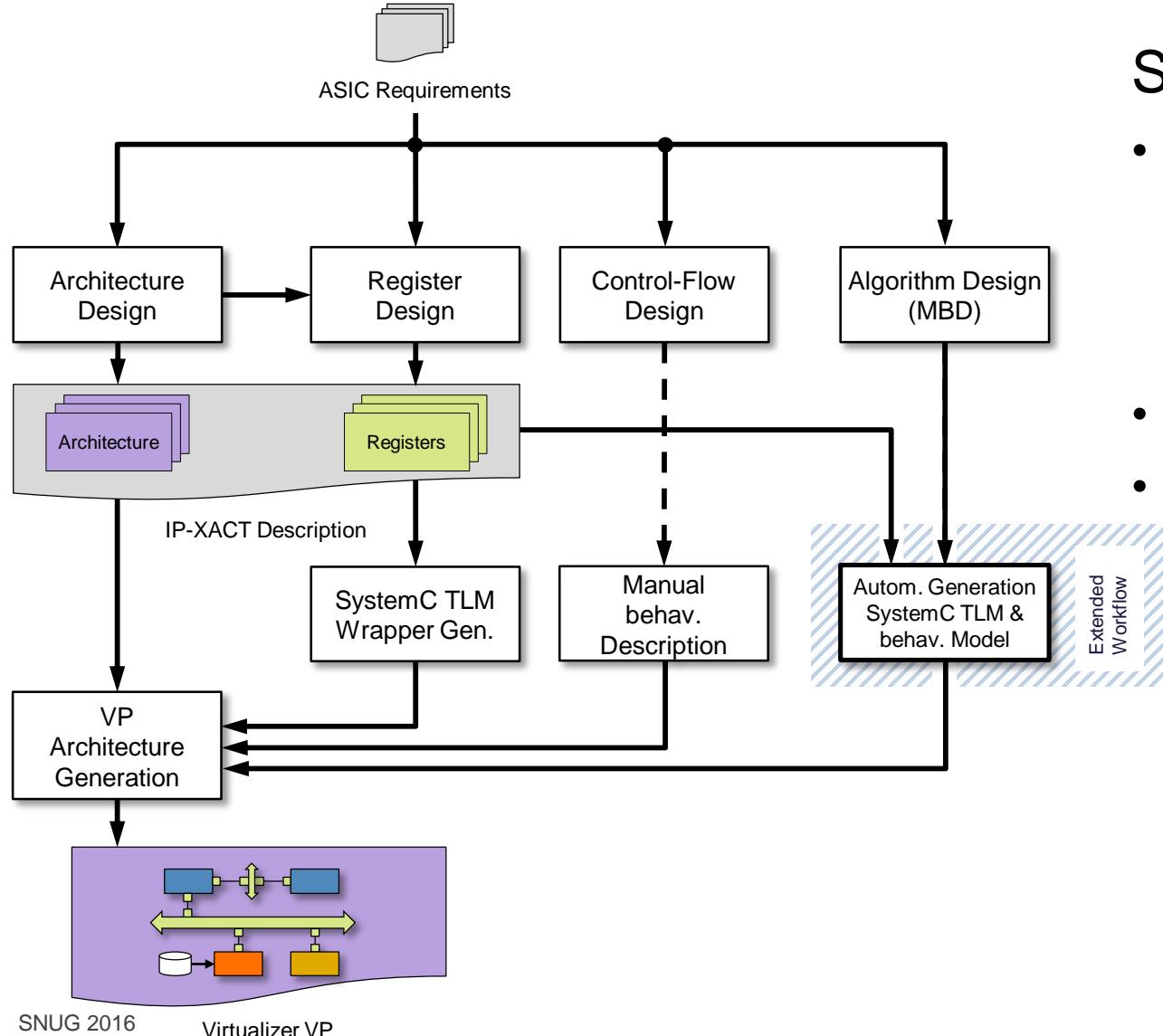
Gap Analysis



- Benefits of Model-Based Design
 - Verified algorithm meeting signal processing characteristics
- Workflow Gap
 - Manual behavioural description of algorithm
 - Manual integration into SystemC TLM wrapper
- Potential Issue
 - Mismatch between manual behavioural description and implementation

IP-XACT-centric VP Generation

Gap Analysis



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Solution:

- Automatic generation of SystemC TLM component
 - Behavioural algorithmic model
 - Integration in SystemC TLM wrapper
- IP-XACT register definition as input
- Support of SCML register



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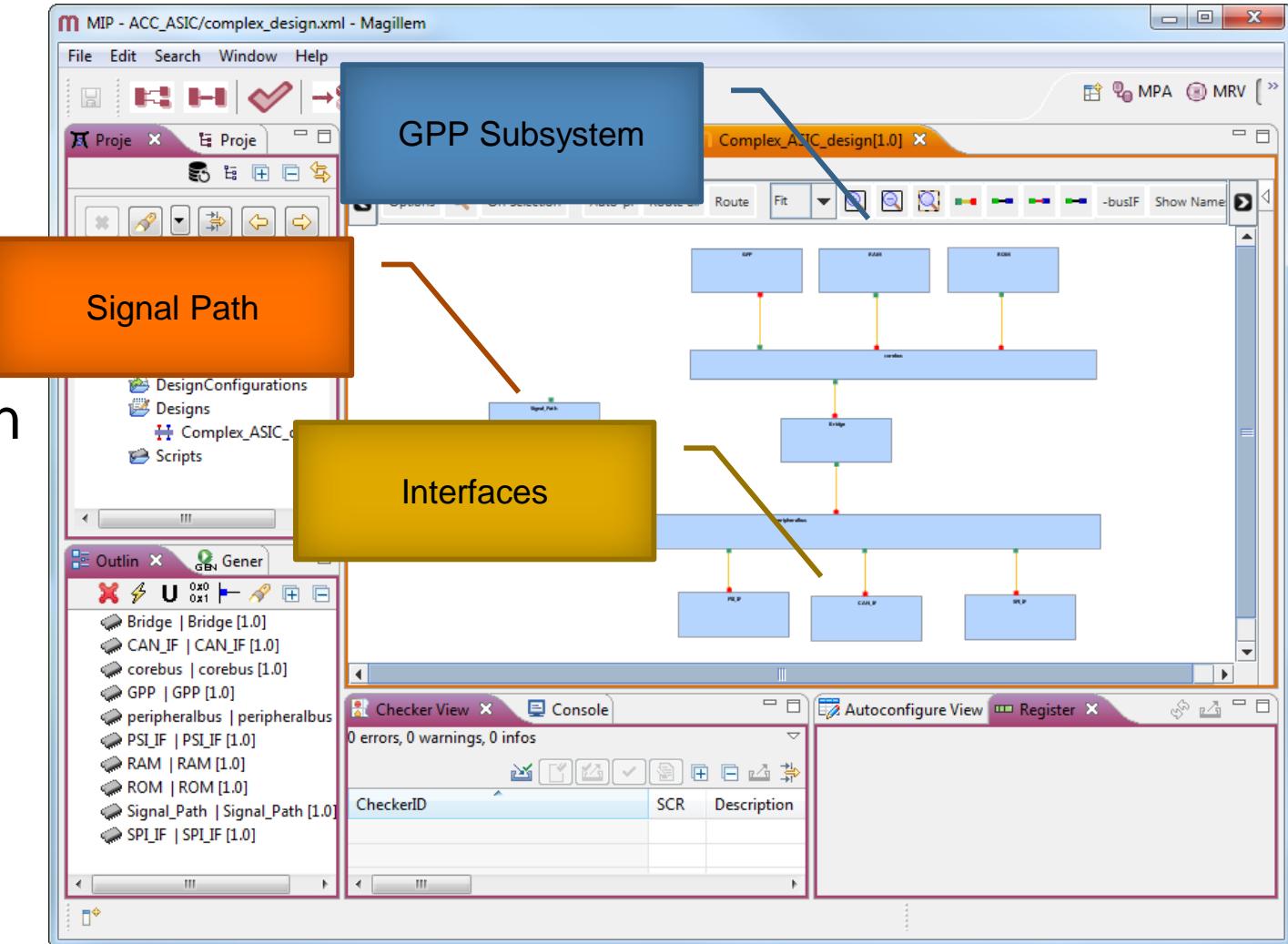
The Improved Workflow



Architecture Design

Magillem IP-XACT Packager (MIP)

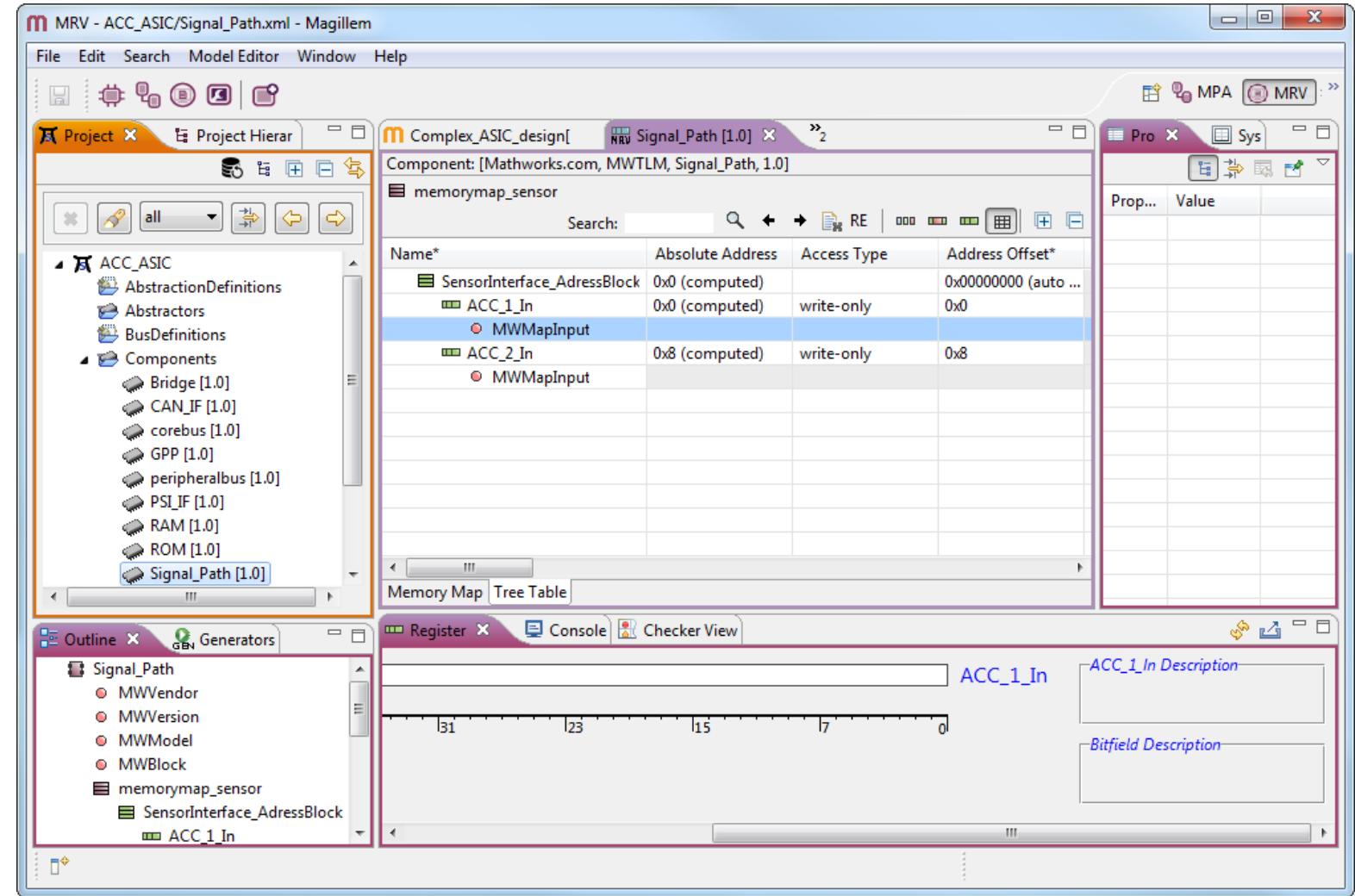
- Design of On-Chip-Architecture in Magillem IP-XACT Packager
- Saved as IP-XACT Design description



Register Interface Design

Magillem Register View (MRV)

- Design of register interfaces in Magillem Register View
- Saved as IP-XACT Component description

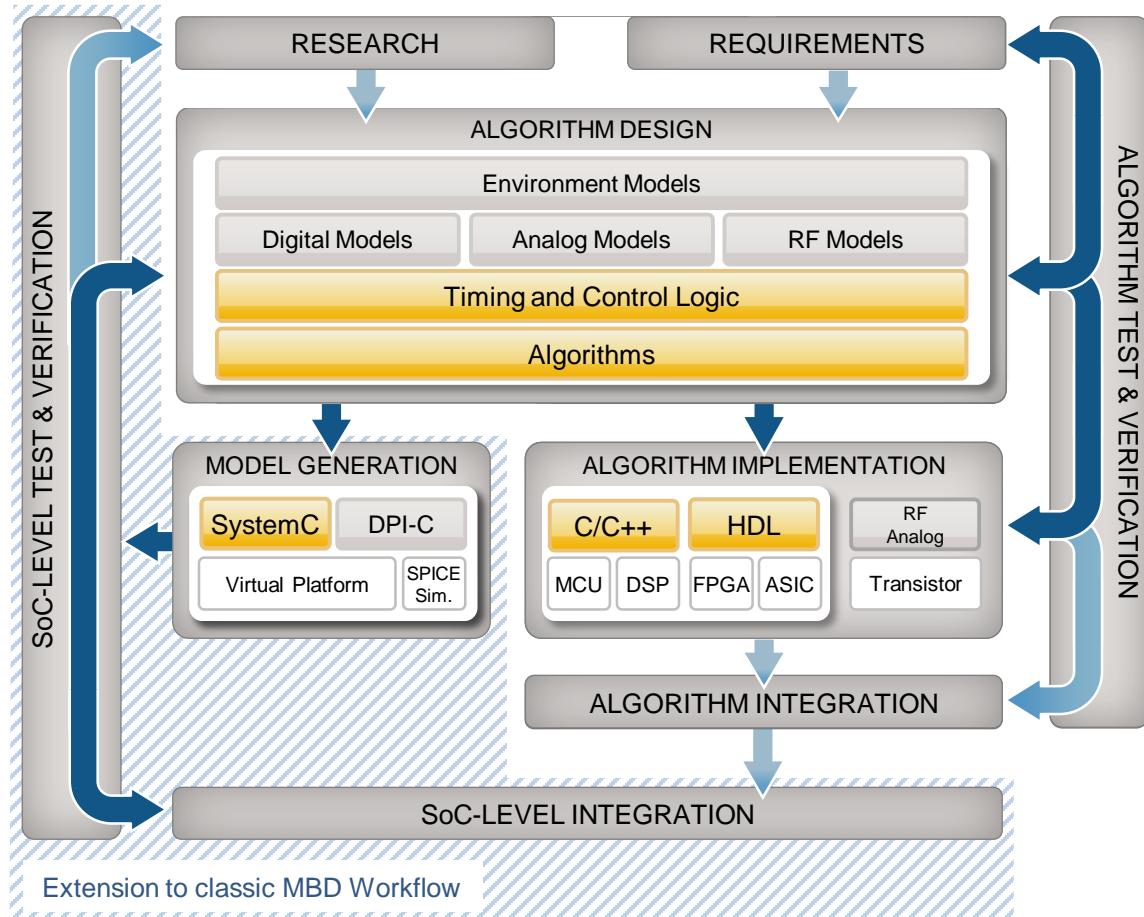


Algorithm Design & Model Generation



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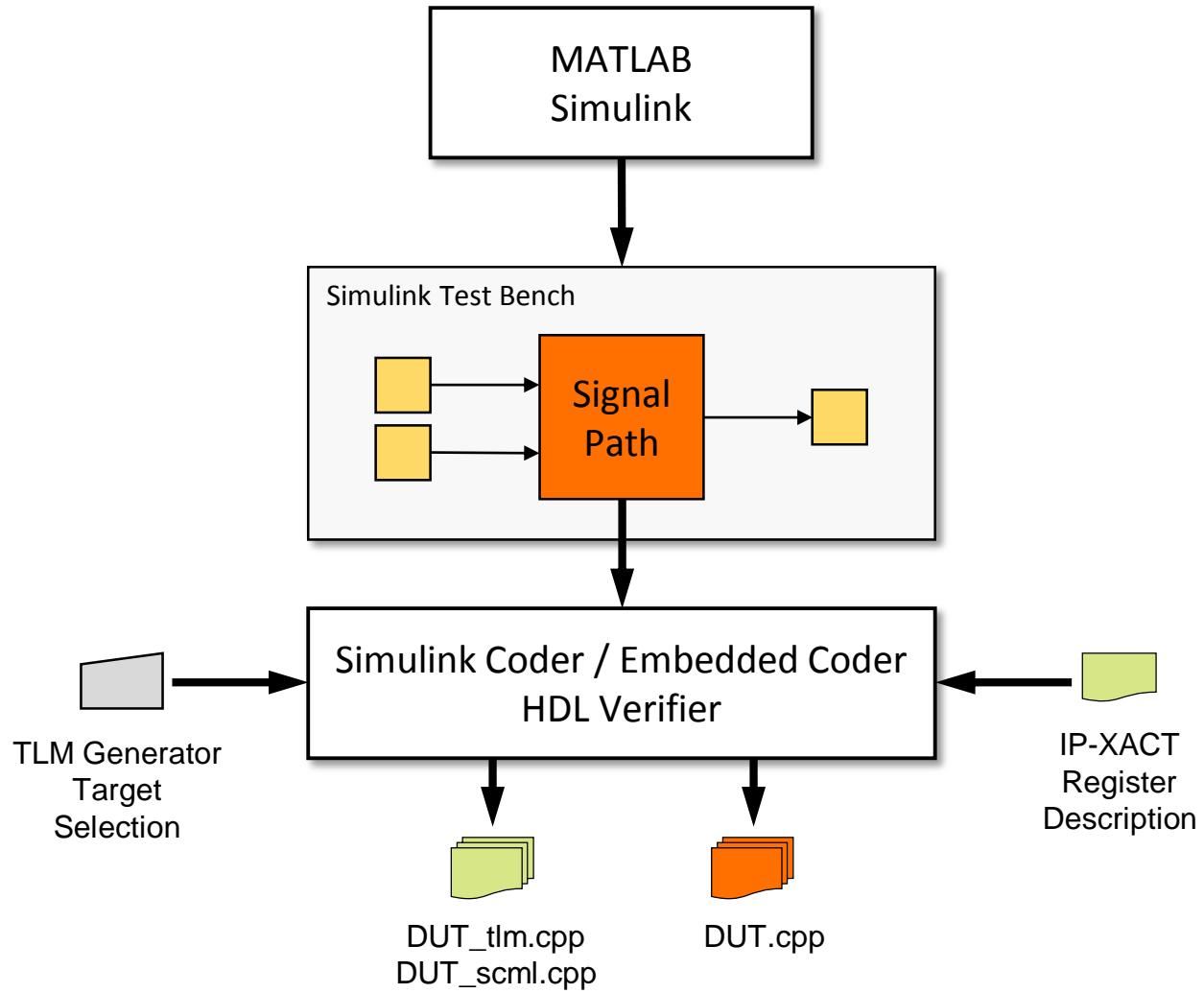
- Extended Model-Based Design Workflow
 - Model Generation
- Additional code generation targets
 - Virtual platforms (e.g. SystemC TLM 2.0)
 - Verification environments (e.g. SystemVerilog DPI-C)
- Benefits
 - Integrated, automated workflow
 - Functional equivalence between ..
 - Algorithm design
 - Virtual Platform model
 - Algorithm implementation

Algorithm Design & Model Generation



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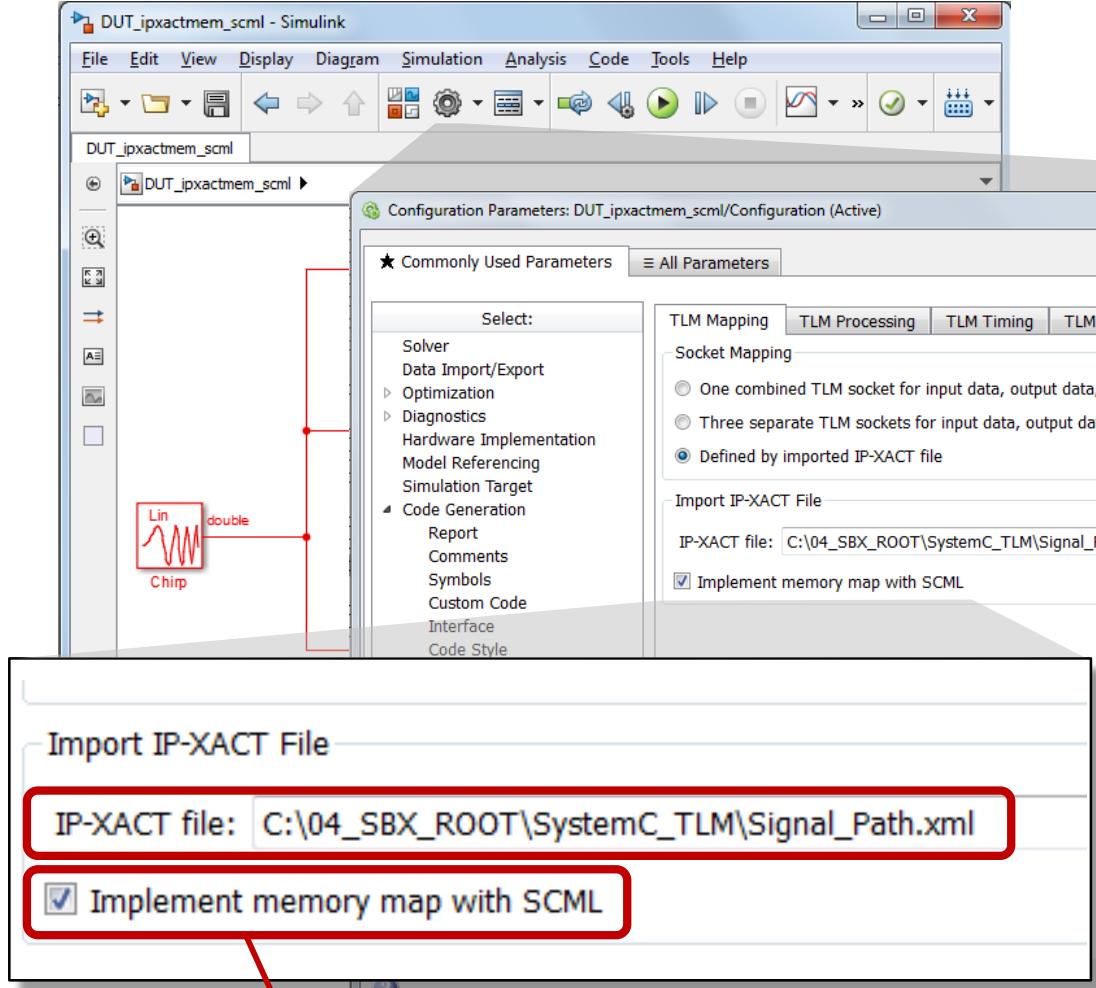
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- Algorithm Design
 - Mathematical representation
 - Multi-domain simulation environment
 - Early algorithm verification within ist environment
- Model Generation
 - Automatic code generation (SystemC TLM)
 - IP-XACT register description as input
 - Behavioural description integrated in SystemC TLM wrapper
 - Self-testing SystemC TLM testbench
 - IP-XACT register description as output

Model Generation

IP-XACT Register Mapping (I/O, Parameters)



SCML Register Support

Input: IP-XACT Register Mapping

```
87 <spirit:memoryMap>
88   <spirit:name>memorymap_bus</spirit:name>
89   <spirit:addressBlock>
90     <spirit:name>BusInterface_AdressBlock</spirit:name>
91     <spirit:baseAddress spirit:id="subsystem_tlm_base_address_output">
92       <spirit:range spirit:resolve="immediate">0x100</spirit:range>
93       <spirit:width>64</spirit:width>
94       <spirit:usage>register</spirit:usage>
95 
96   <spirit:register>
97     <spirit:name>ACC1_Out</spirit:name>
98     <spirit:addressOffset>0x00</spirit:addressOffset>
99       <spirit:access>read-only</spirit:access>
100      <spirit:reset>
101        <spirit:value>0x00</spirit:value>
102      </spirit:reset>
103 
104   <spirit:parameter>
105     <spirit:name>MWMapOutput</spirit:name>
106     <spirit:value>sym_Hlp4</spirit:value>
107   </spirit:parameter>
108 
109 </spirit:register>
```

A red box highlights the first register definition, and another red box highlights the parameter definition. A red arrow points from the 'Implement memory map with SCML' checkbox in the Simulink dialog to the 'Implement memory map with SCML' text in the IP-XACT code.

Interface mapping between
IP-XACT and Simulink



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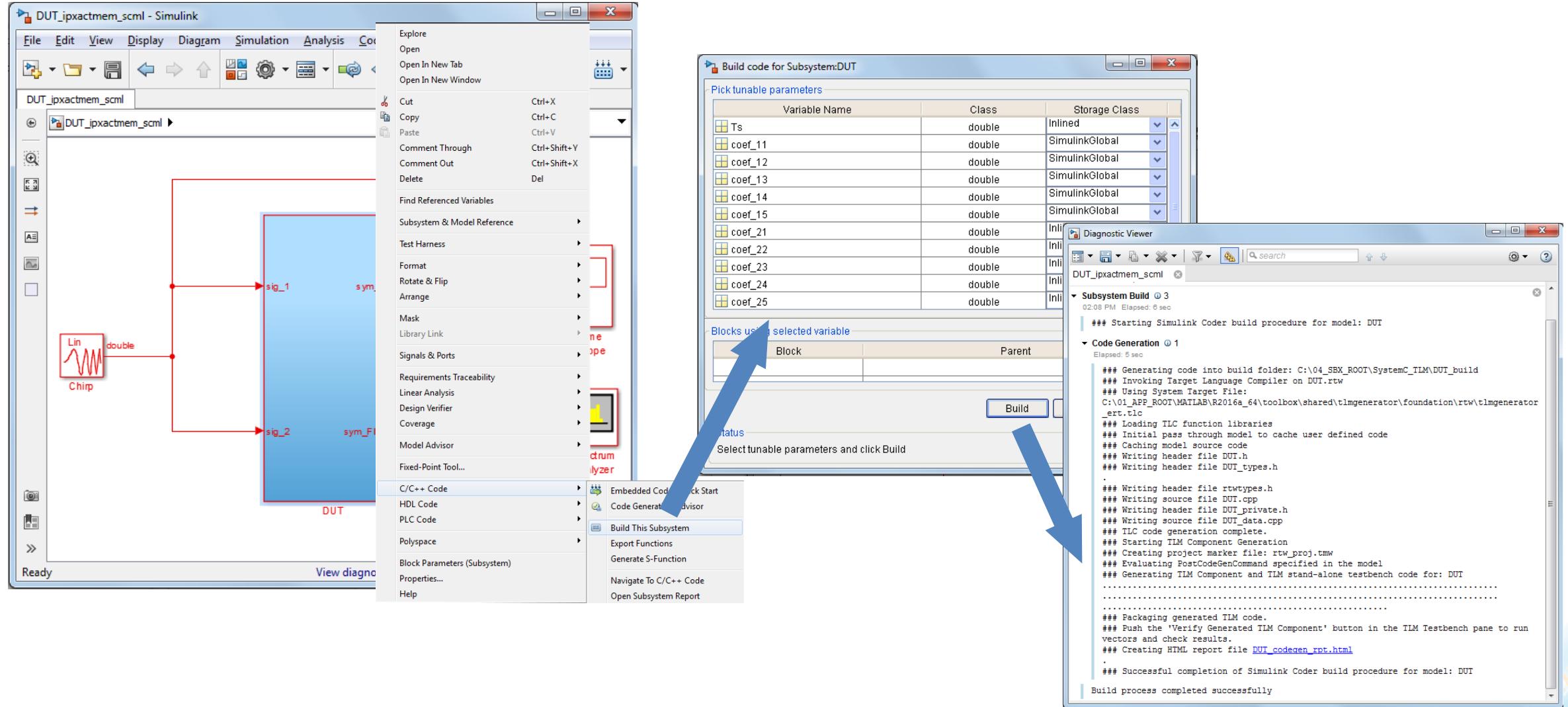
Model Generation

Automatic SystemC TLM 2.0 Code Generation



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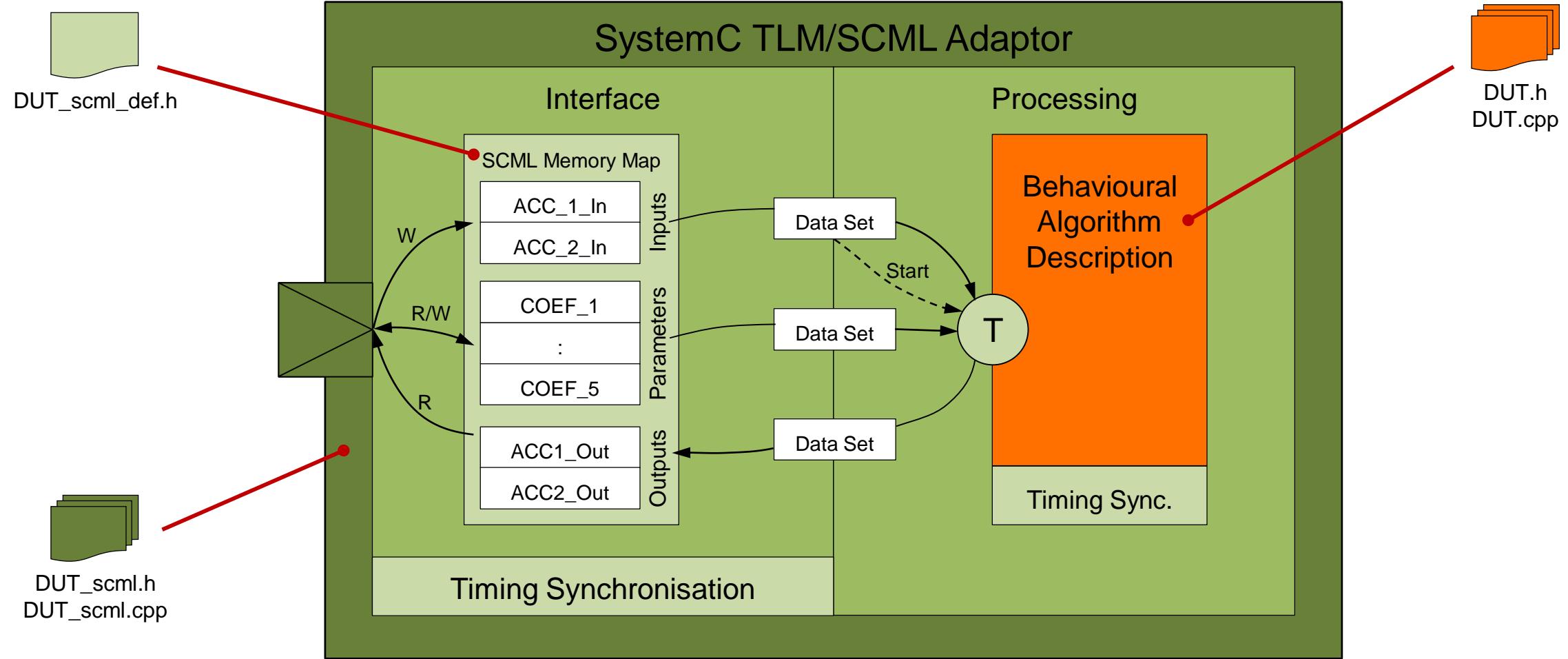
Model Generation

SystemC TLM/SCML Adaptor Architecture



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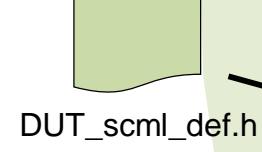
Model Generation

SystemC TLM/SCML Adaptor Architecture



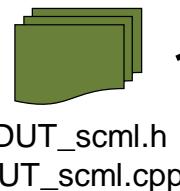
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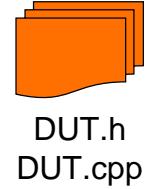
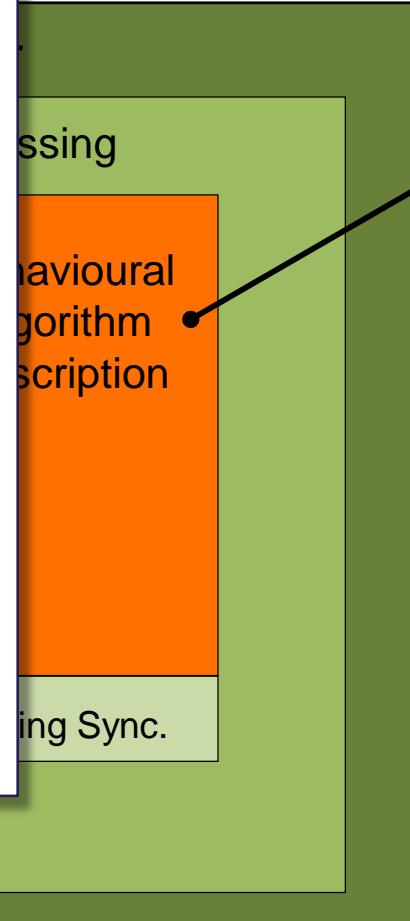


DUT_scml_def.h

```
39 //===== BusInterface SOCKET ======
40 #define BusInterface_BUSWIDTH          64
41
42 //===== BusInterface_AdressBlock BANK ======
43 //Bank base address
44 #define BusInterface_AdressBlock_ADDR   0x00010000
45
46 //===== REGISTERS ======
47 //Address of the registers
48 #define ACC1_Out_ADDR                 0x00000000
49 #define ACC2_Out_ADDR                 0x00000008
50 #define COEF_1_ADDR                  0x00000010
51 #define COEF_2_ADDR                  0x00000018
52 #define COEF_3_ADDR                  0x00000020
53 #define COEF_4_ADDR                  0x00000028
54 #define COEF_5_ADDR                  0x00000030
```



DUT_scml.h
DUT_scml.cpp



DUT.h
DUT.cpp

Model Generation

SystemC TLM/SCML Adaptor Architecture



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DUT_scml_def.h

```
20     BusInterface("BusInterface"),
21     BusInterface_adapter("BusInterface_adapter",BusInterface),
22     BusInterface_router("BusInterface_router",65792/sizeof(uint8_T[8])),
23     BusInterface_AdressBlock("BusInterface_AdressBlock",256/sizeof(uint8_T[8])),
24     ACC1_Out("ACC1_Out",BusInterface_AdressBlock,ACC1_Out_ADDR/sizeof(uint8_T[8])),
25     ACC2_Out("ACC2_Out",BusInterface_AdressBlock,ACC2_Out_ADDR/sizeof(uint8_T[8])),
26     COEF_1("COEF_1",BusInterface_AdressBlock,COEF_1_ADDR/sizeof(uint8_T[8])),
27     COEF_2("COEF_2",BusInterface_AdressBlock,COEF_2_ADDR/sizeof(uint8_T[8])),
28     COEF_3("COEF_3",BusInterface_AdressBlock,COEF_3_ADDR/sizeof(uint8_T[8])),
29     COEF_4("COEF_4",BusInterface_AdressBlock,COEF_4_ADDR/sizeof(uint8_T[8])),
30     COEF_5("COEF_5",BusInterface_AdressBlock,COEF_5_ADDR/sizeof(uint8_T[8])),
```

DUT_scml.h
DUT_scml.cpp

```
37     scml2::set_write_callback(ACC_1_In, SCML2_CALLBACK(ACC_1_In_write_cb), scml2::
38         AUTO_SYNCING);
39     scml2::set_write_callback(ACC_2_In, SCML2_CALLBACK(ACC_2_In_write_cb), scml2::
40         AUTO_SYNCING);
41     BusInterface_adapter(BusInterface_router);
42     BusInterface_router.map(0x00010000,256,BusInterface_AdressBlock,0x00);
43     scml2::set_read_callback(ACC1_Out, SCML2_CALLBACK(ACC1_Out_read_cb), scml2::
44         AUTO_SYNCING);
```

Model Generation

SystemC TLM/SCML Adaptor Architecture



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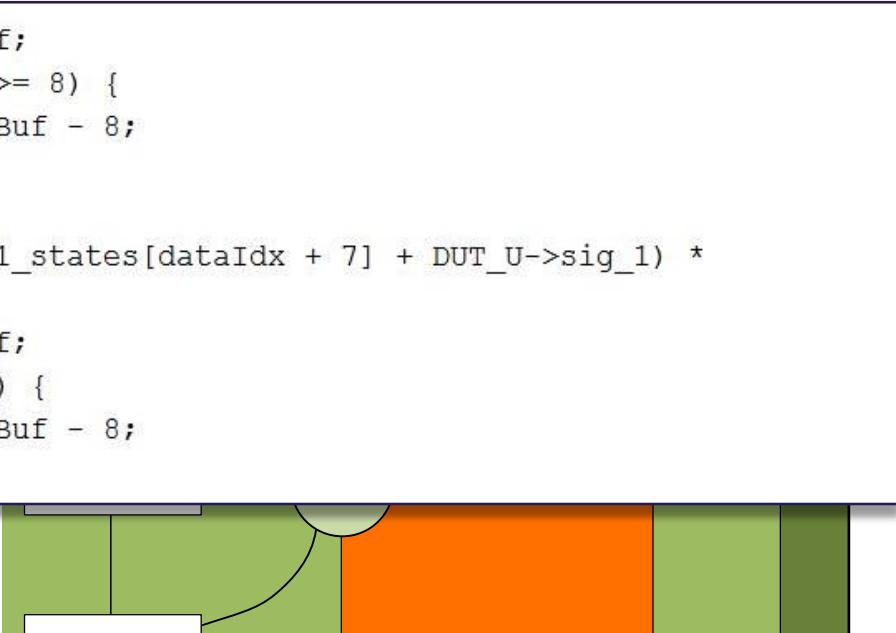

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DUT_scml_def.h

Configurable Filter Coefficients

```
42     dataIdx = DUT_DW->Hlp4_1_circBuf;
43     if (DUT_DW->Hlp4_1_circBuf + 7 >= 8) {
44         dataIdx = DUT_DW->Hlp4_1_circBuf - 8;
45     }
46
47     rtb_UnitDelay1 = (DUT_DW->Hlp4_1_states[dataIdx + 7] + DUT_U->sig_1) *
48     DUT_P->coef_11;
49     dataIdx = DUT_DW->Hlp4_1_circBuf;
50     if (DUT_DW->Hlp4_1_circBuf >= 8) {
51         dataIdx = DUT_DW->Hlp4_1_circBuf - 8;
52     }
```

DUT.h
DUT.cpp



DUT_scml.h
DUT_scml.cpp

Hardcoded Filter Coefficients

```
145     DUT_Y->sym_FIR_LP = (((DUT_DW->UnitDelay7_DSTATE + DUT_U->sig_2) *
146                             0.0067238818976415324 + (DUT_DW->UnitDelay6_DSTATE +
147                             DUT_DW->UnitDelay1_DSTATE) * 0.04407849511924547) +
148                             ((DUT_DW->UnitDelay5_DSTATE + DUT_DW->UnitDelay4_DSTATE) *
149                             0.12545944388173169 + (DUT_DW->UnitDelay4_DSTATE +
150                             DUT_DW->UnitDelay2_DSTATE) * 0.2205467868268888)) +
151                             DUT_DW->UnitDelay3_DSTATE * 0.26388391233352232;
```

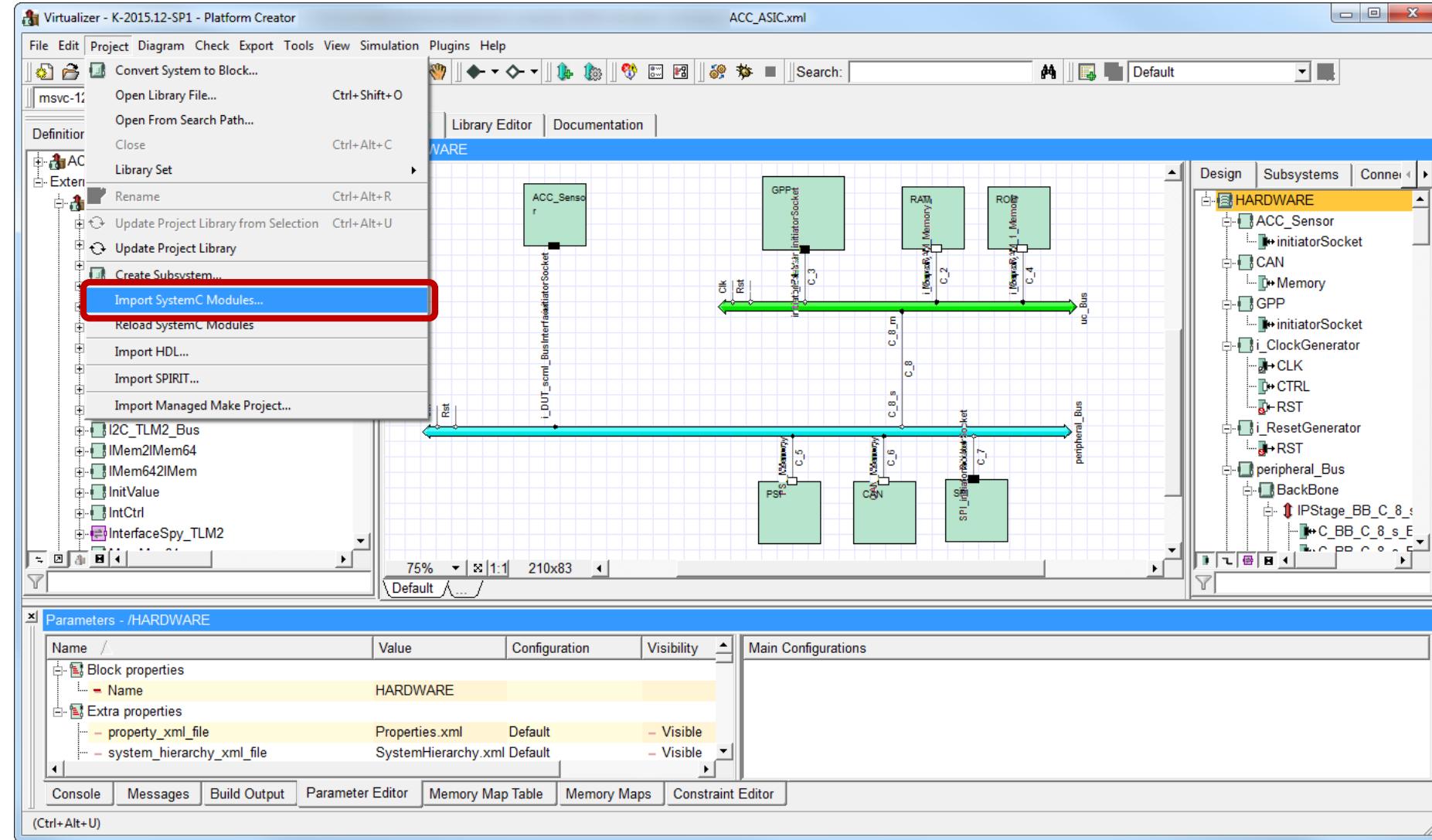
Integration into VP and Simulation

Manual Import of SystemC Module



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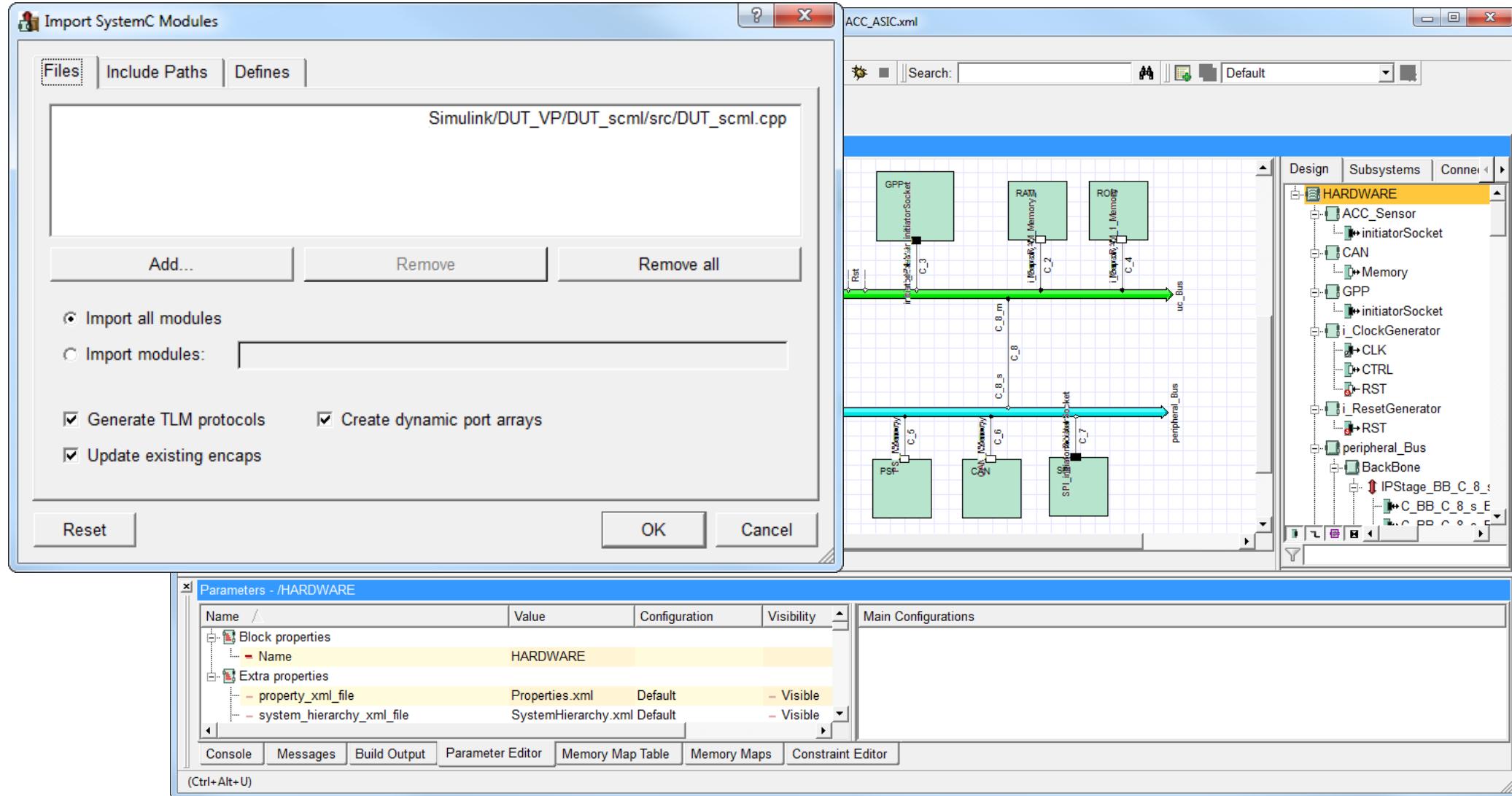
Integration into VP and Simulation



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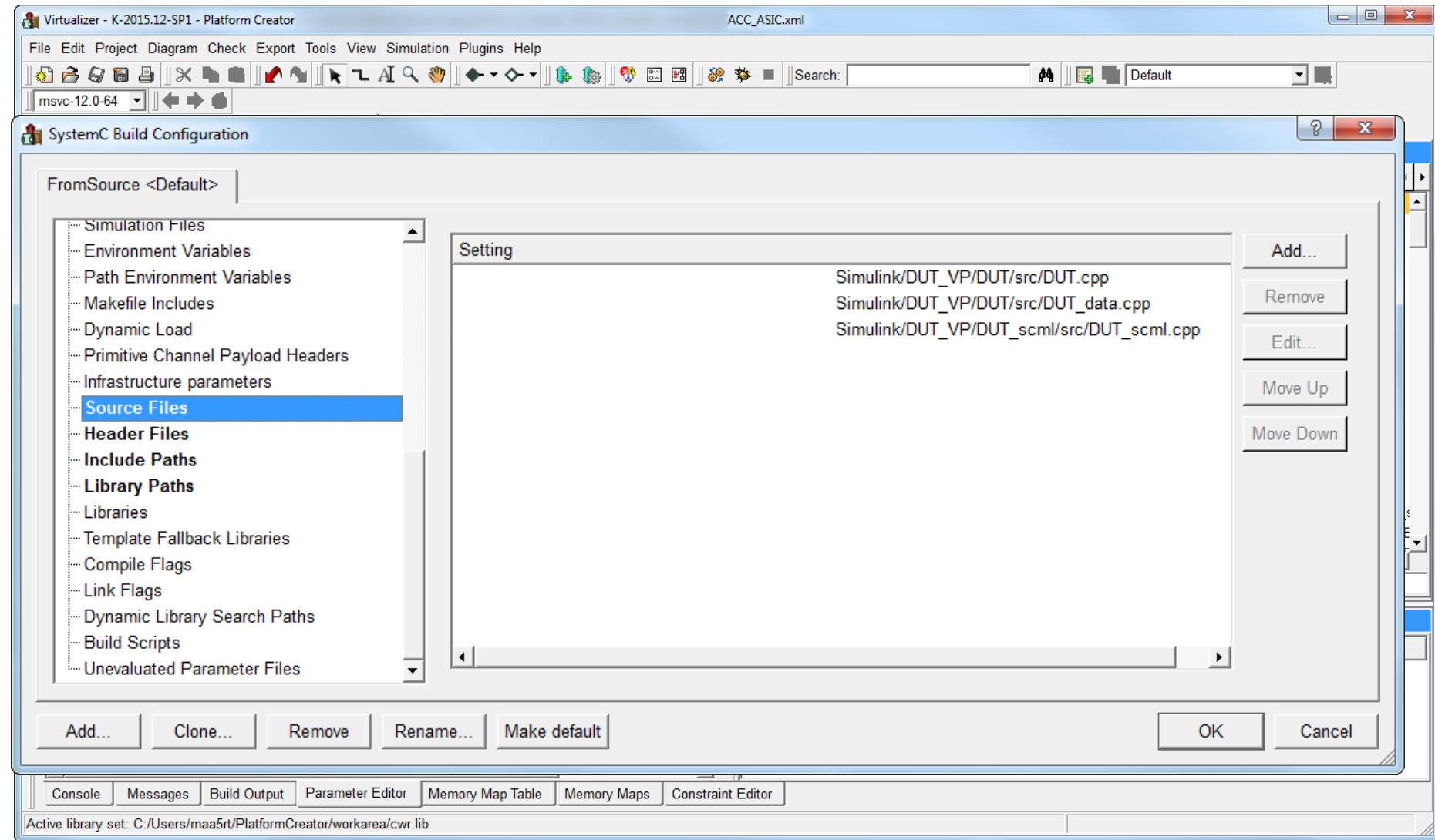


Manual Import of SystemC Module



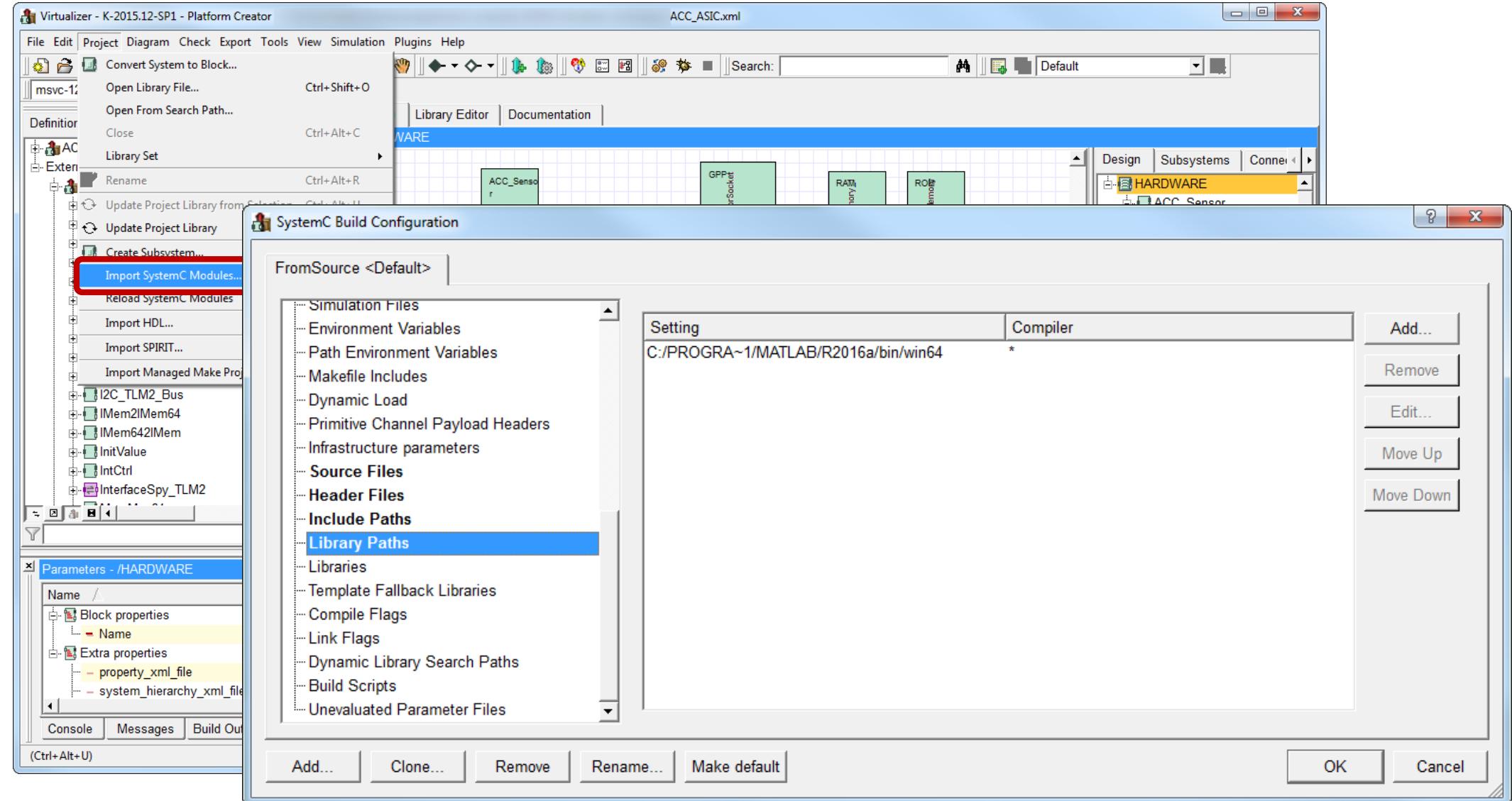
Integration into VP and Simulation

Manual Import of SystemC Module



Integration into VP and Simulation

Manual Import of SystemC Module



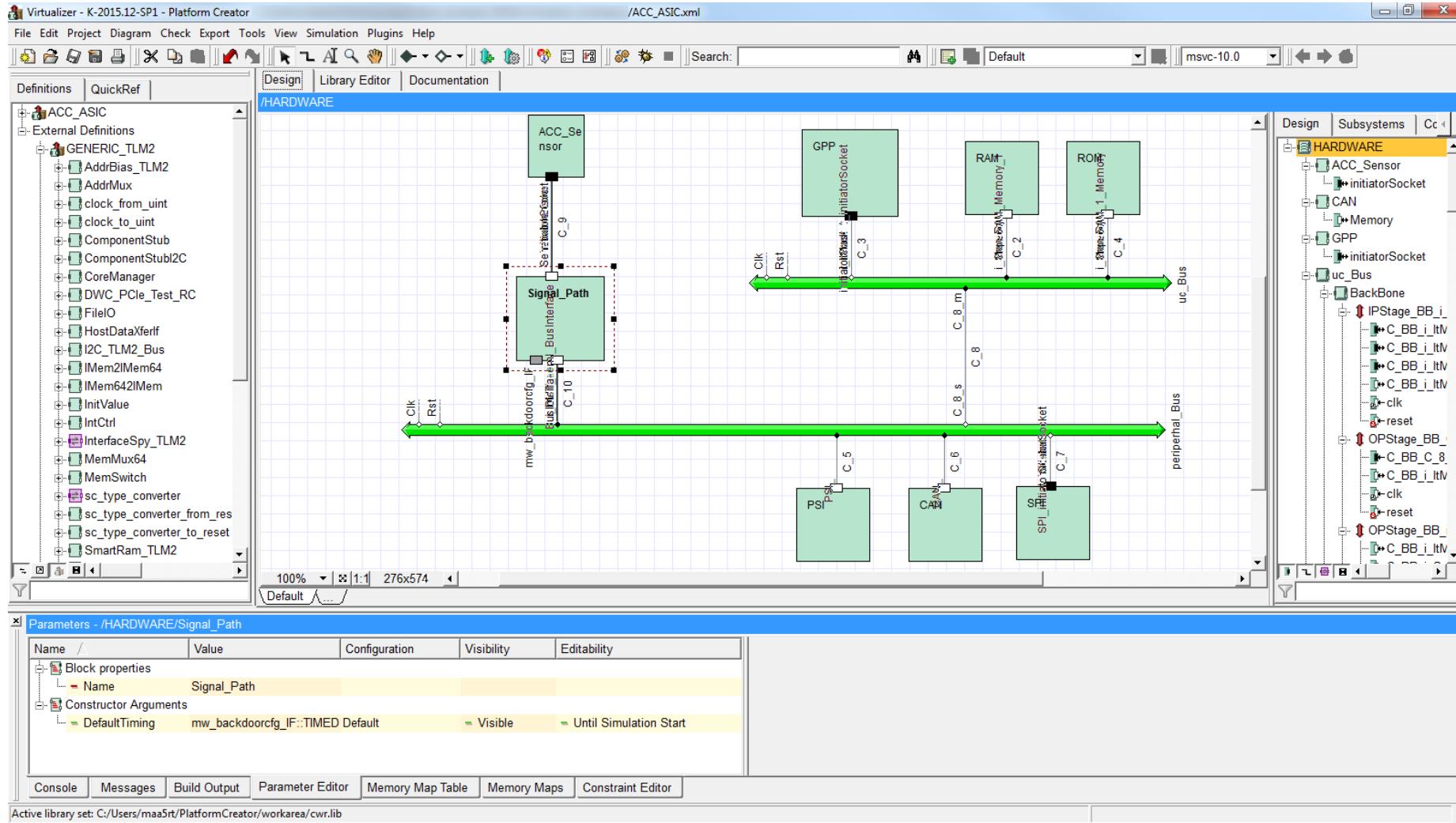
Integration into VP and Simulation

SystemC Module in Virtualizer



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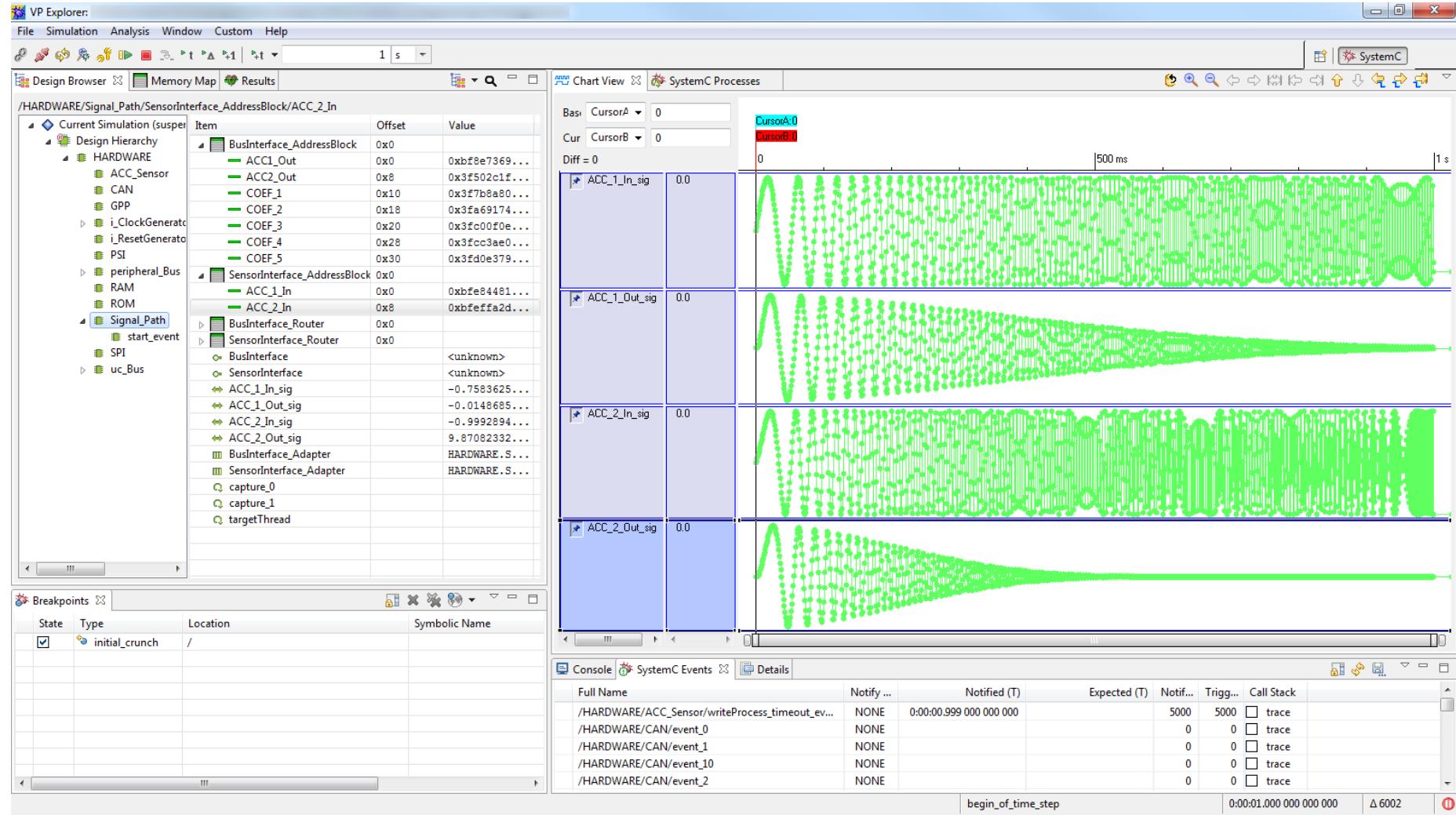
Integration into VP and Simulation

Simulation in VPExplorer



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Summary & Conclusion



Summary

Bosch Workflow

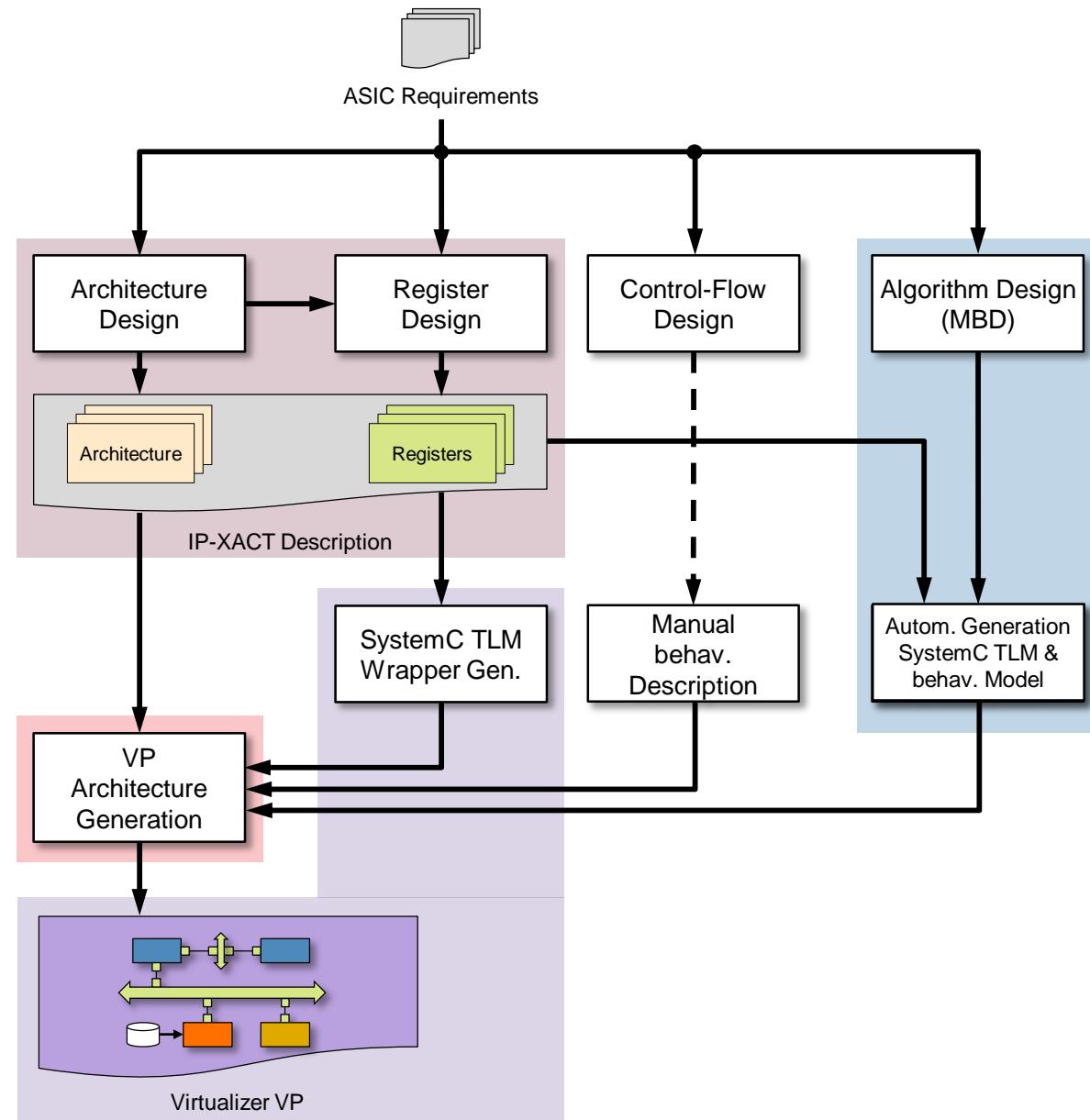


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SYNOPSYS
Silicon to Software™



Summary & Conclusion



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- Developed method:
Automated integration of Simulink signal processing behaviour modules into Virtualizer VPs
- Generated artefacts:
 - Functional core
 - SystemC TLM2.0 Wrapper with SCML registers based on IP-XACT description
 - Code connecting wrapper and functional core
- Benefits:
 - Increase of efficiency for integration signal processing behaviour into VPs
 - Earlier availability of functional VPs of signal processing ASICs
 - Inherent consistency between Simulink model and VP



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Thank You

