

COMPUTER TECHNOLOGY

PRACTICAL SESSION P5 (LOGISIM)

DESIGN OF SEQUENTIAL CIRCUITS

Given the state diagram of Figure 1:

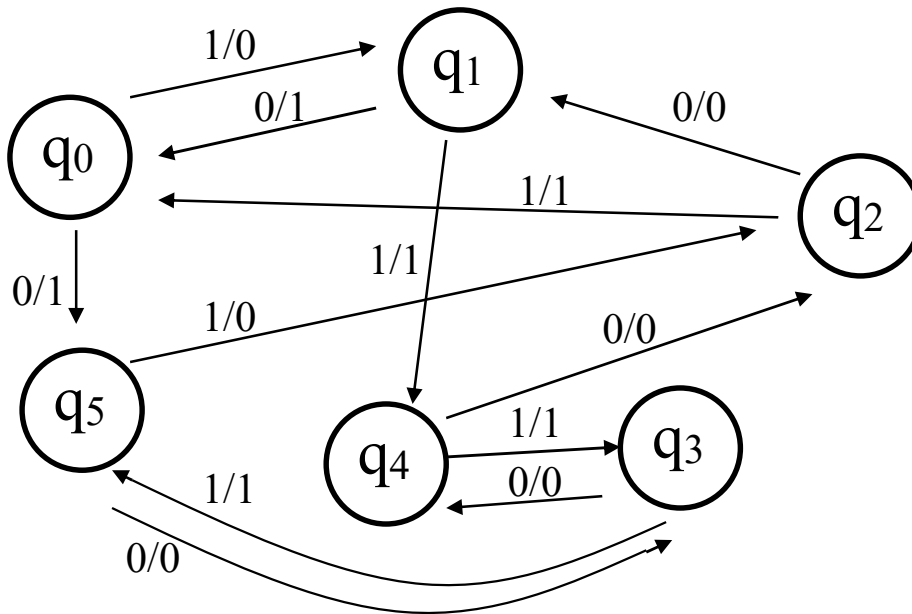


Figure 1

Design the sequential circuit using the following flip flops:

- T FF for the most significant flip-flop (T_2).
- D FF for the middle flip-flop (D_1).
- JK FF for the least significant flip-flop (J_0K_0).

Implement T_2 using logic gates, D_1 at the discretion of the student, and J_0K_0 using an active-high output DEC 4x16. The output S must be implemented using a MUX 4x1. Design and simulate the circuit with Logisim.

Check that if $x=0$ the state sequence is:

$q_0 \rightarrow q_5 \rightarrow q_3 \rightarrow q_4 \rightarrow q_2 \rightarrow q_1 \rightarrow q_0$

Check that if $x=1$ the state sequence is:

$q_0 \rightarrow q_1 \rightarrow q_4 \rightarrow q_3 \rightarrow q_5 \rightarrow q_2 \rightarrow q_0$

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REMARK 1: The state encoding is shown in Table 1.

	Q₂	Q₁	Q₀
q ₀	0	0	0
q ₁	0	0	1
q ₂	0	1	0
q ₃	0	1	1
q ₄	1	0	0
q ₅	1	0	1

Table 1

REMARK 2: The state of the circuit must be visualized using 3 orange LEDs and a display (take *Hex Digit Display*), corresponding to the outputs of the three flip-flops. These LEDs must be placed horizontally, in the following order: Q₂Q₁Q₀. The output S must be visualized using a green LED.

FILL OUT THE TABLE BELOW:

E	Q₂(t)	Q₁(t)	Q₀(t)	Q₂(t+1)	Q₁(t+1)	Q₀(t+1)	T₂	D₁	J₀	K₀	S
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
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