

## Lab exam

### Combinational Circuits

The scoring of this lab exam is 1,2 points

#### Important information

Download the files `LabExam1_eng.doc` and `LabExam1_eng.circ` from Moodle and rename them as `A_surname_name.doc` and `A_surname_name.circ`, respectively. For example, `A_martinez_pedro.doc` and `A_martinez_pedro.circ`.

After finishing the lab exam, the student must submit to Moodle the file `A_surname_name.zip` (or `.rar`) including:

- 1) The file `A_surname_name.doc` with the responses of Part 1.
- 2) The file `A_surname_name.circ` with the designs corresponding to subcircuits of Parts 2 and 3 and the *main* circuit.

Don't use switches for constant signals, instead use Logisim constants 0 and 1 (in *Wiring*).

#### Lab exercise

A particular function  $F(A,B,C,D)$  has been assigned to each student according the ID number in `FuncionF.pdf`. In the first column of `FuncionF.pdf` the student can identify the row corresponding to his/her ID. The rest of the columns on the right contain the positions of the truth table in which F takes value 1. This search can be easily done by typing `<Ctrl + f>`.

#### Part 1 (20%). (Write your answers in the next page)

- a) Find the simplified expression of F as SOP
- b) Find the simplified expression of F as POS. using Karnaugh maps (fill the K-maps and write the corresponding expressions):

#### Part 2 (30%). Design in Logisim subcircuits 2.1, 2.2 and 2.3

- a) (*subcircuit 2.1*). Digital circuit of F using AND/OR/NOT gates.
- b) (*subcircuit 2.2*). Digital circuit of F using NOR gates.
- c) (*subcircuit 2.3*). Digital circuit of F using an active-high output DEC 4x16 and the necessary 3-input gates. Take the decoder from the Logisim library.

#### Part 3 (50%). Design in Logisim subcircuits 3.1, 3.2 and main:

- a) (*subcircuit 3.1*) Digital circuit of F using a MUX 8x1 and the necessary gates. Take the selection inputs freely.(20%)
- b) (*subcircuit 3.2*) Digital circuit of F using several DEC 2x4 and the necessary gates. Important remark: put the property *Disabled Output* of the decoders to Zero. (20%)
- c) (*main*) Design the *main* circuit that integrate the aforementioned 5 subcircuits with common inputs A, B, C and D, and include a display that visualizes the number represented in the binary code ABCD.(10%)

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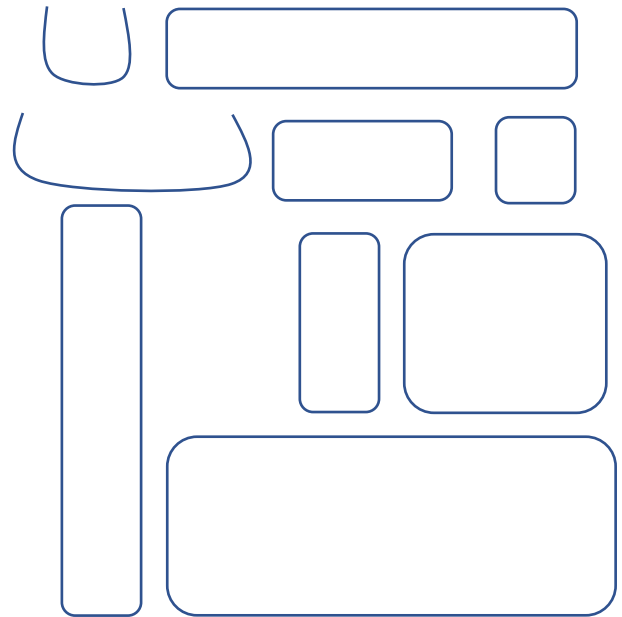
#### Part 1 (20%). Write your answers in this page

	Positions in which function F takes value 1					
2	5	7	8	11	14	15

- a) Find the simplified expression of F as SOP. Fill the Karnaugh Map and takes the necessary figures (copy, paste, drag and rotate (if necessary)) for grouping:

Write here the expression  $F(A,B,C,D) = (A'B'CD') + (AB'C'D') + (A'BD) + (ABC) + (ACD)$

		CD			
		00	01	11	10
F	AB	00			
	00				1
	01		1	1	
	11			1	1
	10	1		1	



- a) Find the simplified expression of F as POS. Fill the Karnaugh Map and get the necessary figures (copy, paste, drag and rotate (if necessary)) for grouping:

Write here the expression  $F(A,B,C,D) =$

$(A+B+C)(A+B+D')(A+B'+C'+D)(A'+B+C'+D)(B'+C+D)(A'+B'+C)(A'+C+D')$

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		CD			
<b>F</b>		00	01	11	10
AB	00	0	0	0	
	01	0			0
	11	0	0		
	10		0		0