COMPUTER TECHNOLOGY PRACTICAL SESSION P6 (LOGISIM) REGISTERS AND COUNTERS

The objective of this practical session is to design and simulate the main sequential modules: registers and counters.

PART 1.

Design the universal shift register circuit shown in Figure 1. Verify the performance of the circuit by following the chronogram below. Select the "Tick Once" mode in order to see the changes in the circuit as a new clock cycle comes and use buttons for asynchronous inputs. Use also two displays to show input E and the content of the register, and a LED for the serial output.

Universal Shift Register S1^A B C D m1 m1 MUX 150 S0 Preset Output CK Clear Valu Name: D CK ■ Preset M₁M₀ 00 shift right D **iii⊶** Clear 01 Load 0 1 0 **I** M[0..1] ΗO 1 3 1 11 shift left Н7 7 **□**F E[0..2] Output D H0Content 0 3 0 3 6

PART 2.

Design a circuit that shows the sequence of numbers 0, 2, 4, 2, 0, 2, 4, 2, 0 To do this, design first a 2-bit counter using T FFs and then, a suitable decoder circuit, which will be connected to the display (*Hex Digit Display*).

