ASMEDIA TECHNOLOGY INC

ASM2364 Data Sheet

SuperSpeed USB 20Gbps to PCIe Gen 3x4 NVMe Bridge

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	April 9, 2019	Initial Release
0.2	April 19, 2019	Corrected typos and updated wordings in Power on sequence Updated Pin Descriptions for VCC33O and VCC5IN Updated General Description Updated Features Updated Section 6.3.2
0.3	June 3, 2019	Updated the title Updated General Descritption Updated Features Updated Power consumption specification Updated Chip temperature calculation Updated pin description of VBUS.
0.4	July 1, 2019	Corrected typos in Power Consumption Specification
		Updated the Recommended Operating Conditions
		Updated Package Information
0.5	July 31, 2019	Updated ASM2364 Pinout and Pin Descriptions

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1. General Description

ASM2364 is an ASMedia PCI Express (Downstream Port) to USB3.2 (Upstream Facing Port) bridge, featuring interface of PCI Express Gen3 x4 and one USB3.2 Gen2x2 device port, doubling the bandwidth up to 20Gbps by expanding PCI Express Gen3 bus and USB lanes. It is used for external USB to NVM Express SSD application without additional driver. ASM2364 USB to NVMe Bridge can achieve over 2000MB/s throughput with excellent performance. This new chip integrates two USB 10Gbps PHYs and Configuration Channel bus for Type-C connector, also supporting PCI Express M.2 socket, CF Express, and U.2 form factor. ASM2364 supports advanced power saving features through USB and PCI Express Link power management and chip power management, compliant with NVM Express Base Specification Revision 1.3c, PCI Express Base Specification Revision 3.1a, USB3.2 Specification Revision 1.0, and USB Type-C Specification Release 1.3.

ASM2364 is highly integrated with ASMedia USB3.2 Gen2x2 PHYs and market proven PCI Express Gen3 self-designed PHYs, supplied by 3.3V and 1.05V voltage power source, and driven by local 25MHz crystal in a compact QFN88 10x10 RoHS Green package, supporting multiple GPIO pins for customization. Target applications are USB3.2 Gen2x2 to NVM Express for high performance external SSD storages, card readers, on-board storage on PCs, laptops, servers, docking stations, embedded systems etc.

2. Features

General Feature

- ◇ USB to PCI Express NVMe SSD bridge
- ◇ Integrated two USB 10Gbps PHYs
- ◇ Integrated CC Logic for Type-C application
- ◇ Support SPI interface with external ROM for customized RAM code
- ◇ Support I2C and GPIOs and UART interface
- ◇ Internal 5V to 3.3V LDO
- ◇ Local 25MHz crystal

Universal Serial Bus Feature

- ◇ Support up to USB3.2 Gen2x2 backward compatible with USB 3.1
- ◇ Support BOT and UAS Protocol
- ◇ Support USB Link power management
- ◇ Support USB Hot Plug
- ◇ Support Spread Spectrum Clock Control
- ◇ Support unmap command set
- ◇ Support SCSI vendor specific command set
- ◇ Compliant with Universal Serial Bus 3.2 Revision 1.0
- ◇ Compliant with USB Type-C specification Release 1.3

PCI Express Feature

- ◇ Support up to PCI Express Gen3 x4
- ◇ Support PCI Express NVMe SSD without driver
- ◇ Support Spread Spectrum Clock Control
- ◇ 100MHz differential reference clock output
- ◇ Support various types of PCI Express socket including M.2, U.2, and CF Express.
- ◇ Support PCI Express Link power management
- ◇ Compliant with PCI Express Base Specification Revision 3.1a
- ◇ Compliant with PCIe M.2 Specification Revision 1.0

NVM Express Feature

- ◇ Support NVMe power management
- ◇ Support NVMe: SCSI Translation Reference Revision 1.5
- ◇ Support TRIM command set
- ◇ Support NVMe Error Reporting & Recovery
- ◇ S.M.A.R.T drive monitoring
- ◇ Compliant with NVM Express Base Specification Revision 1.3c

Package Type

- ◇ Green Package 10x10 mm^2 QFN 88 (Pb-free)
- ◇ RoHS Compliance

3. Functional Diagram

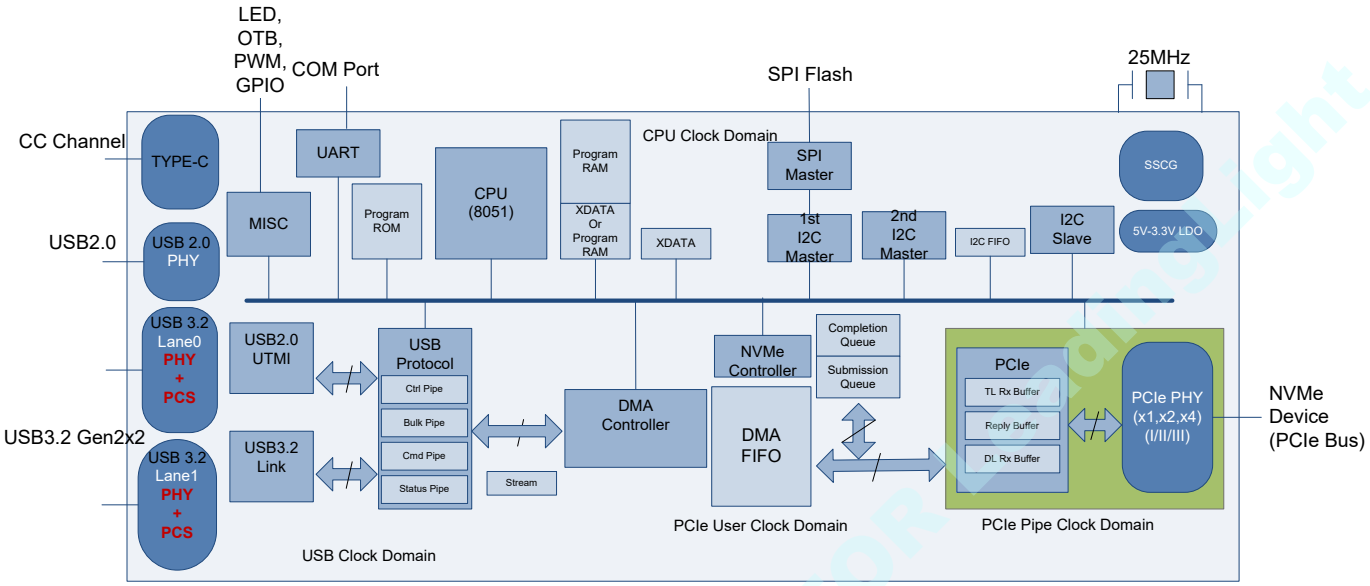


Figure 1: Functional Diagram of ASM2364

4. Pinout Diagrams

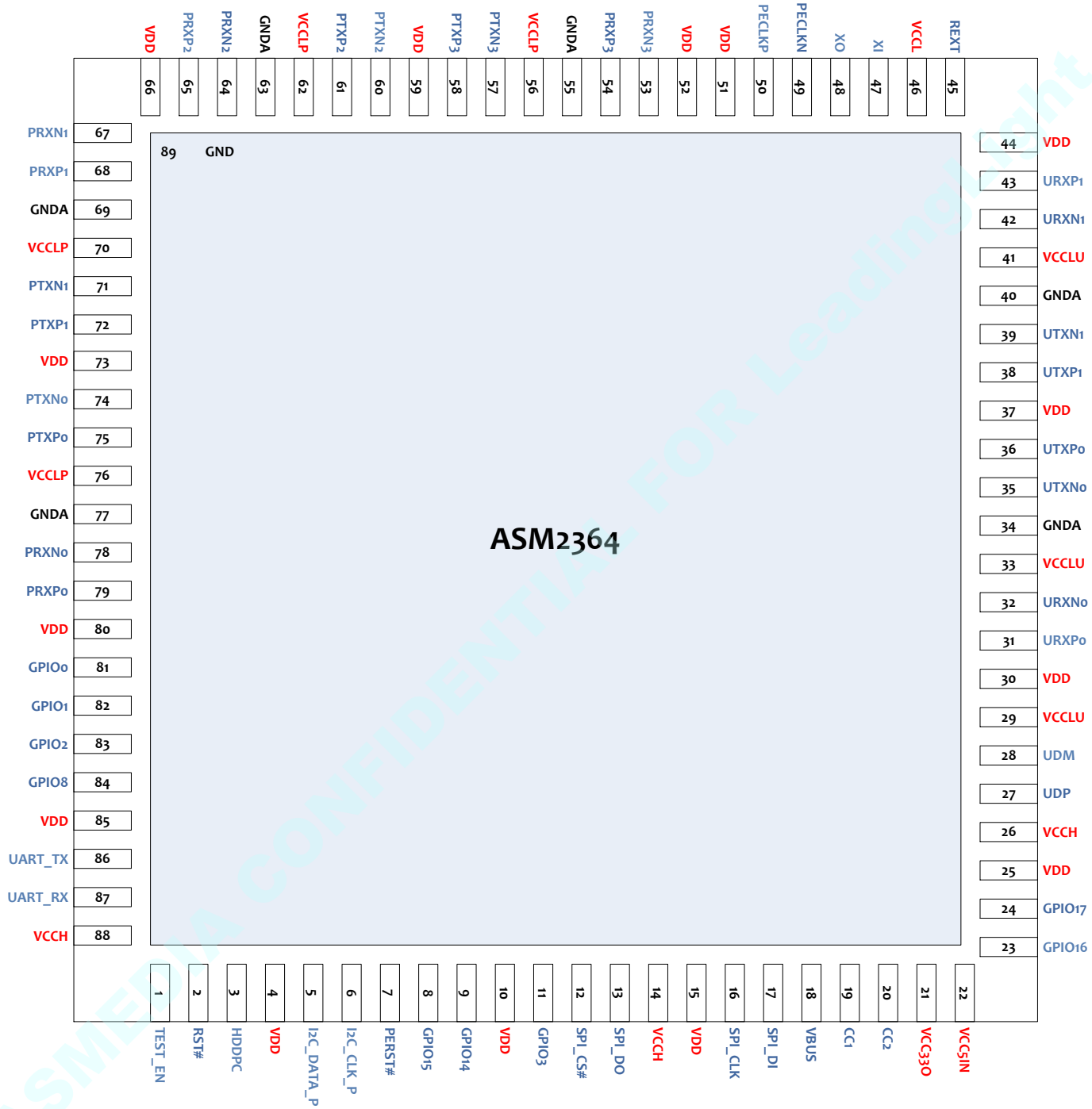


Figure 2: ASM2364 pinout

5. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin name	Pin NO.	TYPE	Power	Descriptions
UDP	27	IO	VCCH	Positive Signal of USB2.0 on Type-C
UDM	28	IO	VCCH	Negative Signal of USB2.0 on Type-C
UTXP0	36	Di O	VCCLU	Positive Signal of SuperSpeed USB Lane 0 Transmitter for Type-C Configuration Channel 1
UTXN0	35	Di O	VCCLU	Negative Signal of SuperSpeed USB Lane 0 Transmitter for Type-C Configuration Channel 1
UTXP1	38	Di O	VCCLU	Positive Signal of SuperSpeed USB Lane 1 Transmitter for Type-C Configuration Channel 2
UTXN1	39	Di O	VCCLU	Negative Signal of SuperSpeed USB Lane 1 Transmitter for Type-C Configuration Channel 2
URXP0	31	Di I	VCCLU	Positive Signal of SuperSpeed USB Lane 0 Receiver for Type-C Configuration Channel 1
URXN0	32	Di I	VCCLU	Negative Signal of SuperSpeed USB Lane 0 Receiver for Type-C Configuration Channel 1
URXP1	43	Di I	VCCLU	Positive Signal of SuperSpeed USB Lane 1 Receiver for Type-C Configuration Channel 2
URXN1	42	Di I	VCCLU	Negative Signal of SuperSpeed USB Lane 1 Receiver for Type-C Configuration Channel 2
VBUS	18	I	VCCH	USB VBUS input. This is a **5V tolerant** pin.
CC1	19	I	VCCH	Configuration Channel 1 for USB Lane 0 on Type-C
CC2	20	I	VCCH	Configuration Channel 2 for USB Lane 1 on Type-C
PECLKN	49	Di O	VCCLP	Negative Signal of PCI Express Differential Clock
PECLKP	50	Di O	VCCLP	Positive Signal of PCI Express Differential Clock
PRXN1	67	Di I	VCCLP	Negative Signal of PCI Express Lane 1 Receiver
PRXP1	68	Di I	VCCLP	Positive Signal of PCI Express Lane 1 Receiver
PRXN0	78	Di I	VCCLP	Negative Signal of PCI Express Lane 0 Receiver
PRXP0	79	Di I	VCCLP	Positive Signal of PCI Express Lane 0 Receiver
PTXN1	71	Di O	VCCLP	Negative Signal of PCI Express Lane 1 Transmitter
PTXP1	72	Di O	VCCLP	Positive Signal of PCI Express Lane 1 Transmitter
PTXN0	74	Di O	VCCLP	Negative Signal of PCI Express Lane 0 Transmitter
PTXP0	75	Di O	VCCLP	Positive Signal of PCI Express Lane 0 Transmitter
PRXN3	53	Di I	VCCLP	Negative Signal of PCI Express Lane 3 Receiver
PRXP3	54	Di I	VCCLP	Positive Signal of PCI Express Lane 3 Receiver
PRXN2	64	Di I	VCCLP	Negative Signal of PCI Express Lane 2 Receiver
PRXP2	65	Di I	VCCLP	Positive Signal of PCI Express Lane 2 Receiver
PTXN3	57	Di O	VCCLP	Negative Signal of PCI Express Lane 3 Transmitter
PTXP3	58	Di O	VCCLP	Positive Signal of PCI Express Lane 3 Transmitter
PTXN2	60	Di O	VCCLP	Negative Signal of PCI Express Lane 2 Transmitter
PTXP2	61	Di O	VCCLP	Positive Signal of PCI Express Lane 2 Transmitter
PERST#	7	O	VCCH	Reset Signal for PCI Express interface
RST#	2	I	VCCH	Power on Reset

TEST_EN	1	I	VCCH	Test enable pin, internal weak pull down
I2C_DATA_P	5	IO	VCCH	I2C data, internal weak pull high
I2C_CLK_P	6	IO	VCCH	I2C clock, internal weak pull high
GPIO0	81	IO	VCCH	GPIO0, internal weak pull high
GPIO1	82	IO	VCCH	GPIO1, internal weak pull high
GPIO2	83	IO	VCCH	GPIO2, Internal weak pull high
GPIO3	11	IO	VCCH	GPIO3, internal weak pull high
SPI_CS#	12	IO	VCCH	GPIO4, SPI Chip Select for external SPI flash, internal weak pull high
SPI_DO	13	IO	VCCH	GPIO5, SPI data output for external SPI flash, as strapping pin for "SKT_DET" when power on. Please refer to strapping table. Internal weak pull high
SPI_CLK	16	IO	VCCH	SPI clock output for external SPI flash, I2C_CLK, internal weak pull high
SPI_DI	17	IO	VCCH	SPI data input for external SPI flash, I2C_DATA, internal weak pull high
GPIO8	84	IO	VCCH	GPIO8, CLKREQ#, internal weak pull high
GPIO14	9	IO	VCCH	GPIO14, internal weak pull high
GPIO15	8	IO	VCCH	GPIO15, internal weak pull high
GPIO16	23	IO	VCCH	GPIO16, internal weak pull high
GPIO17	24	IO	VCCH	GPIO17, internal weak pull high
UART_TX	86	O	VCCH	UART transmitter, as strapping pin for "MEMREPAIR" when power on. Internal weak pull high
UART_RX	87	I	VCCH	UART receiver, Internal weak pull high
HDDPC	3	O	VCCH	Power control for NVMe SSD, internal weak pull high
REXT	45	I	VCCH	External resistor 12.1 kohm+/-1%
XI	47	I	VCCH	Crystal Input
XO	48	O	VCCH	Crystal Output
VCC5IN	22	P	VCC5IN	Regulator 5V Input for VCC33O **Please keep this pin powered by 3.3V when internal regulator is not used.**
VCC33O	21	P	VCCH	Regulator output to supply VCCH **Please keep this pin powered by 3.3V when internal regulator is not used.**
VDD	4, 10, 15, 25, 30, 37, 44, 51, 52, 59, 66, 73, 80, 85	P	VDD	Core power supply input
VCCL	46	P	VCCL	Low voltage VCC power input
VCCLU	29, 33, 41	P	VCCL	Low voltage VCC power input for USB
VCCLP	56, 62, 70, 76	P	VCCL	Low voltage VCC power input for PCI Express
VCCH	14, 26, 88	P	VCCH	High voltage VCC power input
GNDA	34, 40, 55, 63, 69, 77	G		Analog Ground
GND	89	G		Digital Ground

Strapping Table

Function control for PCIe Hot plug support

GPIO5	SKT_DET
H	Support
L	Not support

Function control for internal memory repair

UART_TX	MEMREPAIR
H	Enable
L	Disable

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses the below parameter listed under absolute maximum rating may cause the device permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over those parameter in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal exhibit voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply	-0.5 ~ VCC+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

6.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
V_{CCH}	High voltage VCC power supply	3.0	3.3	3.6	V	
V_{CCHO}	High voltage VCC power supply	3.0	3.3	3.6	V	
V_{CCL}	Low voltage VCC power supply	2.3	2.5	2.7	V	
V_{CCLU}	Low voltage VCC power supply for USB	2.3	2.5	2.7	V	
V_{CCLP}	Low voltage VCC power supply for PCIe	2.3	2.5	2.7	V	
V_{DD}	Core power supply	1.00	1.05	1.1	V	
T_C	Operating Case Temperature	0		85	ºC	
T_J	Silicon Junction Temperature	0	25	120	ºC	
HBM	Human Body mode	4			KV	
MM	Machine mode	150			V	

6.2.1 Chip Temperature (T_J, T_C) Calculation

Symbols	Parameter	How to get?
T_A	Ambient temperature	Measure temperature around chip
T_J	Operating junction temperature	$T_J = \Theta_{JA} * Power + T_A$
T_C	Operating case temperature	$T_C = T_J - \Psi_{JT} * Power$
Θ_{JA}	Junction to Ambient thermal resistance	22.7 (provided by package vendor)
Θ_{JC}	Junction to case thermal resistance	4.4 (provided by package vendor)
Ψ_{JT}	Junction to top thermal characterization	0.08 (provided by package vendor)
Power	Chip power consumption	Measure chip power consumption

- Thermal test board condition, please refer to JEDEC JESD51-5
- Thermal test method environmental conditions refer to JESD51-2
- Example: If chip power consumption is 1.8W; T_A= 44 ^{0}C
  T_J = 22.7 *1.8 + 44 = 84.86^{0}C < 120^{0}C
  T_C =84.86 – 0.08 * 1.8 =84.7 ^{0}C < 85^{0}C

6.3 AC/DC Characteristics

6.3.1 PCI Express Electrical Specification

(Refer to PCI Express Base Specification Rev. 3.1a)

6.3.2 USB3.2 Electrical Specification

(Refer to Universal Serial Bus 3.2 Specification Rev. 1.0)

6.3.3 USB2.0 Electrical Specification

(Refer to Universal Serial Bus Specification Rev. 2.0)

6.3.4 DC Electrical Characteristics for digital pins

(Including VBUS, PERST, I2C, UART, HDDPC and GPIOs)

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage Level	2.0			V
V_{IL}	Input Low Voltage Level			0.8	V
V_{HYS}	Input Hysteresis	0.32	0.37	0.4	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.4	1.6	1.8	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1	1.23	1.4	V
V_{OH}	Output High Voltage Level	2.4			V
V_{OL}	Output Low Voltage Level			0.4	V
I_{OH}	Output Driving Current while V_{OH}	12			mA
I_{OL}	Output Driving Current while V_{OL}	12			mA
R_{UP}	Internal Pull-up resistance while Vin=0V	65	96	140	KΩ
	Internal Pull-up resistance while Vin=VCC/2 V	38	56	81	KΩ
R_{DN}	Internal Pull-down resistance while Vin=VCC	59	96	142	KΩ
	Internal Pull-down resistance while Vin=VCC/2 V	35	55	79	KΩ
I_{IL-UP}	Input pull-up leakage current after Vin is read, Rup is off & Iil < 1uA when VIN=0	21	34.4	56	uA
	Input pull-up leakage current after Vin is read, Rup is off & Iil < 1uA when VIN=VCC/2	18	29.4	47	uA
I_{IL-DN}	Input pull-down leakage current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC	21	34.5	60	uA
	Input pull-down leakage current after Vin is read, Rdn is off & Iil < 1uA when VIN=VCC/2	18	30	50	uA

6.3.4 DC Electrical Characteristics for RST# pin

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage Level	2.6			V
V_{IL}	Input Low Voltage Level			1.4	V
V_{HYS}	Input Hysteresis	0.21	0.23	0.25	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.9	2.2	2.55	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1.65	1.97	2.35	V
Input	Input pull-up leakage current while Vin=0V			1	mA

6.3.5 External Crystal Electrical Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
f_{XTAL}	Frequency		25		MHz
$\triangle f_{XTAL}$	Long Term Stability (at 250C)	-30		30	ppm
t_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

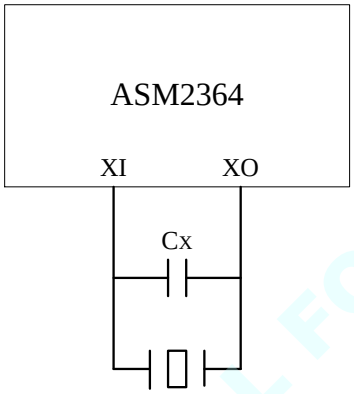


Figure 3: Differential Crystal Design

6.3.6 Differential Clock Oscillator Electrical Specification

Note: The table describes the specification of clock with external 25MHz crystal. Please refer to figure 3.

Symbols	Parameter	Min.	Typ.	Max.	Units
f_{XTAL}	Frequency		25		MHz
$\triangle f_{XTAL}$	Long Term Stability (at 250C)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		10		pF
C_{TATAL}	Total external equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	pF
R_{TOTAL}	Total external equivalent Series Resistance from XI pin to XO pin (Differential mode)			60	Ω

6.3.7 PCI Express 100MHz Output Clock Electrical Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{OH}	Differential Output High Voltage	150			mV
V_{OH}	Differential Output Low Voltage			-150	mV
V_{CROSS}	Absolute crossing point voltage	250		550	mV
t_{CROSS_DELTA}	Variation of V_{CROSS} over all rising clock edges			140	mV
t_{PERIOD_AVG}	Average clock period accuracy	-300		300	ppm
t_{CCJ}	Cycle to Cycle Jitter			150	Ps
t_{DC}	Reference Duty Cycle	40		60	%
RT_{RISING}	Rising Edge Rate	0.6		4.0	V/ns
$RT_{FALLING}$	Falling Edge Rate	-4.0		-0.6	V/ns

6.3.8 Internal Linear Regulator Electrical Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IN}	Input Voltage Range	4.0	5.0	5.5	V
V_{OUT}	Output Voltage Range	3.0	3.3	3.6	V
I_{MAX}	Maximum capacity of current			90	mA

6.3.9 Power Consumption Specification

Symbols	Parameter	Max.	Units
I_{CCHMAX}	Maximum Current consumption of V_{CCH}	10.1	mA
I_{CCLMAX}	Maximum Current consumption of V_{CCL}	314.11	mA
I_{DDMAX}	Maximum Current consumption of V_{DD}	909	mA

7. Power on Sequence

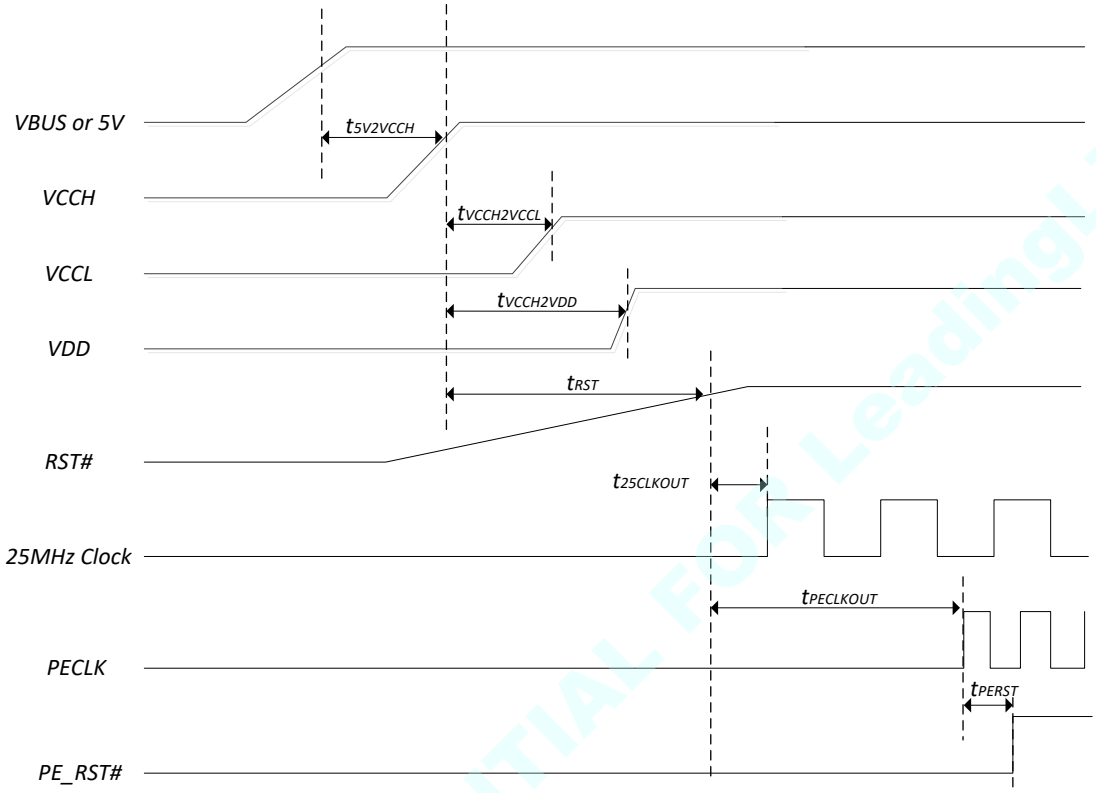
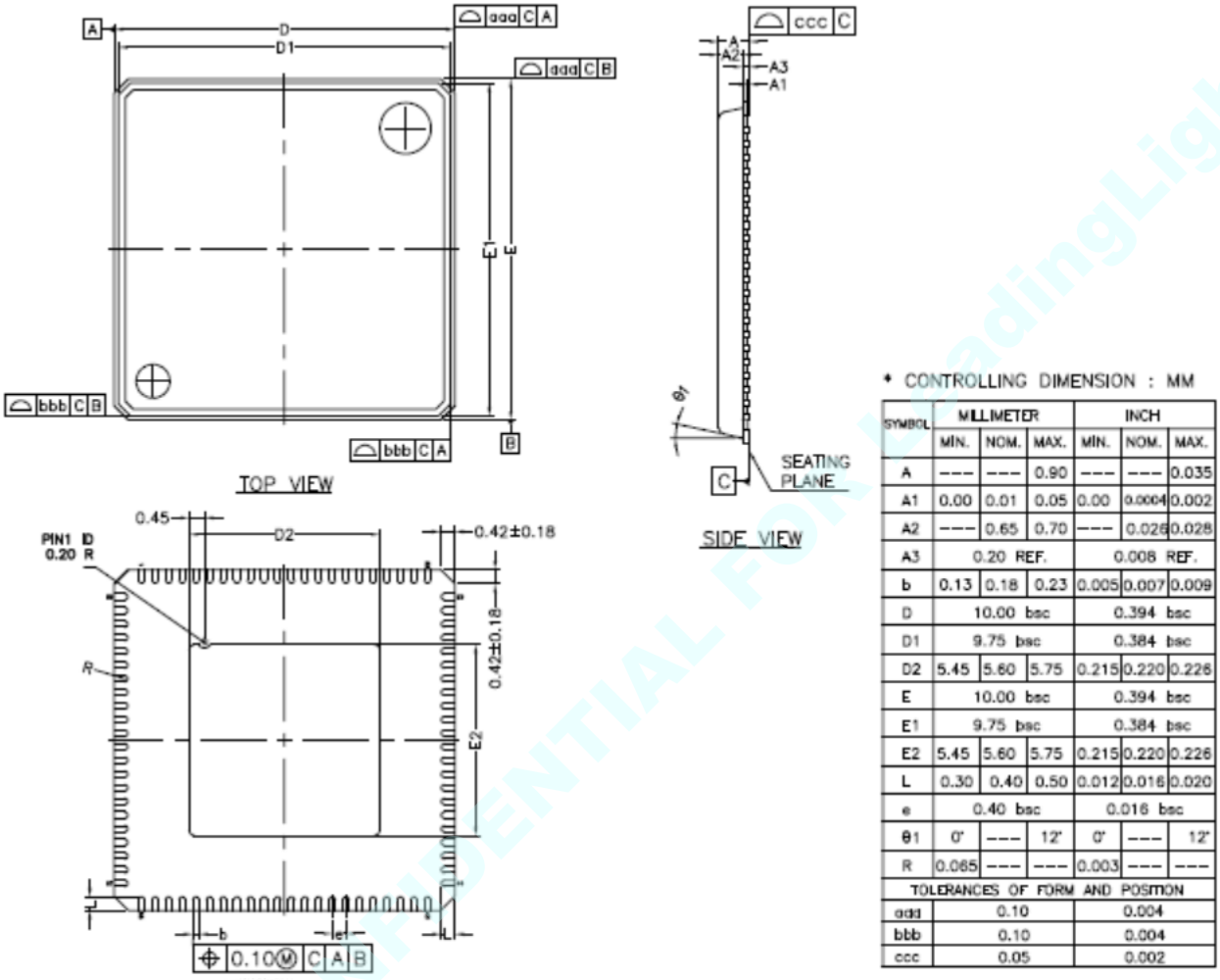


Figure 4: waveform of power on sequence

Symbols	Parameter	Min.	Typ.	Max.	Units
$t_{5V2VCCH}$	V_{CCH} (90%) available after 5V or VBUS (90%) available		3	6	ms
$t_{VCCH2VCCL}$	V_{CCL} (90%) available after V_{CCH} (90%) available	0	5	10	ms
$t_{VCCH2VDD}$	V_{DD} (90%) available after V_{CCH} (90%) available			90	ms
t_{RST}	RST (90%) ready after V_{CCH} (90%) available	0			ms
$t_{25CLKOUT}$	25MHz clock available after RST#(90%) assertion			10	ms
$t_{PECLKOUT}$	PCI Express Reference Clock output after RST#(90%) assertion	100			ms
t_{PERST}	PCI Express Reset (90%) assertion after PCI Express Reference Clock output	0			ms

8. Package Information



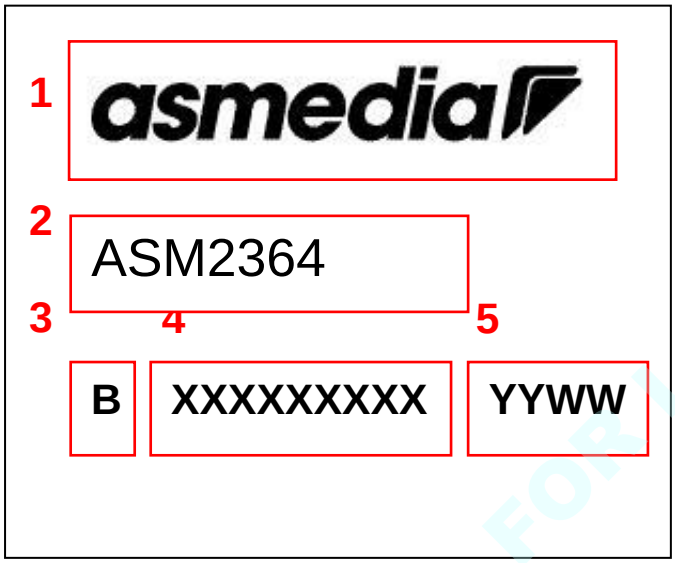
* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3		0.20 REF.			0.008 REF.	
b	0.13	0.18	0.23	0.005	0.007	0.009
D		10.00 bsc			0.394 bsc	
D1		9.75 bsc			0.384 bsc	
D2	5.45	5.60	5.75	0.215	0.220	0.226
E		10.00 bsc			0.394 bsc	
E1		9.75 bsc			0.384 bsc	
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.30	0.40	0.50	0.012	0.016	0.020
e		0.40 bsc			0.016 bsc	
θ1	0°	---	12°	0°	---	12°
R	0.065	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.13 AND 0.23 mm FROM TERMINALTIP.(REFER TO SPEC "b")
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING. (TIN PLATING)
9.APPLIED ONLY TO TERMINALS.(TIN PLATING)
10.PACKAGE CORNERS UNLESS OTHERWISE SPECIFIED ARE R0.175±0.025 mm.

Figure 5: Mechanical Specification

9. Top Marking Information



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4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code