3D NAND Flash: Gen6 X4 1Tb 4-Plane

July 20, 2022
Preview, Revision 0.1

Marketing Part Numbers

SKU	Configuration
TBD	TBD

Western Digital Proprietary and Confidential

SanDisk®
a Western Digital brand

DRAFT Rev. 0.1 7/20/22

Table of Contents

DRAFT Rev. 0.1 7/20/22

DRAFT Rev. 0.1 7/20/22

1 Features

Table 1: Device Features

Feature	Description	
Organization		
Memory cell array (per plane)	18,976 x 8 bits x 3240 pages x 699 blocks	
Planes per die	4	
Block size	QLC: 50.625MB (3240 pages = 162 WL × 5 strings × 4bpc)	SLC: 12.65625MB (810 pages = 162 WL × 5 strings × 1bpc)
Blocks per die	2796	
Shared strings	5	
Wordlines (WLs) per block	162	
Page size	18,976 bytes (16,384 + 2592 ECC)	
Pages per block	QLC: 3240 pages	SLC: 810 pages
Number of valid blocks (N_{VBD}) from factory		
Minimum average number of valid blocks per die in package	TBD	
Modes		
Array-independent modes	**Array-dependent modes***	
ID Read Set/Get Features Status Read Reset operation	Dynamic Read QLC Page Read Cache Read SLC Read	QLC Program Cache Program SLC Program
	QLC Block Erase SLC Erase	
	*These modes are functional in single- or multi-plane operations.	
Access time		
tR: Cell array to register (typ)	Lower page: Middle page: Upper page: Top page:	TBD TBD TBD TBD
	SLC:	TBD
Program/Erase time		
Program (typ)	QLC: = typical total programming QLC 1st cycle: QLC 2nd cycle:	 TBD TBD
	SLC: per page	TBD
Single Block Erase (typ)	per block	TBD
Power supply		
	V_{CC}: 2.35–3.6V	V_{CCQ}: 1.2V (1.14–1.30V)

Table continues on next page

Table 1: Device Features (cont'd)

Feature	Description	
I/O Interface		
Toggle Mode data transfer rate per pin	DDR 5.0 Max: 1000 MHz (2000 Mbps) DDR 4.0 Max: 600 MHz (1200 Mbps)	DDR 3.0 Max: 400 MHz (800 Mbps) DDR 2.0 Max: 266 MHz (533 Mbps)
	NOTE: DDR1 is ***not*** supported in this device	
SDR data transfer rate per pin	**NOTE:** SDR is ***not*** supported in this device	
Operating temperature		
T_{CASE}	0°C to 70°C	
Operating current (typical)		
Read (random data)	QLC: TBD	SLC: TBD
Program (avg)	QLC: TBD	SLC: TBD
Erase (avg)	QLC: TBD	SLC: TBD
Standby:	TBD max per die	
Package		
BGA	132-ball BGA: die-count TBD	TBD

1.1 Part Numbering: TBD

DRAFT Rev. 0.1 7/20/22

2 Device Overview

SanDisk® 3D NAND Flash: Gen6 X4 1Tb 4-Plane memory devices are available in BGA packages. All possible configurations may not be available.

This device supports Toggle Mode interface (I/F) speeds for:

- DDR2: up to 266 MHz (533 Mbps)
- DDR3: up to 400 MHz (800 Mbps)
- DDR4: up to 600 MHz (1200 Mbps)
- DDR5: up to 1000 MHz (2000 Mbps)

Toggle Mode is a NAND Flash interface for high-performance applications that support data-in (D_{IN}) and data-out (D_{OUT}) operations on both the rising and falling edges of the data strobe (DQS) signal.

Toggle Mode NAND implements “Double Data Rate” operation and provides a high data-transfer rate based on the high-speed Toggle Mode interface.

Differential signals (DQS, DQSn, REn, RE) are used in DDR2, DDR3, DDR4, and DDR5 Toggle Mode.

2.1 DDR-Based Termination

DDR2, DDR3, DDR4, and DDR5 use the Center-Tapped Termination (CTT) interface (I/F) which is symmetrical with respect to the V_{CCQ} power supply level and the ground level.

DDR5 supports both the CTT interface and the Low-Tapped Termination (LTT) interface, also known as Low-Voltage Swing Termination Logic (LVSTL).

For additional discussion of the CTT and LTT I/Fs and their specifications, see these sections:

- "6.1 Toggle Mode Interface" on page 37 through "6.1.1 Toggle Mode Interface Switching in DDR5" on page 39
- "8.3.5 Center-Tapped Termination (CTT) Specifications" on page 52 **and** "8.3.6 Low-Tapped Termination (LTT) Specifications" on page 53 (LTT specs)
- "8.6 I/O Drive Strength" on page 66
- "14.1 Toggle Mode-Specific Setting (02h)" on page 121 **through** "14.4 Internal VREFQ Setting (23h)" on page 128

NOTE: From this point on:

- Single-level-cell (SLC) and four-level-cell (QLC) operations are most often referred to by their respective acronyms, SLC and QLC. The term four-bits-per-cell (4bpc) may also occur and is used interchangeably with QLC.
- Text in this blue indicates an active link to cross-referenced content.

3 Device Specifications

3.1 Ball/Pin Functions, Definitions, and Assignments

Table 2: Ball/Pin Functions

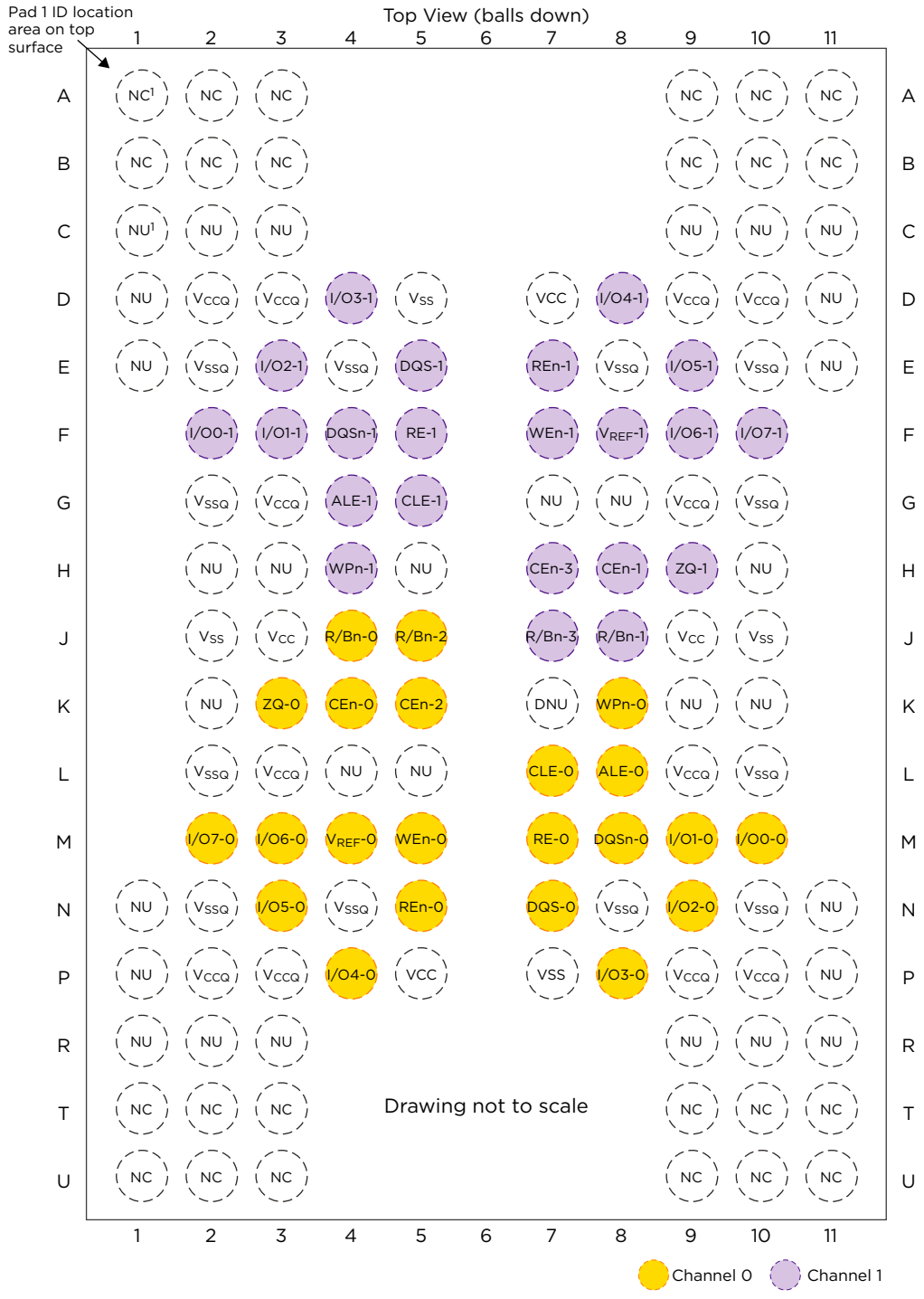
Pin Name	Type	Ball/Pin Function
ALE	Input	**Address Latch Enable** controls the activating path for addresses to internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
CEn	Input	**Chip Enable** controls device selection. When the device is busy, CEn high is ignored, and the device does not return to standby mode following program or erase operations.
CLE	Input	**Command Latch Enable** controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WEn signal.
RE[1]	Input	**Read Enable Complement** reserved for Toggle Mode DDR2 through DDR5.
REn	Input	**Read Enable** controls serial data out, and when active, drives the data onto the I/O bus. Data is valid after tDQSRE of the rising and falling edges of REn, which also increments the internal column address counter by one for each edge.
WEn	Input	**Write Enable** controls writes to the I/O port. Commands and addresses are latched on the rising edge of the WEn pulse.
WPn	Input	**Write Protect** provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WPn pin is active low.
DQS	Input/ Output	**Data Strobe** acts as an output when reading data, and as an input when writing data. DQS is edge-aligned with data read; it is center-aligned with data written.
DQSn[1]	Input/ Output	**Data Strobe Complement** reserved for Toggle Mode DDR2 through DDR5
I/O[7:0]	Input/ Output	**Data Input/Output (I/O)** inputs commands, addresses, and data, and outputs data during Read operations. The I/O pins float to High-z when the chip is deselected or when outputs are disabled.
R/Bn	Output	**Ready/Busy** indicates device operation status. R/Bn is an open-drain output and does not float to High-z when the chip is deselected or when outputs are disabled. When low, it indicates that a program, erase, or random read operation is in process; it goes high upon completion.
ZQ	Supply	ZQ is the reference pin for ZQ calibration
V_{CC}[2]	Supply	Power supply for the device
V_{CCQ}[2]	Supply	I/O power for input and output signals
V_{REF}[1]	Supply	Optional; Reference voltage, reserved for Toggle Mode DDR2 through DDR5.
V_{SS}, V_{SSQ}[2]	Supply	Ground
NC/NU		No connect: Do not connect to PCB/Not used: Can be connected to PCB

Note 1. Toggle Mode DDR2, DDR3, DDR4, and DDR5 = DDR interface with DQS + V_{REF} and complementary signals.

2. Connect all V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} pins of each device to common power supply outputs. Do not leave any power pins unconnected.

3.2 BGA Ball Assignments

Figure 1: 132-Lead BGA Assignments



Note 1. DNU = do not use, NC = no connect, NU = not used.

DRAFT Rev. 0.1 7/20/22

3.3 Packaging

3.3.1 BGA Package Signals

Table 3: BGA Signals: 8-Die Packages

Pad Name	8-Die, 4 CEn, 2 Channels							
	#0	#1	#2	#3	#4	#5	#6	#7
ALE	ALE0	ALE0	ALE0	ALE0	ALE1	ALE1	ALE1	ALE1
CEn	CEn0	CEn0	CEn2	CEn2	CEn1	CEn1	CEn3	CEn3
CLE	CLE0	CLE0	CLE0	CLE0	CLE1	CLE1	CLE1	CLE1
DQS	DQS0	DQS0	DQS0	DQS0	DQS1	DQS1	DQS1	DQS1
DQSn	DQSn0	DQSn0	DQSn0	DQSn0	DQSn1	DQSn1	DQSn1	DQSn1
R/Bn	R/Bn0	R/Bn0	R/Bn2	R/Bn2	R/Bn1	R/Bn1	R/Bn3	R/Bn3
RE	RE0	RE0	RE0	RE0	RE1	RE1	RE1	RE1
REn	REn0	REn0	REn0	REn0	REn1	REn1	REn1	REn1
WEn	WEn0	WEn0	WEn0	WEn0	WEn1	WEn1	WEn1	WEn1
WPn	WPn0	WPn0	WPn0	WPn0	WPn1	WPn1	WPn1	WPn1
V_{REF}	$V_{REF}0$	$V_{REF}0$	$V_{REF}0$	$V_{REF}0$	$V_{REF}1$	$V_{REF}1$	$V_{REF}1$	$V_{REF}1$
ZQ	ZQ0	ZQ0	ZQ0	ZQ0	ZQ1	ZQ1	ZQ1	ZQ1
I/O0	I/O0-0	I/O0-0	I/O0-0	I/O0-0	I/O0-1	I/O0-1	I/O0-1	I/O0-1
I/O1	I/O1-0	I/O1-0	I/O1-0	I/O1-0	I/O1-1	I/O1-1	I/O1-1	I/O1-1
I/O2	I/O2-0	I/O2-0	I/O2-0	I/O2-0	I/O2-1	I/O2-1	I/O2-1	I/O2-1
I/O3	I/O3-0	I/O3-0	I/O3-0	I/O3-0	I/O3-1	I/O3-1	I/O3-1	I/O3-1
I/O4	I/O4-0	I/O4-0	I/O4-0	I/O4-0	I/O4-1	I/O4-1	I/O4-1	I/O4-1
I/O5	I/O5-0	I/O5-0	I/O5-0	I/O5-0	I/O5-1	I/O5-1	I/O5-1	I/O5-1
I/O6	I/O6-0	I/O6-0	I/O6-0	I/O6-0	I/O6-1	I/O6-1	I/O6-1	I/O6-1
I/O7	I/O7-0	I/O7-0	I/O7-0	I/O7-0	I/O7-1	I/O7-1	I/O7-1	I/O7-1
Addr PA23	0	1	0	1	0	1	0	1
Addr PA24	X[1]	X	X	X	X	X	X	X
Addr PA25	X	X	X	X	X	X	X	X

Note 1. X = Don't care.

3.3.2 Package Outline Drawings: TBD

3.4 Device Integrity

3.4.1 Erase Before Initial Program Operation

The device might not be erased prior to shipment. This is done to protect the device in the event that the device will be subjected to IR reflow for the SMT process. If the cells are erased at the factory, the reflow process could cause cell degradation and/or make the device susceptible to data-retention failures.

SanDisk strongly recommends that prior to the reflow process, the host should erase **only** the blocks intended to be programmed.

When it is necessary to perform a firmware download ***before*** SMT:

- Do not erase the entire NAND Flash device.
- Perform a bad-block scan.
- Only erase those blocks that are needed to hold the firmware.
- After the firmware is downloaded, the device can go through SMT.
- When starting the normal operation of the device, do not erase the entire NAND Flash before starting. Over the lifetime of the device, only erase blocks just prior to programming them.

When it is necessary to perform a firmware download ***after*** SMT:

- Do not erase the entire NAND Flash device.
- The device can go through SMT.
- Perform a bad block scan.
- Only erase those blocks that are needed to hold the firmware.
- When starting the normal operation of the device, do not erase the entire NAND Flash before starting. Over the lifetime of the device, only erase blocks just prior to programming them.

Following the bad-block test, it is advisable to create a bad-block table to be used by the system software for mapping around any bad blocks.

3.4.2 Valid Blocks

The specification for the minimum number of valid blocks provided in Table 1, “Device Features,” on page 1 is applicable over the device lifetime.

The first block on each plane of each die is guaranteed to be a valid block at the time of shipment.

The device could occasionally contain unusable blocks, as described in the "Invalid Blocks (Bad Blocks)” section.

3.4.3 Invalid Blocks (Bad Blocks)

Because a device can occasionally contain unusable blocks, designers must consider the following:

- At the time of shipment, bad-block information is marked on each bad block.
- After installing the device in the system, check the device for any bad blocks. Refer to the test flow for bad-block detection. Bad blocks detected by the test flow must be managed by the system as unusable blocks.
- A small percentage of all blocks available on a die could be marked as bad blocks over the course of the device lifetime. The first block on each plane of each die is guaranteed to be good, and each block identified as good at shipment does not have program/erase status failure upon the first program/erase cycle. A bad block does not affect the performance of good blocks, because it is isolated from the bit lines by select gates.

Figure 2: Invalid Blocks

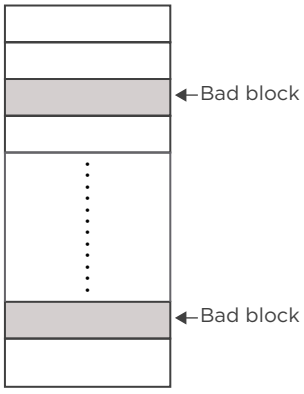
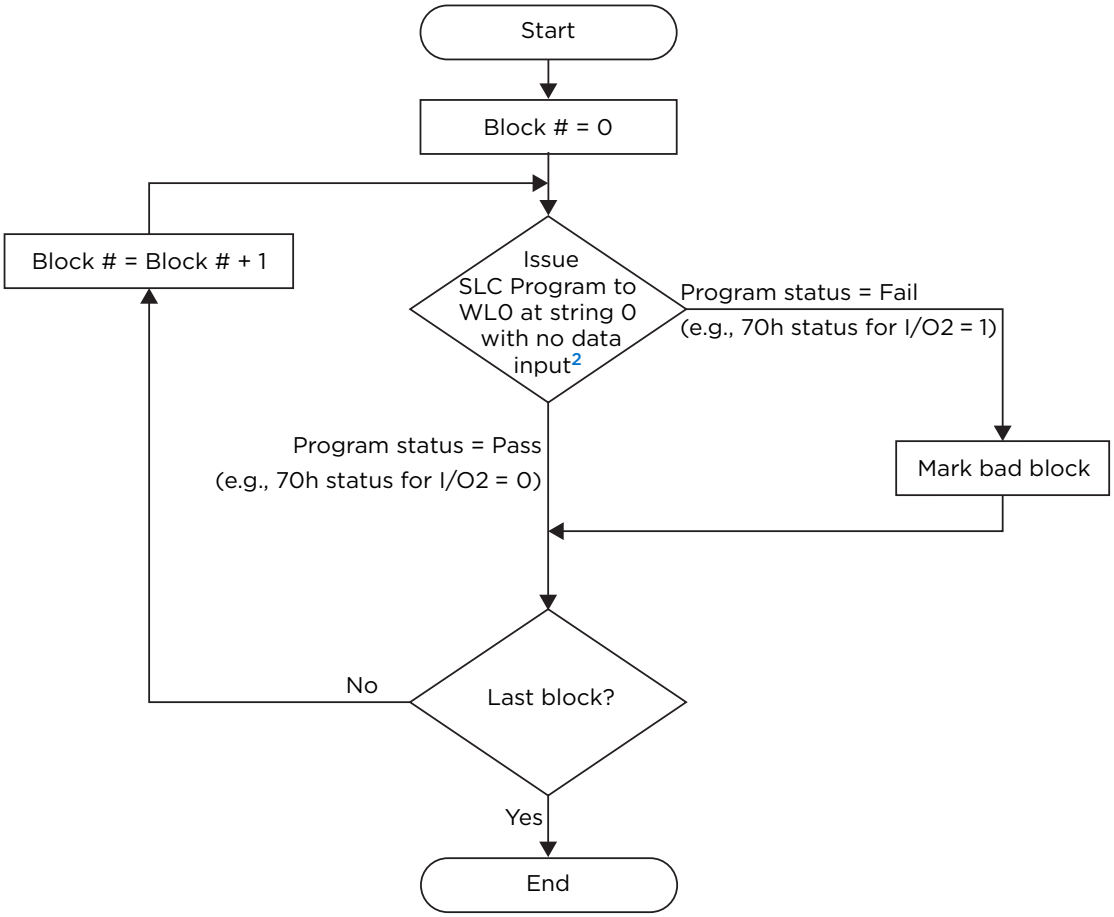


Figure 3: Bad-Block Test Flow



Note 1. Following power-up, an FFh Reset is required before checking for bad blocks,
2. See Figure 58, "Single-Plane SLC Program without Data Input," on page 90.

3.4.4 Error Correction Code (ECC)

Error correction code is necessary to ensure data integrity over the life of the device. Appropriate ECC will provide at least the minimum specified correction capability. In systems where error correction is a primary consideration, ECC that exceeds the minimum required for the device may be the best option.

To help maintain data integrity for the life of the device: Always perform a status check following Program and Erase operations. Use at least the minimum required ECC appropriate for the application. Ensure that system software provides adequate error management and wear distribution across the device.

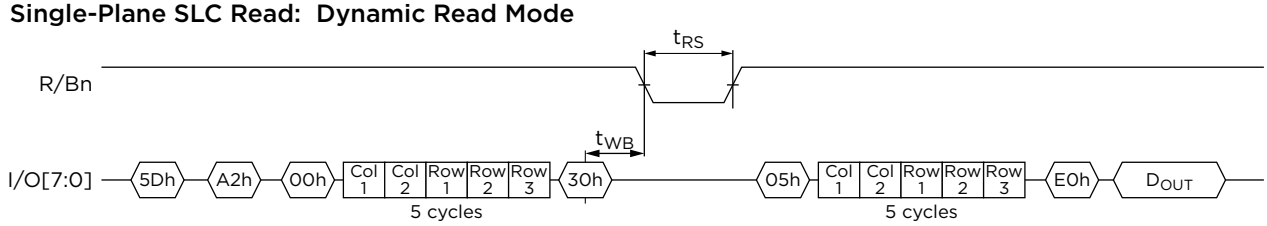
3.4.5 Dynamic Read

The dynamic read function makes it possible to repair soft errors that exceed ECC correction capabilities in the host system. Dynamic Read uses different read settings to attempt recovery, and is implemented by issuing 5Dh as a prefix to Read operations after the initial Read operation is complete. Internal device-read settings are loaded using the Set Features (D5h/EFh) command.

In this section and all subsequent sections of this data sheet, please refer to "4.3.3 Six-Address-Cycle Input" on page 23 regarding the number of address input cycles depicted in figures.

Figure 4: SLC Dynamic Read

Single-Plane SLC Read: Dynamic Read Mode



Multi-Plane SLC Read: Dynamic Read Mode

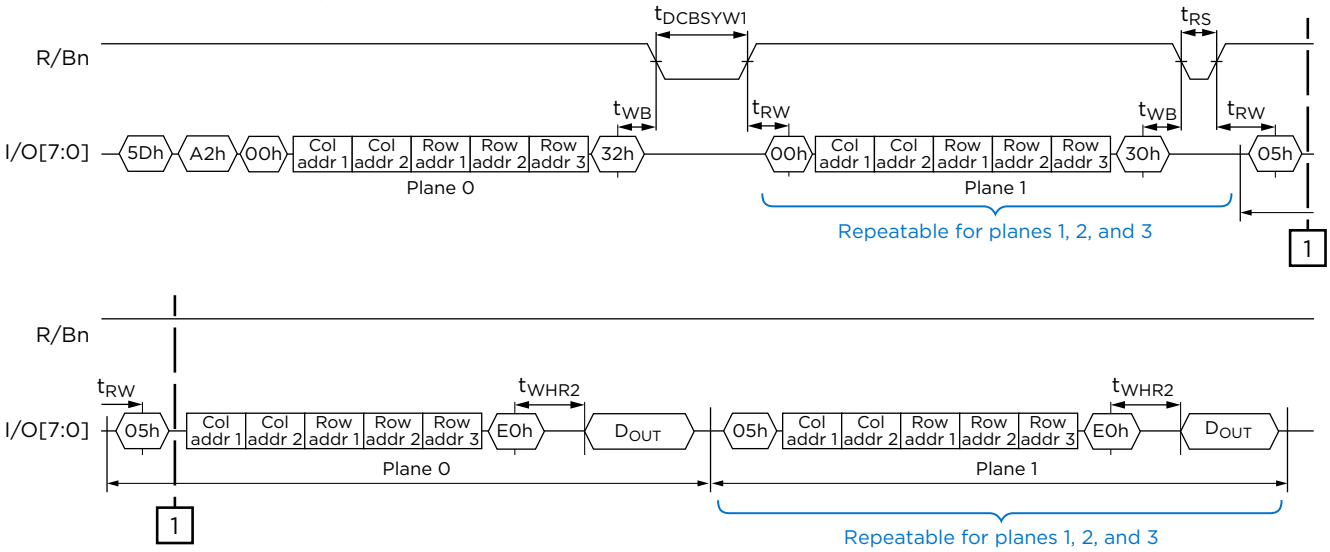
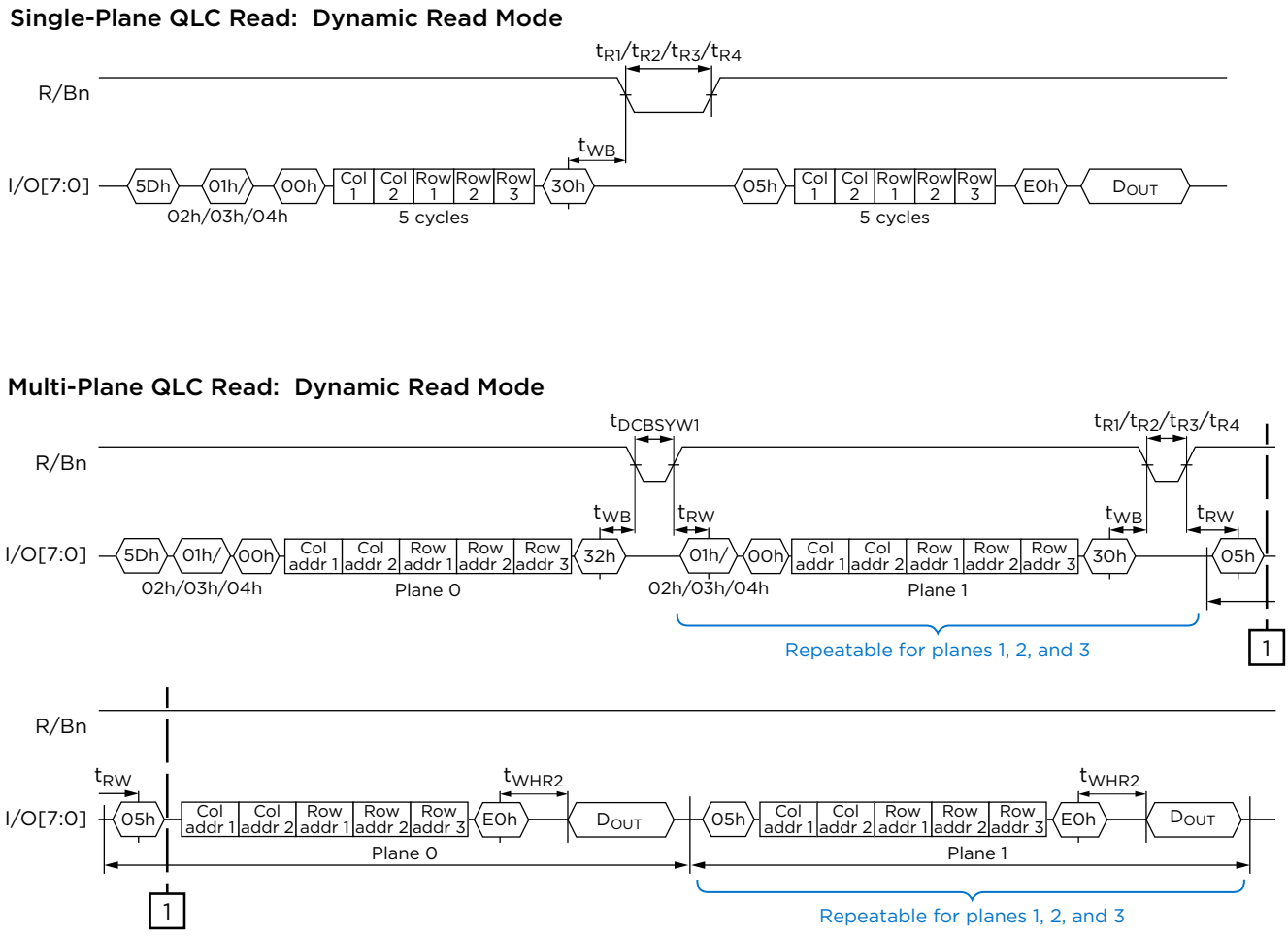


Figure 5: QLC Dynamic Read

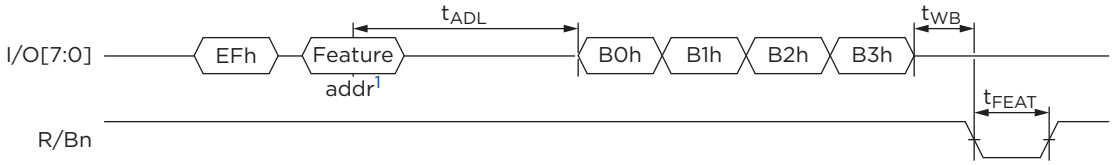


When a host identifies an uncorrectable error, it can issue a D5h/EFh command to feature addresses (see Table 4, “Dynamic Read Mode Settings with 5Dh (w/o aIPR),” on page 14), with sub-features B0, B1, B2, B3, to initiate the dynamic read option (see Figure 6, “Set Dynamic Read Registers,” on page 13). The values loaded into the sub-features remain until one of these events occurs:

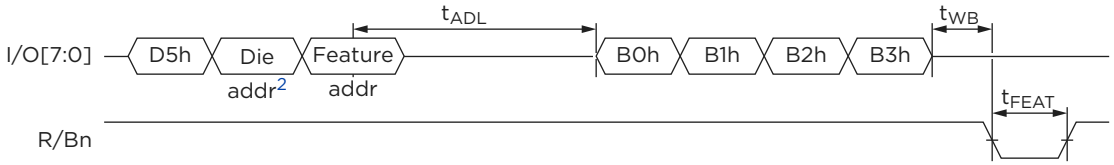
- The NAND Flash power cycles
- The 89h Set Features Register Reset command is issued

Figure 6: Set Dynamic Read Registers

To set the registers (EFh)



To set the registers by die (D5h)



Note 1. Feature addresses are provided in
Table 64, “Set Features Addressing (without aIPR),” on page 120 **or**
Table 65, “Set Features Addressing (with aIPR),” on page 120.
For additional details, see:
Table 4, “Dynamic Read Mode Settings with 5Dh (w/o aIPR),” on page 14 **or**
Table 5, “Dynamic Read Mode Settings with 5Dh (with aIPR),” on page 15.

2. Die address is one byte (00h: die 0, 01h: die 1, 02h: die 2... 07h: die 7)
3. In a multi-die package, after D5h has been initiated on a given die, initiating operations on any other die sharing the same CEn is prohibited until D5h is complete.
4. It is necessary to provide all four bytes of data in the sequences above (B0h, B1h, B2h, and B3h). If there is no data available to input for a particular feature address—for example, for address 13h, where only B0h, B1h, and B2h are required—the last byte (B3h) should be input as 00h.

Following the 5Dh command and a single read operation, the chip resumes normal Read operation; and the last values loaded into the Dynamic Read registers remain there.

Sending a Reset command (FFh) during Dynamic Read terminates the current read operation and resets Dynamic Read mode to normal Read mode for subsequent Read operations. The Dynamic Read registers are ***not*** reset.

Caution: Because the Set Features registers are shared by Dynamic Read (5Dh); and by Program (80h) and Erase (60h) operations with 5Bh enabled, the Set Features registers should be set to appropriate values before initiating any Program or Erase operation following a Dynamic Read.

3.4.5.1 Dynamic Read Mode Settings

Dynamic Read for QLC Read enables read-level adjustment for each state to compensate for the shift in threshold voltage distribution due to charge loss over time. Dynamic Read is also supported for SLC Read.

The QLC Read scheme is the default Read mode with a set of initial Read values used at each power-up. When an uncorrectable error (UECC) is encountered (that is, the number of failed bits exceeds the limit for ECC correction), the Dynamic Read flag is set to trigger a different set (or case) of Dynamic Read values to be used for all subsequent Reads. Multiple cases of Dynamic Read values are available to track the threshold voltage shift over time and after cycling. At subsequent instances of UECC, the case number is incremented.

The Dynamic Read flag, case number, and read-level shift values are stored by the controller.

Table 4: Dynamic Read Mode Settings with 5Dh (w/o aIPR)

Feature Address	Data Byte[1]	Value
9Bh	B0	S2
	B1	S8
	B2	S10
	B3	S12
9Ch	B0	S1
	B1	S3
	B2	S7
	B3	S13
9Dh	B0	S5
	B1	S11
	B2	S14
9Eh	B0	S4
	B1	S6
	B2	S9
	B3	S15
8Bh/14h	B0	SLC

Note 1. If shift is not required in Dynamic Read mode, these data bytes must be set to 00h.

2. For additional information, contact your representative.

Table 5: Dynamic Read Mode Settings with 5Dh (with aIPR)

Feature Address	Data Byte[1]	Value	Plane
9Bh	B0	S2	0
	B1	S8	
	B2	S10	
	B3	S12	
9Ch	B0	S1	
	B1	S3	
	B2	S7	
	B3	S13	
9Dh	B0	S5	
	B1	S11	
	B2	S14	
9Eh	B0	S4	
	B1	S6	
	B2	S9	
	B3	S15	
85h	B0	S2	1
	B1	S8	
	B2	S10	
	B3	S12	
86h	B0	S1	
	B1	S3	
	B2	S7	
	B3	S13	
87h	B0	S5	
	B1	S11	
	B2	S14	
88h	B0	S4	
	B1	S6	
	B2	S9	
	B3	S15	
A0h	B0	S2	2
	B1	S8	
	B2	S10	
	B3	S12	

Table continues at top of right column

Feature Address	Data Byte[1]	Value	Plane
A1h	B0	S1	2
	B1	S3	
	B2	S7	
	B3	S13	
A2h	B0	S5	
	B1	S11	
	B2	S14	
A3h	B0	S4	
	B1	S6	
	B2	S9	
	B3	S15	
A6h	B0	S2	3
	B1	S8	
	B2	S10	
	B3	S12	
A7h	B0	S1	
	B1	S3	
	B2	S7	
	B3	S13	
A8h	B0	S5	
	B1	S11	
	B2	S14	
A9h	B0	S4	
	B1	S6	
	B2	S9	
	B3	S15	
8Bh/14h	B0	SLC	0
8Ah/13h	B0	SLC	1
A5h	B0	SLC	2
ABh	B0	SLC	3

Note 1. If shift is not required in Dynamic Read mode, these data bytes must be set to 00h.

2. For additional information, contact your representative.

4 NAND Flash Logic, Commands, and Addressing

4.1 Logic Tables

Address input, command input, and data input/output are controlled by the CLE, ALE, CEn, WEn, REn, and WPn signals (see Table 6). Program, Erase, Read, and Reset operations are controlled by the command operations shown in Table 7, "Basic Command Set," on page 18.

Table 6: DDR Signal Conditions

H = V_{IH}, L = V_{IL}, X = V_{IH} or V_{IL} (Don't Care)

Event/Condition	CEn	CLE	ALE	WEn	REn	DQS	WPn	Chip select	Cache busy
Address input	L	L	H		H	X[1, 2]	Note 3	Note 4	Ready
Command input	L	H	L		H	X[2]	Note 3	Note 4	Ready
Data input	L	L	L	H	H		H	Selected	Ready
Device ID read	L	L	L	H		NAND drive	X	Selected	Ready
Get features	L	L	L	H		NAND drive	X	Note 4	Ready
Serial data output	L	L	L	H		NAND drive	X	Selected	Ready
Set features	L	L	L	H	H		H	Note 4	Ready
Status output	L	L	L	H		NAND drive	X	Selected	X
During Program (busy)	X[1]	X	X	X	X	X	H	X	—
During Erase (busy)	X	X	X	X	X	X	H	X	—
During Read (busy)	H	X	X	X	X	X	X	X	—
	L	X	X	H[5]	H[5]	X	X	X	—
Program or Erase Inhibit	X	X	X	X	X	X	L	Selected	—
Standby	H	X	X	X	X	X	0V/V_{CCQ}	X	X

Note 1. X = Don't care. Float V_{IH}, or V_{IL}.

2. DQS must be fixed at V_{IH} or V_{IL} after an 80h command, until a 10h, 11h, or 15h command is input.
3. For details regarding Program and Erase operations when WPn goes low, see "5.3.2 WPn Signal" on page 30.
4. See Table 10, "NAND Flash Command Properties," on page 20.
5. If CEn is low during Read (busy), WEn and REn must be held high to prevent unintended Read, command, or address inputs to the device. Reset or Status Read commands can be issued during Read (busy).

4.2 Command Sets

NAND Flash commands and addresses are multiplexed onto I/O[7:0]. Command latch enable (CLE) and Address latch enable (ALE) are used to latch commands and addresses, respectively, wdhile bringing WEn and CEn low. Inputs are latched on the rising edge of WEn.

Caution: Any undefined command inputs are prohibited; only commands listed in Tables 7 through 9 are supported.

Inputting commands other than those specified in this document could cause stored data to be corrupted and undefined results could occur if an unknown command is issued during the command cycle.

The basic command set shown in Table 7 provides only a brief description of basic commands; it is not an exhaustive list. The device operation sections provide additional details for commands and their uses.

Table 7: Basic Command Set

Command	First Set	Address Cycles	Second Set	Acceptable while Busy
Cache Read with Full Address Input	00h	5	3Ch	
Page Read	00h	5	30h	
Random Cache Read	00h	5	31h	
Read for Copy-Back	00h	5	35h	
Read ID	90h	1	—	
Read Start for Last Page Cache Read	3Fh	—	—	
Read Status	70h	—	—	Yes
Read Status2	71h/72h	—	—	Yes
Read Status Enhanced (Fxh = any one of F1h through F8h)	78h/Fxh	3	—	Yes
Cache Program	80h	5	15h	
Copy-Back Program[2, 3]	85h	5	10h/15h	
Page Program[2, 3]	80h	5	10h/15h	
Block Erase[3, 4]	60h	3	D0h	
Change Read Column	05h	5	E0h	
Change Write Column[2, 3]	85h	5	10h/15h	
Get Features	EEh	1	—	
Get Features by die	D4h	2	—	
Power-On Reset	FDh	—	—	
Reset[1]	FFh	—	—	Yes
Reset by die[3]	FAh	3	—	Yes
Set Features	EFh	1	—	
Set Features by die	D5h	2	—	
Set Features Register Reset[5]	89h	—	—	

Note 1. When the device is busy, input only the 70h, the 71h, the 72h, the 78h, an Fxh, the FAh, or the FFh command.

2. If an incomplete [80h or 85h] command sequence is issued, for example, neither the 10h nor the 15h command is issued, the FFh command must be issued to terminate the incomplete command sequence. Note that the FFh command will reset operations on all die sharing the same CEn.
3. The FAh sequence can also be used to terminate the command sequence for the selected die in multi-die-per-CEn configurations.
4. If an incomplete 60h command sequence is issued, for example, and the D0h command is not issued, the FFh command must be issued to terminate the incomplete command sequence. Note that the FFh command will reset operations on all die sharing the same CEn.
5. The Set Features Register Reset (89h) command provides reset functions, including Set Features reset. The device returns to the default interface setting and the default dynamic read case following command execution. Note that the FFh command will reset operations on all die sharing the same CEn.
6. For commands with three or five address cycles, users can send four or six address bytes. The fourth or sixth address byte is unnecessary, and will be ignored ***unless*** more than two die are sharing the same CEn.

Table 8: Command Prefixes

Basic Command Prefixes	Prefix Symbol	Use with Operation:
Dynamic Read	5Dh	Read
Initiate first Program cycle	0Dh	QLC Program
Select lower page for Read and Program	01h	QLC Read, Program
Select middle page for Read and Program	02h	
Select upper page for Read and Program	03h	
Select top page for Read and Program	04h	
Switch to SLC mode	A2h	Block Erase, SLC Page Read, SLC Program

Table 9: Extended Command Set

Command	First Set	Address Cycles for First Set	Second Set	Address Cycles for Second Set
Cache Read with Full Address Input	00h--30h	5	00h--3Ch	5
Multi-Plane Random Cache Read	00h--32h	5	00h--31h	5
Multi-Plane Read	00h--32h	5	00h--30h	5
Multi-Plane Read for Copy-Back	00h--32h	5	00h--35h	5
Multi-Plane Copy-Back Program[1, 2]	85h--11h	5	85h--10h/15h	5
Multi-Plane Cache Program[1, 2]	80h--11h[1]	5	80h/81h--15h	5
Multi-Plane Program[1, 2]	80h--11h[1]	5	80h/81h--10h/15h	5
Multi-Block Erase	60h--	3	60h--D0h	3

Note 1. Between an 11h and an 80h, an 81h, or an 85h command, only a 70h, a 71h, a 72h, an FAh, or an FFh command can be issued; all other commands are prohibited. Note that the FFh command will reset operations on all die sharing the same CEn.

2. Multi-plane block addresses can be different; page addresses must be the same.

3. For commands with three or five address cycles, users can send four or six address bytes, and the last address byte will be ignored unless more than two die share a single CEn.

4.2.1 NAND Flash Command Properties

In multi-die NAND Flash packages, the command properties play an important role in device operation. Command properties enable users to optimize their designs by uniquely identifying global and local commands.

A “global” command is accepted by each die that has CEn set to low; “local” commands are accepted only by die that have CEn set low and receive address-specific inputs.

Table 10: NAND Flash Command Properties

Command Property[1]	Commands					
Global						
	00h	04h	60h	80h[2]	90h	EFh
	01h	05h	70h	81h	A2h	FAh
	02h	0Dh	71h	85h	D4h	FFh
	03h	5Dh	78h	89h	D5h	
Local						
	10h	1Ah	32h	3Fh	EEh	FDh
	11h	30h	35h	D0h		
	15h	31h	3Ch	E0h		

Note 1. A global command is broadcast to every die that has CEn set low. A local command is die-dependent (accepted only by the selected die).

2. The 80h command can be global or local, depending on the device configuration. Contact your representative for additional information.

3. I/O is driven by the selected die during data output in multiple-die-per-CEn scenarios. For details regarding die selection in a multi-die package, refer to “5.4 Chip Select Command” on page 31.

4.3 Addressing

4.3.1 SLC Addressing

Figure 7: SLC Address Assignments

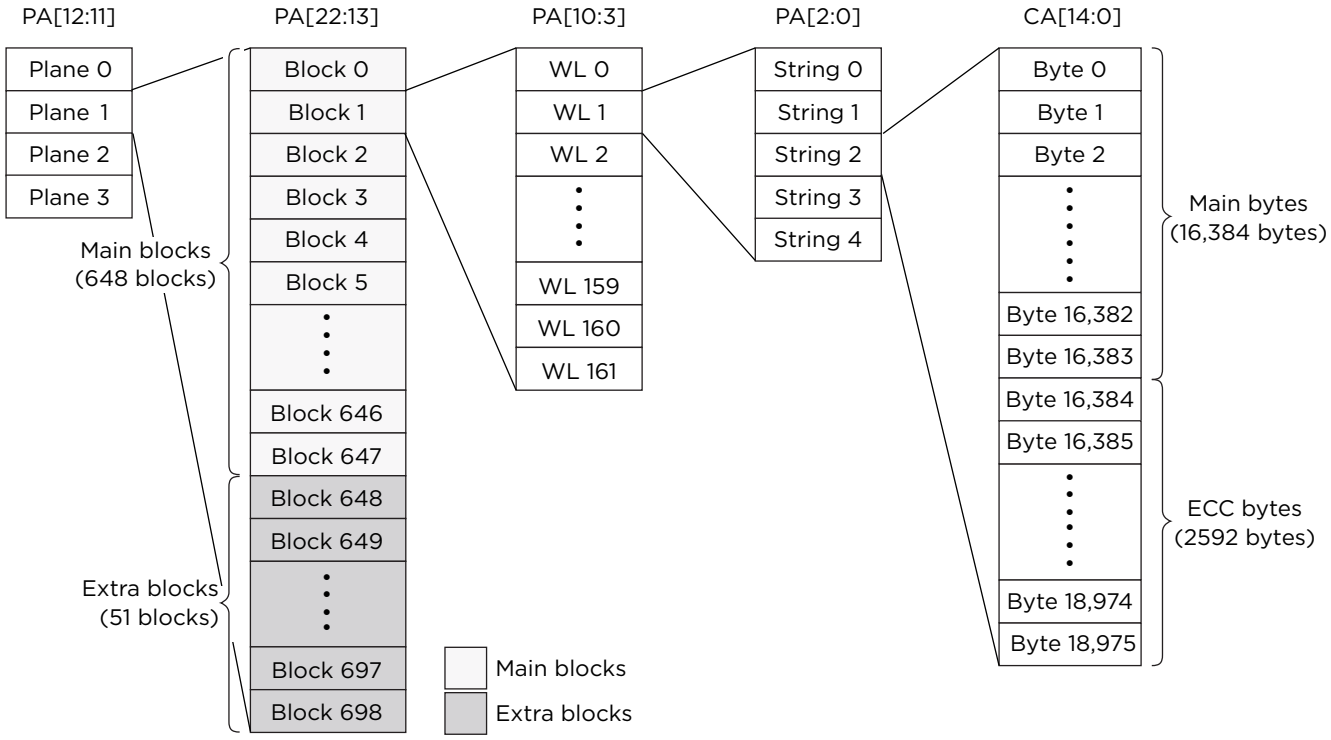


Table 11: SLC Addressing Definitions

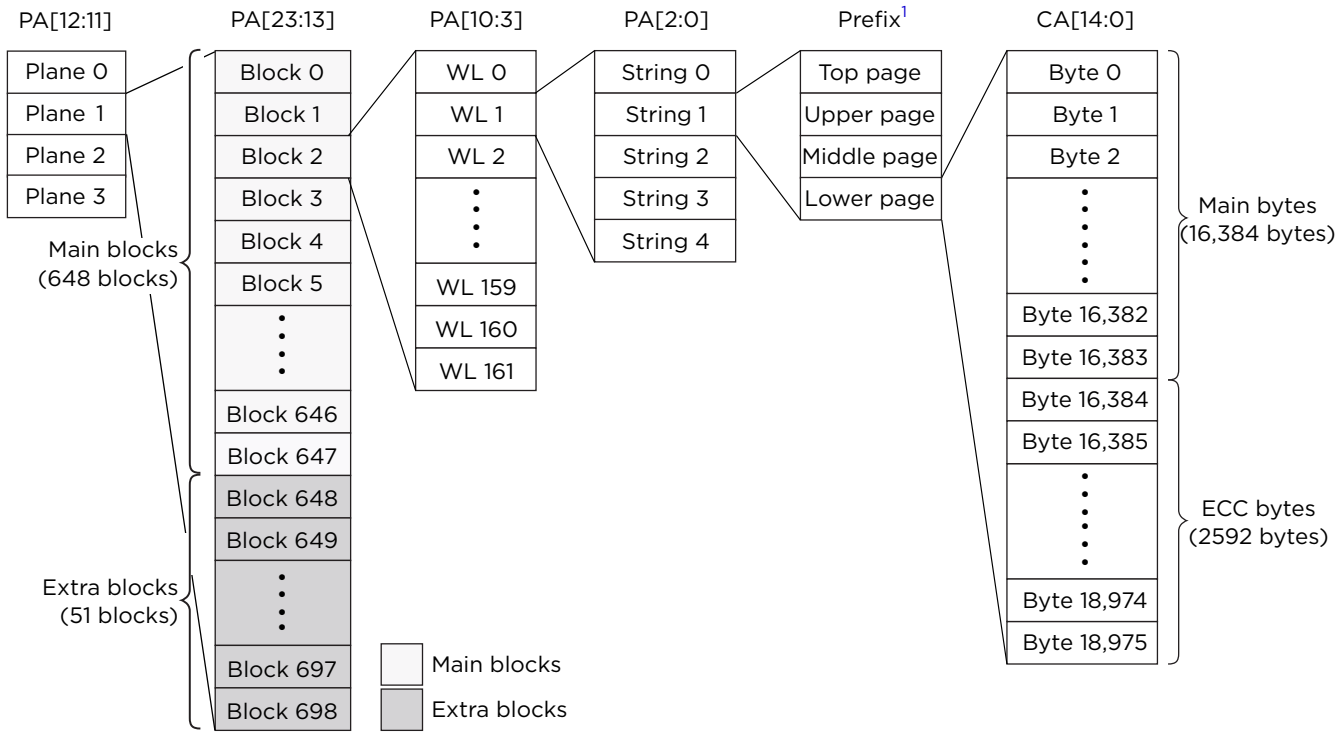
Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First cycle	CA7[1]	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	X[1]	CA14	CA13	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7[1]	PA6	PA5	PA4	PA3	PA2[1]	PA1	PA0
Fourth cycle	PA15	PA14	PA13[1, 3]	PA12[1]	PA11	PA10[1, 2]	PA9	PA8
Fifth cycle	PA23[1, 4]	PA22	PA21	PA20	PA19	PA18	PA17	PA16
Sixth cycle[5]	X	X	X	X	X	X	PA25	PA24

Note 1. CA[14:0] = column addresses; PA[2:0] = string addresses; PA[10:3] = WL addresses; PA[12:11] = plane addresses; PA[22:13] = block addresses; PA[25:23] = chip addresses; X = "Don't Care." Addressing is the same for QLC and SLC.

2. PA[10:3] are WL addresses. Only WL[161:0] are valid WL addresses. For SLC operations, wordlines are the same as pages.
3. PA[22:13] are block addresses. Only blocks [698:0] are valid block addresses.
4. PA[25:23] control chip addressing for up to eight die sharing one CEn.
5. A sixth cycle of addresses is required only when more than two die share a single CEn. See "4.3.3 Six-Address-Cycle Input" on page 23 for additional information.

4.3.2 QLC Addressing

Figure 8: QLC Address Assignments



Note 1. Lower, middle, upper, and top pages are selected using prefix commands (01h/02h/03h/04h).

Table 12: QLC Addressing Definitions

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First cycle	CA7[1]	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	X[1]	CA14	CA13	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7[1]	PA6	PA5	PA4	PA3	PA2[1]	PA1	PA0
Fourth cycle	PA15	PA14	PA13[1, 3]	PA12	PA11	PA10[1, 2]	PA9	PA8
Fifth cycle	PA23[1, 4]	PA22	PA21	PA20[3]	PA19	PA18	PA17	PA16
Sixth cycle[5]	X	X	X	X	X	X	PA25	PA24

Note 1. CA[14:0] = column addresses; PA[2:0] = string addresses; PA[10:3] = WL addresses; PA[12:11] = plane address; PA[22:13] = block addresses; PA[25:23] = chip addresses; X = "Don't Care." Addressing is the same for QLC and SLC.

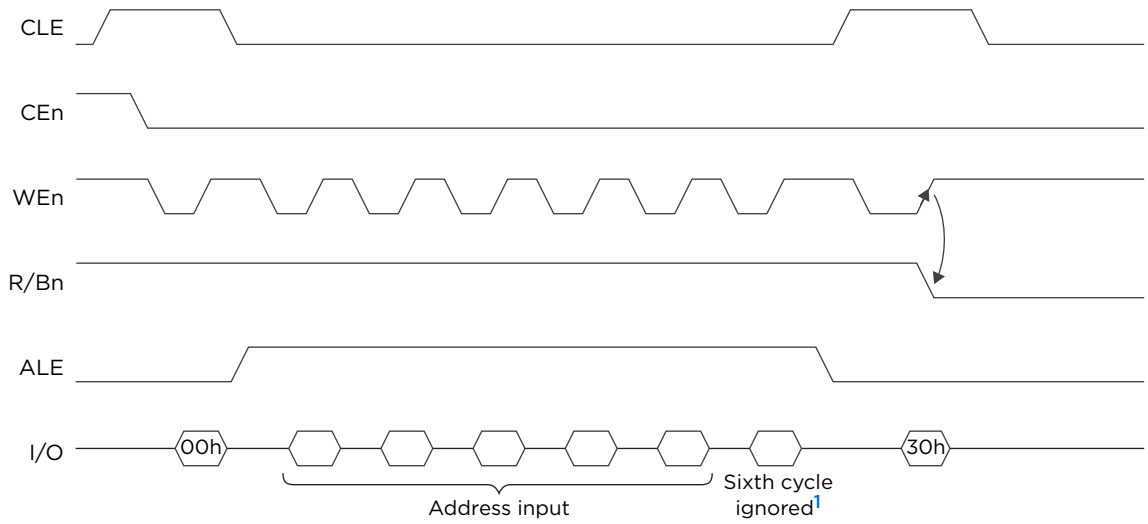
2. PA[10:3] are WL addresses. Only WL[161:0] are valid WL addresses.
3. PA[22:13] are block addresses. Only blocks [698:0] are valid block addresses.
4. PA[25:23] control chip addressing for up to eight die sharing one CEn.
5. A sixth cycle of addresses is required only when more than two die share a single CEn. See "4.3.3 Six-Address-Cycle Input" on page 23 for additional information.

4.3.3 Six-Address-Cycle Input

A sixth cycle of addresses is required only when more than two die share a single CEn; otherwise, a sixth cycle is ignored within the chip.

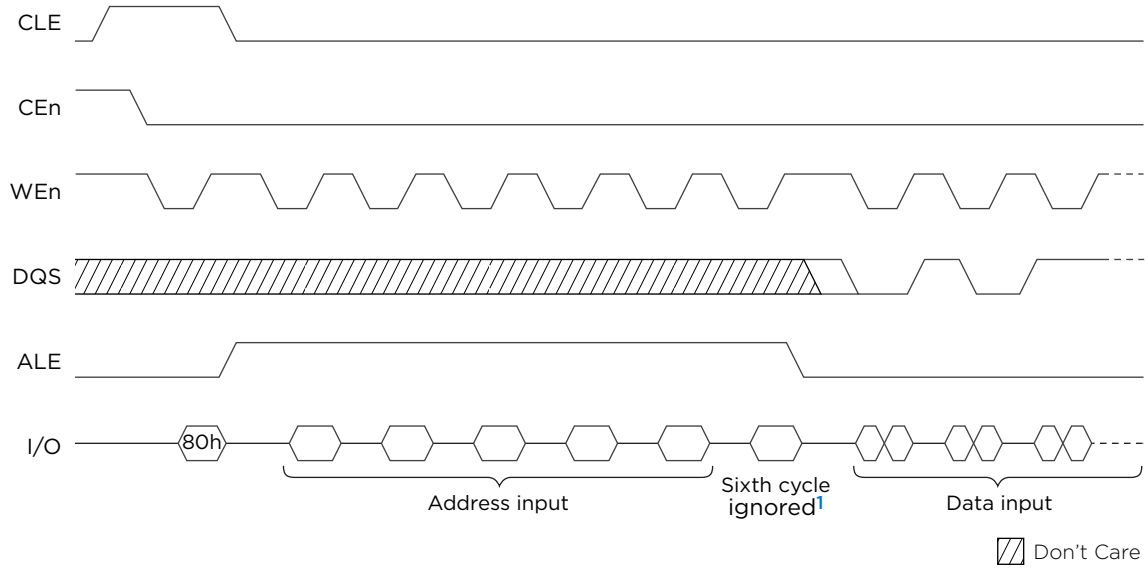
In timing figures with three or five address cycles, it is implied—but not shown—that they will be changed to four or six address cycles, respectively, when more than two die share a single CEn.

Figure 9: Read: Six-Address-Cycle Input



Note 1. A sixth address cycle is ignored, ***unless*** more than two die are sharing one CEn.

Figure 10: Program: Six-Address-Cycle Input



Note 1. A sixth address cycle is ignored, ***unless*** more than two die are sharing one CEn.

4.3.4 2N Rule for Data Input/Output

For Program and Read operations, only an even number of data bytes (2 × N, where N is an integer) can be transferred at the I/O pins.

Additionally, the least significant bit (LSB), address bit CA0 in Table 11, “SLC Addressing Definitions,” on page 21 **and** Table 12, “QLC Addressing Definitions,” on page 22, must be zero (0) when issuing data I/O commands 00h, 05h, 80h, or 85h.

Because DDR means “two bytes of data per clock cycle,” an odd number of data bytes cannot be read from or written to the NAND Flash device, and the 2N rule is automatically satisfied.

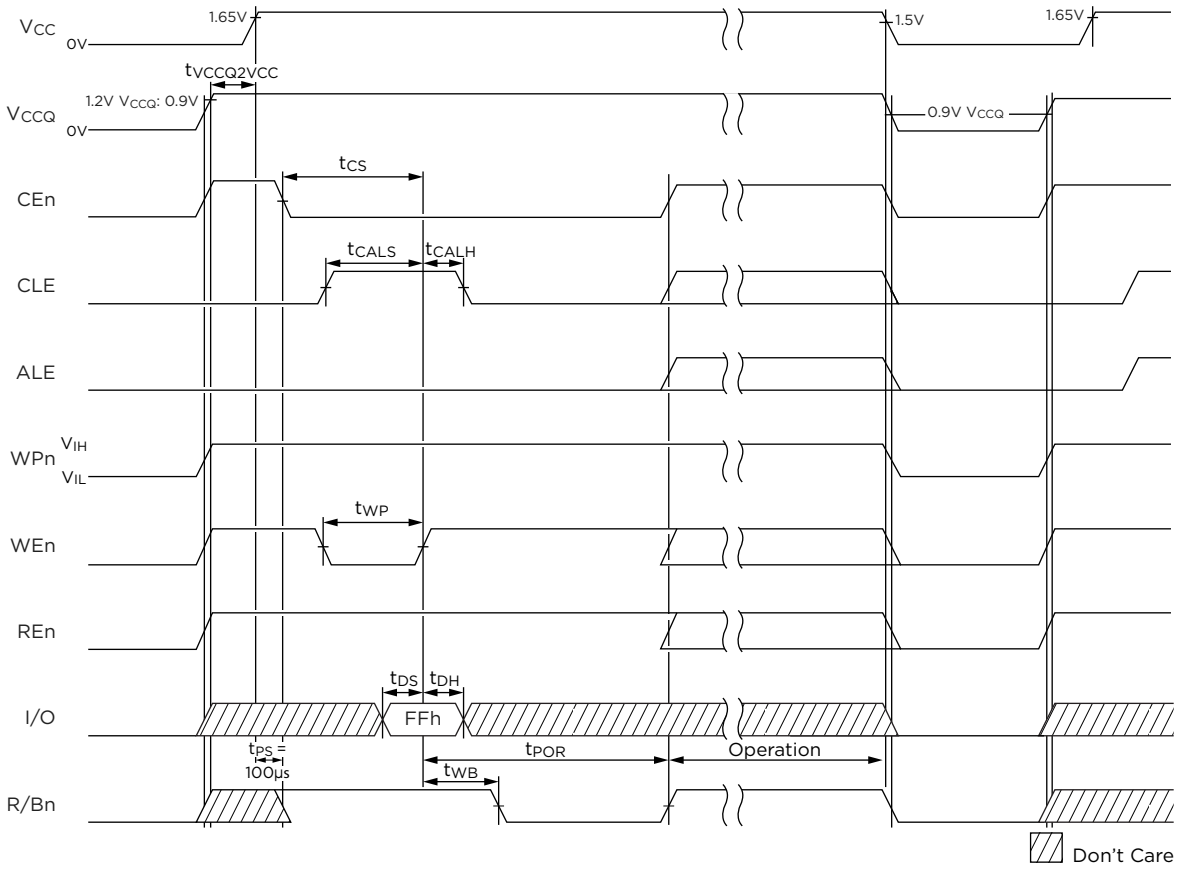
5 Operating Modes and Device Initiation

SanDisk Gen6 NAND Flash devices power up and operate in Toggle Mode. This mode supports the Toggle Mode JEDEC standard to improve I/O interface speed.

5.1 Power-On/Off Sequence

The Reset (FFh) command must be issued following power-up to initialize the device. The maximum current consumed during the Reset busy period (I_{CC0}) is TBDmA (max) per die selected by the CEn pin(s). See Figure 11.

Figure 11: Power-On/Off Sequence



Note 1. tPS is referenced from the first rising edge of V_{CC} or V_{CCQ}—whichever rises latest.

5.2 V_{CC}/V_{CCQ} Ramp Requirements and Specifications

To initiate NAND Flash Power-On Read (POR), the V_{CC} and V_{CCQ} power supplies must be set to their respective minimum voltages before POR can execute. See Table 13, "VCC and VCCQ DC Voltage Specifications," on page 27.

5.2.1 V_{CC} and V_{CCQ} Ramp-Up and Ramp-Down Order and Rates

V_{CCQ} must be powered up first, with all NAND control signals properly set to their power-on default states before ramping V_{CC} (see Table 14, "Control Signal Settings for VCCQ/VCC Ramp," on page 27). This will preclude potential spurious command latching at power-up. The minimum and maximum V_{CC} and V_{CCQ} ramp-up and ramp-down rates are provided in Table 13 on page 27.

The V_{CC} and V_{CCQ} ramp rates are referenced to 10% and 90% of the final V_{CC} and V_{CCQ} levels. When the V_{CC} and V_{CCQ} supplies are between 0% and 10%, and between 90% and 100%, they should be ramped within, or more slowly than the specified ramp-rate range. Ripple during ramp and at 100% DC target should meet the AC specification in Table 16, "VCC and VCCQ AC Ripple Specifications," on page 27.

V_{CCQ} must be above its minimum level for at least 10µs before V_{CC} ramps up. V_{CC} and V_{CCQ} can ramp down in any order.

Figure 12: V_{CCQ} and V_{CC} Ramp-Up Order

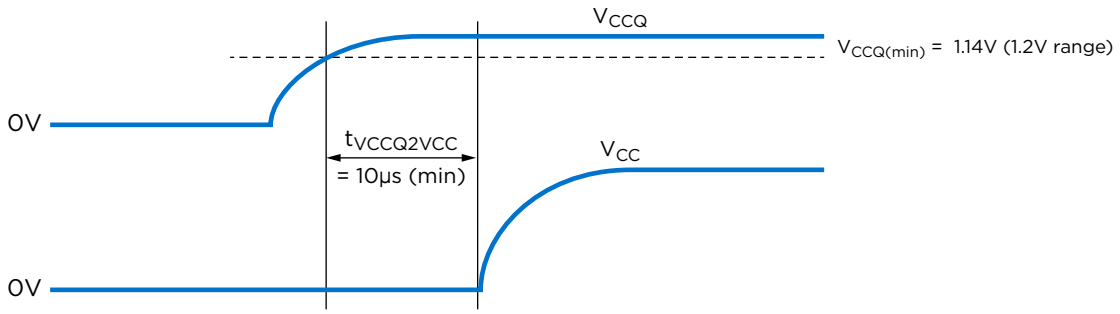


Figure 13: V_{CCQ} and V_{CC} Ramp-Up/Ramp Down Rates

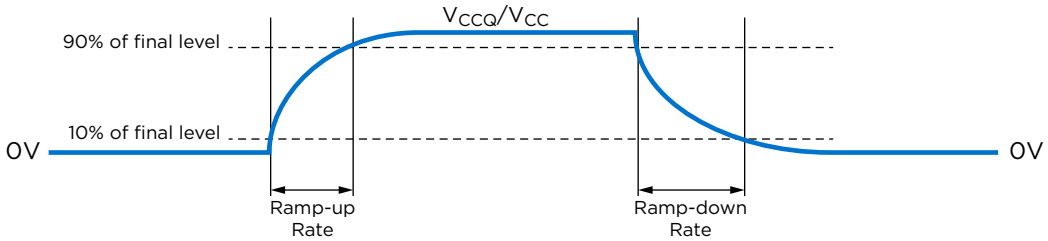


Table 13: V_{CC} and V_{CCQ} DC Voltage Specifications

Specification	V_{CC} (V)	V_{CCQ}
Minimum voltage	2.35	1.14
Typical voltage	—	1.20
Maximum voltage	3.60	1.30

Note 1. All voltage levels are measured at the BGA package balls.

Table 14: Control Signal Settings for V_{CCQ}/V_{CC} Ramp

Control Signal	Default State During Power-Up
ALE	V_{IL}
CLE	V_{IL}
CEn	V_{IH} or no more than 100mV lower than V_{CCQ}
REn	
WEn	
WPn	

Table 15: Ramp-Up and Ramp-Down Specifications

Power Supply	Slowest Ramp-up Rate (min)	Fastest Ramp-up Rate (max)
V_{CC} and V_{CCQ}	0.04 mV/µs	100 mV/µs
Power Supply	**Slowest Ramp-down Rate (min)**	**Fastest Ramp-down Rate (max)**
V_{CC} and V_{CCQ}	—	50 mV/µs

Table 16: V_{CC} and V_{CCQ} AC Ripple Specifications

Power Supply	During 0%–100% Ramp (max)	At 100% DC Target Level (max)
V_{CC}	± 100mV	± 4%
V_{CCQ}	± 50mV	± 3%

Note 1. All voltage levels are measured at the BGA package balls.

Table 17: V_{CC} and V_{CCQ} AC Supply Voltage Noise Specifications

Power Supply	Voltage Range (V)	AC Supply Voltage Noise (max)	Frequency
V_{CC}	2.35–3.60	± 4% (8% peak-to-peak)	0Hz—100MHz
V_{CCQ}	1.14–1.30	± 3% (6% peak-to-peak)	0Hz—20MHz
	1.14–1.30	± 0.6% (1.2% peak-to-peak)	> 20MHz—500MHz

Note 1. The maximum AC supply voltage noise for V_{CC} and V_{CCQ} is a percentage of the target V_{CC} and V_{CCQ} voltage level used.

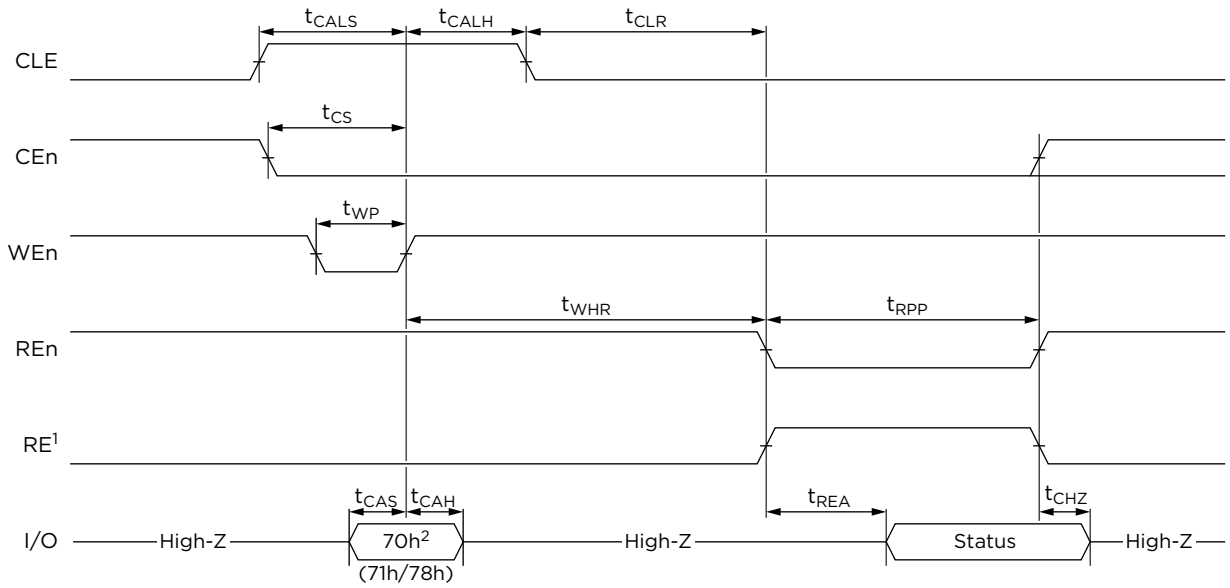
5.3 Status Read Cycle Following a Power-On Sequence or User Reset

The device status can be accessed using the Status Read cycle when either of these conditions exists:

- After the power-on sequence is complete
- The controller has reset and lost track of the device I/O interface setting

For additional Status Read sequences, see:
Figure 98, “Toggle Mode Status Read Cycle,” on page 140.

Figure 14: Status Read Cycle Following a Power-On Sequence or User Reset



Note 1. RE is required for the Toggle Mode DDR2 interface. See Figure 98, “Toggle Mode Status Read Cycle,” on page 140, **and** Figure 100, “Status Read Cycle at Power-On, Prior to Toggle Mode Enable,” on page 141.

2. The Read Status Enhanced (78h) command requires row-address-setting steps prior to reading the status value. This is not depicted in the figure. See “12.1 Read Status” on page 109 **and** “12.2 Read Status Enhanced” on page 112 for additional information.

5.3.1 Power Loss

DO NOT power off during any NAND Flash operation. A power failure during any NAND operation can cause data loss, not only for the current operation but also to data written prior to the power loss in NAND. If there is a sudden power loss, the V_{CC} ramp-down rate ***must not*** be faster than 50 mV/µs (see Table 15, "Ramp-Up and Ramp-Down Specifications," on page 27).

The data integrity of an operation in progress and any previously written data are not guaranteed if the V_{CC} ramp-down rate is faster than 50 mV/µs.

5.3.2 WPn Signal

Erase and Program operations are automatically reset when the WPn signal goes low. These operations are enabled and disabled as shown in Figures 15 through 18.

Figure 15: Program Enable

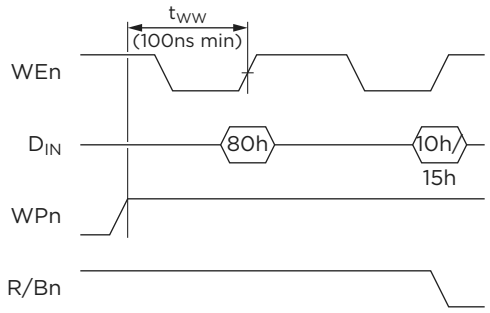


Figure 16: Program Disable

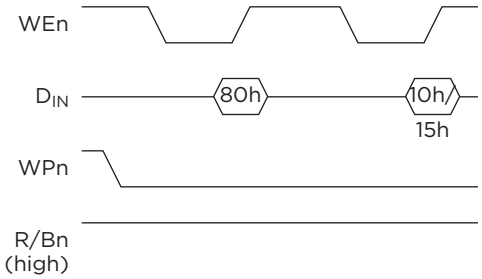


Figure 17: Erase Enable

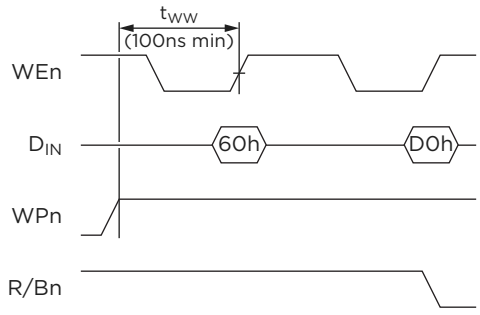
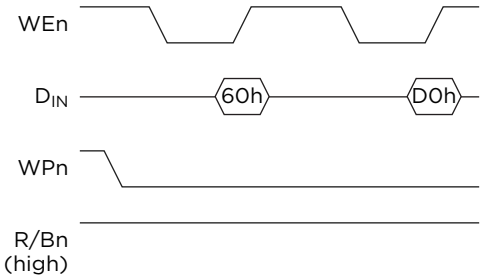


Figure 18: Erase Disable



5.4 Chip Select Command

When multiple chips in a package share the same CEn pin and the same R/Bn pin, it is not possible to monitor the shared R/Bn pin to determine the status of an individual chip during parallel operations.

User-mode commands Fxh (F1h through F8h) enable users to select one of up to eight chips in a package that share a common CEn pin, as follows:

Table 18: User Chip-Select Commands

Command	Selection
F1h	Chip #0
F2h	Chip #1
F3h	Chip #2
F4h	Chip #3
F5h	Chip #4
F6h	Chip #5
F7h	Chip #6
F8h	Chip #7

Note 1. The CEn pin must be low (active) to enable the selection.
2. Following tWB, the Ready/Busy pin is driven low-to-high, or high-to-low by the selected chip only,
3. The chip selection remains valid for subsequent operations until another chip select command is issued or power-down occurs.
4. The F1h through F8h commands can be used with or without the 7xh status check command. Either way, the F1h–F8h command will switch the chip selection and execute a status check.

Figure 19: User Chip Select with 7xh Status Check

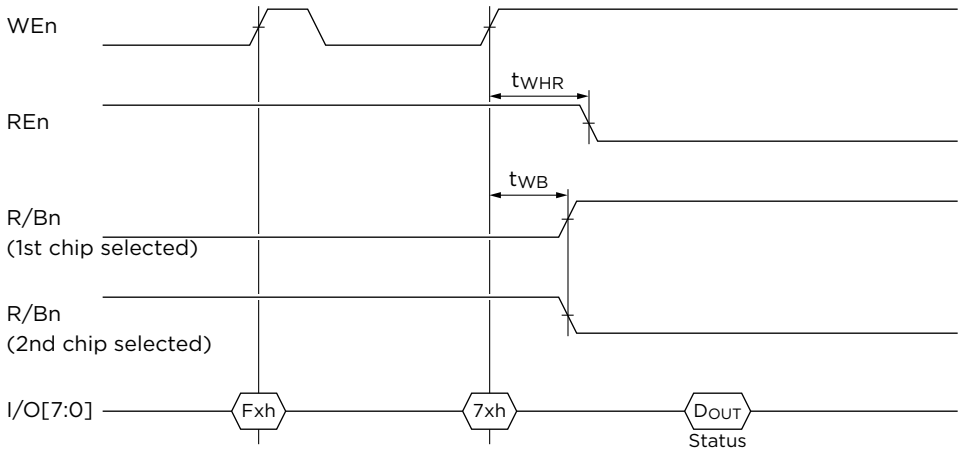
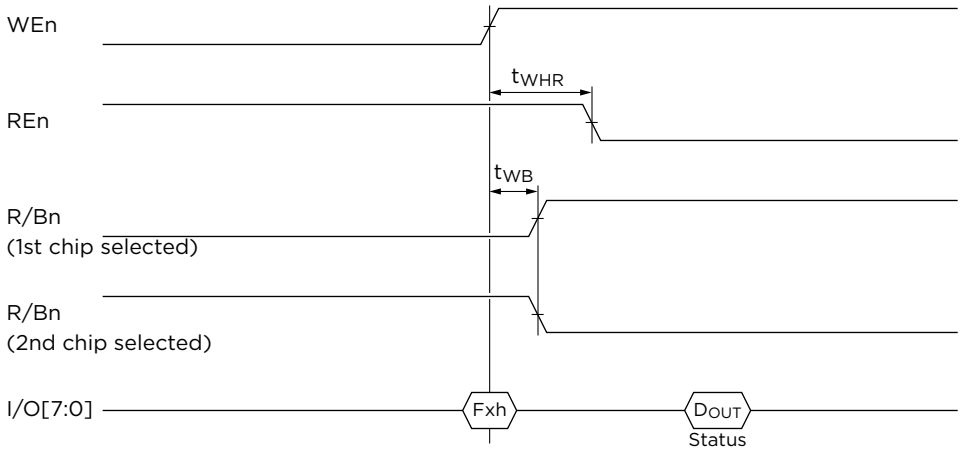


Figure 20: User Chip Select without 7xh Status Check



5.4.1 Multi-chip Chip Switching

Before switching the current chip selection from one chip to another chip, the user must wait tWB for the currently selected chip to go busy for execution. Until busy is achieved, issuing any command to another chip is prohibited, including prefix commands.

5.5 Read ID Operation

The device contains ID codes that can be used to identify the device type, the manufacturer, and device features. To read the proper ID codes, ***after*** power-up and device initialization (using an FFh Reset command) have completed, issue the 90h command followed by an 00h or a 40h address.

Figure 21: Read ID

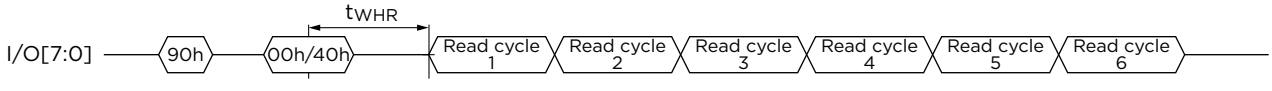


Table 19: SanDisk 00h ID Codes

Cycle	Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Code
1	Manufacturer Code	SanDisk	0	1	0	0	0	1	0	1	45h
2	Device Code (density per CEn)	TBD									TBD
3	Character Code	TBD									TBD
4	Organization Code	Block size: 50.625MB Page size: 16KB									TBD
5	Plane Information	TBD									TBD
6	Technology Code	Toggle Mode									TBD

Table 20: JEDEC 40h ID Codes

Cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Code
1	J	0	1	0	0	1	0	1	0	4Ah
2	E	0	1	0	0	0	1	0	1	45h
3	D	0	1	0	0	0	1	0	0	44h
4	E	0	1	0	0	0	1	0	1	45h
5	C	0	1	0	0	0	0	1	1	43h
6	Toggle Mode	0	0	0	0	0	0	1	0	02h

5.6 Read Unique ID

The 32-byte unique ID is stored in the device as two sets of four copies each, for a total of eight copies stored in different locations. Four copies are stored on WL11 and four copies are stored on WL35. Each unique ID byte holds different data. Within the unique ID, the 16 even bytes are true data and the 16 odd bytes are complement data. Both true and complement data should be checked for data integrity, as follows:

1. Take the bitwise majority from each of the "data" copies. Use all eight copies from both WLs. (Use only four copies when executing Steps 4 or 5.) If there is a bitwise majority, go to Step 2. If it fails (is tied), go to Step 4.

2. Take the bitwise majority from each of the "data bar" copies. Use all eight copies from both WLs. (Use only four copies when executing Steps 4 or 5.) If there is a bitwise majority, go to Step 3. If it fails (is tied), go to Step 4.

3. To ensure that the "data" and the "data bar" bitwise majorities are complementary, execute XOR. If the XOR is FFh, go to Step 6. If it is not FFh, go to Step 4.

4. Repeat Steps 1-3 on only the four copies on WL11. If there is a bitwise majority, go to Step 6. If it fails (is tied, or is not complementary), go to Step 5.

5. Repeat Steps 1-3 on only the four copies on WL35. If there is a bitwise majority, go to Step 6. If it fails (is tied, or is not complementary), abort this flow and fail the die.

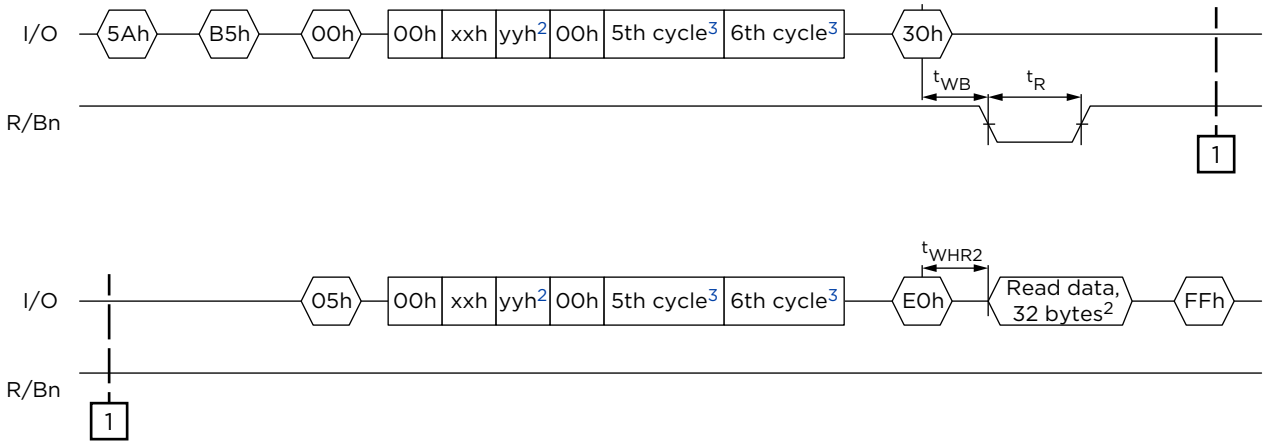
6. The data/data bar integrity is good for the bit pair. Repeat Steps 1–5 for each of the remaining data/data bar bit pairs to obtain the complete unique ID.

To read the unique ID for a given target, the 5Ah–B5h commands are prefixed to a Read command. The prefix commands are only accepted when the target is in the cache-ready or the true-ready state.

After the command sequence is issued, the target is busy for tR. Users can issue a Status Read or check the R/Bn pin to monitor operation status.

A Reset command is required to terminate a Read Unique ID operation.

Figure 22: Read Unique ID



Note 1. There are 32 total bytes. The 16 even bytes are true data; the 16 odd bytes are complement data.

2. The yyh is either **WL11** string 0 or **WL35** string 0.

3. For multi-die configurations, follow the table below for the fifth and sixth address cycles.

Die #	5th Cycle Address	6th Cycle Address
0	00h	00h
1	80h	00h
2	00h	01h
3	80h	01h

Table 21: Unique ID Address Locations

XXh (Second Cycle Address)	Description
00h 02h 04h 06h	Four copies of Unique ID stored in different locations

6 Operating Characteristics

The BiCS6 X4 1Tb 4-Plane NAND Flash device supports only Toggle Mode DDR operation from DDR2 through DDR5.

This device uses the Toggle Mode interface to achieve a high data-transfer rate, in which serial data in the register is output on the falling and rising edges of DQS. The controller also loads data into the device on the falling and rising edges of DQS.

DQS is bi-directional and is not used for commands or addresses; it is used only for data transfers. An even number of bytes is always transferred, satisfying the 2N Rule for data input/output as defined in section "4.3.4 2N Rule for Data Input/Output" on page 24.

In the Toggle Mode interface, the least significant bit of the column address is always 0. If the least significant bit of the column address is set to 1, the data will be corrupted.

The latching edge of DQS is aligned to the transition of the I/O bus for data transfers (D_{OUT}/D_{IN}) between the device and the controller.

6.1 Toggle Mode Interface

Device power-up is always in DDR2 mode with the default CTT setting. After the power supply is stable and V_{CC} and V_{CCQ} are within their normal operating ranges, a Reset command (FFh or FDh) must be issued to initialize the device.

Prior to initialization, only the Read ID command and the Status Read commands are accepted. Additionally, the device will operate at lower interface timing specifications both before and after initialization—and ***before*** interface training. See Table 22 for details.

Table 22: Interface Timing Before and After Initialization

Pre-Initialization	Rate	Frequency
Command and address input	≤ 33 MBps	33 MHz
Data input and output	≤ 66 MBps	33 MHz
Post-Initialization (before interface training)	**Rate**	**Frequency**
Commands and addresses follow normal specifications with:	tWC(min) = 10ns	100 MHz
Data follows normal specifications:		
Exception: Clock-frequency-dependent specs restrictions	TM4: ≤ 533 MBps	—
	TM5: ≤ 66 MBps	—
After Interface Training	**Rate**	**Frequency**
Commands and addresses follow normal specifications with:	tWC(min) = 10ns	100 MHz
Data transfer can operate at highest supported clock speeds	TM4: ≤ 1200 Mbps	≤ 600 MHz
	TM5: ≤ 2000 Mbps	≤ 1000 MHz

Note 1. See Table 23, “Pre-Initialization Timing Specifications,” on page 38

Table 23: Pre-Initialization Timing Specifications

Parameter	Description	Specifications		Unit
		Min	Max	
tADL	Address to data loading tim	400	—	ns
tALH	ALE hold time	5	—	ns
tALS	ALE setup time	15	—	ns
tAR	ALE low to REn low	10	—	ns
tCH	CEn hold time	5	—	ns
tCLH	CLE hold time	5	—	ns
tCLR	CLE low to REn low	10	—	ns
tCLS	CLE setup time	15	—	ns
tCR	CEn low to REn low	10	—	ns
tCS	CEn setup time	20	—	ns
tDH	Data hold time	5	—	ns
tDIPW	DQ input pulse width	0.31 × tDSC	—	ns
tDQSH	DQS input high pulse width	0.45 × tDSC	0.55 × tDSC	ns
tDQSL	DQS input low pulse width	0.45 × tDSC	0.55 × tDSC	ns
tDQSQ	Output data skew with respect to strobe	—	3	ns
tDQSRE	RE to DQS latency	—	25	ns
tDS	Data setup time	5	—	ns
tDSC	Data strobe cycle time	30	—	ns
tQH	Output hold from DQS	0.37 × tRC	—	ns
tQSH	Minimum high DQS Read pulse width	0.37 × tRC	—	ns
tQSL	Minimum low DQS Read pulse width	0.37 × tRC	—	ns
tRC	REn cycle time	30	—	ns
tWB	WEn high to busy	—	100	ns
tWC	Write cycle time	30	—	ns
tWH	WEn high hold time	11	—	ns
tWHR	WEn high to REn low	400	—	ns
tWP	Write pulse width	11	—	ns

6.1.1 Toggle Mode Interface Switching in DDR5

For DDR5 only, after device power up and initialization, the user can choose between the default CTT interface and the LTT interface. The Set Features commands with addresses 22h and 02h are used to switch from the CTT to the LTT interface, if desired. See Figure 23.

After selecting either the CTT or LTT interface, DCC training is required to optimize the device before initiating normal operation. See Figure 24, "CTT Interface Training Flow," on page 40 for CTT interface training and Figure 25, "LTT Interface Training Flow," on page 41 for LTT interface training.

Figure 23: CTT or LTT Interface Selection

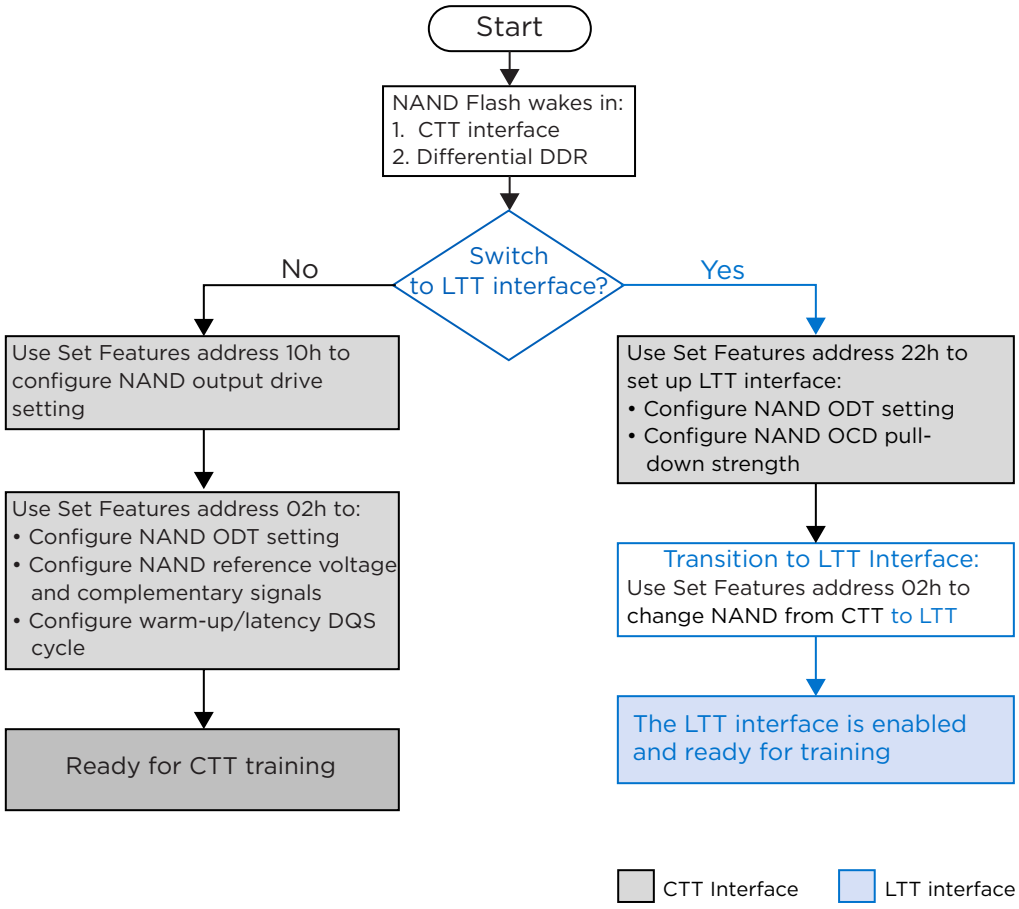
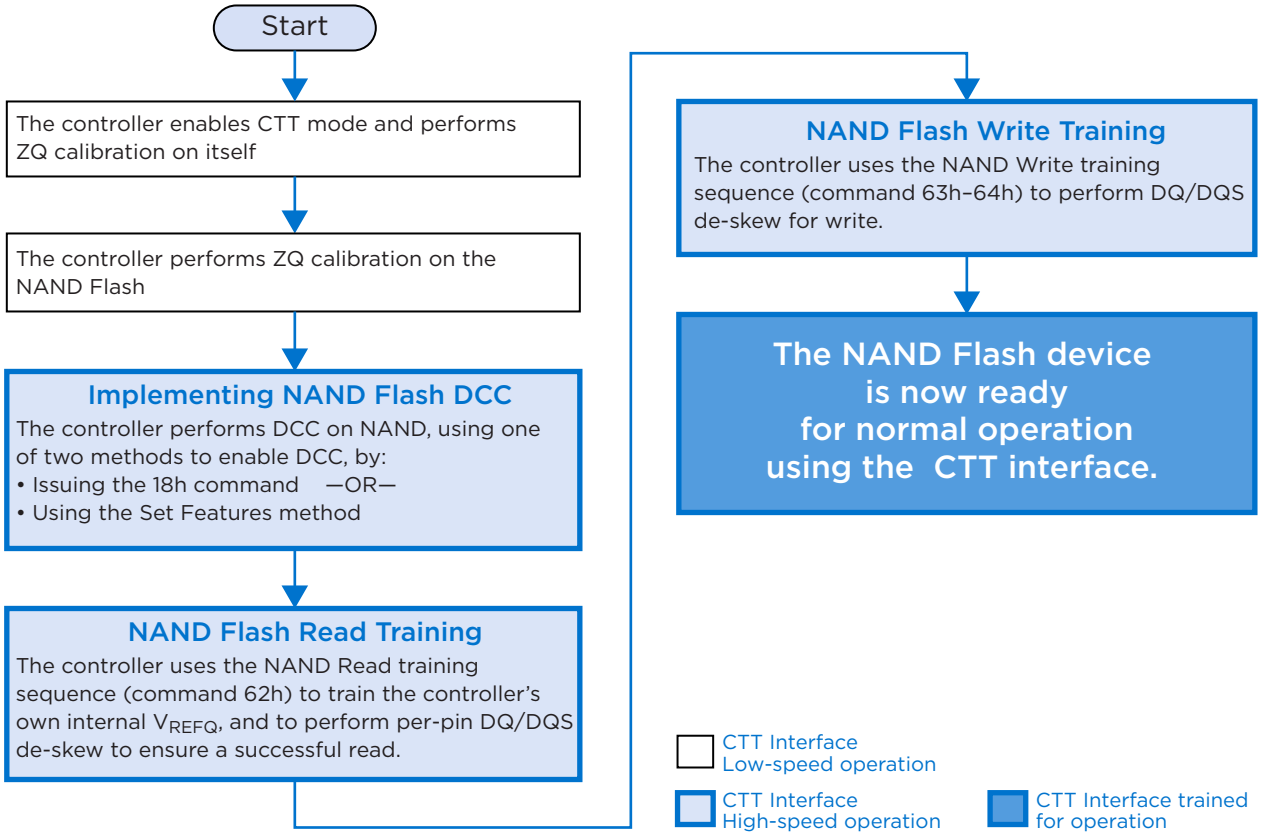


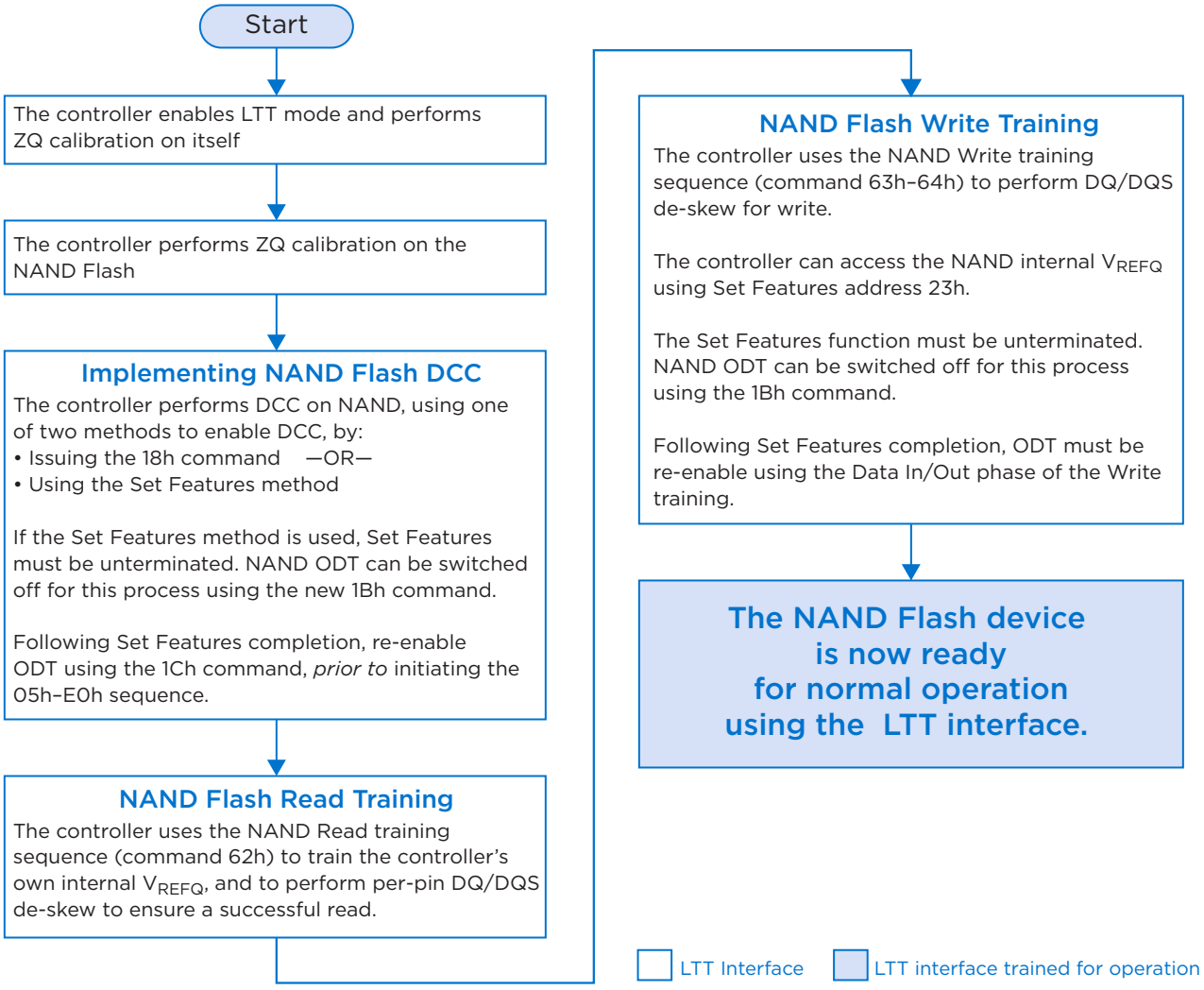
Figure 24: CTT Interface Training Flow



Additional information is available in the Applications Notes for DCC Training, Read Training, and Write Training for NAND Flash.

DRAFT Rev. 0.1 7/20/22

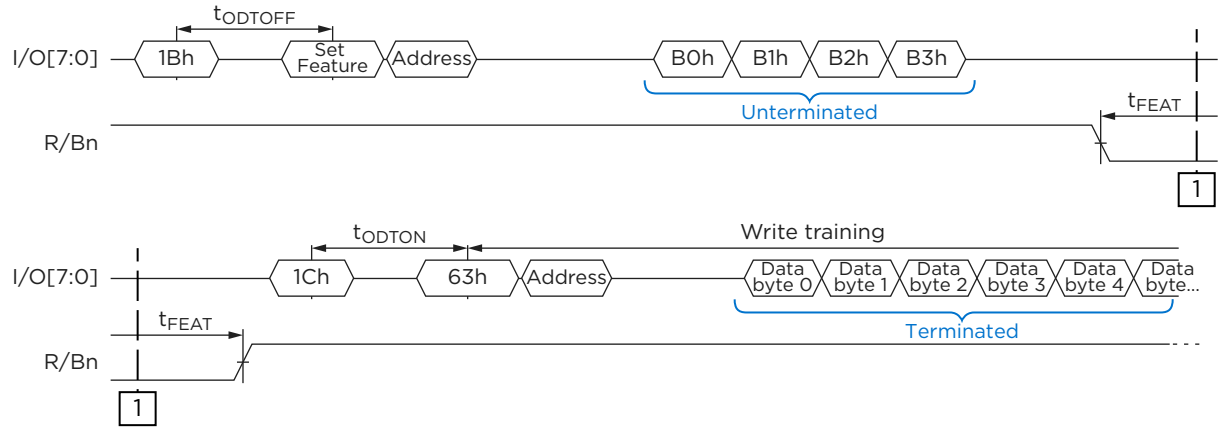
Figure 25: LTT Interface Training Flow



Note 1. See Figure 26, "Enable/Disable ODT for I/O Training," on page 42.

For additional information, contact your representative for the Applications Notes on DCC Training, Read Training, and Write Training for NAND Flash.

Figure 26: Enable/Disable ODT for I/O Training



Note 1. tODTOFF = 100ns (min); tODTON = 100ns (min)

2. tFEAT = 1µs (max), as defined in:
Table 44, “Toggle Mode AC Characteristics and Operating Conditions,” on page 56.

6.2 Single-Level-Cell (SLC) Mode

In addition to QLC operation, these devices support a single-level-cell (SLC) mode that can be used with data that requires frequent updates, high performance, and high reliability.

6.2.1 Switching to SLC Mode

After initial power-up, the device defaults to QLC mode. To operate in SLC mode, an A2h command must be added as a prefix to a Read, Program, or Erase command. A2h is a global command sent to every die with CEn set to low, and is compatible with Read, Program, and Erase commands as well as cache operations.

Data programmed in a block using one mode (QLC or SLC) must be read or erased using the same mode; that is, the mode cannot be switched within a block. Following a Read, Program, or Erase operation, SLC mode automatically resets to QLC operation.

A block assigned to operate in one mode (QLC or SLC) should remain set to operate in the same mode over the life of the device.

7 Device Ratings

Table 24: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	–0.6 to 4.6	V
V_{CCQ}		–0.3 to 2.4	V
V_{IN}	Input voltage	–0.6 to 2.4	V
$V_{I/O}$	Input/output voltage	–0.6 to 2.4	V
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	–40 to 85	°C

Note 1. Permanent device damage could occur if these Absolute Maximum Ratings are exceeded. Functional operations should be restricted to the recommended operating conditions in sections "8 Recommended Operating Conditions" on page 44 **through** "8.4 AC Operation" on page 56. Exposure to absolute maximum rating conditions for extended periods could affect the reliability and functionality of the device.

Table 25: Capacitance

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	—	1	pF
C_{IO}	Input/output capacitance	V_{OUT} = 0V	—	1	pF

Note 1. Capacitance is per die and is not 100% tested. Capacitance is measured at the chip level.

2. Input capacitance is applied only to I/O[7:0], DQS, and DQSn pins. R/Bn pin capacitance is 3pF.

8 Recommended Operating Conditions

Table 26: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC} [1, 2]	Supply voltage for 3.3V core	2.35	—	3.6	V
V_{CCQ} [1, 2]	Supply voltage for I/O signaling	1.14	1.2	1.30	V
V_{SS}	Ground voltage	0	0	0	V
V_{SSQ}	Ground voltage for I/O signaling	0	0	0	V
T_{CASE}	Operating temperature	0	—	70	°C

Note 1. The device supports: V_{CC} = 3.3V, V_{CCQ} = 1.2V

2. V_{CC} and V_{CCQ} are measured at their respective pads, balls, or pins.

8.1 Supported Features and Operating Conditions vs Data Transfer Rate

The NAND Flash features and the host features supported or required under different I/O operating frequencies are summarized in Table 27. Differential signaling is required for this device.

Table 27: Supported Features/Operating Conditions Comparison #1

Conditions vs Data Transfer Rate, V_{CCQ} = 1.2V

NAND Features/Conditions	≈ 100 MHz	≈ 200 MHz	≈ 400 MHz	≥ 600 MHz
I/O Type	**Availability**			
Single-ended signaling for DQS and RE	Not supported			
Differential signaling for DQS and RE	Supported			
ZQ Calibration	Supported			
Training: DCC	Not supported			Required
Training: Read, Write	Supported			
Termination				
CTT	Supported			
LTT	Supported			

The host and the NAND Flash must power up with the CTT interface enabled and with internal V_{REFQ} = V_{CCQ}/2, as defined in Table 28, “Supported Features/Operating Conditions Comparison #2,” on page 45. Further initialization and training are required to operate the device at higher data rates, and/or to operate in LTT mode. Differential signaling is required.

Both internal and external V_{REFQ} are supported for the CTT I/F; only internal V_{REFQ} is supported for the LTT I/F.

The host must ensure that the NAND internal V_{REFQ} is within the NAND minimum internal V_{REFQ}-supported range for the LTT interface ***prior to*** enabling the LTT interface. This constraint applies during any time that the LTT interface is active. External V_{REFQ} must always be disabled when the device runs in LTT mode.

Table 28: Supported Features/Operating Conditions Comparison #2

V_{REFQ} vs Data Transfer Rate, V_{CCQ} = 1.2V

Feature/Conditions			All Frequencies
V_{REFQ}	**Interface**	**Control**	**Availability**
	CTT	Internal V_{REFQ} (V_{CCQ}/2 setting)	Optional
		External V_{REFQ} (V_{CCQ}/2)	Optional
	LTT	Internal V_{REFQ}	Supported
		External V_{REFQ}	Not supported

8.2 DC Operation

Table 29: DC and Operating Characteristics

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max	Unit
Power-on Reset current	I_{CC0}	—	—	TBD	TBD	mA
Page Read operation current QLC/SLC	I_{CC1}	Spec does not guarantee erased data	—	TBD	TBD	mA
Program operation current	I_{CC2}	—	—	TBD	TBD	mA
Erase operation current	I_{CC3}	—	—	TBD	TBD	mA
I/O Read D_{OUT} current for V_{CC}	I_{CC4R}	C_{LOAD} = 0pF (I = 0mA) ; CEn = VIL, Half data switching tRC = 3.75ns (266 MHz) = 2.50ns (400 MHz) = 1.67ns (600 MHz) = 1.00ns (1000 MHz)	—	TBD	TBD	mA
I/O Write D_{IN} current for V_{CC}	I_{CC4W}	CEn = V_{IL}, Half data switching tDSC = 3.75ns (266 MHz) = 2.50ns (400 MHz) = 1.67ns (600 MHz) = 1.00ns (1000 MHz)	—	TBD	TBD	mA
I/O Read D_{OUT} current for V_{CCQ}	I_{CCQ4R}	C_{LOAD}=0pF (I = 0mA) ; CEn = V_{IL}, Half data switching tRC = 3.75ns (266 MHz) = 2.50ns (400 MHz) = 1.67ns (600 MHz) = 1.00ns (1000 MHz)	—	TBD	TBD	mA
I/O Write D_{IN} current for V_{CCQ}	I_{CCQ4W}	CEn = V_{IL}, Half data switching tDSC = 3.75ns (266 MHz) = 2.50ns (400 MHz) = 1.67ns (600 MHz) = 1.00ns (1000 MHz)	—	TBD	TBD	mA
Bus idle current, V_{CC}	I_{CC5}	—	—	—	TBD	mA
Bus idle current, V_{CCQ}	I_{CCQ5}	—	—	—	TBD	mA
Standby current, V_{CC}	I_{SB}[3]/ I_{CCS}	CEn = V_{CCQ} - 0.2V, WP = 0V/V_{CCQ}	—	—	TBD	µA
Standby current, V_{CCQ}	I_{SBQ}[3]/ I_{CCQS}	CEn = V_{CCQ} - 0.2V, WP = 0V/V_{CCQ}	—	—	TBD	µA

Table continues on next page

Table 29: DC and Operating Characteristics (cont'd)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max	Unit
Input leakage current	I_{LI}	V_{IN} = 0 to $V_{CCQ(max)}$	—	—	TBD	µA
Output leakage current	I_{LO}	PU: V_{OUT} = 0	—	—	TBD	µA
		PD: V_{OUT} = V_{CCQ}	—	—	TBD	µA
V_{REFQ}[4] leakage current		Leakage current in V_{REFQ} pin when driven externally	—	—	TBD	µA
Output low current (R/Bn pin)	I_{OL} (R/Bn)	V_{OL} = 0.2 V	TBD	TBD	—	mA

Note 1. All values are per die.

2. Typical value is measured at V_{CC} = 3.0V, T_A = 25°C. Not 100% tested.

3. I_{SBQ} and I_{CCQS} are measured with the I/O and DQS/DQSn pins floating.

4. V_{REFQ} is 0.5 × V_{CCQ}.

8.3 AC/DC Levels

8.3.1 AC/DC Levels for CTT

Table 30: CTT Interface: Single-Ended AC and DC Input Levels[1, 2]

Parameter	Symbol	Up to 600 MHz	> 600 MHz	Unit	Notes
DC input high for control signals	V_{IH} CNT (DC)	0.7 × V_{CCQ}		V	2
DC input low for control signals	V_{IL} CNT (DC)	0.3 × V_{CCQ}			
AC input high for control signals	V_{IH} CNT (AC)	0.8 × V_{CCQ}			
AC input low for control signals	V_{IL} CNT (AC)	0.2 × V_{CCQ}			
DC input high for DQ-related signals, w/o V_{REFQ}	V_{IH} DQrel (DC)	0.7 × V_{CCQ}			3, 4
DC input low for DQ-related signals, w/o V_{REFQ}	V_{IL} DQrel (DC)	0.2 × V_{CCQ}			
AC input high for DQ-related signals, w/o V_{REFQ}	V_{IH} DQrel (AC)	0.8 × V_{CCQ}			
AC input low for DQ-related signals, w/o V_{REFQ}	V_{IL} DQrel (AC)	0.1 × V_{CCQ}			

Note 1. For control and DQ-related signals

2. Control signals are: ALE, CLE, CEn, ODTn/WPn WEn.
3. DQ-related signals are: RE, REn, DQS, DQSn, DQ[7:0]
   For RE, REn, DQS, and DQSn, these are single-ended signal requirements.
4. These specifications apply to NAND Flash command and address bus cycles, and unterminated data-input cycles.

Table 31: CTT Interface: External Reference Voltage Requirements

Parameter	Symbol	MIn	Max	Unit	Notes
External reference voltage	V_{REFQ} (DC)	0.49 × V_{CCQ}	0.51 × V_{CCQ}	V	

Table 32: CTT Interface: Differential AC/DC Input Levels, Cross-Point

Parameter	Symbol	Up to 600 MHz	> 600 MHz	Unit	Notes
DC differential input	$V_{ID(DC)}$	0.160	0.160	V	1
AC differential input	$V_{ID(AC)}$	0.200	0.200		
AC differential input crosspoint	V_{IX}	0.5 × V_{CCQ} ± 0.12	0.5 × V_{CCQ} ± 0.08		2

Note 1. $V_{ID(DC)}$ and $V_{ID(AC)}$ specify the input differential voltage |VTR–VCP| required for switching, where VTR is the "true" input signal, and VCP is the "complementary" input signal. The minimum values are equal to $V_{IH(DC)}$ – $V_{IL(DC)}$ and $V_{IH(AC)}$ – $V_{IL(AC)}$ respectively.

2. For CTT, the typical value for V_{IX} is expected to be ≈ 0.5 × V_{CCQ} of the transmitting device, and V_{IX} is expected to track variations in V_{REFDQ}. V_{IX} indicates the voltage at which differential input signals must cross.

8.3.2 AC/DC Levels for LTT

Table 33: LTT Interface: Single-Ended AC and DC Input Levels[1, 2]

Parameter	Symbol	All Frequencies	Unit	Notes
DC input high for control signals	V_{IH}.CNT (DC)	0.7 × V_{CCQ}	V	2
DC input low for control signals	V_{IL}.CNT (DC)	0.3 × V_{CCQ}		
AC input high for control signals	V_{IH}.CNT (AC)	0.8 × V_{CCQ}		
AC input low for control signals	V_{IL}.CNT (AC)	0.2 × V_{CCQ}		
DC input high for DQ-related signals (unterminated)	V_{IH}.DQrel unterm (DC)	0.5 × V_{CCQ}		3, 4
DC input low for DQ-related signals (unterminated)	V_{IL}.DQrel unterm (DC)	0.080		
AC input high for DQ-related signals (unterminated)	V_{IH}.DQrel unterm (AC)	0.5 × V_{CCQ}		
AC input low for DQ-related signals (unterminated)	V_{IL}.DQrel unterm (AC)	0.060		
DC input high for DQ-related signals, for data input w/ V_{REFQ} (terminated)	V_{IH}.DQrel (DC)	V_{CENT}_DQ_{REL}+ 0.080		3, 4, 6
DC input low for DQ-related signals, for data input w/ V_{REFQ} (terminated)	V_{IL}.DQrel (DC)	V_{CENT}_DQ_{REL}+ 0.080		
AC input high for DQ-related signals, for data input w/ V_{REFQ} (terminated)	V_{IH}.DQrel (AC)	V_{CENT}_DQ_{REL}+ 0.100		3, 4, 7
AC input low for DQ-related signals, for data input w/ V_{REFQ} (terminated)	V_{IL}.DQrel (AC)	V_{CENT}_DQ_{REL}+ 0.100		

Note 1. For control and DQ-related signals

2. Control signals are: CEn, ODTn/WPn, ALE, CLE
3. DQ-related signals are: RE, REn, DQS, DQSn, DQ[7:0]
   For RE, REn, DQS, and DQSn, these are single-ended signal requirements.
4. Termination is disabled during command cycles, address cycles, and during data input/output cycles when ODT from NAND (target and non-target), and from the controller, are disabled.
5. V_{CENT}_DQrel must be regarded as V_{CENT}_RE, V_{CENT}_DQS, and V_{CENT}_DQ, for RE/REn, DQS/DQSn, and DQ[7:0] signals, respectively.
6. For DQ signals, DC signal requirements are replaced with the Rx Mask.
7. For DQ signals, AC signal requirements are replaced with the V_{IH}_AC and V_{IL}_AC specifications.

Table 34: LTT Interface: Differential AC/DC Input Levels, Cross-Point

Parameter	Symbol	Min	Max	Unit	Notes
DC differential input	$V_{ID(DC)}$	0.160	—	V	1
AC differential input	$V_{ID(AC)}$	0.200	—		
AC differential input crosspoint	V_{IX}	V_{REFDQ} – 0.064	V_{REFDQ} + 0.064		2

Note 1. $V_{ID(DC)}$ and $V_{ID(AC)}$ specify the input differential voltage |VTR–VCP| required for switching, where VTR is the "true" input signal, and VCP is the "complementary" input signal. The minimum values are equal to $V_{IH(DC)} - V_{IL(DC)}$, and $V_{IH(AC)} - V_{IL(AC)}$, respectively.

2. For LTT, the typical value for V_{IX} is expected to be ≈ V_{REFDQ} of the NAND Flash internal setting value by V_{REFQ} training, and V_{IX} is expected to track variations in V_{REFDQ}. V_{IX} indicates the voltage at which differential input signals must cross.

Table 35: AC and DC Output Levels for R/Bn Pin

Parameter	Symbol	CTT and LTT at 1.2 V_{CCQ}	Unit	Notes
DC output high for control signals (optional)	V_{OH}.CNT (DC)	0.7 × V_{CCQ} (min)	V	1, 2
DC output low for control signals (optional)	V_{OL}.CNT (DC)	0.3 × V_{CCQ} (max)		
AC output high for control signals (optional)	V_{OH}.CNT (AC)	0.8 × V_{CCQ} (min)		
DC output low for control signals (optional)	V_{OL}.CNT (AC)	0.2 × V_{CCQ} (max)		

Note 1. Control signal: R/Bn

2. V_{OL}.CNT(DC) (max) is specified with an I_{OL}(R/Bn) of 3mA.

8.3.3 CTT/LTT Interfaces in Use

Table 36: CTT and LTT Interface Parameters for Output Slew Rate Measurement

Parameter	I/F	Min	Typ	Max	Unit	Notes
V_{IL}(AC) to V_{IH}(AC)	CTT	0.85	1.0	1.67	RZQ/n	1, 2, 3
0.1 × V_{CCQ}	LTT	0.75	1.0	1.15	RZQ/n	3
0.33 × V_{CCQ}		0.85	1.0	1.15		
0.5 × V_{CCQ}		0.85	1.0	1.35		

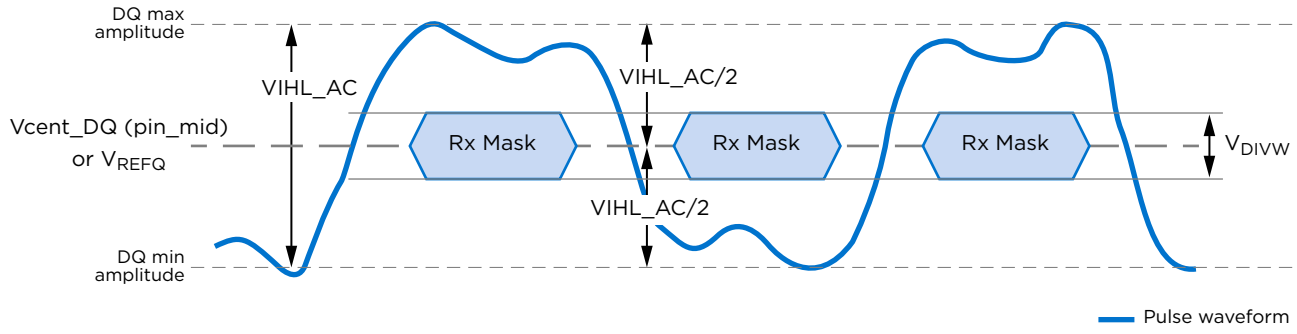
Note 1. Using the CTT interface, for data rates where Rx Mask is ***not*** used:
$V_{IL(AC)}$ = V_{IL}.DQrel (AC), ***and***
$V_{IH(AC)}$ = V_{IH}.DQrel (AC).

2. Using the CTT interface, for data rates where Rx Mask ***is*** used:
$V_{IL(AC)}$ = Vcent_DQ(pin_mid) – VIL_AC/2, ***and***
$V_{IH(AC)}$ = Vcent_DQ(pin_mid) + VIHL_AC/2.

3. All values are ***after*** ZQ calibration.

8.3.4 DQ Rx Mask

Figure 27: VIHL_AC Definition



Note 1. The minimum DQ AC input pulse amplitude (pk-pk) is defined by the VIHL_AC specification.

Table 37: VIHL_AC CTT and LTT Interface Specifications

V_{CCQ} = 1.2V

Parameter	Symbol	Interface	Min	Max	Unit	Notes
DQ AC input pulse amplitude pk-pk	VIHL_AC_CTT	CTT	220	—	mV	1, 2, 3
	VIHL_AC_LTT	LTT	200	—		

Note 1. The DQ-only input pulse amplitude must meet or exceed VIHL_AC at any point over the total UI, except when no transitions are occurring for that UI.

2. VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). For CTT interface, Vcent_DQ (pin_mid) is replaced by V_{REFQ} as the center reference level in the case where External V_{REFQ} is used or Internal V_{REFQ} without V_{REFQ} training is used.
3. There are no timing requirements above or below VIHL_AC levels.

8.3.5 Center-Tapped Termination (CTT) Specifications

Table 38: CTT Specifications

Parameter	Symbol	DDR5	Unit
DQ Rx mask voltage total	vDIVW_total	160	mV
DQ Rx mask timing window at Vcent_DQ (pin_mid)	tDIVW1	0.48	UI[1]
DQ Rx mask timing window at Vcent_DQ ± vDIVW_total/2	tDIVW2	0.30	UI
DQ input pulse width at Vcent_DQ (pin_mid)	tDIPW	0.66	UI

Note 1. UI = Unit interval = width of data window in DDR. UI = tDSC/2 or tRC/2

Figure 28: CTT DQ R_X Mask

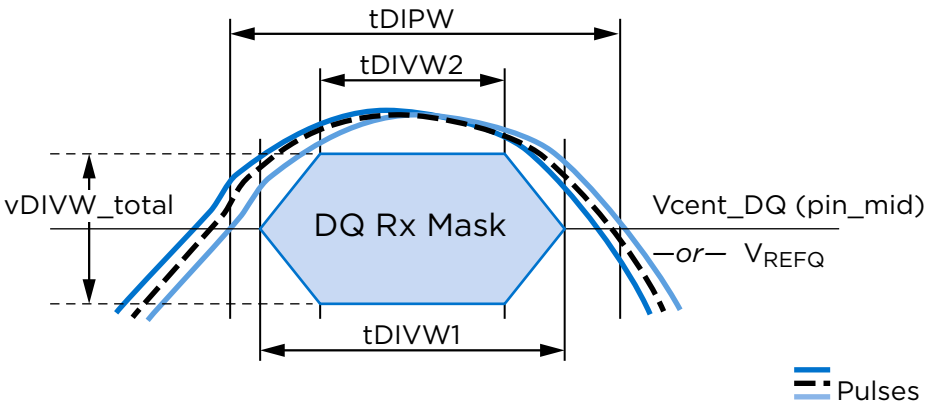


Table 39: CTT Options for Drive Strength and Termination

CTT Drive Strength Options		
Setting	**Drive Strength**	**RZQ Unit**
Nominal	37.5 Ohms	RZQ/8
Underdrive	50 Ohms	RZQ/6
CTT Termination Options		
Termination	**RZQ Unit**	
50 Ohms	RZQ/6	
75 Ohms	RZQ/4	
100 Ohms	RZQ/3	
150 Ohms	RZQ/2	

8.3.6 Low-Tapped Termination (LTT) Specifications

Table 40: LTT Specifications

Parameter	Symbol	DDR5 at 1000 MHz	Unit
DQ Rx mask voltage total	vDIVW_total	160	mV
DQ Rx mask timing window at Vcent_DQ (pin_mid)	tDIVW1	0.48	UI
DQ Rx mask timing window at Vcent_DQ ± vDIVW_total/2	tDIVW2	0.30	UI
DQ input pulse width at Vcent_DQ (pin_mid)	tDIPW	0.66	UI

Note 1. UI = Unit interval = width of data window in DDR. UI = tDSC/2 or tRC/2

Figure 29: LTT DQ R_X Mask

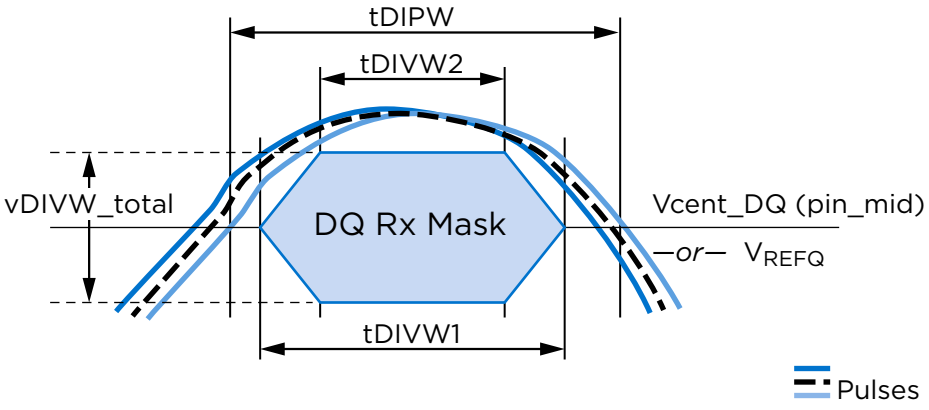


Table 41: LTT Pull-up Specifications

LTT V_{OH} Pull-up (V_{OH} pu), typ	V_{OH}, typ(mV)	Min	Typ	Max	RZQ Unit
V_{CCQ}/3 (default)	400	0.85	1	1.15	V_{OH}, typ
V_{CCQ}/2.5 (optional)	480	0.85	1	1.15	V_{OH}, typ

Table 42: LTT Options for Pull-down and Termination

LTT Pull-down Options	
Drive Strength	**RZQ Unit**
37.5 Ohms	RZQ/8
50 Ohms	RZQ/6
75 Ohms	RZQ/4
100 Ohms	RZQ/3
150 Ohms	RZQ/2
300 Ohms	RZQ/1

LTT Termination Options (NAND Side)	
Termination	**RZQ Unit**
37.5 Ohms	RZQ/8
50 Ohms	RZQ/6
75 Ohms	RZQ/4
100 Ohms	RZQ/3

LTT Termination Options (Channel Termination)	
Termination[1]	**RZQ Unit**
37.5 Ohms	RZQ/8
50 Ohms	RZQ/6
75 Ohms	RZQ/4
100 Ohms	RZQ/3
150 Ohms	RZQ/2
300 Ohms	RZQ/1

Note 1. If the user chooses the $V_{CCQ}/2.5$ pull-up option (see Table 41, "LTT Pull-up Specifications," on page 53), the channel ODT option is limited to ≥ 75 ohms.

8.3.7 AC Differential Input/Output

Table 43: AC Differential Input/Output Parameters (V_{CCQ} only)

Symbol	Parameter	Up to 600 MHz	> 600 MHz	Unit
$V_{IX(AC)}$[1, 3]	AC differential input crosspoint	$0.5 \times V_{CCQ} \pm 0.12$	$0.5 \times V_{CCQ} \pm 0.08$	V
$V_{OX(AC)}$[2, 3]	AC differential output crosspoint	$0.5 \times V_{CCQ} \pm 0.15$	$0.5 \times V_{CCQ} \pm 0.15$	V

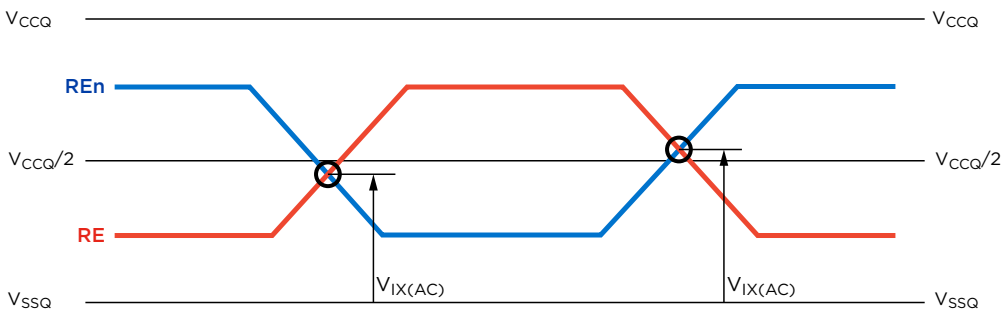
Note 1. The typical value for $V_{IX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

2. The typical value for $V_{OX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ}. $V_{OX(AC)}$ indicates the voltage at which differential input signals must cross.
3. Verified by design and characterization; not tested in production.

8.3.8 AC Characteristics: Differential Input

$V_{IX(AC)}$ indicates the voltage at which differential input signals cross. It is used to track variations in $V_{CCQ}/2$. Each individual component of a differential signal must meet the DC requirements in Table 29, “DC and Operating Characteristics,” on page 46.

Figure 30: Differential Input Signal



8.4 AC Operation

8.4.1 Toggle Mode AC Operation

Toggle Mode AC timing specs are characterized at the die level. Depending on the actual system design, output at the system level could vary. Customers must perform characterization to guarantee their system level performance.

Table 44: Toggle Mode AC Characteristics and Operating Conditions

T_{CASE} = 0 to 70°C, V_{CC} = 2.35–3.6V, V_{CCQ} = 1.2V (1.14–1.30V)

Symbol	Parameter	V_{CCQ} = 1.14–1.30V All frequencies			Unit
		Min	Typ	Max	
tADL	Address to data load time	300	—	—	ns
tAR	ALE low to REn low	10	—	—	ns
tCAH	Command/address hold time	3	—	—	ns
tCALH	CLE/ALE hold time	3	—	—	ns
tCALS	CLE/ALE setup time	15	—	—	ns
tCALS2	CLE/ALE setup time, when ODT is enabled	25	—	—	ns
tCALS3[1]	CLE/ALE setup time (conditional spec)	3	—	—	ns
tCAS	Command/address setup	3	—	—	ns
tCDQSH	DQS hold time for data input finish	100	—	—	ns
tCDQSS[2]	DQS setup time for data input start	100	—	—	ns
tCH	CEn hold time	5	—	—	ns
tCHZ	CEn high to output High-Z	—	—	30	ns
tCLHZ	CLE high to output High-Z	—	—	30	ns
tCLR	CLE to REn low	10	—	—	ns
tCOH	Data output hold time from CEn high	5	—	—	ns
tCR	CEn low to REn low	10	—	—	ns
tCS	CEn setup time	20	—	—	ns
tCS2	CEn setup time when ODT is enabled	30	—	—	ns
tCWAW	Command write cycle to address write cycle time for random data input	300	—	—	ns
tDQSRE	REn to DQS and I/O delay	—	—	25	ns
tFEAT	Set/Get Features busy time	—	—	1	µs
tPOR	Power-on Reset time	—	2	5	ms
tPS	Delay from power-up to CEn	100	—	—	µs
tRPP	Read pulse width for Status Reads	30	—	—	ns
tRPRE	Read preamble	15	—	—	ns
tRPRE2	Read preamble with ODT enabled	30	—	—	ns

Table continues on next page

Table 44: Toggle Mode AC Characteristics and Operating Conditions (cont'd)

T_{CASE} = 0 to 70°C, V_{CC} = 2.35–3.6V, V_{CCQ} = 1.2V (1.14–1.30V)

Symbol	Parameter	V_{CCQ} = 1.14–1.30V All frequencies			Unit
		Min	Typ	Max	
tRPSTH	Read postamble hold	25	—	—	ns
tRR	Ready to REn falling edge	5	—	—	ns
tRST	Device reset time (Ready/Read/Program/Erase)	—	—	10/10/30/100	µs
tRW[3]	Ready to WEn falling edge	20	—	—	ns
tWB	WEn high to busy	—	—	100	ns
tWC	Write cycle time	10	—	—	ns
tWH	WEn high pulse width	0.45 × tWC	—	—	ns
tWHR	WEn high to REn low	120	—	—	ns
tWHR2	WEn high to REn low for random data output	250	—	—	ns
tWP	WEn low pulse width	0.45 × tWC	—	—	ns
tWPRE	Write preamble	15	—	—	ns
tWPRE2	Write preamble when ODT is enabled	25	—	—	ns
tWPST	Write postamble	6.5	—	—	ns
tWPSTH	Write postamble hold time	25	—	—	ns
tWW	WPn high to WEn high	100	—	—	ns

Note 1. The first command or address following CEn low must always follow the tCALS = 15ns specification. For subsequent commands/addresses with CEn held low, if ALE/CLE low to ALE/CLE high is less than 10ns, follow the tCALS3 = 3ns specification; otherwise, follow the tCALS = 15ns spec. See Figure 31, "tCALS3 Operation," on page 58.

2. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

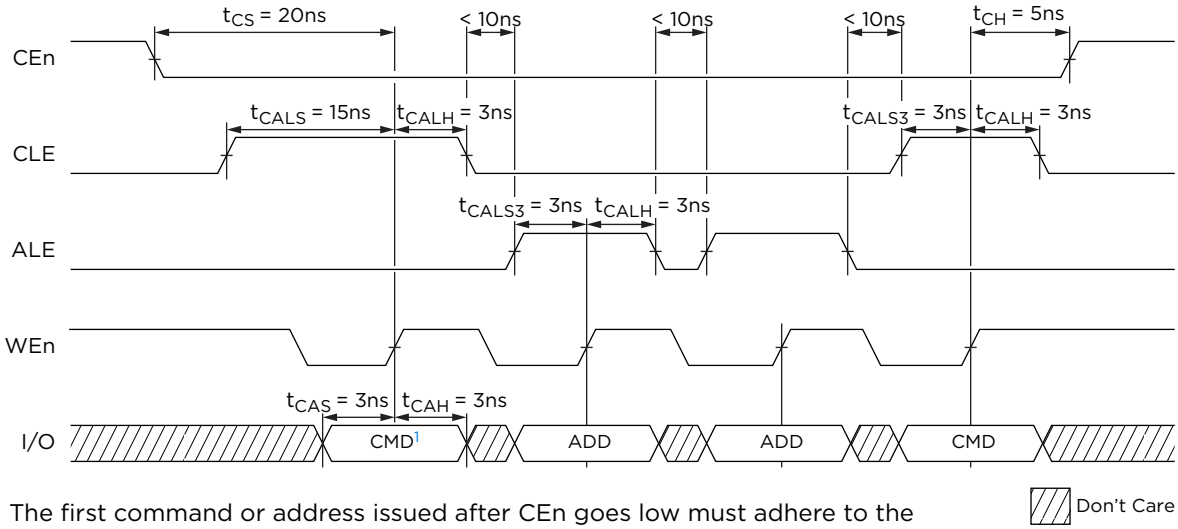
   There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

3. tRW is used to address the status timing mismatch between R/Bn and the interval status. If R/Bn status will not be checked, the tRW spec can be ignored.

4. Use tRC (min) = 30ns and tWC (min) = 30ns prior to initialization (see Table 23, "Pre-Initialization Timing Specifications," on page 38).

Figure 31: tCALS3 Operation

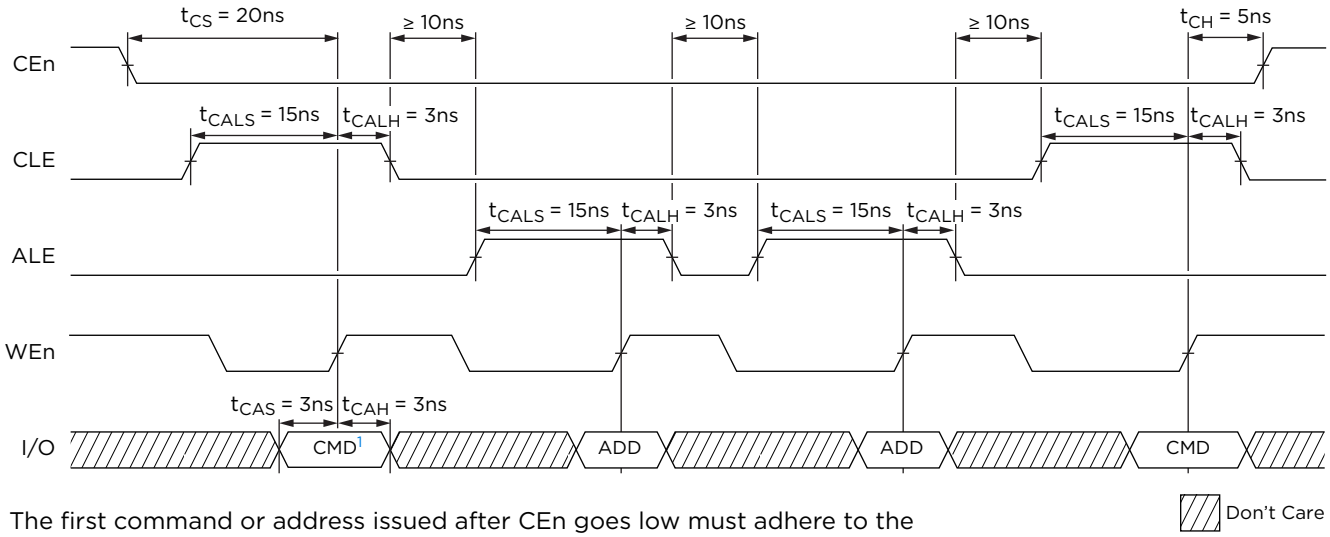
ALE/CLE Transition Under 10ns



The first command or address issued after CEn goes low must adhere to the specification tCALS = 15ns. For subsequent commands or addresses issued while CEn is held low:

If ALE/CLE low to ALE/CLE high is less than 10ns, then follow tCALS = 3ns.

ALE/CLE Transition at or Exceeding 10ns



The first command or address issued after CEn goes low must adhere to the specification tCALS = 15ns. For subsequent commands or addresses issued while CEn is held low:

If ALE/CLE low to ALE/CLE high is greater than 10ns, then follow tCALS = 15ns.

Table 45: AC Characteristics for DDR2/DDR3, V_{CCQ} = 1.2V

T_{CASE} = 0 to 70°C, V_{CC} = 2.35–3.6V, V_{CCQ} = 1.2V (1.14–1.30V)

Symbol	Parameter	DDR2 (≤ 266 MHz) No Training		DDR3 (> 266 to 400MHz)[1] No Training		Unit
		Min	Max			
tDQSH/ tDQSL	DQS input high/low pulse width at crosspoint (absolute)	0.45 × tDSC	0.55 × tDSC	0.45 × tDSC	0.55 × tDSC	ps
tDQSQ[2]	Output skew among data output and corresponding DQS	—	188	—	188	ps
tDS/tDH[2]	Data setup/hold time	200/200	—	200/200	—	ps
tDSC	Data strobe cycle time	2500	—	2500	—	ps
tDVW	Output data-valid window, no training	tQH – tDQSQ	—	tQH – tDQSQ	—	ps
tQH	Output hold time from DQS	0.36 × tRC – RE/REn_jitter (random)	—	0.36 × tRC – RE/REn_jitter (random)	—	ps
tQHS[2]	DQS hold skew factor	—	188	—	188	ps
tQSH/ tQSL[2]	DQS output high/low pulse width w/o DCC training at crosspoint	tREH/tRP – 0.06 × tRC	—	tREH/tRP – 0.06 × tRC	—	ps
tRC	Read cycle time	3750	—	2500	—	ps
tREH/tRP	REn high/low pulse width at crosspoint (absolute)	0.45 × tRC	0.55 × tRC	0.45 × tRC	0.55 × tRC	ps
tRPST	Read postamble	tDQSRE + 0.5 × tRC	—	tDQSRE + 0.5 × tRC	—	ps

Note 1. Duty Cycle Correction (DCC) training is mandatory for frequencies higher than 600 MHz.

2. DDR2/DDR3 = differential REn and DQS.

3. Use tRC (min) = 30ns and tWC (min) = 30ns prior to initialization (see Table 23, “Pre-Initialization Timing Specifications,” on page 38).

Table 46: AC Characteristics and Training for DDR4/DDR5, V_{CCQ} = 1.2V

T_{CASE} = 0 to 70°C, V_{CC} = 2.35–3.6V, V_{CCQ} = 1.2V (1.14–1.30V)

Symbol	Parameter	DDR4 (≥ 400 to 600 MHz)[1] w/Per-pin & DCCTraining		DDR5 (≥ 600 to 1000 MHz)[1] w/Per-pin & DCCTraining		Unit
		Min	Max	Min	Max	
tDIPW	DQ input pulse width	Note 4	—	Note 4	—	ps
tDQSH/ tDQSL	DQS input high/low pulse width at crosspoint (absolute)	0.45 × tDSC	0.55 × tDSC	0.45 × tDSC	0.55 × tDSC	ps
tDQSQ[2]	Output skew among data output and corresponding DQS	—	188	—	225	ps
tDQS2DQ	DQS to DQ skew at NAND Flash pin w/DCC training	—	—	—	± 200	ps
tDQ2DQ	DQ to DQ skew at NAND Flash pin w/DCC training	—	—	—	100	ps
tDS/tDH[2]	Data setup/hold time	200/200	—	—	—	ps
tDS + tDH	tDS + tDH with training	Note 4	—	Note 4	—	ps
tDSC	Data strobe cycle time	1667	—	1000	—	ps
tDVWp	Output data-valid window, with per-pin training, with DCC training	0.32 × tRC – RE/REn_ jitter (random)	—	0.285 × tRC – RE/REn_ jitter (random)	—	ps
tQH	Output hold time from DQS	0.36 × tRC – RE/REn_ jitter (random)	—	—	—	ps
tQHS[2]	DQS hold skew factor	—	188	—	—	ps
tQSH/ tQSL[2]	DQS output high/low pulse width w/DCC training at crosspoint	0.42 × tRC – RE/REn_ jitter (random)	—	0.42 × tRC – RE/REn_ jitter (rand)	—	ps
tRC	Read cycle time	1667	—	1000	—	ps
tREH/tRP	REn high/low pulse width at crosspoint (absolute)	0.45 × tRC	0.55 × tRC	0.45 × tRC	0.55 × tRC	ps
tRPST	Read postamble	tDQSRE + 0.5 × tRC	—	tDQSRE + 0.5 × tRC	—	ps

Note 1. Duty Cycle Correction (DCC) training is mandatory for frequencies higher than 600 MHz.

2. DDR4/DDR5 = differential REn and DQS.

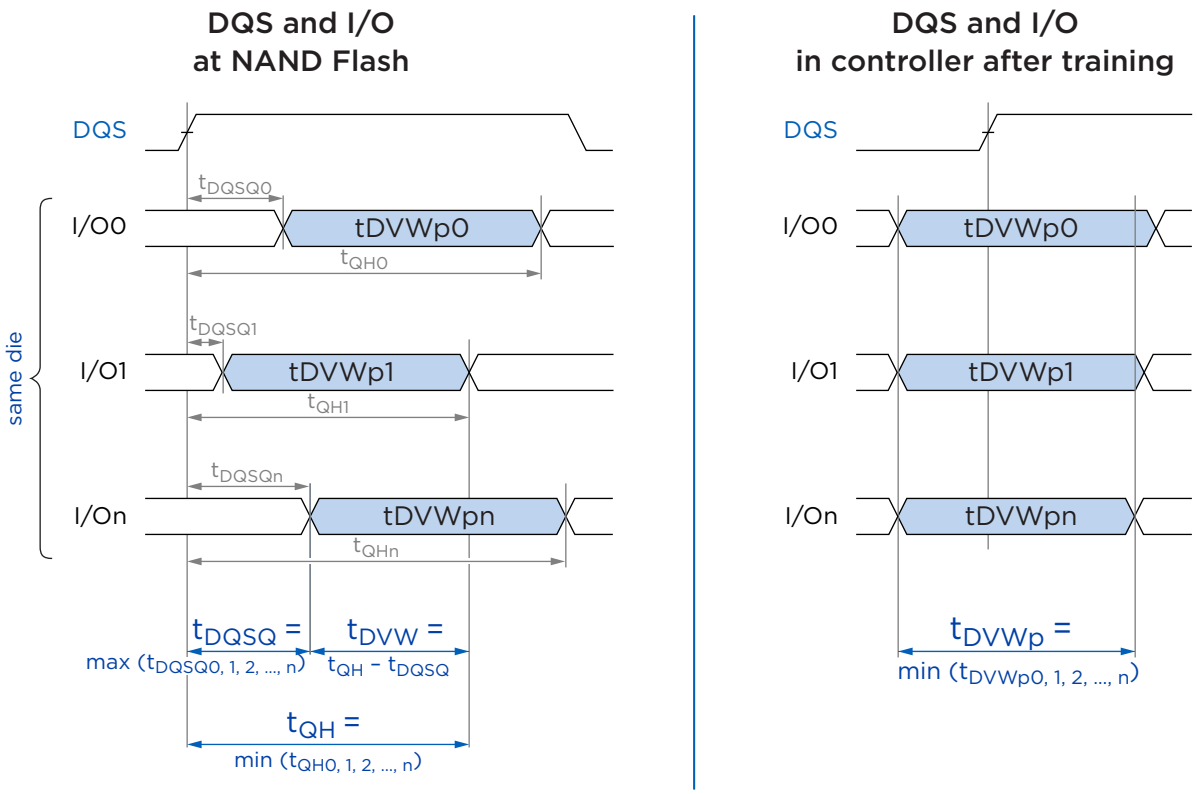
3. Valid window training is required for each pin (see Figure 32, "DDR4/DDR5 Training Effects with tDVWp Per-Pin Training at or Above 600 MHz," on page 61).

4. Not simulated in design. See sections "8.3.5 Center-Tapped Termination (CTT) Specifications" on page 52 **and** "8.3.6 Low-Tapped Termination (LTT) Specifications" on page 53. Use tRC (min) = 30ns and tWC (min) = 30ns prior to initialization (see Table 23, "Pre-Initialization Timing Specifications," on page 38).

8.4.1.1 Per-Pin and DCC Training for DDR4 and DDR5

Per-DQ-pin training is required for optimal tDQSQ performance at higher frequencies (600 MHz and above), by aligning the timing between the memory and the controller.

Figure 32: DDR4/DDR5 Training Effects with tDVWp Per-Pin Training at or Above 600 MHz

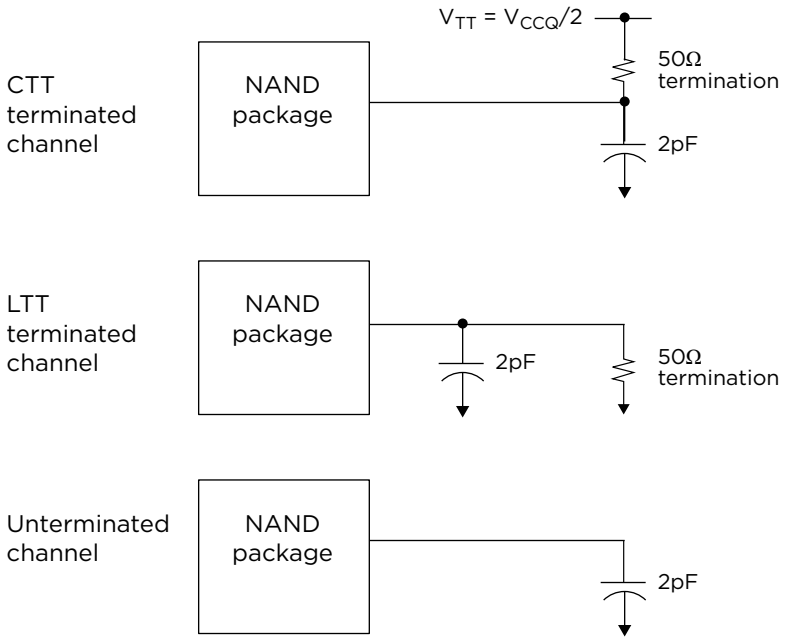


Note 1. DCC training is mandatory for frequencies higher than 600 MHz.
2. DDR2, DDR3, DDR4, and DDR5 are differential REn and DQS.
3. Valid window training is required for each pin.

8.4.2 Output-Timing Reference Loads

Output-timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to their system environment.

Figure 33: Output-Timing Reference Loads



8.4.3 Ready/Busy (R/Bn)

The Ready/Busy signal indicates device operation status. When it is low, R/Bn indicates that the device is busy because a Read, Program, Erase, or Reset operation is under way; it goes high upon completion of the operation, indicating that the device is now ready. It is also possible to determine device status by polling the status register of each die. See section "12.2 Read Status Enhanced" on page 112 for information on polling the die status registers.

R/Bn is an open-drain output and does not float to High-z when the chip is deselected or when outputs are disabled. R/Bn requires a pull-up resistor for correct operation, and the resistor selected must support the requirements of the specific system design. Designers should take into account the expected capacitive loading and desired performance to ensure that the selected resistor will provide optimal functionality.

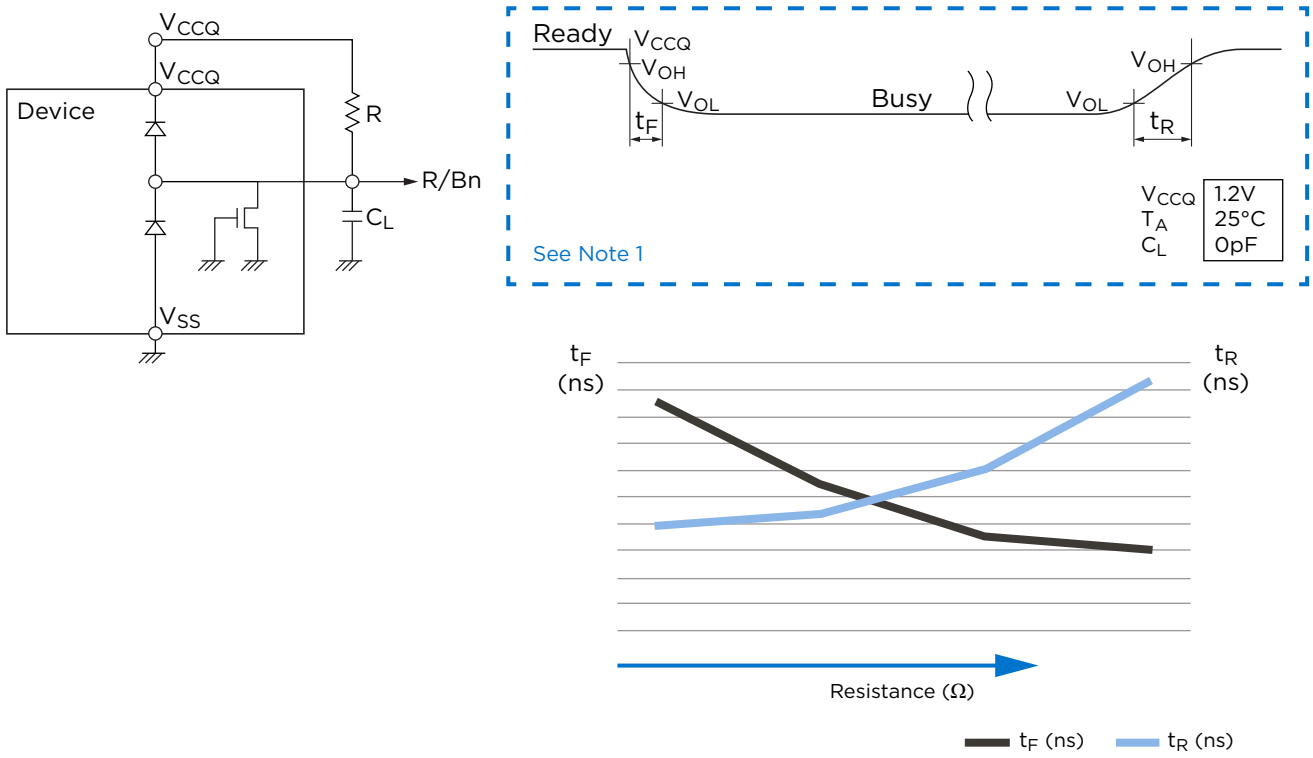
The output voltage (V_O), at the R/Bn pin at any time (t), can be calculated using these formulas:

$$V_O = V_{CCQ} \times (1 - e^{-t/\tau})$$

$$\tau = R \times C_L$$

Where R is the pull-up resistor value, and C_L is the total capacitance value of the R/Bn pin in Figure 34, "Open-Drain Pull-up Resistor and Diode Details," on page 64.

Figure 34: Open-Drain Pull-up Resistor and Diode Details



Note 1. V_{OH} and V_{OL} are defined as 80% and 20% of V_{CCQ} level.

8.5 Toggle Mode Characteristics

8.5.1 AC Overshoot/Undershoot

This device could have AC overshoot or undershoot from V_{CCQ} and V_{SS} levels. The maximum values that AC overshoot or undershoot can attain are provided in Table 47 **and** Table 48.

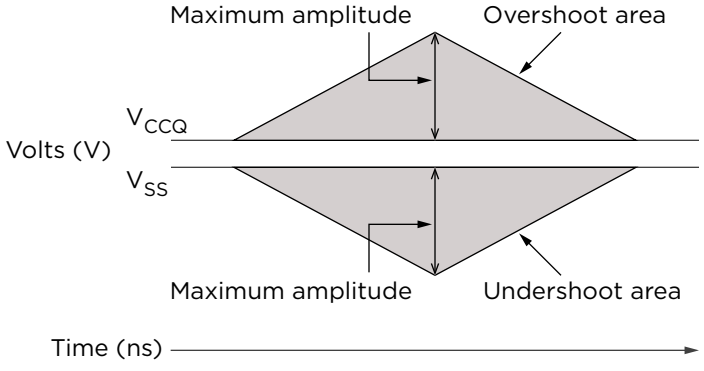
Table 47: CTT and LTT AC Overshoot/Undershoot Requirements (≈ 200 MHz to ≈ 600 MHz)

Parameter	Maximum Value						Unit
	≈ 200 MHz	≈ 266 MHz	≈ 333 MHz	≈ 400 MHz	≈ 533 MHz	≈ 600 MHz	
Max. peak amplitude supported for overshoot area	0.30						V
Max. peak amplitude supported for undershoot area	0.30						V
Max. overshoot area above V_{CCQ}	0.40	0.30	0.24	0.20	0.15	0.13	V × ns
Max. undershoot area below V_{SSQ}	0.40	0.30	0.24	0.20	0.15	0.13	V × ns

Table 48: CTT and LTT AC Overshoot/Undershoot Requirements (at or above 800 MHz)

Parameter	Maximum Value			Unit
	≈ 800 MHz	≈ 900 MHz	≈ 1000 MHz	
Max. peak amplitude supported for overshoot area	0.30			V
Max. peak amplitude supported for undershoot area	0.30			V
Max. overshoot area above V_{CCQ}	0.10	0.09	0.08	V × ns
Max. undershoot area below V_{SSQ}	0.10	0.09	0.08	V × ns

Figure 35: AC Overshoot/Undershoot Definition



8.6 I/O Drive Strength

This device can be configured with multiple drive strengths and termination impedance options using the Set Features command. The options depend on whether Center-Tapped Termination or Low-Tapped Termination is used.

Select the appropriate drive strength setting based on memory-bus loading.

A device that supports only an asynchronous data interface could support all or a subset of the noted drive strength settings, but must, at a minimum, support the nominal drive strength setting. See Table 39, “CTT Options for Drive Strength and Termination,” on page 52.

8.7 Input/Output Slew Rate

The test conditions specified in Table 51, "Output Slew Rate Requirements," on page 74, **and** in Table 52, "Test Conditions for Output Slew Rate," on page 74, must be used to verify output slew rates.

8.7.1 Input Slew Rate De-Rating

When using DQ signals for input, the total required data setup (tDS) time and data hold (tDH) time is calculated by adding a de-rating value to the tDS and tDH values provided in Table 44, "Toggle Mode AC Characteristics and Operating Conditions," on page 56.

Notice: Data setup/hold time (tDS/tDH), is measured from the data signal (I/O) crossing V_{REFQ} to the clock (DQS, DQSn) crosspoint.

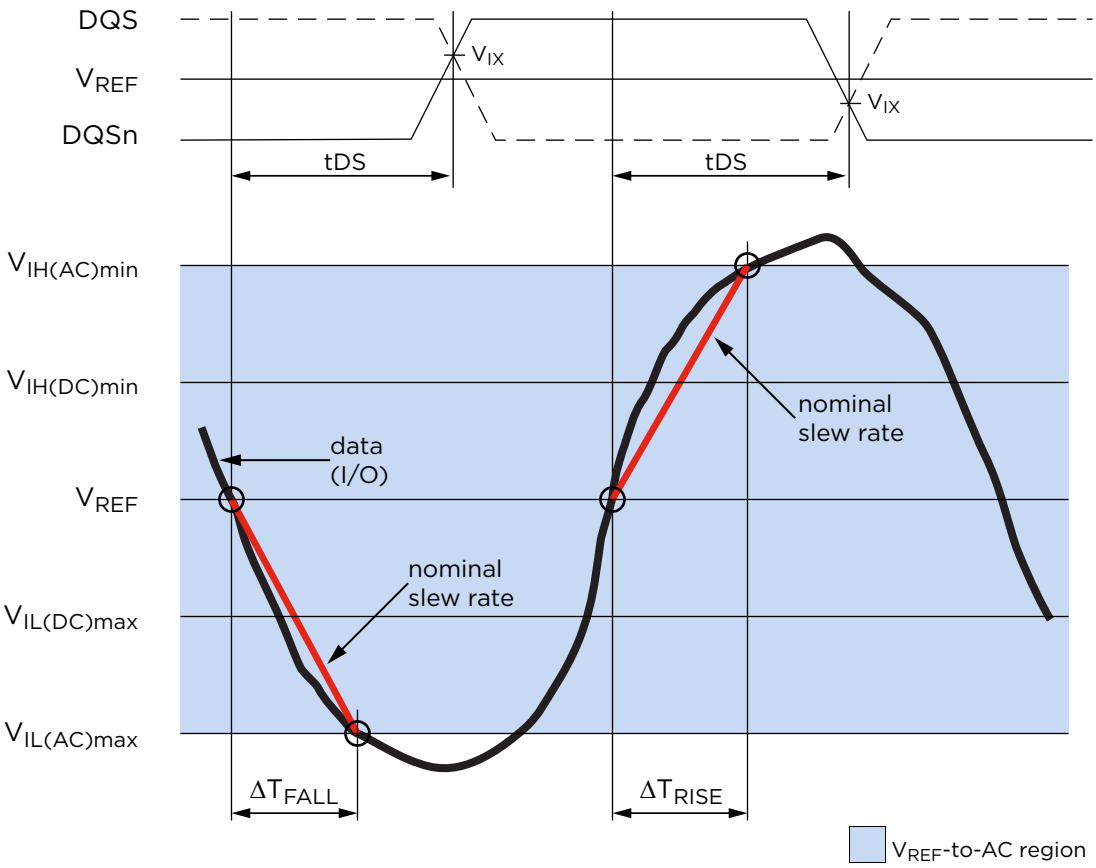
To calculate the total data setup time, tDS is incremented by the appropriate Δset de-rating value. To calculate the total data hold time, tDH is incremented by the appropriate Δhold de-rating value. Table 49, "Input Slew Rate De-rating Table for DQ and Differential DQS: VCCQ = 1.2V—Part I," on page 72 provides input slew rate de-rating values for DQ and differential DQS.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC)min}$. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REFQ} and the first crossing of $V_{IL(AC)min}$.

If the actual signal is always earlier than the nominal slew rate line within the shaded V_{REF}-to-AC region, then the de-rating value uses the nominal slew rate shown in Figure 36, "Nominal Slew for Data Setup Time (tDS)," on page 68.

If the actual signal is later than the nominal slew rate line anywhere within the shaded V_{REF}-to-AC region, then the de-rating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level, as shown in Figure 37, "Tangent Line for Data Setup Time (tDS)," on page 69.

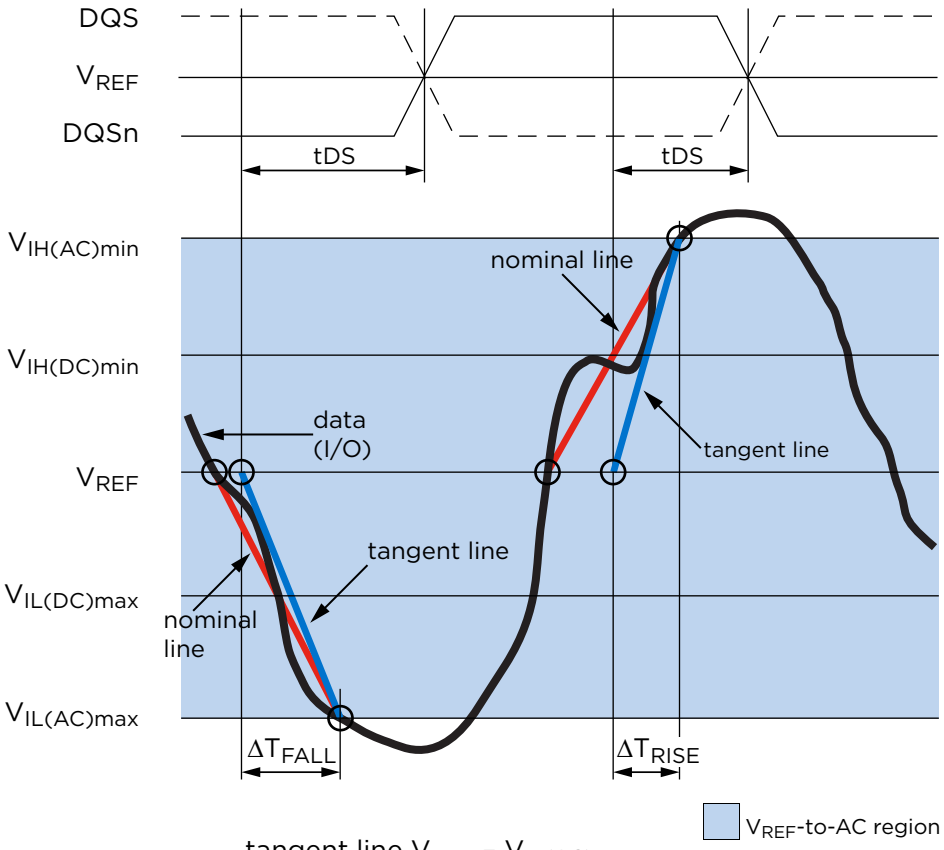
Figure 36: Nominal Slew for Data Setup Time (tDS)



$$\text{Setup slew rate falling signal} = \frac{V_{REF} - V_{IL(AC)max}}{\Delta T_{FALL}}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF}}{\Delta T_{RISE}}$$

Figure 37: Tangent Line for Data Setup Time (tDS)



$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } V_{REF} - V_{IL(AC)max}}{\Delta T_{FALL}}$$

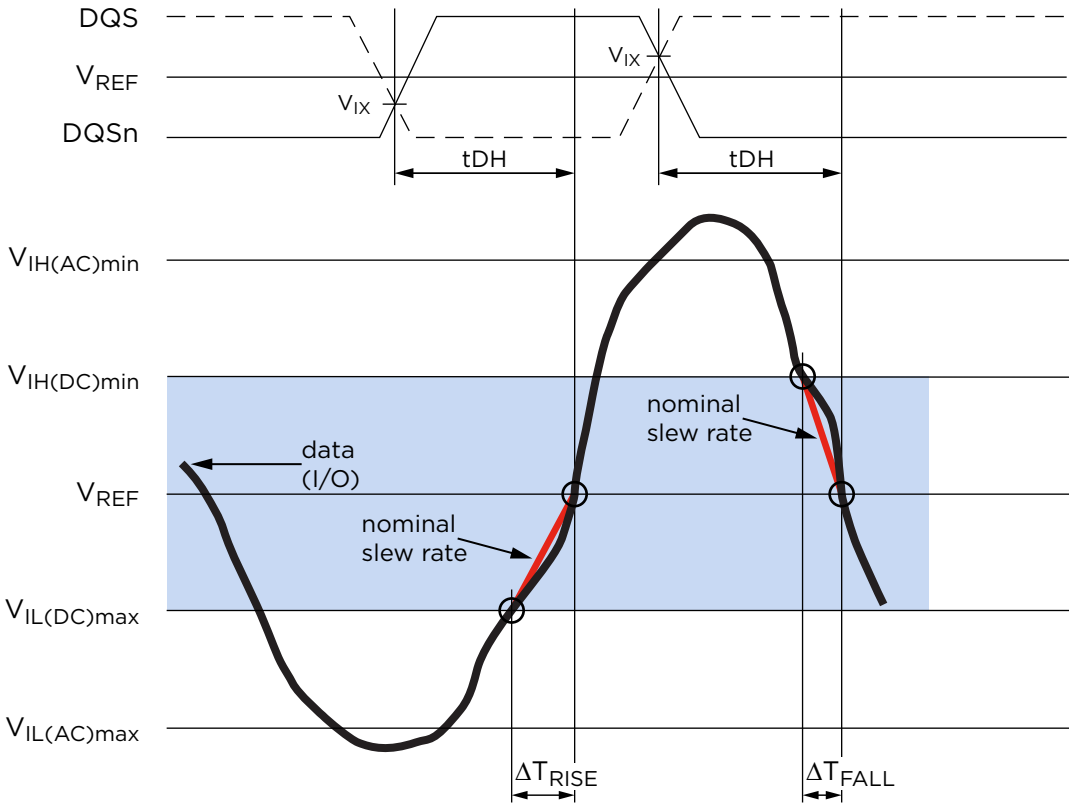
$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } V_{IH(AC)min} - V_{REF}}{\Delta T_{RISE}}$$

The hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of V_{REFQ}. The hold nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of V_{REFQ}.

If the actual signal is always later than the nominal slew rate line within the shaded DC-to-V_{REFQ} region, then the de-rating value uses the nominal slew rate shown in Figure 38, "Nominal Slew Rate for Data Hold Time (tDH)," on page 70.

If the actual signal is earlier than the nominal slew rate line anywhere within the shaded DC-to-V_{REFQ} region, the de-rating value uses the slew rate of a tangent line to the actual signal from the DC level to the V_{REFQ} level, as shown in Figure 39, "Tangent Line for Data Hold Time (tDH)," on page 71.

Figure 38: Nominal Slew Rate for Data Hold Time (tDH)

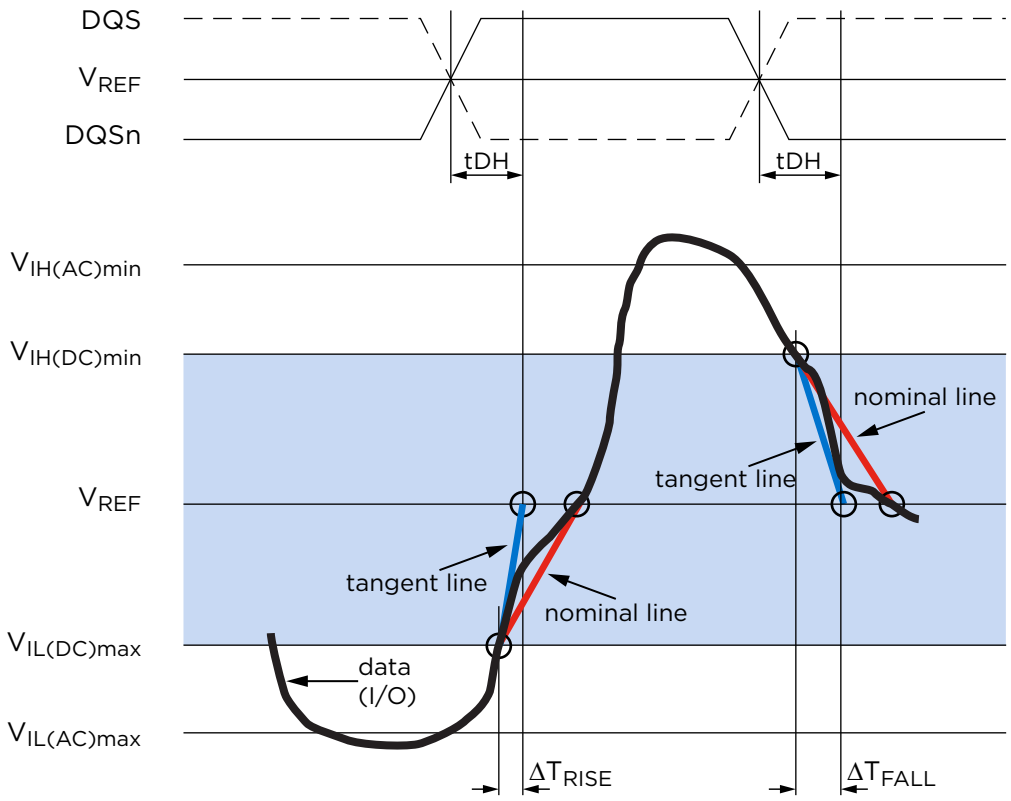


$$\text{Hold slew rate rising signal} = \frac{V_{REF} - V_{IL(DC)max}}{\Delta T_{RISE}} \qquad \text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF}}{\Delta T_{FALL}}$$

If the tangent line is used for de-rating, the setup and hold values must be de-rated from where the tangent line crosses V_{REFQ}, and not the actual signal.

Note: For slew rates not explicitly listed in Table 49, "Input Slew Rate De-rating Table for DQ and Differential DQS: VCCQ = 1.2V—Part I," on page 72, the de-rating values should be obtained by linear interpolation. These values are not typically subject to production test.

Figure 39: Tangent Line for Data Hold Time (tDH)



$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } V_{REF} - V_{IL(DC)max}}{\Delta T_{RISE}}$$

$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } V_{IL(AC)min} - V_{REF}}{\Delta T_{FALL}}$$

8.7.2 Input Slew Rate Requirements

Table 49: Input Slew Rate De-rating Table for DQ and Differential DQS: V_{CCQ} = 1.2V—Part I

V_{IH}/V_{IL} (AC) = 150mV, V_{IH}/V_{IL} (DC) = 100mV, Input slew rate de-rating value unit = ps

DQ Slew Rate (V/ns)	DQS/DQSn Slew Rate (V/ns)											
	12.00		6.00		4.00		3.00		2.00		1.80	
	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold
6.00	0	0	0	0	0	0						
3.00			0	0	0	0	0	0				
2.00					0	0	0	0	0	0		
1.50					0	0	0	0	0	0	6	6
1.00							0	0	0	0	6	6
0.90							3	3	11	11	17	17
0.80									25	25	31	31
0.70											48	48
0.60												
0.50												
0.40												
0.30												

Table 49: Input Slew Rate De-rating Table for DQ and Differential DQS: V_{CCQ} = 1.2V—Part II

V_{IH}/V_{IL} (AC) = 150mV, V_{IH}/V_{IL} (DC) = 100mV, Input slew rate de-rating value unit = ps

DQ Slew Rate (V/ns)	DQS/DQSn Slew Rate (V/ns)											
	1.60		1.40		1.20		1.00		0.80		0.60	
	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold	ΔSet	ΔHold
6.00												
3.00												
2.00												
1.50												
1.00	13	13										
0.90	24	24	33	33								
0.80	38	38	46	46	58	58						
0.70	55	55	64	64	76	76	93	93				
0.60	79	79	88	88	100	100	117	117	142	142		
0.50			121	121	133	133	150	150	175	175	217	217
0.40					183	183	200	200	225	225	267	267
0.30							283	283	308	308	350	350

Note 1. The gray, shaded area indicates input slew rate combinations that are not supported.

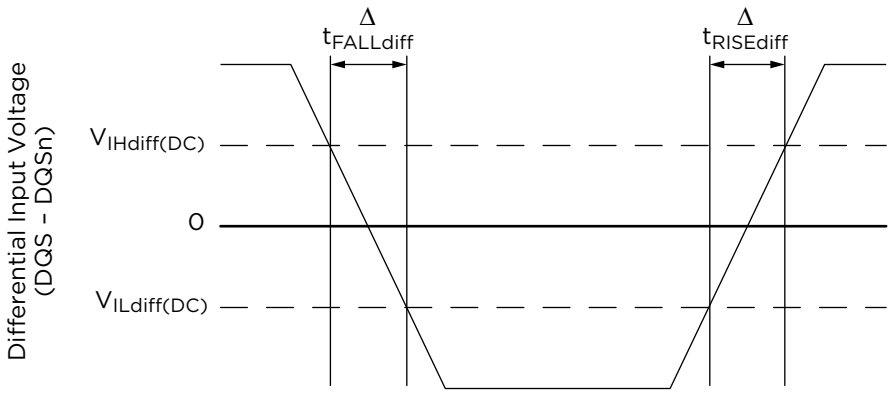
2. DQS slew rates below 0.4 V/ns are not supported for operations above 533 MHz.

Table 50: Differential Input Slew Rate Measurement: Falling Edge/Rising Edge

Description	Measured		Defined by
	From	To	
Differential input slew rate for falling edge (DQS – DQSn)	$V_{IHdiff(DC)}$	$V_{ILdiff(DC)}$	$[V_{IHdiff(DC)} - V_{ILdiff(DC)}]$/ Delta $t_{FALLdiff}$
Differential input slew rate for rising edge (DQS – DQSn)	$V_{ILdiff(DC)}$	$V_{IHdiff(DC)}$	$[V_{IHdiff(DC)} - V_{ILdiff(DC)}]$/ Delta $t_{RISEdiff}$

Note 1. The differential signal must be linear between these thresholds.

Figure 40: Differential Input Slew Rate Definition for tFALL and tRISE



8.7.3 Output Slew Rate Requirements

Table 51: Output Slew Rate Requirements

Parameter	V_{CCQ} = 1.2V		Unit
	Min	Max	
Nominal	1.44	8	V/ns
Underdrive	1.2	7	V/ns

Note 1. Measured with a test load of 5pF connected to V_{SS}.

2. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Table 52: Test Conditions for Output Slew Rate

Parameter	DDR2 Single Ended	DDR2 Differential	DDR3/DDR4 Single Ended	DDR3/DDR4 Differential
$V_{OL(DC)}$	—	—	—	—
$V_{OH(DC)}$	—	—	—	—
$V_{OL(AC)}$	V_{REF} – (V_{CCQ} × 0.15)	—	V_{REF} – (V_{CCQ} × 0.10)	—
$V_{OH(AC)}$	V_{REF} + (V_{CCQ} × 0.15)	—	V_{REF} + (V_{CCQ} × 0.10)	—
$V_{OLdiff(AC)}$	—	–0.3 × V_{CCQ}	—	–0.2 × V_{CCQ}
$V_{OHdiff(AC)}$		0.3 × V_{CCQ}		0.2 × V_{CCQ}
Positive output transition	$V_{OL(AC)}$ to $V_{OH(AC)}$	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$	$V_{OL(AC)}$ to $V_{OH(AC)}$	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Negative output transition	$V_{OH(AC)}$ to $V_{OL(AC)}$	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$	$V_{OH(AC)}$ to $V_{OL(AC)}$	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
tRise	Time from $V_{OL(AC)}$ to $V_{OH(AC)}$	—	Time from $V_{OL(AC)}$ to $V_{OH(AC)}$	—
tFall	Time from $V_{OH(AC)}$ to $V_{OL(AC)}$	—	Time from $V_{OH(AC)}$ to $V_{OL(AC)}$	—
tRISEDiff	—	Time from $V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$	—	Time from $V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
tFALLDiff	—	Time from $V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$	—	Time from $V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / tRISE	[$V_{OHdiff(AC)}$ – $V_{OLdiff(AC)}$] / tRISEdiff	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / tRISE	[$V_{OHdiff(AC)}$ – $V_{OLdiff(AC)}$] / tRISEdiff
Output slew rate falling edge	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / tFALL	[$V_{OHdiff(AC)}$ – $V_{OLdiff(AC)}$] / tFALLdiff	[$V_{OH(AC)}$ – $V_{OL(AC)}$] / tFALL	[$V_{OHdiff(AC)}$ – $V_{OLdiff(AC)}$] / tFALLdiff
Output reference load	5pf	5pf	5pf	5pf

Figure 41: Single-Ended Output Slew Rate

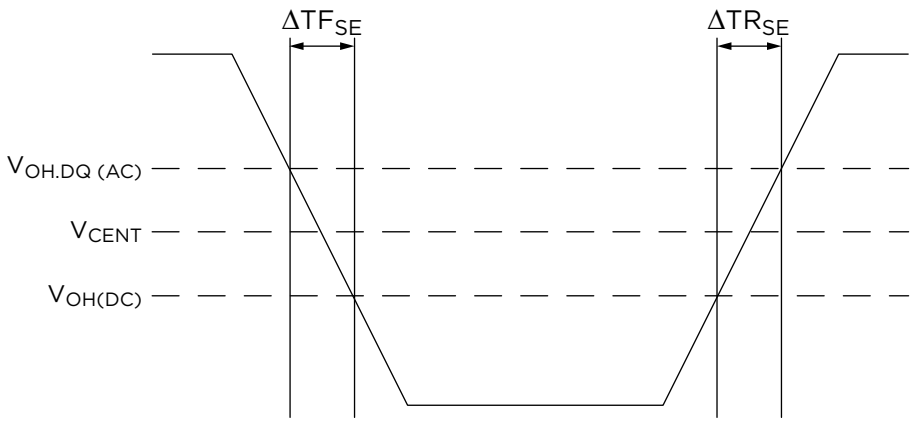


Table 53: Single-Ended Output Slew Rate Measurement Levels

For terminated DQ-related signals

Description	Measures from	Measured to	Defined by
Single-ended output slew rate for falling edge	V_{OH}.DQrel (AC)	V_{OL}.DQrel (AC)	[V_{OH}.DQrel(AC) – V_{OL}.DQrel(AC)] / Δ TFse
Single-ended output slew rate for rising edge	V_{OL}.DQrel (AC)	V_{OH}.DQrel (AC)	[V_{OH}.DQrel(AC) – V_{OL}.DQrel(AC)] / Δ TRse

Table 54: CTT and LTT I/F Parameters for Output Slew Rate Measurement

Parameter	I/F	Symbol	Level	Unit
AC output high for DQ-related signals for slew rate measurements (with output reference load)	CTT	V_{OH}.DQrel (AC)	V_{TT} + 0.1 × V_{CCQ}	V
AC output low for DQ-related signals for slew rate measurements (with output reference load)		V_{OL}.DQrel (AC)	V_{TT} – 0.1 × V_{CCQ}	
AC output high for DQ-related signals for slew rate measurements (with output reference load)	LTT	V_{OH}.DQrel (AC)	0.8 × V_{OH} (nom)	V
AC output low for DQ-related signals for slew rate measurements (with output reference load)		V_{OL}.DQrel (AC)	0.2 × V_{OH} (nom)	

8.8 Termination

This SanDisk device supports termination resistance in specific configurations. On-die termination (ODT) is supported.

In this device, ODT is always on. It can be turned off temporarily and then back on, by command, to enable specific operations such as I/O training. See "6.1.1 Toggle Mode Interface Switching in DDR5" on page 39 **and** Figure 26, "Enable/Disable ODT for I/O Training," on page 42

8.8.1 On-Die Termination

ODT enables a NAND Flash device to turn termination resistance on or off for each I/O, RE, REn, DQS, and DQSn pin. This feature is available for DDR2/DDR3/DDR4/DDR5 operation only.

The ODT feature is designed to improve the signal integrity of the memory channel by enabling the device controller to independently turn termination resistance on or off for a selected target. NAND Flash devices themselves support only self-termination.

For additional details, contact your representative for the BiCS6 Apps Note on ODT.

8.8.2 ODT Turn-On Availability

ODT does not turn on for all data transactions. Table 55 provides the modes for which ODT turn-on is available or unavailable.

Table 55: ODT Turn-On Mode Support

Data Transaction (mode)	Selected-Die ODT
Data in	Supported
Data out	Supported
Read ID	Not supported
Status Read or any single-byte read	Not supported
Set Features	Supported
Get Features	Supported
DQ Read Training (CMD 62h)	Supported
DQ Write Training (CMD 63h/64h from the controller side)	Supported[1]
DCC	Supported

Note 1. See the NAND DQ Training applications note for additional details.

8.8.3 ODT Setting

The ODT setting is configured using the Set Features operation (see Figure 42 **and** "14.1 Toggle Mode-Specific Setting (02h)" on page 121 for additional information).

Figure 42: Set ODT Sequence

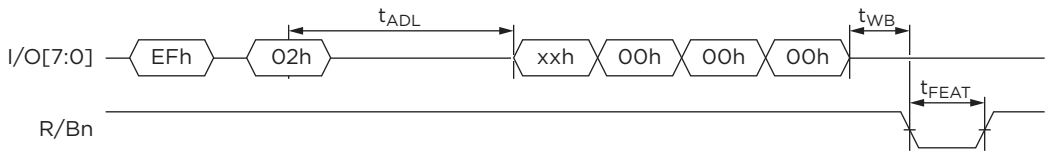
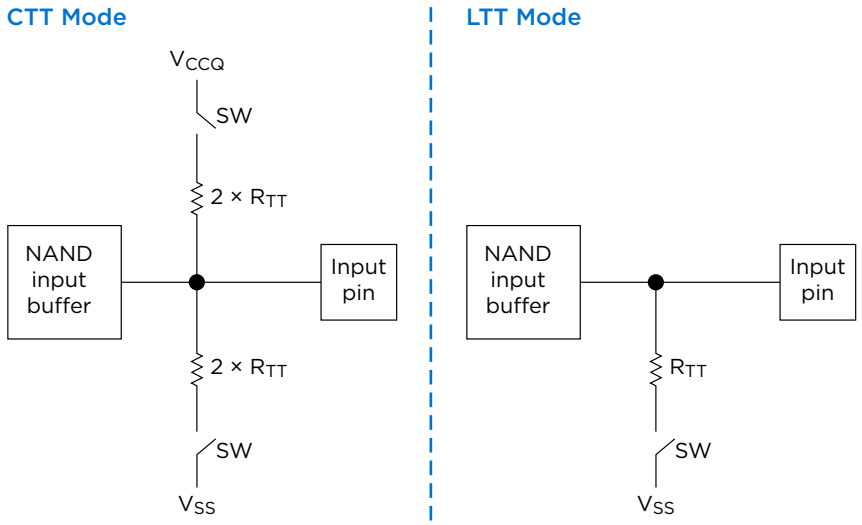


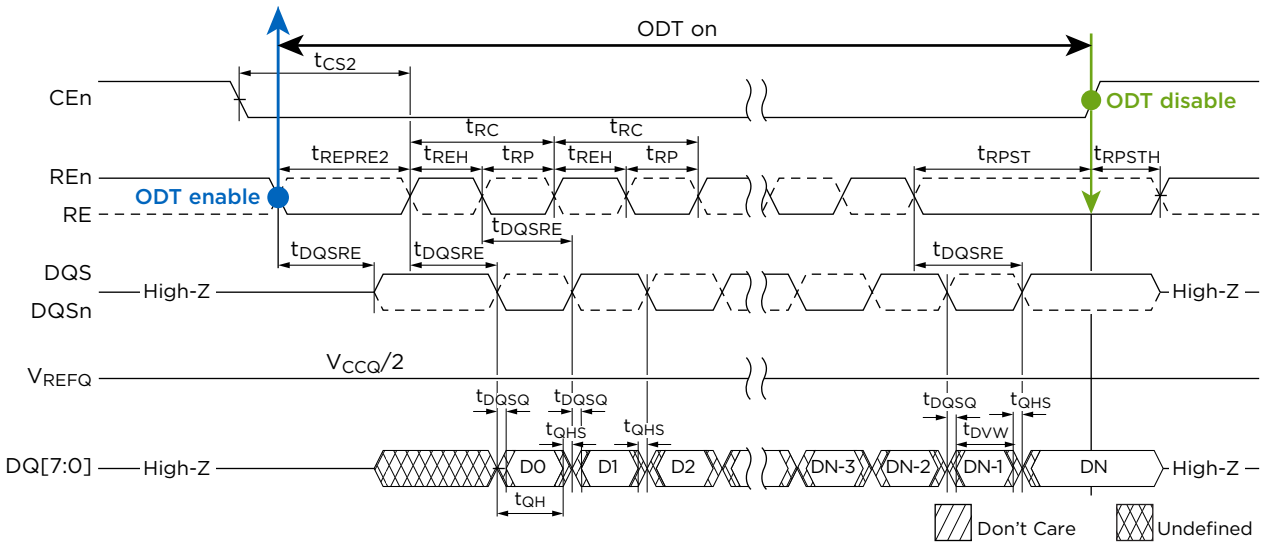
Figure 43: ODT Functional Representation



8.8.4 ODT On/Off During Read

For data out cycles, ODT is enabled as CEn, CLE, ALE, and REn go low. ODT is disabled as CEn goes high.

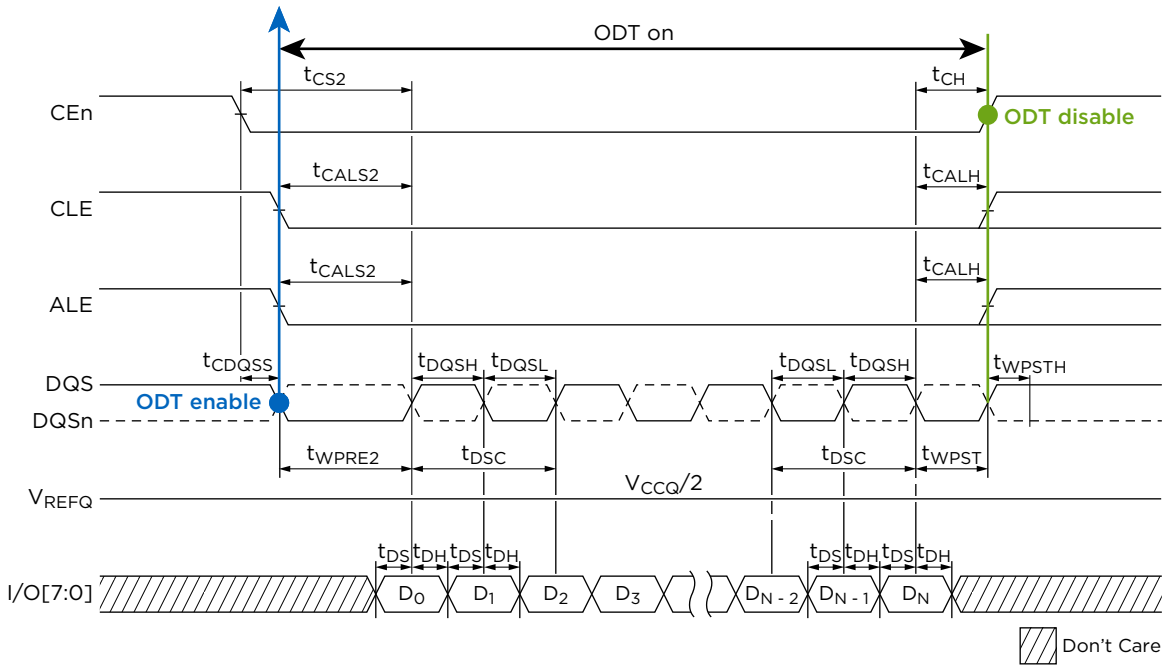
Figure 44: ODT On/Off During Read



8.8.5 ODT On/Off During Program

ODT is enabled within the Write preamble period as ALE, CLE, and DQS go low. ODT is disabled as CEn goes high, or as either CLE or ALE go high while CEn is low.

Figure 45: ODT On/Off During Program



Notice: **This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.**

8.9 Read, Program, and Erase Characteristics

Table 56: Read, Program, and Erase Characteristics

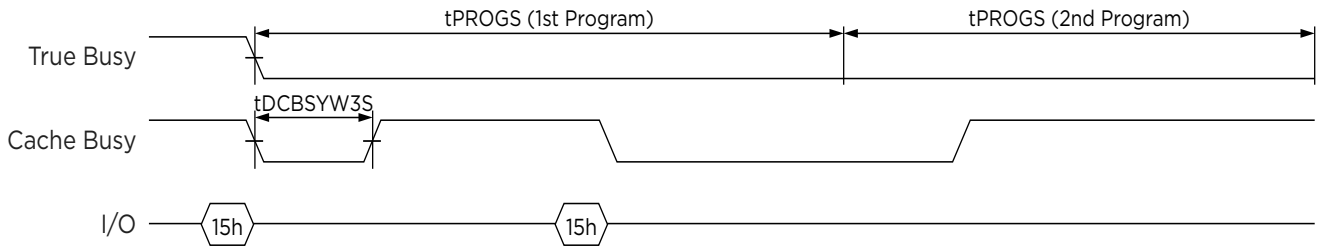
T_{CASE} = 0 to 70°C, V_{CC} = 2.35–3.6V, V_{CCQ} = 1.14–1.30V

Symbol	Parameter	Min	Typ	Max	Unit	Notes
tBERASE	4-bpc block erase time	—	TBD	TBD	ms	
tBERASES	SLC block erase time	—	TBD	TBD	ms	
tDCBSYR	Data cache busy in Read Cache (following 31h, 3Ch, or 3Fh)	—	—	tR (max)	µs	
tDCBSYW1	Data cache busy time in write cache (following 11h) or read cache (following 32h)	—	TBD	TBD	µs	
tDCBSYW2	Data cache busy time in write cache (following 1Ah)	—	—	tPROG (max)	—	1
	Data cache busy time non-cache (following 1Ah)	—	TBD	TBD	µs	
tDCBSYW3	Data cache busy time in write cache for QLC (following the first 15h command)	—	TBD	TBD	µs	
tDCBSYW3S	Data cache busy time in write cache for SLC (following the first 15h command)	—	TBD	TBD	µs	
tPROG1	QLC Programming time (first cycle)	—	TBD	TBD	µs	2
tPROG2	QLC Programming time (second cycle)	—	TBD	TBD	µs	
tPROGS	SLC programming time	—	TBD	TBD	µs	3
tR1	Read access time 1	—	TBD	TBD	µs	4
tR2	Read access time 2	—	TBD	TBD	µs	
tR3	Read access time 3	—	TBD	TBD	µs	
tR4	Read access time 4	—	TBD	TBD	µs	
tRS	SLC Read access time	—	TBD	TBD	µs	

Note 1. tDCBSYW2 depends on the timing between internal programming time and data-in time.

2. tPROG is the typical (typ) total of lower-, middle-, upper-, and top-page internal programming time from a cache or page register to the NAND Flash array.
3. tPROGS is longer after a cache program command (15h) than after a non-cache program command (10h).
4. tR is the average read access time from the NAND array to a cache or page register.

Figure 46: tDCBSYW3S for Back-to-Back SLC Cache Program Operations



Note 1. Cache busy will remain low during the transition from the first Program to the second Program if the second 15h command is issued before the first Program operation is complete.

2. The duration of the second cache busy is determined by the remainder of the tPROGS of the first Program operation plus the tDCBSYW3S after the second 15h command.

9 Read Operations

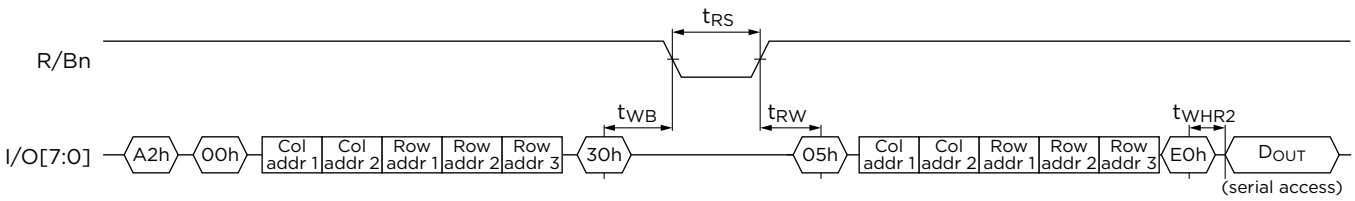
9.1 SLC Page Read

In SLC mode, Page Read requires the A2h command as a prefix to the first 00h or 60h command. All other Read operations, such as Cache Read and Multi-Plane Read, are supported in SLC mode. See Figures 47, 48, 49, and 50.

For timing information, see "17 Toggle Mode Timing Diagrams" on page 136.

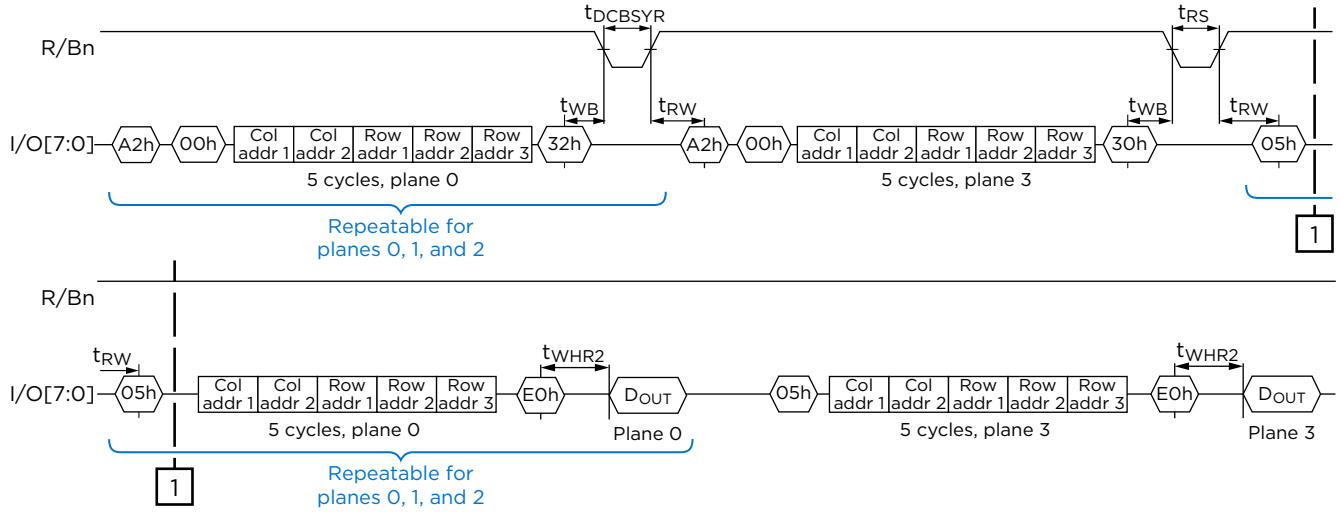
Page Read reads the page of data designated by the row address. The page register makes the page available to be read starting at the specified column address. Reading beyond the end of a page is prohibited and could result in undefined values being returned to the host.

Figure 47: Single-Plane SLC Page Read



Note 1. A2h is the prefix command for SLC mode.

Figure 48: Multi-Plane SLC Page Read



Note 1. A2h is the prefix command for SLC mode.

Figure 49: Single-Plane SLC Random Cache Read

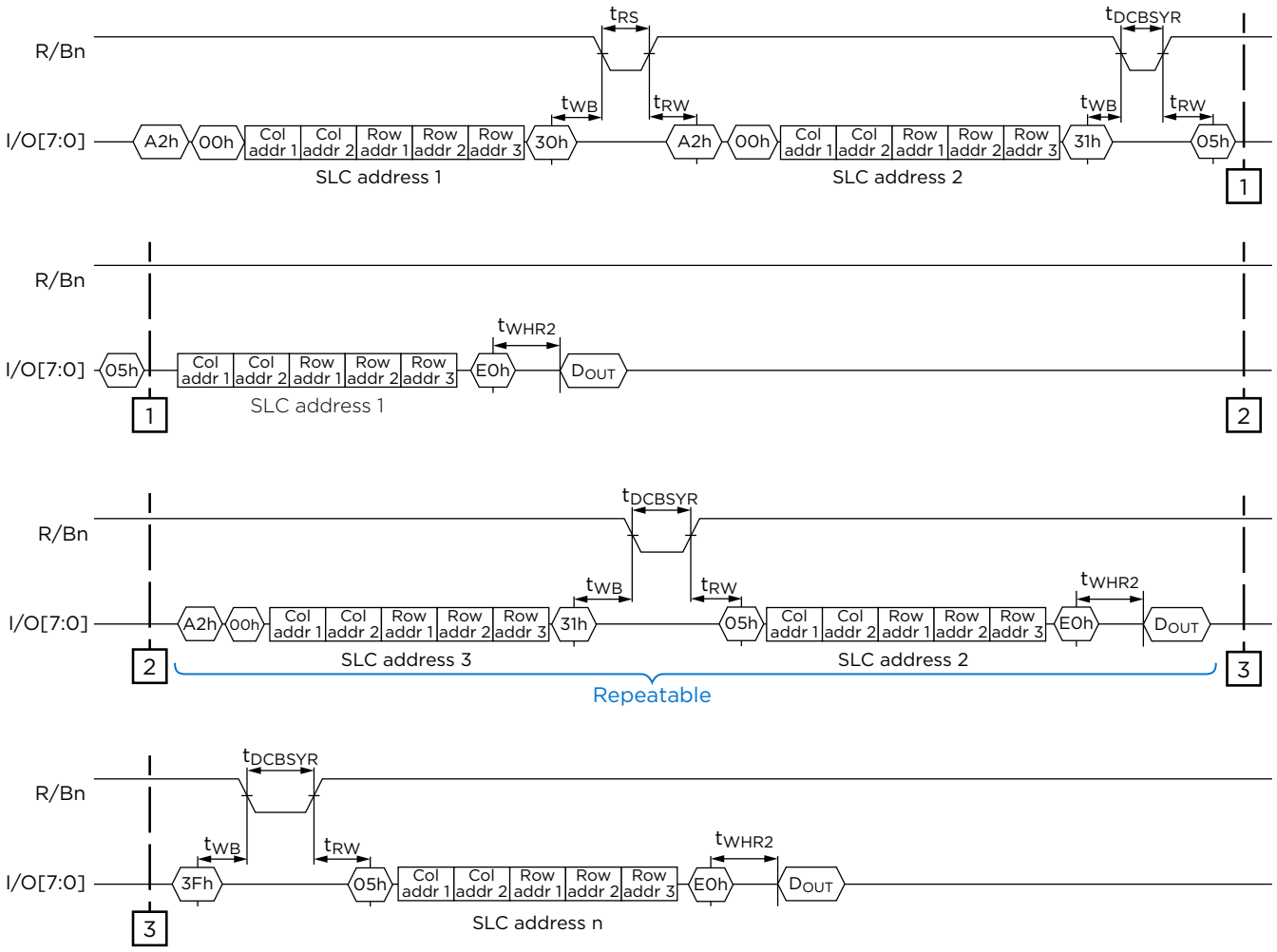
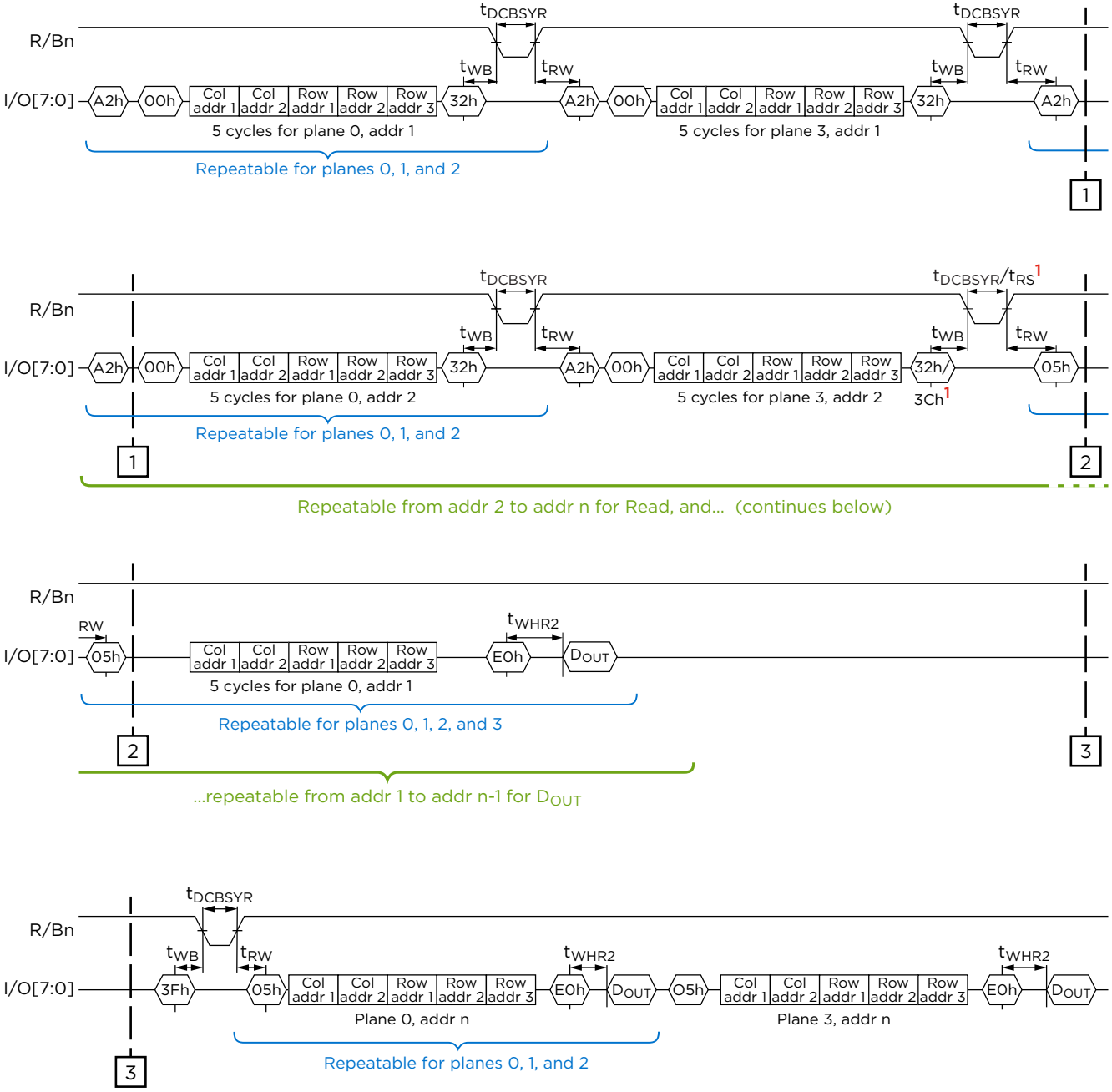


Figure 50: Multi-Plane SLC Random Cache Read



DRAFT Rev. 0.1 7/20/22

9.2 QLC Page Read

9.2.1 QLC Pages and Wordlines

Four pages of data are contained in each WL address for a given string. Selection of the lower, middle, upper, or top page is achieved by using the 01h, 02h, 03h, or 04h prefix, respectively.

Single-Plane QLC Page Read: reads a page of data identified by the row address and the prefix command corresponding to the lower, middle, upper, or top page. The page of data can be read from the page register starting at the specified column address. Clocking out data beyond the end of a page causes indeterminate values to be returned to the host. See Figure 51, “Single-Plane Page-by-Page QLC Read,” on page 85.

Multi-Plane QLC Page Read: is an extension of Page Read. Following a Multi-Plane Read sequence, multiple pages are loaded into page registers. Devices that support Multi-Plane Read also support multiple random data outputs from each page, using the Change Read Column command.

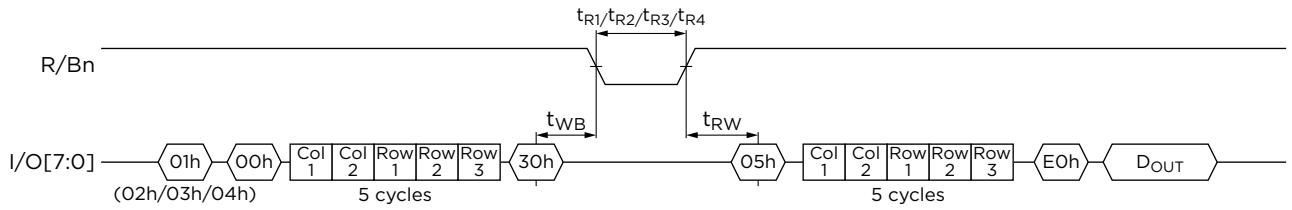
With the Multi-Plane Read command, R/Bn returns to ready immediately after the first 32h command, because this command does not load data from a selected page. The selected page data is transferred to the cache registers via page registers in less than tR following a 30h command.

Multi-plane addresses must be set using the first and second command sets, with the following address input restrictions:

- Multiple page addresses can be set over multiple planes.
- When setting the page address for each plane, the page addresses must be identical, although block addresses could differ.
- The same plane address must only be set one time within an address-setting sequence.
- An even number of planes must be set for this operation.

After the data is loaded into the cache registers, the data on the first page can be read out by issuing the Change Read Column command. The data on other pages can also be read out using the identical command sequence. A multi-plane read operation is shown in Figure 52, “Multi-Plane QLC Read Example (only applies for aIPR = OFF),” on page 85 and a change read column operation is shown in Figure 53, “QLC Page Read with Change Read Column,” on page 86.

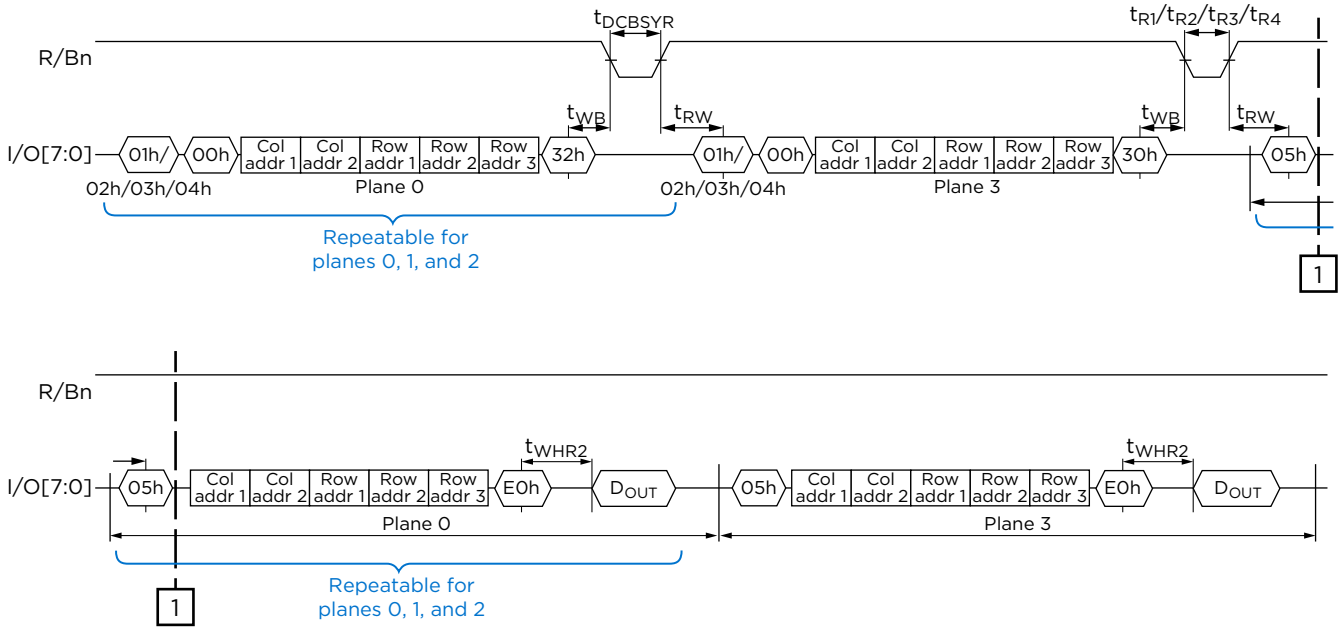
Figure 51: Single-Plane Page-by-Page QLC Read



Note 1. 01h, 02h, 03h, and 04h are prefix commands for the lower, middle, upper, and top pages, respectively. The page data can be read from any of the pages individually, and in any order.

2. Data must be clocked out using the Change Read Column (E0h) command.

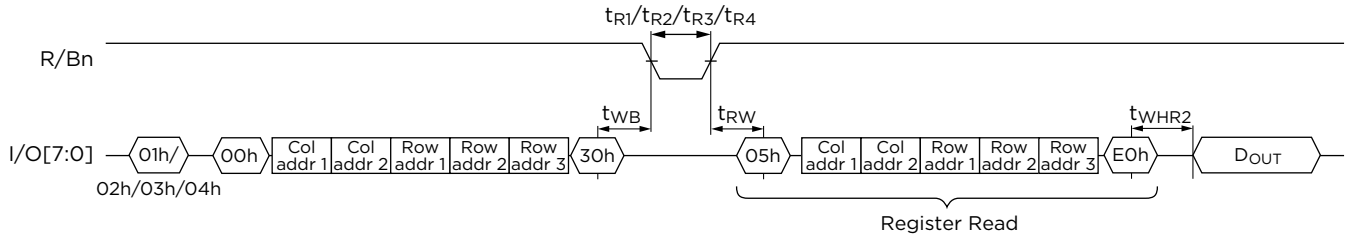
Figure 52: Multi-Plane QLC Read Example (only applies for aIPR = OFF)



9.2.2 QLC Page Read with Change Read Column

Change Read Column changes the column address in the page register from which data is being read. The Change Read Column (05h) command can only be issued when the device is in the cache-ready or the true-ready state. The host must not attempt to clock out data from the device until the second command (E0h) is written and tWHR2 has elapsed.

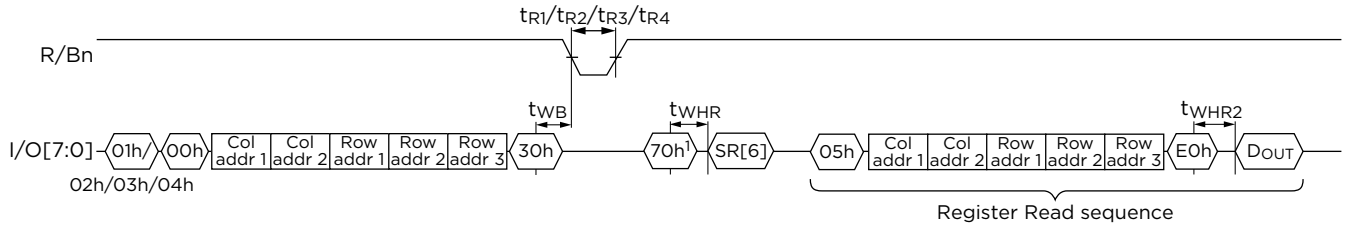
Figure 53: QLC Page Read with Change Read Column



9.2.3 Data Out after QLC Status Read

Monitor Read status to determine if tR (transfer from the Flash array to a page register) is complete. To clock out data following tR, follow the Register Read sequence as shown in Figure 54.

Figure 54: Data Out after QLC Status Read



Note 1. A register read must be performed to clock data out.

2. The following commands can be issued during busy:
   - Status commands 70h, 71h, F1h-F8h
   - Reset commands FAh, FFh

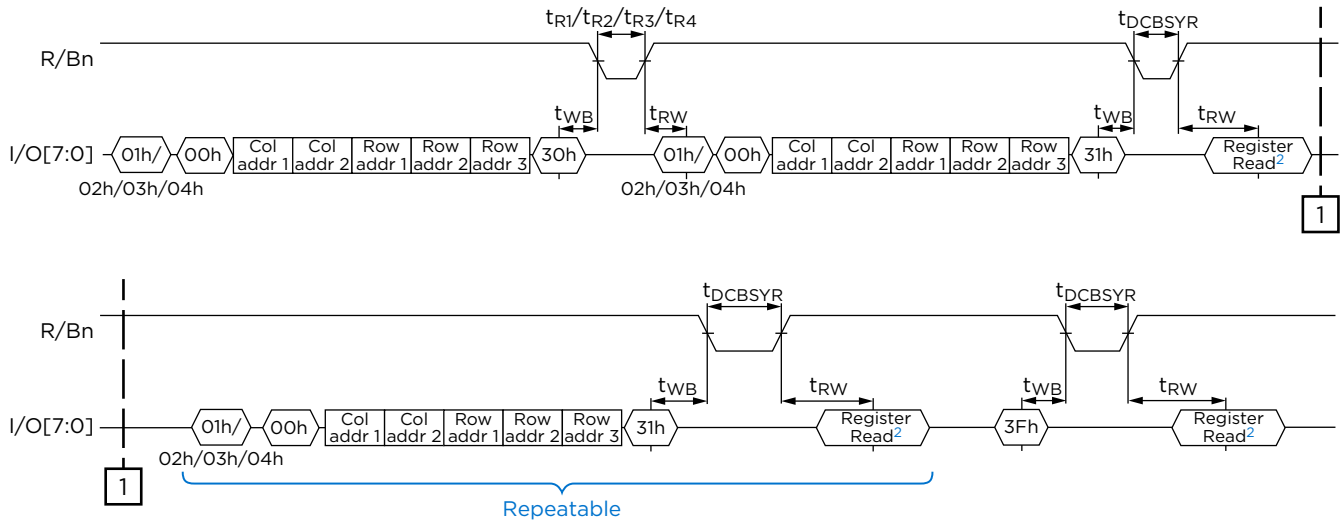
9.2.4 QLC Random Cache Read

Single-Plane QLC Random Cache Read: Prior to issuing the initial Random Cache Read command in a cache read sequence, a Page Read command must be issued. Prior to issuing the 3Fh for the last read, a Random Cache Read command must be issued. Page and block addresses can be accessed randomly. See Figure 55.

Multi-Plane QLC Random Cache Read: To load data from particular pages, Multi-Plane Random Cache Read requires multiple address settings ahead of command 31h. Because the selected pages are loaded to the page register while the host reads data from the cache register where previous data is loaded, R/Bn goes high immediately, unless the previous data is still being loaded.

Multi-plane addresses must be set with the first and second command sets, and must comply with the address input restrictions for multi-plane operation (see "4.2 Command Sets" on page 17). The activated planes for the first Multi-Plane Random Cache Read must also be used in the next address sequence, until the Multi-Plane Random Cache operation is completed by issuing command 3Fh. See Figure 56, "Multi-Plane QLC Random Cache Read," on page 88.

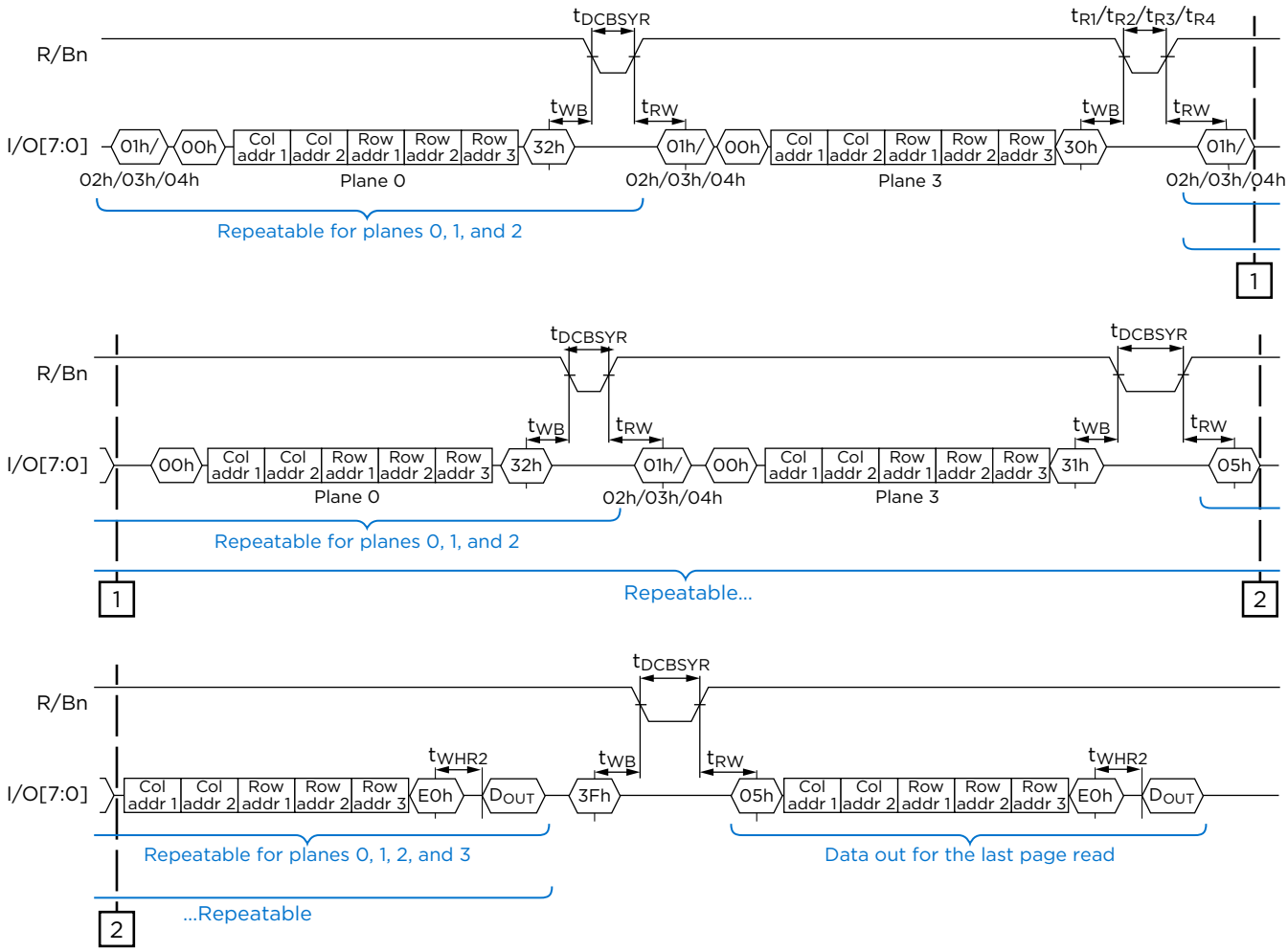
Figure 55: Single-Plane QLC Random Cache Read



Note 1. A register read must be performed to clock data out.

2. See Figure 53, "QLC Page Read with Change Read Column," on page 86 for Register Read sequence definition.

Figure 56: Multi-Plane QLC Random Cache Read



Note 1. Block addresses can be different; page addresses must be the same.

10 Program Operations

10.1 SLC Program

SLC Page Program: In SLC mode, Page Program requires the A2h command as a prefix to the 80h command. All other Program operations, such as Cache Program and Multi-Plane Program, are supported in SLC mode using the A2h command. See Figures 57, 58, 59, and 60.

Table 57: Program Cycles

Description	tBUSY	Command
Program cycle	tPROG	10h/15h[1]
SLC Program cycle	tPROGS	10h/15h[1]
Multi-Plane Program cycle	tDCBSYW1	11h
Multi-Page Program cycle	tDCBSYW2	1Ah
Cache Program cycle for QLC	tDCBSYW3	15h[1]
Cache Program cycle for SLC	tDCBSYW3S	15h[1]

Note 1. If the 10h command is used for the final page, check status on SR[6]. If the 15h command is used for the final page, check SR[5] status for completion.

For timing information, refer to "Toggle Mode Timing Diagrams" starting on page 136.

Addressing order must be sequential within a block. Page register contents are programmed to the Flash array specified by the row address. SR[2] is valid for this command after SR[6] transitions from zero to one, and remains valid until the next transition of SR[6] to zero, assuming that the 10h command was issued for the final page. When the 10h command is used, status is valid on SR[2] when SR[5] is high. When the 15h command is used, status is valid on SR[3] for the previously issued programming when SR[6] is high (see Figure 57). Status remains valid until the next transition of SR[5] or SR[6] to zero. If the 15h command is used for the final page, check SR[5] for device ready/busy status. Writing beyond the end of the page register is prohibited.

Figure 57: Single-Plane SLC Page Program without Cache

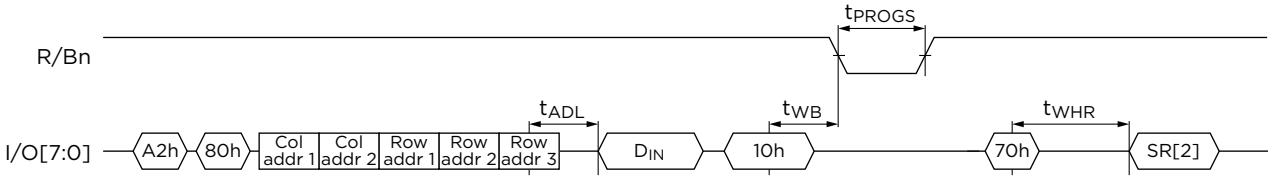
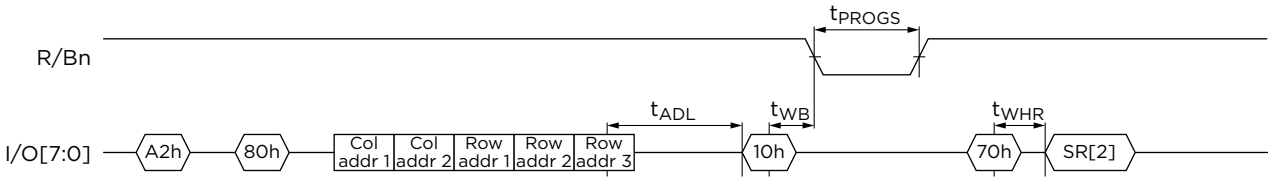


Figure 58: Single-Plane SLC Program without Data Input



10.1.1 SLC Program Order

In SanDisk 3D NAND Flash devices, it is necessary to use the program order provided in Table 58 for programming the page wordlines (WLs) within a block. Random page/WL-program sequences are prohibited.

It is necessary to complete programming of the entire WL (all 5 strings) before continuing with the next WL. On a given WL, data on String 0 should be programmed first, followed by String 1, String 2, String 3, and String 4, as shown in Table 58.

Partial-page programming is NOT supported in SLC operation.

Table 58: SLC Programming Order

WL #	Page Order				
	String 0	String 1	String 2	String3	String 4
WL0	0	1	2	3	4
WL1	5	6	7	8	9
WL2	10	11	12	13	14
:	:	:	:	:	:
WL80	400	401	402	403	404
WL81	405	406	407	408	409
:	:	:	:	:	:
WL159	795	796	797	798	799
WL160	800	801	802	803	804
WL161	805	806	807	808	809

Figure 59: Single-Plane SLC Cache Program

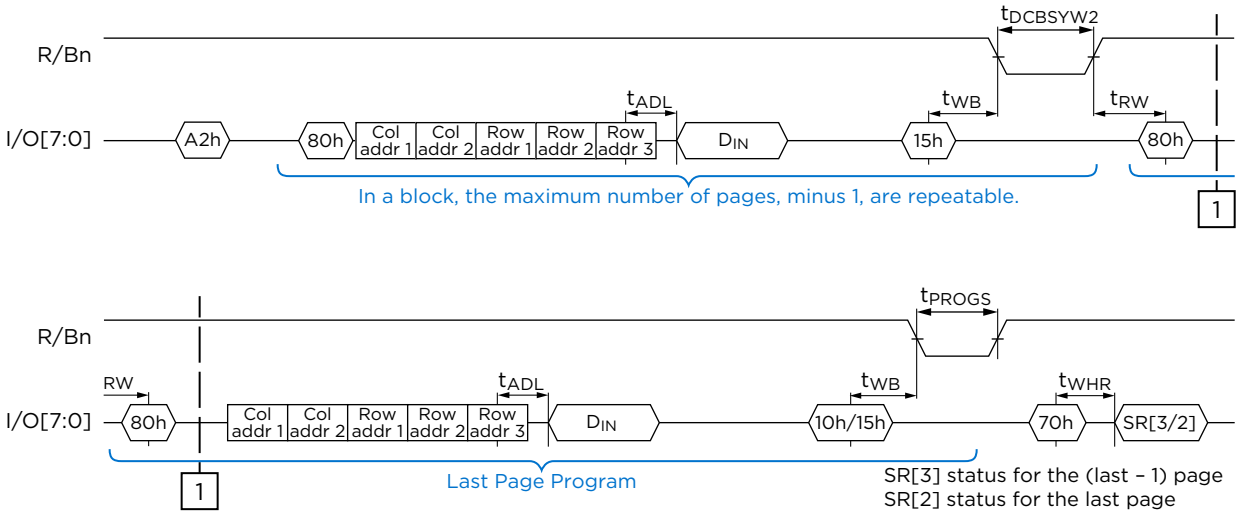
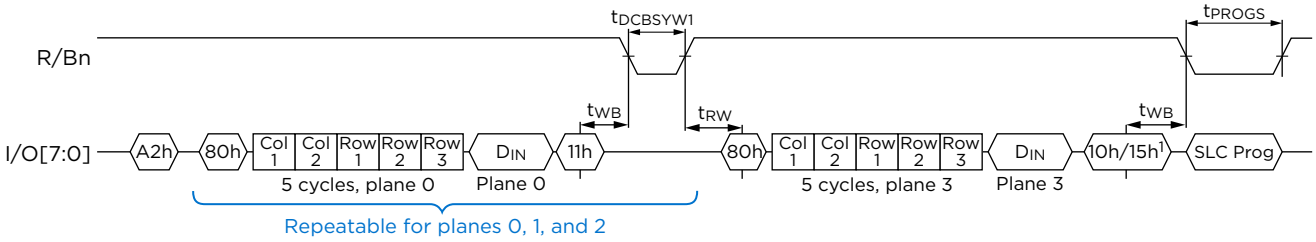


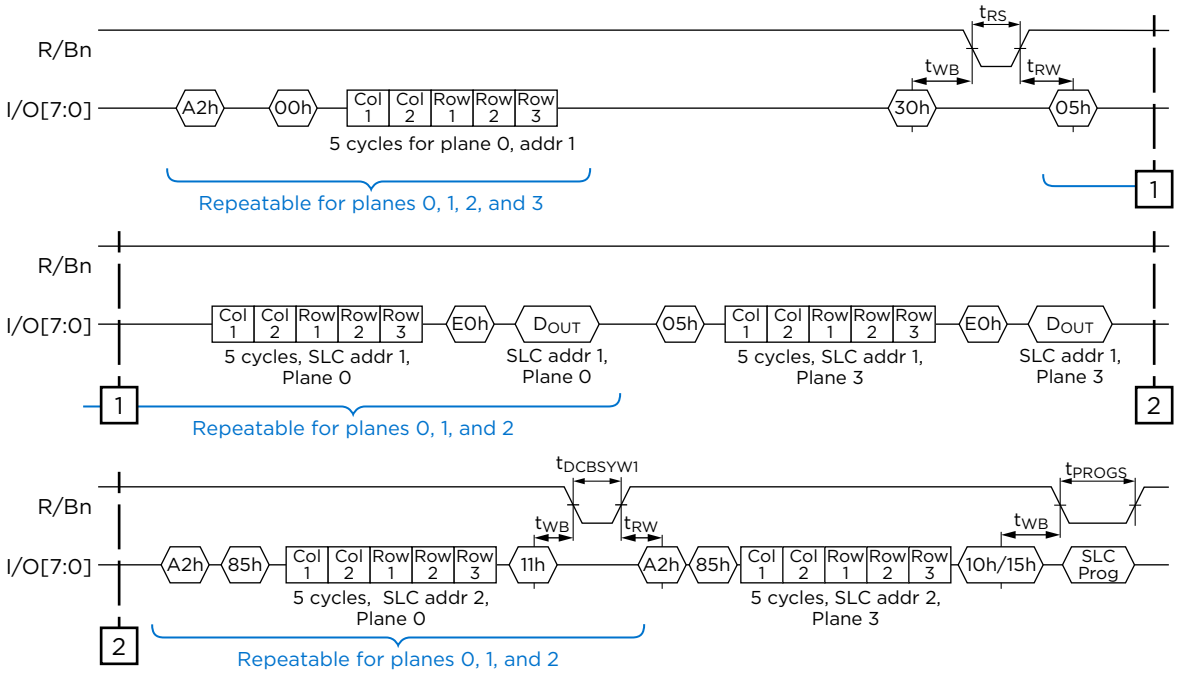
Figure 60: Multi-Plane SLC Program



Note 1. Use the 10h Program command when the write cache is not needed. Use the 15h Program command when using write cache.

2. Block addresses can be different; page addresses must be the same,

Figure 61: Multi-Plane Copy: SLC-to-SLC



Note 1. SLC data out is optional.

DRAFT Rev. 0.1 7/20/22

10.2 QLC Program

This NAND Flash device is programmed on a wordline (WL) basis for QLC operation. The addressing order must be sequential within a block.

Page register content is programmed into the NAND Flash array as specified by the row address. When using the 10h command, check SR[6] status for completion. After SR[6] transitions from 0 to 1, SR[0]—or SR[2] for SLC—is valid for Program commands until the next transition of SR[6] to 0.

When using the 15h command, check both R/Bn and SR[5] status for completion—both must be high for the final page. Writing beyond the end of the page register will yield undefined results.

Multi-Plane Program: Extends the effective programmable page size by using multiple pages. When the host begins to load data for another plane, command 11h is used for the first command. Following the 11h command, R/Bn goes high (ready) immediately, because 11h is not an actual programming command.

At the last page, command 81h is issued before loading data; after the data is loaded, command 10h is issued as the second command. Following command 10h, the device begins simultaneously programming all loaded data from each page to the NAND Flash array. Multi-plane addresses must be set with the first and second command sets, and must comply with the address input restrictions for multi-plane operation (see “4.2 Command Sets” on page 17).

10.2.1 QLC Program Order

In SanDisk 3D NAND Flash devices, it is necessary to use the QLC program order provided in Table 59 for programming the pages within a block. Random page-program sequences are prohibited. Data for all four pages (lower, middle, upper, and top) must be loaded before Program operation can begin. All four pages in a given string will be programmed at the same time.

The QLC Program data for all four pages must be loaded into the respective registers before the actual Program command (10h or 15h) is issued. Partial-page programming is not supported in QLC operation.

Table 59: QLC Programming Order

Wordline	Program Cycle	Page Order				
		String 0	String 1	String 2	String 3	String 4
WL0	First	0	1	2	3	4
	Second	6	8	10	12	14
WL1	First	5	7	9	11	13
	Second	16	18	20	22	24
WL2	First	15	17	19	21	23
	Second	26	28	30	32	34
WL3	First	25	27	29	31	33
	Second	36	38	40	42	44
:	:	:	:	:	:	:
WL159	First	1575	1577	1579	1581	1583
	Second	1586	1588	1590	1592	1594
WL160	First	1585	1587	1589	1591	1593
	Second	1596	1598	1600	1602	1604
WL161	First	1595	1597	1599	1601	1603
	Second	1605	1606	1607	1608	1609

Note 1. All three pages in a given string for a WL are programmed at the same time.

10.2.2 QLC Cache Program

Cache Program enables the host to load the next data chunk to another page of the page register while a page of data is being written to the NAND Flash array.

When command 15h is issued, data in the cache register is transferred to a page register. R/Bn goes high (ready) when the cache register is ready to receive data.

When the 10h command is issued for the final page, R/Bn goes high after the operation and the final page are complete. When using the 15h command, check both R/Bn and SR[5] status for completion—both must be high for the final page.

After SR[5] transitions from 0 to 1, SR[0] is valid for Cache Program until the next transition. After SR[6] transitions from 0 to 1, SR[1] is valid for Cache Program.

SR[1] is invalid after the first Cache Program completes because there was no previous Cache Program operation. Cache Program operation functions only within a block.

The final tPROG of the caching operation could be longer than typical because this time also includes completion of the programming operation for the previous page. Loading data beyond the end of the page register will yield undefined results.

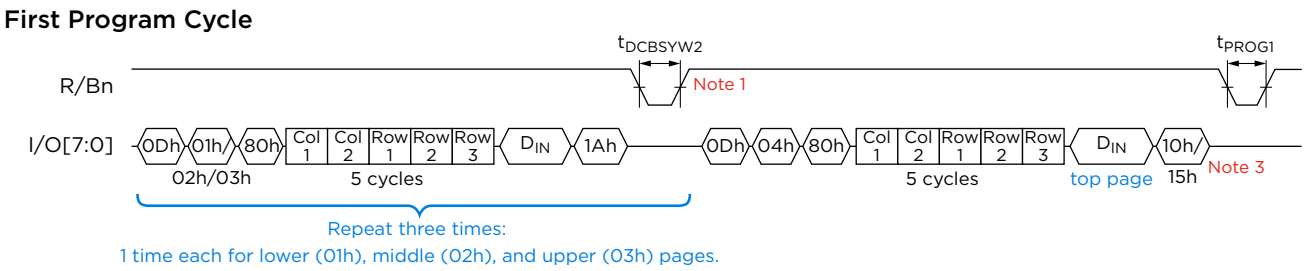
Multi-Plane QLC Cache Program: is an extension of Cache Program. After loading pages for Multi-Plane Cache Program, command 15h is issued. When data transfer from the cache register to the page register is complete, R/Bn goes high. At this point, internal program operation is in progress, while other pages are being loaded by the host.

After the last page of the entire Multi-Plane Cache Program loads, command 10h must be issued to finalize the operation; R/Bn remains busy for the duration of tPROG. When using the 10h command, check the R/Bn status for completion. When using the 15h command, check both R/Bn and SR[5] status for completion—both must be high for the final page.

Multi-Plane Cache Program works only within a block; it cannot be continued beyond the block boundary. Multi-plane addresses must be set with the first and second command sets, and must comply with the address input restrictions for multi-plane operation (see Table 9, “Extended Command Set,” on page 19).

The activated planes for the first Multi-Plane Cache Program must also be used in the next address sequence, until the Multi-Plane Cache Program operation is completed by issuing command 10h. If the 15h command is used for the final page, check SR[5] status for completion.

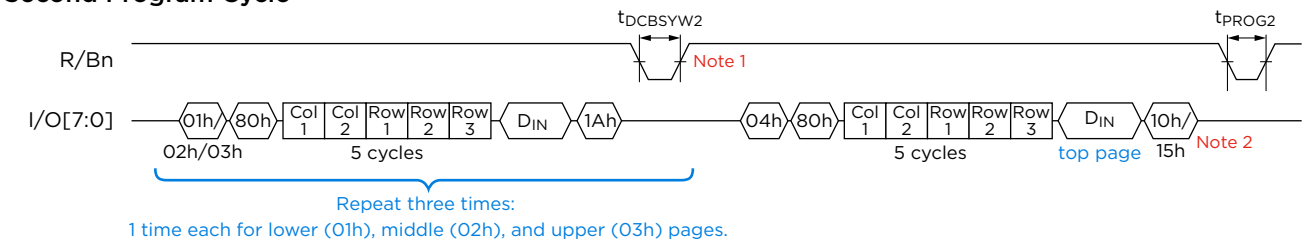
Figure 62: Single-Plane QLC Program, With and Without Cache: First Cycle



Note 1. Prefix 0Dh is required to indicate the first Program cycle. Page prefixes 01h/02h/03h/04h are required for lower-, middle- upper-, or top-page Program operations.

2. QLC Cache Program status on I/O0 and I/O1 are invalid following the 1Ah command.
3. Use 10h for the Program command when ***not*** using cache; use 15h when using cache.

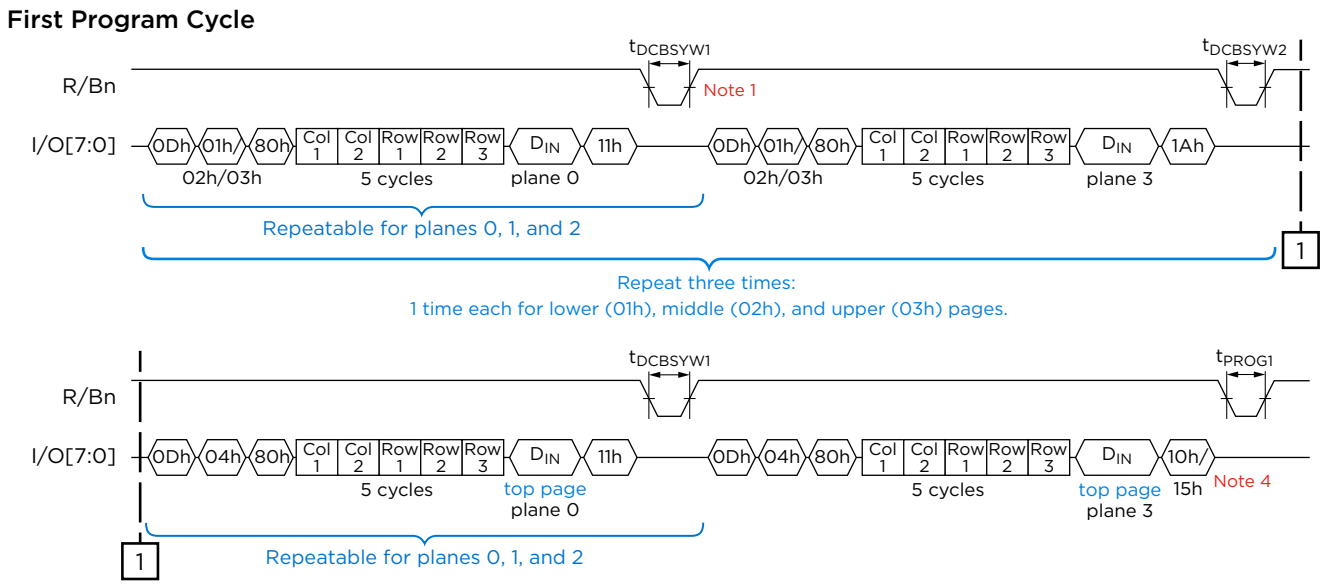
Figure 63: Single-Plane QLC Program, With and Without Cache: Second Cycle



Note 1. In single-plane programming, the 1Ah command is followed by tDCBSYW2.

2. Page prefixes 01h/02h/03h/04h are required for lower-, middle, upper-, and top-page Program operations.
3. Use 10h for the Program command when ***not*** using cache; use 15h when using cache.

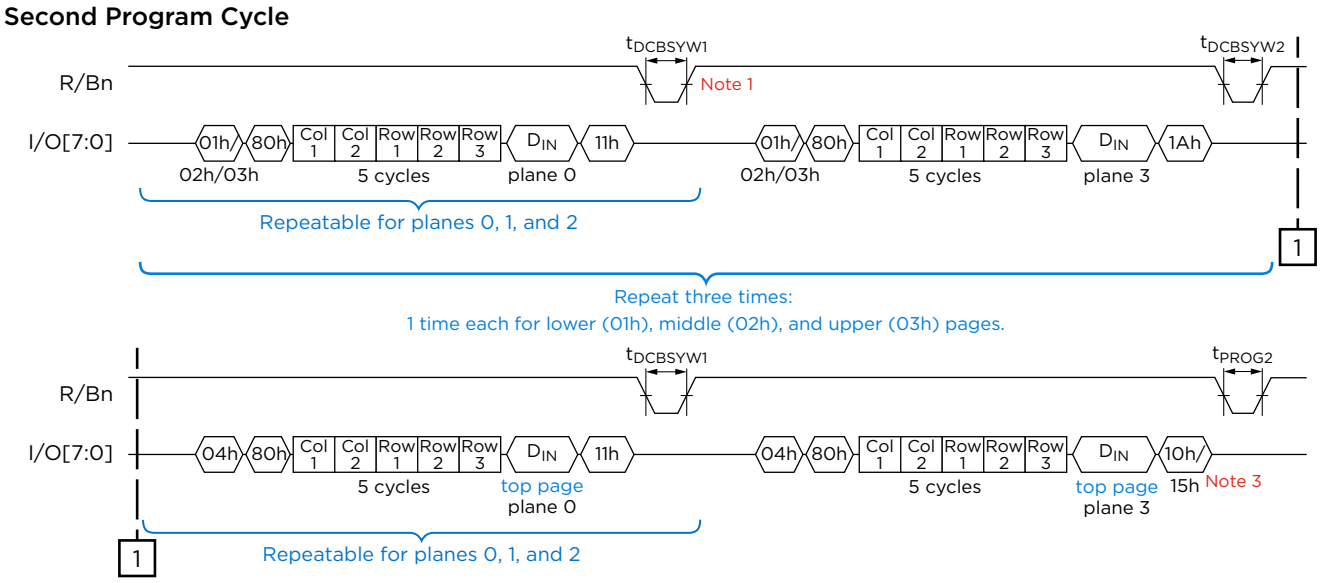
Figure 64: Multi-Plane QLC Program, With and Without Cache: First Cycle



Note 1. In multi-plane programming, the 11h command is followed by tDCBSYW1.

2. Prefix 0Dh is required to indicate the first Program Cycle. Page prefixes 01h/02h/03h/04h are required for lower-, middle-, upper-, and top-page Program operations.
3. Block addresses can be different; page addresses must be the same across the four planes.
4. Use 10h for the Program command when ***not*** using cache; use 15h when using cache.

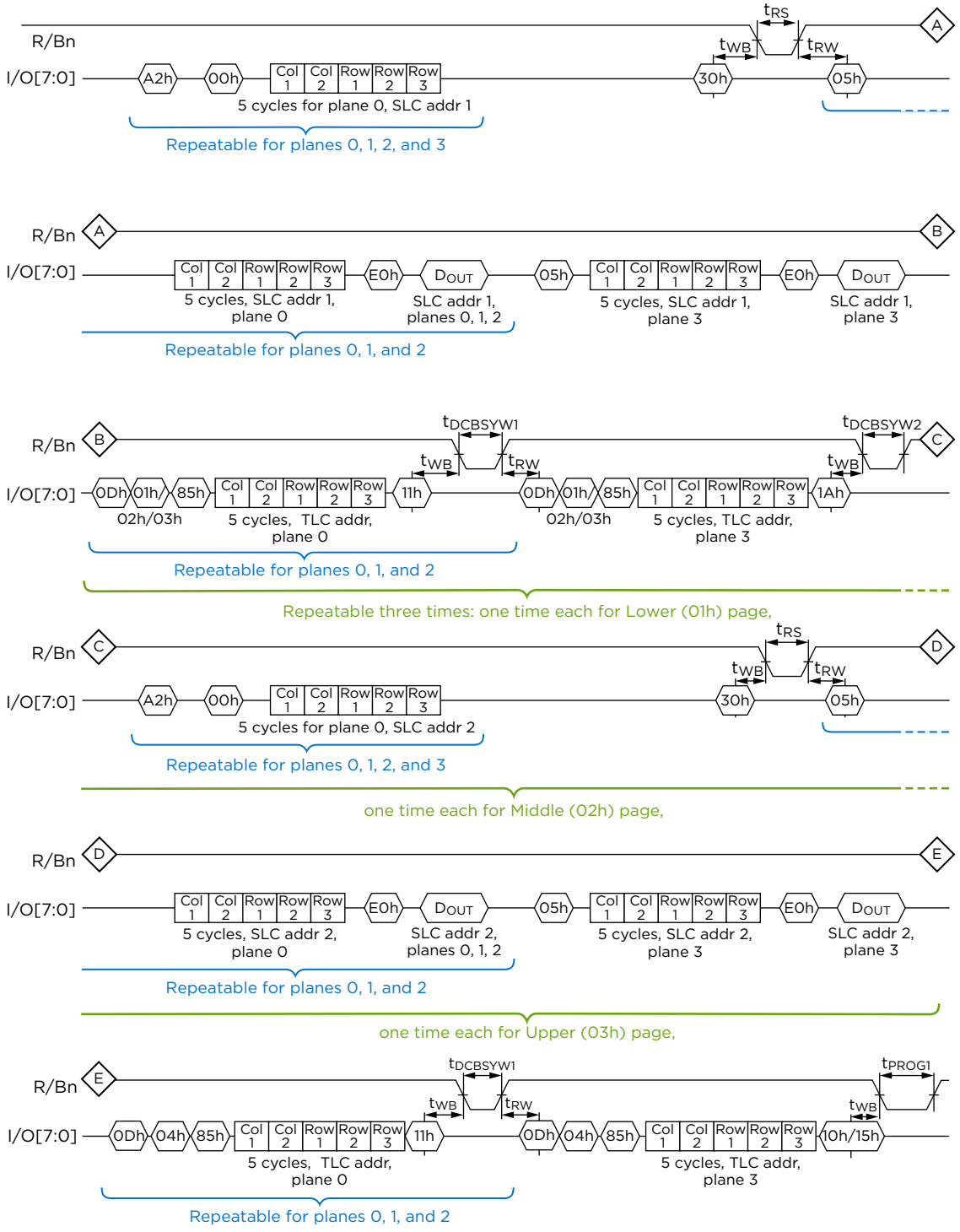
Figure 65: Multi-Plane QLC Program, With and Without Cache: Second Cycle



Note 1. In multi-plane programming, the 11h command is followed by tDCBSYW1.

2. Page prefixes 01h/02h/03h/04h are required for lower-, middle-, upper-, and top-page Program operations.
3. Block addresses can be different; page addresses must be the same across the four planes.
4. Use 10h for the Program command when ***not*** using cache; use 15h when using cache.

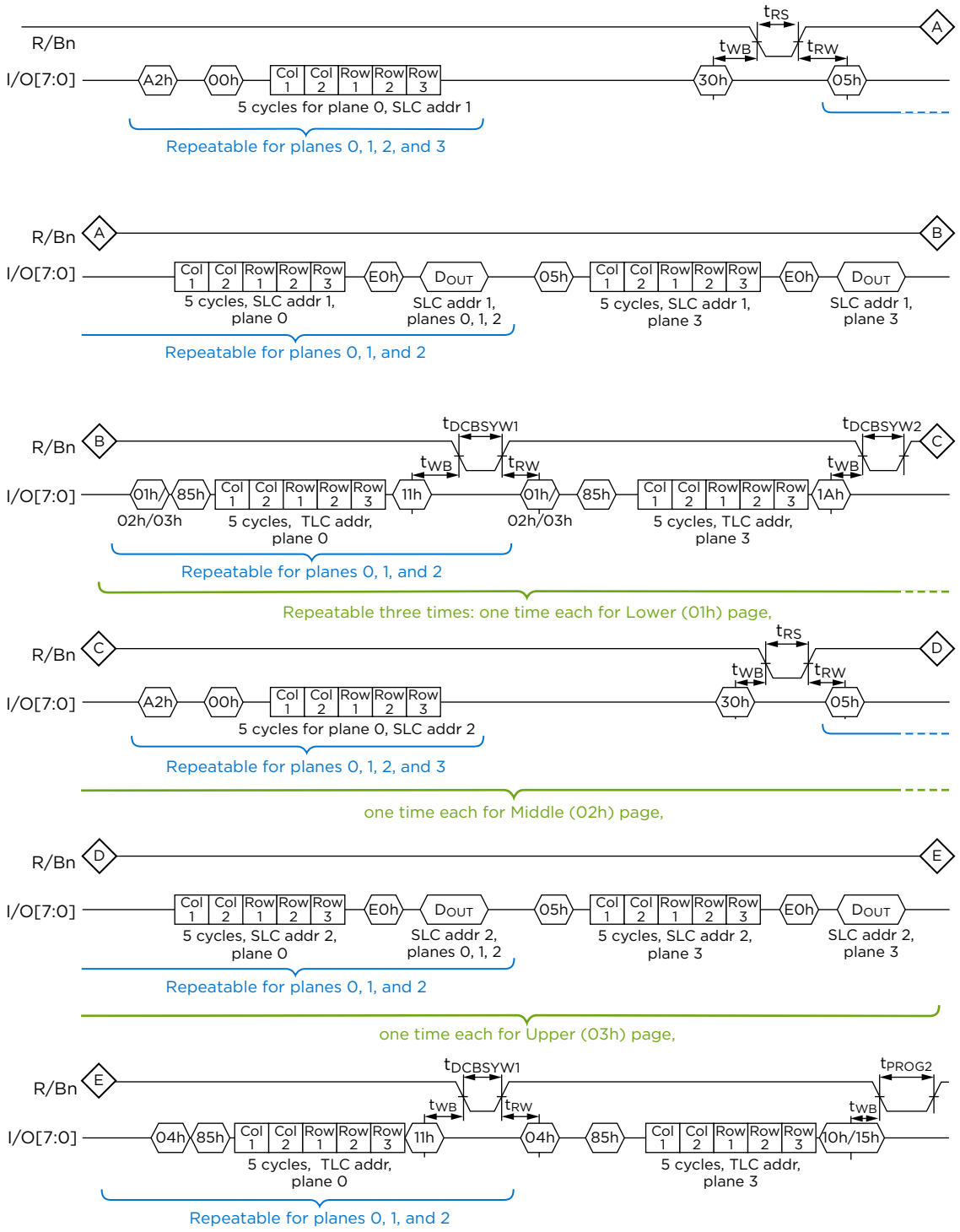
Figure 66: Multi-Plane Copy: SLC to QLC: First Cycle



Note 1. Use of the sequences between 1 & 2, and between 4 & 5 is optional.

2. Use 10h for the Program command when ***not*** using cache; use 15h when using cache..

Figure 67: Multi-Plane Copy: SLC to QLC: Second Cycle



Note 1. Use of the sequences between 1 & 2, and between 4 & 5 is optional.

2. Use 10h for the Program command when ***not*** using cache; use 15h when using cache.

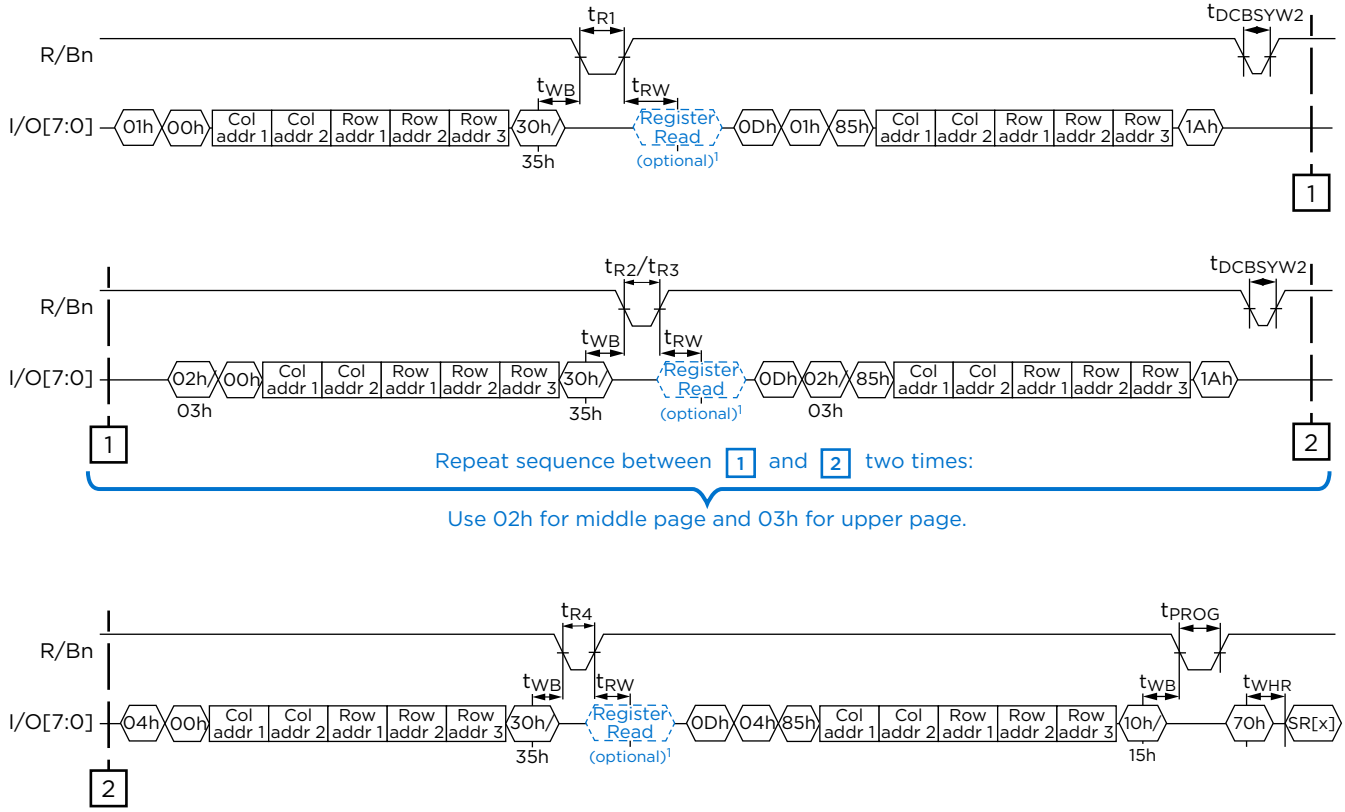
10.2.3 Copy-Back Program

Copy-Back Program with Read for Copy-Back is configured to efficiently reprogram data stored in a page—without data reloading—when no error is found within the page. The copy-back operation helps improve system performance by eliminating time-consuming reloading cycles. This advantage is particularly obvious when updating part of a block, and the rest of the block must be copied to the newly assigned free block.

Copy-Back operation consists of the Read for Copy-Back and Copy-Back Program commands. The host reads a page of data from a source page using Read for Copy-Back, then copies the read data back to a destination page on the same device using the Copy-Back Program command. Copy-Back Program operations work only within the same plane.

Multi-Plane Copy-Back Program: is an extension of Copy-Back Program, and is executed by two command sets: Multi-Read for Copy-Back and Multi-Copy-Back Program. Multi-plane addresses must be set with the first and second command sets, and must comply with the address input restrictions for multi-plane operation (see "4.2 Command Sets" on page 17). Data that has been read must be copied back to a page in the same plane. Be sure WPn is held high during Multi-Copy-Back operation.

Figure 68: Single-Plane Copy-Back Program, First Cycle



Note 1. Data must be clocked out using the Change Read Column command.

2. See Figure 53, "QLC Page Read with Change Read Column," on page 86 for Register Read sequence definition.
3. Use 10h for the Program command when not using cache; use 15h when using cache.

DRAFT Rev. 0.1 7/20/22

Figure 69: Single-Plane Copy-Back Program, Second Cycle

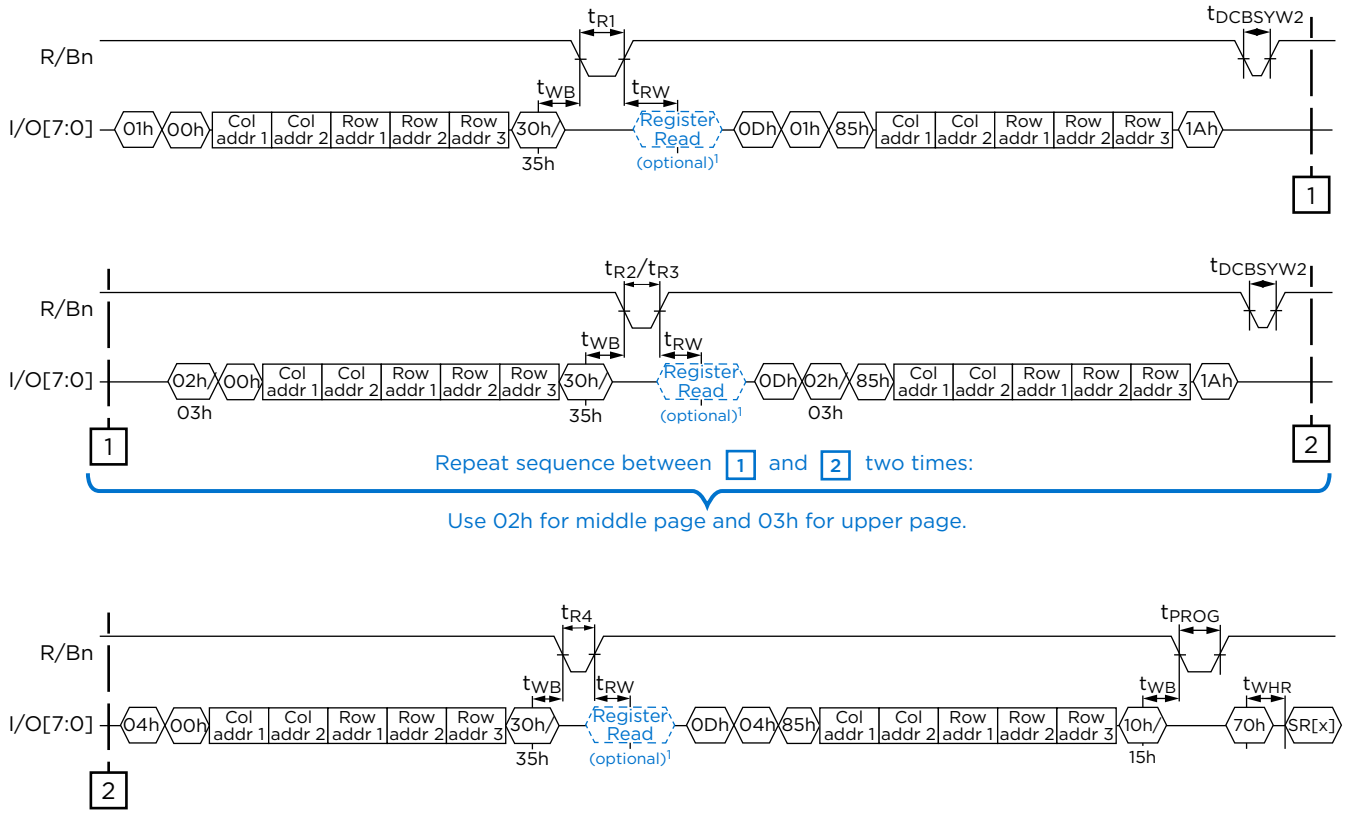


Figure 70: Multi-Plane Copy-Back Program Example: First Cycle

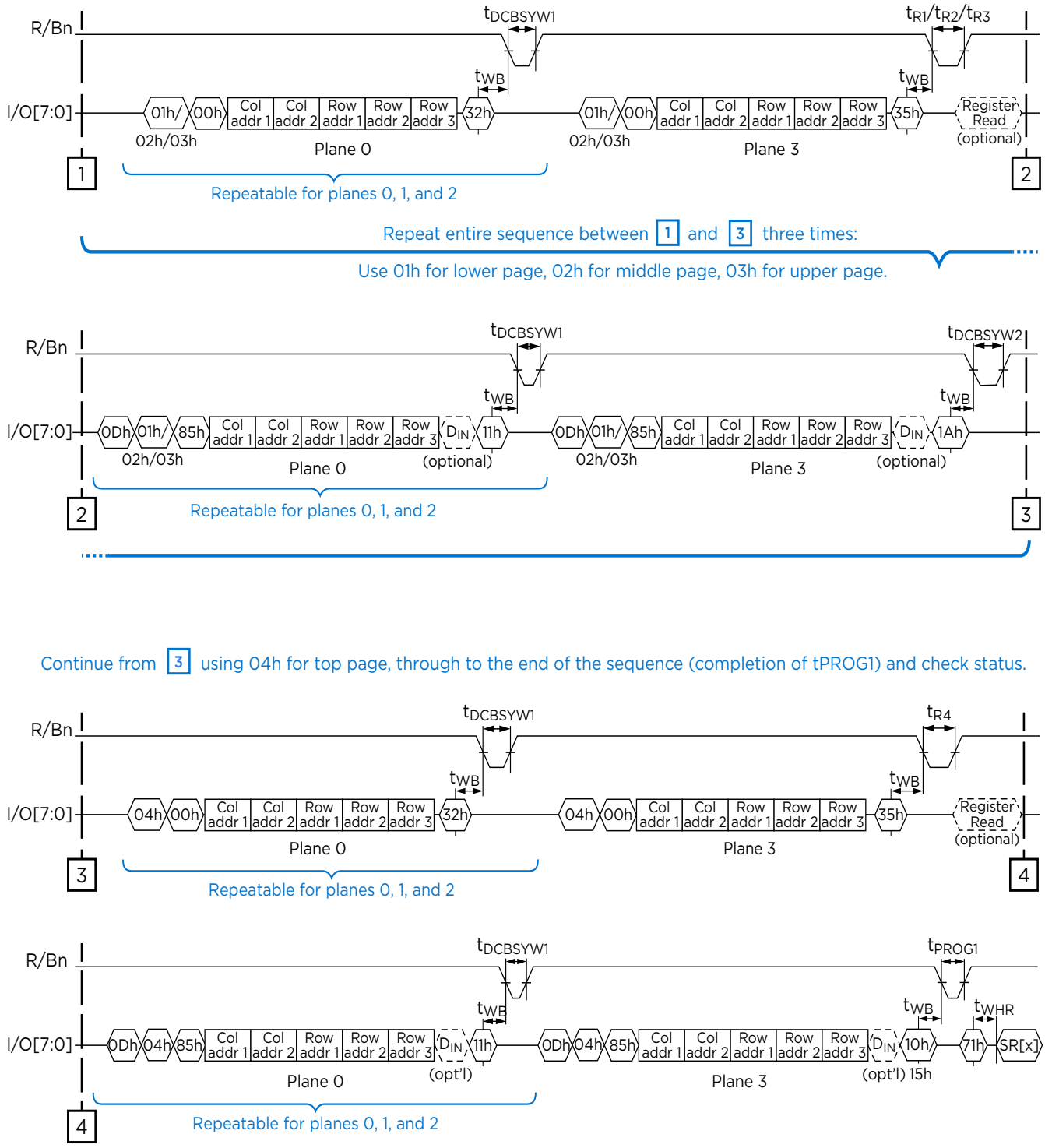
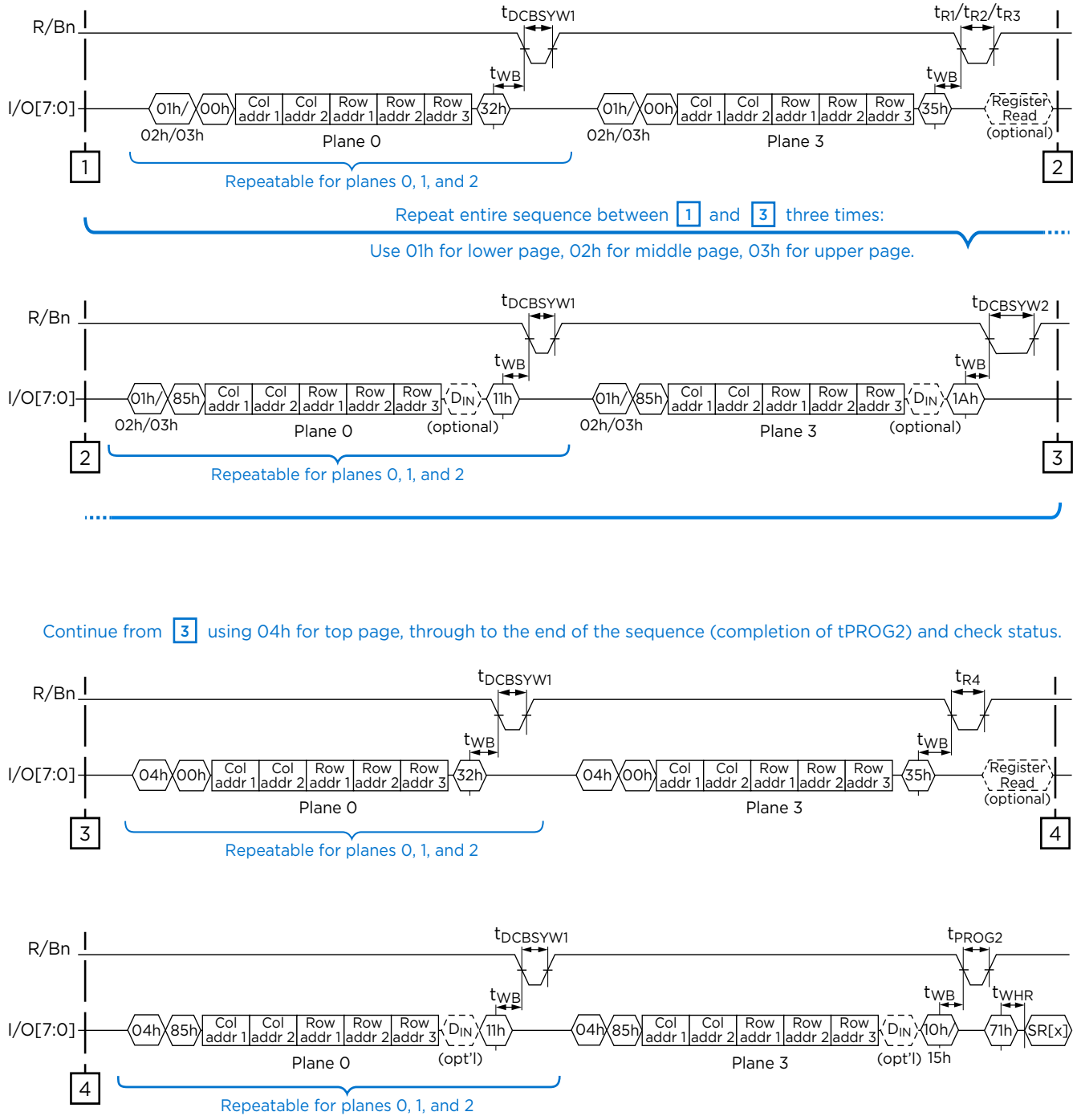


Figure 71: Multi-Plane Copy-Back Program Example: Second Cycle



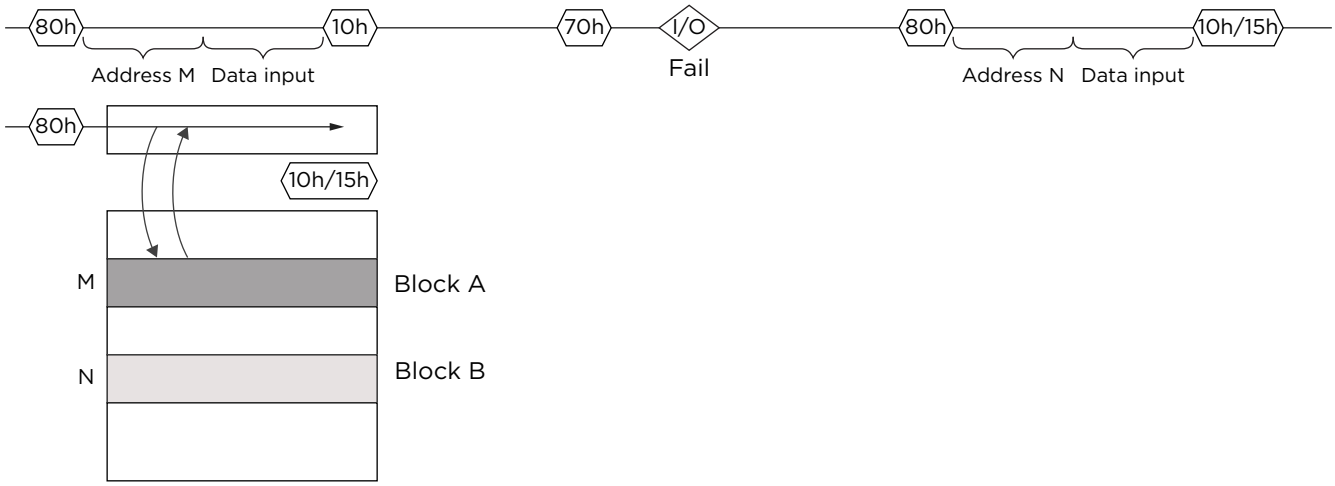
DRAFT Rev. 0.1 7/20/22

10.2.4 Programming Failure

If the programming result for page address M is “fail,” do not try to reprogram the page M data to address N in the same block. Instead, reprogram the page M data to address N in a different block.

The initial input sequence—the 80h command, the address, and data—must be reissued because the previous input data has been lost.

Figure 72: Failed Program Attempt



11 Erase Operations

11.1 SLC Block Erase

Block Erase is performed on a block basis. Only three cycles of row addresses are required for Block Erase. Any page address issued within the cycles is ignored; plane and block addresses are valid. After a Block Erase operation has completed, all bits in the block are set to 1. SR[2] is valid for this command after SR[6] transitions from 0 to 1 until the device goes busy following the next command issued.

In SLC mode, Block Erase requires the A2h command as a prefix to the 60h command.

Multi-Block SLC Erase: enables users to erase blocks on each plane simultaneously.

The same plane address must not be set twice within an address-setting sequence for Multi-Block Erase operations. Block addresses do not have to be the same on each plane.

Figure 73: Single-Plane SLC Block Erase

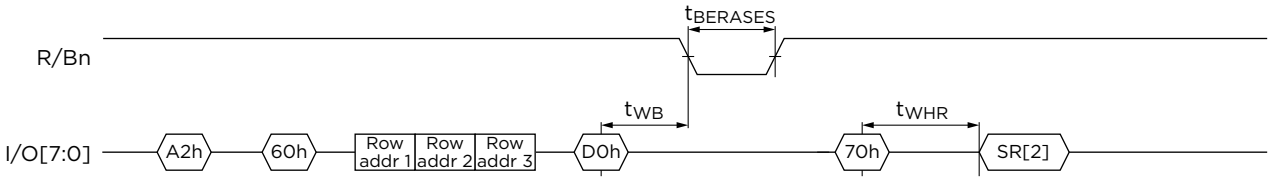
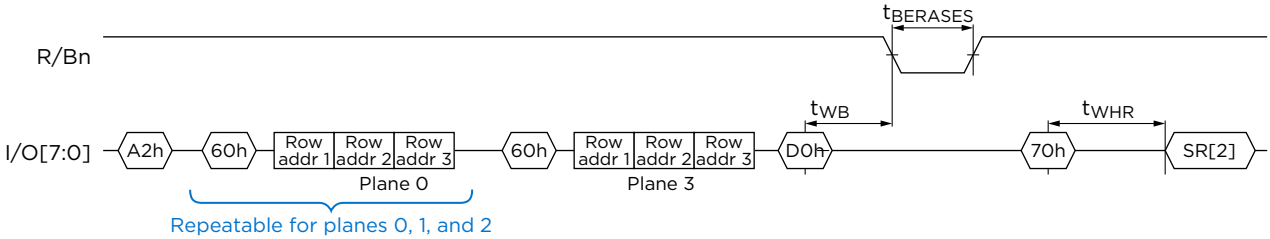


Figure 74: Multi-Plane SLC Block Erase



11.2 QLC Block Erase

Block Erase operates on a block basis. Only three cycles of row addresses are required for a Block Erase operation. A page address issued within these cycles is ignored; however, plane and block addresses are valid.

After a Block Erase operation completes, all bits in the block are set to 1. After SR[6] transitions from 0 to 1, SR[0] is valid for Block Erase until the device goes busy for the next command.

Multi-Block QLC Erase: enables users to erase blocks on each plane simultaneously.

The same plane address must not be set twice within an address-setting sequence for Multi-Block Erase operations. Block addresses do not have to be the same on each plane.

Figure 75: Single-Plane QLC Block Erase

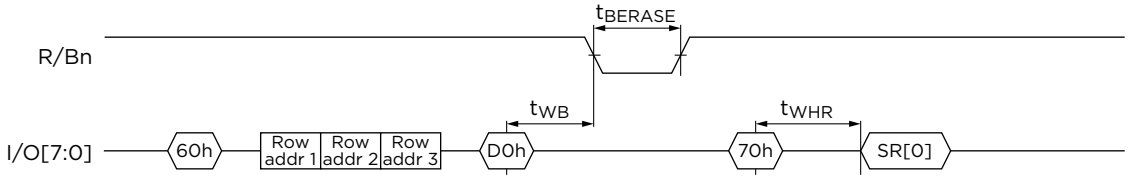
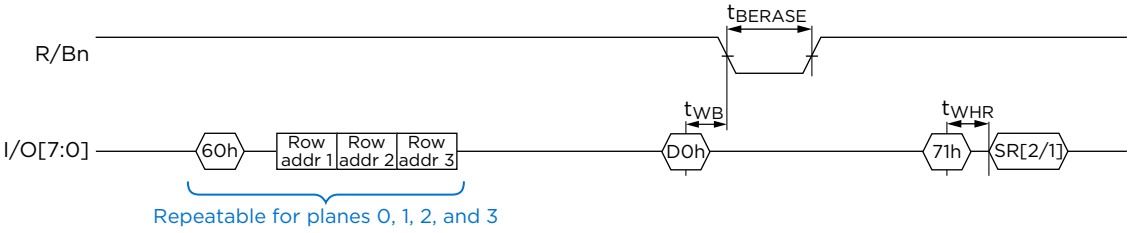


Figure 76: Multi-Plane QLC Block Erase



12 Device Status Operations

12.1 Read Status

In single-plane operations, the Read Status (70h) command retrieves a status value for the last command issued. If more than one multi-plane operation is in progress on a single device, Read Status (70h) returns the collective status value of the independent status register bits as defined in Table 60, and the Read Status (71h) command returns the status of two planes on a single device, as defined in Table 61 on page 110. For timing, see Figure 77, "Read Status," on page 111.

Table 60: Read Status Definition for 70h, and F1h–F8h

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Definition of value	0: Protected 1: Unprotected	Cache Busyn 0: Busy 1: Ready	True Busyn 0: Busy 1: Ready	DNU[1]	SLC previous operation 0: All planes pass 1: Either plane fails	SLC current operation 0: All planes pass 1: Either plane fails	QLC previous operation 0: All planes pass 1: Either plane fails	QLC current operation 0: All planes pass 1: Either plane fails
Block Erase[2]	Write protect	Ready/ Busy	NU[1]	DNU	NU	SLC Pass/Fail	NU	QLC Pass/Fail
Cache Erase	Write protect	Ready/ Busy	Cache Ready/ Busy	DNU	NU	SLC Pass/Fail	NU	QLC Pass/Fail
Page Program[3]	Write protect	Ready/ Busy	Ready/ Busy for Flash array	DNU	NU	SLC Pass/Fail	NU	QLC Pass/Fail
Cache Program[4]	Write protect	Ready/ Busy for host	Ready/ Busy for Flash array	DNU	SLC Pass/ Fail for previous page	SLC Pass/ Fail current page	QLC Pass/ Fail for previous page	QLC Pass/ Fail current page
Read	Write protect	Ready/ Busy	NU	DNU	NU	NU	NU	NU
Cache Read	Write protect	Ready/ Busy for host	Ready/ Busy for Flash array	DNU	NU	NU	NU	NU
Copy-Back[3]	Write protect	Ready/ Busy	Ready/ Busy for Flash array	DNU	NU	SLC Pass/Fail	NU	QLC Pass/Fail

Note 1. DNU = do not use; NU = not used.

2. During Block Erase, I/O0 and I/O2 are valid only when I/O6 is in the ready state.

3. During Page Program or Copy-Back operations, I/O0 and I/O2 are valid only when: a) I/O6 is in the ready state and 10h is used for the final page; ***or*** b) when I/O5 is in the ready state and 15h is used for the final page.
4. During Cache Program operations, I/O0 and I/O2 are valid only when I/O5 is in the ready state, and I/O1 or I/O3 are valid only when I/O6 is in the ready state.

Table 61: QLC Read Status Definition for 71h

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
				Current operation				
				Plane 3	Plane 2	Plane 1	Plane 0	
Definition of value	0: Protected 1: Unprotected	Cache Busyn 0: Busy 1: Ready	True Busyn 0: Busy 1: Ready	0: Pass 1: Fail	0: Pass 1: Fail	0: Pass 1: Fail	0: Pass 1: Fail	QLC current operation 0: All planes pass 1: Either plane fails
Block Erase[2]	Write protect	Ready/ Busy	NU[1]	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail
Page Program[3]	Write protect	Ready/ Busy	Ready/Busy for Flash array	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail
Cache Program[4]	Write protect	Ready/ Busy for host	Ready/Busy for Flash array	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail for current page
Read	Write protect	Ready/ Busy	NU	NU	NU	NU	NU	NU
Cache Read	Write protect	Ready/ Busy for host	Ready/Busy for Flash array	NU	NU	NU	NU	NU
Copy-Back[3]	Write protect	Ready/ Busy	Ready/Busy for Flash array	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail

Note 1. NU = not used.

2. During Block Erase I/O0, I/O1, I/O2, I/O3, and I/O4 are valid only when I/O6 is in the ready state.
3. During Page Program or Copy-Back operations, I/O0, I/O1, I/O2, I/O3, I/O4 are valid only when:
   a) I/O6 is in the ready state and 10h is used for the final page; ***or***
   b) when I/O5 is in the ready state and 15h is used for the final page.
4. During Cache Program operations, I/O0, I/O1, I/O2, I/O3, and I/O4 are valid only when I/O5 is in the ready state.

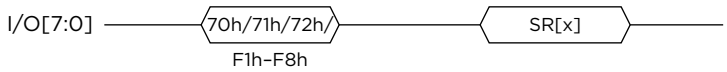
Table 62: SLC Read Status Definition for 72h

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
				Current Operation				
						Plane 1	Plane 0	
Definition of value	0: Protected 1: Unprotected	Cache Busyn 0: Busy 1: Ready	True Busyn 0: Busy 1: Ready	0: Pass 1: Fail	0: Pass 1: Fail	0: Pass 1: Fail	0: Pass 1: Fail	SLC current operation 0: All planes pass 1: Either plane fails
Block Erase[2]	Write protect	Ready/ Busy	NU[1]	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail
Page Program[3]	Write protect	Ready/ Busy	Ready/Busy for Flash array	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail
Cache Program[4]	Write protect	Ready/ Busy for host	Ready/Busy for Flash array	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail for current page
Read	Write protect	Ready/ Busy	NU	NU	NU	NU	NU	NU
Cache Read	Write protect	Ready/ Busy for host	Ready/Busy for Flash array	NU	NU	NU	NU	NU
Copy-Back[3]	Write protect	Ready/ Busy	Ready/Busy for Flash array	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/ Fail	Pass/Fail

Note 1. NU = not used.

2. During Block Erase I/O0, I/O1, I/O2, I/O3, and I/O4 are valid only when I/O6 is in the ready state.
3. During Page Program or Copy-Back operations, I/O0, I/O1, I/O2, I/O3, I/O4 are valid only when:
   a) I/O6 is in the ready state and 10h is used for the final page; ***or***
   b) when I/O5 is in the ready state and 15h is used for the final page.
4. During Cache Program operations, I/O0, I/O1, I/O2, I/O3, and I/O4 are valid only when I/O5 is in ready state.

Figure 77: Read Status



Note 1. See Figure 98, “Toggle Mode Status Read Cycle,” on page 140 for Toggle Mode timing.

12.2 Read Status Enhanced

The Read Status Enhanced (78h) command is used to check the status of the selected device, and requires row-address-setting steps before reading the status value (see Figure 78, “Read Status Enhanced,” on page 113).

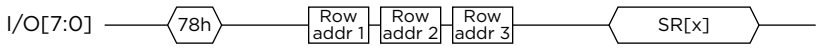
Table 63: Read Status Definition for 78h

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Definition of value	0: Protected 1: Unprotec-ted	Cache Busyn 0: Busy 1: Ready	True Busyn 0: Busy 1: Ready	DNU[1]	SLC previous operation 0: All planes pass 1: Either plane fail	SLC current operation 0: All planes pass 1: Either plane fail	QLC previous operation 0: All planes pass 1: Either plane fail	QLC current operation 0: All planes pass 1: Either plane fail
Block Erase[2]	Write protect	Ready/ Busy	NU[1]	DNU	NU	SLC Pass/ Fail	NU	Pass/Fail
Page Program[3]	Write protect	Ready/ Busy	Ready/ Busy for Flash array	DNU	NU	SLC Pass/ Fail	NU	Pass/Fail
Cache Program[4]	Write protect	Ready/ Busy for host	Ready/ Busy for Flash array	DNU	SLC Pass/Fail for previous page on PB0 or PB1	SLC Pass/Fail for current page on PB0 or PB1	Pass/Fail for previous page on PB0 or PB1	Pass/Fail for cur-rent page on PB0 or PB1
Read	Write protect	Ready/ Busy	NU	DNU	NU	NU	NU	NU
Cache Read	Write protect	Ready/ Busy for host	Ready/ Busy for Flash array	DNU	NU	NU	NU	NU
Copy-Back[3]	Write protect	Ready/ Busy	Ready/ Busy for Flash array	DNU	NU	SLC Pass/ Fail	NU	Pass/Fail

Note 1. DNU = do not use; NU = not used.

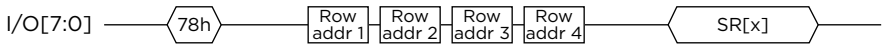
2. During Block Erase, I/O0 and I/O2 are valid only when I/O6 is in the ready state.
3. During Page Program or Copy-Back operations, if 10h is used for the final page, then I/O0 and I/O2 are valid only when I/O6 is in the ready state; if 15h is used for the final page, I/O5 must be in the ready state.
4. During Cache Program operations, I/O0 or I/O2 are valid only when I/O5 is in the ready state, and I/O1 or I/O3 are valid only when I/O6 is in the ready state.

Figure 78: Read Status Enhanced



Note 1. See Figure 98, "Toggle Mode Status Read Cycle," on page 140 for Toggle Mode timing.

Figure 79: Read Status Enhanced with More Than Two Die per CEn



13 Reset Operations

The Reset (FFh) command resets the device to the power-on default settings, and it is required as the first command following power-up. FFh does not reset features controlled by the Set Features commands, such as the interface settings.

Issuing the Reset command with any operation in the busy state will abort all active operations, making content in any cells being programmed invalid because each cell is either erased or only partially programmed. After active operations are aborted, the command register is cleared and ready to receive the next command.

If the Reset command is issued during a caching operation (for example, Cache Program), both the most recent page operation, as well as the previous page operation, could be aborted, based on when the FFh command was issued. If the Reset command is issued during an active Reset operation, the new Reset command will be accepted and the device will complete execution of the reset operation after tRST has elapsed. See Figure 80 through Figure 89, “Power-On Reset,” on page 118, for Reset timing.

13.1 Reset Command Restriction

If the FAh or FFh Reset command is issued during a Program operation, all four pages in the WL will be invalid.

Figure 80: Reset: Input During Read Operation

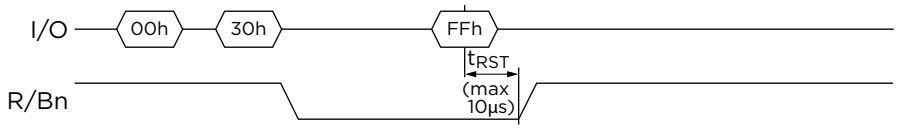


Figure 81: Reset: Input During Program Operation

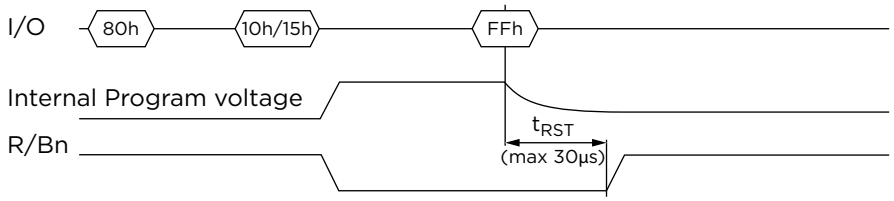


Figure 82: Reset: Input During Erase Operation

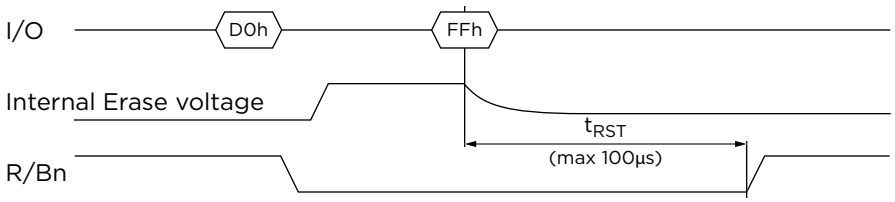


Figure 83: Reset: Input While in the Ready State

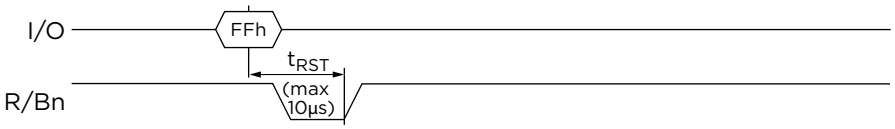


Figure 84: Reset: Input Following Reset Operation

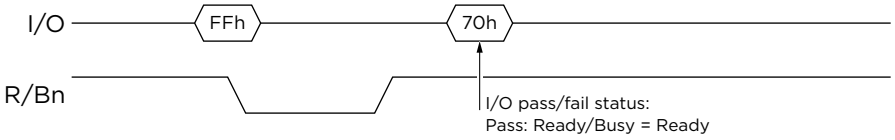
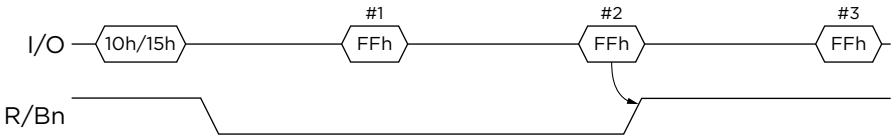


Figure 85: Reset: Multiple Inputs in Succession



Note 1. The second FFh command is invalid; the third is valid.

13.2 Reset by Die

A single die that shares a CEn with another die can be reset individually by issuing the FAh command with the appropriate row address for that die.

Figure 86: Reset by Die

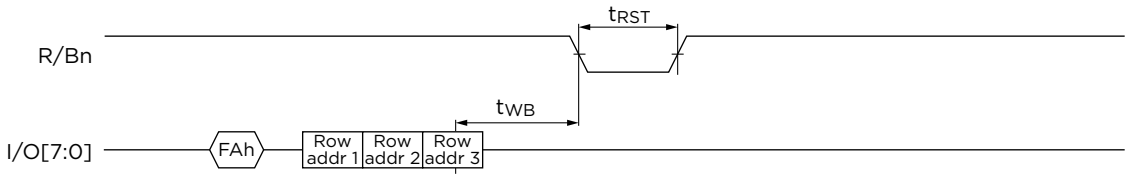
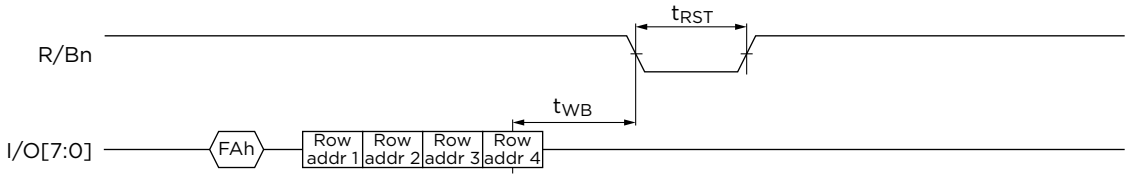


Figure 87: Reset by Die with More Than Two Die per CEn

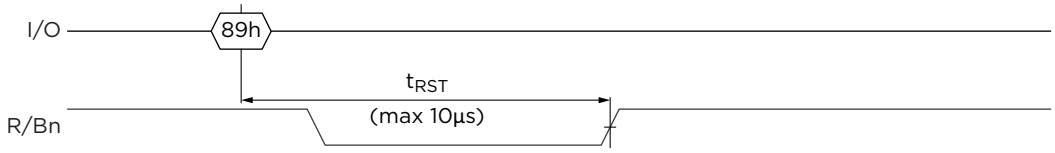


13.3 Set Features Register Reset

The Set Features Register Reset command resets the registers set by the Set Features command, to their default values.

When 89h is issued, the device goes busy for tRST. During this time, the selected device aborts all array operations and resets all of the parameters set by the Set Features command to their default values. Command 89h must not be used as the Reset command at power up; FFh is required following power up.

Figure 88: Set Features Register Reset



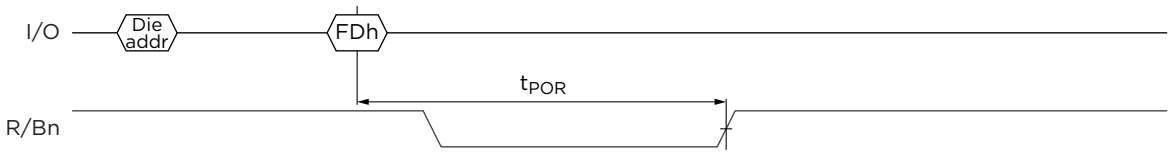
13.3.1 Power-On Reset During Operations

The FDh POR command is issued to trigger a POR operation to NAND Flash. The device will reset to the power-on default settings after tPOR has elapsed, with the exception of the Set Features Register, which is ***not*** reset by the FDh command. This command can only be issued when the device is ready; i.e., there are no active operations in progress and R/Bn is high. Issuing the FDh command while R/Bn is executing an operation is prohibited.

This command can only be used with a chip select command to start a manual POR by die (see Figure 89). If no chip is selected prior to issuing the FDh command, the command is ignored. During the tPOR busy time, only a Status Read (70h) command or one of the chip select commands will be accepted.

If multiple die share the same CEn, the FDh command can be issued to the selected die when any of the non-selected die are executing POR operations or are in the ready state.

Figure 89: Power-On Reset



Note 1. A Chip Select command (Fxh) must be issued prior to issuing the FDh command.

14 Set Features Operations

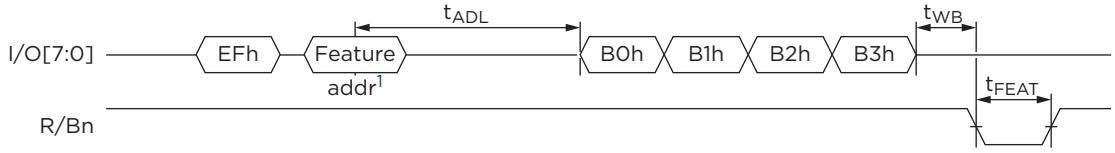
Users can set particular features with the Set Features command by writing four bytes of parameter values to the specified feature address (see Figure 90). The EFh command is accepted by all die as a global command to a specific target (i.e., multiple die sharing the same CEn).

Issuing a D5h command followed by the die address initiates a Set Features command to the selected die on a given target. The EFh command is only accepted when all of the die sharing the same CEn are in the cache-ready or the true-ready state.

The D5h command is only accepted when the selected die is in the cache-ready or the true-ready state. User-changeable features controlled by the Set Features command are provided in Table 64, "Set Features Addressing (without aIPR)," on page 120, **or** Table 65, "Set Features Addressing (with aIPR)," on page 120; **and in** Table 4, "Dynamic Read Mode Settings with 5Dh (w/o aIPR)," on page 14 **or** Table 5, "Dynamic Read Mode Settings with 5Dh (with aIPR)," on page 15.

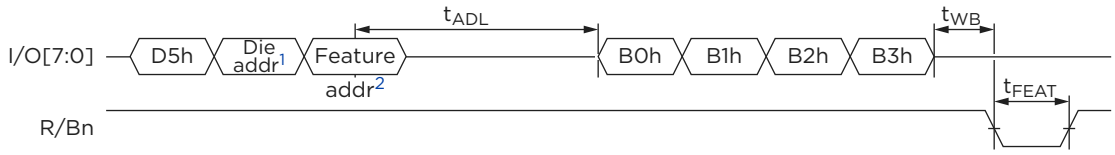
Caution: Do not toggle DQS/DQSn between the EFh/D5h command and the Feature addresses shown in Figures 90 and 91.

Figure 90: Set Features



Note 1. Feature addresses are provided in Table 64, "Set Features Addressing (without aIPR)," on page 120 **and** Table 65, "Set Features Addressing (with aIPR)," on page 120.

Figure 91: Set Features by Die



Note 1. The die address is one byte (00h: die 0, 01h: die 1... 07h: die 7)

2. Feature addresses are provided in Table 64, "Set Features Addressing (without aIPR)," on page 120 **and** Table 65, "Set Features Addressing (with aIPR)," on page 120.
3. In a multi-die package, after D5h has been initiated on a given die, initiating operations on any other die sharing the same CEn is prohibited until D5h is complete.

Table 64: Set Features Addressing (without aIPR)

Command	Feature Address	Description
EFh or D5h + die address	02h	Toggle Mode-specific setting
	10h	CTT interface output drive setting
	22h	LTT interface setting
	23h	Internal V_{REFQ} setting
	8Bh (14h)	Dynamic Read setting for SLC Read
	9Bh	Dynamic Read setting for S2/S8/S10/S12
	9Ch	Dynamic Read setting for S1/S3/S7/S13
	9Dh	Dynamic Read setting for S5/S11/S14
	9Eh	Dynamic Read setting for S4/S6/S9/S15

Table 65: Set Features Addressing (with aIPR)

Command	Feature Address	Description	Plane
EFh or D5h + die address	02h	Toggle Mode-specific setting	N/A
	10h	CTT interface output drive setting	
	22h	LTT interface setting	
	23h	Internal V_{REFQ} setting	
	8Bh (14h)	Dynamic Read setting for SLC Read	0
	8Ah (13h)	Dynamic Read setting for SLC Read	1
	A5h	Dynamic Read setting for SLC Read	2
	ABh	Dynamic Read setting for SLC Read	3
	9Bh	Dynamic Read setting for S2/S8/S10/S12	0
	9Ch	Dynamic Read setting for S1/S3/S7/S13	0
	9Dh	Dynamic Read setting for S5/S11/S14	0
	9Eh	Dynamic Read setting for S4/S6/S9/S15	0
	85h	Dynamic Read setting for S2/S8/S10/S12	1
	86h	Dynamic Read setting for S1/S3/S7/S13	1
	87h	Dynamic Read setting for S5/S11/S14	1
	88h	Dynamic Read setting for S4/S6/S9/S15	1
	A0h	Dynamic Read setting for S2/S8/S10/S12	2
	A1h	Dynamic Read setting for S1/S3/S7/S13	2
	A2h	Dynamic Read setting for S5/S11/S14	2
	A3h	Dynamic Read setting for S4/S6/S9/S15	2
	A6h	Dynamic Read setting for S2/S8/S10/S12	3
	A7h	Dynamic Read setting for S1/S3/S7/S13	3
	A8h	Dynamic Read setting for S5/S11/S14	3
	A9h	Dynamic Read setting for S4/S6/S9/S15	3

14.1 Toggle Mode-Specific Setting (02h)

This setting is required to use reference voltage and complementary signals and ODT. The DQS latency cycle can also be configured by using this Set Features operation to read the first valid data correctly.

The differential clock must be set correctly in Set Features register address 02h, bytes B0 and B1, regardless of the default parameter setting.

Table 66: Feature Address 02h

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
B0	ODT (with RTT value)				0	RE	DQSn	V_{REFQ}
B1	DQS_LATENCY				RE_LATENCY			
B2	0	LTT V_{OH}	0	0	Internal V_{REFQ} value settings		LTT mode enable	
B3	Reserved							

Table 67: Feature Address 02h Parameter Definitions

Parameter	Parameter Value	Default	Function/Value
ODT (with RTT value)	b0000	X	0 Ohms
	b0001		150 Ohms
	b0010		100 Ohms
	b0011		75 Ohms
	b0100		50 Ohms
RE (complement of REn)	0		Off (single-ended)
	1	X	On (differential)
DQSn (complement of DQS)	0		Off (single-ended)
	1	X	On (differential)
V_{REFQ} configuration	0	X	Off (internal V_{REFQ})
	1		On (external V_{REFQ})
DQS_LATENCY (latency cyclesfor DQS/DQSn)	b00	X	0 latency cycles
	b01		1 latency cycle
	b10		2 latency cycles
	b11		4 latency cycles
RE_LATENCY (latency cycles for REn/RE)	b00	X	0 latency cycles
	b01		1 latency cycle
	b10		2 latency cycles
	b11		4 latency cycles
V_{OH} setting (in LTT mode only)	0	X	V_{CCQ}/3
	1		V_{CCQ}/2.5
INT_VREFQ_SET	b00		Reserved
	b01		Reserved
	b10	X	Default range
	b11		Reserved
LTT mode enable	b00	X	CTT
	b01		LTT
	b10		Reserved
	b11		Reserved

Note 1. For more information on latency cycles, see "14.5 Warm-up/Latency Cycles" on page 131.

14.2 CTT Interface Output Drive Settings (10h)

This device supports three kinds of output drive settings for matching system characteristics. Nominal output drive strength is the power-on default value. Using the Set Features (EFh) command, followed by a 10h address (drive setting feature address), the host can select a different drive strength setting.

The output impedance range, from minimum to maximum, covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal value. Users can tune the data output drive impedance by setting the drive-strength register value.

At power-up, the register reverts to the default setting.

Table 68: Feature Address 10h

Data	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
B0	Reserved					CTT mode RON adjustment		
B1	Reserved							
B2	Reserved							
B3	Reserved							

Note 1. B1, B2, and B3 are reserved and must be written with 00h.

Table 69: Feature Address 10h Parameter Definitions

Parameter	Parameter Value	Default	Function/Value	Note
CTT mode output driver RON adjustment	b100	X	Nominal (37.5 Ohms)	Address 10h, B0[7:3] must be set to zeros
	b010		Underdrive (50 Ohms)	
	Others		Nominal	

14.3 LTT Interface Setting (22h)

Table 70: Feature Address 22h

Data	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
B0	LTT mode output driver pull-down drive strength				LTT mode channel ODT value for V_{OH} calibration			
B1	Target ODT parameter for DQ/DQS in LTT mode				Non-target die ODT setting for DQ/DQS in LTT mode			
B2	Target ODT parameter for REn/RE in LTT mode				Non-target die ODT setting for REn/RE input in LTT mode			
B3	Reserved				Non-target die ODT setting for DQ/DQS output in LTT mode			

14.3.1 Bit Definitions for Feature Address 22h

Table 71: B0 Settings [7:4]

LTT Settings: Pull-Down Drive Strength[1]									
Output Drive Strength									
7	6	5	4	3	2	1	0	B0	Ohms
0	0	0	0						RZQ/6 (50)
0	0	0	1						RZQ/2 (150)
0	0	1	0						RZQ/3 (100)
0	0	1	1						RZQ/4 (75)
0	1	0	0					def	RZQ/6 (50)
0	1	0	1						RZQ/1 (300)
0	1	1	0						RZQ/5 (60)
0	1	1	1						RZQ/7 (42.9)
1	0	0	0						RZQ/8 (37.5)
1	0	0	1						RZQ/12 (25)
1	0	1	0						RZQ/6 (50)
1	0	1	1						RZQ/6 (50)
1	1	0	0						RZQ/6 (50)
1	1	0	1						RZQ/6 (50)
1	1	1	0						RZQ/6 (50)
1	1	1	1						RZQ/6 (50)

B0 Settings [3:0]

LTT Channel ODT Settings: V_{OH}[2] Calibration									
Non-Target ODT Resistance									
7	6	5	4	3	2	1	0	B0	Ohms[1]
				0	0	0	0		RZQ/6 (50)
				0	0	0	1		RZQ/2 (150)
				0	0	1	0		RZQ/3 (100)
				0	0	1	1		RZQ/4 (75)
				0	1	0	0	def	RZQ/6 (50)
				0	1	0	1		RZQ/1 (300)
				0	1	1	0		RZQ/5 (60)
				0	1	1	1		RZQ/7 (42.9)
				1	0	0	0		RZQ/8 (37.5)
				1	0	0	1		RZQ/12 (25)
				1	0	1	0		RZQ/6 (50)
				1	0	1	1		RZQ/6 (50)
				1	1	0	0		RZQ/6 (50)
				1	1	0	1		RZQ/6 (50)
				1	1	1	0		RZQ/6 (50)
				1	1	1	1		RZQ/6 (50)

Note 1. RZQ/5, RZQ/7, RZQ/12 are not available [7:0].

2. If VOH_25 = 1, user must set the value to ≥ 75 Ohms [3:0]

Table 72: B1 Settings [7:4]

LTT Settings: Target Die DQ/DQS Input									
									ODT Resistance
7	6	5	4	3	2	1	0	B1	Ohms
0	0	0	0					def	disable
0	0	0	1						RZQ/2 (150)
0	0	1	0						RZQ/3 (100)
0	0	1	1						RZQ/4 (75)
0	1	0	0						RZQ/6 (50)
0	1	0	1						RZQ/1 (300)
0	1	1	0						RZQ/5 (60)
0	1	1	1						RZQ/7 (42.9)
1	0	0	0						RZQ/8 (37.5)
1	0	0	1						RZQ/1.5 (200)
1	0	1	0						disable
1	0	1	1						disable
1	1	0	0						disable
1	1	0	1						disable
1	1	1	0						disable
1	1	1	1						disable

Note 1. RZQ/5, RZQ/7, RZQ/1.5 are not available.

B1 Settings [3:0]

LTT Settings: Non-Target Die DQ/DQS Input									
									ODT Resistance
7	6	5	4	3	2	1	0	B1	Ohms
				0	0	0	0	def	disable
				0	0	0	1		RZQ/2 (150)
				0	0	1	0		RZQ/3 (100)
				0	0	1	1		RZQ/4 (75)
				0	1	0	0		RZQ/6 (50)
				0	1	0	1		RZQ/1 (300)
				0	1	1	0		RZQ/5 (60)
				0	1	1	1		RZQ/7 (42.9)
				1	0	0	0		RZQ/8 (37.5)
				1	0	0	1		RZQ/1.5 (200)
				1	0	1	0		disable
				1	0	1	1		disable
				1	1	0	0		disable
				1	1	0	1		disable
				1	1	1	0		disable
				1	1	1	1		disable

Table 73: B2 Settings [7:4]

LTT Settings: Target Die REn Input									
									ODT Resistance
7	6	5	4	3	2	1	0	B2	Ohms
0	0	0	0					def	disable
0	0	0	1						RZQ/2 (150)
0	0	1	0						RZQ/3 (100)
0	0	1	1						RZQ/4 (75)
0	1	0	0						RZQ/6 (50)
0	1	0	1						RZQ/1 (300)
0	1	1	0						RZQ/5 (60)
0	1	1	1						RZQ/7 (42.9)
1	0	0	0						RZQ/8 (37.5)
1	0	0	1						RZQ/1.5 (200)
1	0	1	0						disable
1	0	1	1						disable
1	1	0	0						disable
1	1	0	1						disable
1	1	1	0						disable
1	1	1	1						disable

Note 1. RZQ/5, RZQ/7, RZQ/1.5 are not available.

B2 Settings [3:0]

LTT Settings: Non-Target Die REn Input									
									ODT Resistance
7	6	5	4	3	2	1	0	B2	Ohms
				0	0	0	0	def	disable
				0	0	0	1		RZQ/2 (150)
				0	0	1	0		RZQ/3 (100)
				0	0	1	1		RZQ/4 (75)
				0	1	0	0		RZQ/6 (50)
				0	1	0	1		RZQ/1 (300)
				0	1	1	0		RZQ/5 (60)
				0	1	1	1		RZQ/7 (42.9)
				1	0	0	0		RZQ/8 (37.5)
				1	0	0	1		RZQ/1.5 (200)
				1	0	1	0		disable
				1	0	1	1		disable
				1	1	0	0		disable
				1	1	0	1		disable
				1	1	1	0		disable
				1	1	1	1		disable

Table 74: B3 Settings [3:0]

LTT Settings: Non-Target Die DQ/DQS Output									
									ODT Resistance
7	6	5	4	3	2	1	0	B3	Ohms
				0	0	0	0	def	disable
				0	0	0	1		RZQ/2 (150)
				0	0	1	0		RZQ/3 (100)
				0	0	1	1		RZQ/4 (75)
				0	1	0	0		RZQ/6 (50)
				0	1	0	1		RZQ/1 (300)
				0	1	1	0		RZQ/5 (60)
				0	1	1	1		RZQ/7 (42.9)
				1	0	0	0		RZQ/8 (37.5)
				1	0	0	1		RZQ/1.5 (200)
				1	0	1	0		disable
				1	0	1	1		disable
				1	1	0	0		disable
				1	1	0	1		disable
				1	1	1	0		disable
				1	1	1	1		disable

Note 1. RZQ/5, RZQ/7, RZQ/1.5 are not available.

14.4 Internal V_{REFQ} Setting (23h)

Table 75: Feature Address 23h—Internal V_{REFQ}

Data	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
B0	Internal V_{REFQ} value settings for training							Reseved
B1	Reserved							
B2	Reserved							
B3	Reserved							

Table 76: Feature Address 23h—Parameter Definitions for Internal V_{REFQ}

Internal V_{REFQ} Value/Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	—	20.50%	—	V_{CCQ}
VREFQ_min	7.50%	—	—	V_{CCQ}
VREFQ_max	—	—	71.00%	V_{CCQ}
VREFQ_step_size		0.50%		V_{CCQ}
VREFQ_setting_tolerance	-1.75%	0%	1.75%	V_{CCQ}
Settling time	—	—	100	ns

Note 1. The default setting for I/O[7:1] is 0011 010, corresponding with V_{REFQ} = 20.50% of V_{CCQ}.

Table 77: Feature Address 23h—Internal V_{REFQ} Settings

VREFIO_DQ (% of V_{CCQ})		7	6	5	4	3	2	1	0	VREFIO_DQ (% of V_{CCQ})		7	6	5	4	3	2	1	0
Part 1 of 2-part table: [7] = 0; Default = 20.50																			
7.50		0	0	0	0	0	0	0		23.50		0	1	0	0	0	0	0	
8.00		0	0	0	0	0	0	1		24.00		0	1	0	0	0	0	1	
8.50		0	0	0	0	0	1	0		24.50		0	1	0	0	0	1	0	
9.00		0	0	0	0	0	1	1		25.00		0	1	0	0	0	1	1	
9.50		0	0	0	0	1	0	0		25.50		0	1	0	0	1	0	0	
10.00		0	0	0	0	1	0	1		26.00		0	1	0	0	1	0	1	
10.50		0	0	0	0	1	1	0		26.50		0	1	0	0	1	1	0	
11.00		0	0	0	0	1	1	1		27.00		0	1	0	0	1	1	1	
11.50		0	0	0	1	0	0	0		27.50		0	1	0	1	0	0	0	
12.00		0	0	0	1	0	0	1		28.00		0	1	0	1	0	0	1	
12.50		0	0	0	1	0	1	0		28.50		0	1	0	1	0	1	0	
13.00		0	0	0	1	0	1	1		29.00		0	1	0	1	0	1	1	
13.50		0	0	0	1	1	0	0		29.50		0	1	0	1	1	0	0	
14.00		0	0	0	1	1	0	1		30.00		0	1	0	1	1	0	1	
14.50		0	0	0	1	1	1	0		30.50		0	1	0	1	1	1	0	
15.00		0	0	0	1	1	1	1		31.00		0	1	0	1	1	1	1	
15.50		0	1	1	0	0	0	0		31.50		0	1	1	0	0	0	0	
16.00		0	1	1	0	0	0	1		32.00		0	1	1	0	0	0	1	
16.50		0	1	1	0	0	1	0		32.50		0	1	1	0	0	1	0	
17.00		0	1	1	0	0	1	1		33.00		0	1	1	0	0	1	1	
17.50		0	1	1	0	1	0	0		33.50		0	1	1	0	1	0	0	
18.00		0	1	1	0	1	0	1		34.00		0	1	1	0	1	0	1	
18.50		0	1	1	0	1	1	0		34.50		0	1	1	0	1	1	0	
19.00		0	1	1	0	1	1	1		35.00		0	1	1	0	1	1	1	
19.50		0	1	1	1	0	0	0		35.50		0	1	1	1	0	0	0	
20.00		0	1	1	1	0	0	1		36.00		0	1	1	1	0	0	1	
20.50	def	0	1	1	1	0	1	0		36.50		0	1	1	1	0	1	0	
21.00		0	1	1	1	0	1	1		37.00		0	1	1	1	0	1	1	
21.50		0	1	1	1	1	0	0		37.50		0	1	1	1	1	0	0	
22.00		0	1	1	1	1	0	1		38.00		0	1	1	1	1	0	1	
22.50		0	1	1	1	1	1	0		38.50		0	1	1	1	1	1	0	
23.00		0	1	1	1	1	1	1		39.00		0	1	1	1	1	1	1	
Continues at top of the column to the right										Continues on the next page									

Table 77: Feature Address 23h—Internal V_{REFQ} Settings (cont'd)

VREFIO_DQ (% of V_{CCQ})	7	6	5	4	3	2	1	0	VREFIO_DQ (% of V_{CCQ})	7	6	5	4	3	2	1	0
Part 2 of 2-part table: [7] = 1																	
39.50	1	0	0	0	0	0	0		55.50	1	1	0	0	0	0	0	
40.00	1	0	0	0	0	0	1		56.00	1	1	0	0	0	0	1	
40.50	1	0	0	0	0	1	0		56.50	1	1	0	0	0	1	0	
41.00	1	0	0	0	0	1	1		57.00	1	1	0	0	0	1	1	
41.50	1	0	0	0	1	0	0		57.50	1	1	0	0	1	0	0	
42.00	1	0	0	0	1	0	1		58.00	1	1	0	0	1	0	1	
42.50	1	0	0	0	1	1	0		58.50	1	1	0	0	1	1	0	
43.00	1	0	0	0	1	1	1		59.00	1	1	0	0	1	1	1	
43.50	1	0	0	1	0	0	0		59.50	1	1	0	1	0	0	0	
44.00	1	0	0	1	0	0	1		60.00	1	1	0	1	0	0	1	
44.50	1	0	0	1	0	1	0		60.50	1	1	0	1	0	1	0	
45.00	1	0	0	1	0	1	1		61.00	1	1	0	1	0	1	1	
45.50	1	0	0	1	1	0	0		61.50	1	1	0	1	1	0	0	
46.00	1	0	0	1	1	0	1		62.00	1	1	0	1	1	0	1	
46.50	1	0	0	1	1	1	0		62.50	1	1	0	1	1	1	0	
47.00	1	0	0	1	1	1	1		63.00	1	1	0	1	1	1	1	
47.50	1	0	1	0	0	0	0		63.50	1	1	1	0	0	0	0	
48.00	1	0	1	0	0	0	1		64.00	1	1	1	0	0	0	1	
48.50	1	0	1	0	0	1	0		64.50	1	1	1	0	0	1	0	
49.00	1	0	1	0	0	1	1		65.00	1	1	1	0	0	1	1	
49.50	1	0	1	0	1	0	0		65.50	1	1	1	0	1	0	0	
50.00	1	0	1	0	1	0	1		66.00	1	1	1	0	1	0	1	
50.50	1	0	1	0	1	1	0		66.50	1	1	1	0	1	1	0	
51.00	1	0	1	0	1	1	1		67.00	1	1	1	0	1	1	1	
51.50	1	0	1	1	0	0	0		67.50	1	1	1	1	0	0	0	
52.00	1	0	1	1	0	0	1		68.00	1	1	1	1	0	0	1	
52.50	1	0	1	1	0	1	0		68.50	1	1	1	1	0	1	0	
53.00	1	0	1	1	0	1	1		69.00	1	1	1	1	0	1	1	
53.50	1	0	1	1	1	0	0		69.50	1	1	1	1	1	0	0	
54.00	1	0	1	1	1	0	1		70.00	1	1	1	1	1	0	1	
54.50	1	0	1	1	1	1	0		70.50	1	1	1	1	1	1	0	
55.00	1	0	1	1	1	1	1		71.00	1	1	1	1	1	1	1	
Continues at top of the column to the right																	

14.5 Warm-up/Latency Cycles

Warm-up cycles for data input and data output can be provided to support higher-speed operation. Warm-up cycles are only supported in the DDR2, DDR3, DDR4, and DDR5 data interfaces.

Warm-up cycles are supported only when the DDR2, DDR3, DDR4, or DDR5 interface is enabled using Set Features.

14.5.1 Input Warm-up/Latency Cycles

Warm-up cycles for data input provide additional DQS clock cycles at the beginning of a data input burst. There is no associated valid data for these extra DQS clock cycles. The number of additional cycles is configured via the Set Features address 02h. (See Table 64, “Set Features Addressing (without aIPR),” on page 120, **or** Table 65, “Set Features Addressing (with aIPR),” on page 120; **and** Table 66, “Feature Address 02h,” on page 121 for details.)

For each DQS warm-up cycle, the host must provide a DQS cycle with no valid data.

The first valid byte of data to be transmitted from the host will be on the first DQS rising edge following the configured number of DQS warm-up cycles.

14.5.2 Output Warm-up/Latency Cycles

Warm-up cycles for data output provide additional REn clock cycles at the beginning of a data output burst. There is no associated valid data for these additional REn clock cycles. The number of extra cycles is configured via Set Features address 02h. (See Table 14.1, “Toggle Mode-Specific Setting (02h),” on page 121 for details.)

For each REn warm-up cycle, the host will receive a corresponding DQS cycle with no valid data.

The first valid byte of data to be transmitted to the host will be on the first REn rising edge following the configured number of REn warm-up cycles.

14.5.2.1 Warm-up/Latency Cycle Options and Constraints

Warm-up/latency cycles are optional for both data input and data output. If the option is used, input and/or output can each be configured for a different number of additional cycles.

When warm-up cycles are enabled, the warm-up cycles must be initiated at the start of each input or output data burst.

14.5.2.2 Warm-up/Latency Requirements for Pause and Hold Functions

All AC specifications, including REn, input duty-cycle specs (tREH/tRP) for data-out, and DQS input duty-cycle specs (tDQSH/tDQSL) for data-in, must also be met for the warm-up cycles.

If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, issuing additional warm-up cycles is prohibited.

The host should take care to avoid signal integrity issues that could occur due to suspending the data transfer, then resuming without warm-up cycles.

If the host initiates a data hold when warm-up cycles are enabled, then warm-up cycles must be issued at the start of the input or output data burst after the data transfer is resumed.

To initiate a data hold, bring ALE, CLE, or CEn high without latching WEn.

Warm-up cycles are supported only when the DDR2 interface is enabled using Set Features.

Table 78: Hold and Warm-up/Latency Cycle Feature Support

Mode	Operation	# of Warm-up/ Latency Cycles	Hold	Warm-up/ Latency Cycle
Data output	Data-out	0	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 1st DQS rising
		1	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 2nd DQS rising
		2	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 3rd DQS rising
		4	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 5th DQS rising
	Status Read	N/A	DDR2/DDR3/DDR4/DDR5	Not supported
	ID Read		DDR2/DDR3/DDR4/DDR5	Not supported
	Get Features		DDR2/DDR3/DDR4/DDR5	Not supported
Data input	Data-in	0	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 1st DQS rising
		1	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 2nd DQS rising
		2	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 3rd DQS rising
		4	DDR2/DDR3/DDR4/DDR5	DDR2/DDR3/DDR4/DDR5 only: 5th DQS rising
	Set Features	N/A	DDR2/DDR3/DDR4/DDR5	Not supported

Note 1. Suspension + latency can be enabled in modes that support latency.

15 Get Features Operations

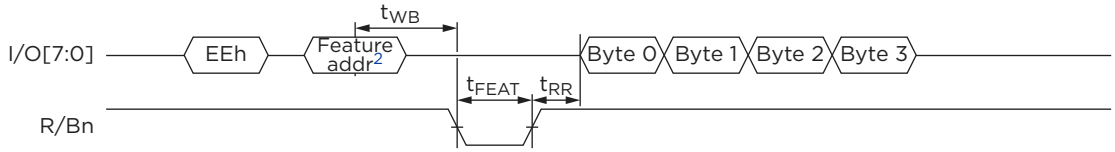
Users can determine target settings using the Get Features command. Issuing the EEh command returns the present settings for the target die. If the host begins to read the first byte of data (the B0 value), it must read all four bytes of data before issuing another command (including Read Status or Read Status Enhanced).

If Read Status (or Read Status Enhanced) is used to monitor whether the tFEAT time is complete, the host must issue a Read command (00h) to read B0, B1, B2, and B3.

Issuing a D4h command followed by the die address initiates a Get Features command to the selected die on a given target (see Figure 93). The EEh command is only accepted when all of the die sharing the same CEn are in the cache-ready or in the true-ready state; the D4h command is only accepted when the selected die is in the cache-ready or in the true-ready state. User-changeable features controlled by the Set Features command and read by the Get Features command are provided in Table 64, "Set Features Addressing (without aIPR)," on page 120 **and** Table 65, "Set Features Addressing (with aIPR)," on page 120.

Caution: Do not toggle DQS/DQSn between the EEh/D4h command and the Feature addresses shown in Figures 92 and 93.

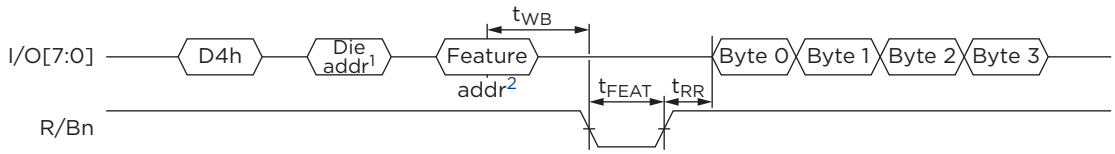
Figure 92: Get Features



Note 1. Only the selected die will output Set Features bytes 0 to byte 3.

2. Feature addresses are provided in Table 64, "Set Features Addressing (without aIPR)," on page 120 **and** Table 65, "Set Features Addressing (with aIPR)," on page 120.

Figure 93: Get Features by Die



Note 1. The die address is one byte (00h = die 0; 01h = die 1...)

2. Feature addresses are provided in Table 64, "Set Features Addressing (without aIPR)," on page 120 **and** Table 65, "Set Features Addressing (with aIPR)," on page 120,

3. In a multi-die package, after D4h has been initiated on a given die, initiating operations on any other die sharing the same CEn is prohibited until all feature bytes are read out.

16 ZQ Calibration

As process, voltage, and temperatures vary in operation, drive strength impedance values will also vary. For applications running at speeds higher than 400 MHz using the CTT interface, SanDisk recommends (but does not require) the use of the ZQ calibration features in this device.

ZQ Calibration addresses drive strength impedance variations, without altering ODT. It also helps maintain signal integrity as bus speeds on the NAND Flash interface continue to increase and make off-chip driver (OCD) adjustments necessary.

ZQ calibration is required for LTT operation at all frequencies.

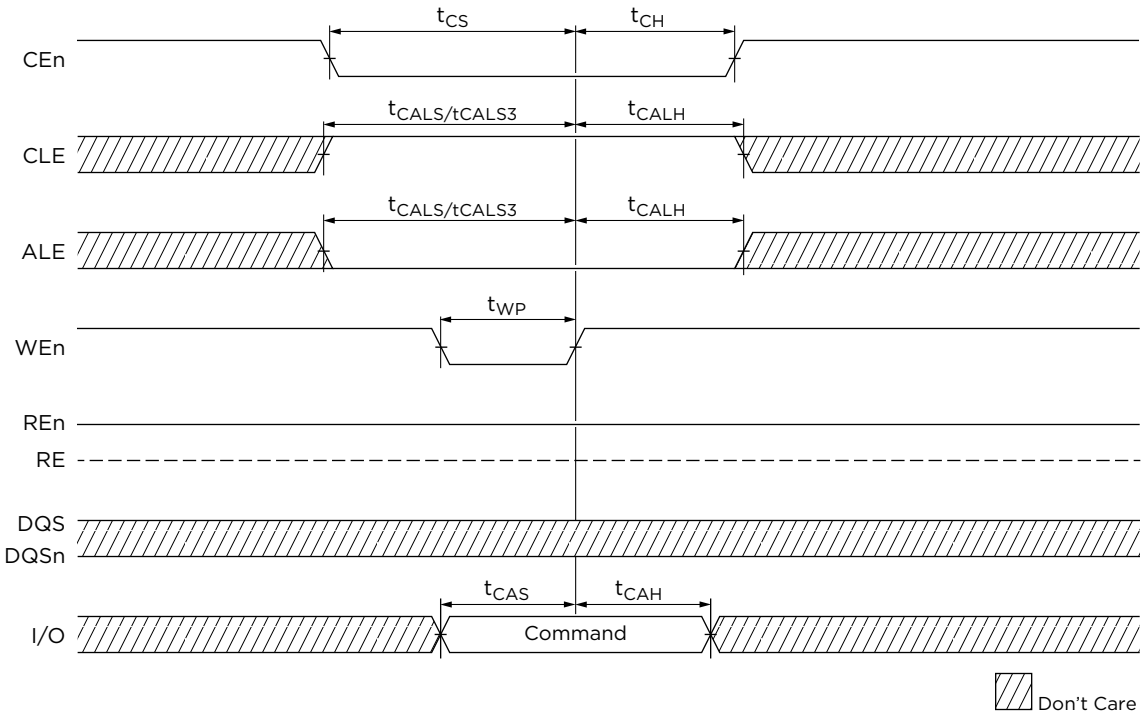
For additional information on ZQ calibration, please contact your representative for the relevant Applications Note(s).

16.1 DCC Concept

For information on Duty Cycle Correction (DCC), please contact your representative for the concept and requirements Applications Note(s).

17 Toggle Mode Timing Diagrams

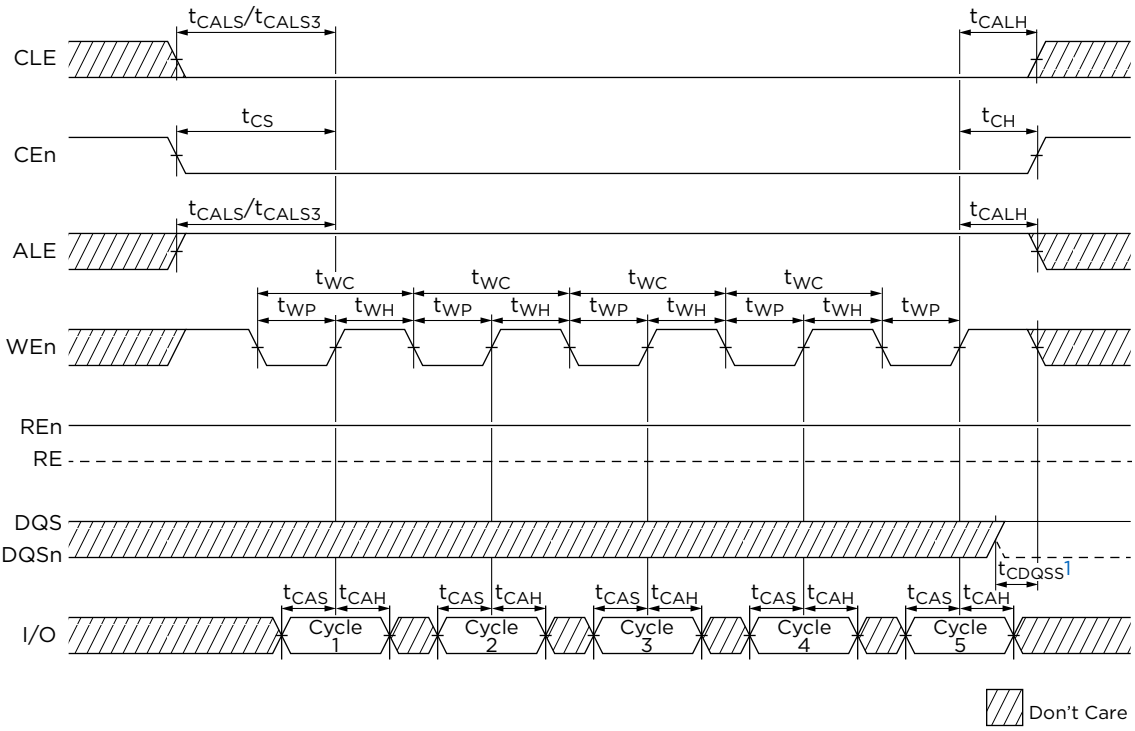
Figure 94: Toggle Mode Command Input Cycle



Note 1. Command information is latched by WEn going high when CEn and ALE are low and CLE is high.

2. DQS should be set to low when the 85h, 10h, or 11h commands are input.

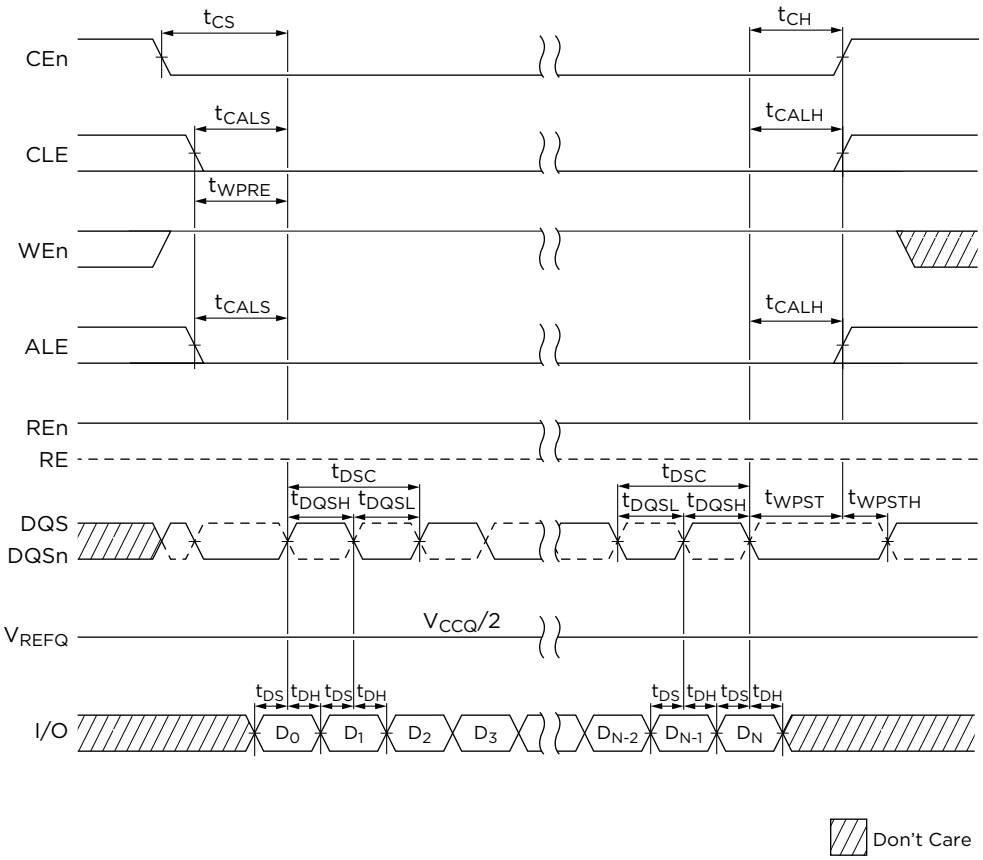
Figure 95: Toggle Mode Address Input Cycle



Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

Figure 96: Toggle Mode Data Input Cycle

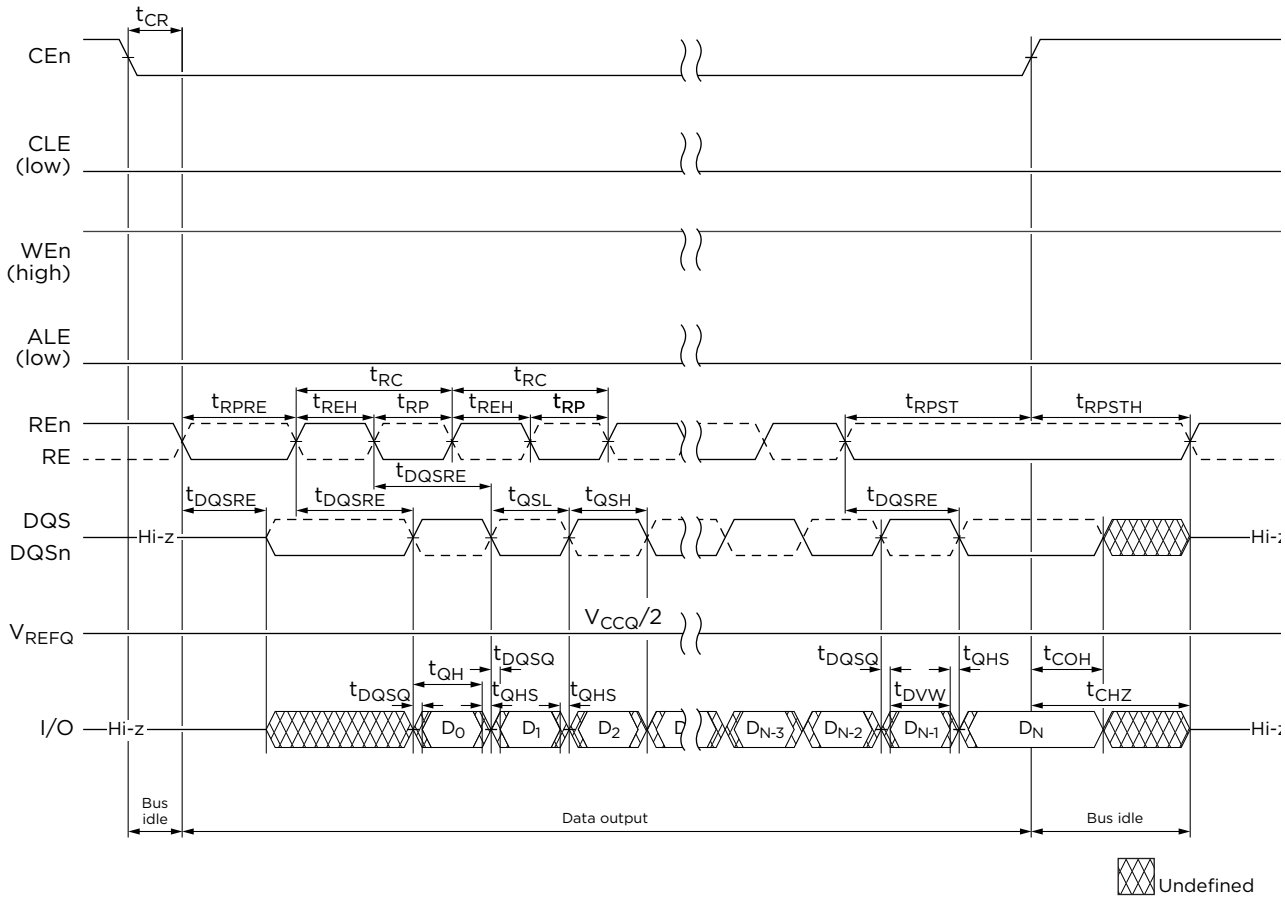


Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Note 1. DQS, DQSn, and data input buffers are turned on when CEn and DQS go low, and data inputs begin with DQS and DQSn toggling simultaneously.

2. ALE and CLE should not toggle during tWPRE, regardless of tCALS.
3. DQS and data input buffers are turned off if either CLE or CEn go high.
4. The least significant bit of the column address must always be zero.
5. DQS and DQSn must be either high or low before the data-input condition is set.
6. When ODT is disabled, use tCS, tCALS, or tWPRE. When ODT is enabled, use tCS2, tCALS2, or tWPRE2.
7. ALE, CEn, and CLE must not toggle during tWPST.

Figure 97: Toggle Mode Data Output Cycle



Note 1. DQS, DQSn, and I/O drivers are turned on when CEn and REn go low for data output operations.
2. ALE and CLE must not toggle during tRPRE, regardless of tCALS.
3. DQS and I/O drivers go from valid to High-Z if either CLE or CEn goes high.
4. The least significant bit of the column address must always be zero.

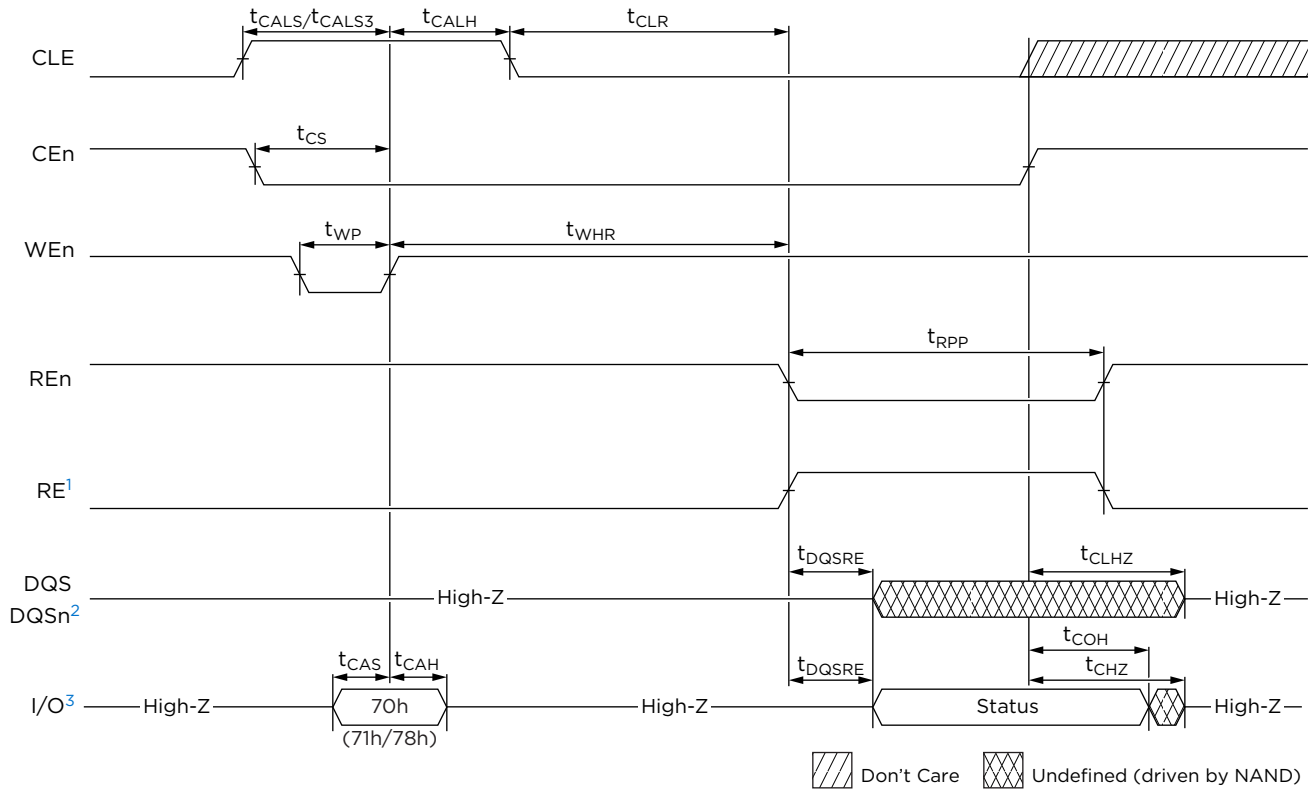
DRAFT Rev. 0.1 7/20/22

17.1 Status Reads

For single-byte reads in Toggle Mode, the recommended approach is to use REn/RE to read status bytes from NAND on the controller, rather than using the DQS/DQSn strobe. ODT is not supported during status read operation.

Caution: User must guarantee signal integrity of REn/RE if using DQS/DQSn strobe to read status bytes from NAND.

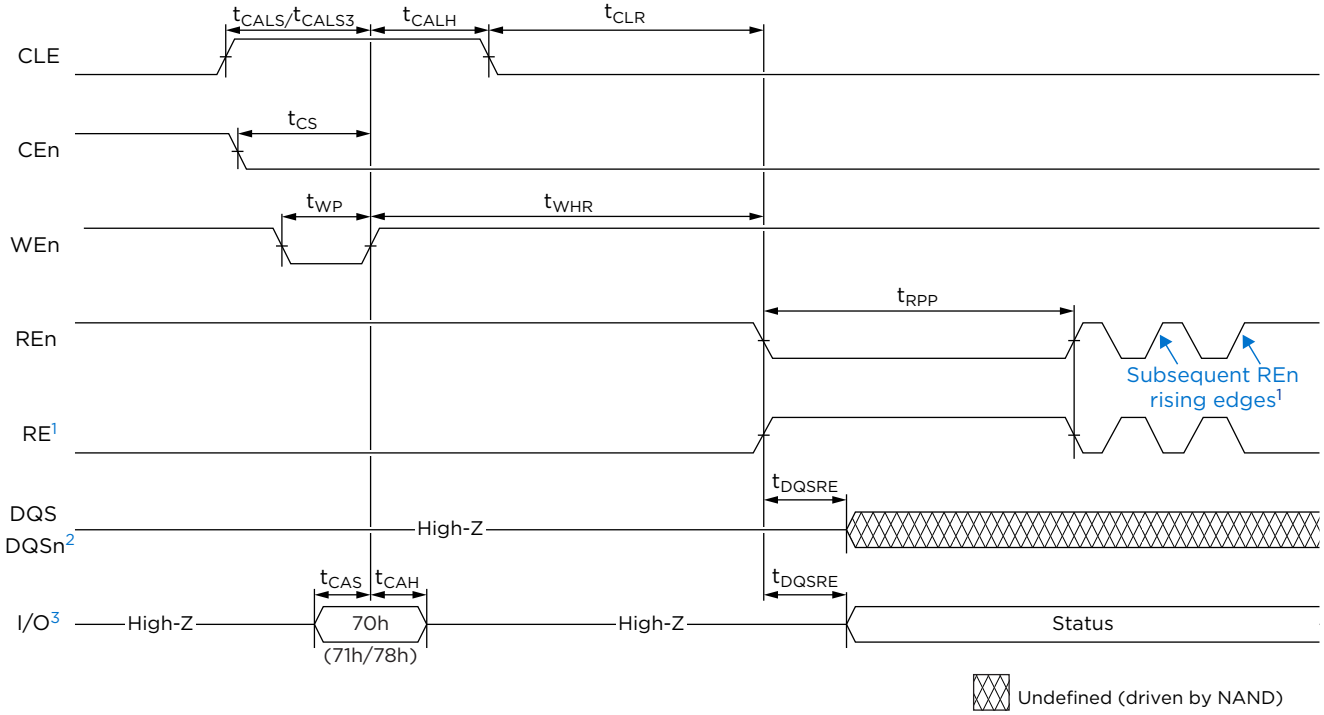
Figure 98: Toggle Mode Status Read Cycle



Note 1. REn can toggle more than one time. If additional REn/RE toggles are desired, see Figure 99, "Toggle Mode Status Read Cycle with Multiple REn/RE Toggles," on page 141.

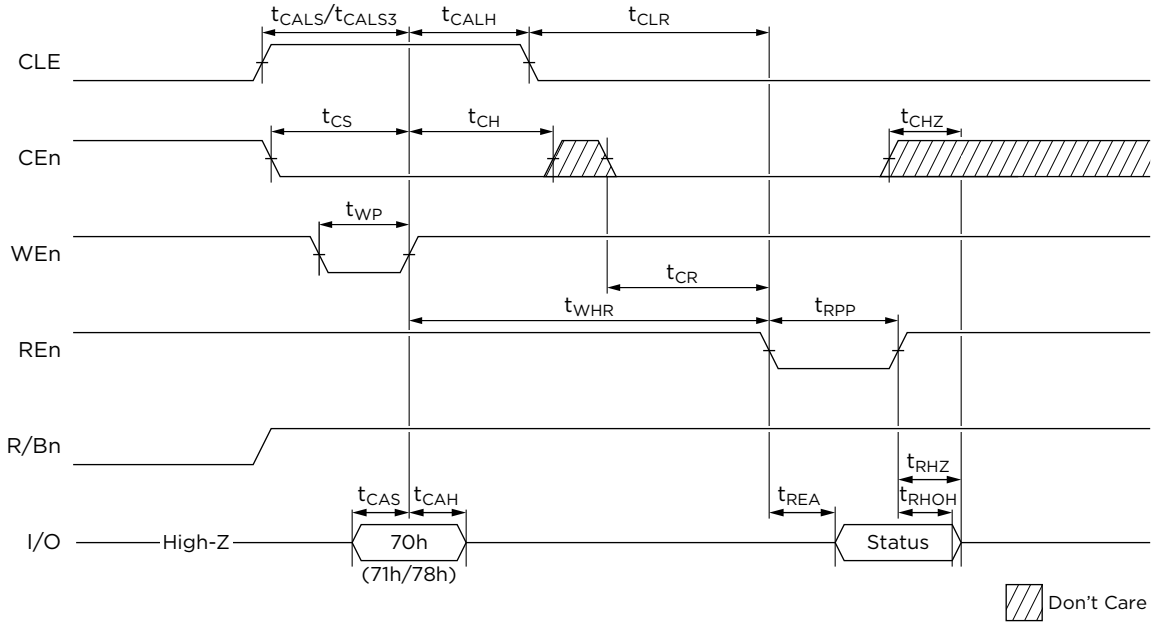
2. DQS and data output buffers go from valid to High-Z when CEn or CLE goes high.
3. Although toggle-mode NAND uses both the rising and falling edges of DQS for Reads, the Status Read operation repeats the same output until the device status changes.
   The device status can change asynchronously. If the status shows busy, the user can continue toggling REn to poll the device status until the status changes to ready.
4. The Read Status Enhanced command (78h) requires row-address-setting steps prior to reading the status value. This is not depicted in the figure.

Figure 99: Toggle Mode Status Read Cycle with Multiple REn/RE Toggles



Note 1. Following tRPP, subsequent REn rising edges can be used to sample status.

Figure 100: Status Read Cycle at Power-On, Prior to Toggle Mode Enable



Note 1. The Read Status Enhanced command (78h) requires row-address-setting steps prior to reading the status value. This is not depicted in the figure.

17.2 Read ID Use Guidelines

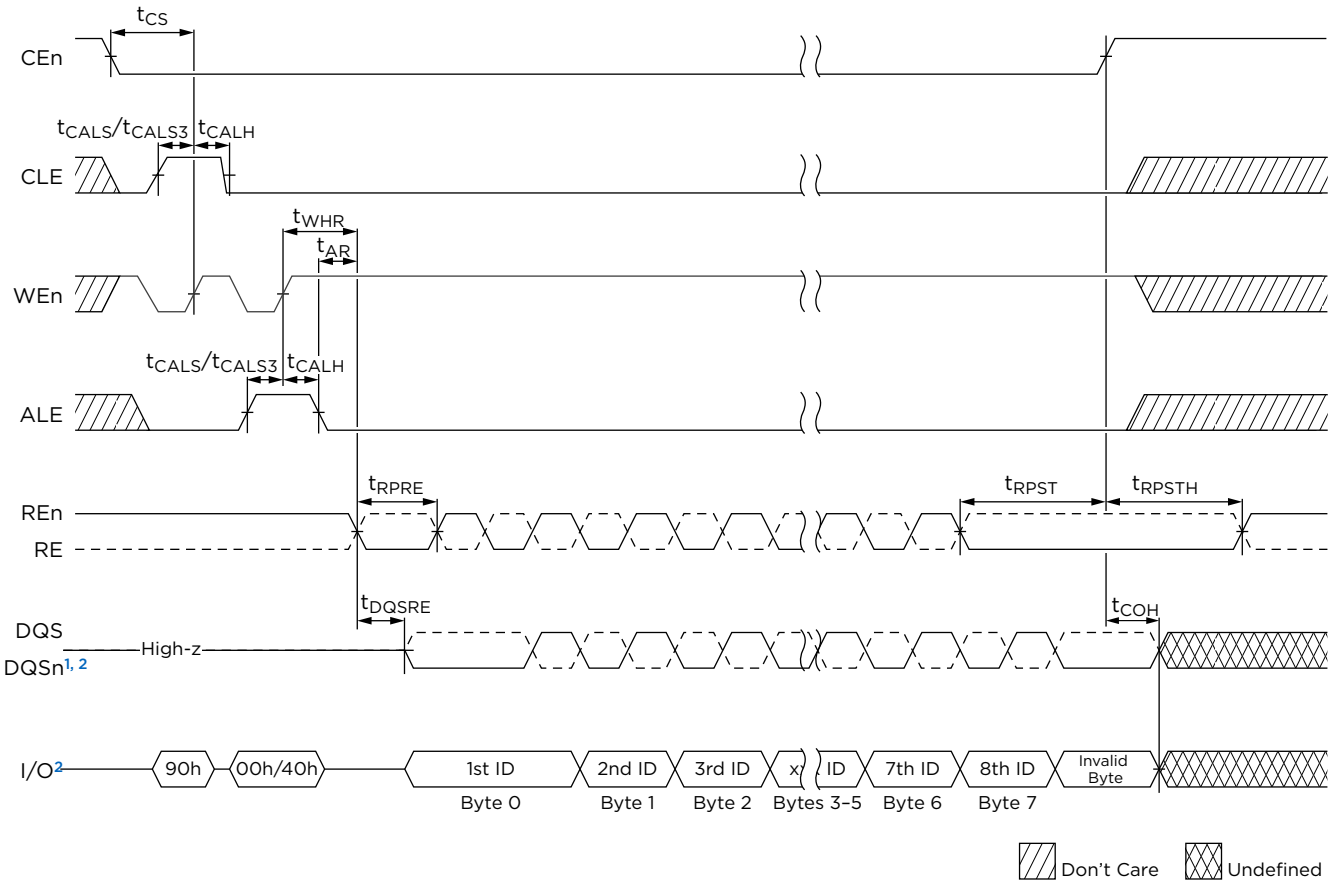
Before transitioning to high-speed operations, initiate Read ID(s) using the pre-initialization timing specifications, with tRC = 30ns.

Read ID bytes are transmitted in SDR fashion (one byte for every DQS/DQSn cycle, rather than two-byte DDR mode), and the DQS rising edge can be used to strobe the ID bytes.

ODT does not turn on for all data transactions; Read ID, Status Read, and single-byte Reads are not supported. See Table 55, "ODT Turn-On Mode Support," on page 76 for ODT turn-on availability.

Because ODT does not turn on during Read ID operation, using a slow speed is recommended for Read ID.

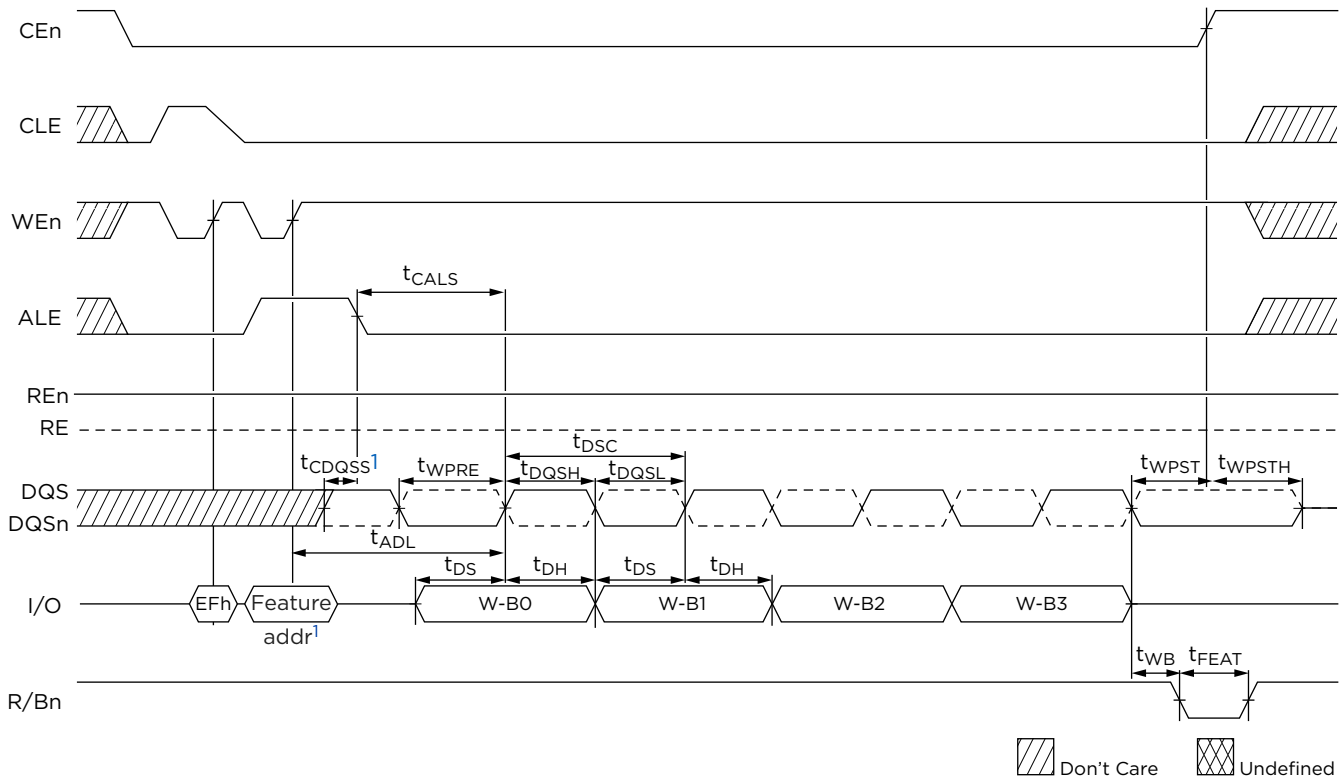
Figure 101: Toggle Mode Read ID



Note 1. DQS and I/O drivers change from valid to High-Z when CEn or CLE goes high.

2. Address 00h is for SanDisk legacy devices; 40h is for new JEDEC ID information.

Figure 102: Toggle Mode Set Features

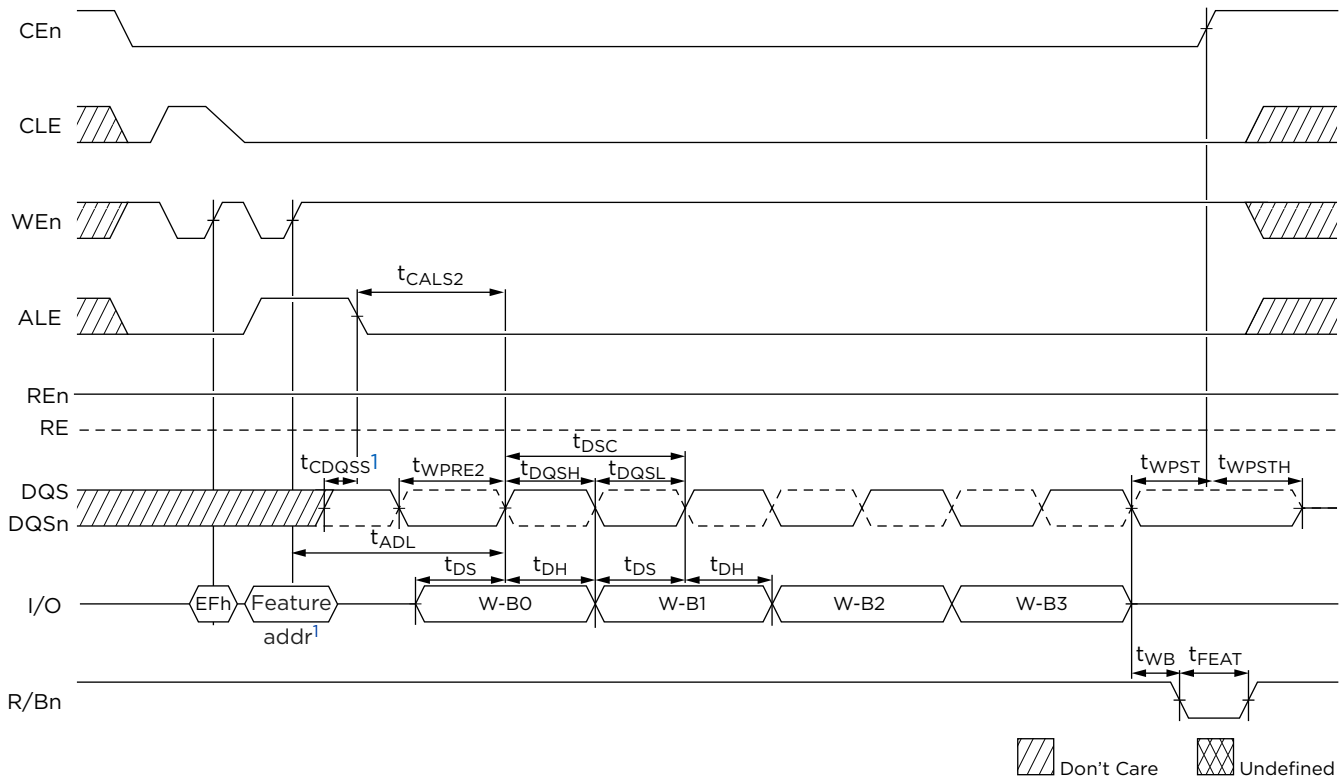


Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

2. W-B[3:0] are parameter values that identify new settings for the specified feature.

Figure 103: Toggle Mode Set Features with ODT



Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

2. B[3:0] are parameters that identify new settings for the specified feature.

Figure 104: Toggle Mode Get Features

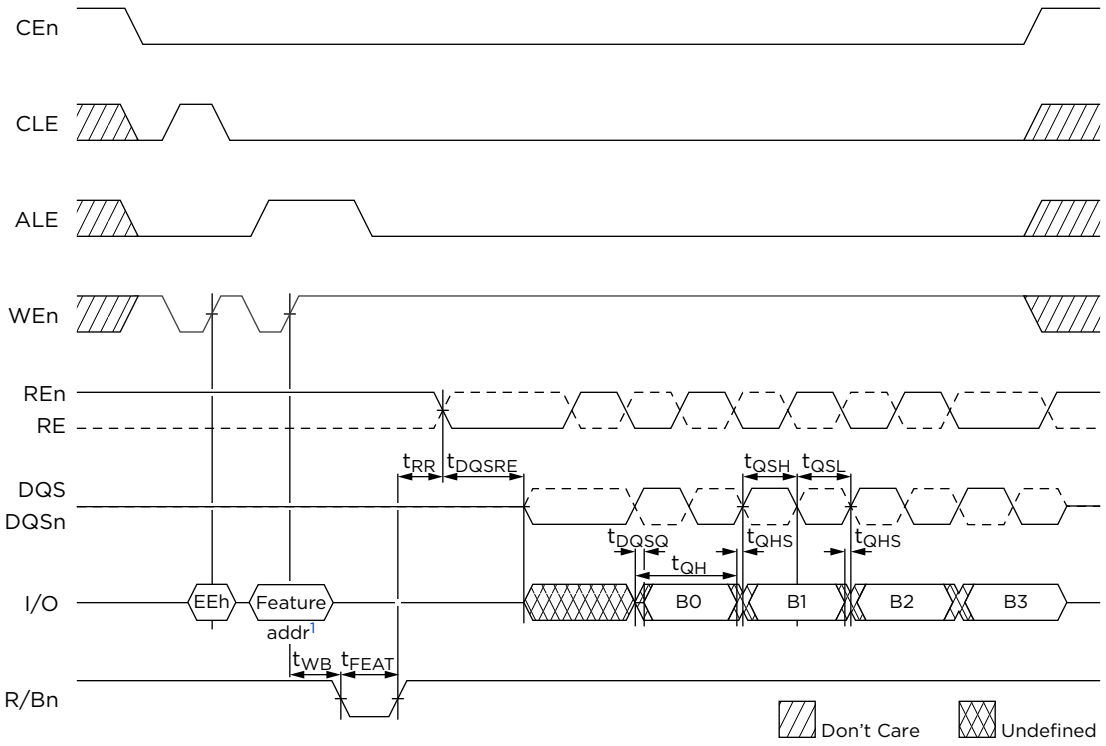


Figure 105: Toggle Mode Page Read

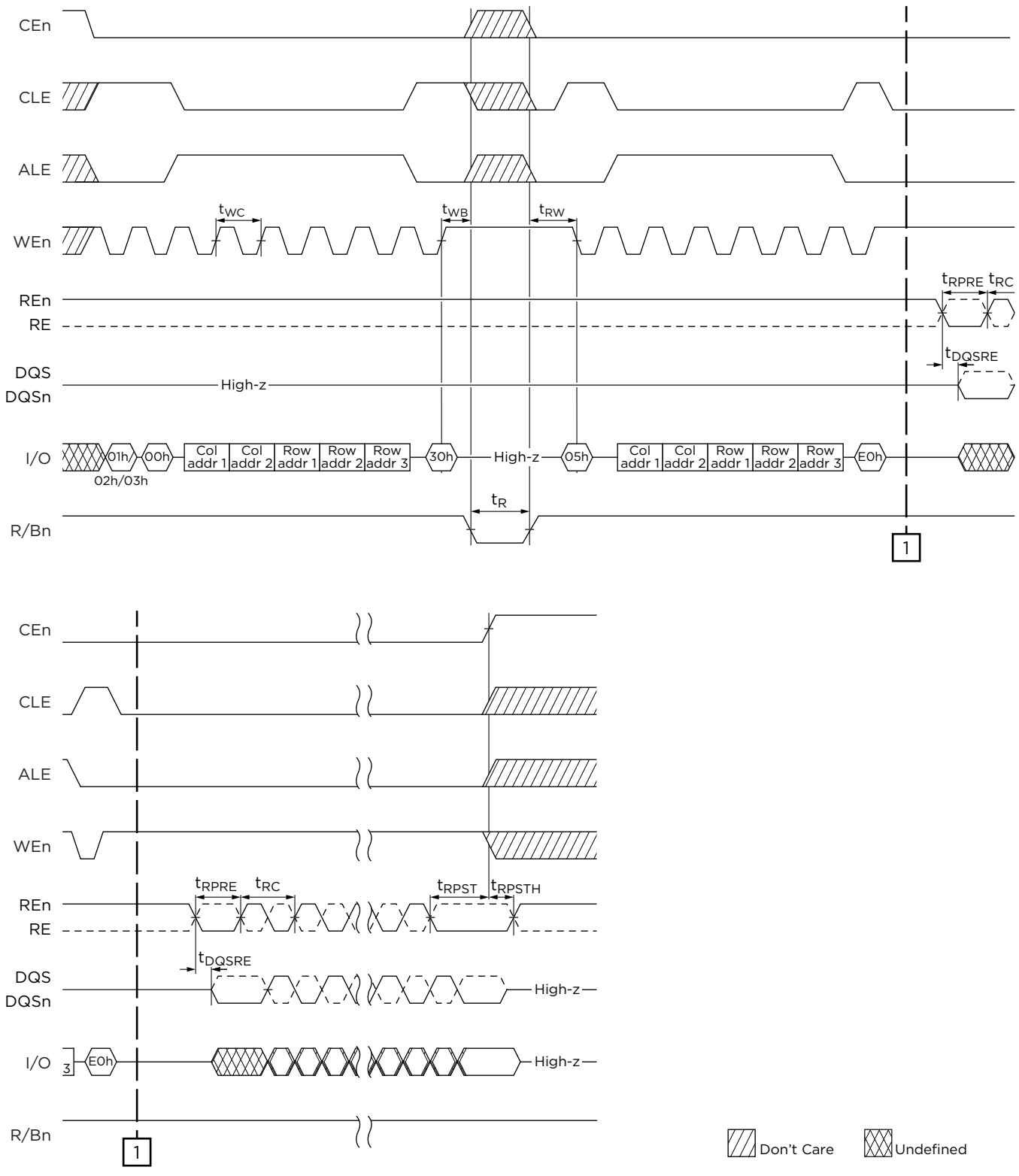


Figure 106: Toggle Mode Single-Plane Program: First Cycle

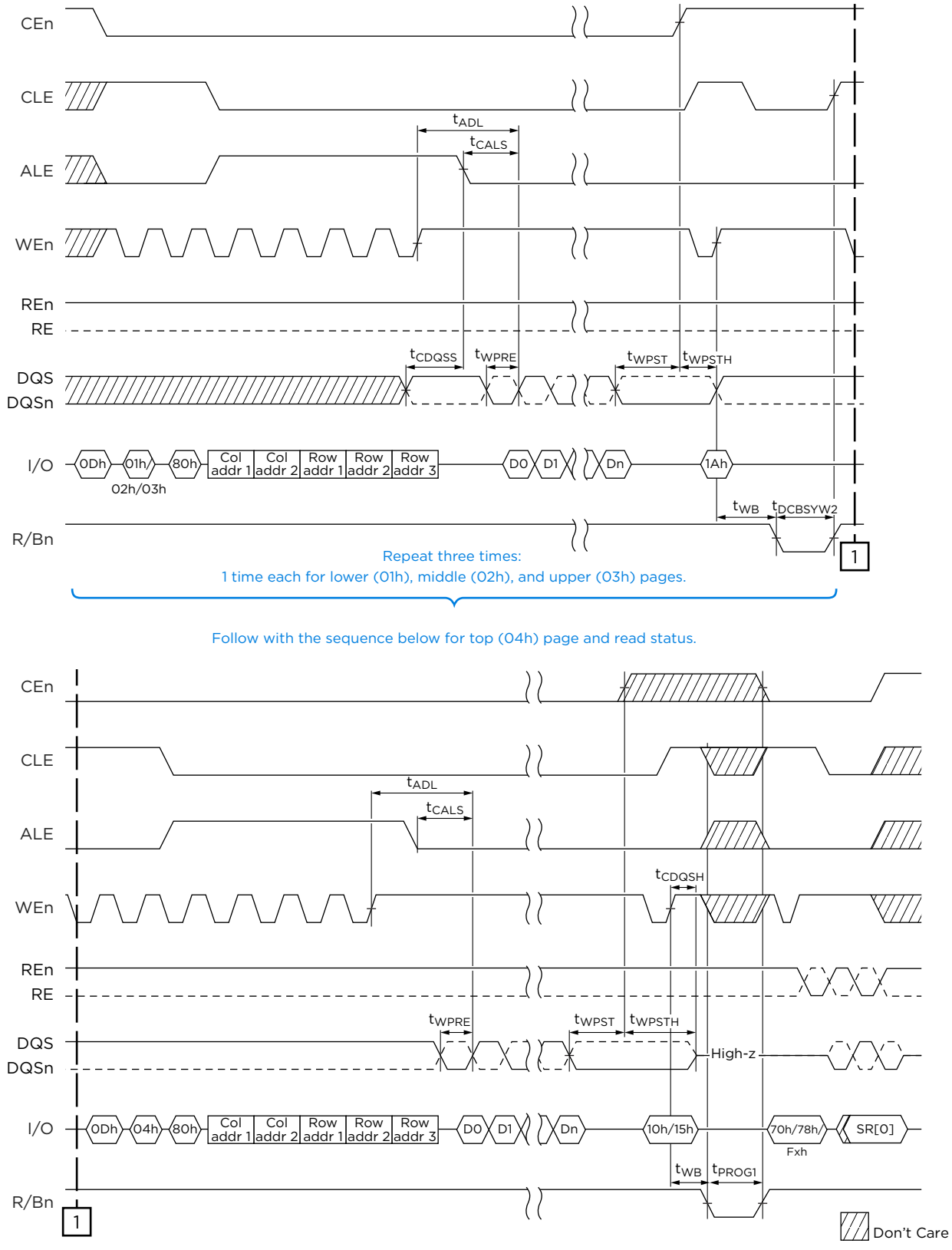


Figure 107: Toggle Mode Single-Plane Program: Second Cycle

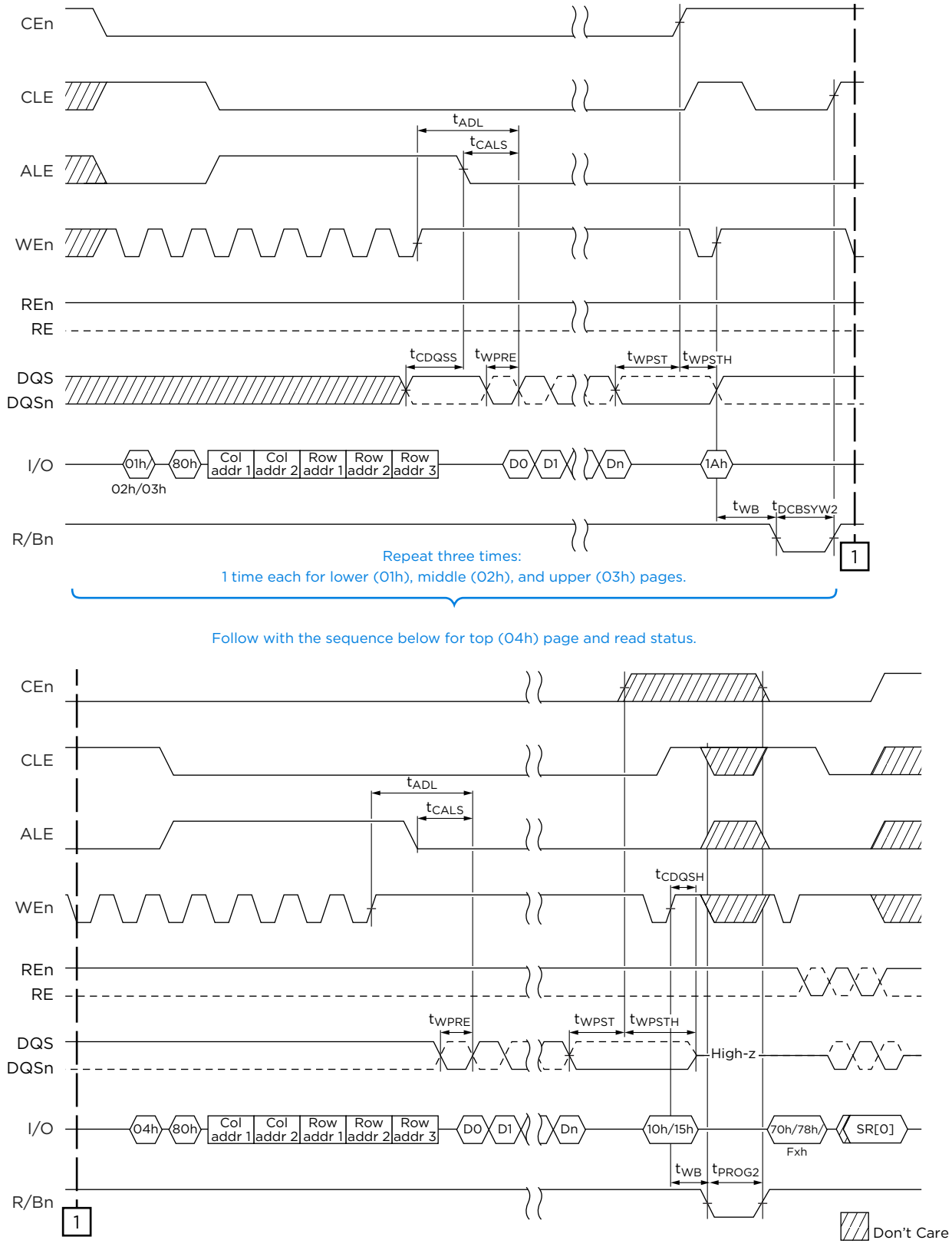
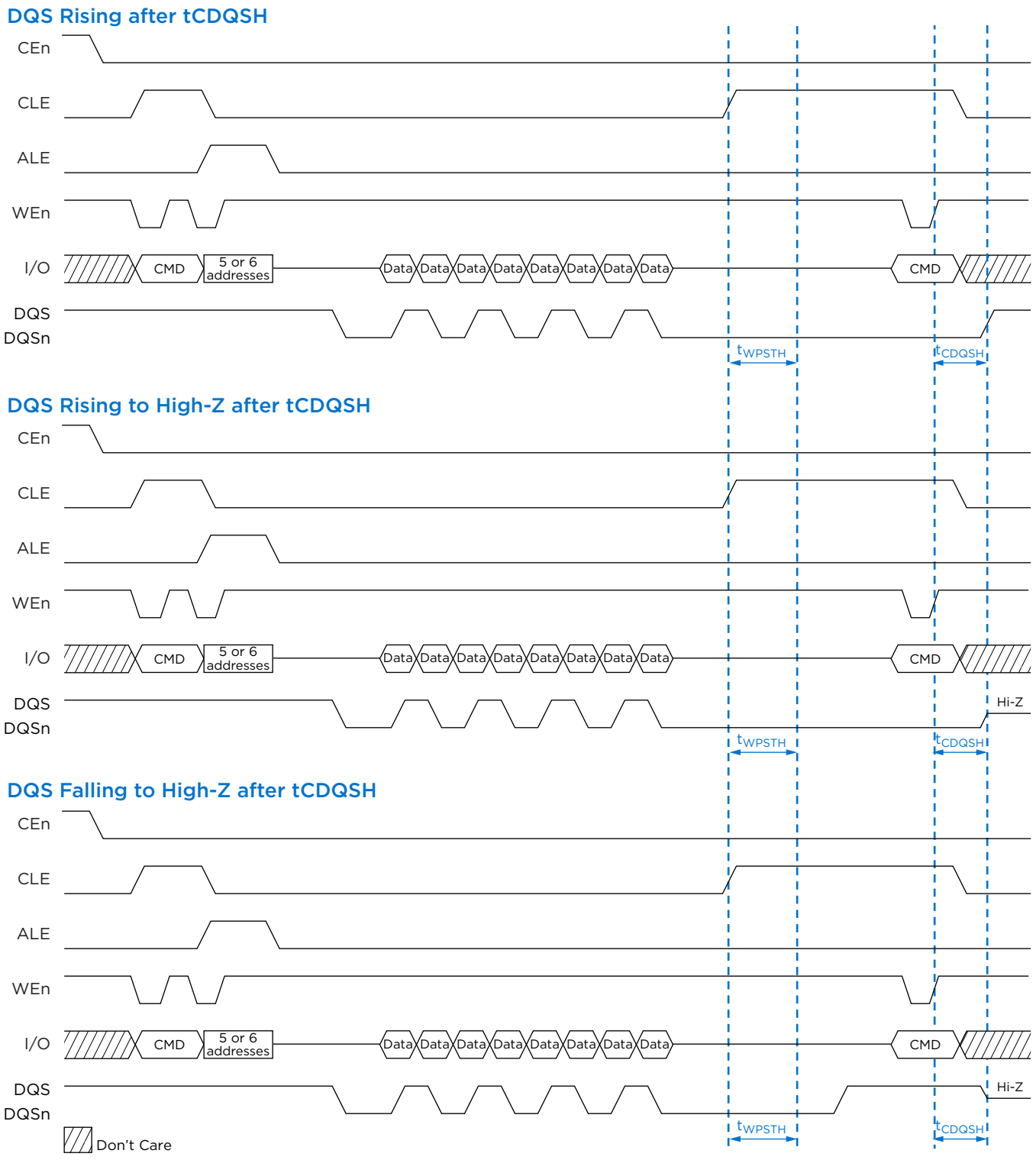
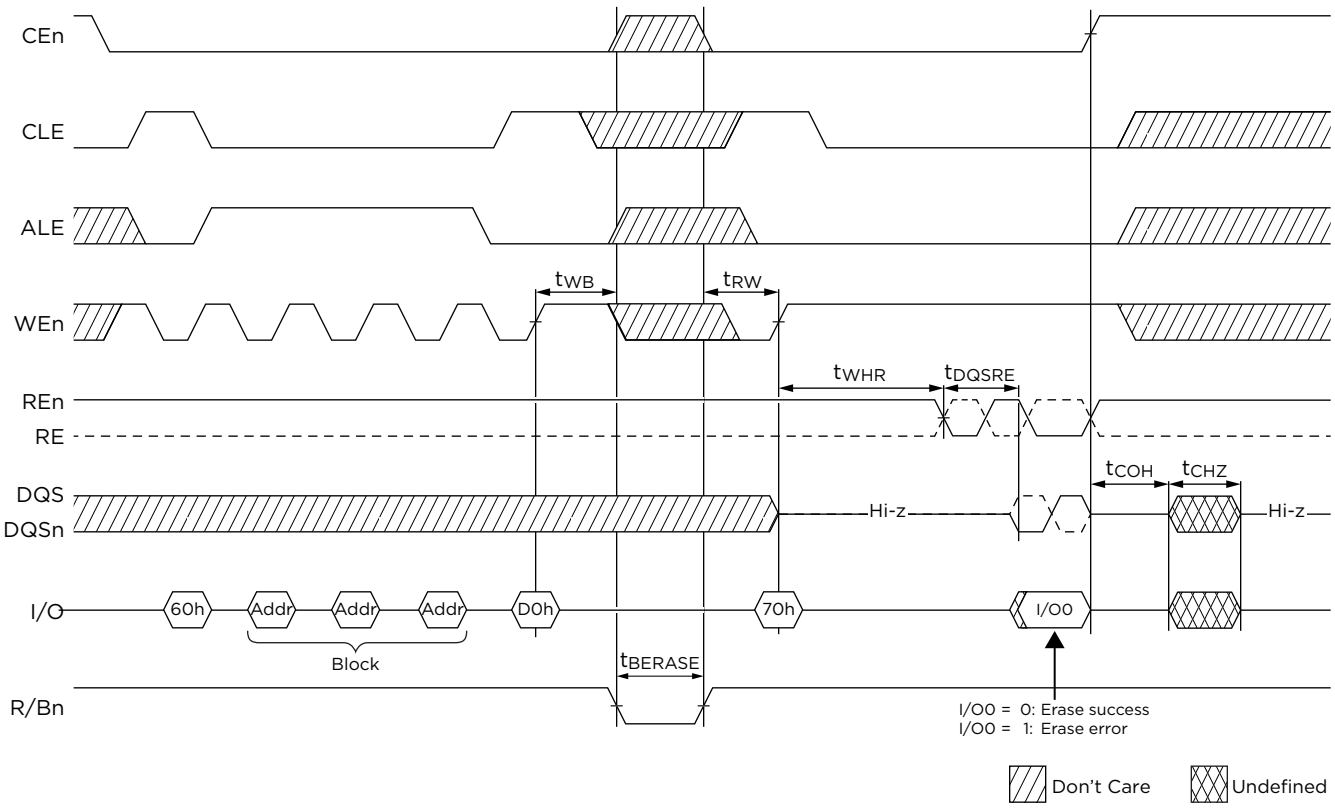


Figure 108: tCDQSH Definition



Note 1. DQS and DQSn will be driven high, low, or to Hi-z after a delay of tCDQSH from the rising edge of WEn to ensure that D_{IN} has terminated.

Figure 109: Toggle Mode Single-Plane Block Erase



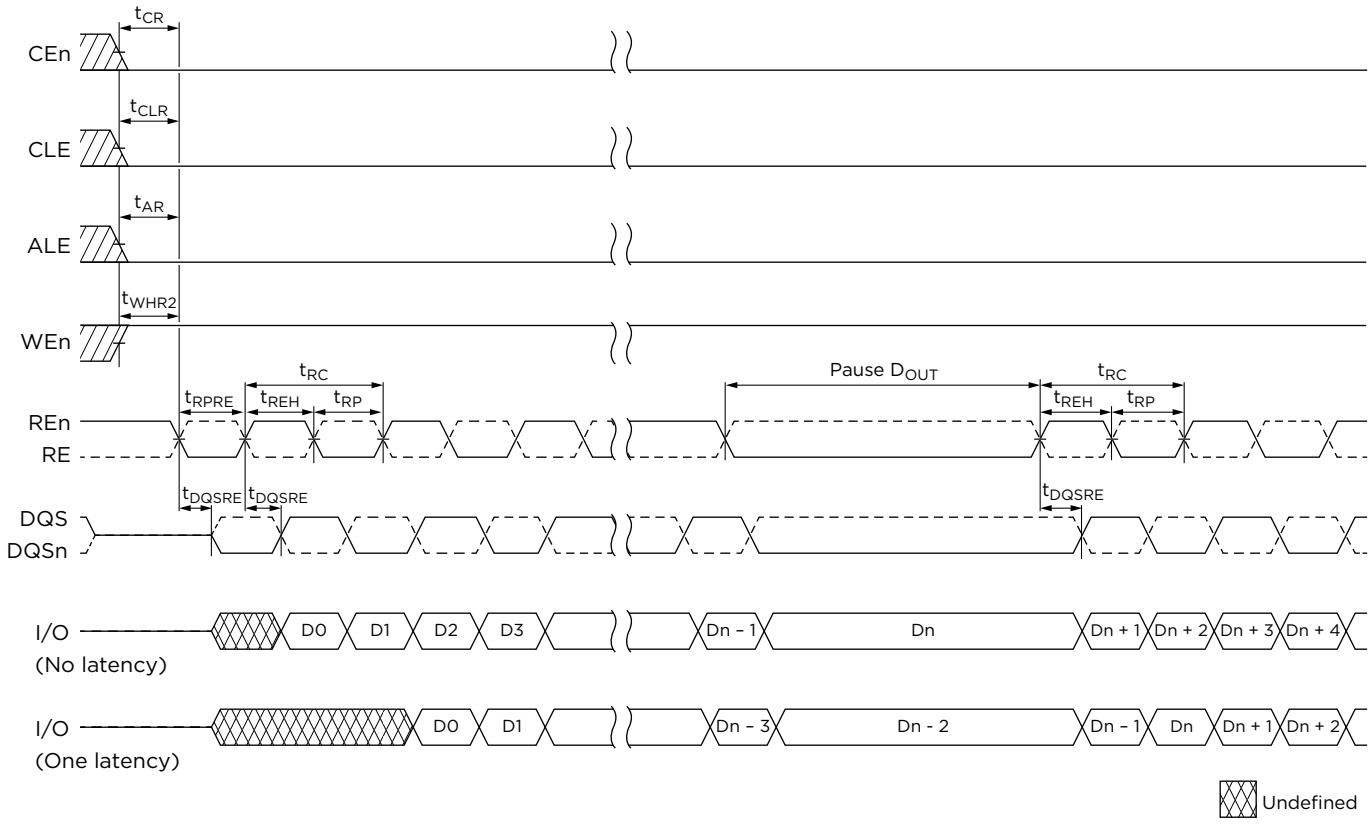
17.3 Pause and Hold Options During Data-out and Data-in

17.3.1 Data-out Pause

When using data-out pause, take into account the following:

- The host can pause data output by entering the idle state.
- To pause data output, place the bus in the idle state by pausing REn (RE) and holding the signal(s) static high or low until the data burst is resumed.
- WEn must be held high and ALE, CLE, and CEn must be low during data-output-burst pause time.
- ODT (if enabled) stays ON during the entire pause time, and Latency/warm-up cycles (if enabled) are not re-issued when restarting a data burst from pause.
- The host must exit the data burst to disable ODT or re-issue warm-up/latency cycles when restarting. If warm-up/latency cycles are required, refer to"Table 66, "Feature Address 02h," on page 121" for details on re-issuing warm-up cycles when exiting and re-starting data bursts.

Figure 110: D_{OUT} Pause

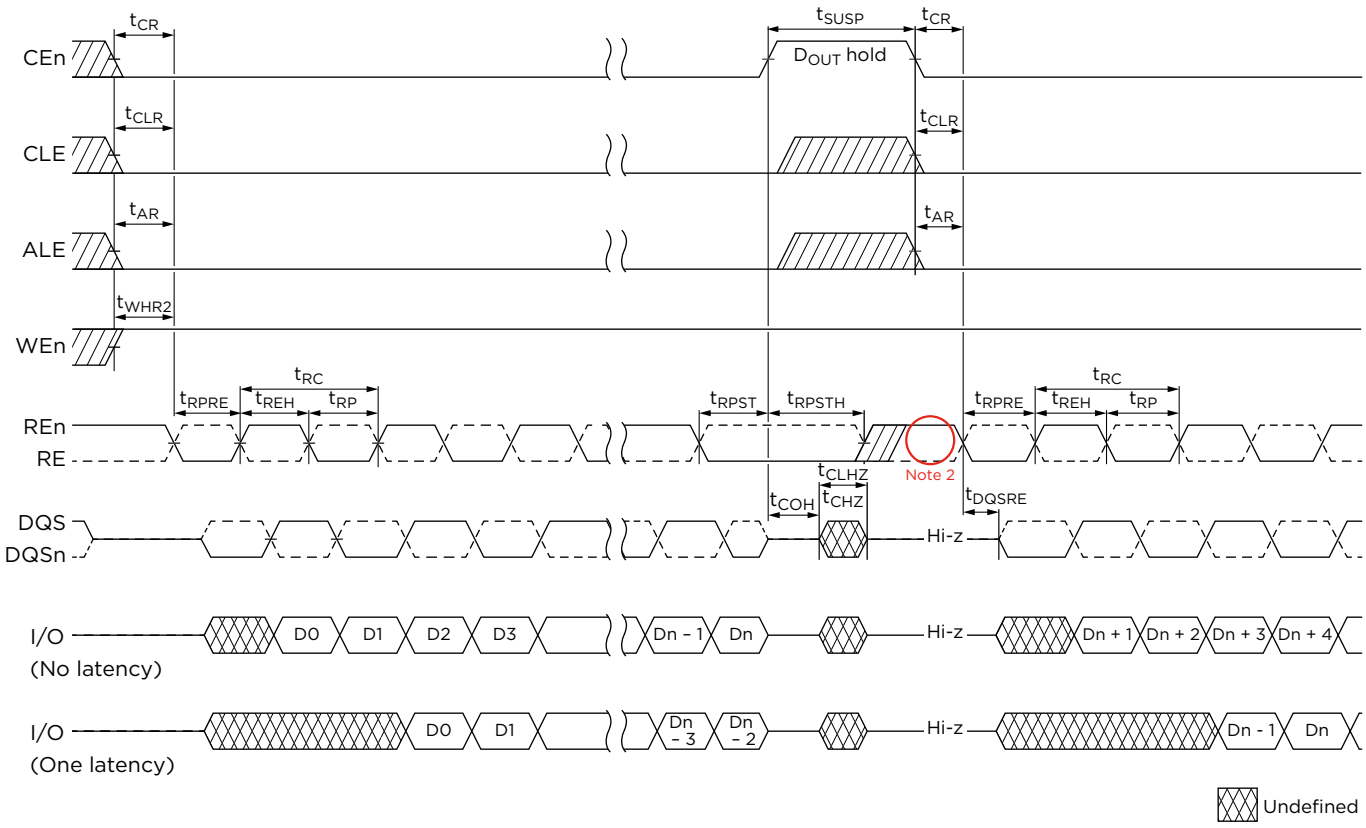


17.3.2 Data-out Hold

Data-out hold is only supported in Toggle Mode. Data-out can be suspended by any one of the following:

- CEn signal going high
- CLE signal going high
- ALE signal going high

Figure 111: D_{OUT} Hold



Note 1. Data-out can also be suspended by driving REn low after each even byte. Take care to eliminate noise on the REn line, because noise may have an adverse effect on data-out operation.

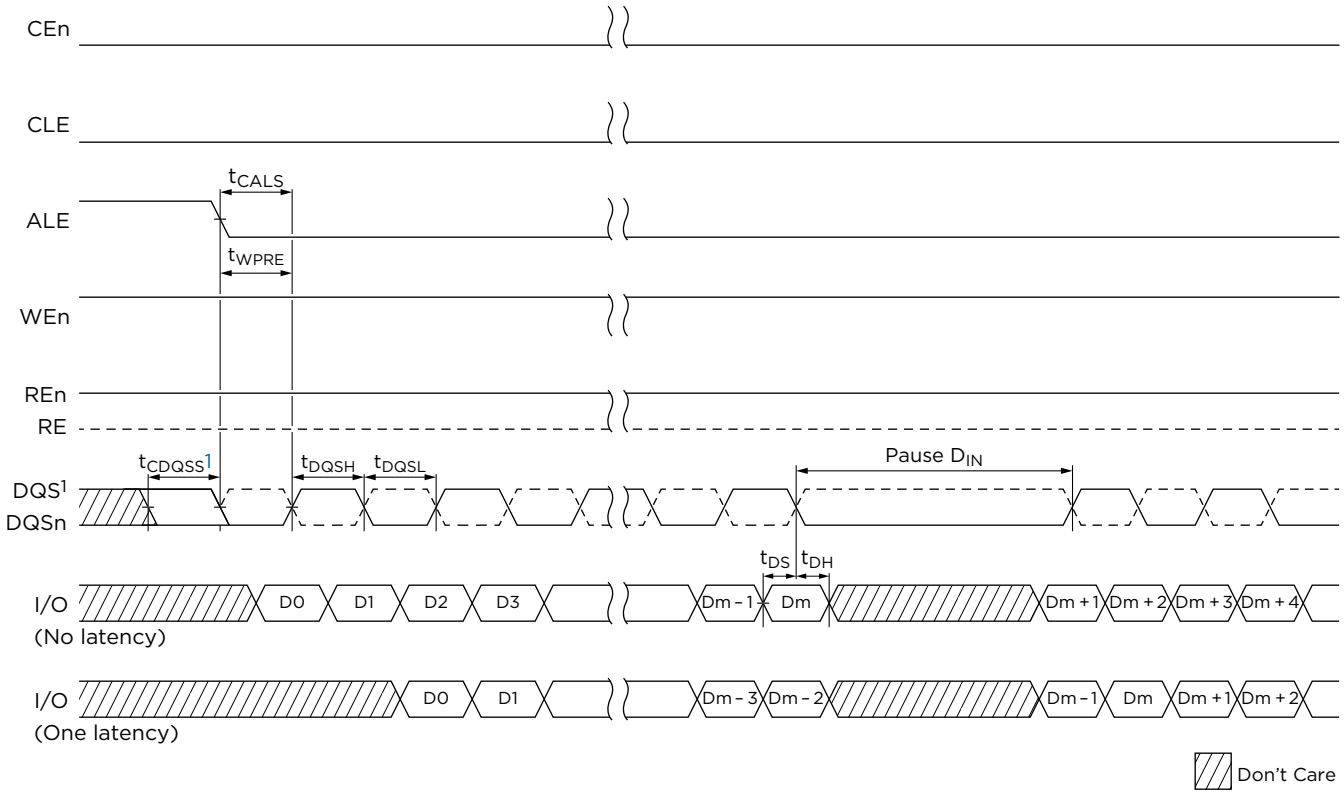
2. REn must be high before resuming D_{OUT} execution.

17.3.3 Data-in Pause

When using data-in pause, take into account the following:

- The host can pause data input by entering the idle state.
- To pause data input, place the bus in the idle state by pausing DQS (DQSn) and holding the signal(s) static high or low until the data burst is resumed.
- WEn and REn (RE) must be held high and ALE, CLE, and CEn must be low during data-input-burst pause time.
- ODT (if enabled) stays ON during the entire pause time, and Latency/warm-up cycles (if enabled), are not re-issued when re-starting a data burst from pause.
- The host must exit the data burst to disable ODT or re-issue warm-up/latency cycles when restarting. If warm-up/latency cycles are required, refer to "Table 14.1, "Toggle Mode-Specific Setting (02h)," on page 121" for details on re-issuing warm-up cycles when exiting and re-starting data bursts.

Figure 112: D_{IN} Pause



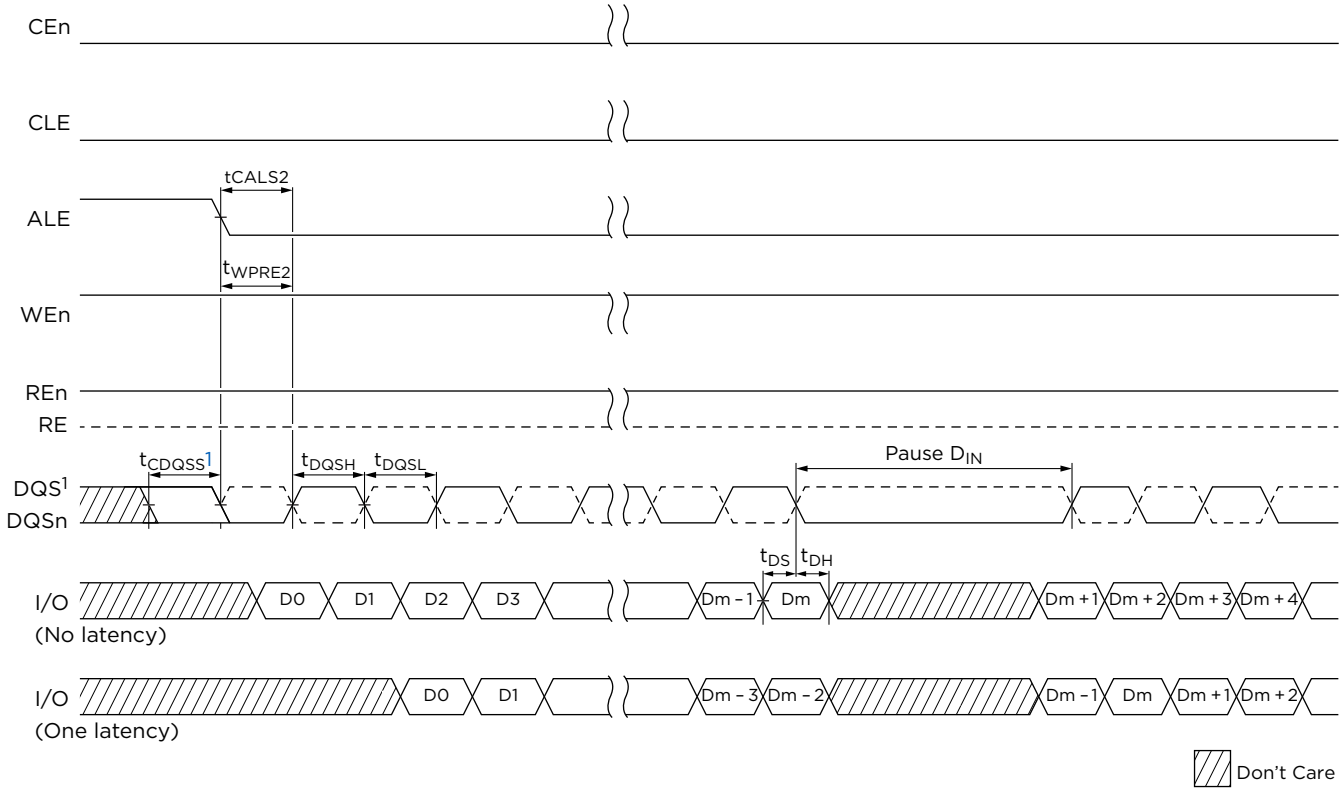
Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in

sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

Figure 113: D_{IN} Pause with ODT



Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

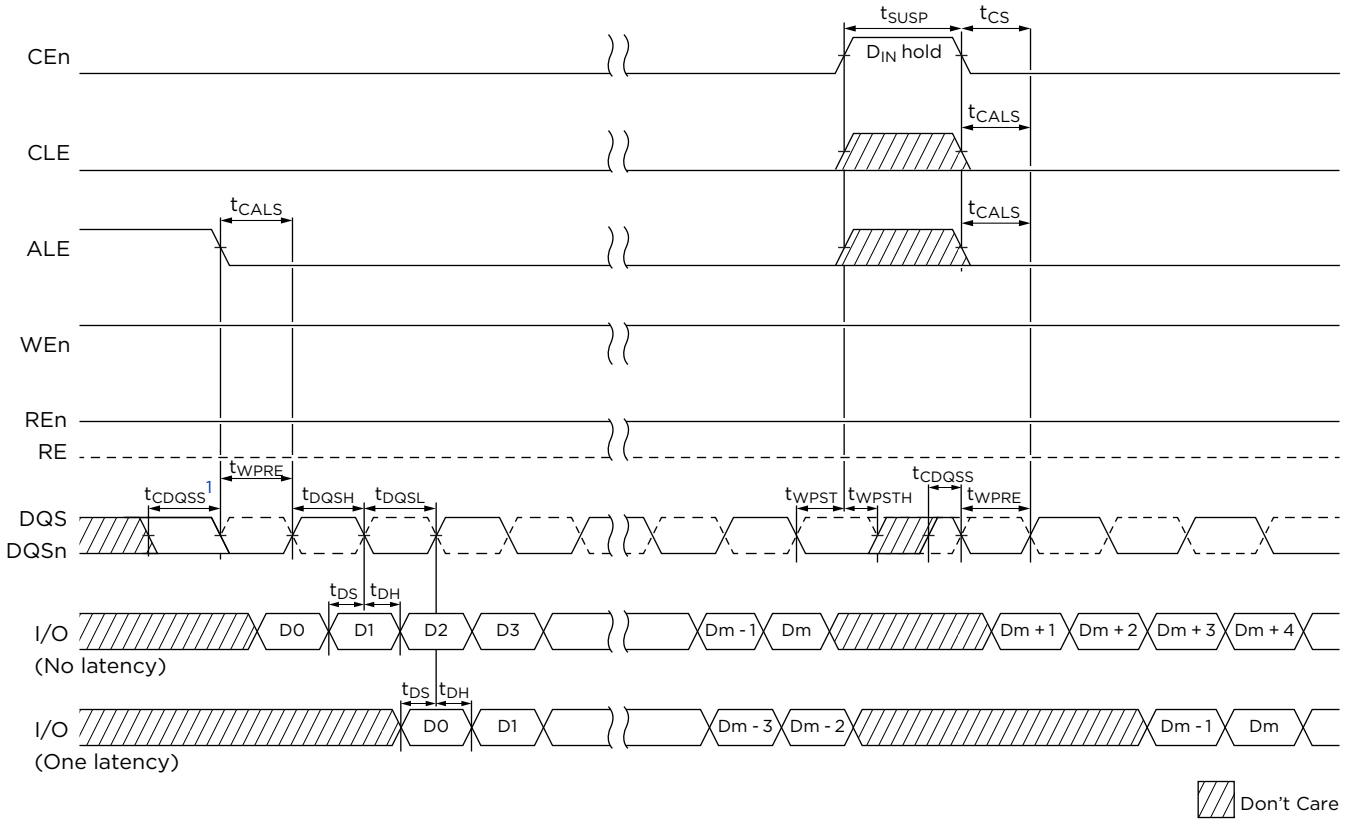
There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

17.3.4 Data-in Hold

Data-in can be suspended using any one of the following:

- CEn signal going high
- CLE signal going high
- ALE signal going high

Figure 114: D_{IN} Hold with DQS Toggle



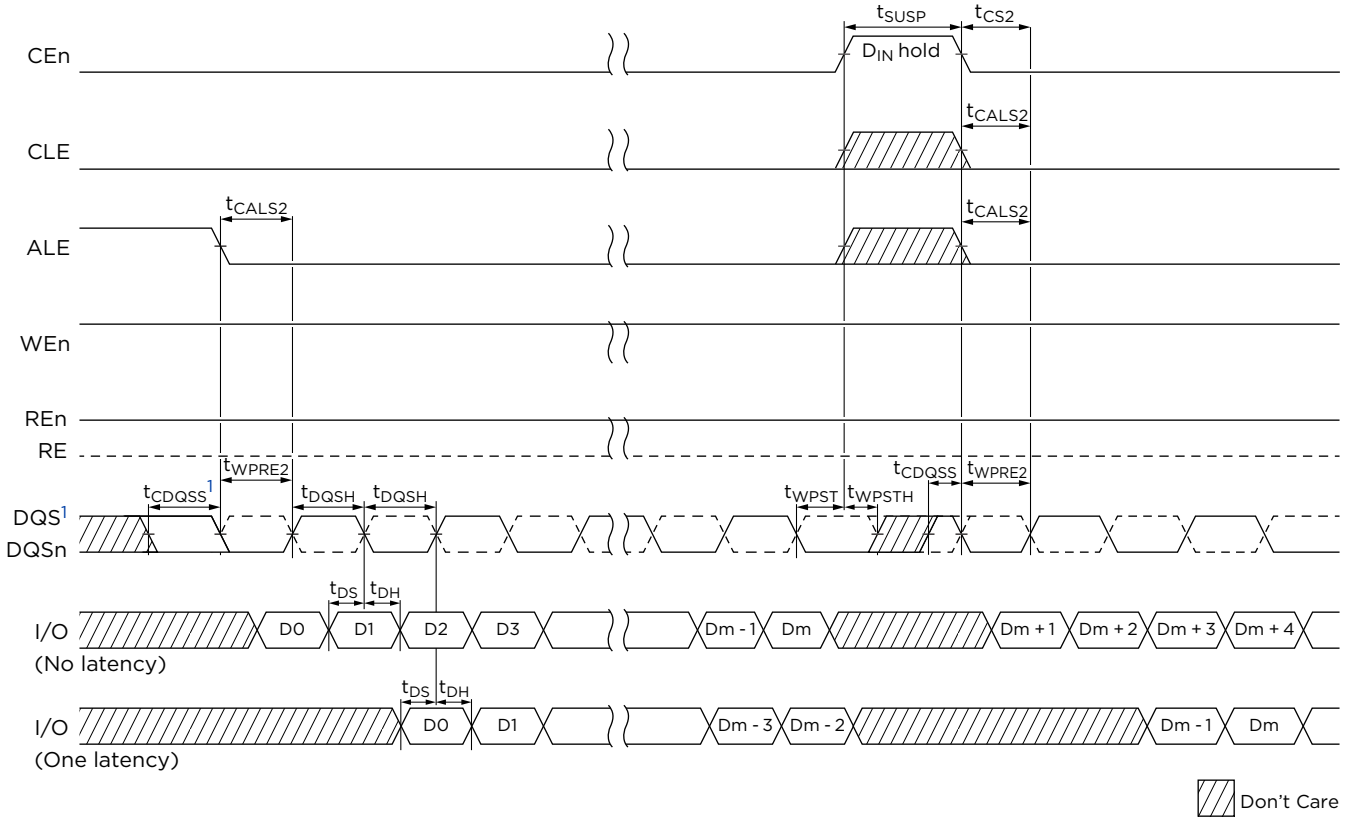
Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

2. During data-in suspension, DQS can toggle or remain low; during data-out, REn must go high before the operation resumes.
3. Data-out can also be suspended by driving DQS low after each even byte. Take care to eliminate noise on the DQS line, because noise could have an adverse effect on data-out operation.

Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Figure 115: D_{IN} Hold with DQS Toggle, with ODT



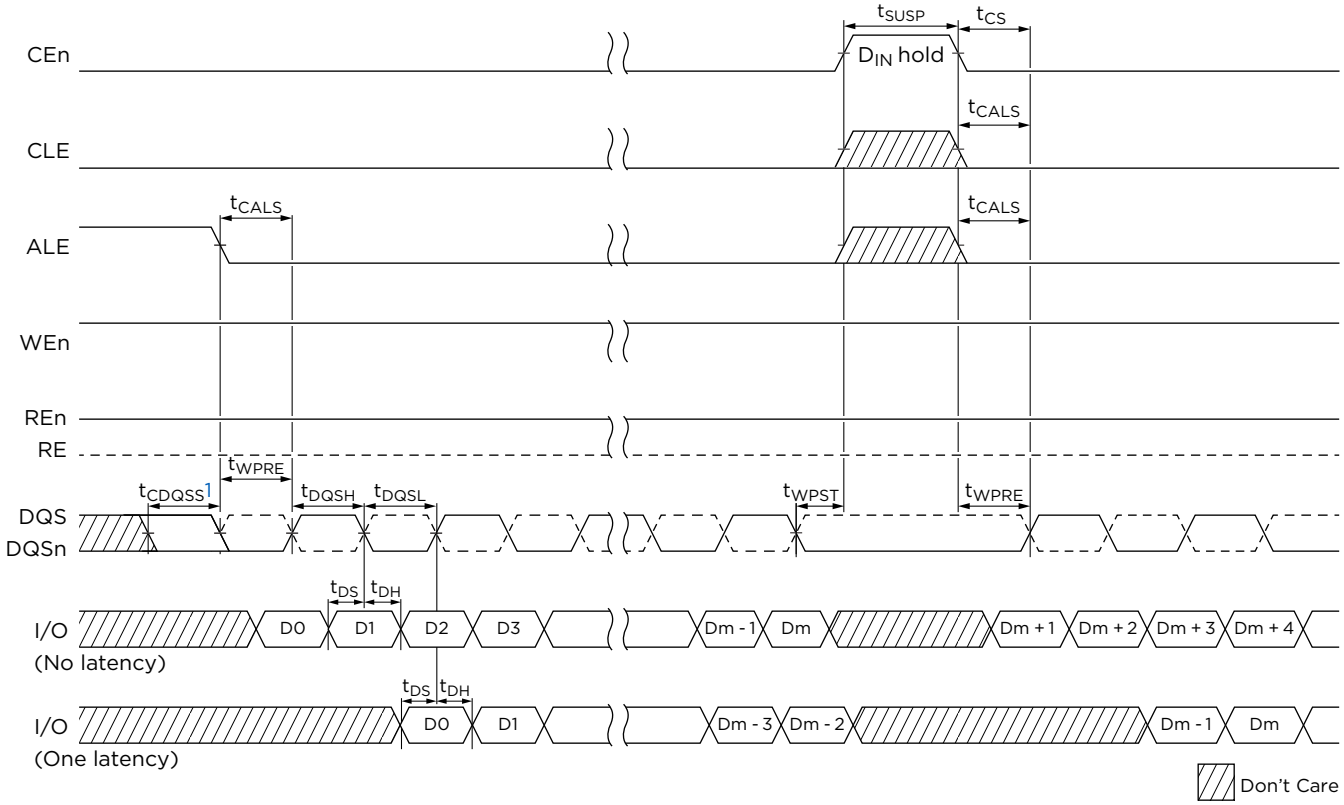
Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

2. During data-in suspension, DQS can toggle or remain low; during data-out, REn must go high before the operation resumes.
3. Data-out can also be suspended by driving DQS low after each even byte. Take care to eliminate noise on the DQS line, because noise could have an adverse effect on data-out operation.

Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Figure 116: D_{IN} Hold with DQS Low

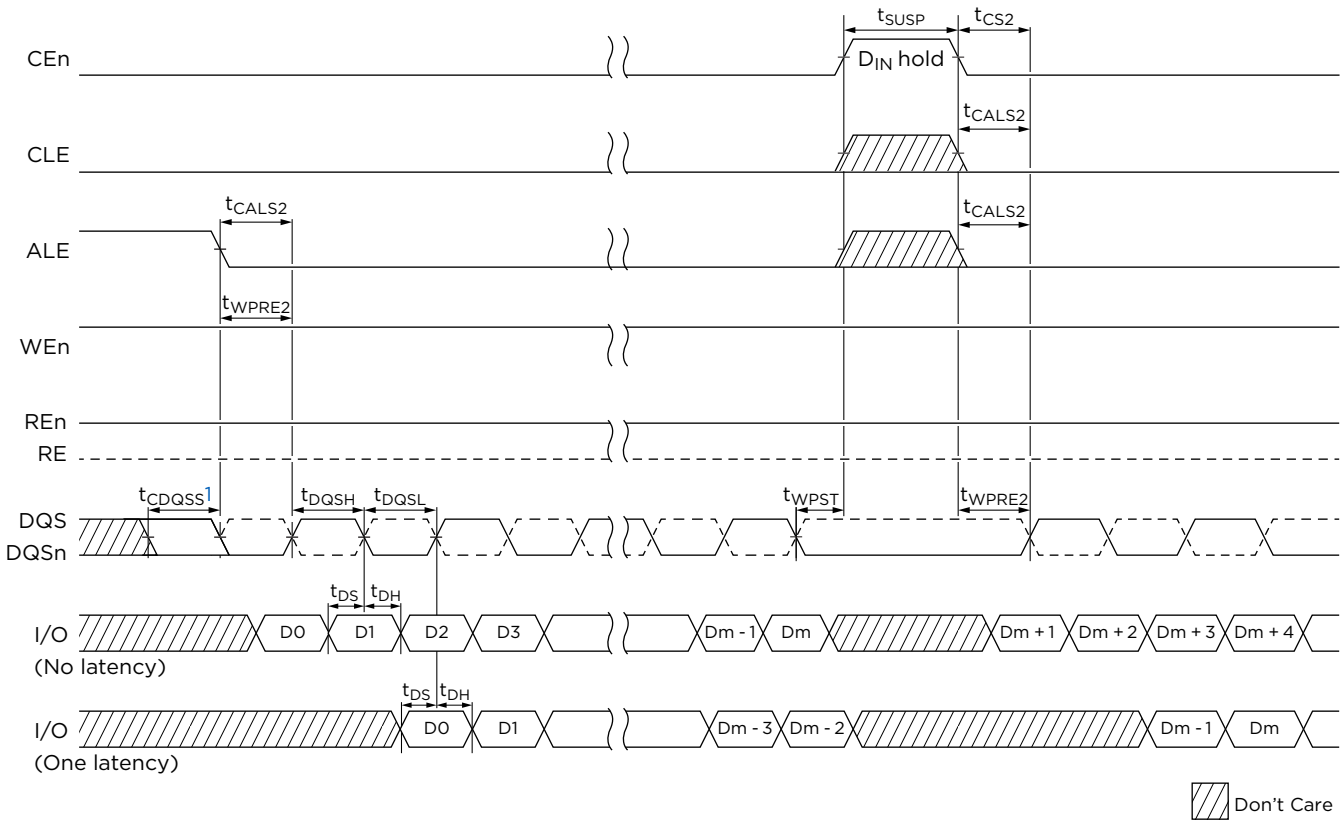


Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

Figure 117: D_{IN} Hold with DQS Low (with ODT)



Notice: This drawing assumes no de-rating of input slew rate. Refer to "8.7 Input/Output Slew Rate" on page 67 and Figure 36, Figure 37, Figure 38, and Figure 39 for exact measurements of tDS and tDH.

Note 1. The tCDQSS spec is used to drive and stabilize DQS before entering data-in mode. Prior to tCDQSS, DQS can be Hi-z. This spec must be maintained during all Toggle Mode data-in sequences occurring before the last valid-address-cycle ALE falling edge (ALE transitioning from high to low), without regard to CEn.

There is one exception, which is for D_{IN} Hold/Resume. Before data input resumes, ensure that tCDQSS is met with respect to the falling edge of the resuming signal (CEn/CLE/ALE = low). During tCDQSS, the DQS/DQSn signals must be driven high or low, with no toggling and no High-z. After tCDQSS completes, DQS/DQSn should follow other specs such as tWPRE/tWPRE2.

Western Digital Corporation
5601 Great Oaks Parkway
San José, CA 95119 U.S.A.
www.westerndigital.com

Western Digital Technologies, Inc. is the seller of record and licensee in the Americas of SanDisk® products.

18 Revision History

Table 79: Revision History

Status	Rev. #	Date	Changes
Preview	0.1	7/20/22	Initial draft release