Embedded Storage

SM2259XT

SATA Solid-State Drive Controller

Datasheet

Revision 0.1 May 2018

Revision History

Revision	Date	Description
0.1	May 28, 2018	Initial release

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1. Overview

1.1 Product Description

The SM2259XT is a high-performance SATA 6Gb/s SSD controller ideally suited for client SSDs, Ultrabooks, and Tablets. The controller fully supports high-speed Toggle, ONFI, as well as the latest generation NAND flash, enabling the realization of fast, reliable, and feature-wise SSDs on the market. Incorporated Silicon Motion's proprietary NANDXtend® error-correcting code (ECC) technology, the SM2259XT provides comprehensive data protection and enhances the endurance and retention of TLC and QLC NAND, achieving longer durability for SSD.

1.2 Key Features

- Host Interface
  - Industrial Standard SATA Revision 3.1 compliant
  - Industrial Standard ATA/ATAPI-8 and ACS-3 command compliant
  - Supports SATA interface rate of 6Gb/s (backward compatible to 1.5Gb/s and 3Gb/s)
  - Native Command Queuing up to 32 commands
  - Supports SATA device sleep mode (DevSleep)
  - Data Set Management command (TRIM support)
  - Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
  - Supports 28-bit and 48-bit LBA (Logical Block Addressing) mode commands
- NAND Flash Support
  - Supports ONFI 4.0 and Toggle 2.0 interface
  - Supports SDR, NV-DDR, NV-DDR2, NV-DDR3, and Toggle DDR/DDR2 NAND flash
  - 4-channel flash interface supports up to 16 NAND flash devices
  - Supports 1.2V/1.8V Flash I/O
  - Supports 8KB and 16KB page size
  - Supports 1-plane, 2-plane, and 4-plane operation
- Data Protection and Reliability
  - End-to-End Protection
  - Supports ATA8 security feature set
  - Hardware LDPC ECC engine with hard-decision and soft-decision decoding
  - RAID engine offers additional level of data protection
  - Internal data shaping technique increases data endurance
  - StaticDataRefresh technology ensures data integrity
  - Early weak block retirement option
  - Global wear leveling algorithm evens program/erase count and extends SSD lifespan

- Architecture
  - 32-bit RISC CPU
  - High-efficiency 64-bit system bus
  - Automatic sleep and wake-up mechanism to save power
  - Built-in voltage detectors for power failure protection
  - Built-in power-on reset and voltage regulators
  - Built-in temperature sensor for SSD temperature detection
  - Supports JTAG interface and UART (RS-232) interface
- Enhanced Security
  - Real time full drive encryption with Advanced Encryption Standard (AES)
  - Trusted Computing Group (TCG) Opal protocol
  - Hardware SHA 256 and True Random Number Generator (TRNG)
  - eFuse Memory (OTP)
- Package
  - 144-ball TFBGA
  - Lead-free and RoHS compliant

1.3 Functional Description

Host Interface

The high-speed SATA interface is compliant with SATA Revision 3.1 and ATA-8 ACS-3 specifications, and supports device sleep mode to efficiently save power consumption.

Flash Interface and Data Transfer

In addition to supporting high-speed Toggle, ONFI, and legacy Asynchronous NAND, the flash interface enables 2-way and 4-way interleaving for a multi-bank NAND flash connection to obtain optimal performance. The SM2259XT uses a superior DMA technology to transfer data between the host and the NAND flash interface. The DMA technology transfers data at a very high rate in both directions (read and write) and in doing so, effectively decreases the loading of micro processor.

LDPC ECC

The LDPC ECC engine executes parity generation and error detection/correction features, and enhances decoding throughput and data reliability. With LDPC of correction capability 1e-2 RBER, the hard and soft decoding mechanism provides powerful error correction. Hence the SM2259XT can enhance the endurance and retention of TLC and QLC NAND and extends the SSD lifespan.

RAID Protection

In case of uncorrectable errors occurring within a superblock (a pre-defined area which consists of a particular set of blocks across physical NAND units), the RAID engine recovers the uncorrectable error chunk by using a certain storage space of parity bits. Incorporated with LDPC, the RAID ensures a comprehensive level of data integrity while providing a broad range of RAID overhead protection.

Data Security

Security commands can be used to lock and unlock the drive by password or through a hardware switch. For those users who require the highest level of security, the SM2259XT provides an enhanced data security option. By utilizing the latest data management techniques such as AES and TCG Opal, the full data encryption on SSD can eventually ensure the security of confidential data and information.

SLC Caching

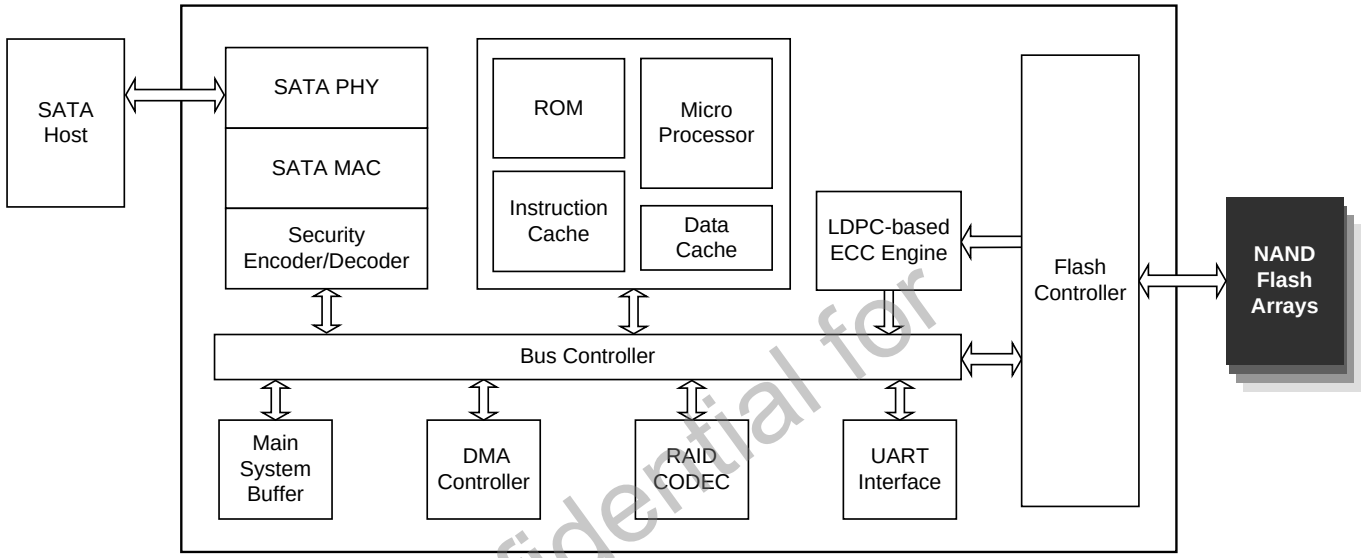
The intelligent SLC caching algorithm enables the NAND flash memory to operate in SLC-mode and hence enhances write performance of SSD.

SMART

The SM2259XT supports SMART commands that allow users to read spare and bad block information. The users can thus evaluate drive health at run time and receive an early warning before the drive life ends.

1.4 Block Diagram

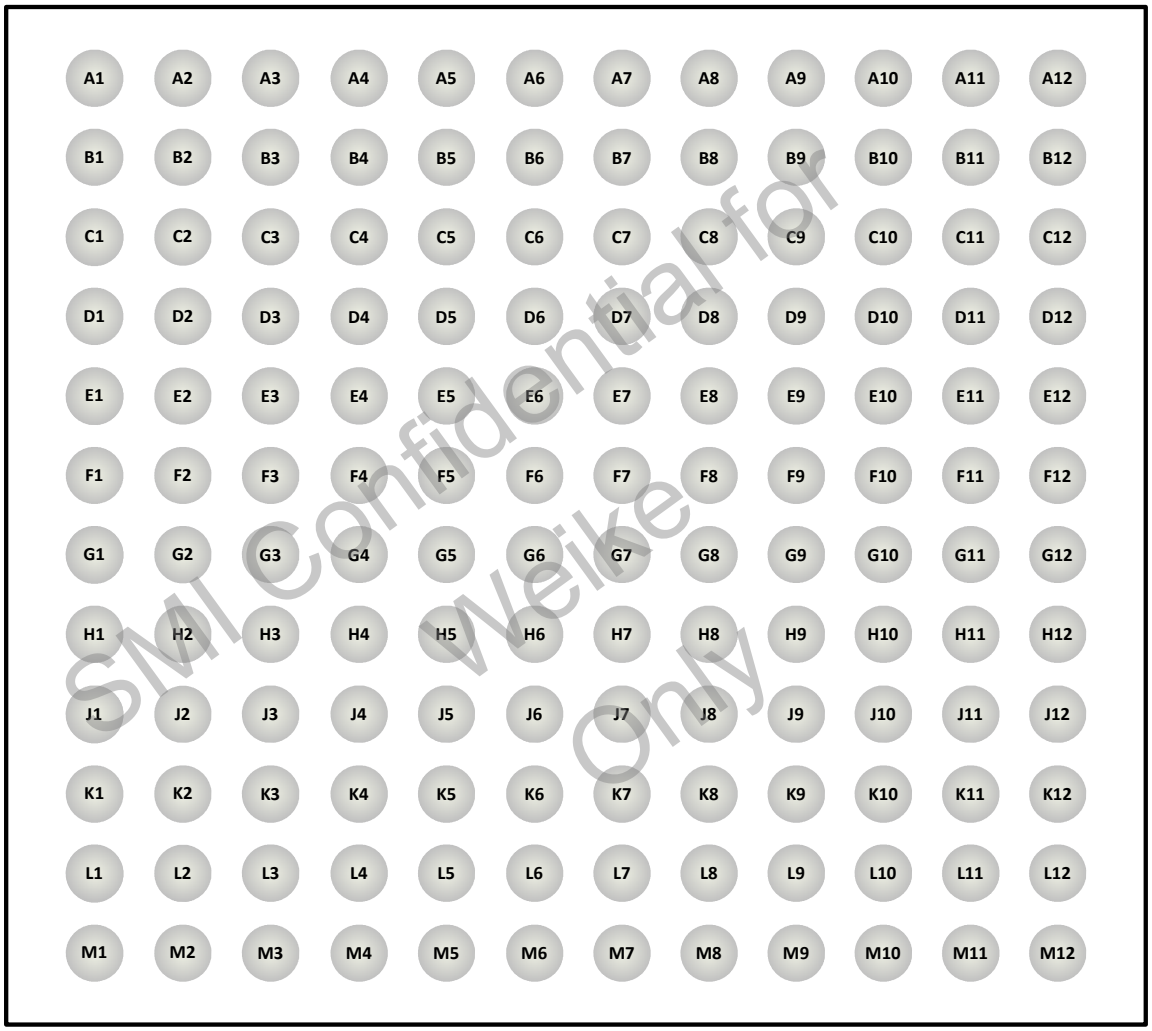
Figure 1: SM2259XT Block Diagram



2. Signal Descriptions

2.1 Ball Assignments

Figure 2: 144-Ball TFBGA Assignments (Top View – Balls Down)



2.2 Signal Descriptions

Table 1: SATA Interface Signals

Signal	Ball NO.	Type	Description
p0_rx_p	A5	CMOS input	SATA Rx Differential Pair
p0_rx_m	A4	CMOS input	
p0_tx_p	A2	CMOS output	SATA Tx Differential Pair
p0_tx_m	A1	CMOS output	
p0_resref	B1	Input	External reference for output drive calibration. Attach a 200Ω (±1%) precision resistor-to-ground on the board.
DEVSLP	B5	CMOS input	SATA device sleep mode (DevSleep) If the host supports DevSleep, the device will enter sleep mode when this pin is asserted high.

Table 2: Flash Interface Signals

Signal	Ball NO.	Type	Description
P_FSH0_DAT[0]	L2	CMOS I/O	Flash data bus for channel 0
P_FSH0_DAT[1]	M2	CMOS I/O	
P_FSH0_DAT[2]	K3	CMOS I/O	
P_FSH0_DAT[3]	M3	CMOS I/O	
P_FSH0_DAT[4]	K4	CMOS I/O	
P_FSH0_DAT[5]	L4	CMOS I/O	
P_FSH0_DAT[6]	K5	CMOS I/O	
P_FSH0_DAT[7]	L5	CMOS I/O	
P_FSH1_DAT[0]	L11	CMOS I/O	Flash data bus for channel 1
P_FSH1_DAT[1]	K10	CMOS I/O	
P_FSH1_DAT[2]	L10	CMOS I/O	
P_FSH1_DAT[3]	K9	CMOS I/O	
P_FSH1_DAT[4]	L9	CMOS I/O	
P_FSH1_DAT[5]	K8	CMOS I/O	
P_FSH1_DAT[6]	L8	CMOS I/O	
P_FSH1_DAT[7]	L7	CMOS I/O	

Table 2: Flash Interface Signals (continued)

Signal	Ball NO.	Type	Description
P_FSH2_DAT[0]	J11	CMOS I/O	Flash data bus for channel 2
P_FSH2_DAT[1]	H10	CMOS I/O	
P_FSH2_DAT[2]	H11	CMOS I/O	
P_FSH2_DAT[3]	G10	CMOS I/O	
P_FSH2_DAT[4]	G11	CMOS I/O	
P_FSH2_DAT[5]	F10	CMOS I/O	
P_FSH2_DAT[6]	F11	CMOS I/O	
P_FSH2_DAT[7]	E11	CMOS I/O	
P_FSH3_DAT[0]	A11	CMOS I/O	Flash data bus for channel 3
P_FSH3_DAT[1]	A12	CMOS I/O	
P_FSH3_DAT[2]	B10	CMOS I/O	
P_FSH3_DAT[3]	B11	CMOS I/O	
P_FSH3_DAT[4]	B12	CMOS I/O	
P_FSH3_DAT[5]	C10	CMOS I/O	
P_FSH3_DAT[6]	C11	CMOS I/O	
P_FSH3_DAT[7]	C12	CMOS I/O	
P_FSH0_ALE	K6	CMOS output	Flash address latch enable – channel 0
P_FSH1_ALE	K11	CMOS output	Flash address latch enable – channel 1
P_FSH2_ALE	D10	CMOS output	Flash address latch enable – channel 2
P_FSH3_ALE	D9	CMOS output	Flash address latch enable – channel 3
P_FSH0_CLE	K7	CMOS output	Flash command latch enable – channel 0
P_FSH1_CLE	J10	CMOS output	Flash command latch enable – channel 1
P_FSH2_CLE	D11	CMOS output	Flash command latch enable – channel 2
P_FSH3_CLE	C9	CMOS output	Flash command latch enable – channel 3
P_FSH0_CEN[0]	J3	CMOS output	Flash chip enable - channel 0
P_FSH0_CEN[1]	J2	CMOS output	
P_FSH0_CEN[2]	J1	CMOS output	
P_FSH0_CEN[3]	L3	CMOS output	
P_FSH1_CEN[0]	K1	CMOS output	Flash chip enable - channel 1
P_FSH1_CEN[1]	K2	CMOS output	
P_FSH1_CEN[2]	L1	CMOS output	
P_FSH1_CEN[3]	M1	CMOS output	
P_FSH2_CEN[0]	D8	CMOS output	Flash chip enable - channel 2
P_FSH2_CEN[1]	C8	CMOS output	
P_FSH2_CEN[2]	B9	CMOS output	
P_FSH2_CEN[3]	A9	CMOS output	

Table 2: Flash Interface Signals (continued)

Signal	Ball NO.	Type	Description
P_FSH3_CEN[0]	A8	CMOS output	Flash chip enable - channel 3
P_FSH3_CEN[1]	B8	CMOS output	
P_FSH3_CEN[2]	C7	CMOS output	
P_FSH3_CEN[3]	D7	CMOS output	
P_FSH0_DQS_P	M5	CMOS I/O	P_FSHx_DQS_P/P_FSHx_DQS_N: Flash data strobe/Flash data strobe complement. • For SDR access mode, these signals are not used (no connect). • For NV-DDR and Toggle DDR 1.0 access modes, the P_FSHx_DQS_P indicates the data valid window. Input with read data, output with write data. Edge-aligned with read data, centered in write data. For NV-DDR2/NV-DDR3 and Toggle DDR 2.0 access modes, P_FSHx_DQS_P indicates the data valid window. P_FSHx_DQS_P is paired with differential signal P_FSHx_DQS_N to provide differential pair signaling to the system during reads and writes.
P_FSH0_DQS_N	M4	CMOS I/O	
P_FSH1_DQS_P	M10	CMOS I/O	
P_FSH1_DQS_N	M11	CMOS I/O	
P_FSH2_DQS_P	K12	CMOS I/O	
P_FSH2_DQS_N	L12	CMOS I/O	
P_FSH3_DQS_P	E12	CMOS I/O	
P_FSH3_DQS_N	D12	CMOS I/O	
P_FSH_WP	J6	CMOS output	Flash write protect signal directly connected to the flash memory write protect signal.
P_FSH_FRB	J7	CMOS input	Flash ready/busy signals indicating the state, ready or busy of flash memory.
P_FSH0_RE_N_P	M6	CMOS output	P_FSHx_RE_N_P / P_FSHx_RE_N_N: Flash read enable and Flash read enable complement. • For SDR access mode, the P_FSHx_RE_N_P enables serial data output. • For NV-DDR2/NV-DDR3 and Toggle DDR 1.0/2.0 access modes, the P_FSHx_RE_N_P signal is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after tDQSRE of rising edge and falling edge of P_FSHx_RE_N_P, which also increments the internal column address counter by each one. The read enable P_FSHx_RE_N_N is paired with differential signal P_FSHx_RE_N_P (only in NV-DDR2 and Toggle DDR 2.0 modes) to provide differential pair signaling to the system during reads. For NV-DDR access mode, P_FSHx_RE_N_N is used as write/read direction control. When this signal is latched high, the controller is driving the DQ bus and DQS (data is being written to the bus). When this signal is latched low, the NAND flash is driving the DQ bus and DQS (data is being read from the bus).
P_FSH0_RE_N_N	M7	CMOS output	
P_FSH1_RE_N_P	M9	CMOS output	
P_FSH1_RE_N_N	M8	CMOS output	
P_FSH2_RE_N_P	J12	CMOS output	
P_FSH2_RE_N_N	H12	CMOS output	
P_FSH3_RE_N_P	F12	CMOS output	
P_FSH3_RE_N_N	G12	CMOS output	

Table 2: Flash Interface Signals (continued)

Signal	Ball NO.	Type	Description
P_FSH0_WE_N	L6	CMOS output	Flash write enable • For SDR access mode, the write enable signal controls the latching of output data. Data, commands, and addresses are latched on the rising edge of P_FSHx_WE_N. • For NV-DDR2/NV-DDR3 and Toggle DDR 1.0/2.0 access modes, this signal controls writes to the DQ bus. Commands and addresses are latched on the rising edge of the WE pulse. • For NV-DDR access mode, this signal is used as the clock.
P_FSH1_WE_N	J9	CMOS output	
P_FSH2_WE_N	E10	CMOS output	
P_FSH3_WE_N	A10	CMOS output	
VREFIO_FSH	M12	Input	External Flash I/O reference voltage (0.5 x VCCFQ)

Table 3: Power Signals

Signal	Ball NO.	Type	Description
V11A_PAD	A7	Analog power input	SATA PHY core and AIP power 1.16V
V25_PAD	E6	Analog power output	3.3V-to-2.5V regulator output
VCCAH	B2	Analog power input	Power supply for SATA PHY and AIP 3.3V
VCCFQ	F9, G9, H9, J8	Power input	Power supply for Flash I/O 1.2V/1.8V
VCCGQ	F1	Power input	Power supply for general I/O 1.8V/3.3V
VDD	E7-E9, F7, F8	Power input	Core power supply 1.16V
VSS	G5, G6, H5, H6	Ground	Core ground connection
VSS33	G7, G8, H7, H8	Ground	GPIO/Flash IO ground connection
VCC5V	B6	Analog input	Voltage detection input for Host power supply
VDTF_VIN	B7	Analog input	Voltage detection input for Flash power
CRY_AVDD33	C1	Analog power input	Crystal power supply 3.3V
VGNDA	A3, B4	Analog ground	SATA PHY and AIP ground connection
CRY_AVSS33	C2	Analog ground	Crystal ground connection

Table 4: Miscellaneous Signals

Signal	Ball NO.	Type	Description
P_EXRSTN	D5	CMOS input	Chip Global Reset
P_EXCLK	C4	CMOS input	Chip External Clock
EX_PWD_N	A6	CMOS output	External Power Control Signal
P_P0[1]	H3	CMOS I/O	General Purpose I/O
P_P1[0]	D2	CMOS I/O	General Purpose I/O
P_P1[1]	E2	CMOS I/O	General Purpose I/O
P_P1[2]	F5	CMOS I/O	General Purpose I/O
P_P1[3]	F4	CMOS I/O	General Purpose I/O
P_P1[4]	F3	CMOS I/O	General Purpose I/O
P_P1[5]	F2	CMOS I/O	General Purpose I/O
P_P1[6]	G4	CMOS I/O	General Purpose I/O
P_P1[7]	H4	CMOS I/O	General Purpose I/O
P_P2[0]	D3	CMOS I/O	General Purpose I/O
P_P2[2]	D4	CMOS I/O	General Purpose I/O
P_P2[3]	B3	CMOS I/O	General Purpose I/O
P_P2[4]	E5	CMOS I/O	General Purpose I/O
P_P2[5]	C3	CMOS I/O	General Purpose I/O
P_P2[6]	E4	CMOS I/O	General Purpose I/O
P_P2[7]	E3	CMOS I/O	General Purpose I/O
efuse_VQPS	F6	Power input	eFuse power
XOUT	D1	CMOS output	Crystal Out
XIN	E1	CMOS input	Crystal In
P_JTAG_TRST_N	G1	CMOS input	JTAG Signal
P_JTAG_TMS	J5	CMOS input	JTAG Signal
P_JTAG_TDI	H1	CMOS input	JTAG Signal
P_JTAG_TDO	J4	CMOS output	JTAG Signal
P_JTAG_TCK	G2	CMOS input	JTAG Signal
P_TEST0	D6	CMOS input	Test signal. Tie to ground for normal operation.
P_TEST1	C6	CMOS input	Test signal. Tie to ground for normal operation.
P_TEST2	C5	CMOS input	Test signal. Tie to ground for normal operation.
NC	G3, H2	/	Used for internal test. Do not connect (N.C.)

Note: For more information on GPIO, please contact project manager or local support personnel.

3. Electrical Specifications

3.1 Recommended Operating Conditions

Table 5: Recommended/Typical Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power Supply	VDD	1.07	1.16	1.21	V
I/O Pad Power Supply	VCCGQ	1.7	1.8	1.95	V
		2.7	3.3	3.6	
Flash I/O Power Supply	VCCFQ	1.14	1.2	1.26	V
		1.7	1.8	1.95	V
Flash I/O Reference Voltage	VREFIO_FSH	0.5 x VCCFQ			V
Analog Power Supply (SATA PHY and AIP)	V11A_PAD	1.07	1.16	1.21	V
	VCCAH	3.06	3.3	3.63	V
	CRY_VDD33	3.06	3.3	3.63	V

3.2 DC Electrical Characteristics

Table 6: Digital DC Electrical Characteristics (VCCGQ of 3.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCGQ	2.7	3.3	3.6	V
High Level Output Voltage	V_{OH}	0.67 x V_{IO}			V
Low Level Output Voltage	V_{OL}			0.4	V
High Level Input Voltage	V_{IH}	0.8 x V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 x V_{IO}	V
Pull-up Resistance	R_{PU}	28.6	40.8	69.4	kΩ
Pull-down Resistance	R_{PD}	27.1	38.7	69.4	kΩ

Table 7: Digital DC Electrical Characteristics (VCCGQ of 1.8V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCGQ	1.7	1.8	1.95	V
High Level Output Voltage	V_{OH}	VCCGQ - 0.1			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Input Voltage	V_{IH}	0.8 x V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 x V_{IO}	V
Pull-up Resistance	R_{PU}	52.6	82.9	129	kΩ
Pull-down Resistance	R_{PD}	47.1	79.3	133.4	kΩ

Table 8: Digital DC Electrical Characteristics (VCCFQ of 1.8V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCFQ	1.7	1.8	1.95	V
High Level Output Voltage	V_{OH}	VCCFQ - 0.1			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Input Voltage	V_{IH}	0.8 x V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 x V_{IO}	V
Pull-up Resistance	R_{PU}	34.4	53.4	81.5	kΩ
Pull-down Resistance	R_{PD}	31.3	51.5	85.1	kΩ

Table 9: Digital DC Electrical Characteristics (VCCFQ of 1.2V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{IO})	VCCFQ	1.14	1.2	1.26	V
High Level Output Voltage	V_{OH}	VCCFQ - 0.1			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Input Voltage	V_{IH}	0.8 x V_{IO}		V_{IO} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{SS33} - 0.3		0.2 x V_{IO}	V
Pull-up Resistance	R_{PU}	67.4	110.2	170.9	kΩ
Pull-down Resistance	R_{PD}	68.8	115.1	186.1	kΩ

3.3 Flash Interface Timing Characteristics

3.3.1 SDR (Legacy NAND) Interface

Table 10: AC Timing Characteristics of SDR Mode

Parameter	Symbol	Min	Max	Unit
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	5.0		ns
CLE Setup Time	tCLS	10.0		ns
CLE Hold Time	tCLH	5.0		ns
ALE Setup Time	tALS	10.0		ns
ALE Hold Time	tALH	5.0		ns
Write Cycle Time	tWC	20.0		ns
WE# Pulse Width	tWP	10.0		ns
WE# High Hold Time	tWH	7.0		ns
Write Data Setup Time	tDS	7.0		ns
Write Data Hold Time	tDH	5.0		ns
Read Cycle Time	tRC	20.0		ns
Ready to RE# Low	tRR	20.0		ns
RE# Pulse Width	tRP	10.0		ns
RE# High Hold Time	tREH	7.0		ns

Figure 3: Command Latch Timing

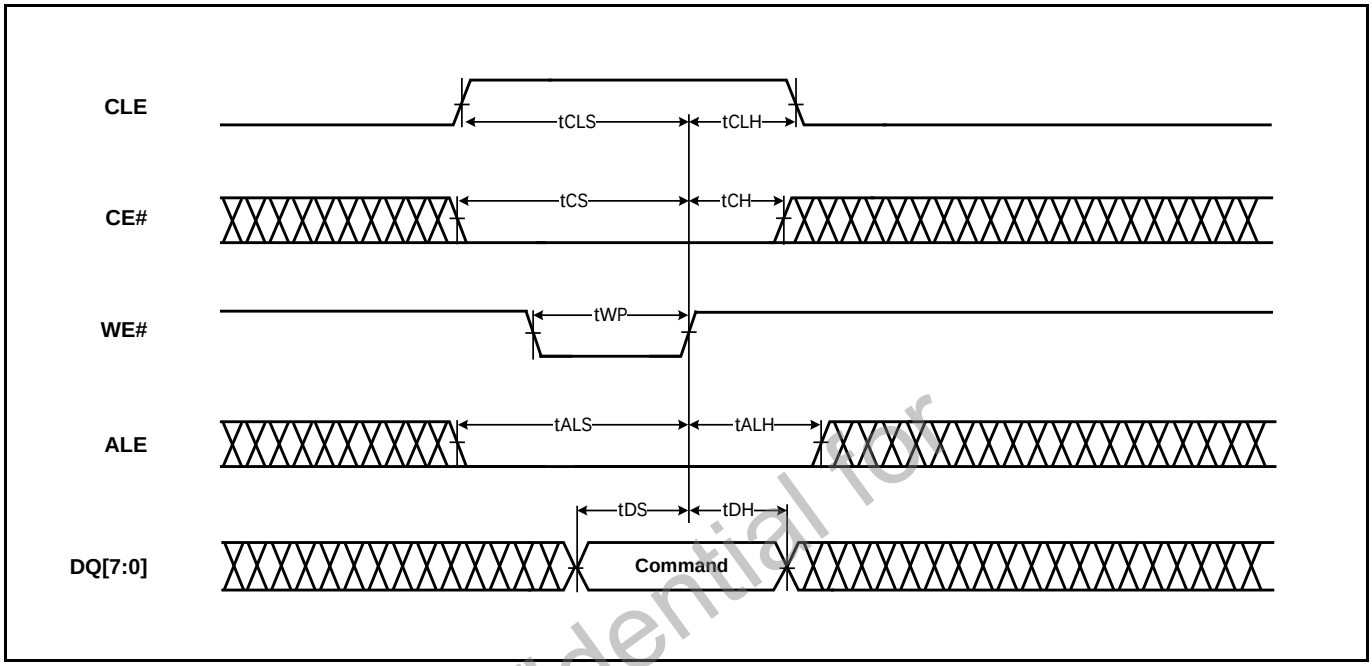


Figure 4: Address Latch Timing

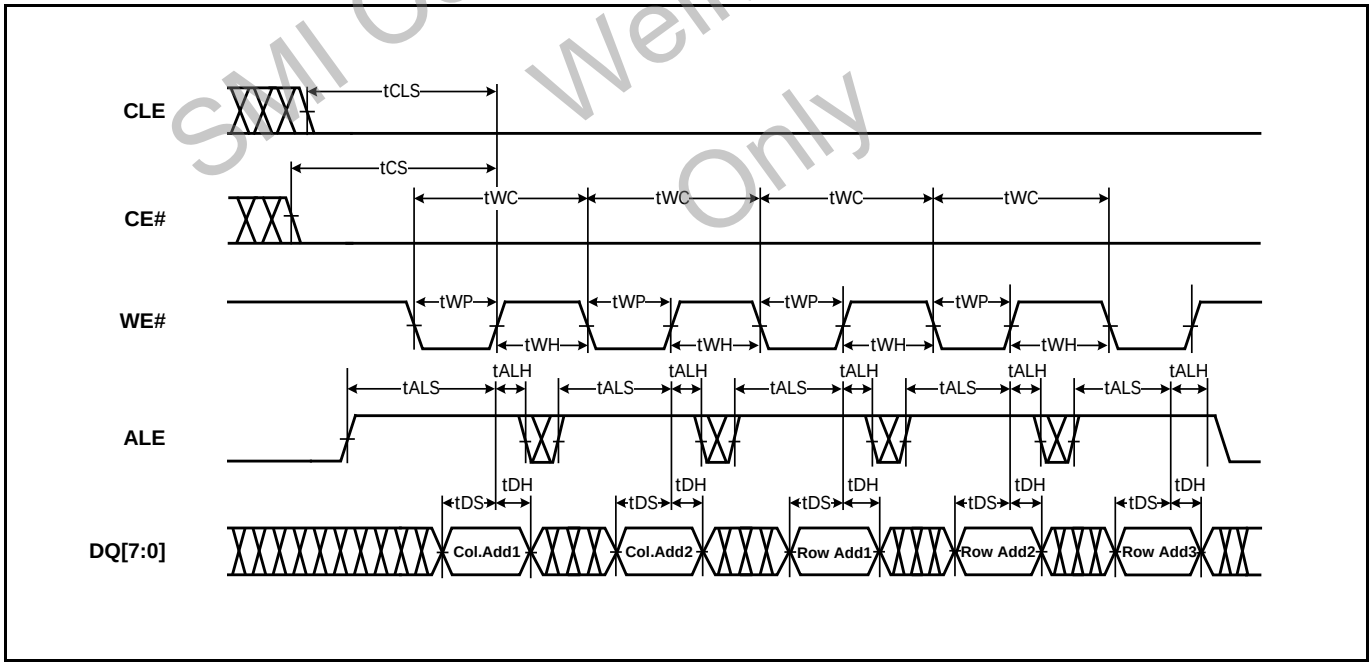


Figure 5: Data Output (Write) Cycle Timing

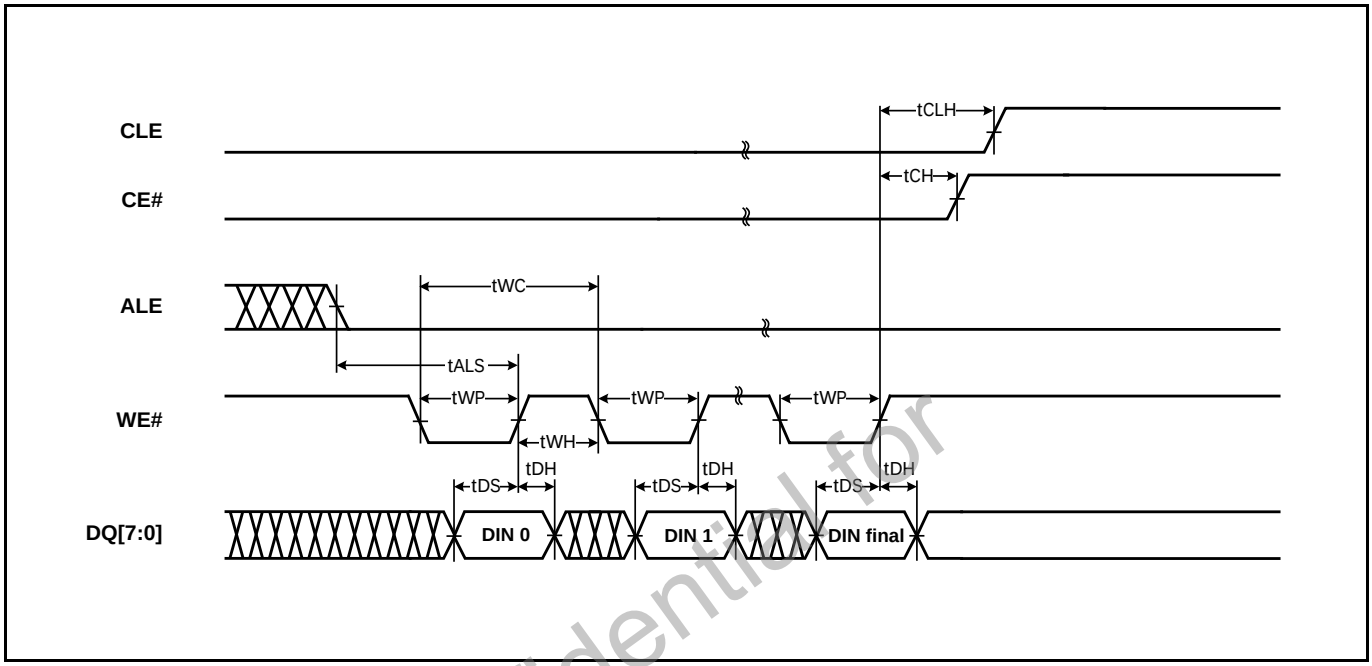
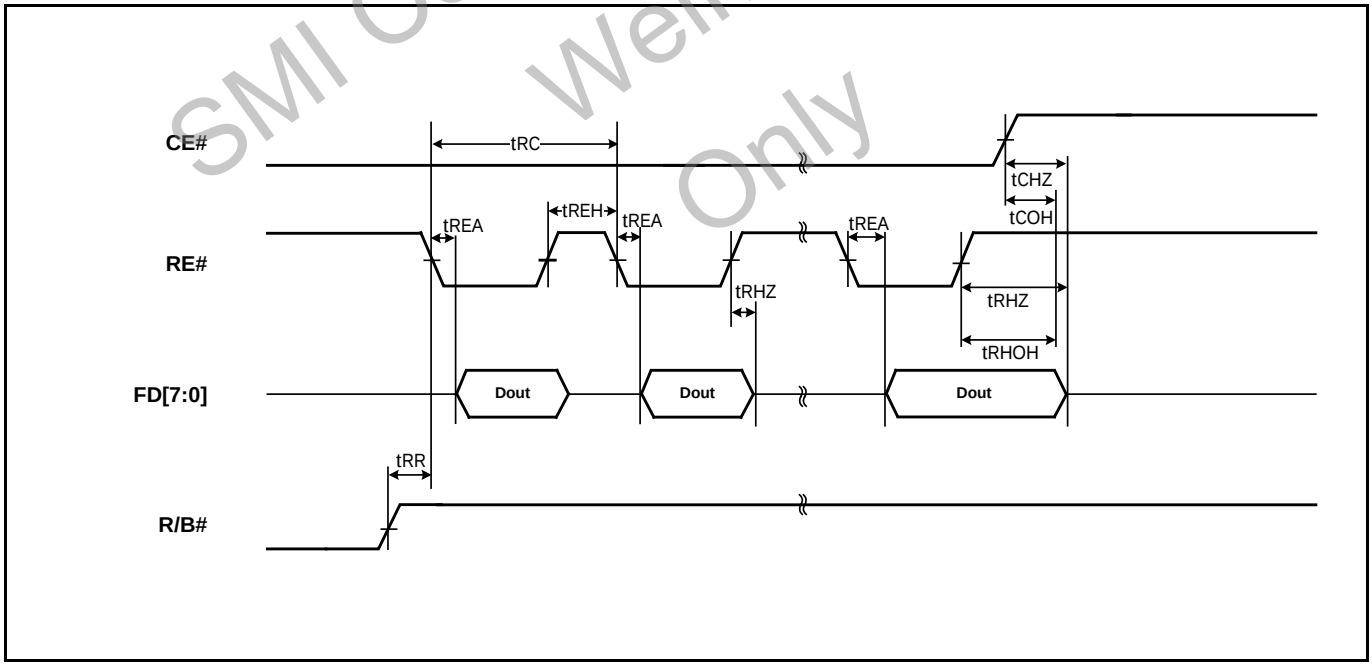


Figure 6: Data Input (Read) Cycle Timing



3.3.2 NV-DDR Interface

Table 11: AC Timing Characteristics of NV-DDR Mode

Parameter	Symbol	Min	Max	Unit
CLK Cycle Time	tCK	10.0		ns
CLK Low Time	tCKL	0.43	0.57	tCK
CLK High Time	tCKH	0.43	0.57	tCK
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	2.0		ns
CLE, ALE, W/R# Setup Time	tCALS	2.0		ns
CLE, ALE, W/R# Hold Time	tCALH	2.0		ns
Command & Address DQ Setup Time	tCAS	2.0		ns
Command & Address DQ Hold Time	tCAH	2.0		ns
Data Output (Write) Setup Time	tDS	0.9		ns
Data Output (Write) Hold Time	tDH	0.9		ns
DQS Falling Edge to CLK Rising Setup Time	tDSS	0.2		tCK
DQS Falling Edge to CLK Rising Hold Time	tDSH	0.2		tCK
DQS Low Pulse Width	tDQSL	0.4	0.6	tCK
DQS High Pulse Width	tDQSH	0.4	0.6	tCK
Data to the 1st DQS Latching Transition	tDQSS	0.75	1.25	tCK
DQS Write Preamble	tWPRE	1.5		tCK
DQS Write Postamble	tWPST	1.5		tCK
W/R# Low To Data Input Cycle	tWRCK	20.0		ns
W/R# Low to DQS/DQ Driven by Flash Memory	tDQSD	0	18.0	ns
Access Window of DQ[7:0] from CLK	tAC	3.0	20.0	ns
Access Window of DQS from CLK	tDQSCK		20.0	ns
DQS-DQ Skew, DQS to Last DQ Valid, Per Access	tDQSQ		0.85	ns
DQ-DQS Hold, DQS to The 1st DQ to Go No-valid	tQH	0.33		tCK
DQ Input Data Valid Window	tDVW	0.24		tCK

Figure 7: NV-DDR Command Cycle Timing

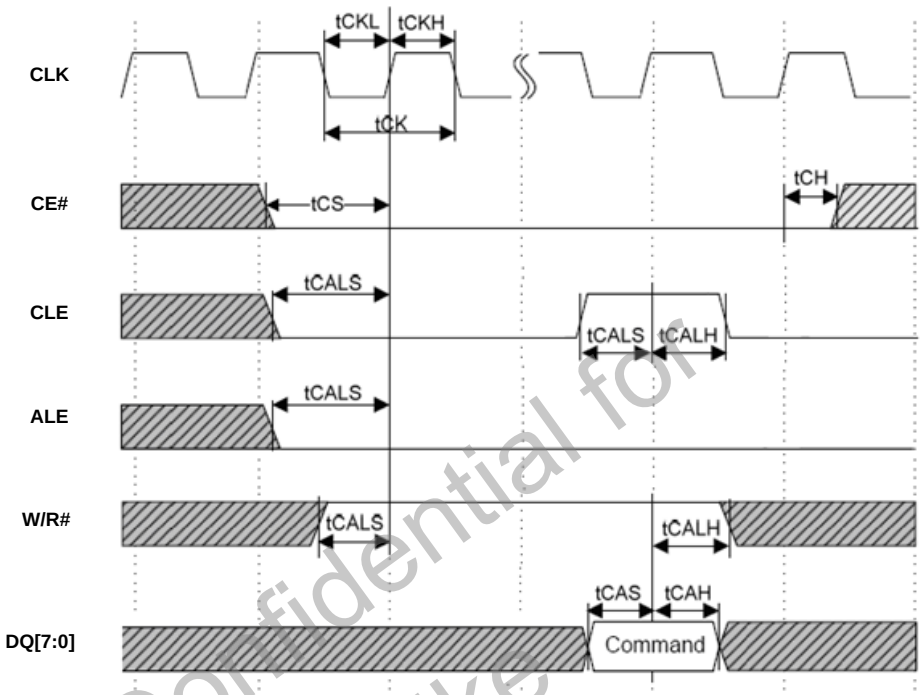


Figure 8: NV-DDR Address Cycle Timing

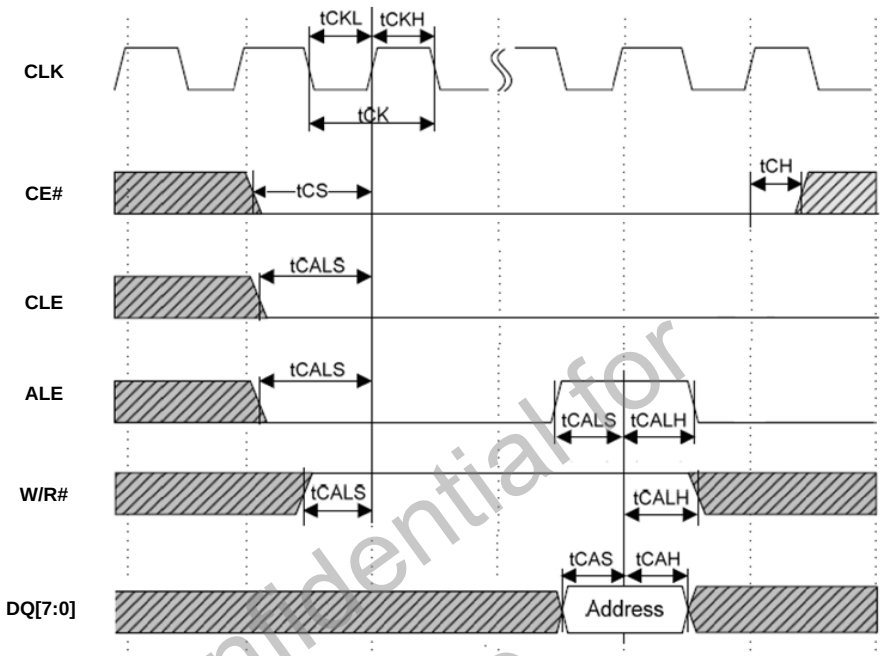


Figure 9: NV-DDR Data Output (Write) Cycle Timing

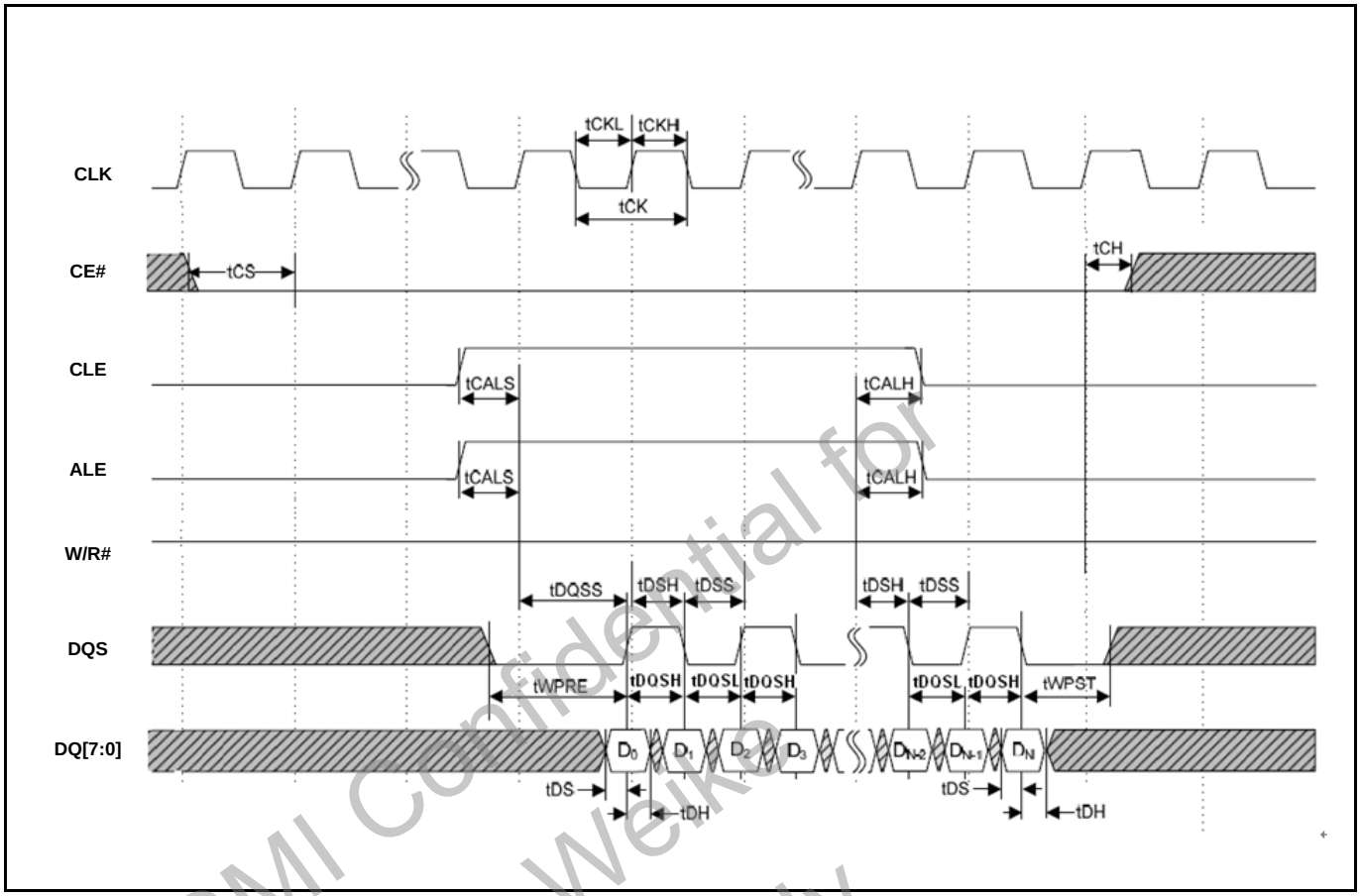
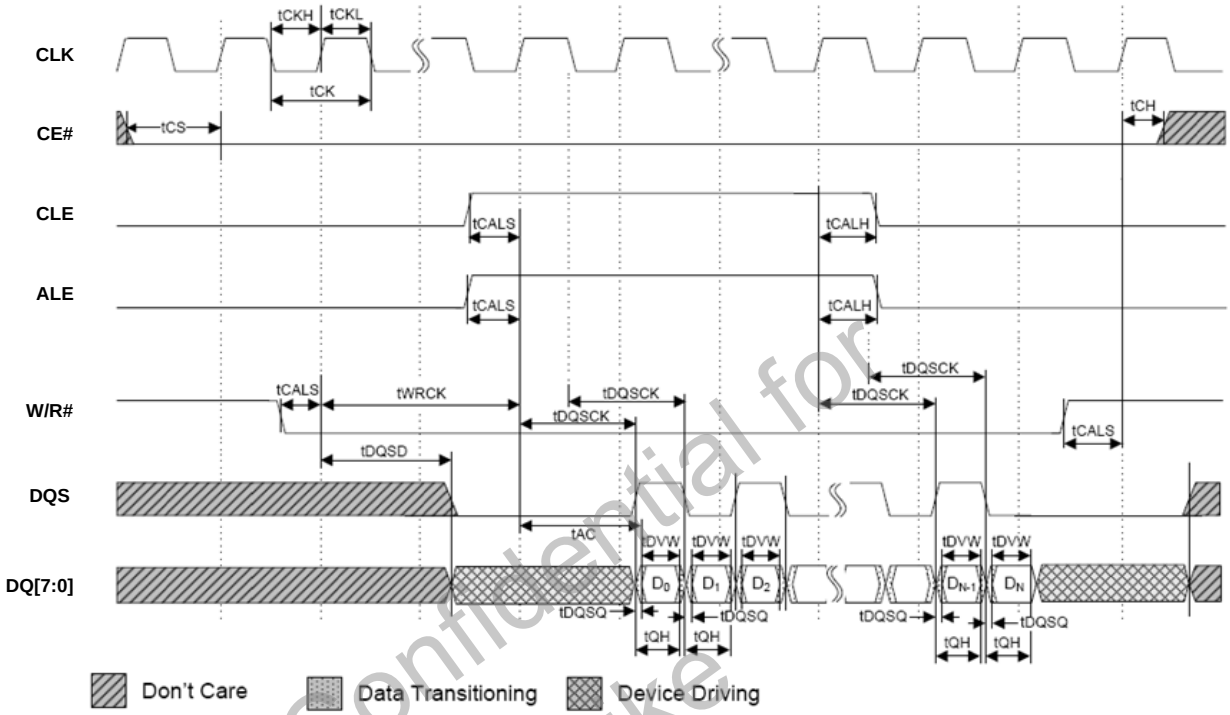


Figure 10: NV-DDR Data Input (Read) Cycle Timing



3.3.3 NV-DDR2 Interface

Table 12: AC Timing Characteristics of NV-DDR2 Mode

Parameter	Symbol	Min	Max	Unit
Address to Data Loading Time	tADL	100		ns
Command/Address Hold Time	tCAH	5		ns
Command/Address Setup Time	tCAS	5		ns
CLE/ALE Hold Time	tCALH	5		ns
CLE/ALE Setup Time	tCALS	15		ns
CLE/ALE Setup Time when ODT is enabled	tCALS2	25		ns
CE# Hold Time	tCH	5		ns
CE# Setup Time	tCS	40		ns
Write Cycle Time	tWC	25		ns
WE# High pulse Width	tWH	11		ns
WE# Low pulse Width	tWP	11		ns
WE# High to RE# Low	tWHR	120		ns
WE# High to RE# Low for Random Data out	tWHR2	300		ns
Data Strobe Cycle Time	tDSC	5		ns
Data Setup Time	tDS	0.4		ns
Data Hold Time	tDH	0.4		ns
DQS Output High Pulse Width	tDQSH	0.45*tRC	0.55*tRC	ns
DQS Output Low Pulse Width	tDQSL	0.45*tRC	0.55*tRC	ns
Read Cycle Time	tRC	5		ns
RE# High Pulse Width	tREH	0.45*tRC	0.55*tRC	ns
RE# Low Pulse Width	tRP	0.45*tRC	0.55*tRC	ns
Read Preamble	tRPRE	15		ns
Read Preamble when ODT is enabled	tRPRE2	25		ns
Read Postamble	tRPST	tDQSRE + 6*tRC		ns
Read Postamble Hold Time	tRPSTH	5		ns
Write Preamble	tWPRE	15		ns
Write Preamble when ODT is enabled	tWPRE2	25		ns
Write Postamble	tWPST	6.5		ns
Write Postamble Hold Time	tWPSTH	5		ns

Figure 11: NV-DDR2 Command Cycle Timing

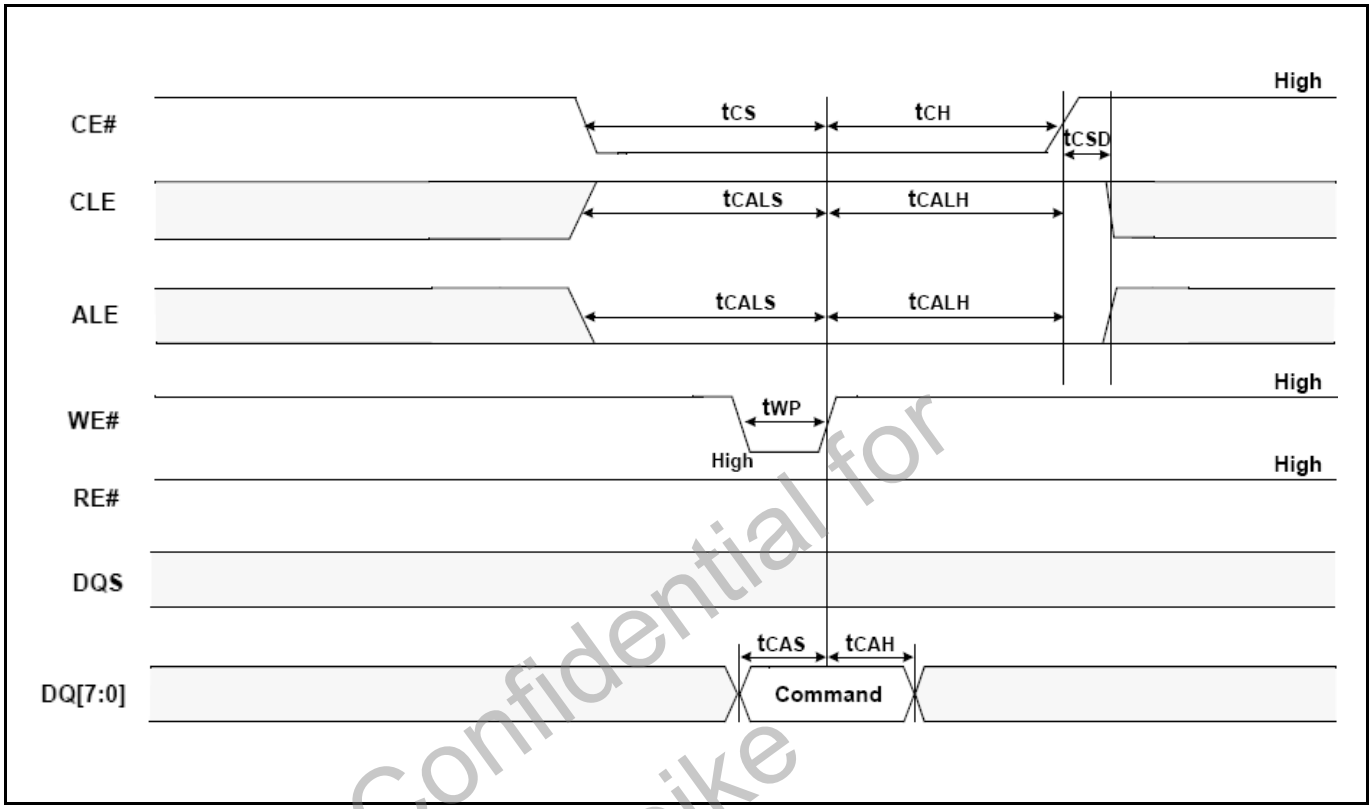


Figure 12: NV-DDR2 Address Cycle Timing

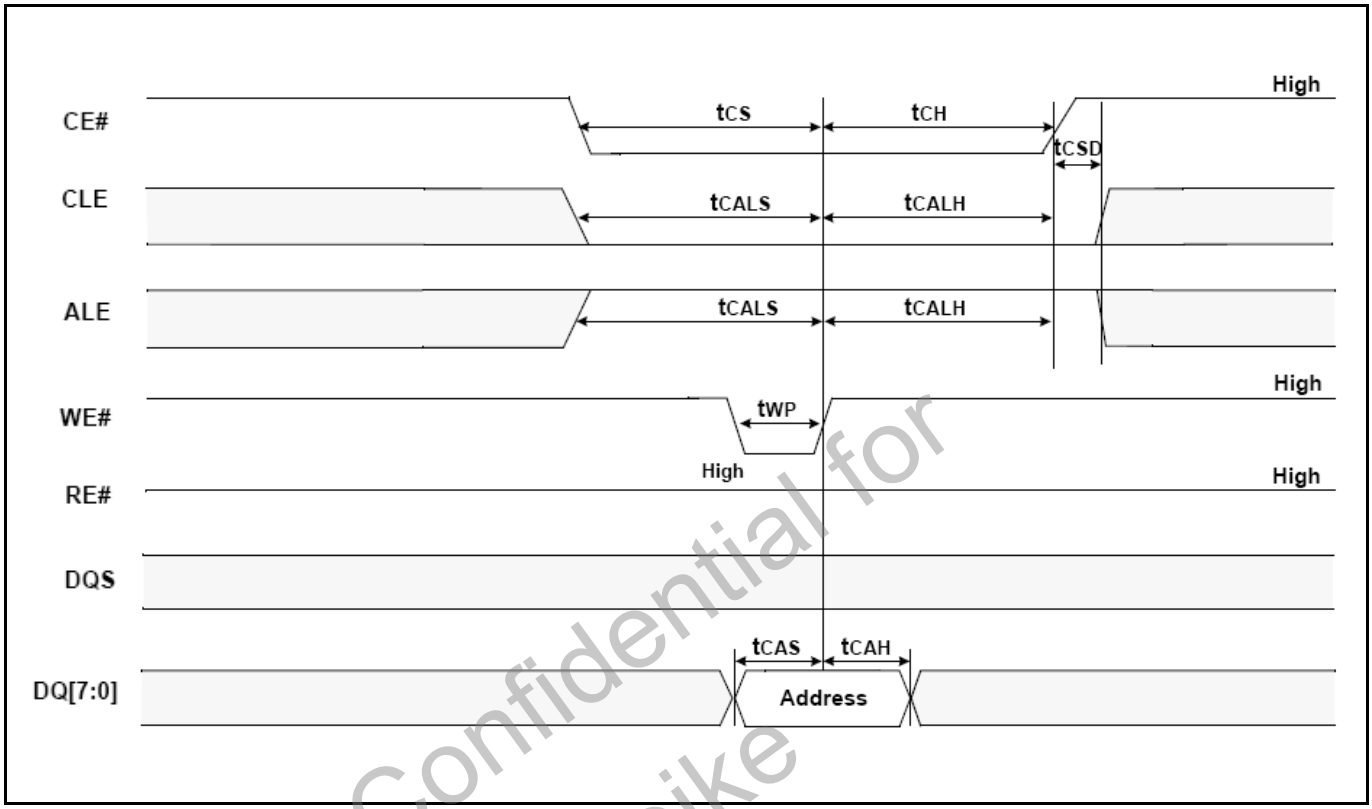


Figure 13: NV-DDR2 Data Output (Write) Cycle Timing

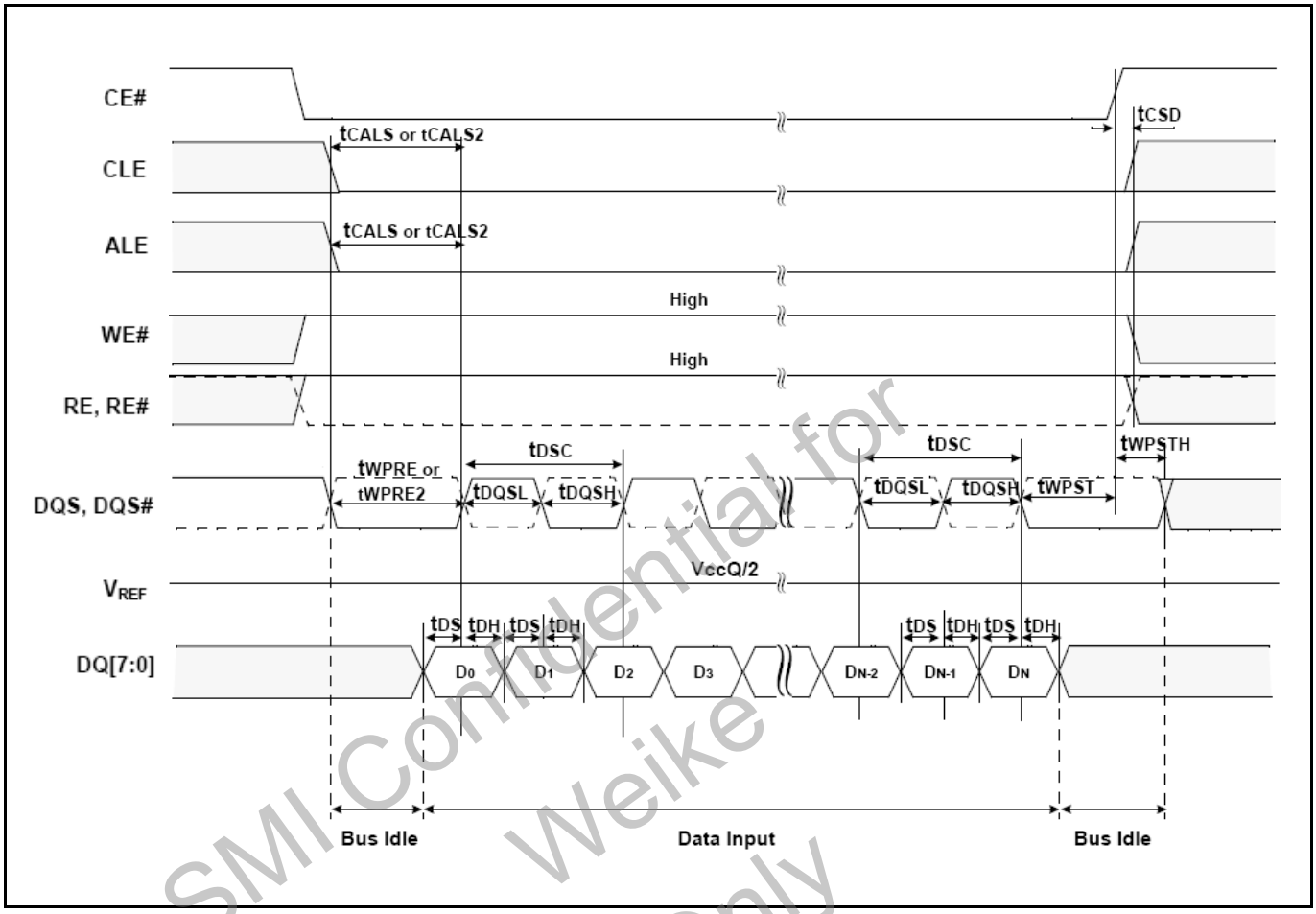
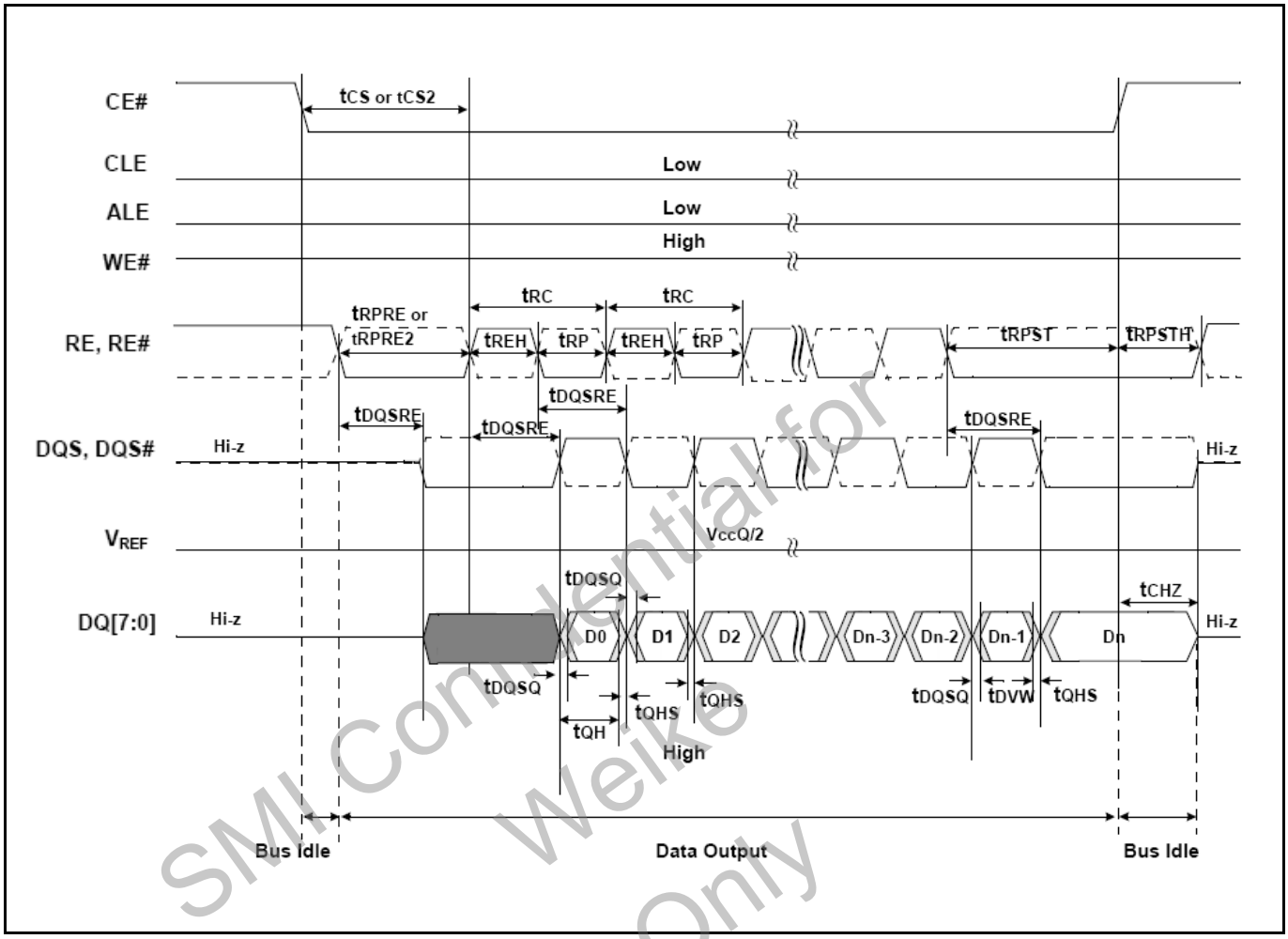
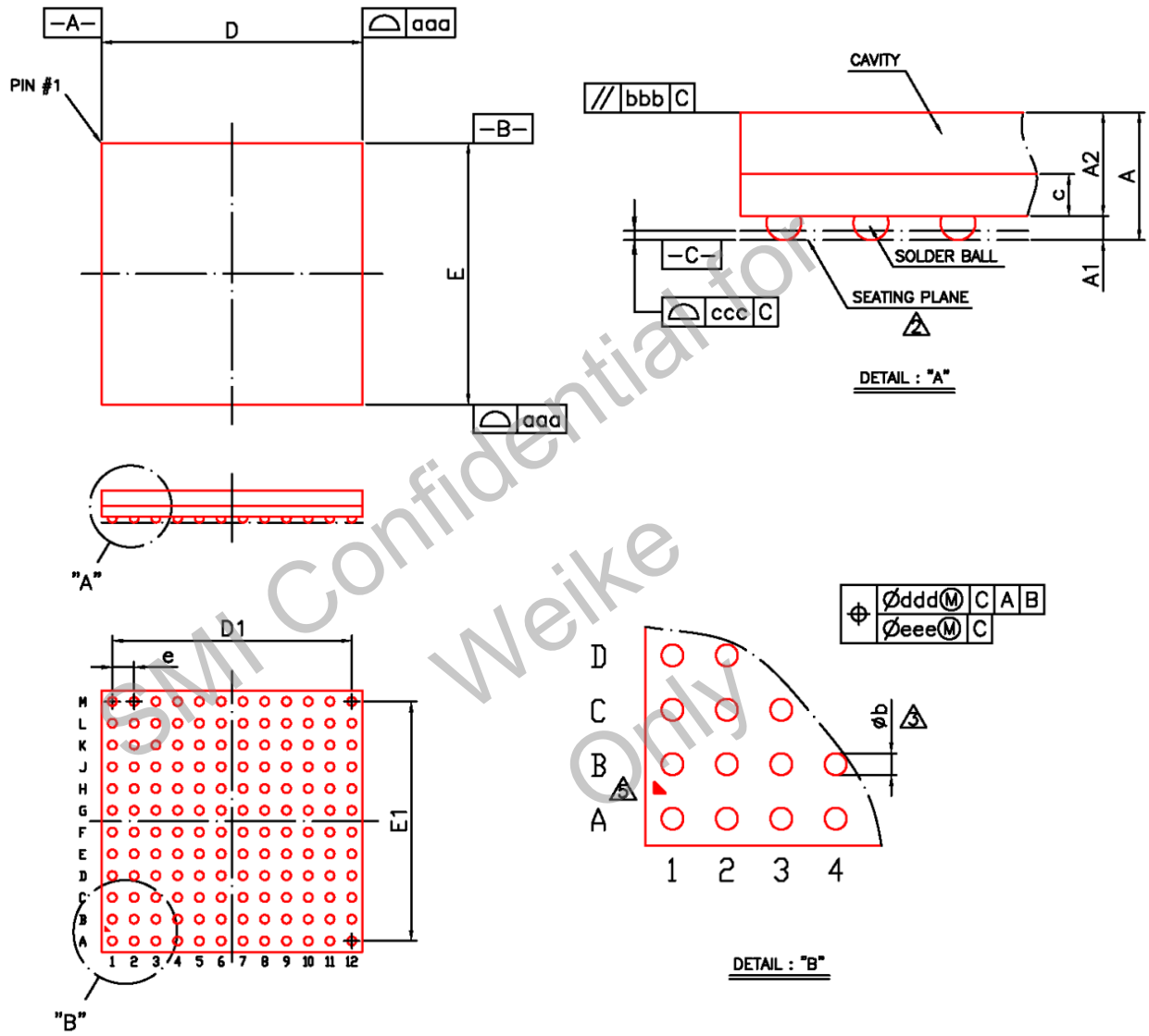


Figure 14: NV-DDR2 Data Input (Read) Cycle Timing



4. Package Information

Figure 15: 144-Ball TFBGA Package (9x9mm)



Symbol	MIN	NOM	MAX	Symbol	MIN	NOM	MAX
A	---	---	1.20	e	---	0.75	---
A1	0.16	0.21	0.26	b	0.25	0.30	0.35
A2	0.84	0.89	0.94	aaa	0.10		
c	0.32	0.36	0.40	bbb	0.20		
D	8.90	9.00	9.10	ccc	0.12		
E	8.90	9.00	9.10	ddd	0.15		
D1	---	8.25	---	eee	0.08		
E1	---	8.25	---	MD/ME	12/12		

Notes:
1. Controlling Dimension: Millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: bbb, ddd.
5. The pattern of Pin 1 fiducial is for reference only.
6. Reference Document: JEDEC Publication 95 Design Guide 4.5
7. Detail B is multi-pitch.

5. Product Ordering Information

5.1 Ordering Information

Table 13: Ordering Information

Ordering Number	Operating Temperature	Package Description
SM225GX0900XT-XX	0°C ~ 70°C	144-ball BGA, 9x9x1.2 (mm)

Note: The suffix “XX” denotes the IC revision.

5.2 Top Marking

Figure 16: Top Marking