3D Gen6 X4 1Tb 4-Plane NAND Flash Die

August 19, 2023,
Advance, Revision 1.0

Part Numbers

SKU
SDWFR-1T00B64JEC

DRAFT Rev. 1.0 8/19/23

SanDisk®
a Western Digital brand

Product Overview

SanDisk® 3D Gen6 X4 1Tb 4-Plane NAND Flash memory is available in wafer form for customers requiring post processing. Die specifications and dimensions are provided in this data sheet. For detailed device operation characteristics, see the SanDisk 3D Gen6 X4 1Tb 4-Plane NAND Flash package data sheet.

Die Features

Table 1: 1Tb Die Features

Feature		General Physical Specifications
Four-bits-per-cell (4bpc) technology		Backside die surface: Polished bare silicon
Power supply voltage: 3.3V (2.35V–3.6V)[1]		Processed wafer thickness: 785µm ± 25µm[2]
I/O Supply Voltage: 1.2V (1.14–1.30V)		Bond pad metalization: Al
Organization		Bond pad metalization thickness: 0.72µm
Page size	18,976 bytes	Passivation: SiO2/SiN/Polyimide
Block size:	QLC: 50.625MB	Passivation thickness: 5.1µm
	SLC: 12.65625MB	
Device size:	1Tb = 699 blocks/plane	
		Die Database and Die Outline
		Die size: 12.697mm × 5.375mm[3]
		Scribe line: X: 70µm × Y: 70µm
		Pads per die: 65
		Ordering information:
		SDWFR-1T00B64JEC

Note 1. Voltages are measured at their respective pads, balls, or pins.
2. Wafer form only.
3. Including scribe line.

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Erase Before Initial Program Operation

The device might not be erased prior to shipment. This is done to protect the device in the event that the device will be subjected to IR reflow for the SMT process. If the cells are erased at the factory, the reflow process could cause cell degradation and/or make the device susceptible to data-retention failures.

SanDisk strongly recommends that prior to the reflow process, the host should erase only the blocks intended to be programmed.

When it is necessary to perform a firmware download ***before*** SMT:

- Do not erase the entire NAND Flash device.
- Perform a bad-block scan.
- Only erase those blocks that are needed to hold the firmware.
- After the firmware is downloaded, the device can go through SMT.
- When starting the normal operation of the device, do not erase the entire NAND Flash before starting. Over the lifetime of the device, only erase blocks just prior to programming them.

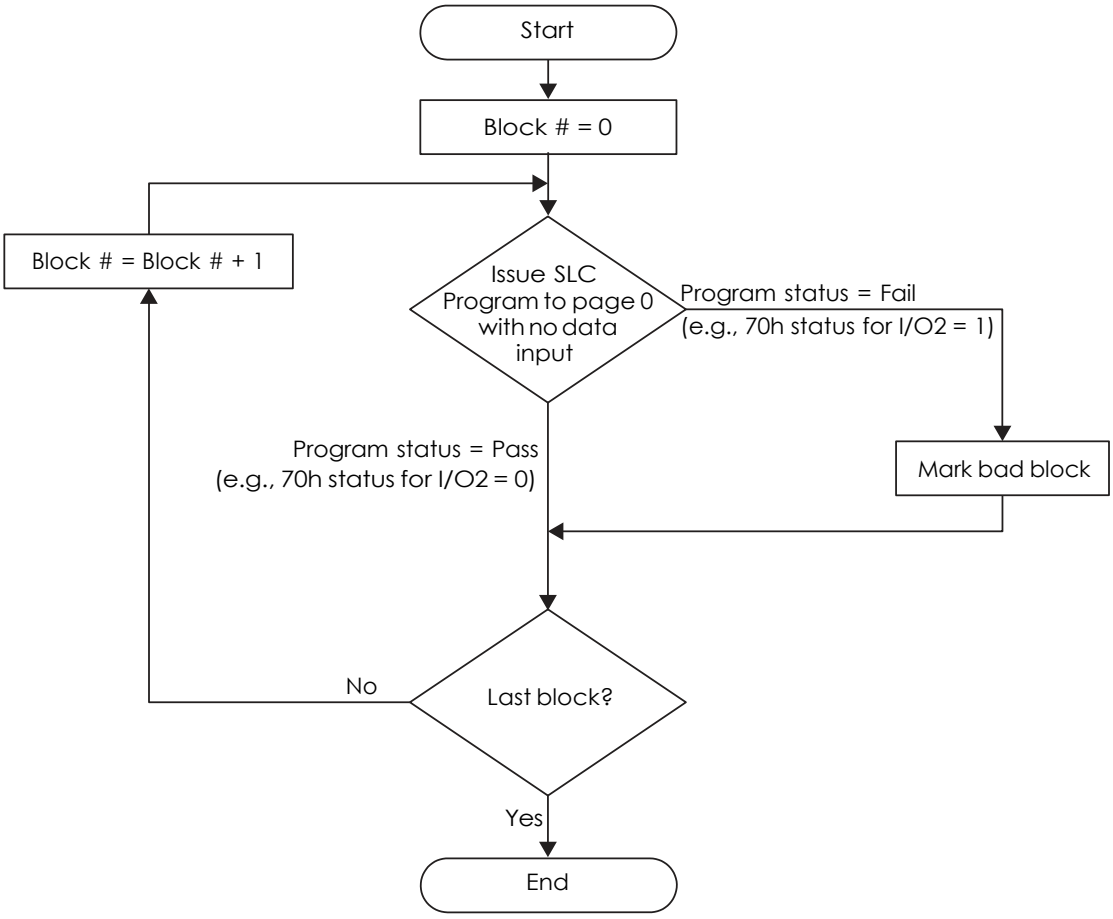
When it is necessary to perform a firmware download ***after*** SMT:

- Do not erase the entire NAND Flash device.
- The device can go through SMT.
- Perform a bad block scan.
- Only erase those blocks that are needed to hold the firmware.
- When starting the normal operation of the device, do not erase the entire NAND Flash before starting. Over the lifetime of the device, only erase blocks just prior to programming them.

Following the bad-block test, it is advisable to create a bad-block table to be used by the system software for mapping around any bad blocks.

For detailed specifications, commands, and operating modes, see the 3D Gen5 X4 1T 2-Plane NAND Flash package data sheet.

Figure 1: Bad Block Test Flow



Note 1. Following power-up, an FFh Reset is required before checking for bad blocks,

Functional Specifications

These specifications are provided for reference only. For detailed functional and parametric specifications, please refer to the package data sheet. Products and specifications are subject to change by SanDisk without notice.

Die Dimensions and Physical Specifications

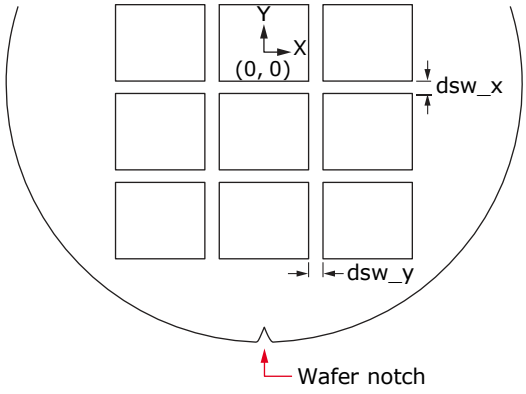
Table 2: Die Characteristics, Dimensions, and Specifications

Characteristic	Specification
Wafer diameter	300mm (12")
Wafer thickness	785µm ± 25µm
Die size	12.697mm × 5.375mm (including scribe line)
Pad size	See Table 5 on page 7
Pads per die	65
Die backside material	Bare silicon
Die backside finishing	Polished/bare silicon
Die backside potential	V_{SS} (GND)
Bond pad metalization	Al
Bond pad metalization thickness	0.72µm
Passivation	SiO2/SiN/Polyimide
Passivation thickness	5.1µm

Table 3: Die Street Widths

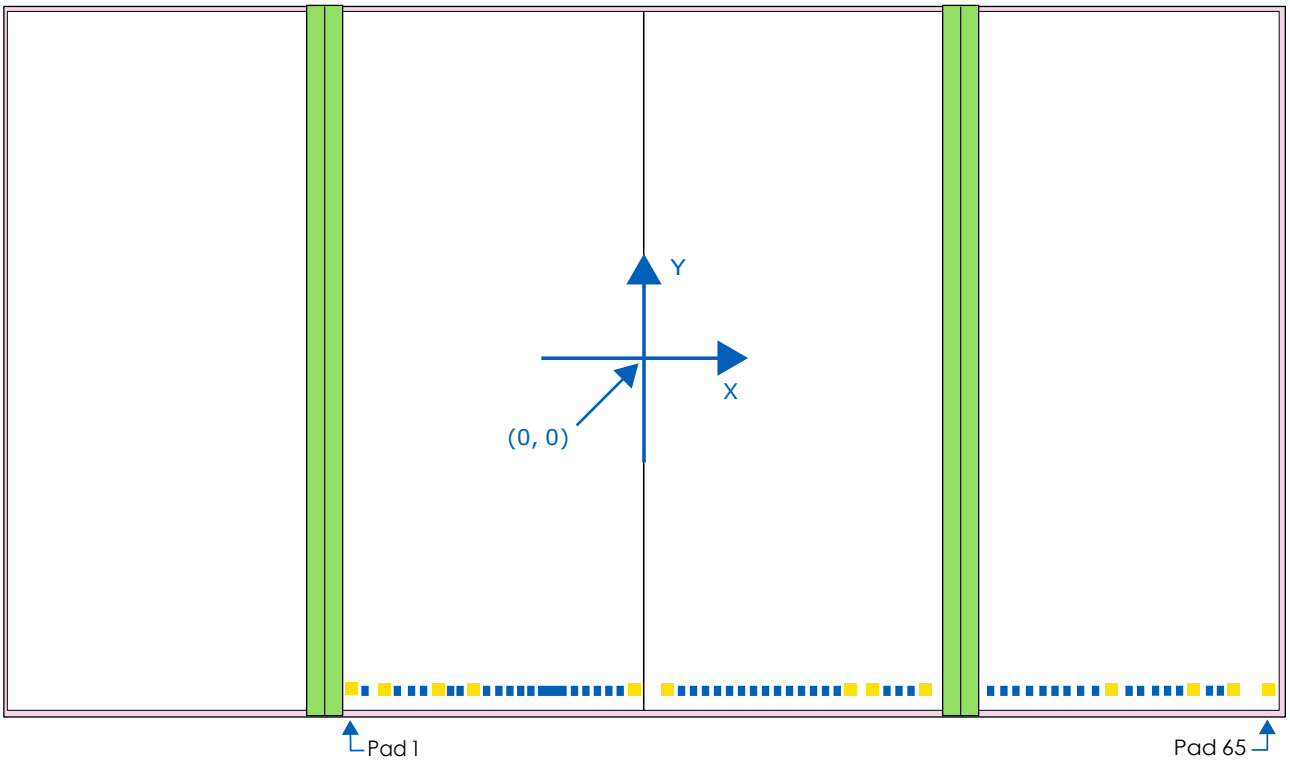
Street	Value	Unit
X-axis die street width (dsw_x)	70	µm
Y-axis die street width (dsw_y)	70	µm

Figure 2: Wafer Die Orientation



Pad Assignments

Figure 3: Floor Plan



Drawing not to scale. Pad locations are approximate, and for general illustration only.

Giant (G) Normal (N-1)

Note 1. See Table 4, "Pad Coordinates at Centers of Pads," on page 6 for pad locations.

Table 4: Pad Coordinates at Centers of Pads

Pad #	Pad Type	Pad Name	X from Center	Y from Center
1	G	V_{SS}	–5650.4	–2574.5
2	N-1	V_{CC}	–5551.8	–2565.2
3	G	V_{CC}	–4602.9	–2574.5
4	N-1	V_{SS}	–4516.2	–2565.2
5	N-1	Option	–3672.0	–2582.5
6	N-1	NC	–3563.4	–2582.5
7	G	V_{CC}	–3427.8	–2574.5
8	N-1	V_{CCQ}	–3310.8	–2565.0
9	N-1	ZQ	–3160.3	–2575.0
10	G	V_{SS}	–3026.4	–2574.5
11	N-1	V_{SS}	–2691.4	–2582.5
12	N-1	I/O7	–2546.5	–2578.5
13	N-1	V_{CCQ}	–2341.4	–2569.0
14	N-1	I/O6	–2136.3	–2578.5
15	N-1	V_{SS}	–1991.4	–2582.5
16	N-1	I/O5	–1846.5	–2578.5
17	N-1	V_{CCQ}	–1641.4	–2569.0
18	N-1	I/O4	–1436.3	–2578.5
19	N-1	V_{SS}	–1291.4	–2582.5
20	N-1	NC	–1146.5	–2578.5
21	N-1	V_{CCQ}	–941.4	–2569.0
22	N-1	REn	–835.2	–2582.5
23	N-1	RE	–711.3	–2582.5
24	G	V_{SS}	–595.1	–2574.5
25	G	V_{CC}	377.4	–2574.5
26	N-1	V_{CCQ}	494.4	–2565.0
27	N-1	V_{SS}	591.4	–2582.5
28	N-1	DQS	763.3	–2578.5
29	N-1	V_{CCQ}	941.4	–2569.0
30	N-1	DQSn	1146.5	–2578.5
31	N-1	V_{SS}	1291.4	–2582.5
32	N-1	I/O3	1436.3	–2578.5
33	N-1	V_{CCQ}	1641.4	–2569.0
34	N-1	I/O2	1846.5	–2578.5
35	N-1	V_{SS}	1991.4	–2582.5
36	N-1	I/O1	2136.3	–2578.5
37	N-1	V_{CCQ}	2341.4	–2569.0
38	N-1	I/O0	2546.5	–2578.5
39	N-1	V_{SS}	2691.4	–2582.5
40	G	V_{SS}	2790.6	–2574.5

Table 4: Pad Coordinates at Centers of Pads (cont'd)

Pad #	Pad Type	Pad Name	X from Center	Y from Center
41	G	V_{CC}	3224.4	–2574.5
42	N-1	CADD0	3325.4	–2568.0
43	N-1	CADD1	3425.4	–2568.0
44	N-1	CADD2	3515.4	–2568.0
45	G	WPn	3604.4	–2574.5
46	N-1	WEn	3737.9	–2565.6
47	N-1	ALE	3847.9	–2565.6
48	N-1	CLE	3956.1	–2565.6
49	N-1	V_{CCQ}	4050.7	–2565.6
50	N-1	V_{SS}	4127.7	–2564.8
51	N-1	V_{REF}	4224.7	–2565.6
52	N-1	Option	4325.4	–2565.6
53	N-1	Option	4400.4	–2565.6
54	N-1	CEn	4498.2	–2565.6
55	G	NC	4664.0	–2574.5
56	N-1	Option	4808.8	–2568.4
57	N-1	Option	4896.4	–2565.2
58	N-1	Option	4986.9	–2565.6
59	N-1	R/Bn	5092.0	–2565.6
60	N-1	V_{SS}	5191.7	–2565.6
61	G	V_{CC}	5275.0	–2574.5
62	N-1	NC	5444.6	–2582.5
63	N-1	V_{CC}	5555.5	–2582.5
64	G	V_{SS}	5655.0	–2574.5
65	G	NC	6184.4	–2574.5

Note 1. Tinted rows are simply to assist in locating where you are in the table.

Table 5: Bond Pad Types

Pad Type	Pad Size (passivation opening)	
	X [µm]	Y [?m]
Normal (N-1)	60	64
Giant (G)	80	80

Table 6: Ball/Pin Functions

Pin Name	Type	Ball/Pin Function
ALE	Input	**Address Latch Enable** controls the activating path for addresses to internal address registers. Addresses are latched on the rising edge of WEn, ALE high.
CEn	Input	**Chip Enable** controls device selection. When the device is busy, CEn high is ignored, and the device does not return to standby mode following program or erase operations.
CLE	Input	**Command Latch Enable** controls the activating path for commands to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WEn signal.
ODTn[1]	Input	**On-Die Termination** enables this device to turn termination resistance on or off for each I/O, RE, REn, DQS, and DQSn pin.
RE[2]	Input	**Read Enable Complement** is reserved for Toggle Mode DDR2, DDR3, DDR4
REn	Input	**Read Enable** controls serial data out, and when active, drives data onto the I/O bus. Data is valid after tDQSRE of the rising and falling edges of REn; it also increments the internal column address counter by one for each edge.
WEn	Input	**Write Enable** controls writes to the I/O port. Commands and addresses are latched on the rising edge of the WEn pulse.
WPn[1]	Input	**Write Protect** provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WPn pin is active low. It can also be set as a control pin for WPn or ODTn.
DQS[2]	Input/Output	**Data Strobe** acts as an output when reading data, and as an input when writing data. DQS is edge-aligned with data read; it is center-aligned with data written.
DQSn[2]	Input/Output	**Data Strobe Complement** is reserved for Toggle Mode DDR2, DDR3, DDR4
I/O[7:0]	Input/Output	**Data Input/Output (I/O)** inputs commands, addresses, and data, and outputs data during Read operations. The I/O pins float to High-z when the chip is deselected or when outputs are disabled.
ZQ	Input/Output	ZQ is the reference pin for ZQ calibration
R/Bn	Output	**Ready/Busy** indicates device operation status. R/Bn is an open-drain output and does not float to High-z when the chip is deselected or when outputs are disabled. When low, it indicates that a program, erase, or random read operation is in process; it goes high upon completion.
V_{CC}[3]	Supply	Power supply for the device
V_{CCQ}[3]	Supply	I/O power for input and output signals
V_{PP}	Supply	Optional, high-voltage, external power supply
V_{REF}[2]	Supply	Reference voltage. Reserved for CTT-interface operation only.
V_{SS}, V_{SSQ}[3]	Supply	Ground
NC	—	No Connect

Note 1. The ODTn and WPn pins are user-selectable, to be used as a control pin for ODTn or WPn using the Set Features command with address C0h. The default setting is WPn.

2. Toggle Mode DDR2, DDR3, DDR4 = DDR interface with DQS + V_{REF} and/or ODT and complementary signals.

3. Connect all V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} pins of each device to common power supply outputs. Do not leave any power pins unconnected.

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Wafer Handling and Storage Requirements

SanDisk die products are packaged for shipping in a clean room environment. Upon receipt, customers should transfer the die or wafers to a similar environment for storage.

SanDisk recommends that customers adhere strictly to the cautions listed below. Failure to do so will result in irreparable damage to the devices.

Caution: Avoid exposing NAND Flash die products to ultraviolet light

Caution: Avoid processing the die at temperatures greater than 250°C for more than five minutes.

SanDisk also recommends that die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ± 10% relative humidity. The storage facility temperature should be maintained at 25°C ± 20%.

Caution: Customers must take the necessary precautions to avoid ESD damage during handling. The die must be in an ESD-protected environment for inspection and assembly at all times.

Revision History

Table 7: Revision History

Status	Rev. #	Date	Changes
Preliminary	0.0	4/12/22	Initial DRAFT release
Preliminary	0.1	6/16/22	• Table 4, "Pad Coordinates at Centers of Pads," on page 6: Corrected pad names for pads 11 and 12
Advance	1.0	8/19/23	• Table 4, "Pad Coordinates at Centers of Pads," on page 6": —Corrected typographic error for pad 14, in column "X from Center" —Updated pad 51 pad name • Table 6, "Ball/Pin Functions," on page 8: —Added ODTn —Updated WPn function description —Updated V_{REF} symbol and function description —Inserted new note 1 and adjusted subsequent note reference numbers

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