FC3379

SuperSpeed USB 3.2 Gen 1 Flash Drive Controller Preliminary Datasheet

Ver 0.2

Revision

Beta 0.3

December.2021

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Revision History

Revision	Date	Description
0.1	Apr 10, 2021	Preliminary release
0.2	August 9, 2021	Beta Added QFN48,QFN36,QFN32 Pin assignments; Added Package outline Updated Signal Descriptions
0.3	December 28,2021	Updated QFN48,QFN32 VREF Pin

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1. Overview

1.1 Product Description

The FC3379 is a USB 3.2 Gen 1 single-channel Flash Drive Controller designed for value-line market. The controller offers the most flexible support for advanced technology node of 3D NAND. By integrating an embedded crystal and other components, the FC3379 can reduce customer overall cost at a system level.

With the powerful ECC engine which can overcome read/write disturbances, the flash drive controller fully supports the new generation 3D TLC/QLC while also ensuring data accuracy and integrity. The FC3379 is available in QFN48/QFN36/QFN32 green packages and die form with manufacturing-ready turnkey solution.

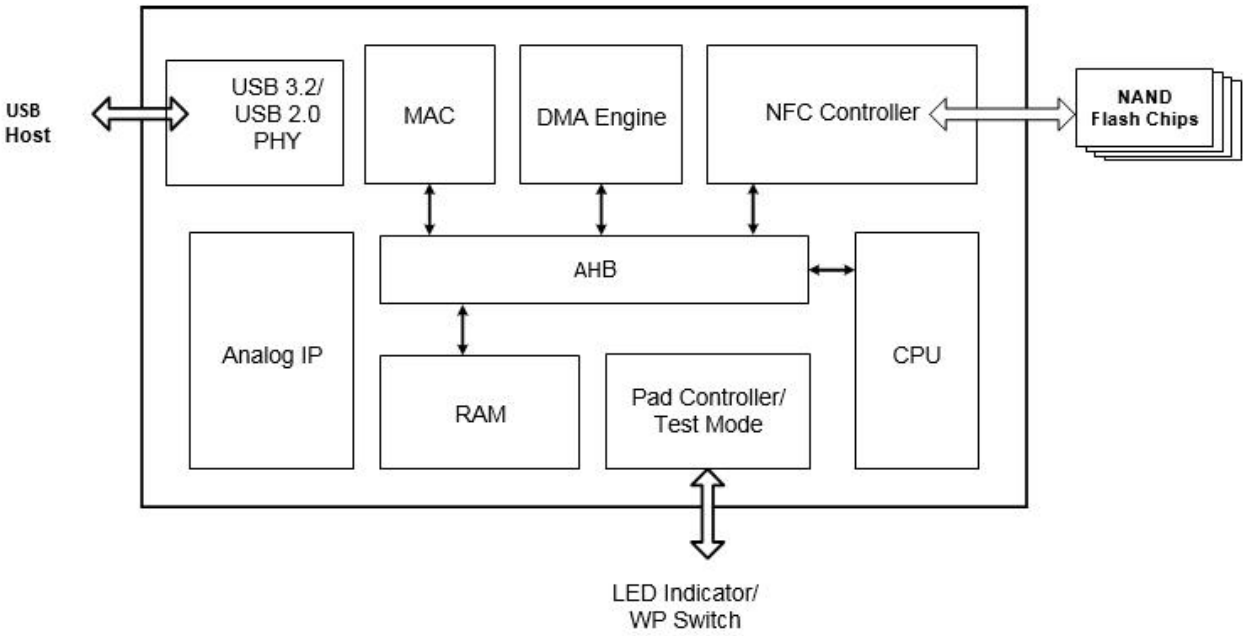
1.2 Key Features

- USB 3.2 Gen 1 SuperSpeed (5 Gbps) and USB High-Speed Interface
  - Compliant with USB 3.2 Specification Rev. 1.0
  - Compliant with USB 2.0 Specification Rev. 2.0
  - USB Mass Storage Class Specification Rev. 1.0
  - USB Mass Storage Class Bulk-Only Transport Protocol
  - Supports USB 3.2 multi-level link power management
- NAND Flash Support
  - Single-channel Flash interface supports up to 4 NAND Flash devices (4CE)
  - Supports Micron 130 series NAND and beyond
  - Supports up to 4-way interleave
  - Configurable ECC engine
  - Supports 2D MLC with 16KB page
  - Supports 3D TLC/QLC with 16KB page
  - Supports Toggle/ONFI DDR NAND Flash
  - Supports 1.8V/1.2V Flash VCCQ
  - Supports 3.3V/2.5V Flash VCC
- Supports VID, PID, serial number, and vender information update
- Operating System Support
  - Windows 10/Windows 8/Windows 7
  - Mac OS 10.x
  - Linux kernel 2.4

- The crystal-less design offers lower BOM cost
- Low power 1.1V core operation
- Built-in 3.3V/2.5V/1.8V/1.2V voltage regulators
- Supports LED indicator to indicate the access status
- Package
  - 48-pin QFN
  - 36-pin QFN
  - 32-pin QFN
  - Die Form
  - Lead-free and RoHS compliant

1.3 Block Diagram

Figure 1: FC3379 Block Diagram



2. Pin Assignments and Signal Descriptions

2.1 Pin Assignments

Figure 2: 48 -Pin QFN Pin Assignments (Top View)

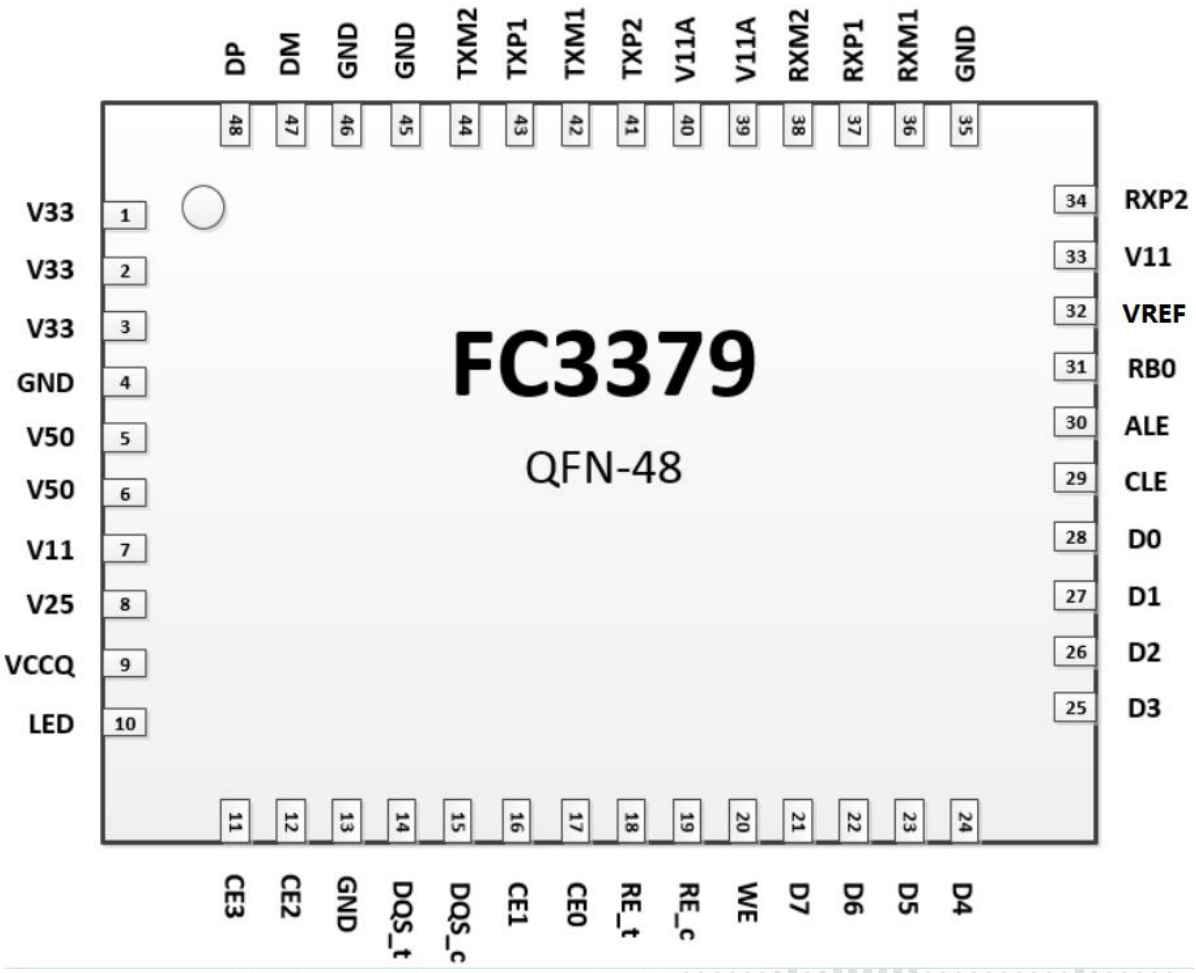


Figure 3: 36 -Pin QFN Pin Assignments (Top View)

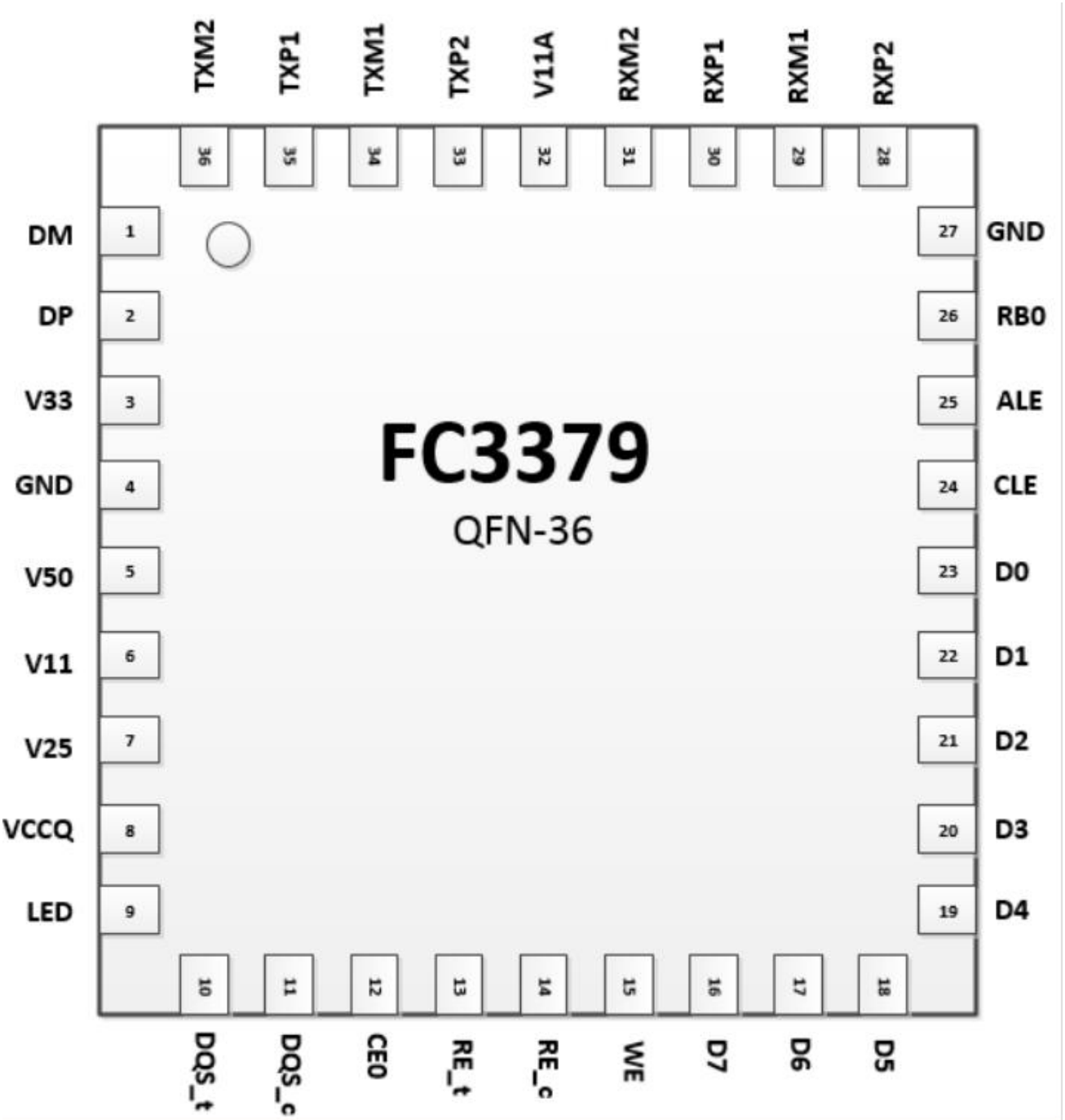
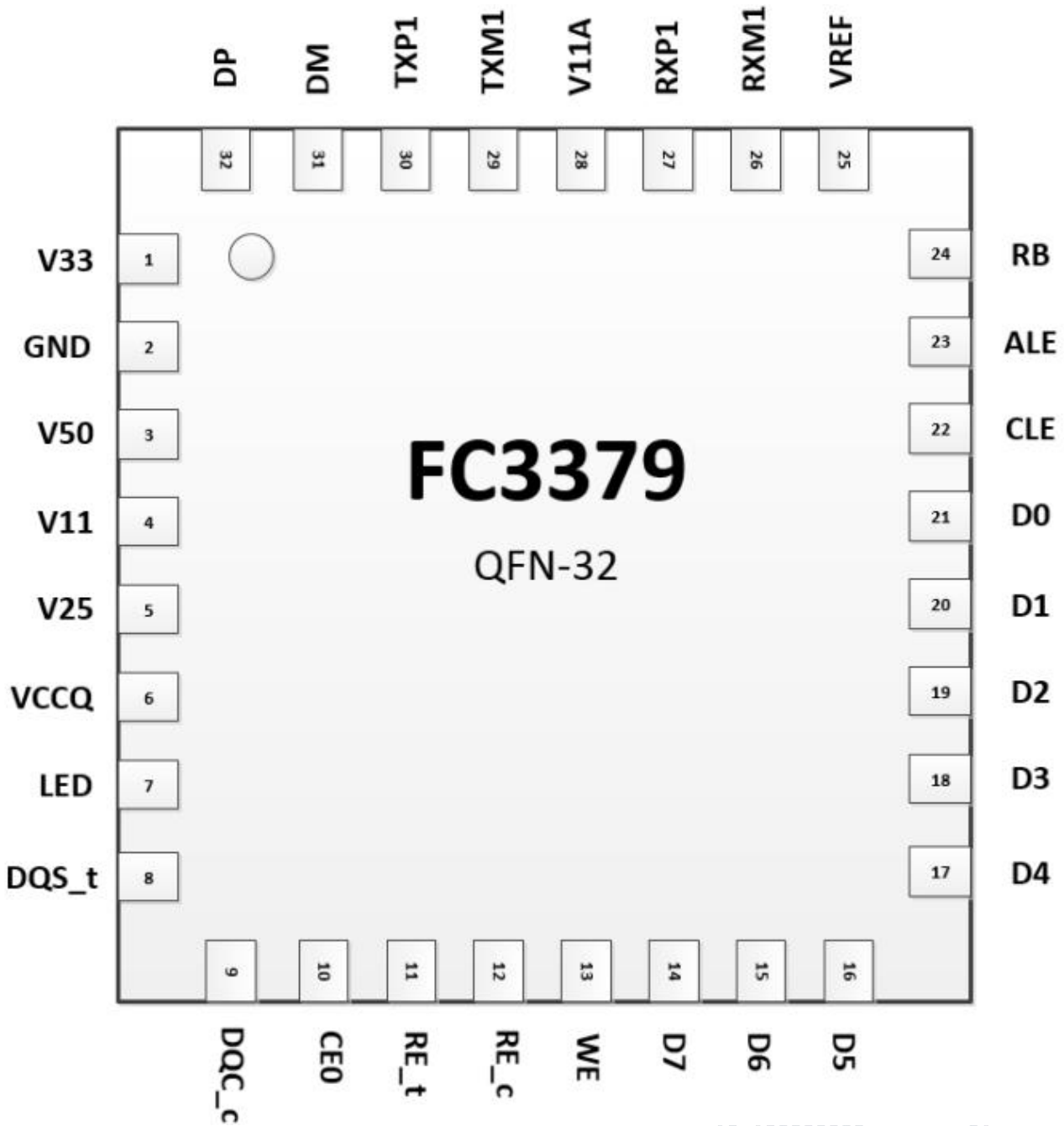


Figure 4: 32 -Pin QFN Pin Assignments (Top View)



2.2 Signal Descriptions

Table 1: FC3379 Signal Descriptions

Signal	Type	48-QFN	36-QFN	32-QFN	Description
V33	PWR	1			3.3V analog supply voltage
V33	PWR	2	3	1	Regulator 3.3V Power output
V33	PWR	3			Regulator 3.3V Power output
GND	GND	4	4	2	Digital Core Ground
V50	PWR	5	5		5.0V analog supply voltage
V50	PWR	6		5	5.0V analog supply voltage
V11	PWR	7	6	4	Digital Core Power 1.1V
V25	PWR	8	7	5	2.5V supply voltage
VCCQ	PWR	9	8	6	VIO digital supply voltage for the NANDFLASH VCCQ: 5 stage: 3.3/2.5/1.8/1.2/0V
LED	O	10	9	7	USB LED Indicator
CE3	I/O	11			Flash Chip Enable 3
CE2	I/O	12			Flash Chip Enable 2
GND	GND	13			Digital Core Ground
DQS_t	I/O	14	10	8	Flash Data Strobe
DQS_c	I/O	15	11	9	Flash Data Strobe Complement (active low)
CE1	I/O	16			Flash Chip Enable 1
CE0	I/O	17	12	10	Flash Chip Enable 0
RE_t	I/O	18	13	11	Flash Read Enable (active low)
RE_c	I/O	19	14	12	Flash Read Enable Complement(active low)
WE	I/O	20	15	13	Flash Write Enable (active low)
D7	I/O	21	16	14	Flash Data Bus Bit 7
D6	I/O	22	17	15	Flash Data Bus Bit 6
D5	I/O	23	18	16	Flash Data Bus Bit 5
D4	I/O	24	19	17	Flash Data Bus Bit 4
D3	I/O	25	20	18	Flash Data Bus Bit 3
D2	I/O	26	21	19	Flash Data Bus Bit 2
D1	I/O	27	22	20	Flash Data Bus Bit 1
D0	I/O	28	23	21	Flash Data Bus Bit 0
CLE	I/O	29	24	22	Flash Command Latch Enable

Signal	Type	48-QFN	36-QFN	32-QFN	Description
ALE	I/O	30	25	23	Flash Address Latch Enable
RB0	I/O	31	26	24	Flash Ready/Busy Signal 0
VREF	I/O	32		25	Supply votage for flash vref
V11	PWR	33			Digital Core Power 1.1V
RXP2	I	34	28		USB 3.2 RX Data Positive Pin for TypeC
GND	GND	35	27		Digital Core Ground
RXM1	I	36	29	26	USB 3.2 RX Data Negative Pin
RXP1	I	37	30	27	USB 3.2 RX Data Positive Pin
RXM2	I	38	31		USB 3.2 RX Data Negative Pin for TypeC
V11A	PWR	39	32	28	1.1V analog supply voltage
V11A	PWR	40			1.1V analog supply voltage
TXP2	O	41	33		USB 3.2 TX Data Negative Pin for TypeC
TXM1	O	42	34	29	USB 3.2 TX Data Positive Pin
TXP1	O	43	35	30	USB 3.2 TX Data Positive Pin
TXM2	O	44	36		USB 3.2 TX Data Negative Pin for TypeC
GND	GND	45			Digital Core Ground
GND	GND	46			Digital Core Ground
DM	I/O	47	1	31	USB 2.0 Data Negative Pin
DP	I/O	48	2	32	USB 2.0 Data Positive Pin

3. Electrical Characteristics

3.1 DC Characteristics

Table 2: Operation Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power Supply Voltage	VDD	0.99	1.1	1.21	V
1.8V Flash I/O Supply Voltage	VCCIOF	1.62	1.8	1.98	V
1.2V Flash I/O Supply Voltage	VCCIOF	1.08	1.2	1.32	V
USB 2.0 PHY 3.3V Input Voltage	VCCA	2.97	3.3	3.63	V
USB 3.1 PHY 1.2V Input Voltage	VPP	1.08	1.2	1.32	V
Regulator Power Supply Voltage	VCC5V	4.5	5	5.5	V
eFuse Program Voltage	VDDQ	2.25	2.5	2.75	V
eFuse Read Voltage	VDDQ	2.25	2.5	2.75	V
Operating Temperature	TOPR	-25		85	°C
Storage Temperature	TSTG	-40		+125	°C

Table 3: DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Regulator 5V Input Voltage	VCC5V	4.5	5	5.5	V
Regulator 3.3V Output Voltage	VCCAH	3.0	3.3	3.6	V
Regulator 2.5V Output Voltage	V25X	2.25	2.5	2.75	V
Regulator 1.8V Output Voltage	V18X	1.62	1.8	1.98	V
Regulator 1.1V Output Voltage	VDDX	0.9	1	1.1	V
Flash I/O Reference Voltage	VREF				V
All Input Leakage Current					μA
All Output Leakage Current					μA
Bus Line Capacitance	C_L				pF

3.2 Flash Interface AC Characteristics

3.2.1 Legacy NAND

Table 4: AC Timing Parameters for Legacy NAND

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS	TBD	TBD	ns
CLE Hold Time	tCLH	TBD	TBD	ns
ALE Setup Time	tALS	TBD	TBD	ns
ALE Hold Time	tALH	TBD	TBD	ns
Write Cycle Time	tWC	TBD	TBD	ns
WE Pulse Width	tWP	TBD	TBD	ns
WE High Hold Time	tWH	TBD	TBD	ns
Write Data Output Setup Time	tDS	TBD	TBD	ns
Write Data Output Hold Time	tDH	TBD	TBD	ns
Read Cycle Time	tRC	TBD	TBD	ns
RE Pulse Width	tRP	TBD	TBD	ns
RE High Hold Time	tREH	TBD	TBD	ns

Figure 5: Command Latch Cycle Timing

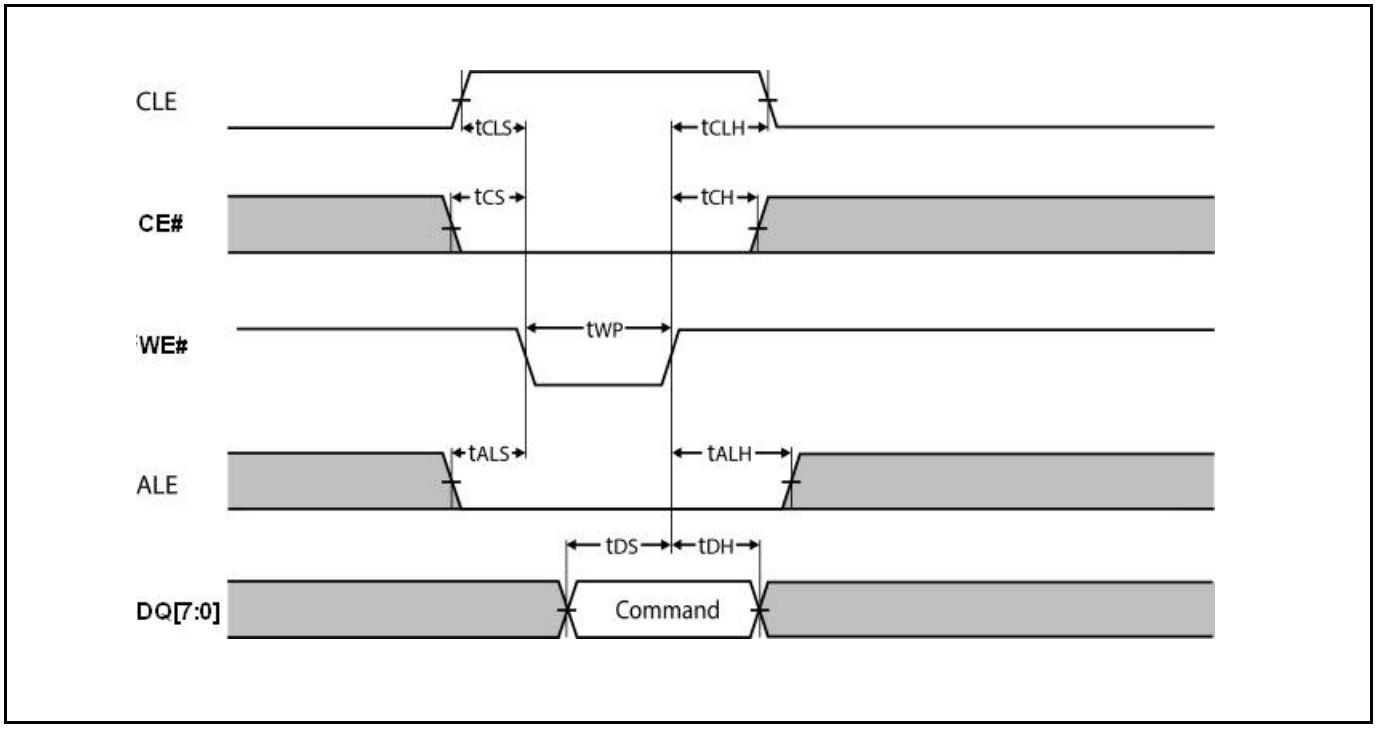


Figure 6: Address Latch Cycle Timing

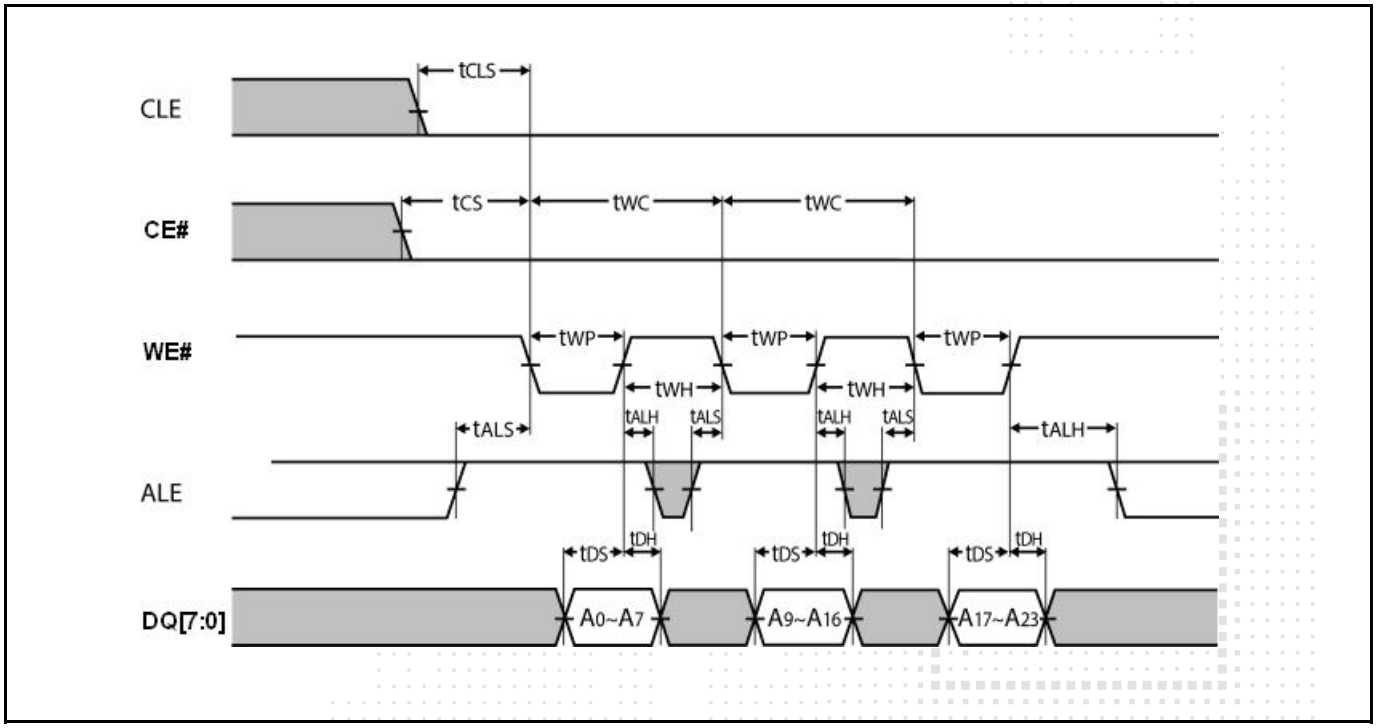


Figure 7: Input Data Latch Cycle Timing

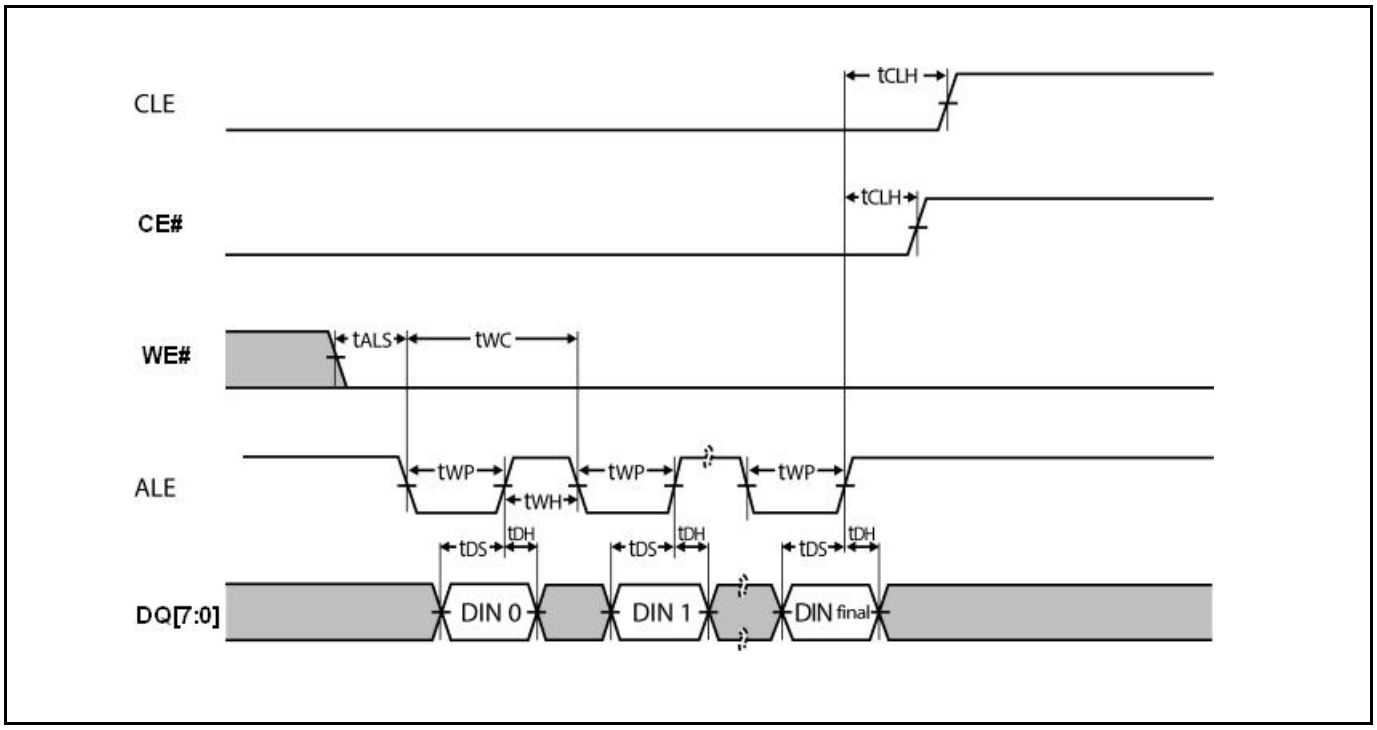
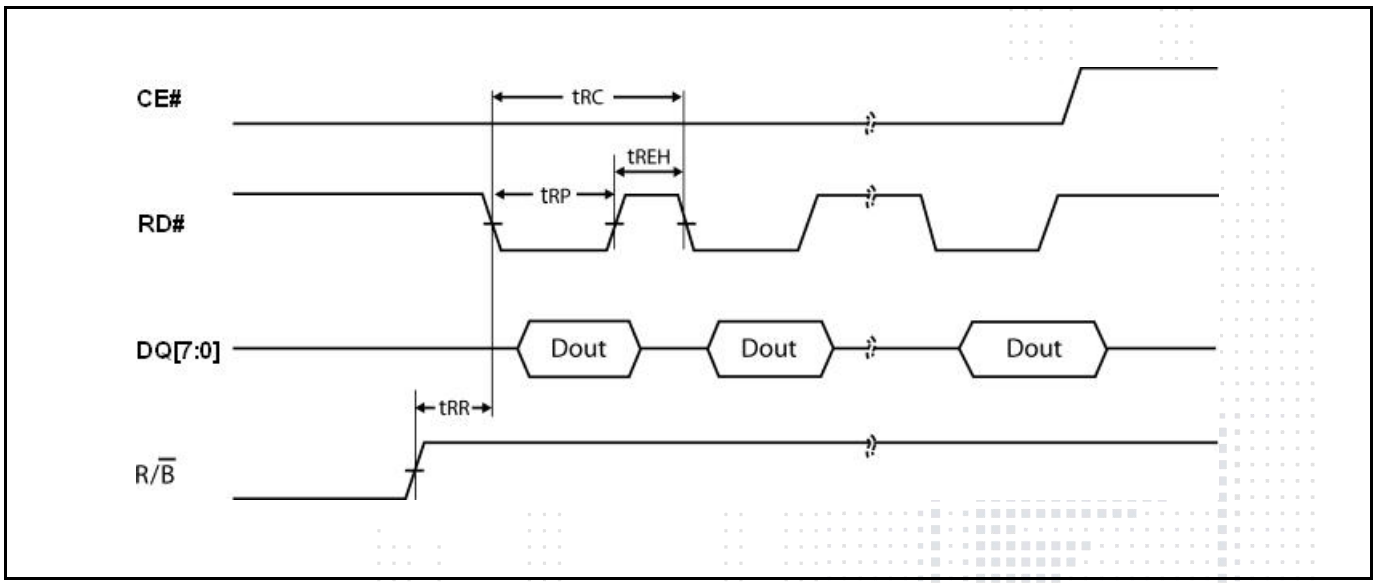


Figure 8: Serial Access Cycle after Read



3.2.2 Toggle NAND

Table 5: AC Timing Parameters for Toggle DDR NAND

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS	TBD	TBD	ns
CLE Hold Time	tCLH	TBD	TBD	ns
ALE Setup Time	tALS	TBD	TBD	ns
ALE Hold Time	tALH	TBD	TBD	ns
Command/Address Setup Time	tCAS	TBD	TBD	ns
Command/Address Hold Time	tCAH	TBD	TBD	ns
CE Setup Time	tCS	TBD	TBD	ns
Write Cycle Time	tWC	TBD	TBD	ns
WE Pulse Width	tWP	TBD	TBD	ns
WE High Hold Time	tWH	TBD	TBD	ns
Read Cycle Time	tRC	TBD	TBD	ns
RE Pulse Width	tRP	TBD	TBD	ns
RE High Hold Time	tREH	TBD	TBD	ns
DQS Data Strobe Output Cycle Time	tDSC	TBD	TBD	ns
DQS Output Pulse Width -- Low	tDQSL	TBD	TBD	ns
DQS Output Pulse Width -- High	tDQSH	TBD	TBD	ns

Data Output (Write) Setup Time	tDS	TBD	TBD	ns
Data Output (Write) Hold Time	tDH	TBD	TBD	ns
DQS Write Preamble	tWPRE	TBD	TBD	ns
DQS Write Postamble	tWPST	TBD	TBD	ns
DQS-DQ Skew, DQS to Last DQ Valid, Per Access	tDQSQ	TBD	TBD	ns
Data Input DQ (Read) Hold Skew Factor	tQHS	TBD	TBD	ns
Data Input Hold time (Refer to DQS Edge)	tQH	TBD	TBD	ns
DQ Input Data Valid Window	tDVW	TBD	TBD	ns
DQS Input Preamble for Read Operation	tRPRE	TBD	TBD	ns
DQS Input Postamble for Read Operation	tRPOST	TBD	TBD	ns
DQS Input Postamble Hold Time for Read Operation	tRPSTH	TBD	TBD	ns
RD to DQS/DQ Input Delay	tDQSRE	TBD	TBD	ns

Figure 9: Toggle NAND Command Latch Cycle Timing

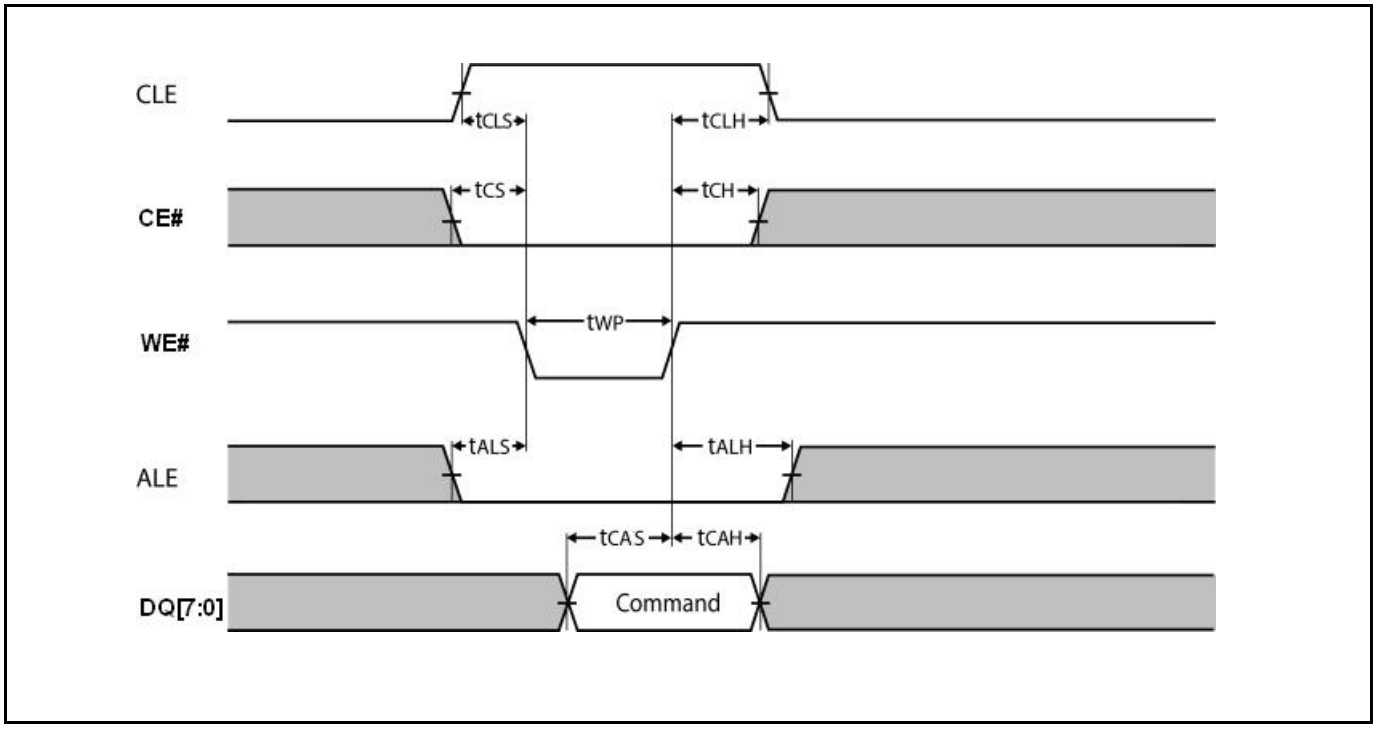


Figure 10: Toggle NAND Address Latch Cycle Timing

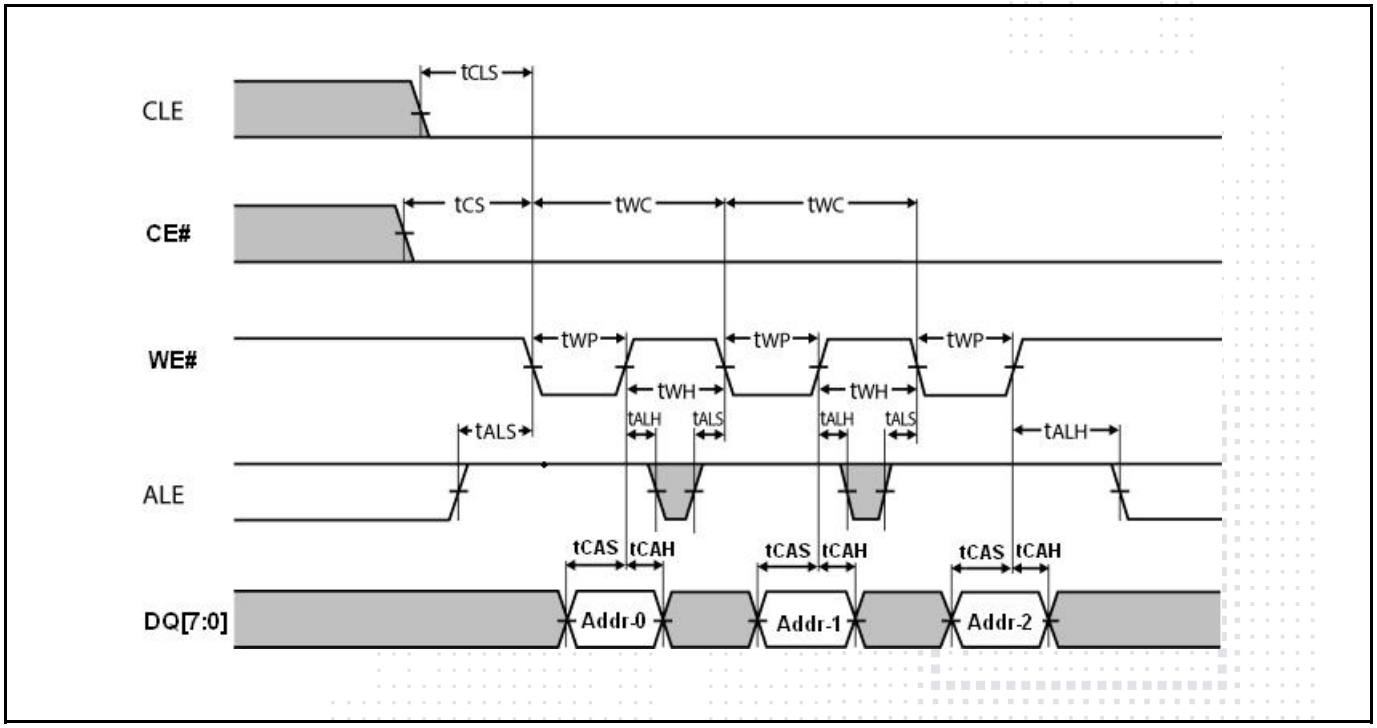


Figure 11: Toggle NAND Output Data (Write) Cycle Timing

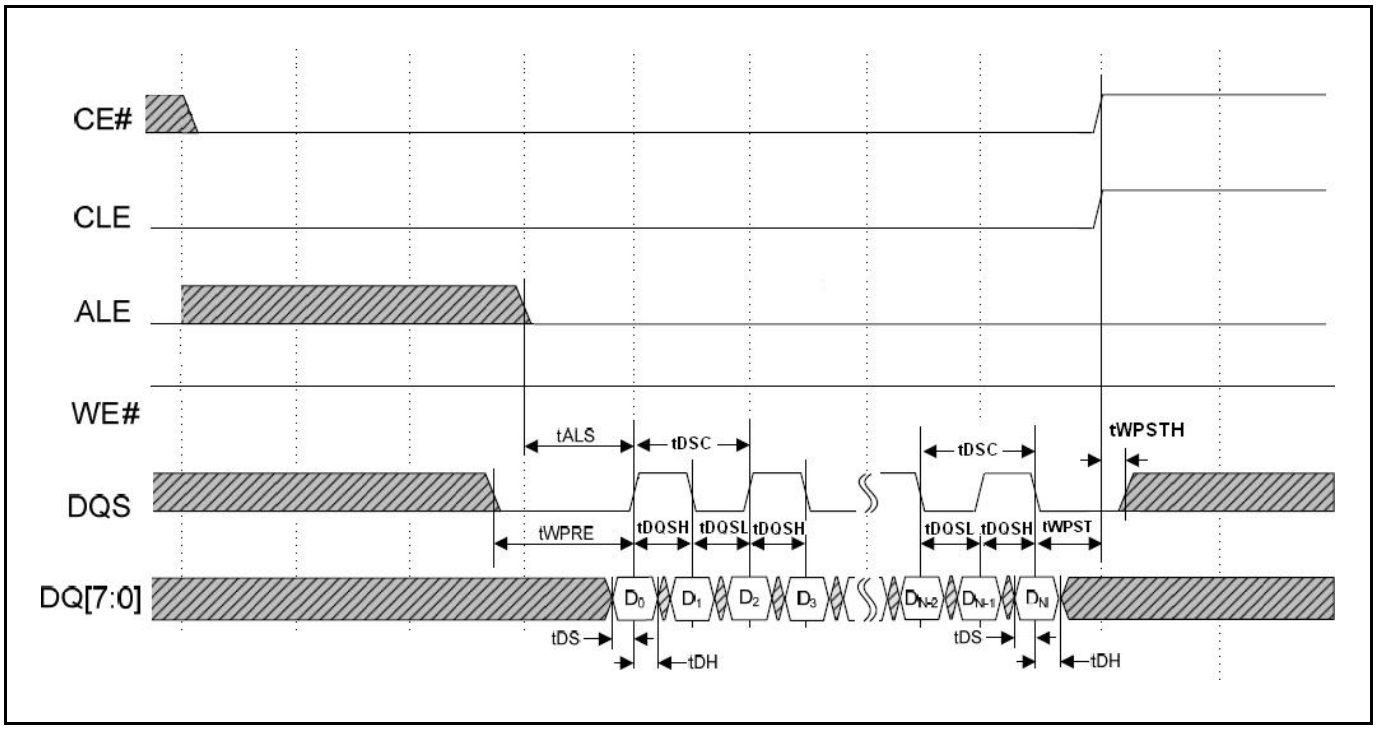
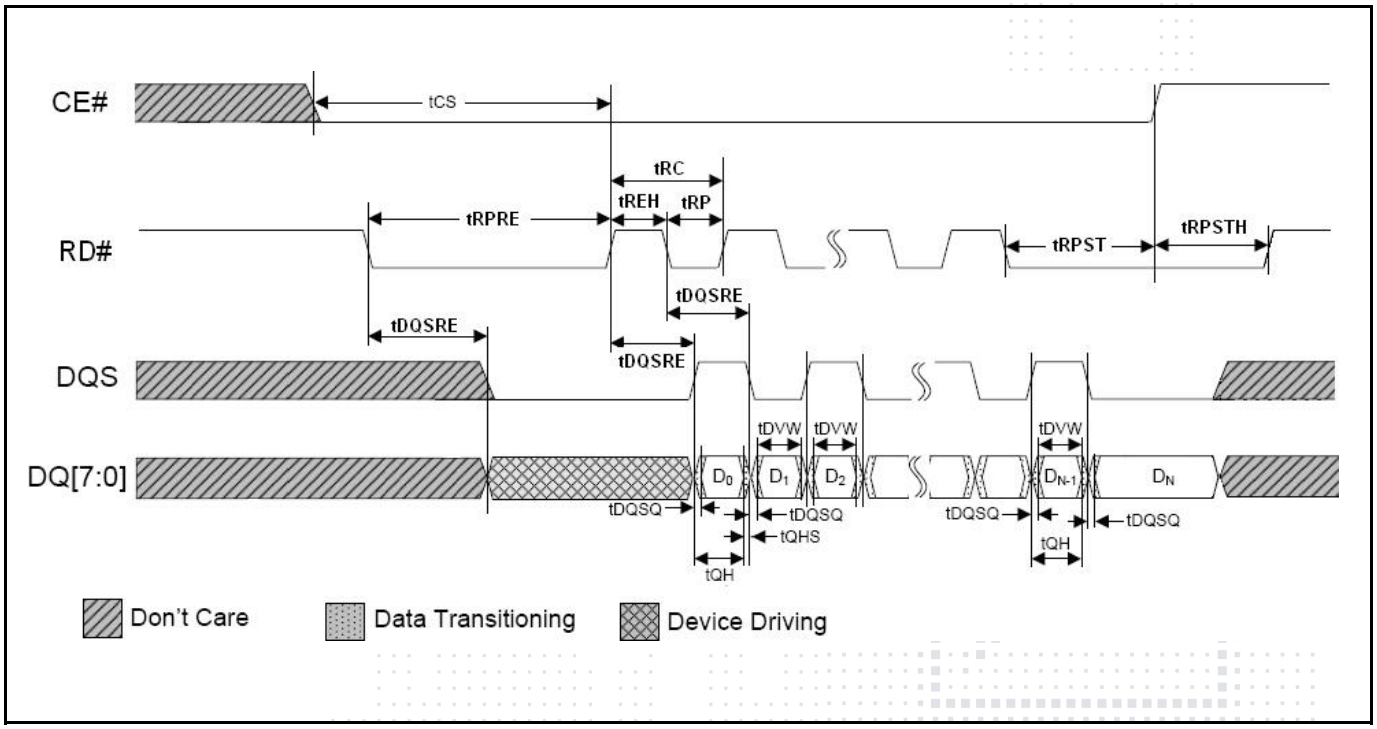
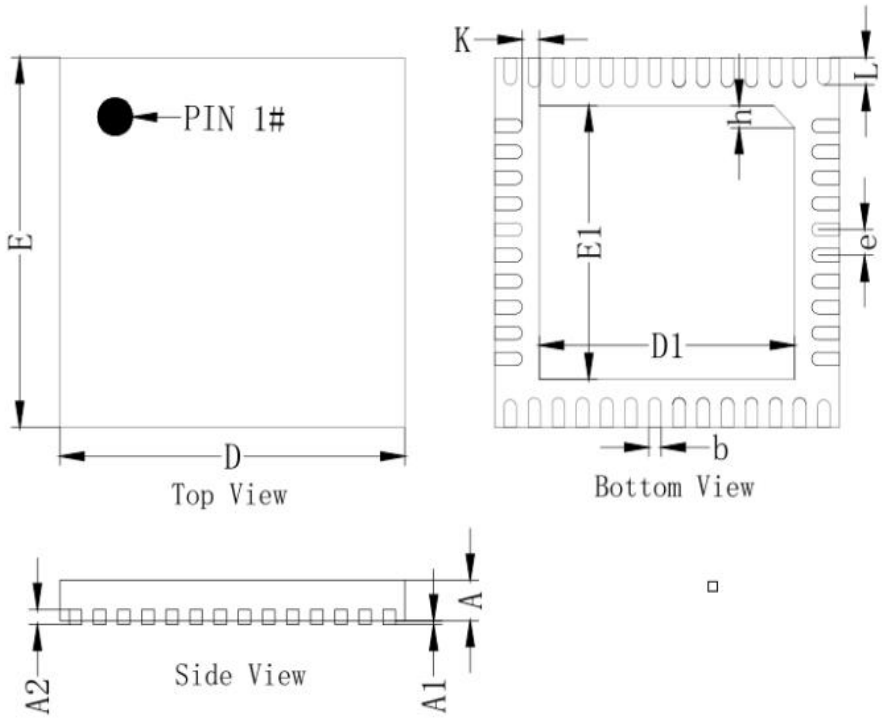


Figure 12: Toggle NAND Input Data (Read) Cycle Timing



4. Package Information

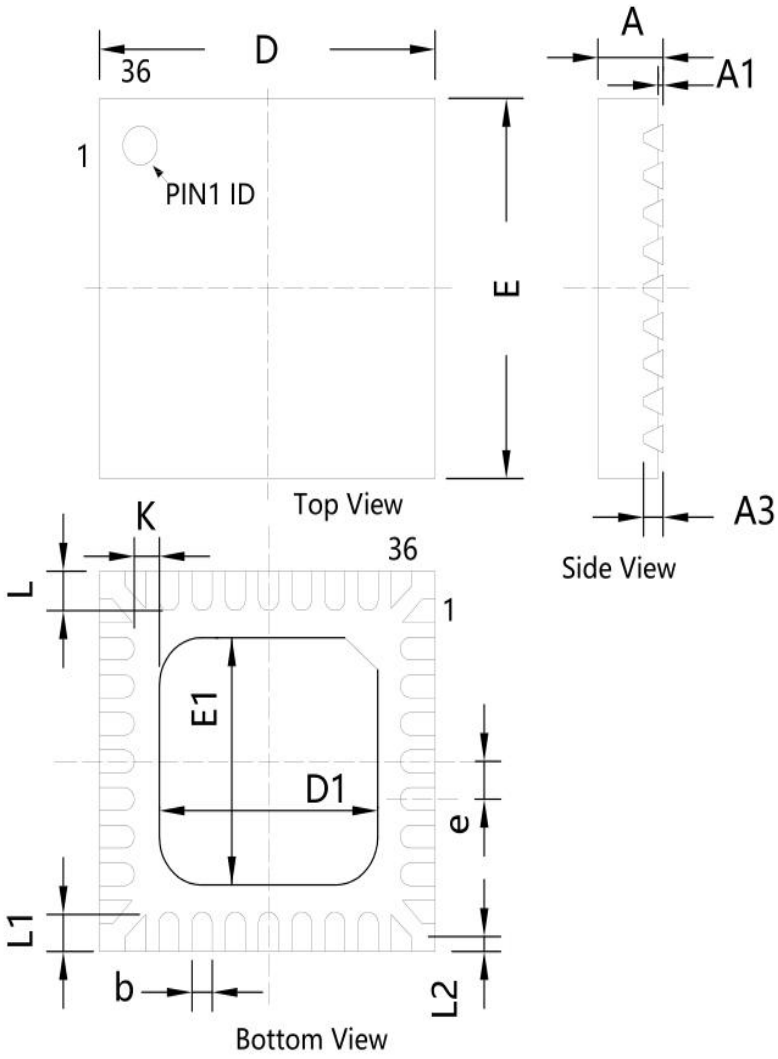
Figure 13: 48-Pin QFN Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETERS)

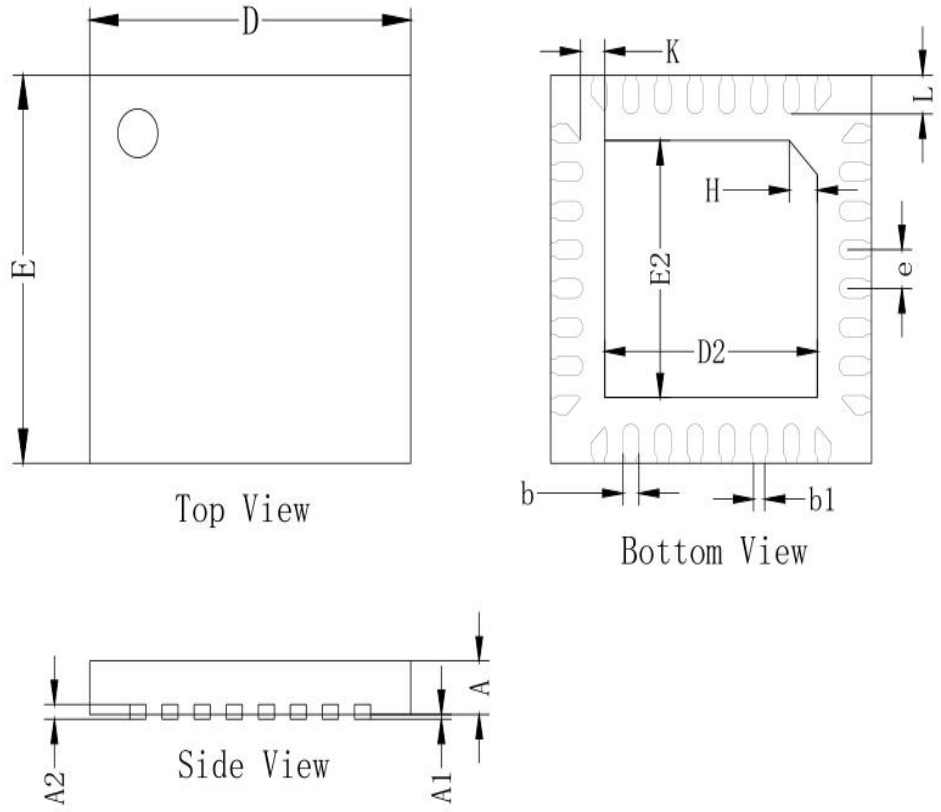
SYMBOL	MILLMETERS		
	MIN	NOM	MAX
A	0.55	0.60	0.65
A1	0.00	0.02	0.05
A2	0.203REF		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.65	3.70	3.75
E1	3.65	3.70	3.75
e	0.35BSC		
L	0.32	0.37	0.42
b	0.13	0.18	0.23
K	0.20	0.25	0.30
h	0.25	0.30	0.35

Figure 14: 36-Pin QFN Package Outline



尺寸 / 标注	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.152 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.50	2.60	2.70
E1	2.50	2.60	2.70
e	0.35 BSC		
K	0.30	-	-
L	0.30	0.40	0.50
L1	0.33	0.38	0.43
L2	0.15	0.20	0.25

Figure 15: 32-Pin QFN Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETERS)

SYMBOL	MILLMETERS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.152REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.55	2.65	2.75
E2	2.55	2.65	2.75
e		0.40BSC	
H		0.35REF	
L	0.35	0.40	0.45
K	0.25	0.30	0.35
b	0.15	0.20	0.25
b1		0.14REF	

5. Product Ordering Information

5.1 Ordering Information

Table 6: Ordering Information

Ordering Number	Operating Temperature	Package Type	Dimension
FC3379 XX5	-25℃ ~ 85 ℃	QFN 48PIN	5 *5*0.60(mm)
FC3379 XX4	-25℃ ~ 85 ℃	QFN 36PIN	4 *4*0.55(mm)
FC3379 XX6	-25℃ ~ 85 ℃	QFN 32PIN	4*4*0.55(mm)
FC3379 XX0	-25℃ ~ 85 ℃	Die Form	--

Note: The suffix “XX” denotes the IC revision.

5.2 Top Marking

Figure 16: FC3379 AA6 Top Marking (Example)