NAND Flash Memory- SpecTek Addendum

FBNB58R1T1KLBAHD4
FBNB58R2T1KLEAHD4
FBNB58R4T1KLMAHD4
FBNB58R8T1KLUAHD5

B58R Features

- Open NAND Flash Interface (ONFI) 5.0 compatible[1]
- JEDEC (JESD230E) NAND Flash Interface Interoperability compatible[2]
- Triple-level cell (TLC) technology
- Organization:
  - Page size x8: 18,352 bytes (16,384 + 1968 bytes)
  - Block size: 2784 pages, (44,544K + 5350.5K bytes)
  - Plane size: 6 planes x 567 blocks
  - Device size: 1Tb: 3402 blocks; 2Tb: 6804 blocks; 4Tb: 13,608blocks; 8Tb: 27,216 blocks
- NV-DDR3 I/O performance:
  - Up to NV-DDR3 time mode 15
  - Clock rate: 1.25ns (NV-DDR3)
  - Read/write throughput per pin: 1.6GT/s
- NV-LPDDR4 I/O performance:
  - Up to NV-LPDDR4 time mode 15
  - Clock rate: 1.25ns (NV-DDR3)
  - Read/write throughput per pin: 1.6GT/s
- TLC Array performance
  - IWL READ operation time: 55µs (TYP)
  - READ PAGE operation time: 61µs (TYP)
  - Effective program page time: 600µs (TYP)
  - Erase block time: 6ms (TYP)
- Operating Voltage Range
  - V_{CC}: 2.35–3.6V
  - V_{CCQ}: 1.14–1.26V
- Command set: ONFI NAND Flash Protocol
- V_{PP} not supported
- Data is required to be randomized by the external host prior to being inputted to the NAND device
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Minimum required ECC
  - TLC: LDPC to correct 1E-2 RBER
  - SLC: 60-bit ECC per 1147 bytes of data
- On-die Termination (ODT)[3]
- Copyback operations supported within the plane from which data is read
- Quality and reliability[4]
  - Testing methodology: JESD47
  - Data retention: Consult factory
  - Endurance: Product Grades AS
    - TLC Endurance: 1000 PROGRAM/ERASE cycles
    - SLC Endurance: 41,000 PROGRAM/ERASE cycles
  - Endurance: Product Grade AR
    - TLC Endurance: 500 PROGRAM/ERASE cycles
    - SLC Endurance: 21,000 PROGRAM/ERASE cycles
- Operating temperature: +10ºC to +70ºC
- Package:
  - 154-ball BGA
- This device is not intended for use in applications that require data to be pre-programmed in the NAND array prior to Reflow, Surface Mount, or any thermal processing. Please contact your Micron representative for details.
- Consult factory for approved controller list: https://www.spectek.com/menus/secure/flash_controllers.aspx)

Notes: 1. The ONFI 5.0 specification is available at http://www.onfi.org/
2. The JEDEC specification is available at www.jedec.org/standards-documents.
3. ODT functionality is supported.
4. Read Retry and Auto Read Calibration operations are required to achieve specified endurance and for general array data integrity.
5. For the definition of Gib, refer to IEEE 1541-2002 (www.ieee.org)

Part Numbering Information

SpecTek NAND Flash devices are available in several different configurations and densities (see Figure 1). Verify valid part numbers by using the part's catalog at www.micron.com. Contact the factory for devices not found.

Figure 1: Marketing Part Number Chart

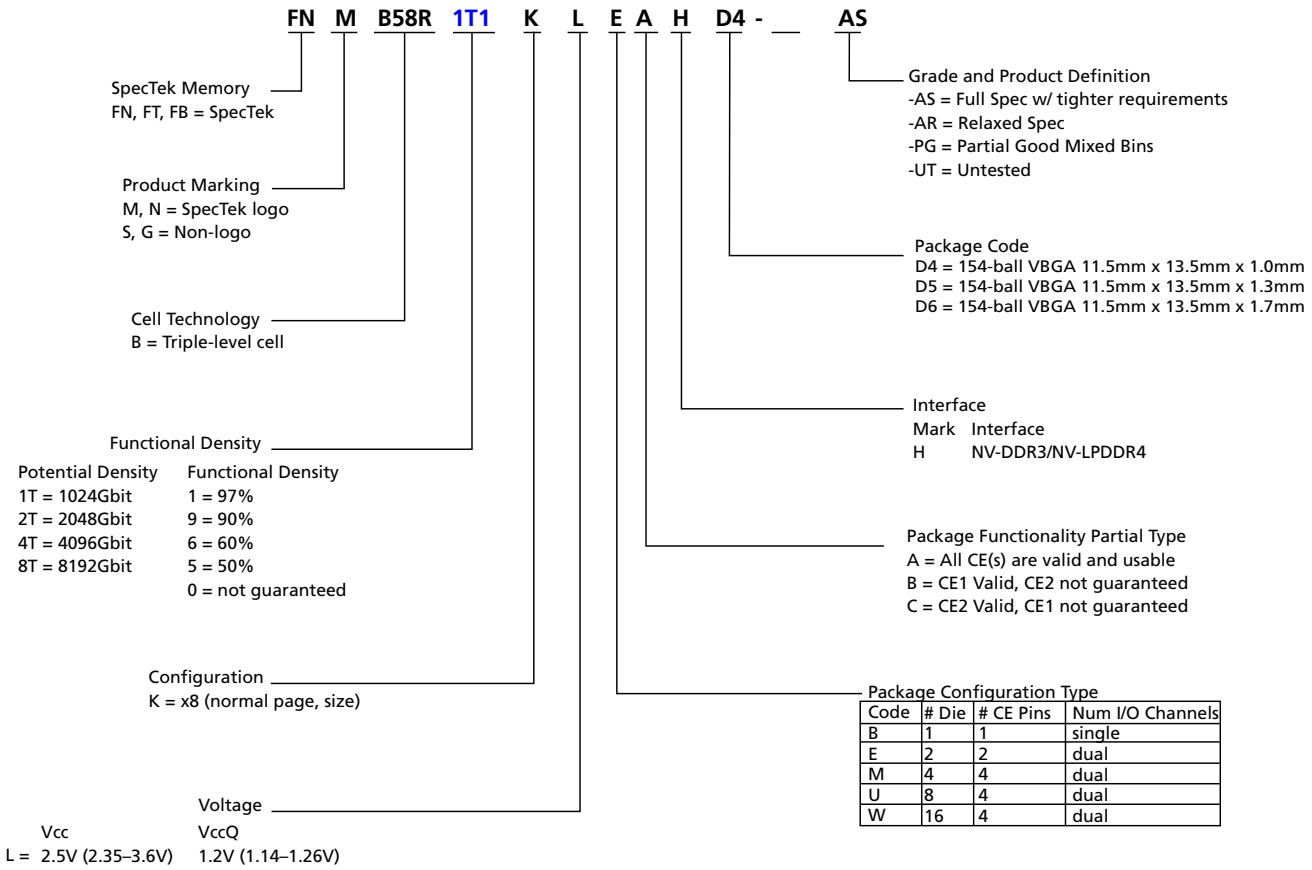

Table 1: Flash Product Grade Definitions

Product Grade	Name	Description
-AS	Full Specification	Product meets the full specifications with additional screening: Block 0 through 1 are valid, READ ID Byte 0 = 0x2C. Minimum Number Valid Blocks (NVB) per plane.
-AR	Relaxed Density	Product is allowed to have lower Valid Blocks (NVB) and ICC Standby current (CMOS). See Tech Note -- AR Grade for further details. Customer is expected to use an application that is able to scan/test remaining blocks.
-PG	Partial Good Mixed Bins	Product is untested with a variety of mixed defects including, but not limited to high ICC, bent leads, missing balls, package issue, visual defects, lower NVB count, etc. Also includes parts with less than 85% NVB. This data sheet is just for reference for basic functionality. For warranty information, see the SpecTek NAND Buyer's Guide (link).

Table 1: Flash Product Grade Definitions

Product Grade	Name	Description
-UT	Untested	Product is untested in package form, but originally passed die-level testing. For warranty information, see the SpecTek NAND Buyer's Guide (link).

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part is offered and valid by using the Parametric Part Search Web Site at: https://www.micron.com/support/sales-support. If the device required is not on this list, contact the factory.

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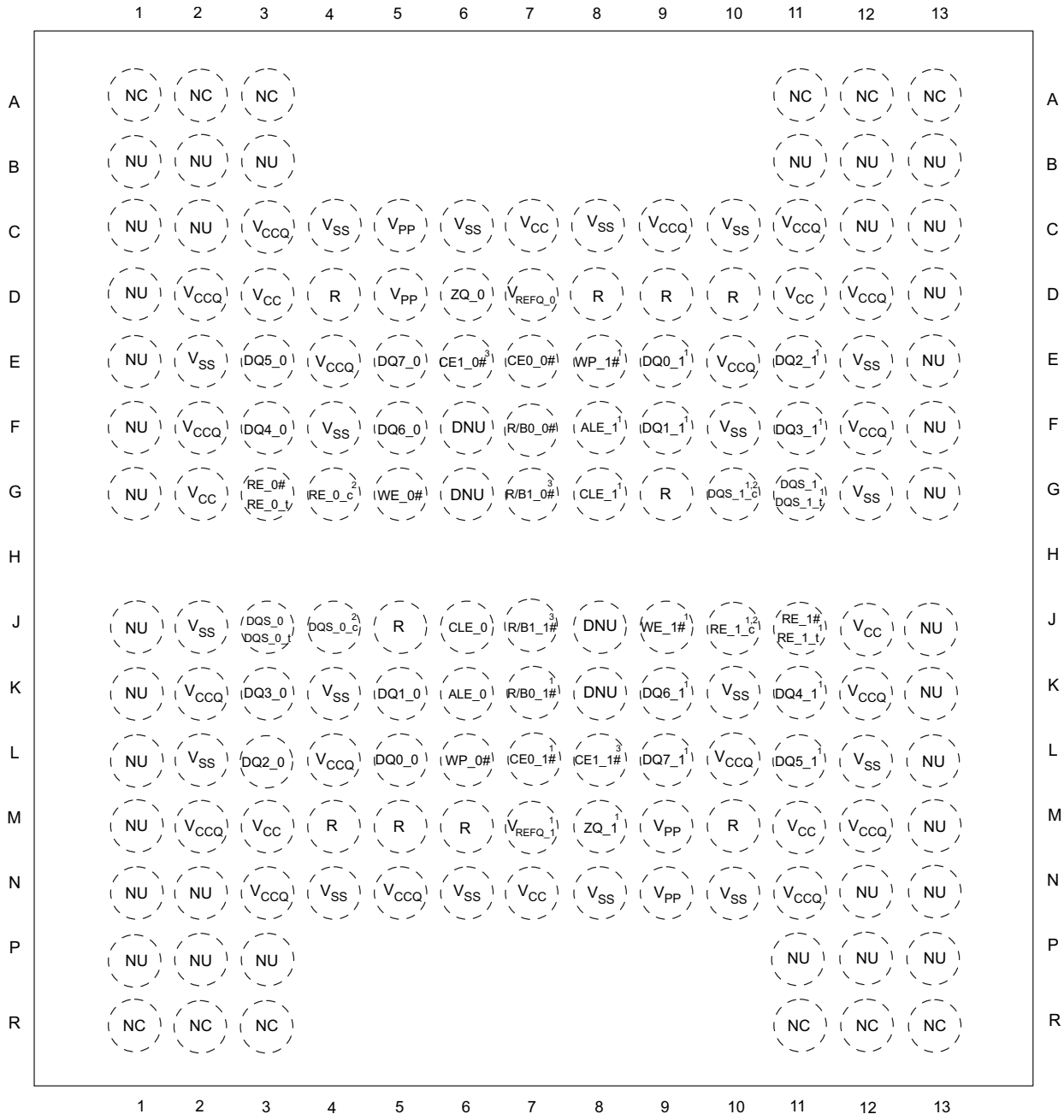
Signal Assignments

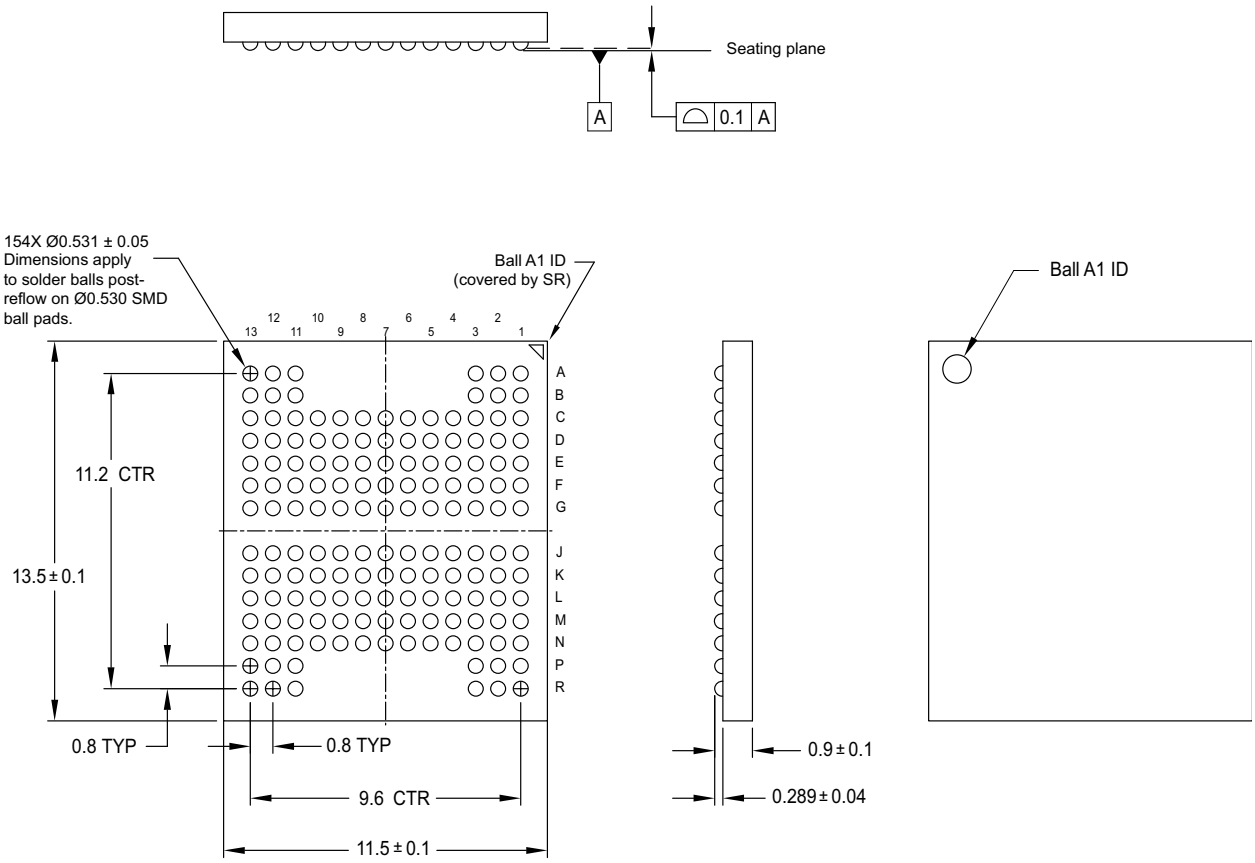
Figure 2: Ball Assignment (Ball-Down, Top View) 154-Ball BGA



Notes: 1. These signals are available on dual, quad, octal, or higher die stacked die packages. They are NC for other configurations.
2. These signals are available when differential signaling is enabled.
3. These signals are available on quad die four CE#, octal die, or 16 die stacked packages. They are NC for other configurations.

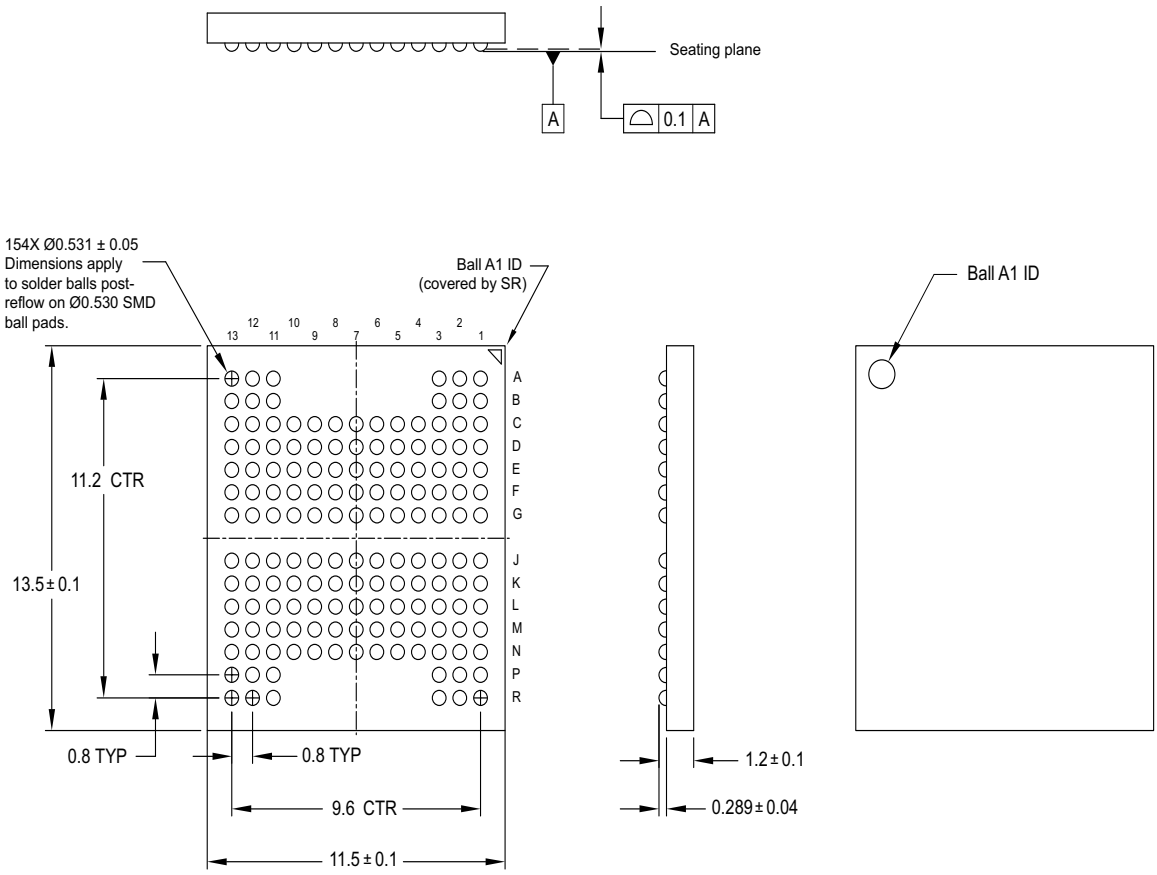
Package Dimensions

Figure 3: 154-Ball VBGA – 11.5mm x 13.5mm x 1.0mm (D4 Package Code)



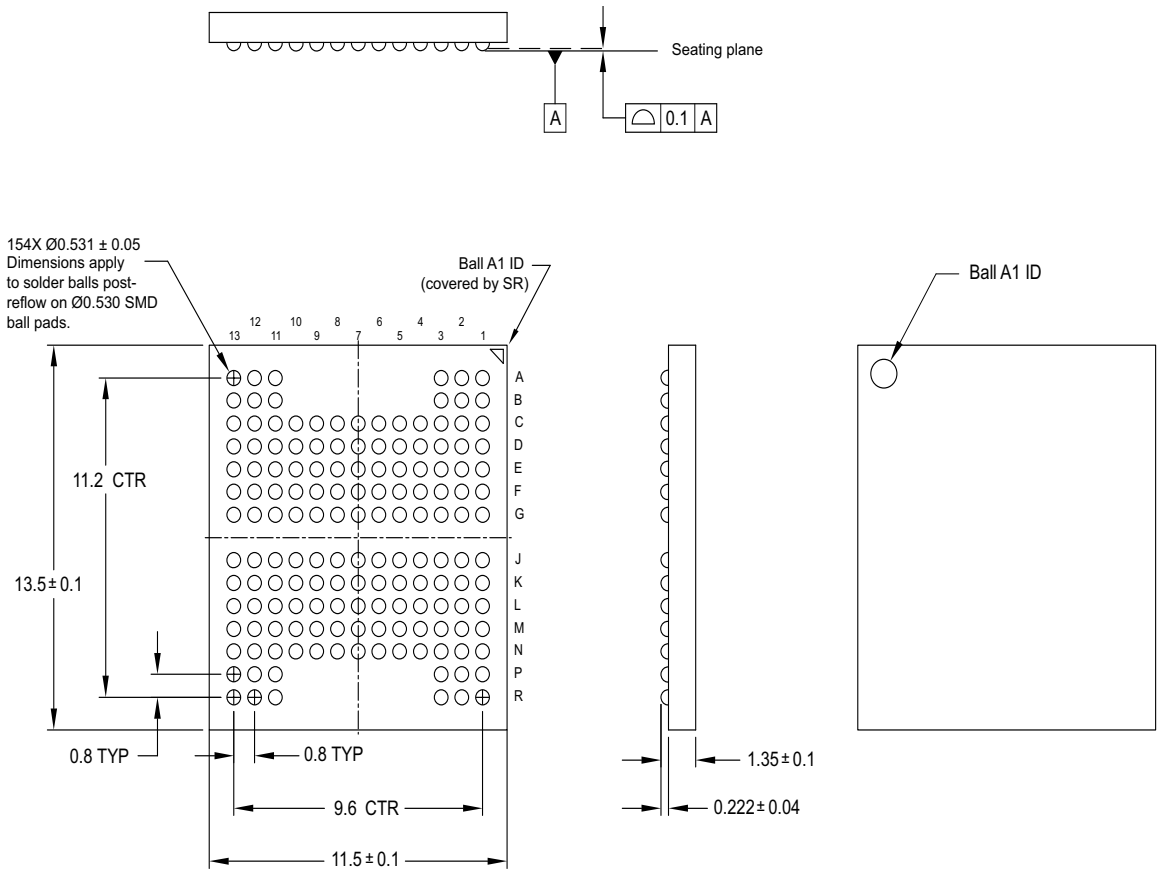
Notes: 1. All dimensions in mm.
2. Solder ball material: SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni).

Figure 4: 154-Ball VBGA – 11.5mm x 13.5mm x 1.3mm (D5 Package Code)



Notes: 1. All dimensions in mm.
2. Solder ball material: SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni).

Figure 5: 154-Ball VBGA – 11.5mm x 13.5mm x 1.45mm (D8 Package Code)



Notes: 1. All dimensions in mm.
2. Solder ball material: SACQ (92.45% Sn, 4.0% Ag, 3.0% Bi, 0.5% Cu, 0.05% Ni).

Electrical Specification – Array Characteristics

Table 2: TLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	^{t}BERS	5	19	ms	5
Cache program operation time	^{t}CBSY	TBD	TBD	µs	5
Change column setup time to data in/out or next command for both single LUN and multi LUN operation	^{t}CCS	–	–	ns	11
Dummy busy time	^{t}DBSY	0.5	0.5	µs	
ERASE SUSPEND operation time	^{t}ESPD	85	100	µs	
Busy time for SET FEATURES and GET FEATURES operations Feature Address <80h	^{t}FEAT1	–	1	µs	13
Busy time for SET FEATURES and GET FEATURES operations Feature Address 80h or above	^{t}FEAT2	–	2	µs	13
ERASE SUSPEND operation time	^{t}ESPD	85	100	µs	
CACHE LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	µs	2, 6
Page Buffer Transfer Busy time	^{t}PBSY	4	5	µs	
Power-on reset time	^{t}POR	1	4	ms	
PROGRAM PAGE operation time	^{t}PROG	1800	3000	µs	5, 15
Effective PROGRAM PAGE operation time	^{t}PROG_eff	600	–	µs	4
PROGRAM SUSPEND operation time	^{t}PSPD	50	100	µs	
Busy time when PROGRAMSUSPEND is issued when LUN is already in suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing	^{t}PSPDN	–	18	µs	
READ PAGE operation time	^{t}R	61	78	µs	10, 12
Single Bit Soft Bit Read (SBSBR) Time	^{t}R_SBSBR	TBD	TBD	µs	
Auto Read Calibration time	^{t}RARC	TBD	TBD	µs	
Cache read busy time when RDY/ARDY = 1	^{t}RCBSY1	3	TBD	µs	10, 12
Cache read busy time when RDY = 1, ARDY = 0	^{t}RCBSY2	3	TBD	µs	10, 12
ERASE RESUME to ERASE SUSPEND delay	^{t}RSESPD	–	–	ms	8
PROGRAM RESUME to PROGRAM SUSPEND delay	^{t}RSPSPD	–	–	µs	9
IWL READ operation time	^{t}RSNAP	55	67	µs	
Device reset time (Erase)	^{t}RST	75	150	µs	14
Reset during ^{t}PBSY time in a programming sequence	^{t}RST	–	15	µs	
Reset during READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh)	^{t}RST	–	40	µs	
Reset during DQ training	^{t}RST	–	70	µs	
Reset during Program OTP	^{t}RST	–	150	µs	
Reset at any other time	^{t}RST	–	5	µs	
Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation	^{t}RTABSY	TBD	TBD	µs	16
Busy time for IWL read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array IWL read operation	^{t}RTABSY_IWL	TBD	TBD	µs	17
Full calibration time	^{t}ZQCL	–	1	µs	3
Short calibration time	^{t}ZQCS	–	0.3	–s	3

Notes:
1. The pages in the OTP Block have an NOP of 2.
2. Multi-Plane Read operation on any Shared Page Group that has a mismatched number of programmed shared pages paring across the physical planes is supported.
3. Increased time beyond TYP may result when greater than 8 LUNs share a ZQ resistor.
4. ^{t}PROG_eff excludes the time taken to enter the same data multiple-times in multi-pass programming method and is the effective time taken to program the data into the flash array.
5. In the case of a program operation that exceeds ^{t}PROG/ ^{t}CBSY Max, that specific NAND block may be retired by the host system.
6. ^{t}CBSY and ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
7. In the case of a erase operation that exceeds ^{t}BERS Max, that specific NAND block may be retired by the host system.
8. ^{t}RSESPD (Min) = 2.75ms; Issuing an ERASE SUSPEND (61h) command after an ERASE RESUME (D2h) with a delay shorter than ^{t}RSESPD is not recommended but is allowed, but there may not be forward progress in the suspended erase operation. Regardless of forward progress, a single erase operation may not be suspended more than 30 times.
9. ^{t}RSPSPD (Min) = 200us; Issuing an PROGRAM SUSPEND (84h) command after an PROGRAM RESUME (13h)with a delay shorter than ^{t}RSPSPD is not recommended but is allowed, but there may not be forward progress in the suspended program operation. Regardless of forward progress, a single program operation may not be suspended more than 30 times.
10. If a page read is a page where not all associated shared pages have been programmed, the Max array busy time for the read operation may be up to TBDµs.
11. ^{t}CCS (Min) = 275ns. For NV-DDR3 and NV-LPDDR4 interfaces, during data output command sequences which require ^{t}CCS, ^{t}CCS is referenced from WE# high to the RE_t falling edge marking the start of the read pre-amble (^{t}RPRE/^{t}RPRE2). For NV-DDR3 and NV-LPDDR4 interface, during data input command sequences which require ^{t}CCS, ^{t}CCS is referenced from WE# high to the first byte input (DQS_t rising edge) when warmup cycles are disabled, and from WE# high to the first byte of the first input warmup cycle (DQS_t rising edge) when warmup cycles are enabled.
12. Max spec is the worst ^{t}R time when reading a page with all shared pages programmed.
13. For Feature Addresses 80h and above, ^{t}FEAT time may be up to 3us. For all other Feature Addresses, ^{t}FEAT time may be up to 1us.
14. After any array command, upon SR5/SR6 = 0, if a reset is issued, ^{t}RST will follow ^{t}RST (Program/Read/Erase). Array commands include all read operations/program operations/erase operations/copyback operations in the command set table.
15. ^{t}RTABSY applies to all array Read operations (excluding IWL). In Cache Read based operations ^{t}RTABSY still applies before the next array Cache Read operation begins.
16. ^{t}RTABSY_IWL applies to all IWL Read operations.

Any parameters not referenced in the SLC Array Characteristics table should be referenced in the TLC Array Characteristics table.

Table 3: SLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	^{t}BERS	6	19	ms	4
Program Cache busy	^{t}CBSY	TBD	TBD	µs	2, 3
ERASE SUSPEND operation time	^{t}ESPD	85	100	µs	
Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing	^{t}ESPDN	–	18	µs	
LAST PROGRAM PAGE operation time	^{t}LPROG	–	–	µs	2, 3
PROGRAM PAGE operation time	^{t}PROG	155	677	µs	3, 5, 6
PROGRAM SUSPEND operation time	^{t}PSPD	50	100	µs	3
Busy time when PROGRAMSUSPEND is issued when LUN is already in suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing	^{t}PSPDN	–	18	µs	
READ PAGE operation time	^{t}R	39	41	µs	
Cache read busy time when RDY/ARDY = 1	^{t}RCBSY1	3	TBD	µs	
Cache read busy time when RDY = 1, ARDY = 0	^{t}RCBSY2	3	TBD	µs	
IWL READ operation time	^{t}RSNAP	TBD	TBD	µs	
Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation	^{t}RTABSY	TBD	TBD	µs	7
Busy time for IWL read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array IWL read operation	^{t}RTABSY_IWL	TBD	TBD	µs	8

Notes:
1. The pages in the OTP Block have an NOP of 2.
2. ^{t}CBSY and ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
3. In the case of a program operation that exceeds ^{t}PROG/^{t}CBSY Max, that specific NAND block may be retired by the host system.
4. In the case of a erase operation that exceeds ^{t}BERS Max, that specific NAND block may be retired by the host system.
5. OTP Program operations could be up to Xus.
6. When using program suspend, the observed total ^{t}PROG may exceed ^{t}PROG (Max).
7. ^{t}RTABSY applies to all array Read operations (excluding IWL). In Cache Read based operations ^{t}RTABSY still applies before the next array Cache Read operation begins.
8. ^{t}RTABSY_IWL applies to all IWL Read operations.

Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns 8 bytes, most of which is an identifier code that includes the manufacturer ID, device configuration, and part-specific information.

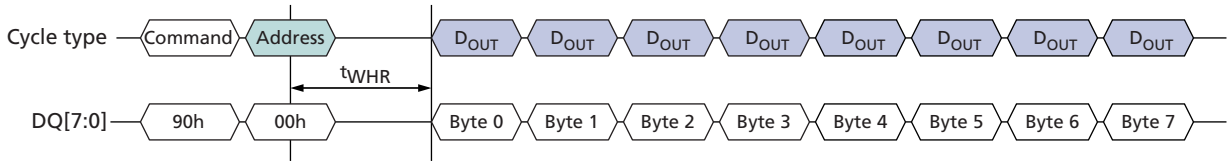
When the 90h command is followed by a 20h address cycle, the target returns 6 bytes of data beginning with the 4-byte ONFI identifier code ('O'=4Fh, 'N'=4Eh, 'F'=46h, 'I'=49h).

When the 90h command is followed by a 40h address cycle, the target returns 6 bytes of data beginning with the 5-byte JEDEC identifier code ('J'=4Ah, 'E'=45h, 'D'=44h,'E'=45h, 'C'=43h).

After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. One data byte is output per rising edge of DQS when ALE and CLE are LOW; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

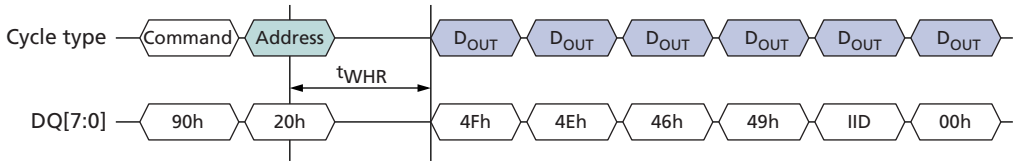
If host issues READ ID (90h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Figure 6: READ ID (90h) with 00h Address Cycle Operation



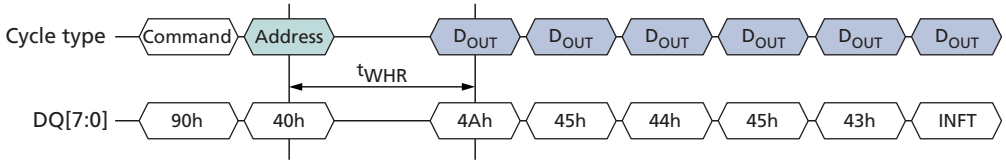
Notes: 1. See READ ID Parameters for Address 00h for byte definitions.

Figure 7: READ ID (90h) with 20h Address Cycle Operation



Notes: 1. See READ ID Parameters for Address 20h for byte definitions.

Figure 8: READ ID (90h) with 40h Address Cycle Operation



Notes: 1. See READ ID Parameters for Address 40h for byte definitions.

READ ID Parameter Tables

Table 4: READ ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
FBNB58R1T1KLBAHD4-AS	2Ch	D3h	08h	32h	E8h	31h	02h	00h
FBNB58R2T1KLEAHD4-AS	2Ch	D3h	08h	32h	E8h	31h	02h	00h
FBNB58R4T1KLMAHD4-AS	2Ch	D3h	08h	32h	E8h	31h	02h	00h
FBNB58R8T1KLUAHD5-AS	2Ch	E3h	89h	32h	E8h	31h	02h	00h

Note: 1. h = hexadecimal.

Table 5: READ ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
B58R	4Fh or “O”	4Eh or “N”	46h or “F”	49h or “I”	01h

Note: 1. h = hexadecimal.

Table 6: READ ID Parameters for Address 40h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
All	4Ah or “J”	45h or “E”	44h or “D”	45h or “E”	43h or “C”	10h

Notes: 1. h = hexadecimal.

Parameter Page Data Structure Tables

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:13]: Reserved (0) Bit 12: 1 = supports ONFI version 5.0 Bit 11: 1 = supports ONFI version 4.2 Bit 10: 1 = supports ONFI version 4.1 Bit 9: 1 = supports ONFI version 4.0 Bit 8: 1 = supports ONFI version 3.2 Bit 7: 1 = supports ONFI version 3.1 Bit 6: 1 = supports ONFI version 3.0 Bit 5: 1 = supports ONFI version 2.3 Bit 4: 1 = supports ONFI version 2.2 Bit 3: 1 = supports ONFI version 2.1 Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	00h, 10h
6–7	Features supported Bit 15: 1 = supports Package Electrical Specification Bit 14: 1 = supports ZQ calibration Bit 13: 1 = supports NV-DDR3 Bit 12: 1 = supports external V_{PP} Bit 11: 1 = supports Volume addressing Bit 10: 1 = supports NV-DDR2 interface Bit 9: 1 = supports NV-LPDDR4 Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports extended parameter page Bit 6: 1 = supports interleaved (multi-plane) read operations Bit 5: 1 = supports NV-DDR interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	FBNB58R1T1KLBAHD4 FBNB58R2T1KLEAHD4 FBNB58R4T1KLMAHD4	D8h, FBh
		FBNB58R8T1KLUAHD5	DAh, FBh

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
8–9	Optional commands supported Bit[15:14]: Reserved (0) Bit 13: 1 = supports ZQ calibration (Long and Short) Bit 12: 1 = supports GET/SET Features by LUN Bit 11: 1 = supports ODT CONFIGURE Bit 10: 1 = supports VOLUME SELECT Bit 9: 1 = supports RESET LUN Bit 8: 1 = supports small data move Bit 7: 1 = supports CHANGE ROW ADDRESS Bit 6: 1 = supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports READ STATUS ENHANCED Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE	–	FFh, 3Fh
10	ONFI-JEDEC JTG primary advanced command support Bit[7:4]: Reserved (0) Bit 3: 1 = supports ERASE BLOCK MULTI-PLANE Bit 2: 1 = supports COPYBACK PROGRAM MULTI-PLANE Bit 1: 1 = supports PROGRAM PAGE MULTI-PLANE Bit 0: 1 = supports CHANGE READ COLUMN	–	0Fh
11	Training commands supported Bit[7:5]: Reserved (0) Bit 4: 1 = supports Write Rx DQ training Bit 3: 1 = supports Write Tx DQ training Bit 2: 1 = supports Read DQ training Bit 1: 1 = supports Implicit (command based) DCC training Bit 0: 1 = supports Explicit DCC training	–	0Dh
12–13	Extended parameter page length	–	03h, 00h
14	Number of parameter pages	–	3Ch
15–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) SpecTek	–	53h, 50h, 45h, 43h, 54h, 45h, 4Bh, 20h, 20h, 20h, 20h, 20h

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	FBNB58R1T1KLBAHD4-AS	46h, 42h, 4Eh, 42h, 35h, 38h, 52h, 31h, 54h, 31h, 4Bh, 4Ch, 42h, 41h, 48h, 44h, 34h
		FBNB58R2T1KLEAHD4-AS	46h, 42h, 4Eh, 42h, 35h, 38h, 52h, 32h, 54h, 31h, 4Bh, 4Ch, 45h, 41h, 48h, 44h, 34h
		FBNB58R4T1KLMAHD4-AS	46h, 42h, 4Eh, 42h, 35h, 38h, 52h, 34h, 54h, 31h, 4Bh, 4Ch, 4Dh, 41h, 48h, 44h, 34h
		FBNB58R8T1KLUAHD5-AS	46h, 42, 4Eh, 42h, 35h, 38h, 52h, 38h, 54h, 31h, 4Bh, 4Ch, 55h, 41h, 48h, 44h, 35h
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	B0h, 07h
86–91	Reserved (0)	–	All 00h
92–95	Number of pages per block	–	E0h, 0Ah, 00h, 00h
96–99	Number of blocks per LUN	–	4Ah, 0Dh, 00h, 00h
100	Number of LUNs per chip enable	FBNB58R1T1KLBAHD4	01h
		FBNB58R2T1KLEAHD4	02h
		FBNB58R4T1KLMAHD4	04h
		FBNB58R8T1KLUAHD5	08h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	24h
102	Number of bits per cell	–	03h
103–104	Bad blocks maximum per LUN	–	D2h, 00h
105–106	Block endurance	–	0Ah, 03h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid block	–	00h, 00h
110	Number of programs per page	–	01h
111	Reserved (0)	–	00h
112	Number of bits ECC correctability	–	FFh

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	03h
114	Interleaved operation attributes Bit[7:6]: Reserved (0) Bit 5: Reserved Bit 4: 1 = supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = supports program cache Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	1Eh
115	Reserved (0)	–	00h
116-117	NV-DDR3 timing mode support Bit[15:1]: Reserved (0) Bit 0: supports timing mode 19		01F, 00h
118-121	NV-LPDDR4 timing mode support Bit[31:17]: Reserved (0) Bit 16: 1 = supports timing mode 19 Bit 15: 1 = supports timing mode 18 Bit 14: 1 = supports timing mode 17 Bit 13: 1 = supports timing mode 16 Bit 12: 1 = supports timing mode 15 Bit 11: 1 = supports timing mode 14 Bit 10: 1 = supports timing mode 13 Bit 9: 1 = supports timing mode 12 Bit 8: 1 = supports timing mode 11 Bit 7: 1 = supports timing mode 10 Bit 6: 1 = supports timing mode 9 Bit 5: 1 = supports timing mode 8 Bit 4: 1 = supports timing mode 7 Bit 3: 1 = supports timing mode 6 Bit 2: 1 = supports timing mode 5 Bit 1: 1 = supports timing mode 4 Bit 0: 1 = supports timing mode 0 to 3	–	FFh, 1Fh, 00h, 00h
122–127	Reserved (0)	–	All 00h
Electrical parameters block			
128	Reserved (0)		00h
129–130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
131–140	Reserved (0)	–	All 00h

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
141	NV-DDR timing mode support Bit[7:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h
142	NV-DDR2 timing mode support Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h
143	NV-DDR/NV-DDR2 features Bit[7:4]: Reserved (0) Bit 3: 0 = device does not require V_{PP} enablement sequence Bit 2: 1 = devices support CLK stopped for data input Bit 1: 1 = typical capacitance values present Bit 0: 0 = use ^{t}CAD MIN value	–	00h
144–150	Reserved (0)	–	All 00h
151	Driver strength support. If the device supports NV-DDR, NV-DDR2, or NV-DDR3 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. Bit[7:5]: Reserved (0) Bit 4: 1 = supports 35 Ohm, 37.5 Ohm, and 50 Ohm drive strength (Default is 35 Ohm) Bit 3: 1 = supports 37.5 Ohm and 50 Ohm drive strength (Default is 37.5 Ohm) Bit 2: 1 = supports 18 Ohm driver strength Bit 1: 1 = supports 25 Ohm driver strength Bit 0: 1 = supports 35 Ohm and 50 Ohm driver strength (Default is 35 Ohm)	–	08h
152–157	Reserved (0)	–	All 00h
158	NV-DDR2/3 features Bit[7:6]: Reserved (0) Bit 5: 0 = external V_{REFQ} not required for >= 200MT/s Bit 4: 1 = supports differential signaling for DQS Bit 3: 1 = supports differential signaling for RE# Bit 2: 1 = supports ODT value of 30 ohms Bit 1: 1 = supports matrix termination ODT Bit 0: 1 = supports self-termination ODT	–	1Bh
159	NV-DDR2/3 warmup cycles Bit[7:4]: Data input warmup cycles support Bit[3:0]: Data output warmup cycles support	–	44h

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
160–161	NV-DDR3 timing mode support Bit 15: 1 = supports timing mode 18 Bit 14: 1 = supports timing mode 17 Bit 13: 1 = supports timing mode 16 Bit 12: 1 = supports timing mode 15 Bit 11: 1 = supports timing mode 14 Bit 10: 1 = supports timing mode 13 Bit 9: 1 = supports timing mode 12 Bit 8: 1 = supports timing mode 11 Bit 7: 1 = supports timing mode 10 Bit 6: 1 = supports timing mode 9 Bit 5: 1 = supports timing mode 8 Bit 4: 1 = supports timing mode 7 Bit 3: 1 = supports timing mode 6 Bit 2: 1 = supports timing mode 5 Bit 1: 1 = supports timing mode 4 Bit 0: 1 = supports timing mode 0 to 3	–	FFh, FFh
162	NV-DDR2 timing mode support Bit [7:3]: Reserved (0) Bit 2: 1 = supports timing mode 10 Bit 1: 1 = supports timing mode 9 Bit 0: 1 = supports timing mode 8	–	00h
163	Reserved (0)	–	00h
Vendor block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support SpecTek-specific read cache function	–	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support SpecTek-specific READ UNIQUE ID	–	00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	–	00h
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable DQ output impedance settings	–	02h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	04h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	–	1Ch
179	OTP Feature Address	–	90h
180	Read Retry Options Bit[7:5]: Reserved (0) Bit[4:0] = Number of Read Retry options supported	–	14h
181–184	Read Retry Options available. A value of ‘1’ in a bit position shows that Read Retry option is available for use. A value of ‘0’ in a bit position shows that Read Retry option is not available for use. For example, the binary value of ‘37h, 00h, 00h, 00h’ would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	–	00h, 00h, 00h, 00h
185	LDPC ECC requirement Bit[7:1]: Reserved (0) Bit 0: 1 = LDPC ECC is required	–	01h
186	Address Cycle Read Retry (ACRR) enablement Feature Address		96h
187-188	Address Cycle Read Retry (ACRR) subfeature position for enablement and subfeature bit position for enablement Bits[15:12]: Reserved (0) Bits[11:8]: Subfeature for enablement Bits[7:0]: Subfeature bit position for enablement		01h, 04h
189-192	Address Cycle Read Retry (ACRR) Options available. A value of '1' in a bit position shows that ACRR option is available for use. A value of 'o' in a bit position shows that ACRR option is not available for use.		FFh, 00h, 00h, 00h

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
193-194	SLC mode support Bits[15:3]: Reserved (0) Bit[2] 1 = Factory Reserved Setting Bit[1:0] 11 = Op-Code 3Bh supported only Bit[1:0]10 = Op-Codes 3Bh/3Ch supported only Bit[1:0] 01 = Feature Address 91h and Op-Codes 3Bh/3Ch supported Bit[1:0] 00 = Feature Address 91h and Op-Codes DAh/DFh supported		03h, 00h
195-196	Plane Select LSB Bit Position in the Row Address Field		0Ah, 00h
197–249	Reserved (0)	–	All 00h
250–252	Designator Bytes 1 to 3 (ASCII characters) Byte 250 = Designator Byte 1, “R”, Byte 251 = Designator Byte 2 Byte 252 = Designator Byte 3	–	54h, 00h, 00h
253	Parameter page revision	–	01h
254–255	Integrity CRC	FBNB58R1T1KLBAHD4	17h, 3Fh
		FBNB58R2T1KLEAHD4	80h, 63h
		FBNB58R4T1KLMAHD4	23h, A8h
		FBNB58R8T1KLUAHD5	D4h, CCh
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
...	...	–	...
15,104–15,359	Value of bytes 0–255	–	See bytes 0–255
15,360–15,615	Value of bytes 0–255	–	See bytes 0–255
Extended parameter pages			
15,360–15,361	Extended parameter page Integrity CRC	–	93h, 12h
15,362–15,365	Extended parameter page signature Byte 0: 45h, “E” Byte 1: 50h, “P” Byte 2: 50h, “P” Byte 3: 53h, “S”	–	45h, 50h, 50h, 53h
15,366–15,375	Reserved (0)	–	All 00h
15,376	Section 0 type	–	02h
15,377	Section 0 length	–	01h
15,378–15,391	Reserved (0)	–	All 00h
15,392	Number of bits ECC correctability	–	9Bh
15,393	ECC codeword size	–	0Bh
15,394–15,395	Bad blocks maximum per LUN	–	D2h, 00h
15,396–15,397	Block endurance	–	0Ah, 03h

Table 7: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
15,398–15,407	Reserved (0)	–	All 00h
Redundant extended parameter pages			
15,408–15,455	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
15,456–15,503	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
...	...	–	
18,192–18,239	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
18,240 to end of page	Reserved (FFh)	–	All FFh

Notes: 1. h = hexadecimal.
2. The ONFI READ ID values are not supported on Product Grades -AR and -MB.

Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. It is not permitted to issue any PROGRAM or ERASE operation to any block that has reported a fail status via the NAND status register after a PROGRAM or ERASE operation. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 8: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	See Table 9, Valid Blocks per LUN
Total available blocks per LUN	3402
First spare area location	Byte 16,384
Bad-block mark	00h
Minimum required ECC	TLC: LDPC to correct 1E-2 RBER[1] SLC: 60-bit ECC per 1147 bytes of data[2]

Notes: 1. Advance ECC required to achieve specified endurance and for general array data integrity. Please contact factory for information on soft data gathering and approved list of qualified controllers.

2. This is intended for host systems operating the entire NAND device only in SLC mode and does not apply to operation in any combination of TLC and SLC mode.

Table 9: Valid Blocks per LUN

Marketing Page Number	Symbol	Min	Max	Unit	Notes
FxxB58R -AS	NVB	3072	3402	blocks	1, 2
FxxB58R -AR		2874	3402		

Notes: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.
2. The -AS grade also guarantees the number of valid blocks per plane to be greater than TBD per plane.

Table 10: Approved Controller List

Marketing Part Number	Controller Vendor	Controller ID	FW Version	Notes
FxxB58R-AS	TBD	TBD	TBD	TBD
FxxB58R-AR	TBD	TBD	TBD	TBD

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Revision History

Rev. B 6/2022

- Updated Figure 2: Ball Assignment (Ball-Down, Top View) 154-Ball BGA on page 8.

Rev. A 2/2022

- SpecTek Initial Release.