JMicron Technology Corporation

DATASHEET

JMS583
USB 3.2 Gen 2 to PCIe Gen3x2 Bridge

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JMicron Technology Corporation

1F, No. 13, Innovation Road 1, Science-Based Industrial Park,

Hsinchu, Taiwan 300, R.O.C.

Tel: 886-3-5797389

Fax: 886-3-5799566

Email: sales@jmicron.com

Website: http://www.jmicron.com

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For more information on JMicron products, please visit the JMicron web site at http://www.JMicron.com or send e-mail to sales@jmicron.com.

JMicron Technology Corporation
1F, No.13, Innovation Road 1, Science-Based Industrial Park, Hsinchu, Taiwan 300, R.O.C.
Tel: 886-3-5797389
Fax: 886-3-5799566

Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
0.1	11/09/2017	-	Draft release.	Joe Chang
0.2	04/12/2018	Table 9 Section 5.4.1	1. Add XAVDDH signal description 2. GPIO [4] is used as LED indicator by default	Joe Chang
0.3	06/06/2018	Figure 4 Section 6.5 Chapter 6	1. Package outline drawing of QFN64 8x8 2. Update crystal electrical 3. Update electrical characteristics	Joe Chang
1.0	06/30/2018	Section 2.3 Table 11	1. Support SCSI/ NVMe Pass-through command 2. Change the typical value of 1.0V power supply	Joe Chang
1.1	03/29/2019	Section 6.9 Section 6.8	1. Modified T4 measure point of Figure 4 2. Modified Table 26	Mika Cheng
1.2	04/12/2019	Chapter 5	1. Change pin assignment diagram 2. Added note on pin19	Mika Cheng
2.0	06/12/2019	Section 5.4 Table 11、13 Section 6.6	1. Add Function Description for GPIO use 2. Add Note for testing result 3. Add IC condition and setting environment	Katie Shih
2.1	07/16/2019	Table 13	1. Delete DC Driving at I_{OH} and I_{OL}	Katie Shih
2.11	01/05/2021	Figure 4	1. Modified Mechanical Dimensions	Katie Shih

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1 Overview

JMS583 is a bridge controller between the USB host and the storage devices with PCIe/NVMe interface. Its upstream port provides a USB which data speed can reach up to ten gigabits per second (10 Gb/s), or the data transmission rate for USB 3.2 Gen2 specification. Meanwhile, its downstream port can connect to PCIe/NVMe storage devices, such as a solid-state drive (SSD). The data speed for the PCIe port can arrive at 16 Gb/s, or the data rate for the PCIe Gen3x2 requirements.

Also, JMS583 has USB Type-C™ connectivity built in to the controller that any device using JMS583 can have a USB Type-C™ connector without adding any additional peripheral part. It can save costs to buy parts, and efforts to build inventory, and it can reduce printed circuit board area for the system designs.

JMS583 supports TRIM to the SSD and can transmit and receive data by both of the USB Mass Storage Class Bulk-Only Transport (BOT) and USB Attached SCSI Protocol (UASP) to and from the host respectively. The data storage devices can achieve its summit of performance by taking advantage of these built-in unmatched features.

JMS583 is well equipped for power management that it can meet a wide variety of power requirements from different scales of data storage systems: those for data center, network attached storage (NAS) systems, and portable SSDs, and even those for thumb-sized Internet-of-Thing (IoT) devices.

Owing to its USB Type-C™ connectivity, JMS583 can work with some power management controllers to a USB Power Delivery (PD) enabled data storage device. The data storage devices having SSDs of large capacity can accept the electrical power from sources of energy, such as hosts acting as a power provider of USB PD to supply sufficient electricity to the device after they negotiate with each other, without plugging in.

Finally, JMS583 is a new product that almost reaches USB3.2 Gen2 line bandwidth. Using JMS583, the security system can transfer higher quality video, such as 4K or even 8K, and quicker to their data storage devices than ever.

2 Features

2.1 General Features

- Design for Windows 7, Windows 10 and MAC 10.10.5 or later version
- Embedded 5V to 1.0V voltage regulator
- Embedded 5V to 3.3V linear voltage regulator (LDO)
- Provide hardware controlled PWMs
- Provide software utilities for downloading the upgraded firmware code under USB2.0/ USB 3.2 Gen1 and Gen2
- QFN64 8x8 package
- Support 25MHz external crystal
- Support 3.3V I/O
- Thirteen GPIOs for customization

2.2 Universal Serial Bus

- Comply with USB 3.2 Gen 1 and Gen 2 Specification,
- Comply with USB Mass Storage Class, Bulk-Only Transport Specification (Revision 1.0)
- Comply with USB Attached SCSI Protocol (UASP) Specification (Revision 4)
- Integrate with USB Type-C™ multiplexer & configuration channel (CC) logic
- Support USB Super-Speed/ High-Speed/ Full-Speed Operation
- Support USB2.0/ USB 3.2 Gen 1/ Gen 2 power saving mode
- Support external SPI NVRAM for Vendor VID/PID of USB2.0/USB 3.2 Gen 1/2 device controller

2.3 PCI Express

- Comply with PCI Express Base Specification Revision 3.1a
- Comply with NVM Express 1.3
- Support TRIM to the SSD
- Support SCSI/ NVMe Pass-through command to allow an application client to transmit a NVMe command to a NVMe device.

3 Block Diagram

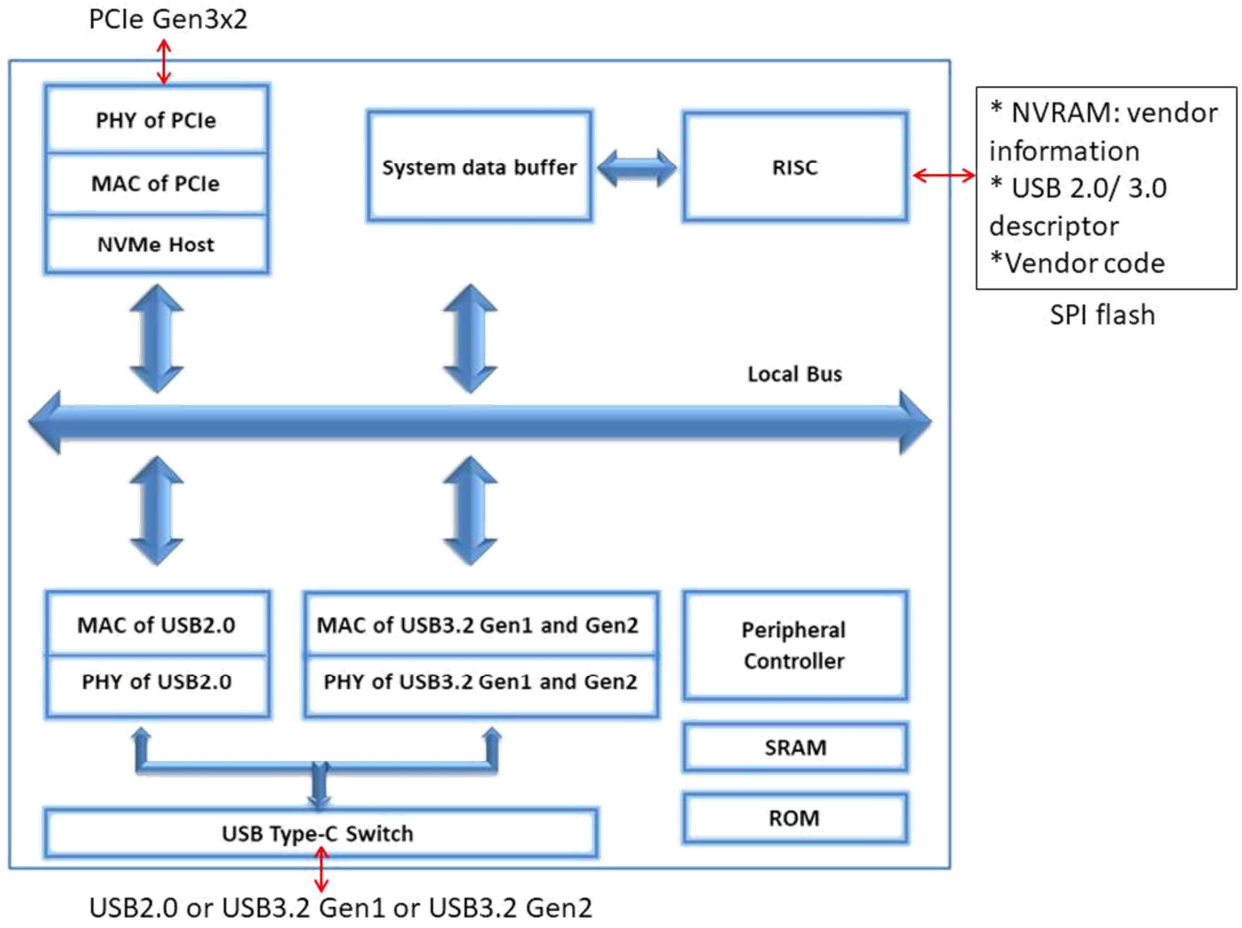


Figure 1 Block Diagram

4 Application

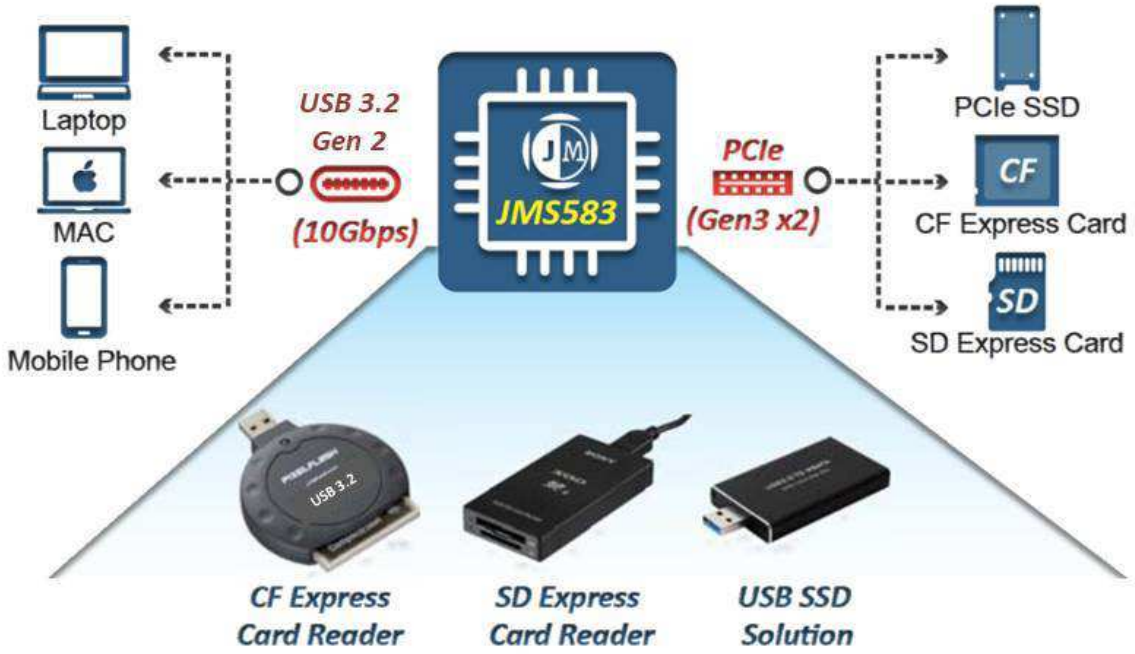


Figure 2 Application Scenarios

5 Package and Pin Assignments

5.1 Pin Diagram

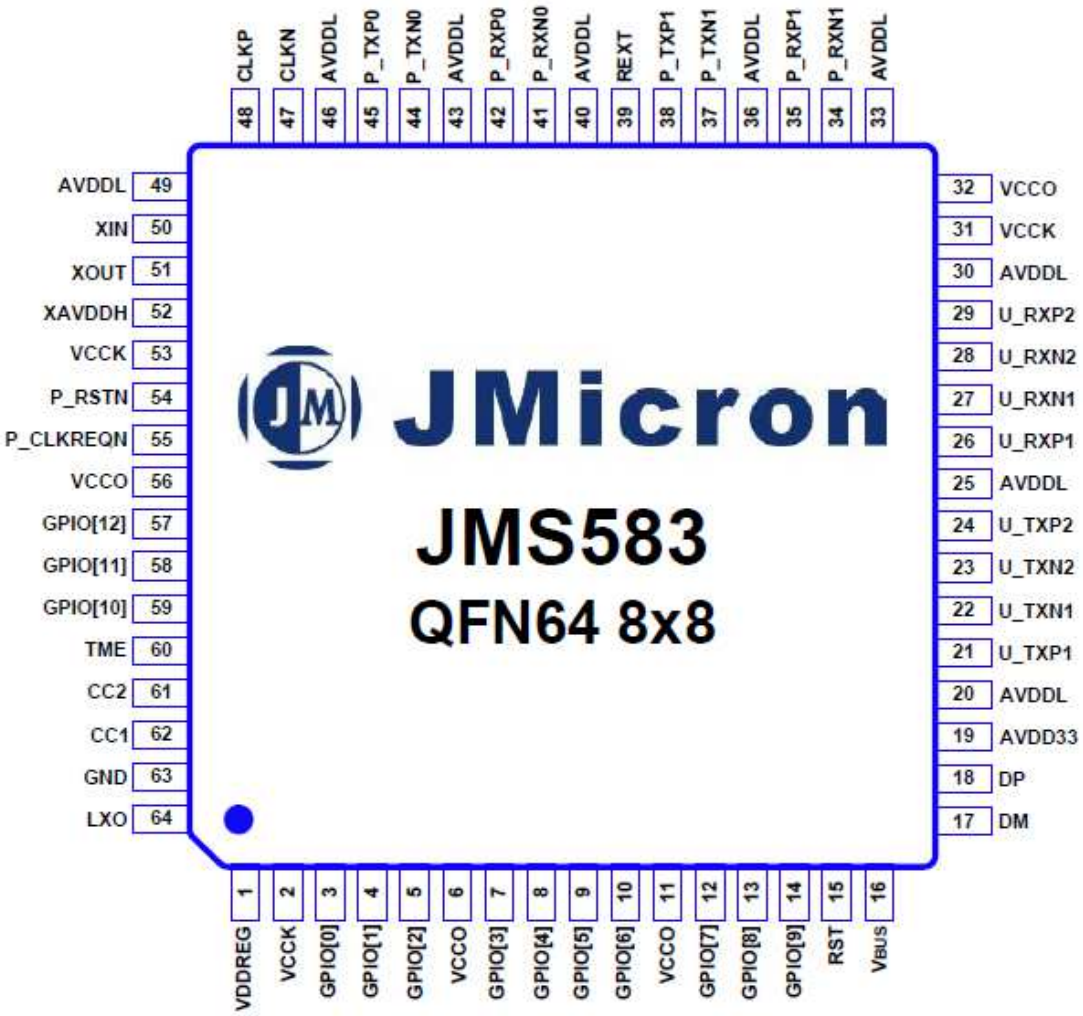
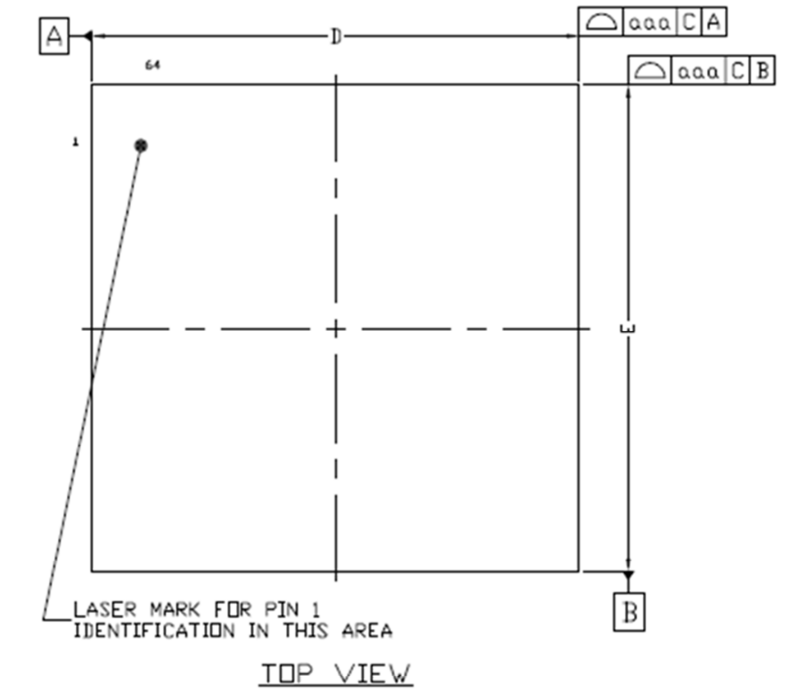
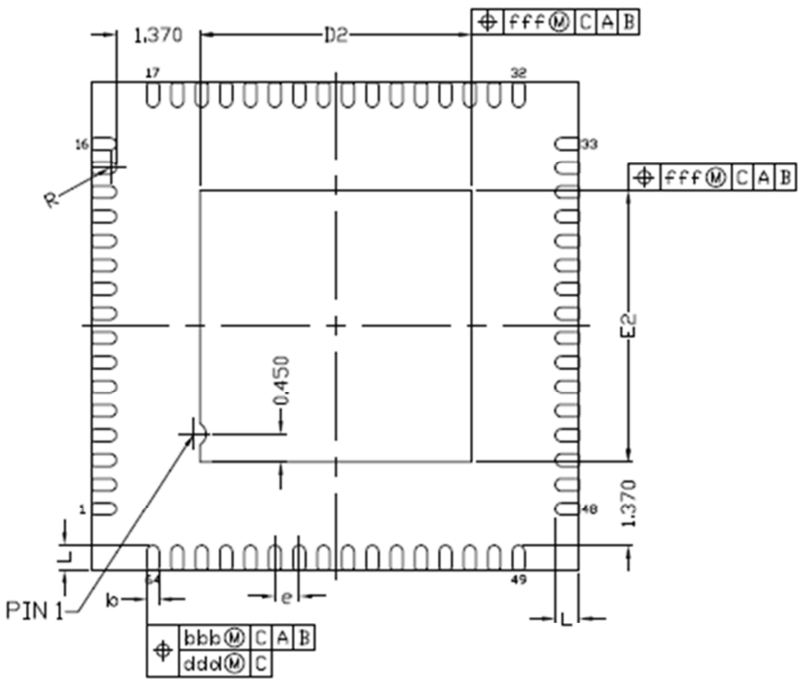


Figure 3 Pin Assignment of JMS583

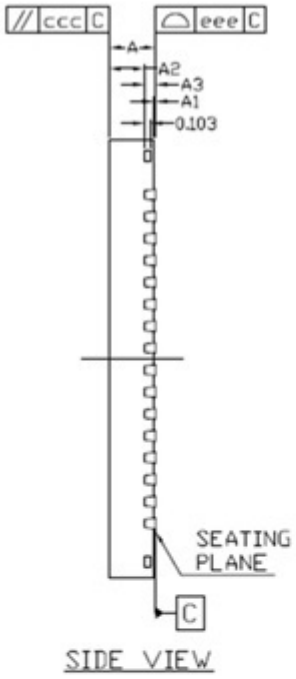
5.2 Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.900	---	---	0.035
A1	0.000	---	0.050	0.000	---	0.002
A2	---	0.650	0.700	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	8 BSC			0.315 BSC		
D2	4.160	4.460	4.560	0.164	0.176	0.180
E	8 BSC			0.315 BSC		
E2	4.160	4.460	4.560	0.164	0.176	0.180
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Figure 4 Package Outline Drawing of QFN64 8x8

5.3 Signal Descriptions

5.3.1 Pin Type Definitions

Table 1 Pin Type Definitions

Pin Type	Definitions
A	Analog
D	Digital
P	Power
I	Input
O	Output
IO	Bi-directional
OD	Open-Drain
H	Internal weak pull-high
L	Internal weak pull-low

5.3.2 Pin Descriptions

PCIe Interface Signals

Table 2 PCIe Interface Signals

Signal Name	Pin Number	Type	Description
P_RXN1	34	AI	**PCIe Port RX- Signal of Lane 1**
P_RXP1	35	AI	**PCIe Port RX+ Signal of Lane 1**
P_TXN1	37	AO	**PCIe Port TX- Signal of Lane 1** A 220 nF capacitor should be connected between this pin and PCIe connector.
P_TXP1	38	AO	**PCIe Port TX+ Signal of Lane 1** A 220 nF capacitor should be connected between this pin and PCIe connector.
REXT	39	AI	**External Reference Resistance** A 12kΩ ±1% external resistor should be connected to this pin.
P_RXN0	41	AI	**PCIe Port RX- Signal of Lane 0**
P_RXP0	42	AI	**PCIe Port RX+ Signal of Lane 0**
P_TXN0	44	AO	**PCIe Port TX- Signal of Lane 0** A 220 nF capacitor should be connected between this pin and PCIe connector.
P_TXP0	45	AO	**PCIe Port TX+ Signal of Lane 0** A 220 nF capacitor should be connected between this pin and PCIe connector.
CLKP	48	DO	**Differential Clock P** 100Mhz reference clock for Device.
CLKN	47	DO	**Differential Clock N** 100Mhz reference clock for Device.
P_RSTN	54	DO	**PCIe Reset for Device**
P_CLKREQN	55	DIO	**This is for L1 substrate**

USB 3.2 Gen1 and Gen2 Shard Interface Signals

Table 3 USB 3.2 Gen1 and Gen2 Shard Interface Signals

Signal Name	Pin Number	Type	Description
U_RXP2	29	AI	**Super Speed RX+ 2 signal**
U_RXN2	28	AI	**Super Speed RX- 2 signal**
U_RXN1	27	AI	**Super Speed RX- 1 signal**
U_RXP1	26	AI	**Super Speed RX+ 1 signal**
U_TXP2	24	AO	**Super Speed TX+ 2 signal** A 100 nF capacitor should be connected between this pin and USB connector.
U_TXN2	23	AO	**Super Speed TX- 2 signal** A 100 nF capacitor should be connected between this pin and USB connector.
U_TXN1	22	AO	**Super Speed TX- 1 signal** A 100 nF capacitor should be connected between this pin and USB connector.
U_TXP1	21	AO	**Super Speed TX+ 1 signal** A 100 nF capacitor should be connected between this pin and USB connector.

USB 2.0 Interface Signals

Table 4 USB 2.0 Interface Signals

Signal Name	Pin Number	Type	Description
DP	18	AIO	**USB 2.0 Bus D+ Signal**
DM	17	AIO	**USB 2.0 Bus D- Signal**
VBUS	16	PI	**USB 5V V_{BUS} power for LDO input**
AVDD33	19	PO	**USB 2.0 Analog 3.3V Output** A capacitor to ground is recommended on this pin. The value should be one uF. The output voltage range is 3.3V ±10% Note: 1. This pin provides power less than 100mA @ 3.3V. 2. This pin can afford chip internal power usage only. 3. If this pin does not provide an external power supply,

Signal Name	Pin Number	Type	Description
			this pin must be connected to a 4.7uF capacitor to ground.

Switching Regulator Interface

Table 5 Switching Regulator Interface

Signal Name	Pin Number	Type	Description
VDDREG	1	PI	**Voltage Regulator 5V Power Supply**
GND	63	PI	**Voltage Regulator Ground**
LXO	64	PO	**Voltage Regulator 1.0V Output** Switch node. Connect with external power inductor with a value of 4.7 uH.

Crystal Interface

Table 6 Crystal Interface

Signal Name	Pin Number	Type	Description
XIN	50	AI	**Crystal Input/ Oscillator Input** It is connected to a 25MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage should range in 3.3V ±5%.
XOUT	51	AO	**Crystal Output** It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved for No Connection (NC). The output variation range is around ±30ppm (input dependent). And the input voltage range is 3.3V ±5% (input dependent).

USB Type-C™ Configuration Channel

Table 7 USB Type-C™ Configuration Channel

Signal Name	Pin Number	Type	Description
CC1	62	AI	**CC Pin1 input for voltage detection** The maximum tolerant input voltage is 3.3V.
CC2	61	AI	**CC Pin2 input for voltage detection** The maximum tolerant input voltage is 3.3V.

Control and GPIO Interface

Table 8 Control and GPIO Interface

Signal Name	Pin Number	Type	Description
RST	15	DI	**System Global Reset Input** Active-low to reset the entire chip. An external RC should be connected to this pin.
TME	60	DI	**MP Test Mode Enable** The pin is reserved for IC mass production testing. Keep this pin to logic “0” in normal operation.
GPIO [0]	3	DIOH	**Serial Flash (SO)** After power on status detecting, this pin becomes Data Output of serial flash. This pin is by default set to input.
GPIO [1]	4	DIOH	**Serial Flash (SCK)** This pin is Serial Flash Data Clock (SCK) of serial flash. This pin is by default set to output.
GPIO [2]	5	DIOH	**Serial Flash (SI)** Serial Flash Data Input (SI) of Serial Flash. This pin is by default set to output.
GPIO [3]	7	DIOH	**Serial Flash (CE0#)** This pin functions as Chip Enable (CE#0) of Serial Flash.
GPIO [4]	8	DIOH	**GPIO [4]** Can be configured by customer firmware.
GPIO [5]	9	DIOH	**GPIO [5]** Can be configured by customer firmware.
GPIO [6]	10	DIOH	**GPIO [6]** Can be configured by customer firmware.
GPIO [7]	12	DIOH	**GPIO [7]** Can be configured by customer firmware.
UAO/GPIO [8]	13	DIOH	**RISC UART TX Interface/ GPIO[8]** Can be configured by customer firmware.
UAO/GPIO [9]	14	DIOH	**RISC UART RX Interface/ GPIO[9]** Can be configured by customer firmware.
GPIO [10]	59	DIOH	**GPIO[10]** Can be configured by customer firmware.
GPIO [11]	58	DIOH	**GPIO[11]** Can be configured by customer firmware.
GPIO [12]	57	DIOH	**GPIO[12]** Can be configured by customer firmware.

Power Supply Interface

Table 9 Power Supply Interface

Signal Name	Pin Number	Type	Description
VCCO	6, 11, 32, 56	PI	**3.3V I/O power supply**
VCCK	2, 31, 53	PI	**1.0V core power supply**
AVDDL	20, 25, 30, 33, 36, 40, 43, 46, 49	PI	**Analog 1.0V power supply**
XAVDDH	52	PI	**3.3V crystal pad power (i.e., AVDDXTAL)**

5.4 Function Description

5.4.1 LED Indicator

By default, GPIO [4] is used as LED indicator. If the user has a different application for LED function, please contact JMicron's AE before PCB layout.

5.4.2 GPIO Initial Value

All GPIOs set as input mode and enable internal pull-up function while in reset. After reset, the firmware will program all GPIOs as input mode. Afterward, the initial value of GPIOs is read and stored in the system RAM for future using.

- V_{BUS} detector

GPIO[6] is used for V_{BUS} detection. There is a voltage divider circuit on a board. Power source is connected from V_{BUS} 5V. The output is connected to GPIO[6] for V_{BUS} detection.

6 Electrical Specifications

6.1 Absolute Maximum Ratings

Warning: Absolute maximum rating may cause the device permanent damage or reliability will be affected. All voltage is a specified reference to the ground unless otherwise specified.

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
Digital 3.3V	$VCCO_{(ABS)}$	-0.3	-	4.13	V
Digital 1.0V	$VCCK_{(ABS)}$	-0.3	-	1.15	V
Switching regulator power	$AVDDS_{(ABS)}$	-0.3	-	5.5	V
3.3V Crystal Pad power	$XAVDDH_{(ABS)}$	-0.3	-	4.13	V
Analog 1.0V	$AVDDL_{(ABS)}$	-0.3	-	1.15	V
USB V_{BUS}	V_{BUS}	-	-	5.5	V
Digital I/O input voltage	$V_{I(D)}$	-0.3	-	4.13	V
Storage temperature	$T_{STORAGE}$	-40	-	150	°C

6.2 Recommended Operating Voltage and Temperature

Table 11 Operating Voltage and Temperature

Parameter	Symbol	Min	Typical	Max	Units
Digital 3.3V Power Supply	VCCO	3.0	3.3	3.6	V
Digital 1.0V Power Supply	VCCK	0.95	1.0	1.1	V
Switching Regulator	AVDDS	4.5	5.0	5.5	V
3.3V Crystal Pad Power	XAVDDH	3.0	3.3	3.6	V
Analog 1.0V Power Supply	AVDDL	0.95	1.0	1.1	V

USB V_{BUS}	V_{BUS}	4.5	5.0	5.5	V
Digital I/O input voltage	$V_{I(D)}$	3.0	3.3	3.6	V
Ambient Operation Temperature	T_A	0	-	70	°C
Maximum Junction Temperature	T_J	-	-	125	°C

Note:

1. All supply mean voltage power noise <±5%

6.3 External Clock Source Conditions

Table 12 External Clock Source Conditions

Parameter	Symbol	Min	Typical	Max	Units
External reference clock		-30ppm	25	+30ppm	MHz
Clock Duty Cycle		45	50	55	%

6.4 DC Electrical Characteristics

Table 13 DC Specifications

Parameter	Symbol	Min	Typical	Max	Units
Input low voltage	V_{IL}	-0.3	-	0.8	V
Input high voltage	V_{IH}	2	-	5.5	V
Output low voltage	V_{OL}	-	-	0.4	V
Output high voltage	V_{OH}	2.4	-	-	V
Low Level Output Current	I_{OL}	9.7	-	21.5	mA

High Level Output Current	I_{OH}	17.0	-	56.5	mA
Internal weak pull-high resistance	R_{pu}	27	38	59	KΩ
Internal pull-low resistance	R_{pd}	-	-	-	KΩ

Note:

1. The above test results are under the environment at ambient temperature 25 °C.

6.5 Crystal input

Signal crystal input (25MHz) is needed.

Table 14 Crystal Electrical Specification

Parameter	Symbol	Min	Typical	Max	Units
Crystal start up time vs. AVDDL	$T_{Crystal}$	-	-	5	mS
Crystal Frequency	F_{clk}	-	25	-	MHz
Long term stability (Crystal Only)	$\Delta f_{MAX\_Crystal}$	-30	-	30	ppm
Long term stability (On Board)	$\Delta f_{MAX\_OnBoard}$	-150	-	150	ppm
Equivalent Series Resistance	ESR	-	-	55	Ω

6.6 Power Consumption

The power consumption is tested by the following setting environment and IC condition.

➢ **Setting Environment**

- Operation System: Windows 10 64bit
- Test tool: IOMeter
- Connected device: SSD Samsung 960 pro

➢ **IC Condition**

- Device Under Test: Evaluation Board(JMS583-EV-01-01-2)
- Voltage: 1.0V / 3.3V
- Firmware version: v00.01.00.03
- Device: JMS583

6.6.1 USB 2.0 to PCIe

Operation with PCIe L0 state

Table 15 Power Dissipation – USB 2.0 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	1.8	-	mA	Operate @ 3.3V Temperature = 25℃
Digital 1.0V	VCCK	-	157.6	-	mA	Operate @ 1.0V Temperature = 25℃
Analog 3.3V	XAVDDH	-	1.3	-	mA	Operate @ 3.3V Temperature = 25℃
Analog 1.0V	AVDDL	-	292.8	-	mA	Operate @ 1.0V Temperature = 25℃

Idle with PCIe L0 state

Table 16 Power Dissipation – USB 2.0 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	1.6	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	152.1	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	1.2	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	273.8	-	mA	Operate @ 1.0V

Suspend with PCIe L2 state

Table 17 Power Dissipation – USB 2.0 to PCIe L2

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	0.3	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	2.0	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	0.0	-	mA	Operate @ 3.3V

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Analog 1.0V	AVDDL	-	0.6	-	mA	Operate @ 1.0V

6.6.2 USB 3.2 Gen 1 to PCIe

Operation with PCIe L0 state

Table 18 Power Dissipation –USB 3.2 Gen 1 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	1.6	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	177.3	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	1.2	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	346.3	-	mA	Operate @ 1.0V

Idle with PCIe L0 state

Table 19 Power Dissipation –USB 3.2 Gen 1 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	1.6	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	150.0	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	1.2	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	344.6	-	mA	Operate @ 1.0V

Suspend with PCIe L2 state

Table 20 Power Dissipation – USB 2.0 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	0.3	-	mA	Operate @ 3.3V

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 1.0V	VCCK	-	2.0	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	0.0	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	2.0	-	mA	Operate @ 1.0V

6.6.3 USB 3.2 Gen 2 to PCIe

Operation with PCIe L0 state

Table 21 Power Dissipation – USB 3.2 Gen 2 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	1.7	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	238.3	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	1.2	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	422.6	-	mA	Operate @ 1.0V

Idle with PCIe L0 state

Table 22 Power Dissipation – USB 3.2 Gen 2 to PCIe L0

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	1.6	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	176.3	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	1.2	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	421.7	-	mA	Operate @ 1.0V

Suspend with PCIe L2 state

Table 23 Power Dissipation – USB 3.2 Gen 2 to PCIe L2

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital 3.3V	VCCO	-	0.3	-	mA	Operate @ 3.3V
Digital 1.0V	VCCK	-	2.0	-	mA	Operate @ 1.0V
Analog 3.3V	XAVDDH	-	0.0	-	mA	Operate @ 3.3V
Analog 1.0V	AVDDL	-	2.0	-	mA	Operate @ 1.0V

z

6.7 Internal Linear Regulator

Table 24 Internal Linear Regulator Specification

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Input Voltage Range	V_{IN_LINEAR}	-	5	-	V	
Output Voltage Range	V_{OUT_LINEAR}	-	3.3	-	V	
Max Output Current	I_{MAX}	-	-	150	mA	

6.8 Power-on Sequence

The power-on sequence is defined in Figure 5. Designers should follow all the rules for external power designs.

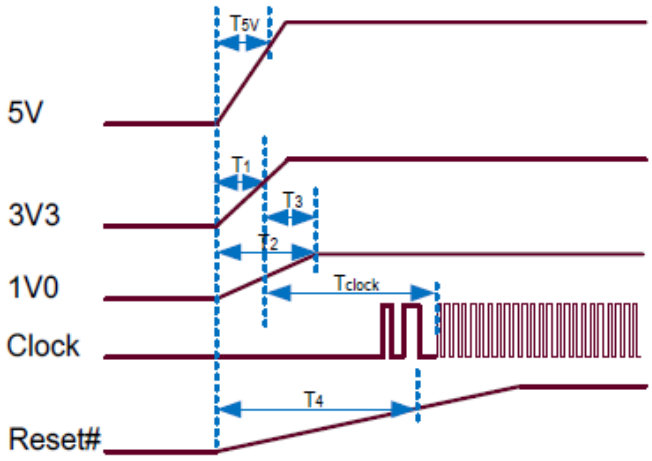


Figure 5 Power-on Sequence

T_{5V}: Rise time for 5Vpowerrailfrom 10% to 90%

T1: Rise time for 3V3 power rail from 5V 10% to 3V3 90%

T2: Rise time for 1V0power rail from 10% to 90%

T3: Time interval between 3V3power and 1V0Power

T4: Rise time for RST# signal from 0V to 1V77

T_{Clock}**:** Time interval between3V3and 90% clock swing

Note: Clock must meet 25MHz +/-30ppm during the sequence.

The recommended power sequence and timing requirements are listed in Table 25.

Table 25 Power-on timing Requirements

Time	Minimum	Maximum
T_{5V}	-	20 ms
T1	0 ms	10 ms
T2	0 ms	10 ms
T3	-5 ms	5 ms
T4	120 ms	500 ms

Time	Minimum	Maximum
T_{Clock}	-	5 ms

The RESET timing constraint is based on the external RC reset circuits. To control the charge and discharge time for RC circuits, minimum, and maximum requirements are listed. If designers apply timing control chip to control the reset signal, the only requirement will be the minimum value. In other words, the maximum value can be ignored without problems.

7 Product Naming Rule

7.1 Format of Part Number

The part number consists of the information of provider, product category, device number, package type, material type, product grade (operating temperature), mask ROM version and device version. The format of the part number is illustrated in Figure 6 below.

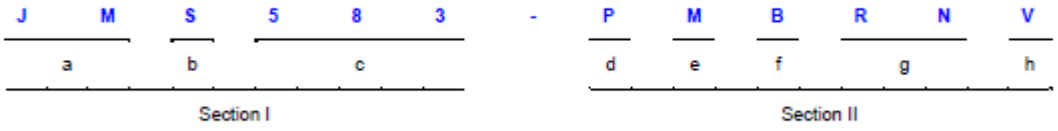


Figure 6 Format of the Part Number

7.2 Explanation of Part Number

Table 26 Explanation of Part Number

Section	Length	Purpose	Code(s)	Meaning
a (JM)	2 digits	Brand name	JM	The provider JMicron
b (S)	1 digit	Product category	S	SoC, system-on-a-chip
c (583)	3 digits	Device number	583	The serialnumber assigned randomly to form the device name "JMS583"in conjunction with brand name and product category.
d (P)	1 digit	Package type	B, L, Q, T	B = BGA; L = LQFP; Q = QFN; T = TQFP
e (M)	1 digit	Material & grade	G, H, I, J	G = Gold wired RoHS compliant halogen-free green product; Ta: 0 ~ 70°C. H = Copper wired RoHS compliant halogen-free green product; Ta: 0 ~ 70°C. I = Gold wired RoHS compliant halogen-free green product; Ta: -40 ~ 85°C. J= Copper wired RoHS compliant

				halogen-free green product; Ta: -40 ~ 85°C.
f (B)	1 digit	Internal bonding type	A, B, C, …	**A, B, C, …**
g (RN)	2 digit	Version of mask ROM	A0, A1, A2, … B0, B1, B2, … Z0	**Version A0, A1, A2, …** **Version B0, B1, B2, …** **Version Z0= no mask ROM**
h (V)	1 digit	Version of the IC	A, B, C, …	**Version A, B, C, …**

7.3 Top Mark

Each device has its unique top mark containing the information of provider, device name, part number, manufacturing date code, lot number and pin one identifier for identification. The top mark is illustrated in Figure 7 below.

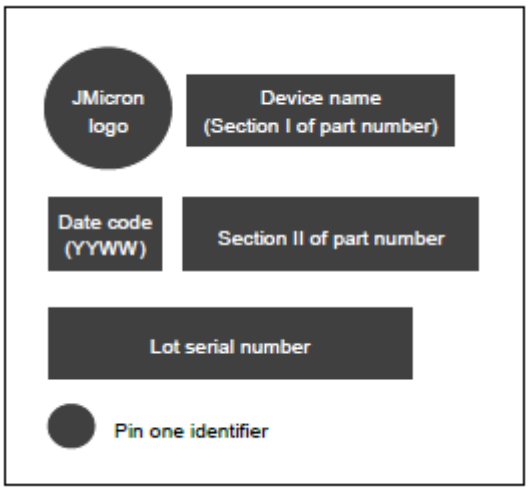


Figure 7 Illustration of Device Top Mark

Note: The above information is only for use in this product datasheet. For more detailed ordering information, please contact to JMicron's Sales Department, representatives, or distributors when ordering parts.

How to Reach Us:

- Home Page: http://www.jmicron.com
- Technical & Order Support: sales@jmicron.com