NAND Flash Die
1Tib Die: x8 300mm TLC

W3UB58RDUNXNZ-NAE4U / W3UB58RDUNXNZ-NAE5U
W1UB58RDUNXNZ-NAE8U / W1UB58RDUNXNZ-NAE9U
WYMB58RNNNXAA-NAE0E
W3UB58RDUNXNZ-NAE5U

B58R Die Features

- Open NAND Flash Interface (ONFI) 5.0 compatible[1]
- JEDEC NAND Flash Interoperability (JESD230E) compatible[2]
- Triple-level cell (TLC) technology
- Organization:
  - Page size x8: 18,352 bytes (16,384 + 1968 bytes)
  - Block size: 2784 pages, (44,544K + 5350.5K bytes)
  - Plane size: 6 planes x 567 blocks per plane
  - Device size: 1Tb: 3402 blocks
- NV-DDR3 I/O performance[3]
  - Up to NV-DDR3 timing mode 15
  - Clock rate: 1.25ns (NV-DDR3)
  - Read/write throughput per pin: 1.6 GT/s
- NV-LPDDR4 I/O performance
  - Up to NV-DDR4 timing mode 15
  - Clock rate: 1.25ns (NV-DDR3)
  - Read/write throughput per pin: 1.6 GT/s
- TLC Array performance
  - IWL READ operation time: 55µs (MAX)
  - READ PAGE operation time: 61µs (MAX)
  - Program page time: 600µs (MAX)
  - Erase block time: 6ms (TYP)
- Operating Voltage Range (at package ball)
  - V_{CC}: 2.35–3.6V
  - V_{CCQ}: 1.14–1.26V
- Absolute Minimum Voltage (at die pad)
  - V_{CC}: 2.25V
  - V_{CCQ}: 1.09V
- Command set: ONFI NAND Flash Protocol
  - IWL is not guaranteed
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data is required to be randomized by the external host prior to being inputted to the NAND device
- Copyback operations supported within the plane from which data is read
- On-die Termination (ODT)
- Quality and reliability:
  - TLC Endurance: 1000 PROGRAM/ERASE cycles
  - SLC Endurance: 41,000 PROGRAM/ERASE cycles
- Minimum required ECC: LDPC to correct 1e-2 RBER for TLC and 60-bits ECC per 1,147 bytes of data for SLC[1]
- This device is not intended for use in applications that require data to be pre-programmed in the NAND array prior to Reflow, Surface Mount, or other thermal processing. Please contact your SpecTek representative for details.
- Junction temperature: +10ºC to +70ºC

Die Outline

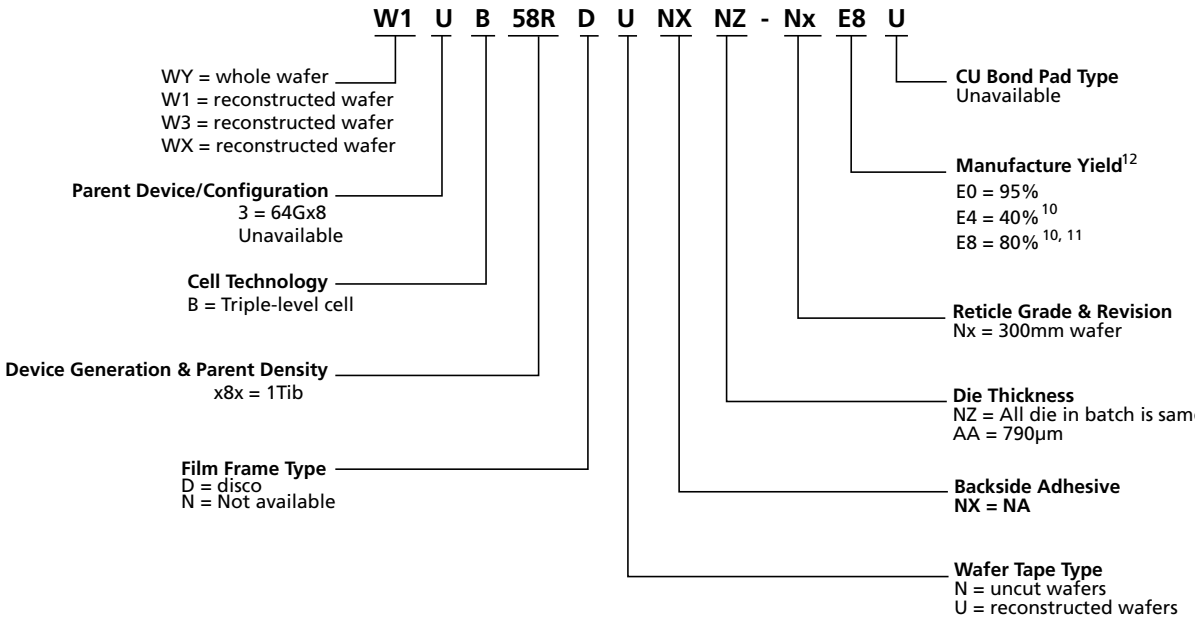
- Die size (stepping distance): 5.4994mm x 12.7992mm
- Bond pad location and identification, see Bond Pad Location and Identification.

General Physical Specifications

- Nominal whole wafer thickness: 790µm ±25µm. Reconstructed wafer thickness: varies batch to batch
- Typical bond-pad metal thickness: 7.1kÅ
- Typical topside passivation: 3.5µm polyimide over 8kÅ nitride over 10kÅ of undoped oxide
- Metallization composition: 7kÅ Al over 100Å Ti

Notes: 1. This is intended for host systems operating the entire NAND device only in SLC mode and does not apply to operation in any combination of TLC and SLC modes.

Figure 1: Marketing Part Number Information



Notes:
1. The ONFI 5.0 specification is available at www.onfi.org.
2. The READ JEDEC PARAM PAGE is NOT guaranteed or supported.
3. The I/O performance quoted only applies to NAND packages and channel topologies with up to 4 die per channel load. The 16-die 2-channel package only supports up to 1200 MT/s. The maximum data rate the actual system can achieve however, depends heavily on the user's board design and topology. Thus, the user must determine whether their system can achieve the desired data rate through signal integrity simulations and analysis.
4. For details, see the "Features" and "Error Management" sections of the packaged product data sheet.
5. Contact factory for part availability.
6. The READ PARAM PAGE or READ ONFI data is NOT guaranteed or supported.
7. The information listed in this supplement datasheet supersedes any differences listed in Micron's B58R Media Die datasheet.pdf
8. Yields do vary from wafer to wafer. Please refer the Yield Expectation document: https://www.spectek.com/menus/secure/AcceptNDA.aspx?object_name=SpecTek_Yield_Expectation.pdf.
9. No maps are needed for reconstructed wafers. Consult with Sales for die thickness and backside adhesive.
10. All die have between 50% and 97% valid blocks. Average effective yield is expected to be 85% by valid blocks.
11. Reconstructed wafer thickness varies batch to batch.
12. Please refer the SpecTek NAND Buyer's Guide document: https://media-www.micron.com/-/media/client/global/documents/spectek/buyers-guide/specteknandbuyers-guide.pdf?rev=c0cc479e396b4e46a820a465c2f7fe50

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General Die Instructions

Die Testing Procedures

SpecTek® wafer products are tested at a standard probe test level. Wafer probe is performed at an elevated temperature to ensure product functionality in SpecTek's standard packages. The package environment is not within SpecTek's control, so the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Wafer-Level Testing

The standard probe flow is the same probe flow used for SpecTek's package products.

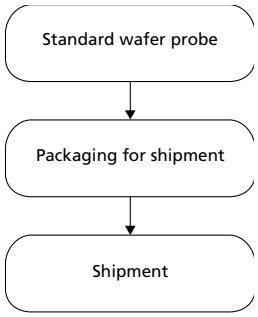
The following list provides an example of a standard probe test performed at wafer level for SpecTek's products:

- Opens/shorts
- Input/output leakage tests
- I_{CC} standby
- Voltage regulator performance
- Nominal V_{CC} and V_{CCQ} functional
- Memory array algorithmic patterns
- High voltage stress
- PROGRAM performance
- ERASE performance
- Invalid block marking

Repairs are implemented at each repair test. Repairable die are processed through repair algorithms based on the repair solutions defined during the tests described above. Post-repair testing is conducted with appropriate guardbands to ensure a consistently high quality level.

The status register reports the status of die operations.

Figure 2: Standard Probe Flow



SpecTek retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. SpecTek reserves the right to change the probe program at any time to improve the reliability, package device yield, or performance of the product. Die users may experience differences in performance and reliability relative to SpecTek data sheet specifications. This is due to differences in package capacitance, inductance, resistance, trace length, and device testing.

Functional Specification

The specifications in this die data sheet are provided for reference only. For target functional and parametric specifications, refer to the packaged product data sheet. This datasheet is available to customers under NDA; to obtain a copy, contact SpecTek NAND Flash support at nandsupport@micron.com.

Bonding Instructions

Refer to the Bond Pad Location from Pad 1 Center Table for a complete list of bond pads and coordinates from bond pad 1 center, and to the Bond Pad Location from Die Center Table for bond pad locations from center of die.

The back side of the die is at V_{SS} potential. For improved thermal performance, it is recommended that the die be connected to the ground plane. It is also possible to leave the back side of the die floating.

SpecTek recommends following the best practices guidelines defined in the technical note TN-00-22, “Micron Wire-Bonding Techniques,” located on Micron's Web site.

Wafer-Level Processing

SpecTek provides full-thickness wafers to accommodate post-processing. Post-processing includes adding extra passivation or metal layers, or bumping bond-pads. The street width is provided in the die outline, which also provides a reference from the center of bond pad 1 to the center of the intersection of the two streets for easy alignment.

Due to inherent structural differences for this 3D NAND wafer design, advanced wafer processing/dicing methods may be needed. SpecTek recommends customers work with their wafer processing partner in regards to wafer processing/dicing methods to qualify and quantify those methods for customer quality and reliability requirements.

Thermal Processing

This device is not intended for use in applications that require data to be pre-programmed in the NAND array prior to Reflow, Surface Mount or other thermal processing. Please contact your SpecTek representative for details.

Storage Requirements

SpecTek's wafer products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. SpecTek advises that customers avoid exposing Flash die products to ultraviolet light or processing them at temperatures greater than 250°C for more than five minutes. Failure to adhere to these handling instructions will result in irreparable damage to the devices.

SpecTek also recommends that the wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. Precautions for avoiding ESD damage are necessary during handling. The die must be in an ESD-protected environment for inspection and assembly at all times.

Product Reliability Monitors

SpecTek's QRA department continually samples product families for reliability studies. These samples are subjected to a battery of tests known as "accelerated life and environmental stress tests." During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product-family evaluations is published on a regular basis and is available upon request.

Die/Wafer-Level Reliability and Screening

Extensive SpecTek qualification of both the die and the die manufacturing process shows that production burn-in is not required to meet the endurance and data retention specifications on Flash products. Additional information is available upon request.

Bond Pad Location and Identification

Bond pad locations are provided from the center of pad 1, and from the center of the die.

Table 1: Bond Pad Location from Pad 1 Center

		Coordinates from Center of Pad 1 (0,0)		Passivation Openings		
Pad #	Pad Name	Xµm[1]	Yµm[1]	Xµm	Yµm	Notes
1	V_{SS}	0	0	80	50	2
2	V_{SS}	-7.5	70	65	50	2
3	V_{SS}	-7.5	140	65	50	2
4	V_{CC}	-7.5	210	65	50	2
5	V_{CC}	-7.5	280	65	50	2
6	V_{CC}	-7.5	350	65	50	2
7	V_{CC}	-7.5	420	65	50	2
8	V_{SS}	-7.5	490	65	50	2
9	V_{PP}	-7.5	560	65	50	6
10	DNU	-7.5	670	65	50	3
11	DNU	-7.5	780.7325	65	50	3
12	MDS2	-7.5	850.7325	65	50	4
13	NC	-7.5	920.7325	65	50	5
14	MDS1	-7.5	990.7325	65	50	4
15	MDS0	-7.5	1060.7325	65	50	4
16	V_{CC}	-7.5	1130.7325	65	50	2
17	V_{CC}	-7.5	1228.7325	65	50	2
18	V_{CC}	-7.5	1329.7325	65	50	2
19	V_{CC}	-7.5	1427.7325	65	50	2
20	WP#	-7.5	1497.7325	65	50	
21	NC	-7.5	1567.7325	65	50	5
22	ALE	-7.5	1637.7325	65	50	
23	NC	-7.5	1707.7325	65	50	5
24	CLE	-7.5	1777.7325	65	50	
25	NC	-7.5	1847.7325	65	50	5
26	V_{SS}	-7.5	1917.7325	65	50	2
27	V_{SSQ}	-7.5	1987.7325	65	50	2
28	DQ0	-7.5	2087.7325	65	50	
29	V_{CCQ}	-7.5	2193.9825	65	105	2
30	DQ1	-7.5	2300.2325	65	50	
31	V_{SSQ}	-7.5	2400.2325	65	50	2
32	V_{SSQ}	-7.5	2647.7325	65	50	2
33	DQ2	-7.5	2747.7325	65	50	
34	V_{CCQ}	-7.5	2853.9825	65	105	2
35	DQ3	-7.5	2960.2325	65	50	
36	V_{SSQ}	-7.5	3060.2325	65	50	2
37	RE_c	-7.5	3160.2325	65	50	
38	V_{CCQ}	-7.5	3266.4825	65	105	2
39	RE# (RE_t)	-7.5	3372.7325	65	50	
40	V_{SSQ}	-7.5	3612.7825	65	50	2

Table 1: Bond Pad Location from Pad 1 Center

		Coordinates from Center of Pad 1 (0,0)		Passivation Openings		
Pad #	Pad Name	Xµm[1]	Yµm[1]	Xµm	Yµm	Notes
41	DQS_c	-7.5	3712.7825	65	50	
42	V_{CCQ}	-7.5	3819.0325	65	105	2
43	DQS (DQS_t)	-7.5	3925.2825	65	50	
44	V_{SSQ}	-7.5	4025.2825	65	50	2
45	DQ4	-7.5	4125.2825	65	50	
46	V_{CCQ}	-7.5	4231.5325	65	105	2
47	DQ5	-7.5	4337.7825	65	50	
48	V_{SSQ}	-7.5	4437.7825	65	50	2
49	V_{SSQ}	-7.5	4685.2825	65	50	2
50	DQ6	-7.5	4785.2825	65	50	
51	V_{CCQ}	-7.5	4891.5325	65	105	2
52	DQ7	-7.5	4997.7825	65	50	
53	V_{SSQ}	-7.5	5097.7825	65	50	2
54	WE#	-7.5	5167.7825	65	50	
55	NC	-7.5	5237.7825	65	50	5
56	CE#	-7.5	5307.7825	65	50	
57	NC	-7.5	5377.7825	65	50	5
58	NC	-7.5	5447.7825	65	50	5
59	R/B#	-7.5	5517.7825	65	50	
60	V_{SS}	-7.5	5587.7825	65	50	2
61	V_{CCQ}	-7.5	5657.7825	65	50	2
62	V_{REFQ}	-7.5	5727.7825	65	50	
63	V_{SSQ}	-7.5	5797.7825	65	50	2
64	ZQ	-7.5	5917.7825	65	50	
65	V_{CCQ}	-7.5	6187.9325	65	50	2
66	DNU	-7.5	6381.2675	65	50	3
67	V_{SS}	-7.5	6451.2675	65	50	2
68	DNU	-7.5	6521.2675	65	50	3
69	V_{CC}	-7.5	6591.2675	65	50	2
70	V_{CC}	-7.5	6661.2675	65	50	2
71	V_{CC}	-7.5	6731.2675	65	50	2
72	V_{CC}	-7.5	6801.2675	65	50	2
73	V_{SS}	-7.5	6871.2675	65	50	2
74	V_{SS}	0	6941.2675	80	50	2

Notes:
1. Reference is to center of each bond pad from center of die.
2. All die V_{CC} and V_{SS} pads must have separate connections.
3. DNU = do not use.
4. See "Multiple-Die Stack Configurations" on page 11 for bonding configuration.
5. NC = No Connect internally.
6. V_{PP} is not supported.

Table 2: Bond Pad Location from Die Center

		Coordinates from Center of Pad 1 (0,0)		Passivation Openings		
Pad #	Pad Name	Xµm[1]	Yµm[1]	Xµm	Yµm	Notes
1	V_{SS}	-2599.85	-3542.758	80	50	2
2	V_{SS}	-2607.35	-3472.758	65	50	2
3	V_{SS}	-2607.35	-3402.758	65	50	2
4	V_{CC}	-2607.35	-3332.758	65	50	2
5	V_{CC}	-2607.35	-3262.758	65	50	2
6	V_{CC}	-2607.35	-3192.758	65	50	2
7	V_{CC}	-2607.35	-3122.758	65	50	2
8	V_{SS}	-2607.35	-3052.758	65	50	2
9	V_{PP}	-2607.35	-2982.758	65	50	6
10	DNU	-2607.35	-2872.758	65	50	3
11	DNU	-2607.35	-2762.025	65	50	3
12	MDS2	-2607.35	-2692.025	65	50	4
13	NC	-2607.35	-2622.025	65	50	5
14	MDS1	-2607.35	-2552.025	65	50	4
15	MDS0	-2607.35	-2482.025	65	50	4
16	V_{CC}	-2607.35	-2412.025	65	50	2
17	V_{CC}	-2607.35	-2314.025	65	50	2
18	V_{CC}	-2607.35	-2213.025	65	50	2
19	V_{CC}	-2607.35	-2115.025	65	50	2
20	WP#	-2607.35	-2045.025	65	50	
21	NC	-2607.35	-1975.025	65	50	5
22	ALE	-2607.35	-1905.025	65	50	
23	NC	-2607.35	-1835.025	65	50	5
24	CLE	-2607.35	-1765.025	65	50	
25	NC	-2607.35	-1695.025	65	50	5
26	V_{SS}	-2607.35	-1625.025	65	50	2
27	V_{SSQ}	-2607.35	-1555.025	65	50	2
28	DQ0	-2607.35	-1455.025	65	50	
29	V_{CCQ}	-2607.35	-1348.775	65	105	2
30	DQ1	-2607.35	-1242.525	65	50	
31	V_{SSQ}	-2607.35	-1142.525	65	50	2
32	V_{SSQ}	-2607.35	-895.025	65	50	2
33	DQ2	-2607.35	-795.025	65	50	
34	V_{CCQ}	-2607.35	-688.775	65	105	2
35	DQ3	-2607.35	-582.525	65	50	
36	V_{SSQ}	-2607.35	-482.525	65	50	2
37	RE_c	-2607.35	-382.525	65	50	
38	V_{CCQ}	-2607.35	-276.275	65	105	2
39	RE# (RE_t)	-2607.35	-170.025	65	50	
40	V_{SSQ}	-2607.35	70.025	65	50	2
41	DQS_c	-2607.35	170.025	65	50	
42	V_{CCQ}	-2607.35	276.275	65	105	2
43	DQS (DQS_t)	-2607.35	382.525	65	50	

Table 2: Bond Pad Location from Die Center

		Coordinates from Center of Pad 1 (0,0)		Passivation Openings		
Pad #	Pad Name	Xµm[1]	Yµm[1]	Xµm	Yµm	Notes
44	V_{SSQ}	-2607.35	482.525	65	50	2
45	DQ4	-2607.35	582.525	65	50	
46	V_{CCQ}	-2607.35	688.775	65	50	2
47	DQ5	-2607.35	795.025	65	50	
48	V_{SSQ}	-2607.35	895.025	65	50	2
49	V_{SSQ}	-2607.35	1142.525	65	50	2
50	DQ6	-2607.35	1242.525	65	50	
51	V_{CCQ}	-2607.35	1348.775	65	105	2
52	DQ7	-2607.35	1455.025	65	50	
53	V_{SSQ}	-2607.35	1555.025	65	50	2
54	WE#	-2607.35	1625.025	65	50	
55	NC	-2607.35	1695.025	65	50	5
56	CE#	-2607.35	1765.025	65	50	
57	NC	-2607.35	1835.025	65	50	5
58	NC	-2607.35	1905.025	65	50	5
59	R/B#	-2607.35	1975.025	65	50	
60	V_{SS}	-2607.35	2045.025	65	50	2
61	V_{CCQ}	-2607.35	2115.025	65	50	2
62	V_{REFQ}	-2607.35	2185.025	65	50	
63	V_{SSQ}	-2607.35	2255.025	65	50	2
64	ZQ	-2607.35	2375.025	65	50	
65	V_{CCQ}	-2607.35	2645.175	65	50	2
66	DNU	-2607.35	2838.51	65	50	3
67	V_{SS}	-2607.35	2908.51	65	50	2
68	DNU	-2607.35	2978.51	65	50	3
69	V_{CC}	-2607.35	3048.51	65	50	2
70	V_{CC}	-2607.35	3118.51	65	50	2
71	V_{CC}	-2607.35	3188.51	65	50	2
72	V_{CC}	-2607.35	3258.51	65	50	2
73	V_{SS}	-2607.35	3328.51	65	50	2
74	V_{SS}	-2599.85	3398.51	80	50	2

Notes:
1. Reference is to center of each bond pad from center of pad 1.
2. All die V_{CC} and V_{SS} pads must have separate connections.
3. DNU = do not use.
4. See "Multiple-Die Stack Configurations" on page 11 for bonding configuration.
5. NC = No Connect internally. This pad is not connected internally to any circuitry in NAND die.
6. V_{PP} is not supported.

Multiple-Die Stack Configurations

More than one NAND die can be stacked into a package. It is possible for two or four die to share a single CE# signal. When two or four die are connected to a single CE#, this permits Multi-LUN operations.

The multiple-die stack (MDS) bond pads are used to configure the NAND die to share a single CE#.

Table 3: MDS Bonding Configuration

Die per CE#	Configuration	MDS2	MDS1	MDS0	Enable Address
1	Die 0	DNU[1]	DNU	DNU	–
2	Die 0	GND[2]	DNU	DNU	LA0 = 0
	Die 1	GND	DNU	GND	LA0 = 1
4	Die 0	DNU	GND	DNU	LA1 = 0, LA0 = 0
	Die 1	DNU	GND	GND	LA1 = 0, LA0 = 1
	Die 2	GND	GND	DNU	LA1 = 1, LA0 = 0
	Die 3	GND	GND	GND	LA1 = 1, LA0 = 1

Notes: 1. DNU = do not use.
2. GND = ground.

Device and Array Organization

Figure 3: Example Device Organization for Single-Die Package

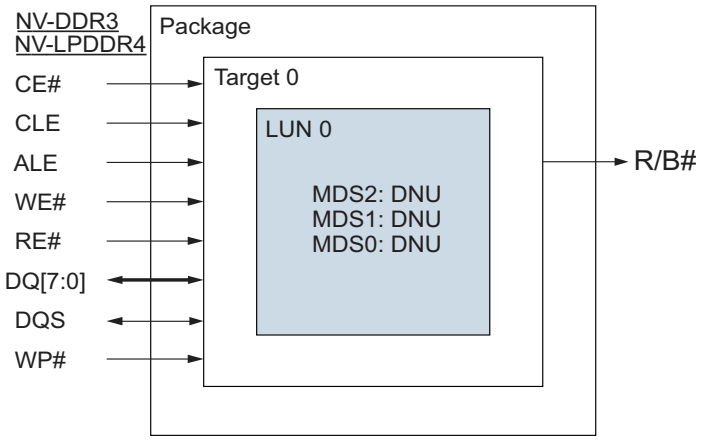


Figure 4: Example Device Organization for Two-Die Package with Single CE#, Single I/O Channel

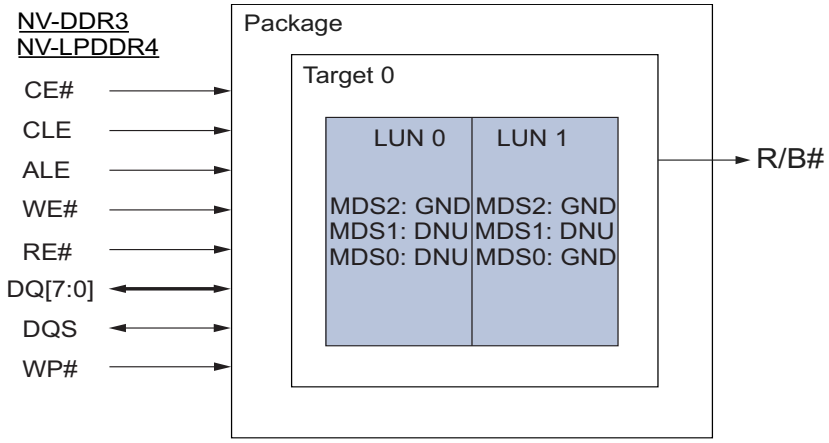


Figure 5: Example Device Organization for Two-Die Package with Two CE#s, Two I/O Channel

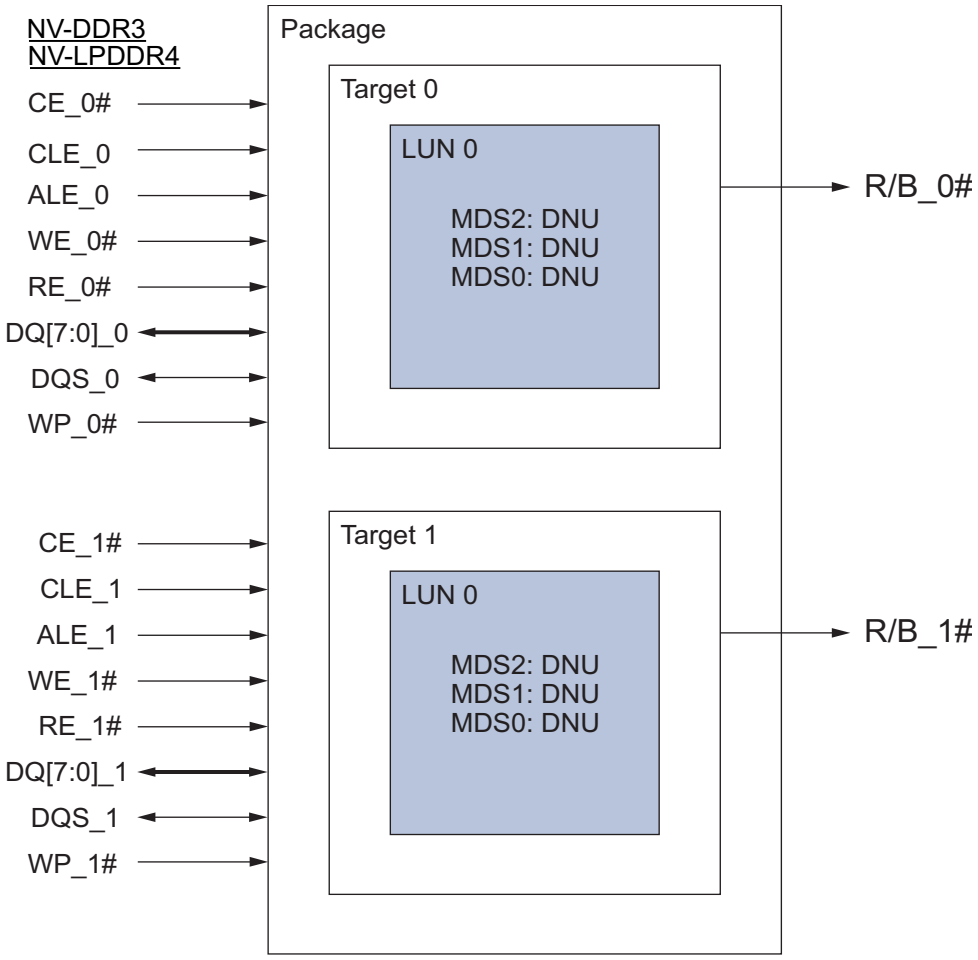


Figure 6: Example Device Organization for Four-Die Package with Single CE#, Single I/O Channel

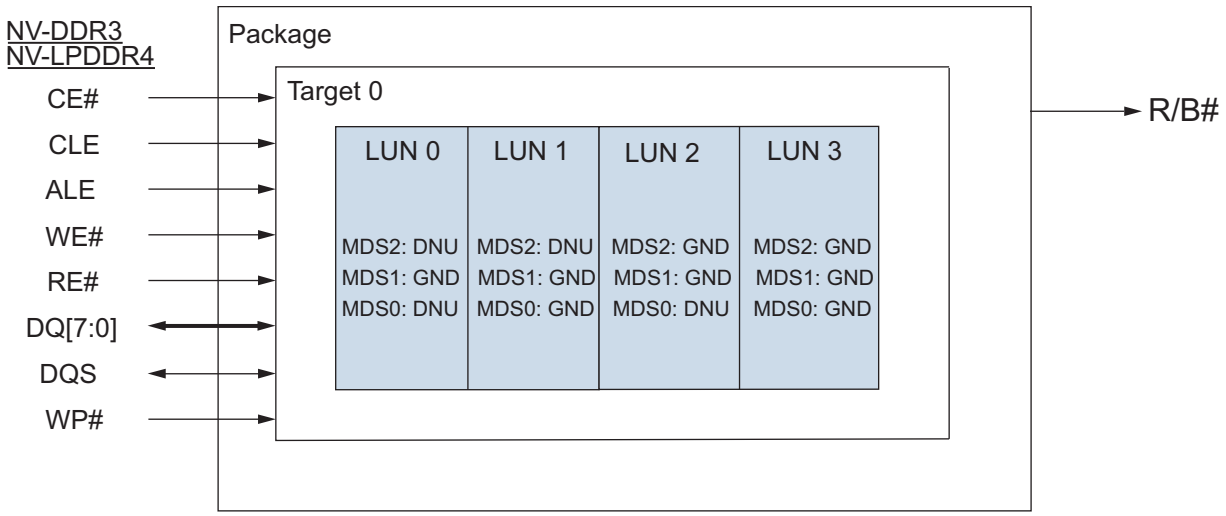


Figure 7: Array Organization per Logical Unit (LUN) in TLC mode

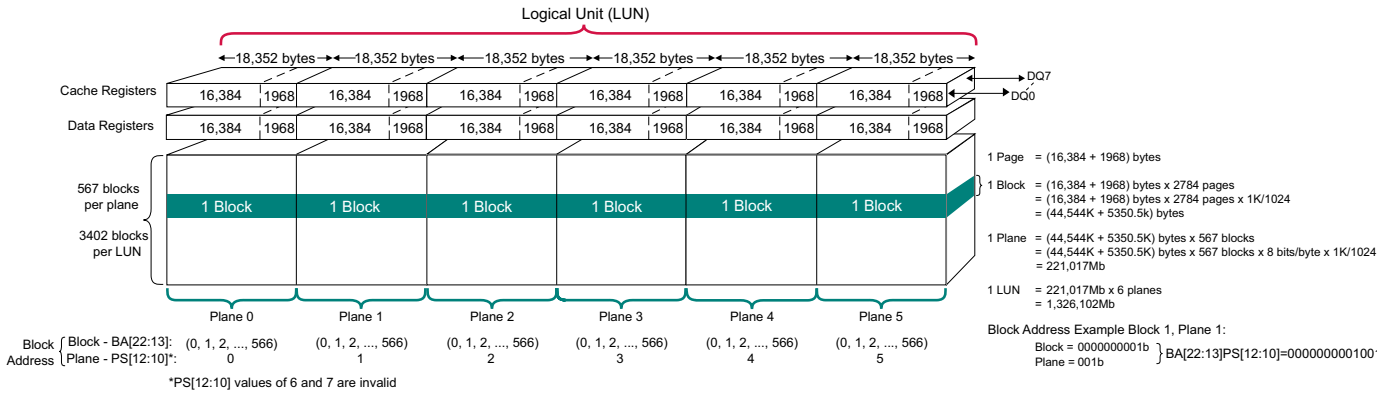


Table 4: Array Addressing for Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	PS12[5]	PS11[5]	PS10[5]	PA9[4]	PA8
Fifth	LA0[6, 7]	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LA1[6, 7]

Notes:
1. CAx = column address, PAx = page address, PSx = plane select, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, fifth, and sixth cycles containing the row addresses cycles are known as R1, R2, R3, and R4 respectively.
2. For NV-DDR3 or NV-LPDDR4 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. CA [14:0] address column addresses 0 through 18,351 (16,384 + 1968) (47AFh), therefore column addresses 18,352 (47B0h) through 32,767(7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. PA [9:0] address page addresses 0 through 935 (03A7h), therefore page addresses 936 (03A8h) through 1023 (3FFh) are invalid, out of bounds, and do not exist in the device. It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds pages.
5. PS[12:10] are the plane-select bits:
   Plane 0: PS[12:10] = 000b
   Plane 1: PS[12:10] = 001b
   Plane 2: PS[12:10] = 010b
   Plane 3: PS[12:10] = 011b
   Plane 4: PS[12:10] = 100b
   Plane 5: PS[12:10] = 101b
   Invalid: PS[12:10] = 110b
   Invalid: PS[12:10] = 111b
   PS[12:10] address planes 0 through 5, therefore plane addresses 6 and 7 are invalid, out of bounds, do not exist in the device, and cannot be addressed. Any command incorrectly using these address bits would be considered an invalid operation. Please see on how to properly handle these invalid address ranges.

6. LA0, LA1 are the LUN-select bits. They are present only when two or more LUNs are shared on the target; otherwise, they should be held LOW.
   LUN 0: LA0 = 0, LA1 = 0
   LUN 1: LA0 = 1, LA1 = 0
   LUN 2: LA0 = 0, LA1 = 1
   LUN 3: LA0 = 1, LA1 = 1
7. For single LUN Targets block addresses 3402 through 4095 are invalid, out of bounds, and do not exist in the device.
   For two LUN Targets block addresses 3402 through 4095 and 7498 through 8191 are invalid, out of bounds, and do not exist in the device.
   For four LUN Targets block addresses 3402 through 4095, 7498 through 8191, 11,594 through 12,287, and 15,690 through 16,383 are invalid, out of bounds, and do not exist in the device.
   It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds blocks.

Figure 8: Array Organization per Logical Unit (LUN) in SLC mode

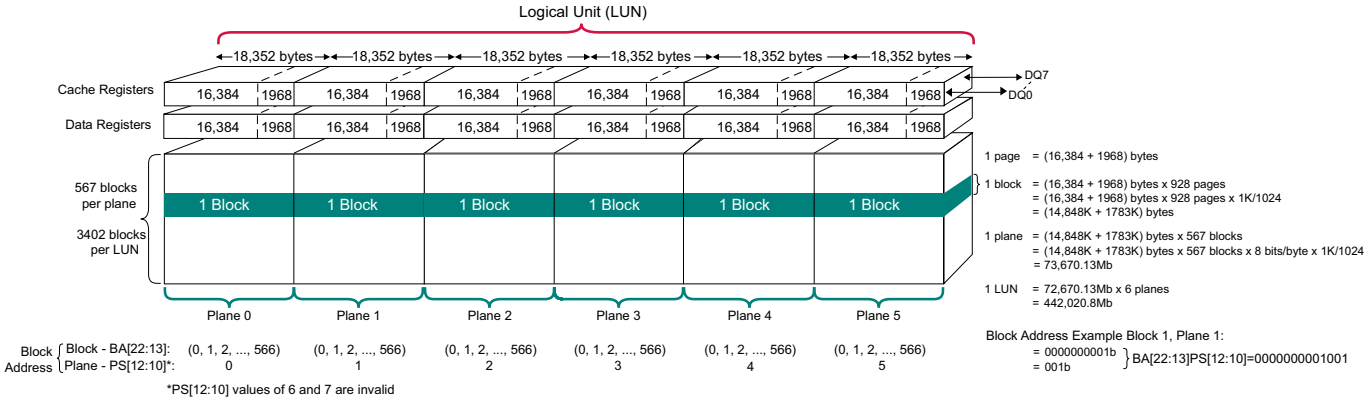


Table 5: Array Addressing for Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	PS13	PS12[5]	PS11[5]	PS10[5]	PA9[4]	PA8
Fifth	LA0[6, 7]	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LA1[6, 7]

Notes:
1. CAx = column address, PAx = page address, PSx = plane select, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, fifth, and sixth cycles containing the row addresses cycles are known as R1, R2, R3, and R4 respectively.
2. For NV-DDR3 or NV-LPDDR4 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. CA [14:0] address column addresses 0 through 18,351 (16,384 + 1968) (47AFh), therefore column addresses 18,352 (47B0h) through 32,767(7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. PA [9:0] address page addresses 0 through 927 (39Fh), therefore page addresses 928 (3A0h) through 1023 (3FFh) are invalid, out of bounds, and do not exist in the device. It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds pages.
5. PS[12:10] are the plane-select bits:
   Plane 0: PS[12:10] = 000b
   Plane 1: PS[12:10] = 001b
   Plane 2: PS[12:10] = 010b
   Plane 3: PS[12:10] = 011b
   Plane 4: PS[12:10] = 100b
   Plane 5: PS[12:10] = 101b
   Invalid: PS[12:10] = 110b
   Invalid: PS[12:10] = 111b
   PS[12:10] address planes 0 through 5, therefore plane addresses 6 and 7 are invalid, out of bounds, do not exist in the device, and cannot be addressed. Any command incorrectly using these address bits would be considered an invalid operation. Please see on how to properly handle these invalid address ranges.

6. LA0, LA1 are the LUN-select bits. They are present only when two or more LUNs are shared on the target; otherwise, they should be held LOW.
   LUN 0: LA0 = 0, LA1 = 0
   LUN 1: LA0 = 1, LA1 = 0
   LUN 2: LA0 = 0, LA1 = 1
   LUN 3: LA0 = 1, LA1 = 1
7. For single LUN Targets block addresses 3402 through 4095 are invalid, out of bounds, and do not exist in the device.
   For two LUN Targets block addresses 3402 through 4095 and 7498 through 8191 are invalid, out of bounds, and do not exist in the device.
   For four LUN Targets block addresses 3402 through 4095, 7498 through 8191, 11,594 through 12,287, and 15,690 through 16,383 are invalid, out of bounds, and do not exist in the device.
   It is not allowed to issue any PROGRAM, READ, ERASE, or any other array operation on out of bounds blocks.

Identification Operations for Multiple-Die Stack Configurations

The data returned by the READ ID (90h) and READ PARAMETER PAGE (ECh) commands are different depending on the MDS configuration (see Multiple-Die Stack Configurations).

Table 6: READ ID Parameters for Address 00h

Die per CE#	READ ID Values							
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
1	2Ch	D3h	08h	32h	EAh	30h	00h	00h
2	2Ch	E3h	89h	32h	EAh	30h	00h	00h
4	2Ch	F3h	8Ah	32h	EAh	30h	00h	00h

Note: 1. h = hexadecimal.

Table 7: READ ID Parameters for Address 20h

Die per CE#	READ ID Values				
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
All	4Fh	4Eh	46h	49h	01h

Note: 1. h = hexadecimal.

Table 8: READ ID Parameters for Address 40h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
All	4Ah	45h	44h	45h	43h	19h

Note: 1. h = hexadecimal.

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
4–5	Revision number Bit[15:13]: Reserved (0) Bit 12: 1 = supports ONFI version 5.0 Bit 11: 1 = supports ONFI version 4.2 Bit 10: 1 = supports ONFI version 4.1 Bit 9: 1 = supports ONFI version 4.0 Bit 8: 1 = supports ONFI version 3.2 Bit 7: 1 = supports ONFI version 3.1 Bit 6: 1 = supports ONFI version 3.0 Bit 5: 1 = supports ONFI version 2.3 Bit 4: 1 = supports ONFI version 2.2 Bit 3: 1 = supports ONFI version 2.1 Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	00h, 10h
6–7	Features supported[2] Bit15: 1 = supports Package Electrical Specification Bit 14: 1 = supports ZQ calibration Bit 13: 1 = supports NV-DDR3 Bit 12: 1 = supports external V_{PP} Bit 11: 1 = supports Volume addressing Bit 10: 1 = supports NV-DDR2 interface Bit 9: 1 = supports NV-LPDDR4 Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports extended parameter page Bit 6: 1 = supports interleaved (multi-plane) read operations Bit 5: 1 = supports NV-DDR interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	1	D8h, EDh
		2	DAh, EDh
		4	
8–9	Optional commands supported Bit[15:14]: Reserved (0) Bit 13: 1 = supports ZQ calibration (Long and Short) Bit 12: 1 = supports GET/SET Features by LUN Bit 11: 1 = supports ODT CONFIGURE Bit 10: 1 = supports VOLUME SELECT Bit 9: 1 = supports RESET LUN Bit 8: 1 = supports small data move Bit 7: 1 = supports CHANGE ROW ADDRESS Bit 6: 1 = supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports READ STATUS ENHANCED Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE	–	FFh, 3Fh

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
10	ONFI-JEDEC JTG primary advanced command support Bit[7:4]: Reserved (0) Bit 3: 1 = supports ERASE BLOCK MULTI-PLANE Bit 2: 1 = supports COPYBACK PROGRAM MULTI-PLANE Bit 1: 1 = supports PROGRAM PAGE MULTI-PLANE Bit 0: 1 = supports CHANGE READ COLUMN	–	0Fh
11	Training commands supported Bit[7:5]: Reserved (0) Bit 4: 1 = Supports write Rx DQ training Bit 3: 1 = Supports write Tx DQ training Bit 2: 1 = Supports read DQ training Bit 1: 1 = Supports implicit (command based) DCC training Bit 0: 1 = Supports explicit DCC training	–	0Dh
12–13	Extended parameter page length	–	03h, 00h
14	Number of parameter pages	–	3Ch
15–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) SpecTek	–	53h, 70h, 65h, 63h, 54h, 65h, 6bh, 20h, 20h, 20h, 20h, 20h
44–63	Device model (20 ASCII characters)[2]	–	not defined
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	B0h, 07h
86–91	Reserved (0)	–	All 00h
92–95	Number of pages per block	–	40h, 08h, 00h, 00h
96–99	Number of blocks per LUN	–	B0h, 08h, 00h, 00h
100	Number of LUNs per chip enable	1	01h
		2	02h
		4	04h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	24h
102	Number of bits per cell	–	03h
103–104	Bad blocks maximum per LUN	–	2Ch, 01h
105–106	Block endurance[2]	–	01h, 03h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid block	–	00h, 00h
110	Number of programs per page	–	01h
111	Reserved (0)	–	00h
112	Number of bits ECC correctability	–	FFh

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	03h
114	Interleaved operation attributes Bit[7:6]: Reserved (0) Bit 5: Reserved Bit 4: 1 = supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = PROGRAM CACHE supported Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	1Eh
115	Reserved (0)	–	00h
116–117	NV-DDR3 timing mode support Bit[15:1]: Reserved (0) Bit 0: supports timing mode 19	–	00h, 00h
118–121	NV-LPDDR4 timing mode support Bit[31:17]: Reserved (0) Bit 16: 1 = supports timing mode 19 Bit 15: 1 = supports timing mode 18 Bit 14: 1 = supports timing mode 17 Bit 13: 1 = supports timing mode 16 Bit 12: 1 = supports timing mode 15 Bit 11: 1 = supports timing mode 14 Bit 10: 1 = supports timing mode 13 Bit 9: 1 = supports timing mode 12 Bit 8: 1 = supports timing mode 11 Bit 7: 1 = supports timing mode 10 Bit 6: 1 = supports timing mode 9 Bit 5: 1 = supports timing mode 8 Bit 4: 1 = supports timing mode 7 Bit 3: 1 = supports timing mode 6 Bit 2: 1 = supports timing mode 5 Bit 1: 1 = supports timing mode 4 Bit 0: 1 = supports timing mode 0 to 3	–	FFh, 1Fh, 00h, 00h
122–127	Reserved (0)	–	All 00h
Electrical parameters block			
128	Reserved (0)	–	00h
129–130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
131–140	Reserved (0)	–	All 00h

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
141	NV-DDR timing mode support Bit[7:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h
142	NV-DDR2 timing mode support Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	00h
143	NV-DDR/NV-DDR2 features Bit[7:4]: Reserved (0) Bit 3: 0 = device does not require V_{PP} enablement sequence Bit 2: 1 = devices support CLK stopped for data input Bit 1: 1 = typical capacitance values present Bit 0: 0 = use ^{t}CAD MIN value	–	00h
144–150	Reserved (0)	–	All 00h
151	Driver strength support.If the device supports NV-DDR3 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. Bit[7:5]:Reserved (0) Bit 4: 1 = supports 35 Ohm, 37.5 Ohm, and 50 Ohm drive strength (Default is 35 Ohm) Bit 3: 1 = supports 37.5 Ohm and 50Ohm drive strength (Default is 37.5 Ohm) Bit 2: 1 = supports 18 Ohm driver strength Bit 1: 1 = supports 25 Ohm driver strength Bit 0: 1 = supports 35 Ohm and 50 Ohm driver strength (Default is 35 Ohm)	–	08h
152–157	Reserved (0)	–	All 00h
158	NV-DDR2/3 features Bit[7:6]: Reserved (0) Bit 5: 0 = external V_{REFQ} is required for >= 200MT/s Bit 4: 1 = supports differential signaling for DQS Bit 3: 1 = supports differential signaling for RE# Bit 2: 1 = supports ODT value of 30 ohms Bit 1: 1 = supports matrix termination ODT Bit 0: 1 = supports self-termination ODT	–	1Bh
159	NV-DDR2/3 warmup cycles Bit[7:4]: Data input warmup cycles support Bit[3:0]: Data output warmup cycles support	–	44h

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
160–161	NV-DDR3 timing mode support[2] Bit[15:13]: Reserved (0) Bit 15: 1 = supports timing mode 18 Bit 14: 1 = supports timing mode 17 Bit 13: 1 = supports timing mode 16 Bit 12: 1 = Supports timing mode 15 Bit 11: 1 = Supports timing mode 14 Bit 10: 1 = Supports timing mode 13 Bit 9: 1 = Supports timing mode 12 Bit 8: 1 = Supports timing mode 11 Bit 7: 1 = Supports timing mode 10 Bit 6: 1 = Supports timing mode 9 Bit 5: 1 = Supports timing mode 8 Bit 4: 1 = Supports timing mode 7 Bit 3: 1 = Supports timing mode 6 Bit 2: 1 = Supports timing mode 5 Bit 1: 1 = Supports timing mode 4 Bit 0: 1 = Supports timing mode 0 to 3	–	FFh, 1Fh
162	NV-DDR2 timing mode support[2] Bit [7:3]: Reserved (0) Bit 2: 1 = supports timing mode 10 Bit 1: 1 = supports timing mode 9 Bit 0: 1 = supports timing mode 8	–	00h
163	Reserved (0)	–	All 00h
Vendor block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support SpecTek-specific read cache function	–	00h
168	Reserved (0)	–	All 00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	–	00h
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable DQ output impedance settings	–	02h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	04h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	–	1Ch
179	OTP Feature Address	–	90h
180	Read Retry Options Bit[7:5]: Reserved (0) Bit[4:0] = Number of Read Retry options supported	–	00h
181–184	Read Retry Options available. A value of ‘1’ in a bit position shows that Read Retry option is available for use. A value of ‘0’ in a bit position shows that Read Retry option is not available for use. For example, the binary value of ‘37h, 00h, 00h, 00h’ would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	–	00h, 00h, 00h, 00h
185	LDPC requirement Bit[7:1]: Reserved (0) Bit 0: 1 =LDPC ECC is required	–	01h
186	Address cycle read retry (ACRR) enablement Feature Address		96h
187–188	Address Cycle Read Retry (ACRR) subfeature position for enablement and subfeature bit position for enablement Bits[15:12]: Reserved (0) Bits[11:8]: Subfeature for enablement Bits[7:0]: Subfeature bit position for enablement		01h, 04h
189–192	Address cycle read retry (ACRR) Options available. A value of ‘1’ in a bit position shows that ACRR option is available for use. A value of ‘0’ in a bit position shows that ACRR option is not available for use.		FFh, 00h, 00h, 00h
193–194	SLC mode support Bits[15:3]: Reserved (0) Bit[2] 1 = Factory Reserved Setting Bit[1:0] 11 = Op-Code 3Bh supported only Bit[1:0] 10 = Op-Codes 3Bh/3Chsupported only Bit [1:0] 01 = Feature Address 91h and op-codes 3Bh/3Ch supported only Bit [1:0] 00 = Feature Address 91h and op-codes DAh/DFh supported		03h, 00h
195–249	Reserved (0)	–	All 00h

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
250–252	Designator Bytes 1 to 3 (ASCII characters)[2] Byte 250 = Designator Byte 1 Byte 251 = Designator Byte 2 Byte 252 = Designator Byte 3	–	4Dh, 00h, 00h
253	Parameter page revision[2]	–	01h[2]
254–255	Integrity CRC[2]	1	04h, D5h
		2	15h, 85h
		4	D1h, D3h
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
...	...	–	...
15,104–15,359	Value of bytes 0–255	–	See bytes 0–255
Extended parameter pages			
15,360–15,615	Extended parameter page Integrity CRC[2]	–	0Ch, CFh
15,362–15,365	Extended parameter page signature Byte 0: 45h, “E” Byte 1: 50h, “P” Byte 2: 50h, “P” Byte 3: 53h, “S”	–	45h, 50h, 50h, 53h
15,366–15,375	Reserved (0)	–	All 00h
15,376	Section 0 type	–	02h
15,377	Section 0 length	–	01h
15,378–15,391	Reserved (0)	–	All 00h
15,392	Number of bits ECC correctability	–	9Bh
15,393	ECC codeword size	–	0Bh
15,394–15,395	Bad blocks maximum per LUN	–	2Ch, 01h
15,396–15,397	Block Endurance[2]	–	01h, 03h
15,398–15,407	Reserved (0)	–	All 00h
Redundant extended parameter pages			
15,408–15,455	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
15,456–15,503	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407
...	...	–	...
18,192–18,239	Value of bytes 15,360–15,407	–	See bytes 15,360–15,407

Table 9: ONFI Parameter Page Data Structure

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
18,240 to end of page	Reserved (FFh)	–	All FFh

Notes: 1. h = hexadecimal.
2. This value may not be reflective of the Media device datasheet specification.

Table 10: Parameter Page Data Structure for JEDEC

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Ah, "J" Byte 1: 45h, "E" Byte 2: 53h, "S" Byte 3: 44h, "D"	–	4Ah, 45h, 53h, 44h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports JEDEC version 1.0 Bit 1: 1 = supports vendor specific parameter page Bit 0: Reserved (0)	–	06h, 00h
6–7	Features supported[2] Bit[15:10]: Reserved (0) Bit 9: 1 = supports changing pin function between WP# and ODT# Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports external V_{PP} Bit 6: 1 = supports toggle mode DDR Bit 5: 1 = supports Synchronous interface Bit 4: 1 = supports MULTI-PLANE READ operations Bit 3: 1 = supports MULTI-PLANE PROGRAM and ERASE operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	1	18h, 01h
		2	1Ah, 01h
		4	
8–10	Features supported Bit[23:11]: Reserved (0) Bit 10: 1 = supports synchronous reset Bit 9: 1 = supports reset LUN (primary) Bit 8: 1 = supports small data move Bit 7: 1 = supports multi-plane copyback program (primary) Bit 6: 1 = supports random data out (primary) Bit 5: 1 = supports read unique ID Bit 4: 1 = supports copyback Bit 3: 1 = supports read status enhanced (primary) Bit 2: 1 = supports get features and set features Bit 1: 1 = supports READ CACHE commands Bit 0: 1 = supports PAGE CACHE PROGRAM command	–	FFh, 03h, 00h

Table 10: Parameter Page Data Structure for JEDEC

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
11–12	Secondary commands supported Bit[15:8]: Reserved (0) Bit 7: 1 = supports secondary READSTATUS ENHANCED Bit 6: 1 = supports secondary MULTI-PLANE BLOCK ERASE Bit 5: 1 = supports secondary MULTI-PLANE COPYBACK PROGRAM Bit 4: 1 = supports secondary MULTI-PLANE PROGRAM Bit 3: 1 = supports secondary RANDOMDATA OUT Bit 2: 1 = supports secondary MULTI-PLANE COPYBACK READ Bit 1: 1 = supports secondary MULTI-PLANE READ CACHE RANDOM Bit 0: 1 = supports secondary MULTI-PLANE READ	–	58h, 00h
13	Number of parameter pages	–	23h
14–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) SpecTek	–	53h, 70h, 65h, 63h, 54h, 65h, 6bh, 20h, 20h, 20h, 20h, 20h
44–63	Device model (20 ASCII characters)[2]	–	not defined
64–69	JEDEC manufacturer ID	–	2Ch, 00h, 00h, 00h, 00h, 00h
70–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	B0h, 07h
86–89	Number of data bytes per partial page	–	00h, 08h, 00h, 00h
90–91	Number of spare bytes per partial page	–	F6h, 00h
92–95	Number of pages per block	–	E0h, 0Ah, 00h, 00h
96–99	Number of blocks per LUN	–	4Ah, 0Dh, 00h, 00h
100	Number of LUNs per chip enable	1	01h
		2	02h
		4	04h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	24h
102	Number of bits per cell	–	03h
103	Number of programs per page	–	01h
104	Multi-plane operation addressing Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	02h
105	Multi-plane operation attributes Bit[7:3]: Reserved (0) Bit 2: 1 = address restrictions for CACHE operations Bit 1: 1 = READ CACHE operations supported Bit 0: 1 = PROGRAM CACHE operations supported	–	07h
106–143	Reserved (0)	–	All 00h
Electrical parameters block			

Table 10: Parameter Page Data Structure for JEDEC

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
144–145	Asynchronous SDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
146–147	Synchronous DDR2 speed grade support Bit[15:11]: Reserved (0) Bit 10: 1 = supports timing mode 10 Bit 9: 1 = supports timing mode 9 Bit 8: 1 = supports timing mode 8 Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
148–149	Synchronous DDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	00h, 00h
150	Asynchronous SDR features Bit[7:0]: Reserved (0)	–	00h
151	Reserved (0)	–	00h
152	Synchronous DDR features Bit[7:2]: Reserved (0) Bit 1: 1 = devices leave CLK running for data input Bit 0: 0 = use ^{t}CAD MIN value	–	00h
153–154	^{t}PROG maximum PROGRAM PAGE time (µs)[2]	–	8Ch, 0Ah
155–156	^{t}BERS maximum BLOCK ERASE time (µs)[2]	–	38h, 4Ah
157–158	^{t}R maximum PAGE READ time (µs)[2]	–	46h, 00h
159–160	^{t}R maximum Multi-PLANE PAGE READ time (µs)[2]	–	46h, 00h
161–162	^{t}CCS minimum change column setup time (ns)[2]	–	13h, 01h
163–164	I/O pin capacitance, typical	–	00h, 00h
165–166	Input capacitance, typical	–	10h, 00h
167–168	CLK input pin capacitance, typical	–	00h, 00h

Table 10: Parameter Page Data Structure for JEDEC

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
169	Driver strength support. If the device supports NV-DDR, NV-DDR2, or NVDDR3 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. Bit[7:5]: Reserved (0) Bit 4: 1 = Supports 35 ohm, 37.5 ohm, and 50 ohm drive strength (default is 35 ohm) Bit 3: 1 = Supports 37.5 ohm and 50ohm drive strength (default is 37.5 ohm) Bit 2: 1 = Supports 18 ohm driver strength Bit 1: 1 = Supports 25 ohm driver strength Bit 0: 1 = Supports 35 ohm and 50 ohm driver strength (default is 3 ohm)	–	08h
170–171	^{t}ADL program page register clear enhancement value (ns)	–	96h, 00h
172–175	DDR3 speed grade support Bit[31:18]: Reserved (0) Bit 17: 1 = supports 0.833 ns speed grade (~1200 MHz) Bit 16: 1 = supports 0.909 ns speed grade (~1100 MHz) Bit 15: 1 = supports 1.0 ns speed grade (1000 MHz) Bit 14: 1 = supports 1.111 ns speed grade (~900 MHz) Bit 13: 1 = supports 1.25 ns speed grade (800 MHz) Bit 12: 1 = supports 1.667 ns speed grade (~600 MHz) Bit 11: 1 = supports 1.875 ns speed grade (~533 MHz) Bit 10: 1 = supports 2.5 ns speed grade (400 MHz) Bit 9: 1 = supports 3 ns speed grade (~333 MHz) Bit 8: 1 = supports 3.75 ns speed grade (~266 MHz) Bit 7: 1 = supports 5 ns speed grade (200 MHz) Bit 6: 1 = supports 6 ns speed grade (~166 MHz) Bit 5: 1 = supports 7.5 ns speed grade (~133 MHz) Bit 4: 1 = supports 10 ns speed grade (100 MHz) Bit 3: 1 = supports 12 ns speed grade (~83 MHz) Bit 2: 1 = supports 15 ns speed grade (~66 MHz) Bit 1: 1 = supports 25 ns speed grade (40 MHz) Bit 0: 1 = supports 30 ns speed grade (~33 MHz)		FFh, 3Fh, 00h, 00h

Table 10: Parameter Page Data Structure for JEDEC

Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
176–179	NV-LPDDR4 speed grade Bit[31:18]: Reserved (0) Bit 17: 1 = supports 0.833 ns speed grade (~1200 MHz) Bit 16: 1 = supports 0.909 ns speed grade (~1100 MHz) Bit 15: 1 = supports 1.0 ns speed grade (1000 MHz) Bit 14: 1 = supports 1.111 ns speed grade (~900 MHz) Bit 13: 1 = supports 1.25 ns speed grade (800 MHz) Bit 12: 1 = supports 1.667 ns speed grade (~600 MHz) Bit 11: 1 = supports 1.875 ns speed grade (~533 MHz) Bit 10: 1 = supports 2.5 ns speed grade (400 MHz) Bit 9: 1 = supports 3 ns speed grade (~333 MHz) Bit 8: 1 = supports 3.75 ns speed grade (~266 MHz) Bit 7: 1 = supports 5 ns speed grade (200 MHz) Bit 6: 1 = supports 6 ns speed grade (~166 MHz) Bit 5: 1 = supports 7.5 ns speed grade (~133 MHz) Bit 4: 1 = supports 10 ns speed grade (100 MHz) Bit 3: 1 = supports 12 ns speed grade (~83 MHz) Bit 2: 1 = supports 15 ns speed grade (~66 MHz) Bit 1: 1 = supports 25 ns speed grade (40 MHz) Bit 0: 1 = supports 30 ns speed grade (~33 MHz)	–	FFh, 3Fh, 00h, 00h
180–207	Reserved (0)	–	00h
Vendor block			
208	Guaranteed valid block sat beginning of target	–	01h
209–210	Block endurance for guaranteed valid blocks	–	00h, 00h
211	Number of bits ECC correctability	–	9Bh
212	ECC codeword size	–	0Bh
213–214	Bad blocks maximum per LUN	–	2Ch, 01h
215–216	Block Endurance	–	01h, 03h
217–218	Reserved (0)	–	All 00h
219–271	Reserved (0)	–	All 00h
Redundant parameter pages			
272–419	Reserved (0)	–	All 00h
Extended parameter pages			
420–421	Vendor-specific revision number	–	01h, 00h
422	Read retry options Bit[7:5]: Reserved (0) Bit[4:0]: Number of read retry options supported	–	00h
423–426	Read retry options available. A value of ‘1’ in a bit position shows that read retry option is available for use. A value of ‘0’ in a bit position shows that read retry option is not available for use. For example, the binary value of ‘37h, 00h, 00h, 00h’ would represent that read retry options 0, 1, 2, 4, and 5 are available, which would correspond to read retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that read retry options 3, 6, and 7 to 32, which would correspond to read retry input option selections 03h, 06h, 07h to 20h, are not available.	–	00h, 00h, 00h, 00h

Table 10: Parameter Page Data Structure for JEDEC

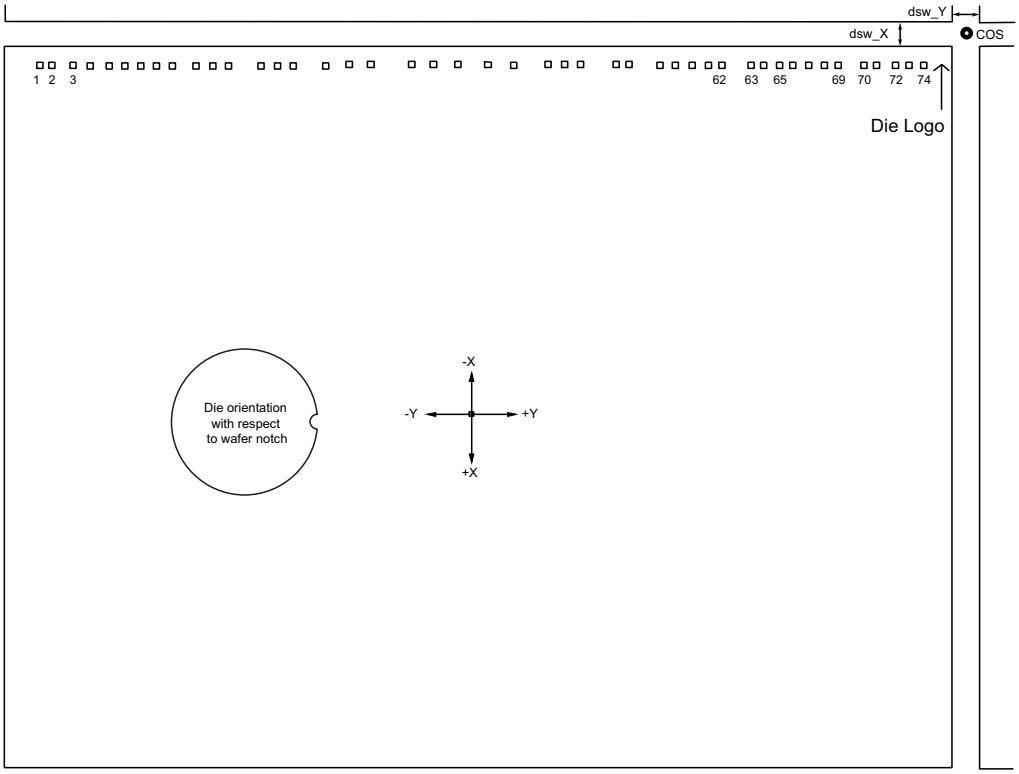
Note: Values are not guaranteed in wafer form.

Byte	Description	Die per CE# (Device P/N)	Values
427–429	Designator bytes 1 to 3(ASCII characters) Byte 427 = designator byte 1 Byte 428 = designator byte 2 Byte 429 = designator byte 3	–	4Dh, 00h, 00h
430	LDPC ECC requirement Bit[7:1]: Reserved (0) Bit 0: LDPC ECC is required	–	01h
431	Address cycle read retry (ACRR) enablement feature address		96h
432–433	Address Cycle Read Retry (ACRR) subfeature position for enablement and subfeature bit position for enablement Bits[15:12]: Reserved (0) Bits[11:8]: Subfeature for enablement Bits[7:0]: Subfeature bit position for enablement		01h, 04h
434–437	Address cycle read retry (ACRR) options available. A value of '1' in a bit position shows that ACRR option is available for use. A value of '0' in a bit position shows that ACRR option is not available for use.		FFh, 00h, 00h, 00h
438–439	SLC mode support Bits[15:3]: Reserved (0) Bit[2] 1 = Factory Reserved Setting Bit[1:0] 11 = Op-Code 3Bh supported only Bit[1:0] 10 = Op-Codes 3Bh/3Chsupported only Bit[1:0] 01 = Feature Address 91h and Op-Codes 3Bh/3Ch supported Bit[1:0] 00 = Feature Address 91h and Op-Codes DAh/DFh supported		03h, 00h
440–509	Reserved (0)	–	All 00h
CRC for parameter pages			
510–511	Integrity CRC	1	BFh, 48h
		2	10h, 99h
		4	AFh, EBh
Redundant extended parameter pages			
512–1023	See byte values 0–511	–	See bytes 0–511
1024–1535	See byte values 0–511	–	See bytes 0–511
...	...	–	...
17,408–17,919	See byte values 0–511	–	See bytes 0–511
17,920 to end of page	Reserved (FFh)	–	All FFh

Notes: 1. h = hexadecimal.
2. This value may not be reflective of the Media device datasheet specification.

Die Features and Physical Specifications

Figure 9: B58R Die Outline



Note: 1. Die is not drawn to scale. Dimensions are shown in the table below.

Table 11: Die Dimensions

Characteristic	Dimensions
Wafer diameter	300mm
Whole Wafer thickness	790µm ± 25µm
Reconstructed Wafter thickness	Varies from batch to batch
Die size (stepping interval)	5.4994mm x 12.7992mm
Street width along X-axis (dsw_X)	80µm
Street width along Y-axis (dsw_Y)	80µm
Bond pad size (MIN)	65µm x 50µm
Passivation openings (MIN)	65µm x 50µm
Minimum bond pad pitch	70µm

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Revision History

Rev A. 04/2022

- SpecTek initial release