CBM2099

USB 2.0 Flash Disk Controller

Datasheet

Rev 1.0

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Revision History

Date	Rev No	Description
2015-01-15	1.0	Initial release

Contents

1 Description

Fastest & Securest USB 2.0 Flash Disk Controller with dedicated 32-bit microprocessor

The CBM2099 is the USB 2.0 Flash Disk controller with the fastest transfer speed on the market. CBM2099 can reach theoretical flash access speed limit of over 32MByte/s for read and 20MByte/s for write.

The on-the-fly ECC engine is capable of correcting up to 72bits per 1024 bytes page . For data security, CBM2099 is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

The CBM2099 supports all 8 /16 bit BUS wide async NAND flash memory available in the market. New flash can be supported by software re-configuration.

The CBM2099 supports all 8 bit BUS wide ONFI/TOGGLE NAND flash memory available in the market. New flash can be supported by software re-configuration.

The CBM2099 has both a) 5V to 3.3V LDO and b) power on reset circuits integrated. Thus greatly reduced BOM cost and eased layout burden.

The CBM2099 runs smoothly with all available hosts and PC platforms. Complied with USB specification rev. 2.0, the CBM2099 can be supported without additional driver under Win XP, Win 2000, Windows Me, Mac OS and Linux OS. With device driver installed, it can support Win 98/98SE as well. Comprehensive applications, such as PC boot up, disk partitions, password check for security disk, are available as part of our standard mass production software package.

The CBM2099 is available in 48-pin TQFP package, which are thinnest and smallest on the market. The 48-pin CBM2099 support up to 8 flash chips.

2 Features

■ **USB Interface**

   High-speed USB 2.0 interface;

■ **Non-crystal support**

■ **Fastest data transfer rate on the market**

   Single-channel mode(16bit): 32MB/s for Read, 20MB/s for Write
   Single-channel mode(8bit): 26MB/s for Read, 20MB/s for Write
   Fastest file copy rate on the market.

■ **On-the-fly ECC built-in Hardware enhances reliability**

   ECC for NAND flash: 72 bit per page (1 page = 1024bytes)

■ **Special wear leveling algorithm to improve the flash life-time**

■ **Hardware & Software Data Protection Technology**

   Prevent data corruption even if it is powered off or unplugged during data transfer.

■ **SLC** & **MLC** & **TLC NAND Flash Interface**
Support 8-bit and 16-bit Samsung SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Toshiba SLC&MLC&TLC NAND flash
Support 8-bit and 16-bit Hynix SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Sandisk SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Micron/Intel SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit ST/Numony SLC&MLC NAND flash.
Support 8-bit and 16-bit Infineon SLC&MLC NAND flash.
Support PowerChip SLC&MLC Nand flash
Support Spansion 3.3V MirrorBit-Quad flash
Support Actrans Nand Flash
Support ONFI2.0 DDR mode flash
Support Samsung Toggle mode flash
Support 16K page flash
Supports up to 8 flash chips
Software configuration to support various new flash memories

■ **Proprietary 32-bit CISC microprocessor feature**

Proprietary 32-bit CISC processor for USB protocol processing and flash access.

Single cycle instruction period

■ **Integrated 5v to 3.3v voltage regulator**

■ **Disk partitions and password check for security disk available**

■ **PC boot up as USB Zip Disk, USB Hard Disk or USB CDROM**

■ **Auto run function**

■ **Low power dissipation**

Operating current 40mA (Bus power compatible)

■ **Build-in LDO**
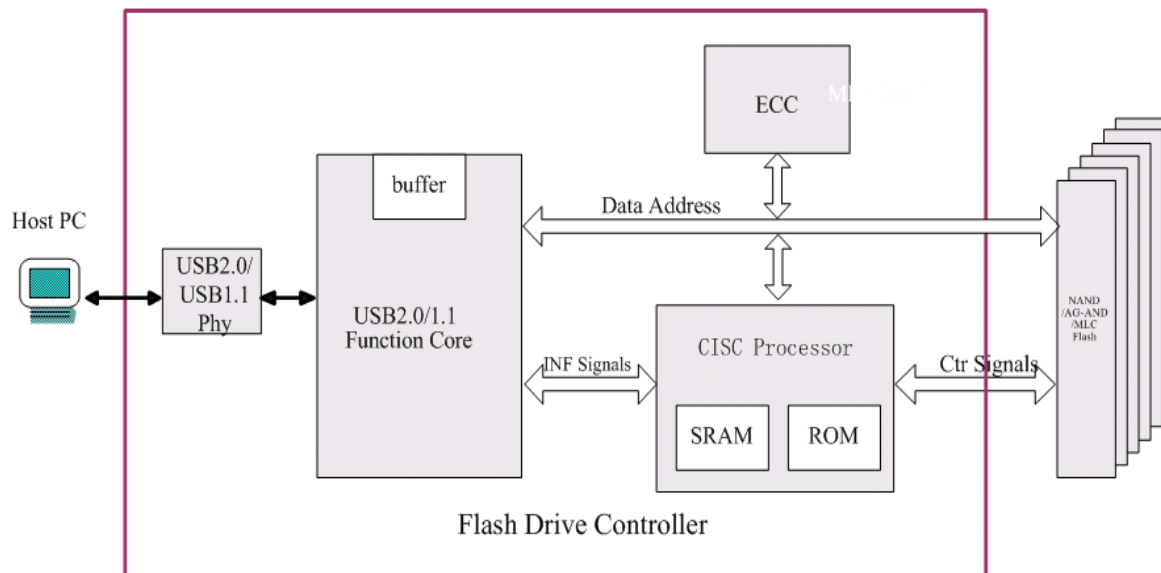
Output maximum current up to 200mA

■ **Leading 0.11um CMOS technology**

■ **48-pin TQFP**

48-pin CBM2099 supports up to 8 Flash Chips

Windows, Mac and Linux compatible

3 Block Diagram

4 Pin Assignment

4.1 TQFP48 (Top Side)
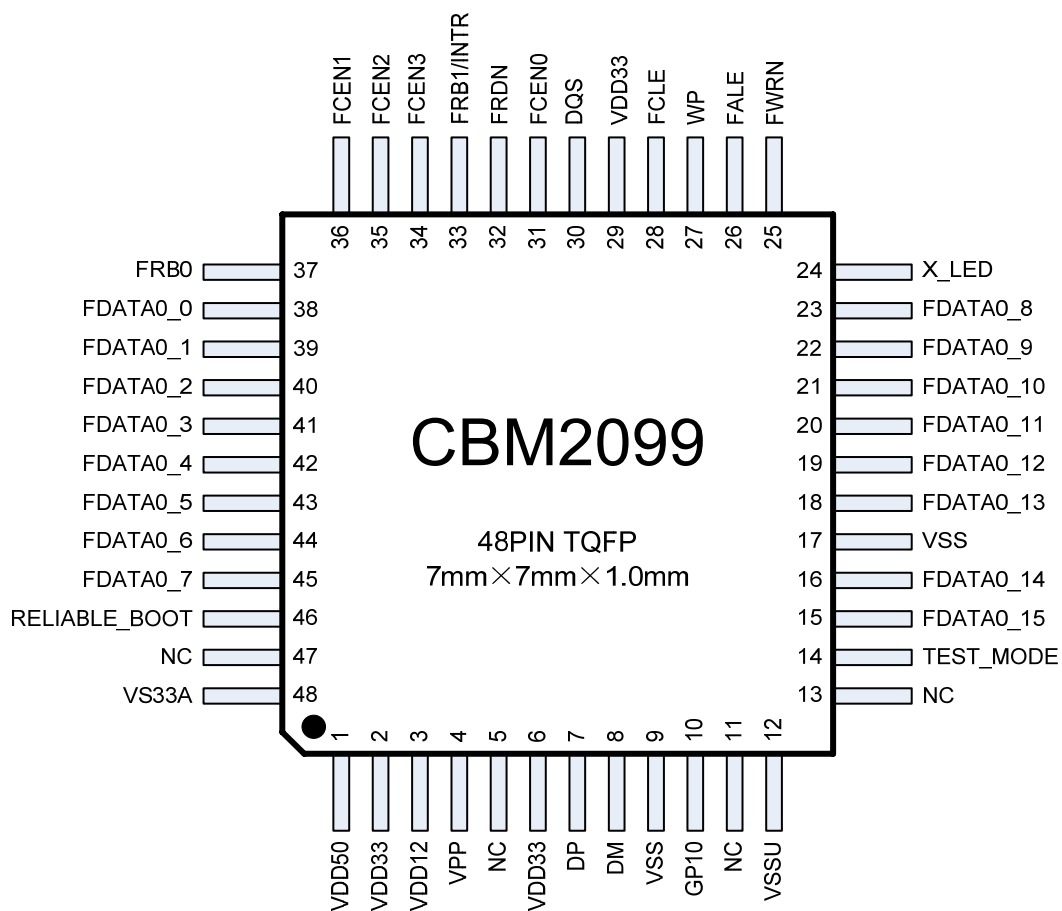
5 Pin Description

Brief CBM2099 pin functions are shown in the following tables.

I: Input signal

O: Output signal

I/O: Bi-direction signal

PWR: Power signal

GND: Ground signal

PU: pull up

PD: pull down

CBM2099 TQFP48 Pin Description

TQFP48 Pin No.	Pin Name	Type	Description
1	VDD50	PWR	Regulator 5V Power Input
2	VDD33	PWR	Regulator 3.3V Power OUT
3	VDD12	PWR	Regulator 1.2V Out
4	VPP	PWR	CORE 1.2V in
5	NC	I/O	Left open
6	VDD33	PWR	Padring 3.3V Power
7	DP	I/O	USB Data D+
8	DM	I/O	USB Data D-
9	VSS	GND	Padring 3.3V / Logic 1.2V Ground
10	GP10	I/O	Debug Mode PIN (Active low)
11	NC	I/O	Left open
12	VSSU	GND	Analog 1.2V Ground
13	NC	I/O	Left open
14	TEST_MODE	I PD	Test Mode Enable Pin When high , test mode When low , normal mode

15	FDATA0_15 GPIO15	I/O PU	Group 0 Flash Data Bus - bit 15 General I/O port 15 When select spi mode ,as spi chip select . (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select master mode , configure output , otherwise, configure as input.).
16	FDATA0_14 GPIO14	I/O PU	Group 0 Flash Data Bus - bit 14 General I/O port 14 When select spi mode, as clock out support ligh-tun sensor (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select ligh-tun mode , configure output).
17	VSS	GND	Padring 3.3V / Logic 1.2V Ground
18	FDATA0_13 GPIO13	I/O PU	Group 0 Flash Data Bus - bit 13 General I/O port 13
19	FDATA0_12 GPIO12	I/O PU	Group 0 Flash Data Bus - bit 12 General I/O port 12
20	FDATA0_11 GPIO11	I/O PU	Group 0 Flash Data Bus - bit 11 General I/O port 11
21	FDATA0_10 GPIO10	I/O PU	Group 0 Flash Data Bus - bit 10 General I/O port 10
22	FDATA0_9 GPIO9	I/O PU	Group 0 Flash Data Bus - bit 9 General I/O port 9
23	FDATA0_8 GPIO8	I/O PU	Group 0 Flash Data Bus - bit 8 General I/O port 8
24	X_LED	I/O	When TEST_MODE =1, as scan clock input. When TEST_MODE =0, as LED Indication
25	FWRN	O	Group Flash Write Enable (active low)
26	FALE	O	Group Flash Address Latch Enable
27	WP	I	Write Protect Switch Input
28	FCLE	O	Group Flash Command Latch Enable
29	VDD33	PWR	Padring 3.3V Power
30	DQS	I/O PD	DQS, only for onfi/toggle nand flash
31	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
32	FRDN	O	Group Flash Read Enable (active low)
33	FRB1 /INTR	I	Group Flash Ready_Busy 1, when select flash_rb1 mode, as Group Flash Ready_Busy1 signal input(detail in soft_flag [25]). 2, when select intr mode, as external interrupt input signal(detail in soft_flag [25]).
34	/SCK(I2c) FCEN3	O	1, When select test-mode, as scan-chain output 2, When select i2c , as sck 3, When select chip select2/3 mode, as CE3 output
35	FCEN2	I/O PU	1, When select test_mode, As scan-chain input 2, when select chip select2/3 mode, as CE2 output .(active

			when disable test_mode)
36	X_CLK_OUT /FCEN1	I/O PU	1, When select clock input mode (1), X_CLK_OFF=1, as external input test clock. 2, When select chip select1 mode or spi master mode, as output. (only active when X_CLK_OFF =0 or de-slect spi slve mode) (1), select chip select1 mode (detail in soft_flag [28]/[25]), as CE1 output (2), otherwise, as normal clock_out ,which defined at config_r[20].
37	FRB0	I	Group Flash Ready_Busy0
38	FDATA0_0 GPIO0	I/O PU	Group 0 Flash Data Bus - bit 0 General I/O port 0
39	FDATA0_1 GPIO1	I/O PU	Group 0 Flash Data Bus - bit 1 General I/O port 1
40	FDATA0_2 GPIO2	I/O PU	Group 0 Flash Data Bus - bit 2 General I/O port 2
41	FDATA0_3 GPIO3	I/O PU	Group 0 Flash Data Bus - bit 3 General I/O port 3
42	FDATA0_4 GPIO4	I/O PU	Group 0 Flash Data Bus - bit 4 General I/O port 4
43	FDATA0_5 GPIO5	I/O PU	Group 0 Flash Data Bus - bit 5 General I/O port 5
44	FDATA0_6 GPIO6	I/O PU	Group 0 Flash Data Bus - bit 6 General I/O port 6
45	FDATA0_7 GPIO7	I/O PU	Group 0 Flash Data Bus - bit 7 General I/O port 7
46	RELIABLE_BO OT	I PU	Reliable boot selection (active low)
47	NC	I/O	Left open
48	VSS33A	GND	Analog 3.3V Ground

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions		min	max	unit
VDD33	analog supply voltage			-0.5	5.5	v
VDD12	digital supply voltage			-0.5	4.5	v
VDD50	input voltage			-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A	DP, DM and GND pins	-4000	+4000	v
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	℃

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VDD33	analog supply voltage		3.0	3.3	3.6	V
VDD12	digital supply voltage		1.08	1.2	1.32	V
VDD50	input voltage		4.5	5	5.5	V
VI(AI/O)	input voltage on analog I/O pins DP DM	Low/Full speed	0	3.3	3.6	V
		High speed	0	400	-	mV
Tamb	ambient temperature		0	-	+70	℃

6.3 Static characteristics

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V;
Tamb = -10 to 75 °C;

| symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	operating supply current	Full-speed transmitting and receiving;	-	22.8	-	mA
		high-speed transmitting and receiving	-	40		
ICC(susp)	suspend supply current	in suspend mode	-	0.8		mA

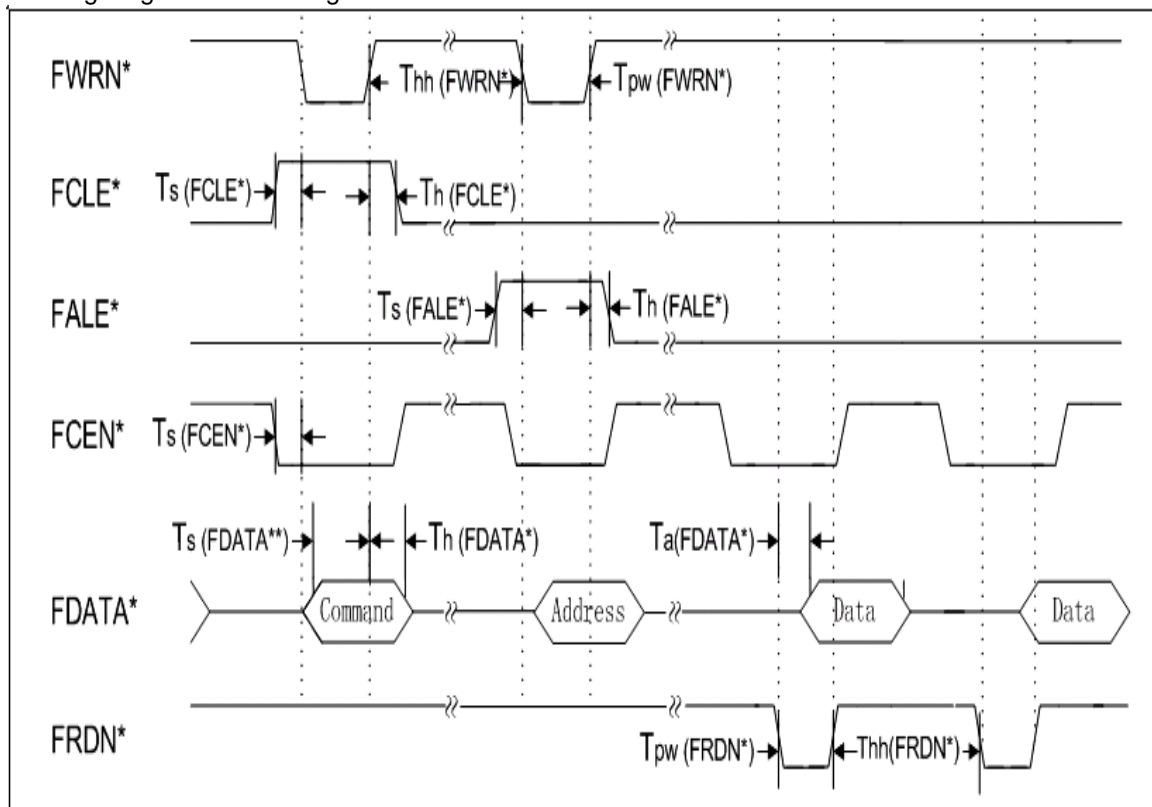## 6.4 Dynamic characteristics

6.4.1 Normal NAND FLASH Dynamic characteristics

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V;
Tamb = -10 to 75 °C ;

symbol	Parameter	conditions	min	Typ	max	Unit
Ts(FDATA*)	FDATA* setup time relative to rising FWRN* edge	Configured by firmware	8	33	75	ns
Th(FDATA*)	FDATA* hold time relative to falling FWRN* edge	Configured by firmware	8	33	75	ns
Ts (FCLE*)	FCLE* setup time relative to falling FWRN* edge	Configured by firmware	8	16	25	ns
Th (FCLE*)	FCLE* hold time relative to rising FWRN* edge	Configured by firmware	10	16	75	ns
Ts (FALE*)	FALE* setup time relative to falling FWRN* edge	Configured by firmware	8	16	25	ns
Th (FALE*)	FALE* hold time relative to rising FWRN* edge	Configured by firmware	10	16	75	ns
Ts (FCEN*)	FCEN* setup time relative to falling FWRN* edge	Configured by firmware	-	99		ns
Tpw (FWRN*)	FWRN* Pulse Width	Configured by firmware	8	33	75	ns
Thh (FWRN*)	FWRN* high hold time	Configured by firmware	8	33	75	ns
Ta(FDATA*)	FDATA* access time relative to falling FRDN* edge		-5	0	5	ns
Tpw (FRDN*)	FWRN* Pulse Width	Configured by firmware	8	33	75	ns
Thh (FRDN*)	FWRN* high hold time	Configured by firmware	8	33	75	ns

Timing diagram for Writing of Data
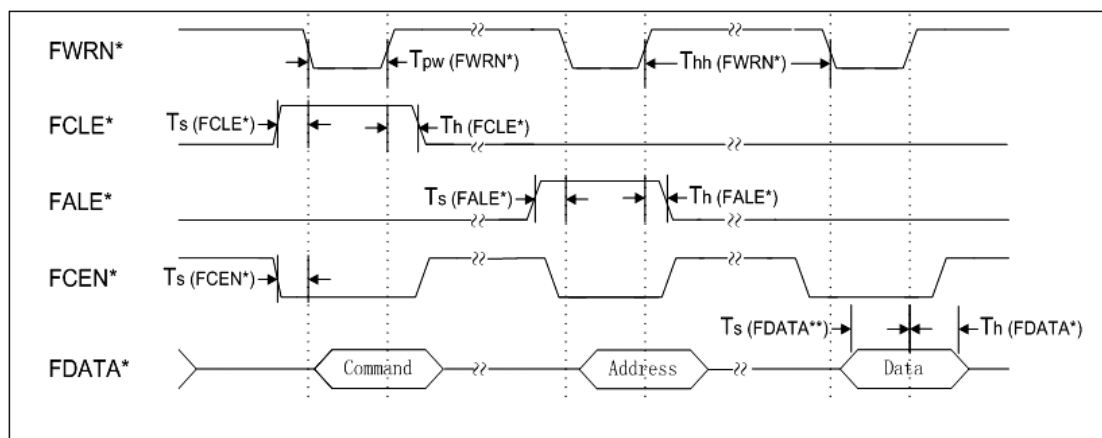

Timing diagram for Reading of Data

6.4.2 ONFI NAND FLASH Dynamic characteristics

CBM2099 only support Mode0/Mode1/Mode2.

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		50		30		20		15		12		ns	–
Frequency		≈20		≈33		≈50		≈67		≈83		MHz	–
Access window of DQ[7:0] from CLK	^tAC	–	20	–	20	–	20	–	20	–	20	ns	–
ALE to data loading time	^tADL	100	–	100	–	70	–	70	–	70	–	ns	–
Cmd, Addr, Data delay	^tCAD	25	–	25	–	25	–	25	–	25	–	ns	1
ALE, CLE, W/R# hold	^tCALH	10	–	5	–	4	–	3	–	2.5	–	ns	–
ALE, CLE, W/R# setup	^tCALS	10	–	5	–	4	–	3	–	2.5	–	ns	–
DQ hold - Cmd, Addr	^tCAH	10	–	5	–	4	–	3	–	2.5	–	ns	–
DQ setup - Cmd, Addr	^tCAS	10	–	5	–	4	–	3	–	2.5	–	ns	–
Change column setup to data in/out or next command	^tCCS	200	–	200	–	200	–	200	–	200	–	ns	2
CE# hold	^tCH	10	–	5	–	4	–	3	–	2.5	2	ns	–
Average CLK cycle time	^tCK (avg)	50	100	30	50	20	30	15	20	12	15	ns	3
Absolute CLK cycle time, from rising edge to rising edge	^tCK (abs)	$^tCK(abs)\ MIN = {}^tCK(avg) + {}^tJIT(per)\ MIN$ $^tCK(abs)\ MAX = {}^tCK(avg) + {}^tJIT(per)\ MAX$										ns	–
CLK cycle HIGH	^tCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^tCK	4
CLK cycle LOW	^tCKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^tCK	4
Data output end to W/R# HIGH	^tCKWR	$^tCKWR(MIN) = RoundUp[^tDQSCK(MAX) + {}^tCK) / {}^tCK]$										^tCK	–
CE# setup	^tCS	35	–	25	–	15	–	15	–	15	–	ns	–
Data In hold	^tDH	5	–	2.5	–	1.7	–	1.3	–	1.1	–	ns	–
Access window of DQS from CLK	^tDQSCK	–	20	–	20	–	20	–	20	–	20	ns	–
DQS, DQ[7:0] Driven by NAND	^tDQSD	0	20	0	20	0	20	0	20	0	20	ns	–
DQS, DQ[7:0] to tri-state	^tDQSHZ	–	20	–	20	–	20	–	20	–	20	ns	5
DQS input high pulse width	^tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	–
DQS input low pulse width	^tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	–
DQS-DQ skew	^tDQSQ	–	5	–	2.5	–	1.7	–	1.3	–	1.1	ns	–
Data input	^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	–
Data In setup	^tDS	5	–	3	–	2	–	1.5	–	1.1	–	ns	–

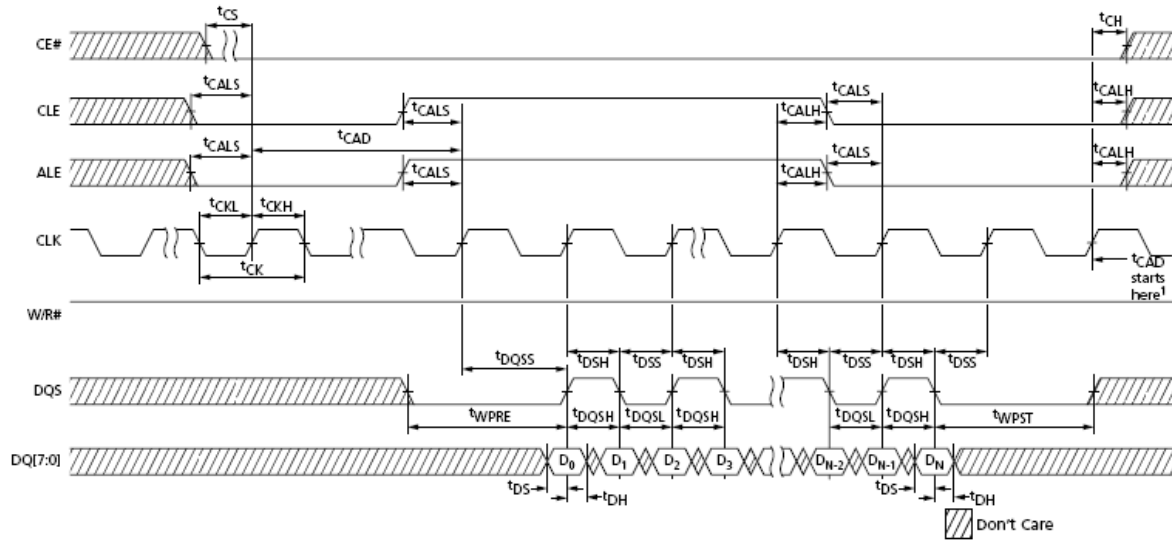| Parameter	Symbol	Mode 0 Min	Mode 0 Max	Mode 1 Min	Mode 1 Max	Mode 2 Min	Mode 2 Max	Mode 3 Min	Mode 3 Max	Mode 4 Min	Mode 4 Max	Unit	Notes
DQS falling edge from CLK rising - hold	^{t}DSH	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	^{t}CK	–
DQS falling to CLK rising - setup	^{t}DSS	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	^{t}CK	–
Data Valid Window	^{t}DVW	^{t}DVW = ^{t}OH - ^{t}DQSQ										ns	–
Half Clock Period	^{t}HP	^{t}HP = Min(^{t}CKH, ^{t}CKL)										ns	–
The deviation of a given ^{t}CK(abs) from ^{t}CK (avg)	^{t}JIT(per)	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	ns	–
DQ-DQS hold, DQS to first DQ to go non-valid, per access	^{t}QH	^{t}QH = ^{t}HP - ^{t}QHS										ns	–
Data Hold Skew Factor	^{t}QHS	–	6	–	3	–	2	–	1.5	–	1.2	ns	–
Data output to command, address, or data input	^{t}RHW	100	–	100	–	100	–	100	–	100	–	ns	–
Ready to data output	^{t}RR	20	–	20	–	20	–	20	–	20	–	ns	–
Device reset time (Read/Program/Erase)	^{t}RST	–	5/10/500	–	5/10/500	–	5/10/500	–	5/10/500	–	5/10/500	µs	6
CLK high to R/B# low	^{t}WB	–	100	–	100	–	100	–	100	–	100	ns	–
Command cycle to data output	^{t}WHR	80	–	60	–	60	–	60	–	60	–	ns	–
DQS write preamble	^{t}WPRE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	^{t}CK	–
DQS write postamble	^{t}WPST	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	^{t}CK	–
W/R# LOW to data output cycle	^{t}WRCK	20	–	20	–	20	–	20	–	20	–	ns	–
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	100	–	100	–	ns	–

Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. This value is specified in the parameter page.
3. ^{t}CK(avg) is the average clock period over any consecutive 200-cycle window.
4. ^{t}CKH(abs) and ^{t}CKL(abs) include static offset and duty cycle jitter.
5. ^{t}DQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
6. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5µs.
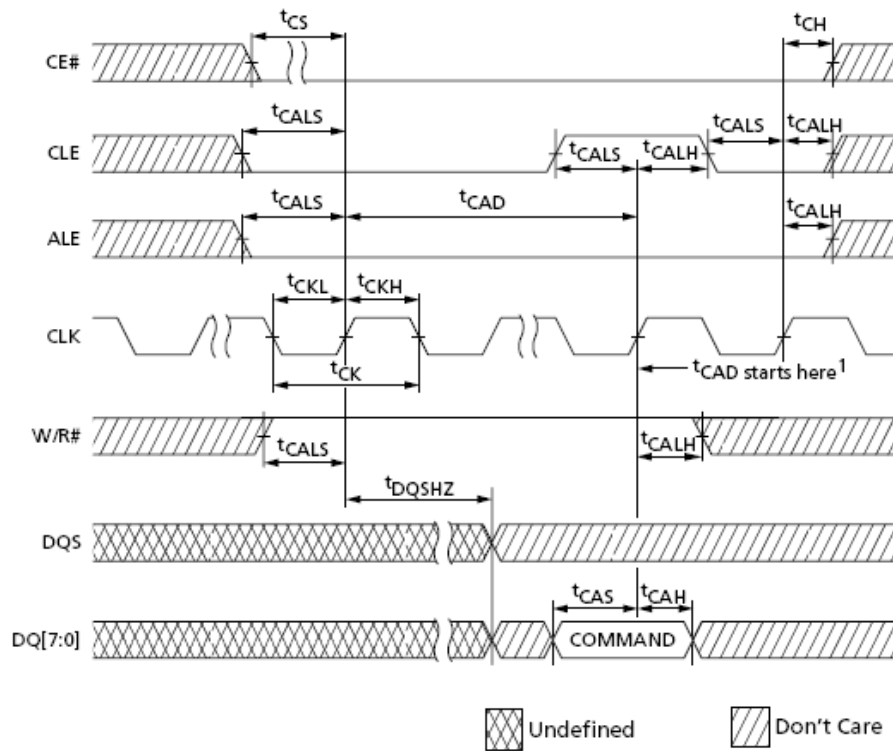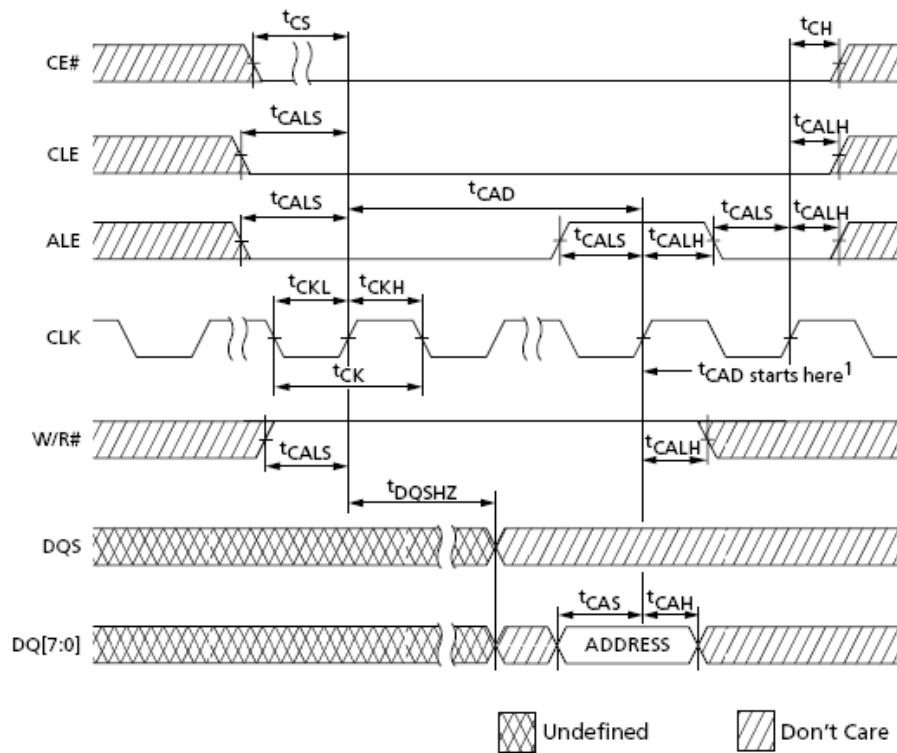
Notes: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Notes: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

CE# t_{CS} t_{CH}

CLE t_{CALS} t_{CALS} t_{CALS} t_{CALH} t_{CALH}

ALE t_{CALS} t_{CAD} t_{CALS} t_{CALH} t_{CALS} t_{CALH}

CLK t_{CKL} t_{CKH} t_{CK} t_{CAD} starts here[1]

W/R#

DQS t_{DQSS} t_{DSH} t_{DSS} t_{DSH} t_{DSH} t_{DSS} t_{DSH} t_{DSS} t_{WPRE} t_{DQSH} t_{DQSL} t_{DQSH} t_{DQSL} t_{DQSH} t_{WPST}

DQ[7:0] D_0 D_1 D_2 D_3 D_{N-2} D_{N-1} D_N t_{DS} t_{DH} t_{DS} t_{DH}

Don't Care

Notes: 1. When CE# remains LOW, t_{CAD} begins at the first rising edge of the clock after t_{WPST} completes.
2. t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
3. t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).

Notes:
1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock after ^{t}CKWR for subsequent command or data output cycle(s).
2. See Figure 25 on page 33 for details of W/R# behavior.
3. ^{t}AC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH: DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW: DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

6.4.3 TOGGLE NAND FLASH Dynamic characteristics
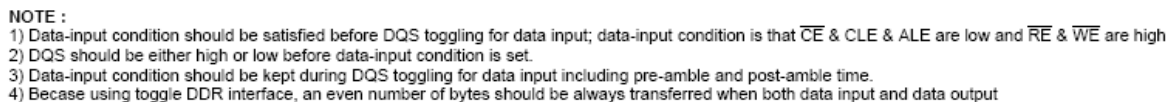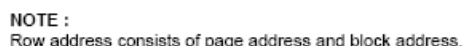
CBM2099 only support 66Mbps/80Mbps.

Parameter	Sym-bol	66Mbps Min	66Mbps Max	80Mbps Min	80Mbps Max	133Mbps Min	133Mbps Max	Unit
CLE/ALE Setup Time	tCALS	15	-	15	-	15	-	ns
CLE/ALE Hold Time	tCALH	5	-	5	-	5	-	ns
DQS Setup Time for data input start	tCDQSS	100	-	100	-	100	-	ns
DQS Hold Time for data input finish	tCDQSH	100	-	100	-	100	-	ns
Command Write cycle to Address Write cycle Time for Random data input	tCWAW	300	-	300	-	300	-	ns
$\overline{CE}$ Setup Time	tCS	20	-	20	-	20	-	ns
$\overline{CE}$ Hold Time	tCH	5	-	5	-	5	-	ns
Command/Address Setup Time	tCAS	5	-	5	-	5	-	ns
Command/Address Hold Time	tCAH	5	-	5	-	5	-	ns
Data Setup Time	tDS	4	-	3.3	-	2.0	-	ns
Data Hold Time	tDH	3.6	-	3	-	1.8	-	ns
Write Cycle Time	tWC	25	-	25	-	25	-	ns
$\overline{WE}$ High pulse width	tWH	11	-	11	-	11	-	ns
$\overline{WE}$ Low pulse Width	tWP	11	-	11	-	11	-	ns
Address to Data Loading Time	tADL	300	-	300	-	300	-	ns
Data Transfer from Cell to Register	tR	-	100	-	100	-	100	μs
Ready to $\overline{RE}$ High	tRR	20	-	20	-	20	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	tCR	10	-	10	-	10	-	ns
ALE Low to $\overline{RE}$ Low	tAR	10	-	10	-	10	-	ns
CLE to $\overline{RE}$ Low	tCLR	10	-	10	-	10	-	ns
$\overline{WE}$ High to Busy	tWB	-	100	-	100	-	100	ns
Read Cycle Time	tRC	30	-	25	-	15	-	ns
$\overline{RE}$ High pulse width	tREH	13	-	11	-	6.5	-	ns
$\overline{RE}$ Low pulse width	tRP	13	-	11	-	6.5		ns
$\overline{CE}$ High to Output Hi-Z	tCHZ	-	30	-	30	-	30	ns
CLE High to Output Hi-Z	tCLHZ	-	30	-	30	-	30	ns
Data Strobe Cycle Time	tDSC	30	-	25	-	15	-	ns
DQS Input Low Pulse Width	tDQSL	13	-	11	-	6.5	-	ns
DQS Input High Pulse Width	tDQSH	13	-	11	-	6.5	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	tWHR	120	-	120	-	120	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low for Random data out	tWHR2	300	-	300	-	300	-	ns

RE to DQS and DQ delay	t_{DQSRE}	-	25	-	25	-	25	ns
Read Preamble	t_{RPRE}	15	-	15	-	15	-	ns
Read Postamble	t_{RPST}	tDQSRE+0.5xtRC	-	tDQSRE+0.5xtRC	-	tDQSRE+0.5xtRC	-	ns
Read Postamble Hold Time	t_{RPSTH}	5		5		5	-	ns
Write Preamble	t_{WPRE}	15		15		15	-	ns
Write Postamble	t_{WPST}	6.5		6.5		6.5	-	ns
Write Postamble Hold Time	t_{WPSTH}	5		5		5	-	ns
Output skew among data output and corresponding DQS	t_{DQSQ}	-	2.5	-	2	-	1.4	ns
DQS hold skew factor	t_{QHS}	-	2.5	-	2	-	1.4	ns
Output hold time from DQS	t_{QH}	$t_{QH} = t_{REH}/t_{RP} - t_{QHS}$						ns
Output data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$						ns
Device Resetting Time (Read/Program/Erase)	t_{RST}[1]	10/30/100						μs
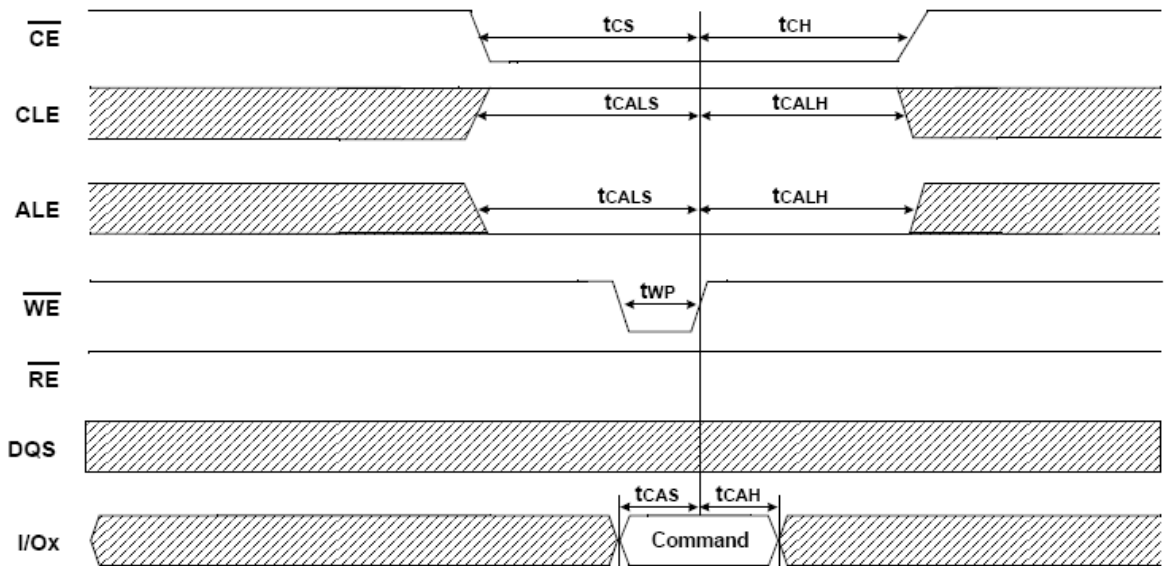
NOTE :
1. Command information is lached by WE going high, when CE is Low, CLE is High, and ALE is Low.
2. DQS should be set to 'Low' when these commands(85h, 10h, 11h) is input.

NOTE :
Row address consists of page address and block address.

NOTE :
1) Data-input condition should be satisfied before DQS toggling for data input; data-input condition is that $\overline{CE}$ & CLE & ALE are low and $\overline{RE}$ & $\overline{WE}$ are high
2) DQS should be either high or low before data-input condition is set.
3) Data-input condition should be kept during DQS toggling for data input including pre-amble and post-amble time.
4) Becase using toggle DDR interface, an even number of bytes should be always transferred when both data input and data output

```
          : undefined
          : don't care
```
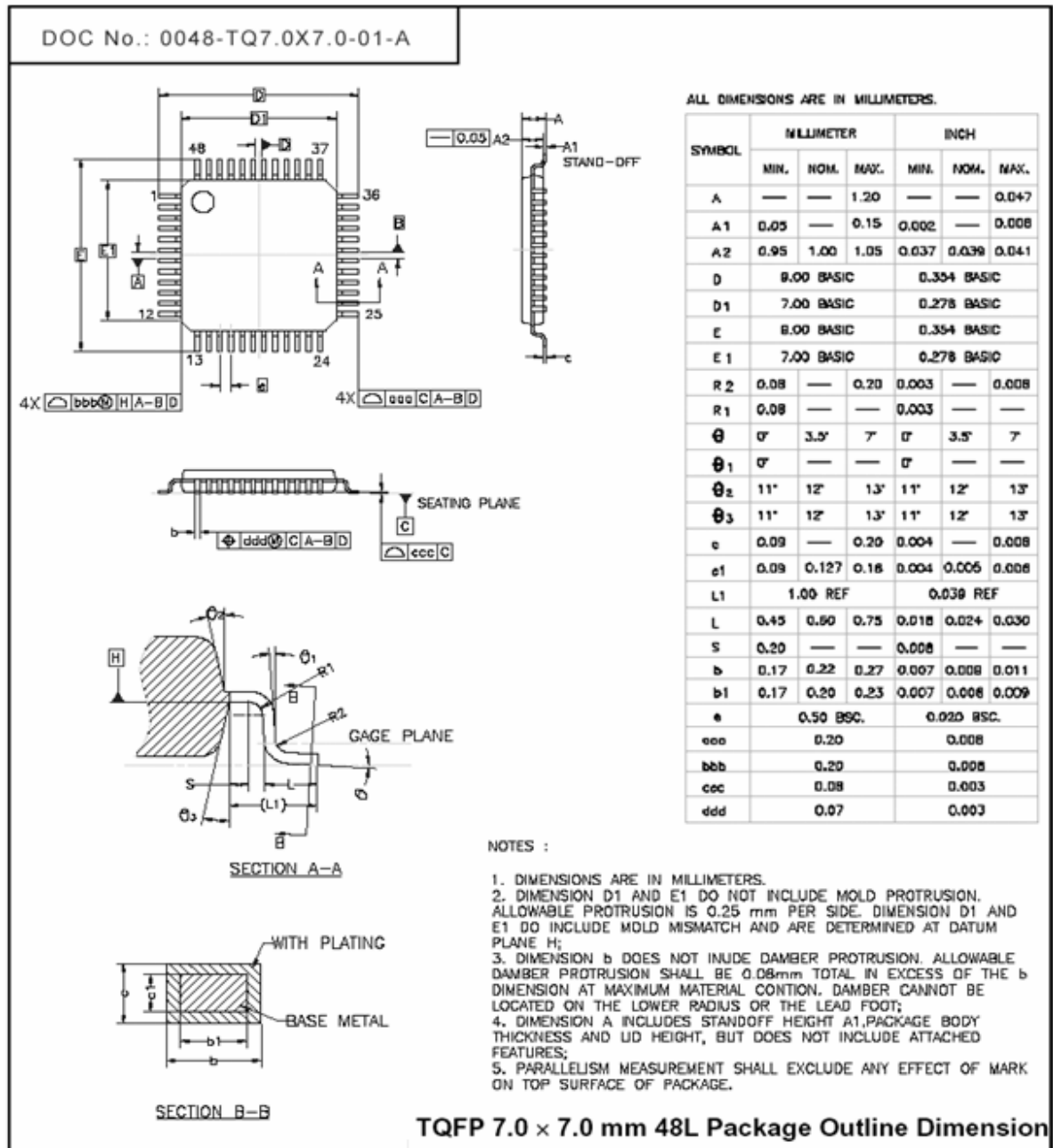
NOTE :
1) Data-output condition should be satisfied before $\overline{RE}$ toggling for data output; data-output condition is that $\overline{CE}$ & CLE & ALE are low and $\overline{WE}$ is high
2) $\overline{RE}$ should be either high or low before data-output condition is set.
3) Data-output condition should be kept during $\overline{RE}$ toggling for data output including pre-amble and post-amble time.
4) DQS and Data out buffers are turned on when $\overline{RE}$ is low for pre-amble operation under data-out condition
5) DQS and Data out buffers turn from valid value to high-z if either $\overline{CE}$ or CLE goes High.
6) an even number of bytes should be always transferred when both data input and data output

7 Mechanical Dimensions

7.1 48-Pin CBM2099 Package Outline Dimension

DOC No.: 0048-TQ7.0X7.0-01-A

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

STAND-OFF

SEATING PLANE

SECTION A-A

GAGE PLANE

WITH PLATING

BASE METAL

SECTION B-B

NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSION D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H;
3. DIMENSION b DOES NOT INUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONTION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT;
4. DIMENSION A INCLUDES STANDOFF HEIGHT A1, PACKAGE BODY THICKNESS AND UD HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES;
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TQFP 7.0 × 7.0 mm 48L Package Outline Dimension

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