Datorteknik
Lab 1: Digital Logic Circuits

Todor Stoyanov

September 20, 2018

1 Objectives and Lab Materials

In this lab you will learn how to build digital logic circuits on a bredboard and how to interface to a microcontroller.

The matrerials for this lab are:

- A solderless bredboard.
- An Adafruit Trinket microcontroller board.
- Wiring kit.
- Micro USB cable.
- LED set.
- 3x 7400-series (SN74ACT00) quad NAND gate arrays.
- 2x 7402-series (SN74HCT02) quad NOR gate arrays.

The following tasks will guide you through setting up a 2-bit adder circuit. Please follow the tasks in order and demonstrate your circuits to the lab assistant. In your report, describe the steps you have taken to solve each task, as well as the results you obtained and the methods you used to verify that the system functions properly. Explain what experiments you performed, how and why. Provide your Arduino sketch as an attachment and demonstrate the final system to the lab assistant. If you think it is necessary, you may take pictures of the system in action, and/or include screenshots.

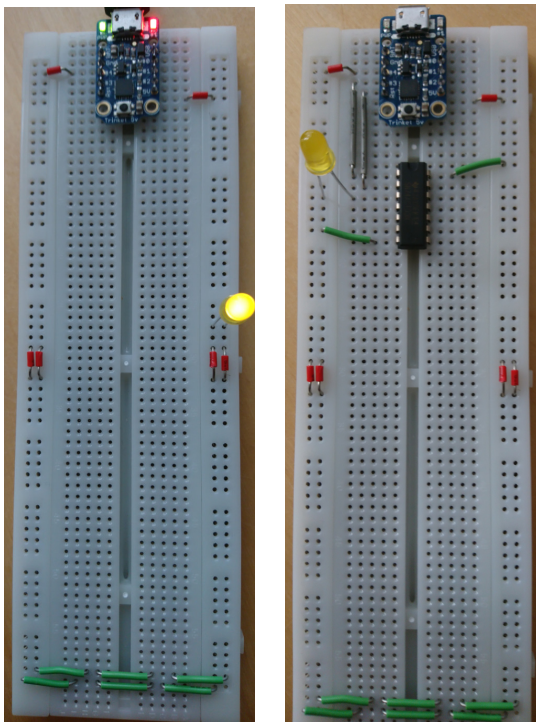
1.1 Preliminaries

Before starting with this lab please verify you have performed these preliminary steps:

- On your desktop PC open the Arduino IDE.
- Install the Adafruit Trinket board by following the steps in this tutorial: `https://learn.adafruit.com/adafruit-arduino-ide-setup/arduino-1-dot-6-x-ide`. Note that the IDE and USB drivers are already installed.
- Verify that you can upload code to the microcontroller by following this tutorial: `https://learn.adafruit.com/introducing-trinket/setting-up-with-arduino-ide`.
- Familiarize yourself with the Adafruit Trinket pinout (`https://learn.adafruit.com/introducing-trinket/pinouts`) and the manuals of the NAND and NOR gate ICs (see Appendix).

2 Task 1: Breadboard Setup and a NAND gate (5 points)

- As a first step, you need to set up your bredboard and let the arduino power other logic circuits. Follow the setup on Figure 1(a).
- The vertical lines of the board should provide logic HIGH nd LOW values, taken from the corresponding trinket PINs.
- As the bredboard vertical lines are not fully connected, you need to use the wiring set to transfer power accross.
- Use an LED to test that power is flowing correctly through the circuit. NOTE: the longer leg of the LED should be connected to HIGH, while the shorter leg should be connected to LOW.
- Once you are satisfied that the circuit works, place a 7400 series chip accross the bredboard. every leg of the circuit should be connected to only one horizontal line.
- Provide digital HIGH and LOW (ground) values to the correct terminals of the 7400. Please note that the 7400 has an indentation on one side of the chip, which should be pointing up, as in the manual.
- Connect PINS 3 and 4 of the microcnotroller to the inputs 1A and 1B of the gate.
- Connect the output 1Y of the 7400 chip through an LED to the ground. Again, please note the polarity of the LED.
- You should now have a setup similar to the one in Fig. 1(b).



(a) (b)

Figure 1: (a) Basic setup of a bredboard for the lab. (b) Setup of a NAND IC with input from the adafruit Trinket and output through an LED.

- Devise an arduino sketch to test your setup and verify that the NAND gate works as expected. Note that you need to setup PINS 3 and 4 for output, before writing HIGH or LOW values.

3 Task 2: Half-adder (10 points)

In this task, you should construct a half-adder circuit which accepts two input bits A0 and B0, and outputs the sum as a bit C0 and a CARRY bit. Review the circuit of a half-adder in Fig. 2.

- Adapt the circuit to use a maximum of 4 NAND and one NOR gates.
- Add a 7402 chip to your setup.
- Implement and test your setup. Provide inputs from the arduino and use LEDs to test that the output is as expected.

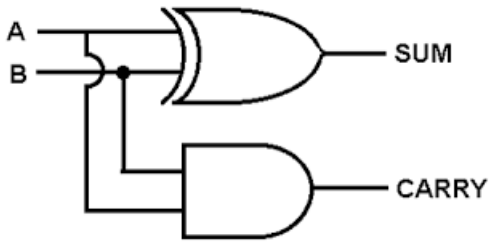


Figure 2: A half-adder circuit implemented with one XOR and one AND gate.

4 Task 3: Full-adder and 2-bit adder circuit (10 points)

In this task you will implement a full-adder circuit and chain it together with your half-adder to produce a two-bit adder. Recall that a one-bit full adder can be implemented as two half-adders and an OR gate, as in Fig. 3.

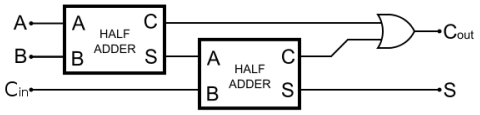


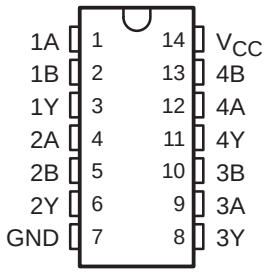
Figure 3: A full-adder circuit implemented with two half-adders and one OR gate.

- Replicate your half-adder design two times. You will end up with three half-adder circuits on your board (one from Task 2, and two new ones).
- What spare gates do you have left on your 5 ICs? Implement the OR gate using the leftover gates.
- Add another input from your arduino (for the carry-in bit of the full adder).
- Modify your arduino sketch and test that the one-bit full adder circuit works as expected. Use two LEDs to verify your circuit.
- Once you are certain the circuit works, chain the carry out output from the half-adder to the carry in input of the full adder.
- Use four PINs of the arduino to input two two-bit numbers into your circuit (A0, A1, B0 and B1).
- Use three LEDs (for C0, C1, and carry out) to verify that your circuit adds number correctly.

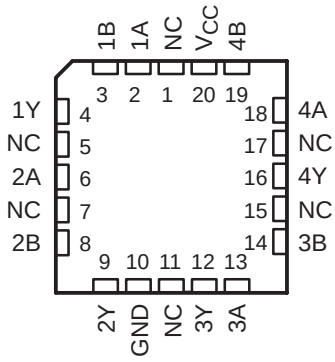
Appendix: Manuals of the Logic Gate Arrays

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 8 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT00 . . . J OR W PACKAGE
SN74ACT00 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT00 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The ‘ACT00 devices contain four independent 2-input NAND gates. Each gate performs the Boolean function of $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube	SN74ACT00N	SN74ACT00N
	SOIC − D	Tube	SN74ACT00D	ACT00
		Tape and reel	SN74ACT00DR	
	SOP − NS	Tape and reel	SN74ACT00NSR	ACT00
	SSOP − DB	Tape and reel	SN74ACT00DBR	AD00
	TSSOP − PW	Tube	SN74ACT00PW	AD00
		Tape and reel	SN74ACT00PWR	
−55°C to 125°C	CDIP − J	Tube	SNJ54ACT00J	SNJ54ACT00J
	CFP − W	Tube	SNJ54ACT00W	SNJ54ACT00W
	LCCC − FK	Tube	SNJ54ACT00FK	SNJ54ACT00FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram, each gate (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

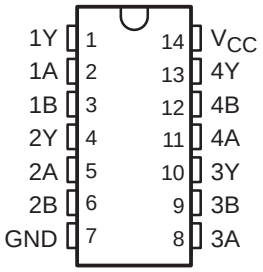
recommended operating conditions (see Note 3)

		SN54ACT00		SN74ACT00		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

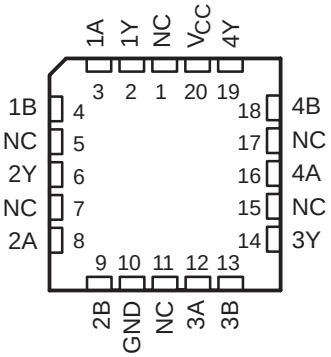
NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

- **Operating Voltage Range of 4.5 V to 5.5 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 10 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**

SN54HCT02 . . . J OR W PACKAGE
SN74HCT02 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HCT02N	SN74HCT02N
	SOIC – D	Tube of 50	SN74HCT02D	HCT02
		Reel of 2500	SN74HCT02DR	
		Reel of 250	SN74HCT02DT	
	SOP – NS	Reel of 2000	SN74HCT02NSR	HCT02
	SSOP – DB	Reel of 2000	SN74HCT02DBR	HT02
	TSSOP – PW	Tube of 90	SN74HCT02PW	HT02
		Reel of 2000	SN74HCT02PWR	
		Reel of 250	SN74HCT02PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT02J	SNJ54HCT02J
	CFP – W	Tube of 150	SNJ54HCT02W	SNJ54HCT02W
	LCCC – FK	Tube of 55	SNJ54HCT02FK	SNJ54HCT02FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram, each gate (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT02			SN74HCT02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.