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UNIVERSITY OF TECHNOLOGY  
FACULTY OF ELECTRICAL ELECTRONIC ENGINEERING



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## **ANALOG AND MIXED SIGNAL IC DESIGN (EE4453)**

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### **PROJECT**

### **VOLTAGE CONTROL OSCILLATOR (VCO)**

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# TABLE OF CONTENTS

<b>I. INTRODUCTION ABOUT VOLTAGE CONTROL OSCILLATOR.....</b>	<b>2</b>
<b>II. OPERATING PRINCIPLES OF VCO.....</b>	<b>3</b>
<b>III. STRUCTURE AND CIRCUITRY OF VCO.....</b>	<b>4</b>
<b>PART A: CURRENT STARVED VCO.....</b>	<b>4</b>
1. INTRODUCTION.....	4
1.1. Theory.....	4
1.2. Schematic.....	5
2. MEASUREMENT.....	7
2.1. Ring VCO.....	7
2.2. Current Starved VCO.....	8
2.2.1. The output response of VCO with target frequency using transient analysis.....	8
2.2.2. Jitter.....	11
2.2.3. Phase noise.....	11
2.2.4. Power.....	12
<b>PART B: LC VCO.....</b>	<b>13</b>
1. INTRODUCTION.....	13
1.1. Theory.....	13
1.2. Schematic.....	14
2. MEASUREMENT.....	15
2.1. The output response of VCO with target frequency using transient analysis.....	15
2.2. Jitter.....	19
2.3. Phase noise.....	19
2.4. Power.....	20
<b>IV. APPLICATION OF VCO.....</b>	<b>21</b>
<b>V. CONCLUSION.....</b>	<b>22</b>
<b>VI. REFERENCE DOCUMENT.....</b>	<b>23</b>

## I. INTRODUCTION ABOUT VOLTAGE CONTROL OSCILLATOR

A voltage-controlled oscillator (VCO) is an electronic device that generates oscillations, with its frequency controlled by an applied voltage. This feature allows it to be utilized in frequency modulation (FM) or phase modulation (PM) by applying a modulating signal to its control input. VCOs are essential components of phase-locked loops and are commonly used in synthesizers to produce waveforms with adjustable pitch based on voltage inputs, such as those from musical keyboards.



**Figure 1:** A microwave (12–18 GHz) voltage-controlled oscillator  
VCOs can be generally categorized into two groups based on the type of waveform produced

- **Linear or harmonic oscillators** generate a sinusoidal waveform. Harmonic oscillators in electronics usually consist of a resonator with an amplifier that replaces the resonator losses (to prevent the amplitude from decaying) and isolates the resonator from the output (so the load does not affect the resonator). Some examples of harmonic oscillators are LC oscillators and crystal oscillators.



**Figure 2:** A negative-resistance microwave oscillator



**Figure 3:** A miniature 16 MHz quartz crystal oscillator

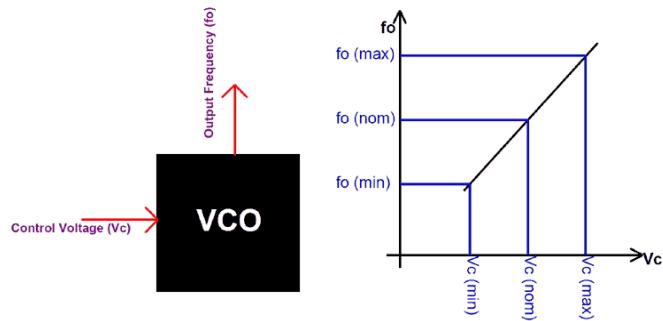
- **Relaxation oscillators** can generate a sawtooth or triangular waveform. They are commonly used in integrated circuits (ICs). They can provide a wide range of operational frequencies with a minimal number of external components.



**Figure 4:** A vacuum tube Abraham-Bloch multivibrator relaxation oscillator

## II. OPERATING PRINCIPLES OF VCO

There are many **types of VCO circuits**; a very basic one can be built by just utilizing a capacitor, inductor and resistor to make a tank circuit. Also Op-Amps, Multivibrator, transistors, 555 timers can also be utilized to build **oscillating circuits**. Apart from that there are dedicated IC packages like LM566 LM567 etc. which can act as VCO. To understand the basic idea of a VCO let us consider a RC oscillator.



**Figure 5:**  $V_c$  versus the output frequency

Let us assume the control voltage to be  $V_c$  and the output frequency as  $f_o$ . Then under normal operating conditions a nominal voltage is provided to the VCO for which a nominal Frequency is produced by the VCO. As the input voltage (control voltage) is increased the output frequency increases and the vice versa is also possible.

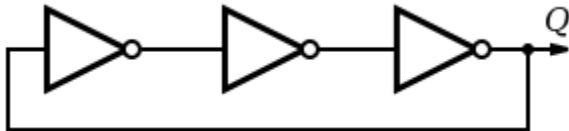
### III. STRUCTURE AND CIRCUITRY OF VCO

#### PART A: CURRENT STARVED VCO

##### 1. INTRODUCTION

###### 1.1. Theory

###### Ring oscillator



**Figure 6:** A schematic of a simple 3-inverter ring oscillator whose output frequency is  $1/(6 \times \text{inverter delay})$ .

A **ring oscillator** is a device composed of an odd number of NOT gates in a ring, whose output oscillates between two voltage levels, representing *true* and *false*. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first.

The ring oscillator is a type of time-delay oscillator, where an inverting amplifier with a delay element between input and output generates oscillations. Initially balanced, any noise causes a slight output rise. The negative gain amplifier amplifies and reverses this signal, creating a sequential loop producing a square-wave output. As the signal grows, it stabilizes when the amplifier reaches its output limits.

If  $t$  represents the time delay for a single inverter and  $n$  represents the number of inverters in the inverter chain, then the frequency of oscillation is given by:

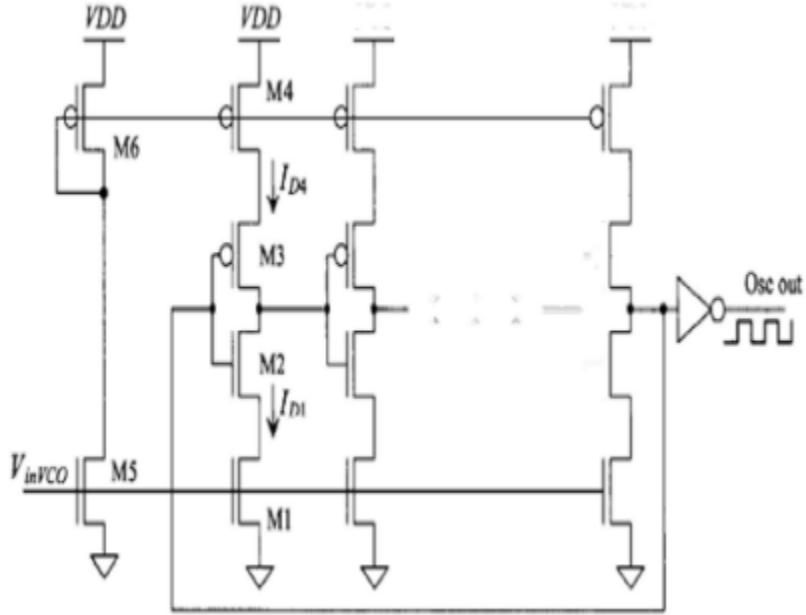
$$f = \frac{1}{2tn}$$

###### Jitter

The period of a ring oscillator varies in a random manner as  $T+T'$  where  $T'$  is a random value. In high-quality circuits, the range of  $T'$  is relatively small compared to the average period  $T$ . This variation in oscillator period is called *jitter*.

Temperature fluctuations affect the period of a ring oscillator, causing it to vary around the average period. Cold silicon speeds up propagation delay, increasing oscillator frequency and raising local temperature. Hot silicon slows propagation delay, decreasing frequency and lowering temperature. Stability occurs with constant ambient temperature and consistent heat transfer to the environment.

## Current Starved Voltage Controlled Oscillator



**Figure 7.** Conventional Current Starved VCO.

Ring oscillators can be used to design current-starved voltage-controlled oscillators (CSVCOs). In ring oscillators, controlling the gate capacitances of inverters affects charging and discharging, altering the oscillation frequency. Decreasing peak charging current increases charging and discharging time, reducing frequency. CSVCOs operate similarly to ring oscillators, with transistors M2 and M3 acting as an inverter, and M1 and M4 as current sources limiting current to M2 and M3, starving the inverter for current.

The input control voltage sets the drain current of transistors M5 and M6, which is mirrored across all inverter/current source stages. Therefore, any change in the control voltage leads to a corresponding change in the inverter current at each stage.

Total Capacitance of CSVCO can be determined by the following equation

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = C_{ox} + (A_p + A_n) + \frac{3}{2}C_{ox}(A_p + A_n)$$

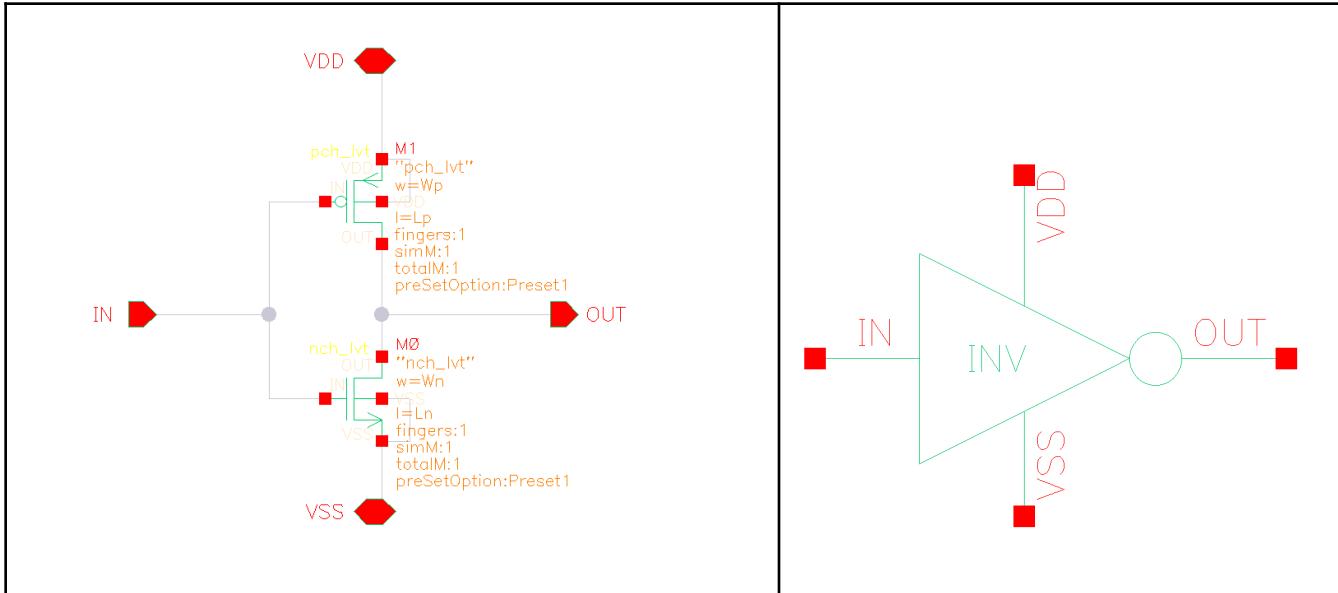
$$C_{tot} = \frac{5}{2}C_{ox}(A_p + A_n)$$

Where,

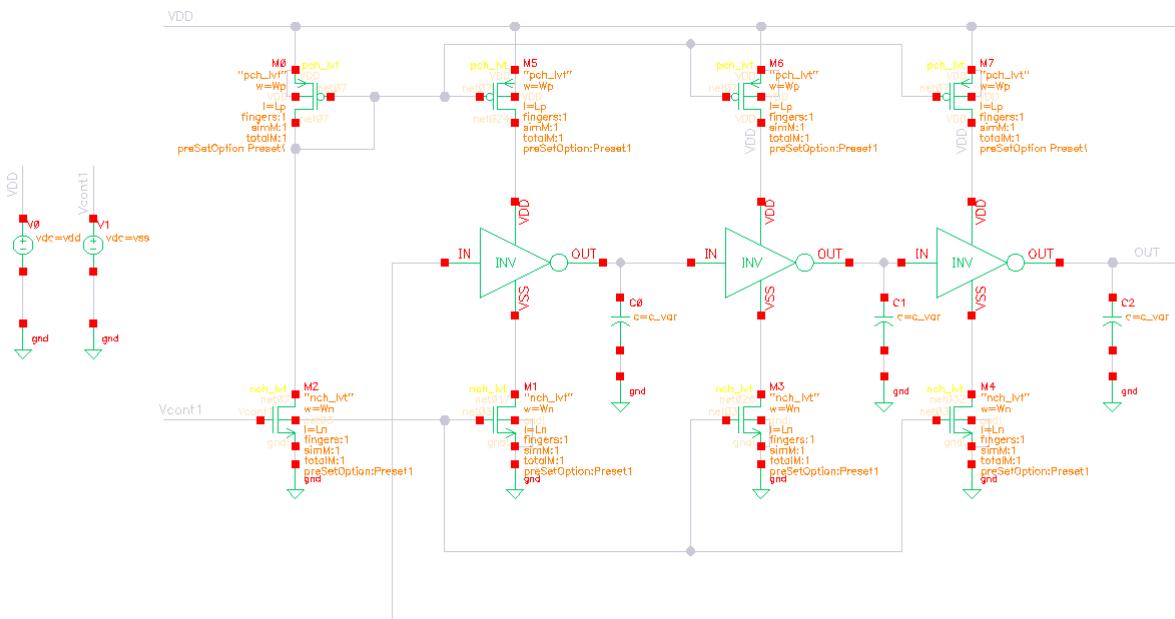
- $A_n = W_n L_n$ ,  $A_p = W_p L_p$ ;
- $C_{ox}$  is the oxide capacitance
- $L_p, L_n$  are channel lengths
- $W_p, W_n$  are channel widths
- $A_p, A_n$  are cross sectional areas of the PMOS and NMOS transistors respectively

## 1.2. Schematic

### Schematic and symbol of inverter



### Schematic of Current Starved VCO



## 2. MEASUREMENT

### 2.1. Ring VCO

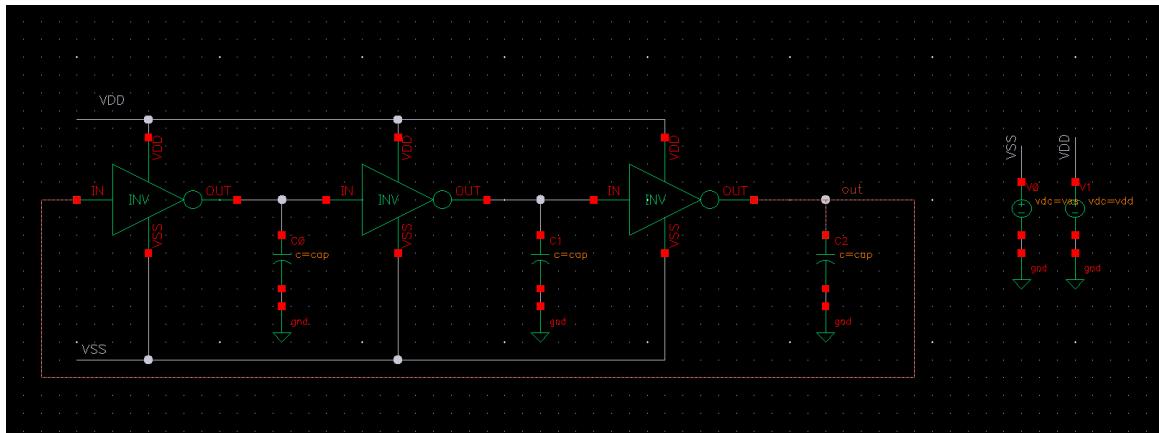


Figure 8 : Schematic of Ring VCO

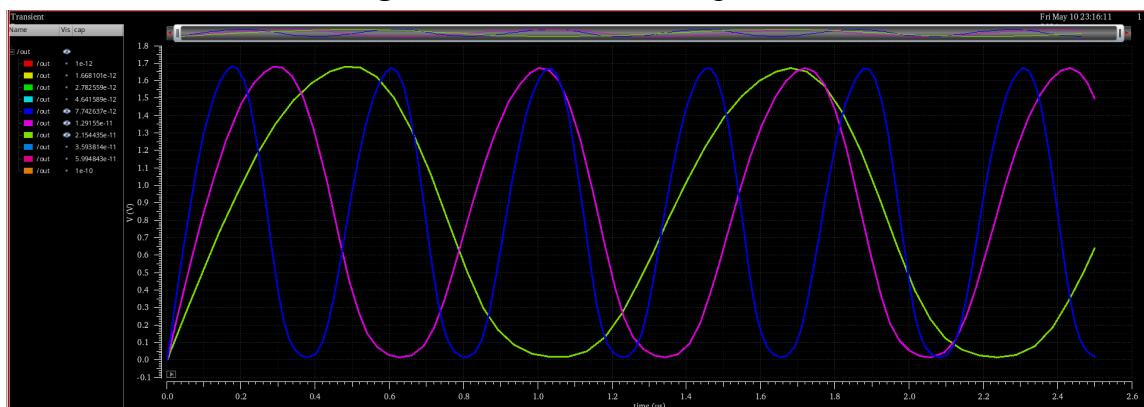


Figure 9: TRAN analysis of Vout with different capacitors

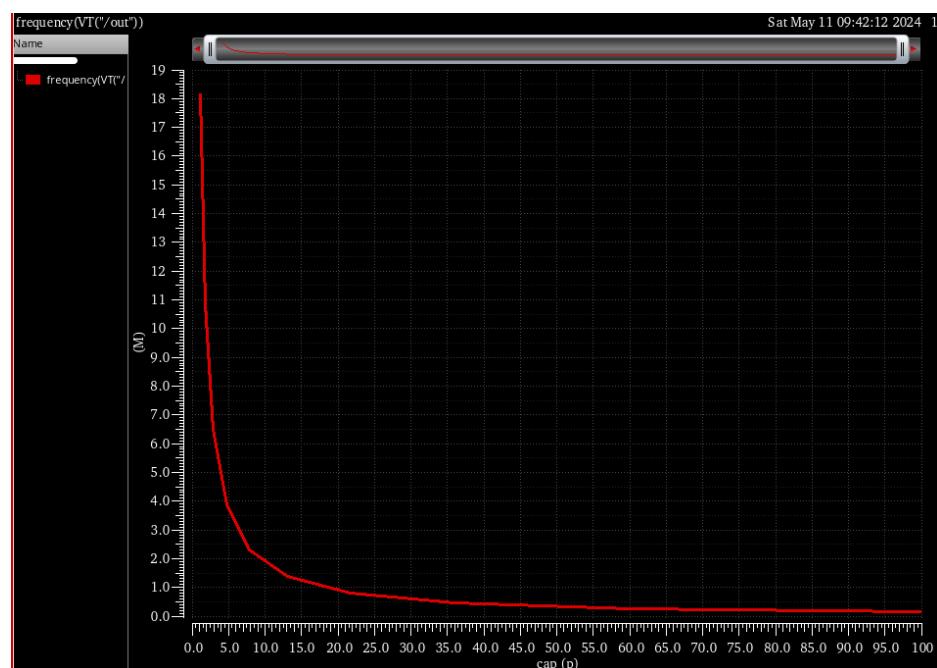
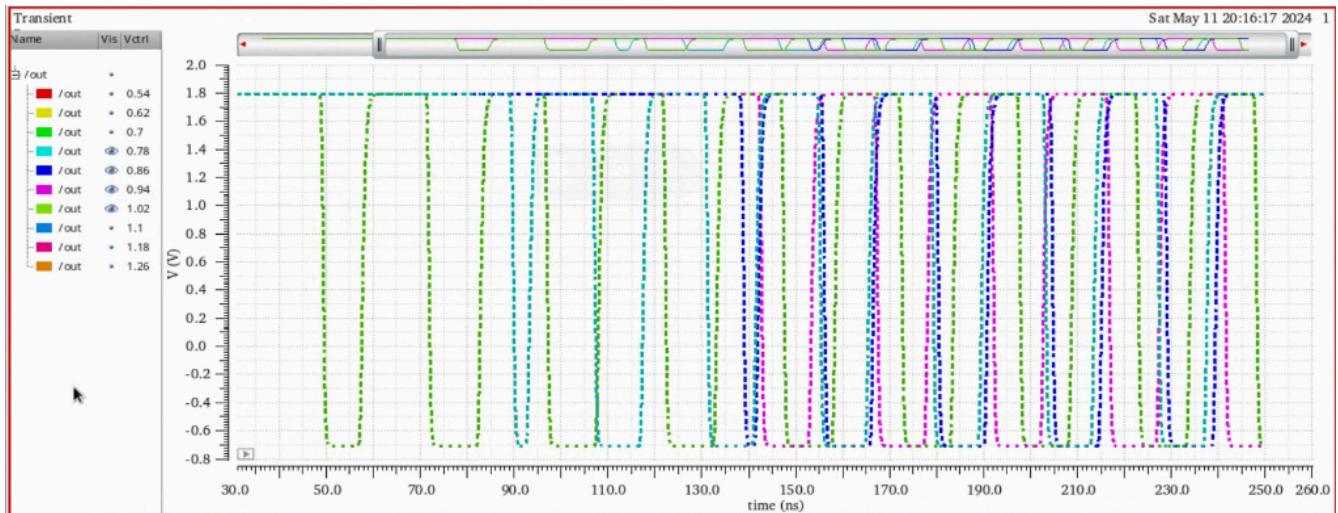


Figure 10: Frequency analysis based on capacitor changes

In a ring VCO circuit, changing the capacitor affects the charging and discharging time of the inverters in the chain. When the capacitor increases, the charging and discharging time also increases, leading to a decrease in the oscillation frequency of the VCO. Conversely, when the capacitor decreases, the charging and discharging time decreases, resulting in an increase in the oscillation frequency of the VCO.

## 2.2. Current Starved VCO

### 2.2.1. The output response of VCO with target frequency using transient analysis



**Figure 11:** TRAN analysis based on Vctrl change

#### Output rising time

```
riseTime(VT("/out") 0 nil VAR("vdd") nil 10 90 nil "time")
```

In a current-starved VCO, decreasing the control voltage typically increases rise time, slowing down the charging of capacitors and reducing oscillation frequency.

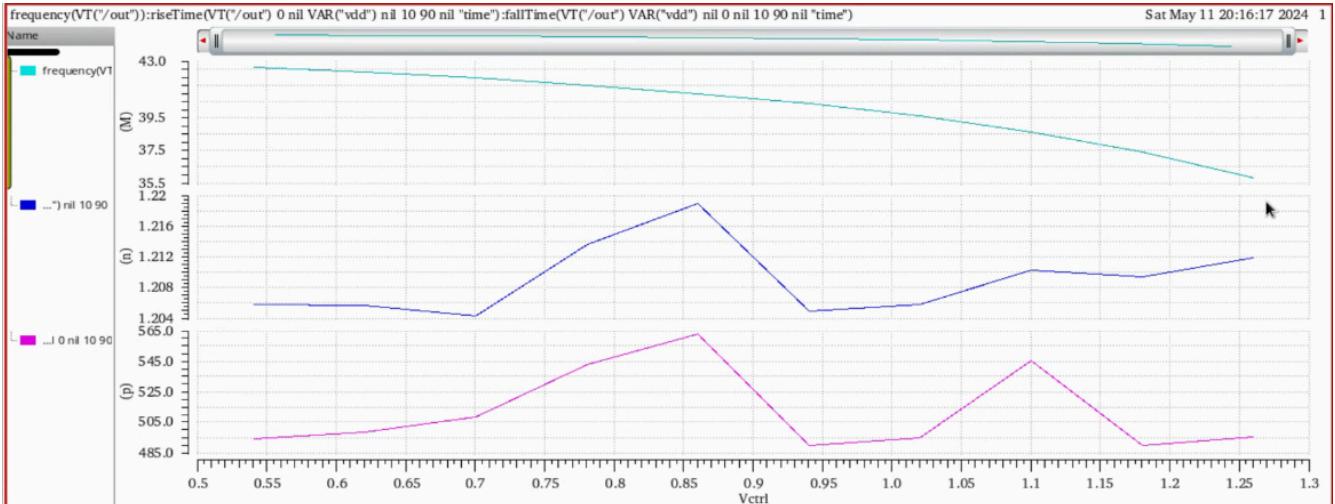
Additionally, the rise time can also be influenced by the sizes and characteristics of the transistors used in the current sources and inverters, as well as any parasitic capacitances present in the circuit.

#### Output falling time

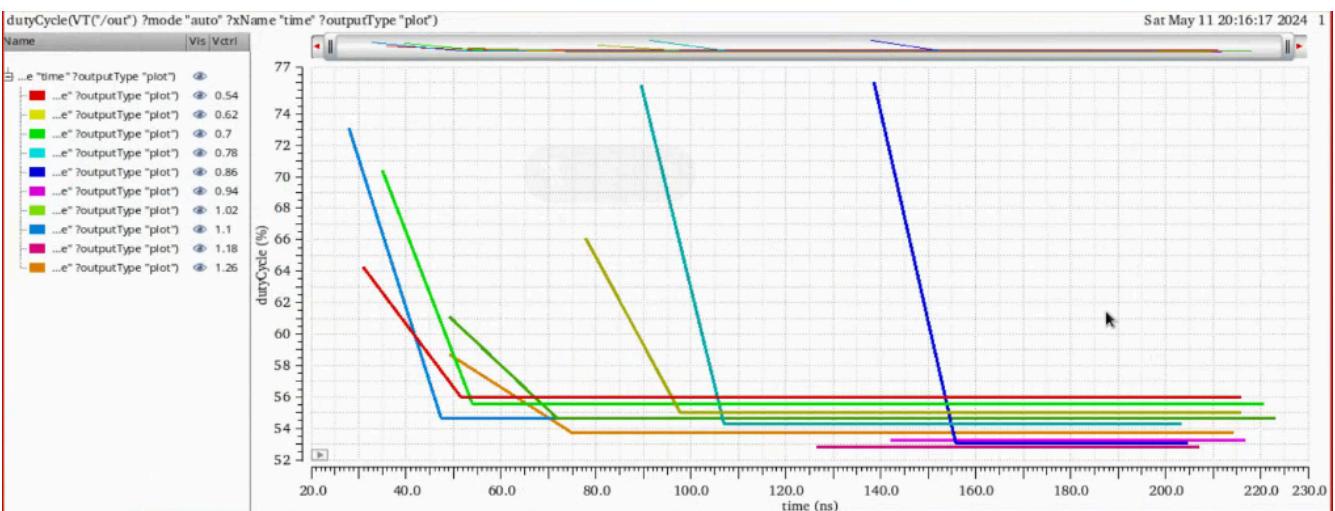
```
fallTime(VT("/out") VAR("vdd") nil 0 nil 10 90 nil "time")
```

#### Duty cycle

```
dutyCycle(VT("/out") ?mode "auto" ?xName "time" ?outputType "plot")
```



**Figure 12:** risingTime (blue line) and fallingTime (pink line) based on Vctrl change



**Figure 13:** dutyCycle of output signal

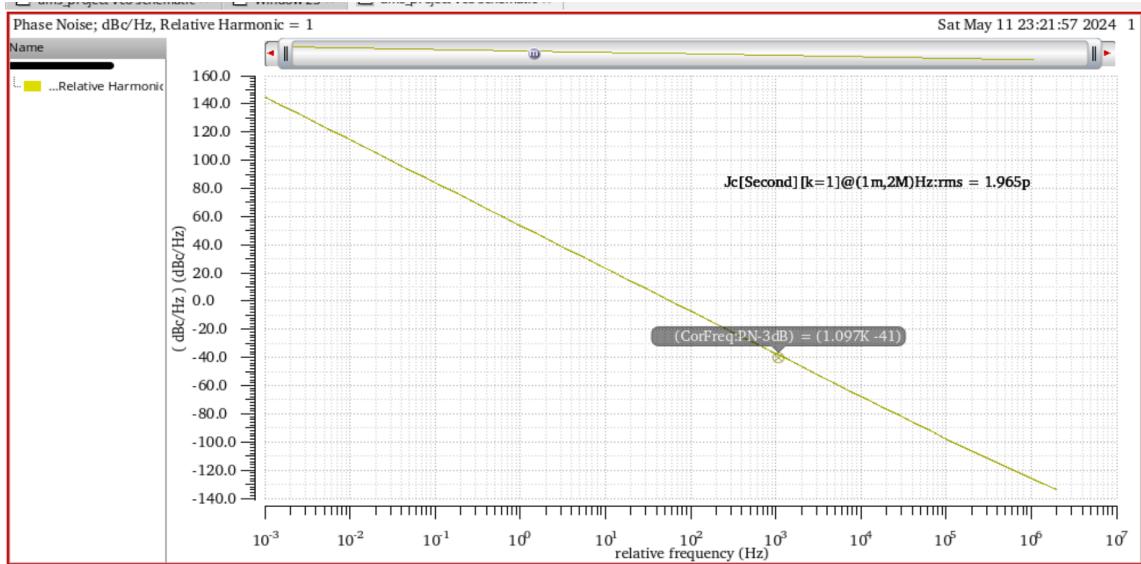
If the circuit operates under unstable conditions, such as temperature or supply voltage fluctuations, the duty cycle may be uneven. When adjusting the input voltage from 0.3VDD to 0.7VDD, the duty cycle level is about 55% when operating stably.

### The tuning range of VCO with control voltage from 0.3VDD to 0.7VDD

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Vctrl=540m						
1	ams_project:vco:1	/out				
1	ams_project:vco:1	frequency(VT("/out"))	42.66M			
1	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
1	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.206n			
1	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	494.5p			
Parameters: Vctrl=620m						
2	ams_project:vco:1	/out				
2	ams_project:vco:1	frequency(VT("/out"))	42.37M			
2	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
2	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.206n			
2	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	499.4p			
Parameters: Vctrl=700m						
3	ams_project:vco:1	/out		Vctrl=700m		
3	ams_project:vco:1	frequency(VT("/out"))	42.01M			
3	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
3	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.204n			
3	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	509p			
Parameters: Vctrl=780m						
4	ams_project:vco:1	/out				
4	ams_project:vco:1	frequency(VT("/out"))	41.56M			
4	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
4	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.214n			
4	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	543.7p			
Parameters: Vctrl=860m						
Parameters: Vctrl=700m						
3	ams_project:vco:1	/out				
3	ams_project:vco:1	frequency(VT("/out"))	42.01M			
3	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
3	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.204n			
3	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	509p			
Parameters: Vctrl=780m						
4	ams_project:vco:1	/out				
4	ams_project:vco:1	frequency(VT("/out"))	41.56M			
4	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
4	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.214n			
4	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	543.7p			
Parameters: Vctrl=860m						
5	ams_project:vco:1	/out				
5	ams_project:vco:1	frequency(VT("/out"))	41.01M			
5	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
5	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.219n			
5	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	563.5p			
Parameters: Vctrl=940m						
6	ams_project:vco:1	/out				
6	ams_project:vco:1	frequency(VT("/out"))	40.46M			
6	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
6	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.205n			
6	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	490.3p			
Parameters: Vctrl=1.02						
6	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	490.3p			
Parameters: Vctrl=1.02						
7	ams_project:vco:1	/out				
7	ams_project:vco:1	frequency(VT("/out"))	39.68M			
7	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
7	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.206n			
7	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	495p			
Parameters: Vctrl=1.1						
8	ams_project:vco:1	/out				
8	ams_project:vco:1	frequency(VT("/out"))	38.69M			
8	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
8	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.21n			
8	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	545.9p			
Parameters: Vctrl=1.18						
9	ams_project:vco:1	/out				
9	ams_project:vco:1	frequency(VT("/out"))	37.45M			
9	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
9	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.21n			
9	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	490p			
Parameters: Vctrl=1.26						
10	ams_project:vco:1	/out				
10	ams_project:vco:1	frequency(VT("/out"))	35.88M			
10	ams_project:vco:1	dutyCycle(VT("/out"))?mode "aut..."				
10	ams_project:vco:1	riseTime(VT("/out")) 0 nil VAR("vd..."	1.212n			
10	ams_project:vco:1	fallTime(VT("/out")) VAR("vdd") ni...	496.2p			

Figure 14: Analysis some measurement by calculator

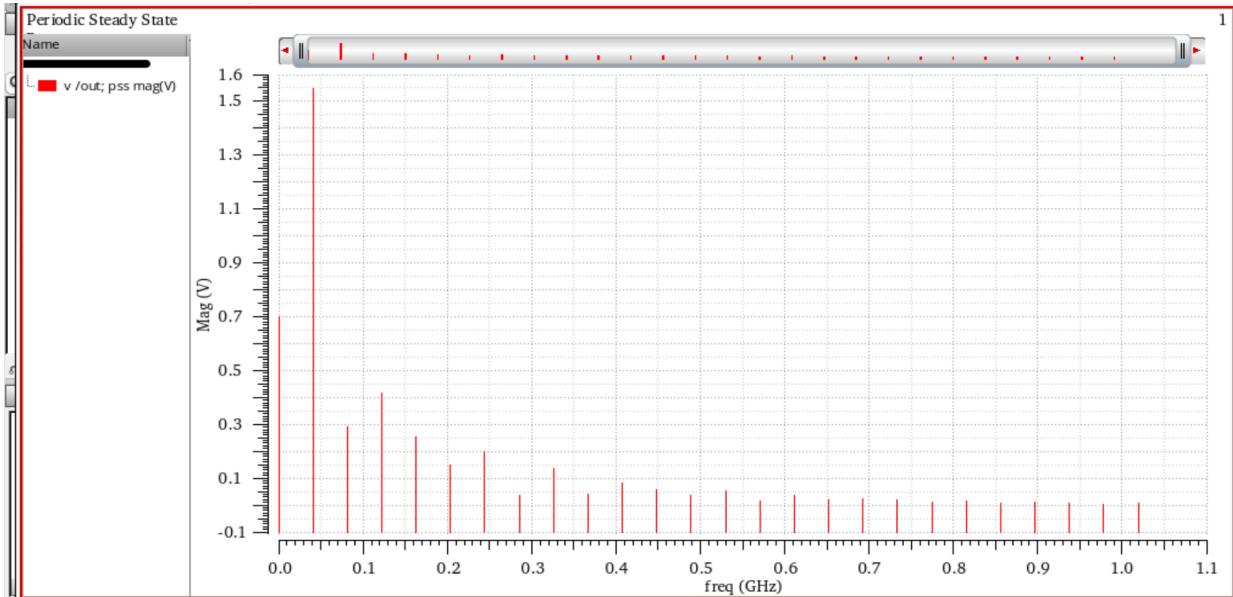
## 2.2.2. Jitter



**Figure 15:** Analysis Jitter

## 2.2.3. Phase noise

### Periodic Steady State (PSS)



**Figure 16:** Analysis PSS

Frequency can be adjusted to change pss magnitude power. Some ways to adjust frequency include changing the capacitor or control voltage.

## Phase noise

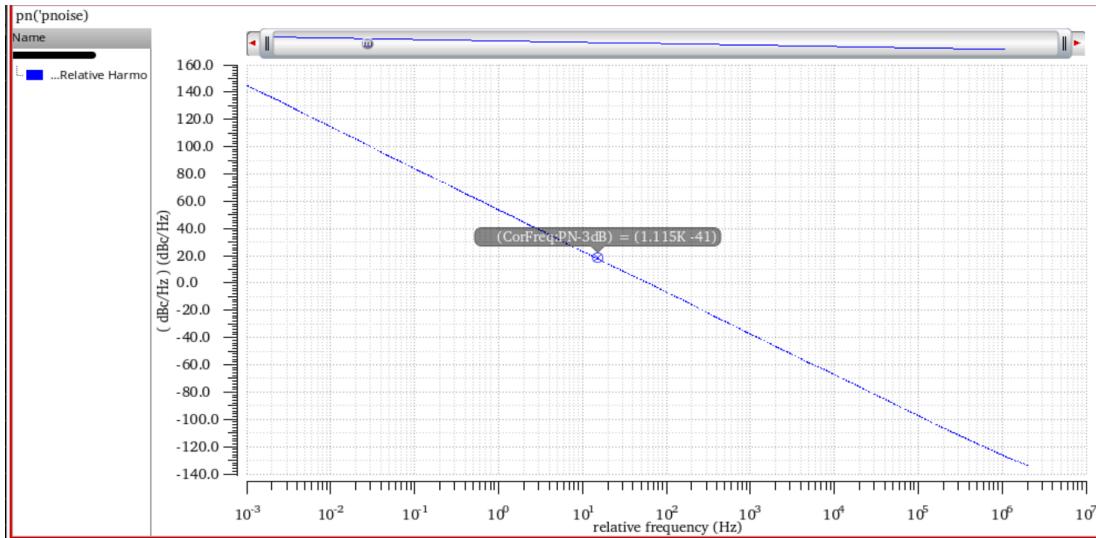


Figure 16: Analysis Phase noise

### 2.2.4. Power

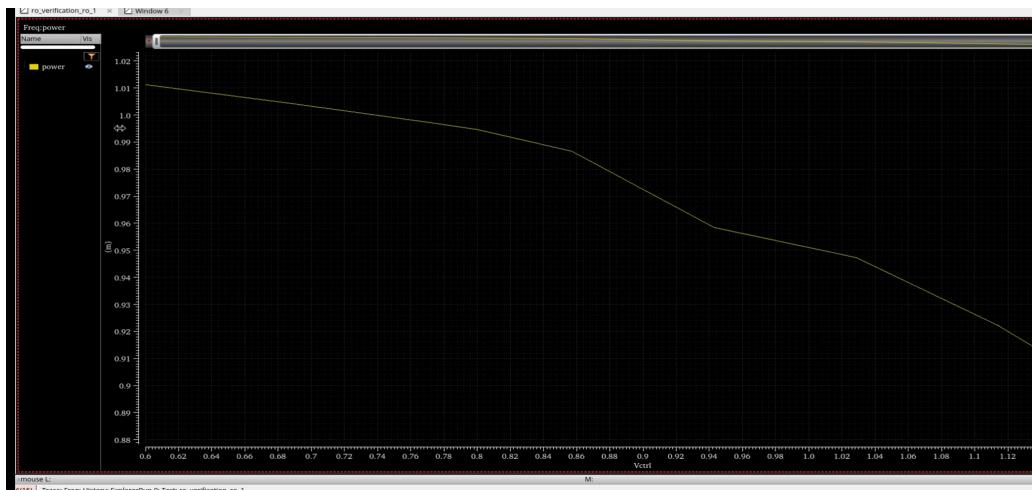


Figure 17: Analysis power consumption

## PART B: LC VCO

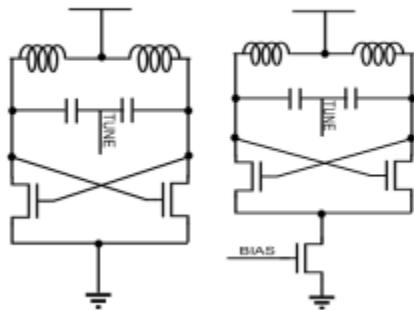
### 1. INTRODUCTION

An LC VCO, or Voltage-Controlled Oscillator, is a type of oscillator circuit that generates an oscillating output signal whose frequency is controlled by a varying voltage input. The "LC" in LC VCO stands for the components typically used in its resonant tank circuit: an inductor (L) and a capacitor (C).

In an LC VCO, the inductor and capacitor are arranged in a feedback loop configuration that allows the circuit to sustain oscillations at a certain frequency determined by the values of these components. The voltage-controlled element, often a varactor diode, is incorporated into the resonant tank circuit to modulate the capacitance, thereby altering the resonant frequency of the circuit in response to changes in the control voltage.

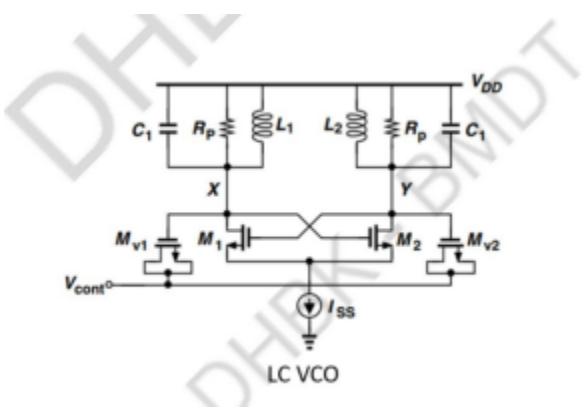
LC VCOs find extensive applications in various electronic systems, including frequency synthesizers, phase-locked loops, and communication systems. They offer advantages such as high tuning range, low phase noise, and compact size, making them suitable for use in a wide range of frequency agile and modulation applications.

#### 1.1. Theory



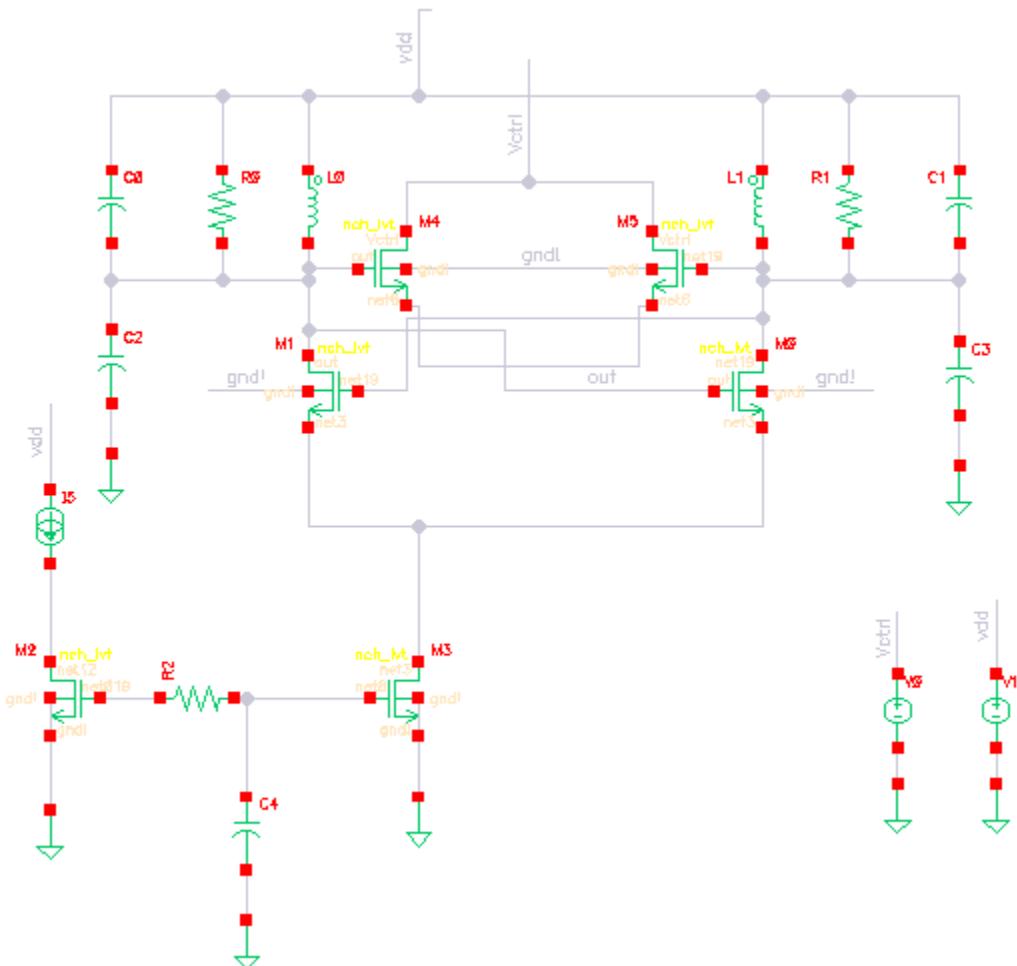
**Figure 18:** NMOS VCO

The LC VCO depicted in Figure 18 utilizes NMOS transistors, two inductors, two capacitors, and cross-coupled NMOS switches. The negative resistance is generated by the transconductance of the cross-coupled NMOS devices. The varactor capacitors, which change with tuning voltage, are isolated from the power supply by inductors and from ground by the cross-coupled NMOS pair. While this design is susceptible to supply disturbances, a tail current source is introduced in a similar topology to limit supply current and control total power consumption. This allows designers to regulate negative resistance and oscillation amplitude. However, studies have shown that removing the tail current source can improve phase noise performance, presenting a trade-off between design controllability, power consumption, and phase noise.



The complementary LC VCO combines features of both PMOS-only and NMOS-only LC VCOs. It clips voltage swing to VDD and ground, providing swing between them to avoid transistor stress. It's advantageous in CMOS tech for immunity to process variation. Symmetrical rise and fall reduce 1/f noise. However, it increases area due to more transistors and may lead to larger noise from additional noise sources. Overall, it's effective in reducing stress and process variation but may trade off with increased area and noise.

## 1.2. Schematic



**Figure 19:** LC VCO schematic

## 2. MEASUREMENT

### 2.1. The output response of VCO with target frequency using transient analysis

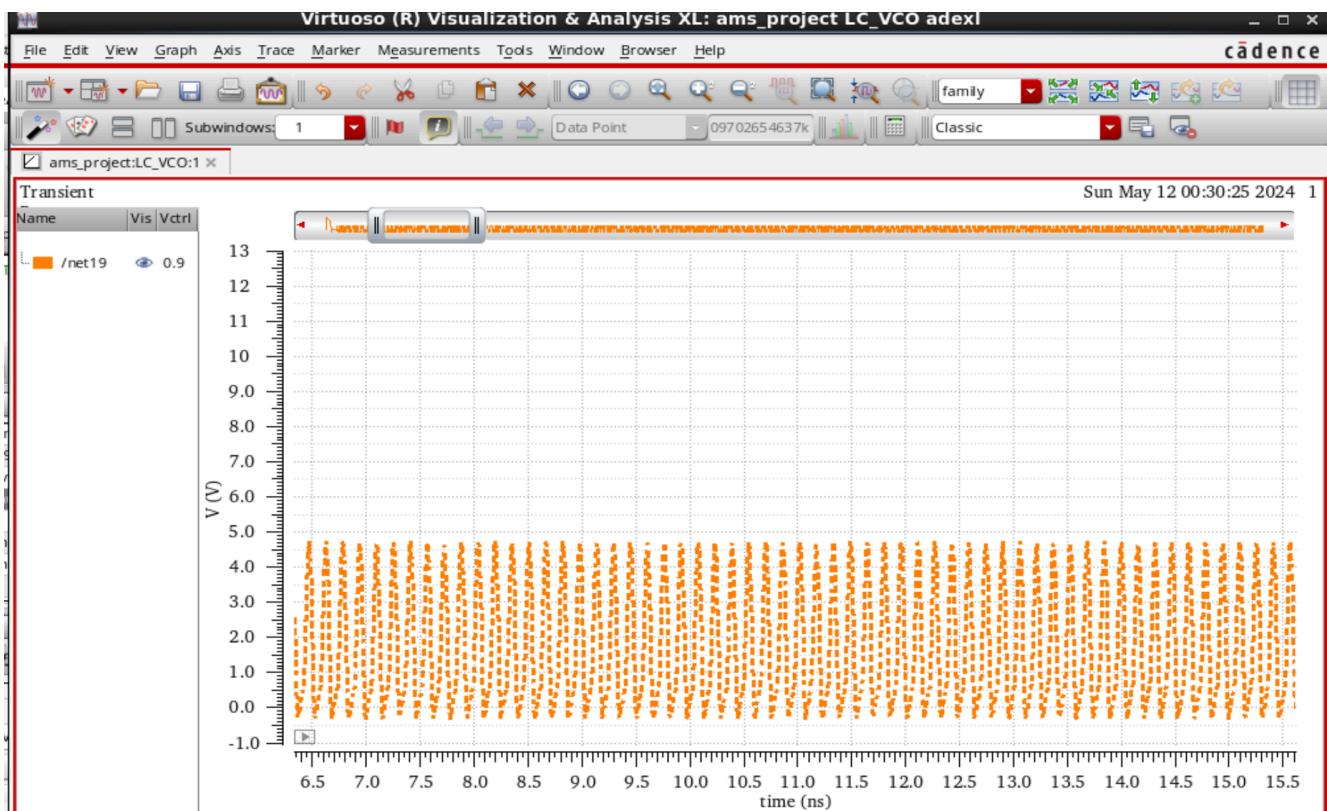
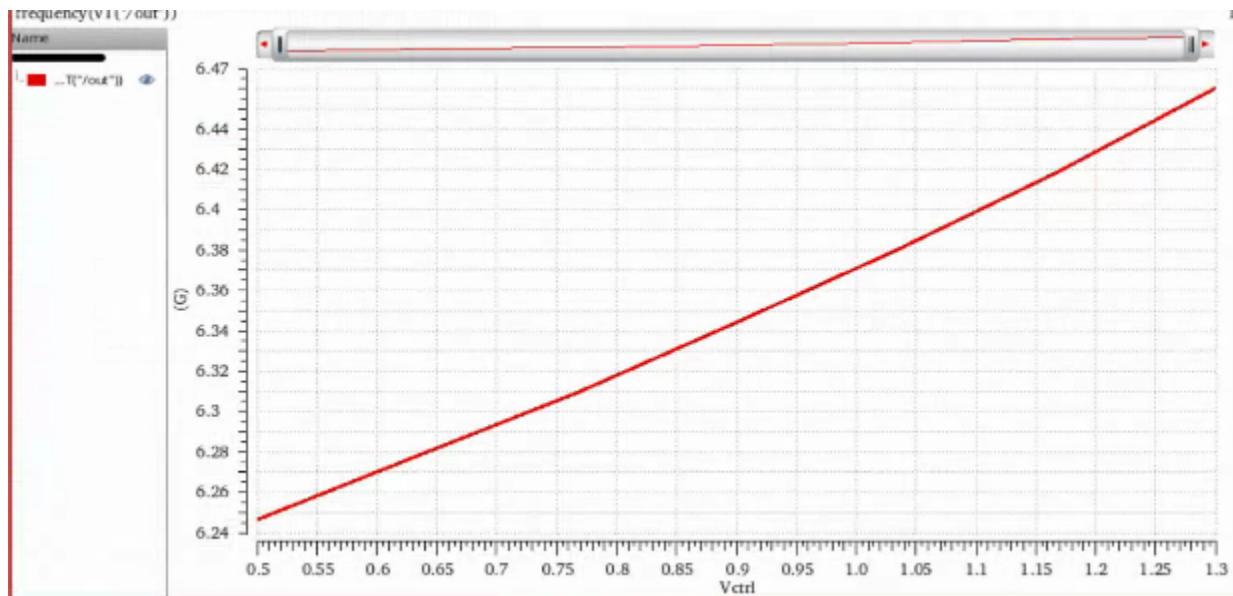


Figure 20: TRAN analysis of output



**Figure 21:** Frequency analysis of output

Figure 21 show Frequency analysis of output when Vctrl is in range  $0.3 \times Vdd$  to  $0.7 \times Vdd$ . As we can see, the higher Vctrl, the higher frequency value too.

### Output rising time

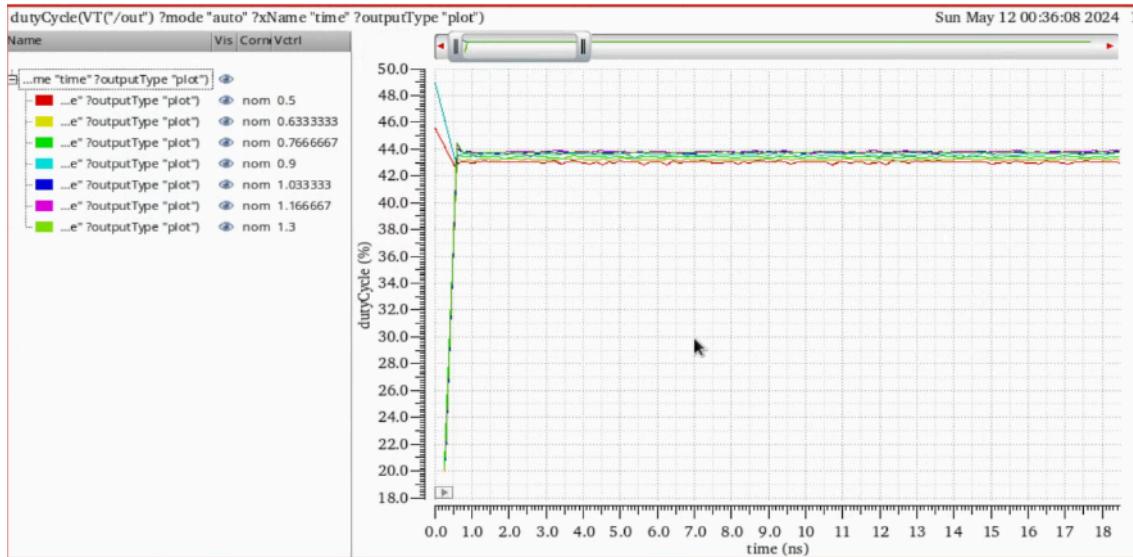
```
riseTime(VT("/out") 0 nil VAR("vdd") nil 10 90 nil "time")
```

### Output falling time

```
fallTime(VT("/out") VAR("vdd") nil 0 nil 10 90 nil "time")
```

### Duty cycle

```
dutyCycle(VT("/out") ?mode "auto" ?xName "time" ?outputType "plot")
```



**Figure 22:** dutyCycle analysis of output

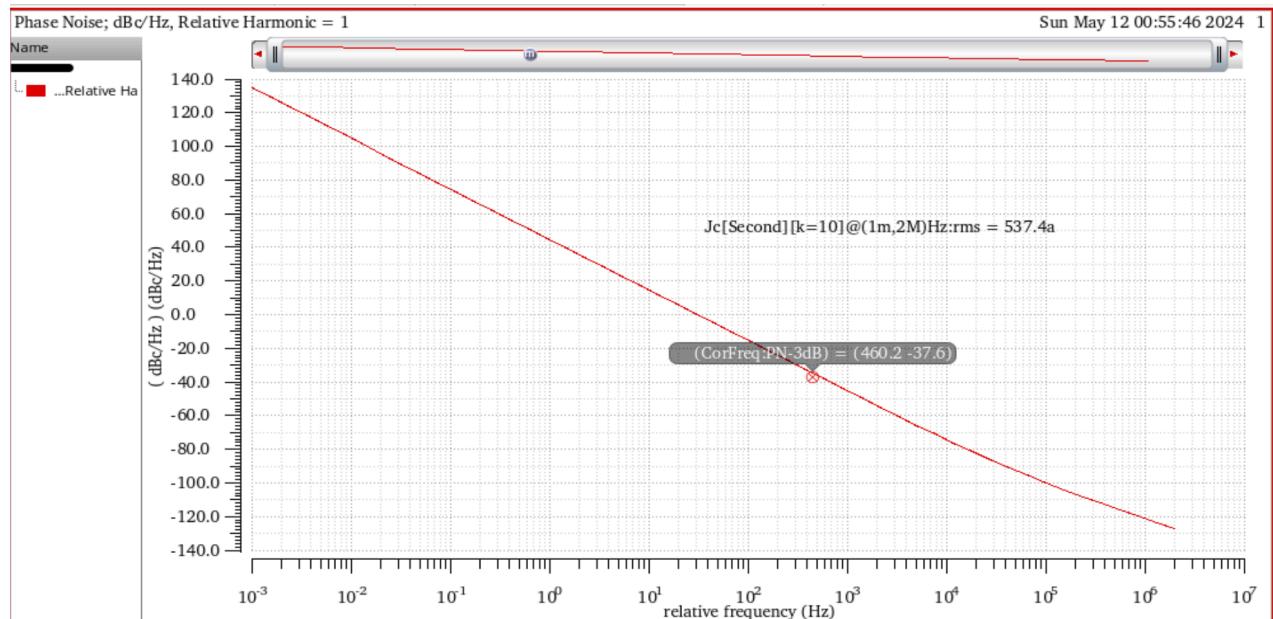
The tuning range of VCO with control voltage from 0.3VDD to 0.7VDD

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Vctrl=900m						
5	ams_project:LC_VCO:1 /net19					
5	ams_project:LC_VCO:1 frequency(VT("/out"))	6.345G				
5	ams_project:LC_VCO:1 dutyCycle(VT("/out")) ?mode "aut..."					
5	ams_project:LC_VCO:1 riseTime(VT("/out") 0 nil VAR("vdd"))	11.25p				
5	ams_project:LC_VCO:1 fallTime(VT("/out") VAR("vdd") ni...)	11.25p				
Parameters: Vctrl=1.033						
6	ams_project:LC_VCO:1 /net19					
6	ams_project:LC_VCO:1 frequency(VT("/out"))	6.381G				
6	ams_project:LC_VCO:1 dutyCycle(VT("/out")) ?mode "aut..."					
6	ams_project:LC_VCO:1 riseTime(VT("/out") 0 nil VAR("vdd"))	10.28p				
6	ams_project:LC_VCO:1 fallTime(VT("/out") VAR("vdd") ni...)	10.28p				
Parameters: Vctrl=1.166						
7	ams_project:LC_VCO:1 /net19					
7	ams_project:LC_VCO:1 frequency(VT("/out"))	6.419G				
7	ams_project:LC_VCO:1 dutyCycle(VT("/out")) ?mode "aut..."					
7	ams_project:LC_VCO:1 riseTime(VT("/out") 0 nil VAR("vdd"))	9.727p				
7	ams_project:LC_VCO:1 fallTime(VT("/out") VAR("vdd") ni...)	9.727p				
Parameters: Vctrl=1.3						
8	ams_project:LC_VCO:1 /net19					
8	ams_project:LC_VCO:1 frequency(VT("/out"))	6.461G				
8	ams_project:LC_VCO:1 dutyCycle(VT("/out")) ?mode "aut..."					
8	ams_project:LC_VCO:1 riseTime(VT("/out") 0 nil VAR("vdd"))	8.852p				
8	ams_project:LC_VCO:1 fallTime(VT("/out") VAR("vdd") ni...)	8.852p				

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Vctrl=500m						
2	ams_project:LC_VCO:1	/net19				
2	ams_project:LC_VCO:1	frequency(VT("/out"))	6.247G			
2	ams_project:LC_VCO:1	dutyCycle(VT("/out")) ?mode "aut..."				
2	ams_project:LC_VCO:1	riseTime(VT("/out")) 0 n1l VAR("vd..."	15.25p			
2	ams_project:LC_VCO:1	fallTime(VT("/out")) VAR("vdd") ni...	15.25p			
Parameters: Vctrl=633.3m						
3	ams_project:LC_VCO:1	/net19				
3	ams_project:LC_VCO:1	frequency(VT("/out"))	6.279G			
3	ams_project:LC_VCO:1	dutyCycle(VT("/out")) ?mode "aut..."				
3	ams_project:LC_VCO:1	riseTime(VT("/out")) 0 n1l VAR("vd..."	13.35p			
3	ams_project:LC_VCO:1	fallTime(VT("/out")) VAR("vdd") ni...	13.35p			
Parameters: Vctrl=766.7m						
4	ams_project:LC_VCO:1	/net19				
4	ams_project:LC_VCO:1	frequency(VT("/out"))	6.31G			
4	ams_project:LC_VCO:1	dutyCycle(VT("/out")) ?mode "aut..."				
4	ams_project:LC_VCO:1	riseTime(VT("/out")) 0 n1l VAR("vd..."	11.23p			
4	ams_project:LC_VCO:1	fallTime(VT("/out")) VAR("vdd") ni...	11.23p			
Parameters: Vctrl=900m						
5	ams_project:LC_VCO:1	/net19				
5	ams_project:LC_VCO:1	frequency(VT("/out"))	6.345G			
5	ams_project:LC_VCO:1	dutyCycle(VT("/out")) ?mode "aut..."				
5	ams_project:LC_VCO:1	riseTime(VT("/out")) 0 n1l VAR("vd..."	11.25p			
5	ams_project:LC_VCO:1	fallTime(VT("/out")) VAR("vdd") ni...	11.25p			

**Figure 21:** The tuning range of VCO with control voltage from 0.3VDD to 0.7VDD

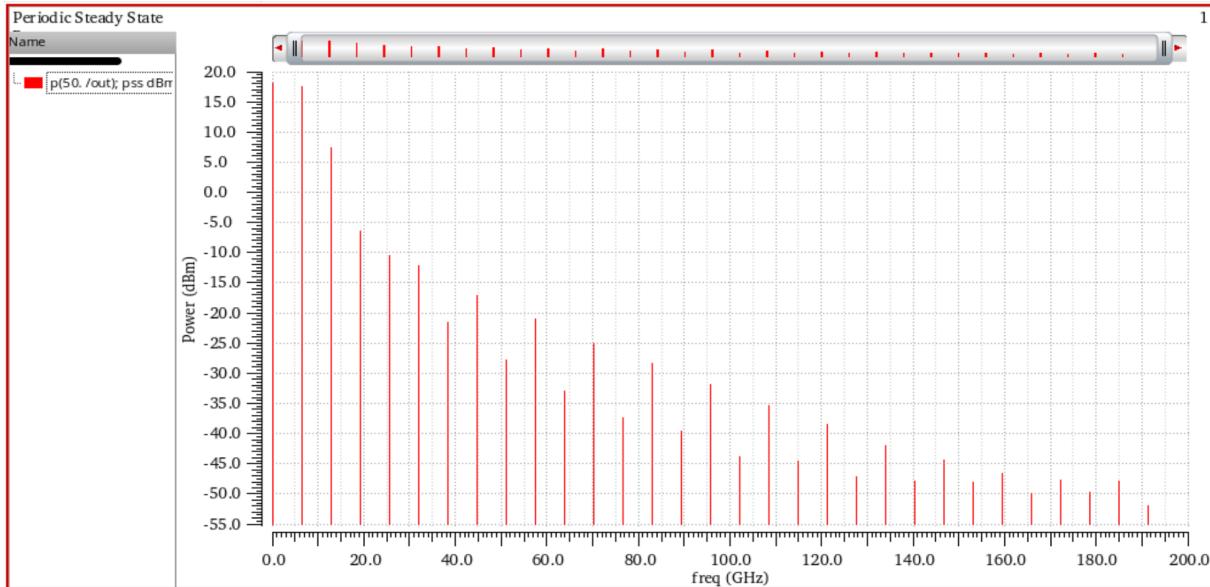
## 2.2. Jitter



**Figure 22:** Analysis Jitter

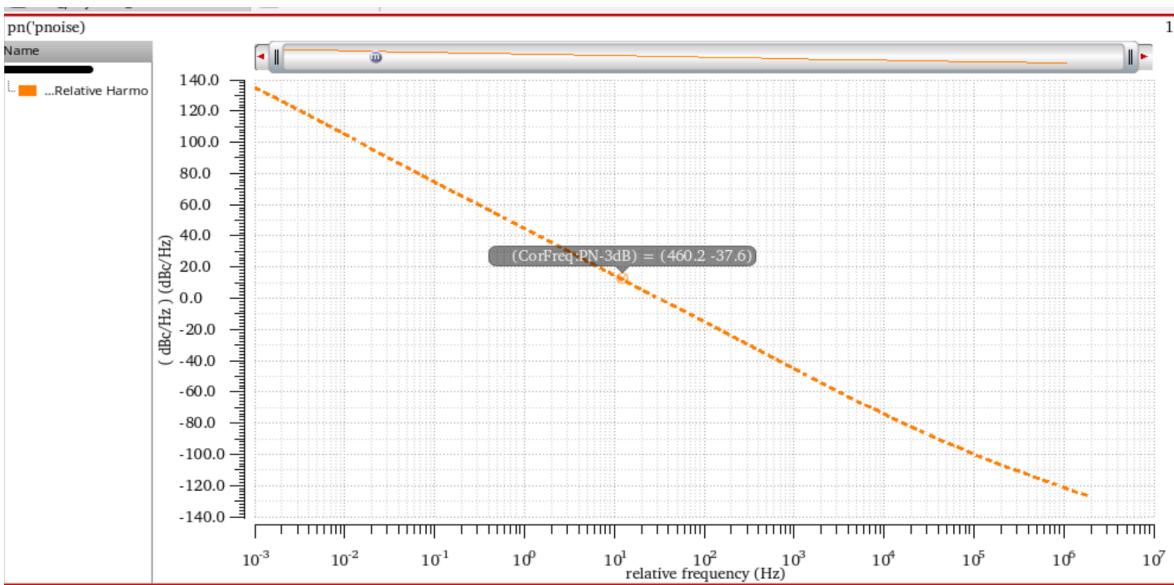
### 2.3. Phase noise

#### Periodic Steady State (PSS)



**Figure 23:** Analysis PSS

#### Phase noise



**Figure 24:** Analysis of phase noise

### 2.4. Power

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Vctrl=900m						
1	ams_project:LC_VCO:1	(IDC("/V1/MINUS") * VDC("/vdd"))	224.7m			
1	ams_project:LC_VCO:1	/V1/MINUS				

**Figure 25:** Analysis of power consumption

## IV. APPLICATION OF VCO

Voltage-Controlled Oscillators (VCOs) find a multitude of applications across various fields due to their ability to generate oscillations with a frequency that can be controlled by an input voltage. Some common applications of VCOs include:

1. Frequency Modulation (FM) and Phase Modulation (PM): VCOs are extensively used in FM and PM communication systems. By modulating the control voltage of the VCO, the frequency or phase of the output signal can be varied, allowing for the transmission of information.
2. Phase-Locked Loops (PLLs): VCOs are integral components of PLLs, which are widely employed in frequency synthesis, clock generation, and synchronization applications. In a PLL, the VCO locks onto a reference signal and produces an output signal with a frequency and phase that tracks the reference signal.
3. Frequency Synthesizers: VCOs play a crucial role in frequency synthesizers, which are used to generate precise and stable output frequencies across a wide range. By controlling the voltage applied to the VCO, the output frequency of the synthesizer can be adjusted.
4. Radar Systems: VCOs are utilized in radar systems for generating continuous-wave (CW) signals, as well as for frequency agility in frequency-modulated continuous-wave (FMCW) radar systems. They enable the radar to transmit and receive signals at different frequencies, facilitating target detection and tracking.
5. Wireless Communication Systems: VCOs are essential components in wireless communication systems, including cellular networks, Wi-Fi, Bluetooth, and satellite communication systems. They are used in frequency synthesizers, local oscillators, and transmitters to generate carrier signals and modulate data.
6. Test and Measurement Instruments: VCOs are employed in various test and measurement instruments, such as signal generators, spectrum analyzers, and frequency counters. They provide stable and adjustable oscillation frequencies for testing and analyzing electronic circuits and systems.

## V. CONCLUSION

Ring VCO	LC VCO
1) highly integrated in VLSI 2) low power 3) small die area occupancy	1) outstanding phase noise and jitter performance at high frequency.
1) As frequency increases phase noise and jitter performance degrades.	1) contains an inductor and a varactor (variable capacitor) which are large area components, and thus is not as suitable for VLSI 2) high power consumption 3) occupies a large die area

Clearly, the ringVCO is most suitable for low power, highly integrated applications that require a large tuning range and a low die space area. In contrast, the LC VCO out performs the ringVCO in low noise applications. For mobile wireless applications one desires low power, hence the ringVCO may be of choice. However, wireless applications require outstanding noise (phase noise and jitter) performance at high frequency, hence the LC VCO may be of choice.

For mobile wireless applications one desires low power, hence the ringVCO may be of choice. However, wireless applications require outstanding noise (phase noise and jitter) performance at high frequency, hence the LC VCO may be of choice. Having said that, there may be specific applications where either the ring VCO or the LC VCO topology may be optimized to perform sufficiently well.

## **VI. REFERENCE DOCUMENT**

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