LABORATORY 1

MOS DEVICE CHARACTERIZATION

OBJECTIVES

No.	Objectives	Requirements
1	I/V characteristics of NMOS transistor	▪ Drawing curves $I_{DS} = f(V_{GS})$, and $I_{DS} = f(V_{DS})$ ▪ Determine the threshold voltage and operation region of the NMOS device.
2	The effects on I/V characteristics when V_{GS}, width, and length vary of NMOS transistor	▪ Drawing curves $I_{DS} = f(V_{DS})$ when these parameters vary. ▪ Consider curves drawn.
3	Second order effects (body effect, channel-length modulation) of NMOS transistor	▪ Drawing curves $I_{DS} = f(V_{GS})$, and $I_{DS} = f(V_{DS})$ when these effects occur. ▪ Consider curves drawn.
4	The effects on I/V characteristics when V_{SG}, width, and length vary of PMOS transistor	▪ Drawing curves $I_{SD} = f(V_{SD})$ when these parameters vary. ▪ Consider curves drawn.

PREPARATION FOR LAB 1

- Finished Lab 0 at home. Requirement:
  - Create library, schematic cellview and symbol of INV with ***tsmc65 technology***.
  - Simulate transient analysis with ADE-L.

EXPERIMENT 1

Objective: Known NMOS operations and I-V characteristics

Requirements: Simulate and draw curves $I_{DS} = f(V_{GS})$ and $I_{DS} = f(V_{DS})$ of NMOS currently used.

Instruction: Assemble the circuit as shown in ***Figure 1***, setting parameters for power supplies (using ***vdc*** source), with $L = 60nm$, $W = 120nm$, $V_{SB} = 0V$.

Note: Consider "***nch_lvt"*** device in ***tsmc65 technology*** for all lab experiments.

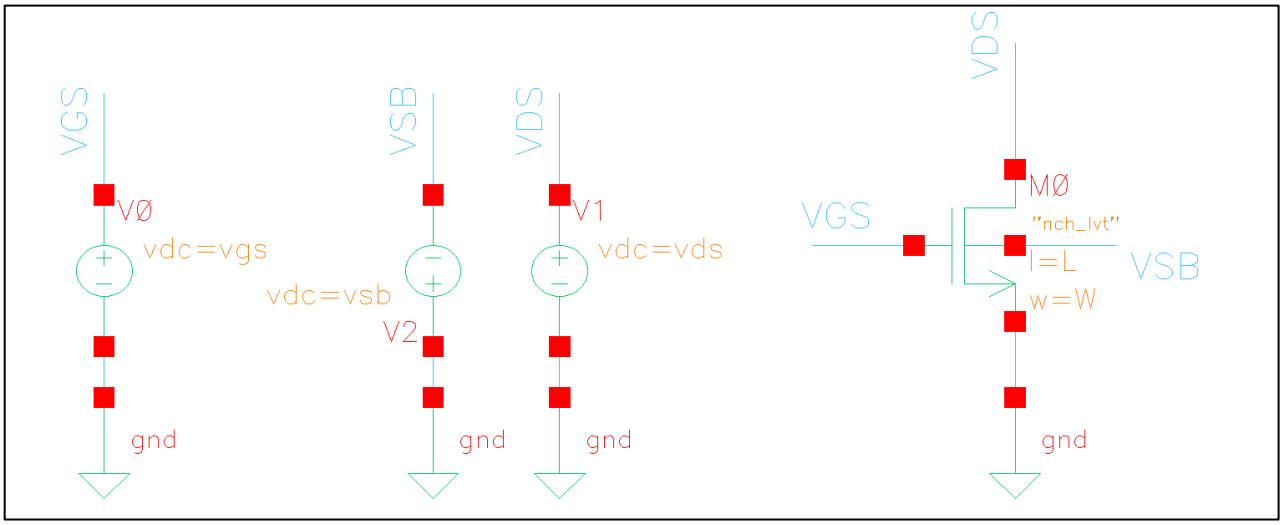
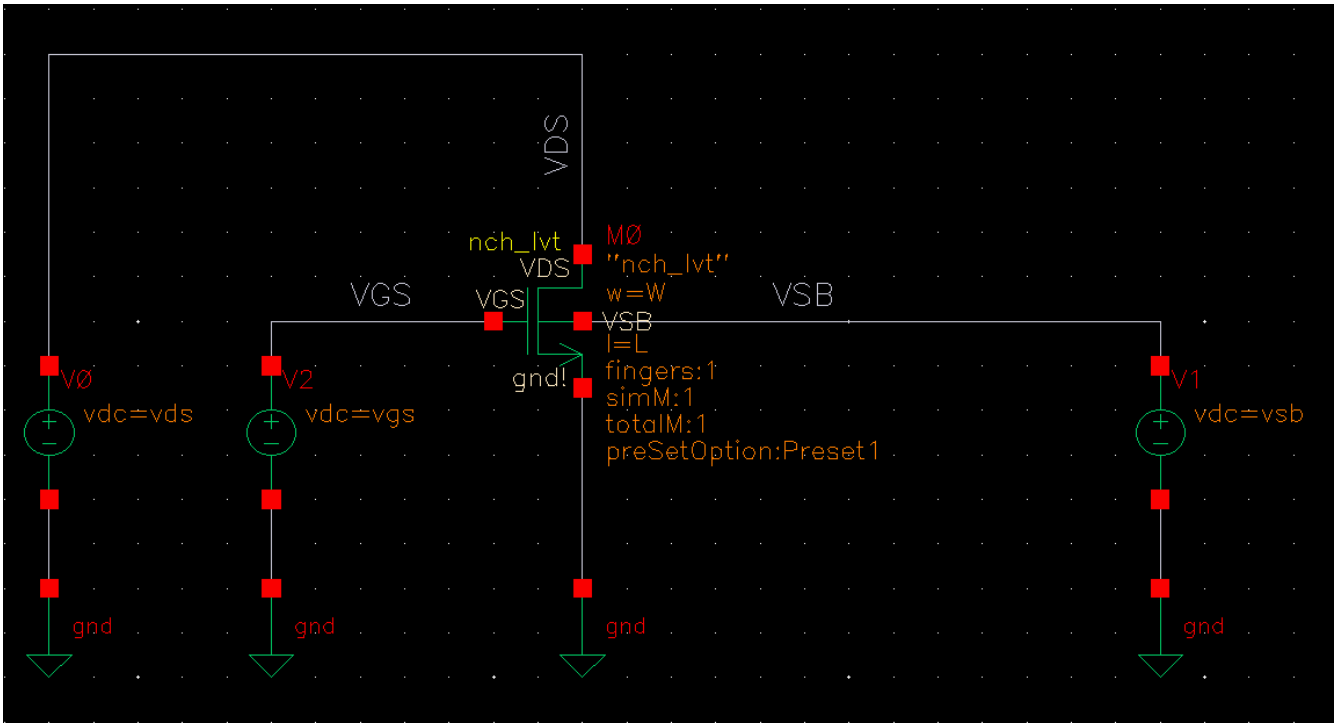


Figure 1. Circuit diagram for characterizing NMOS characteristics



Check: Your report must show these results and explain the NMOS operation region based on waveform.

Draw a curve when fixing the value $V_{GS} = 1.0V$, and sweeping variable V_{DS} from 0V to 1.2V to characterize the change of I_{DS} with respect to V_{DS}.

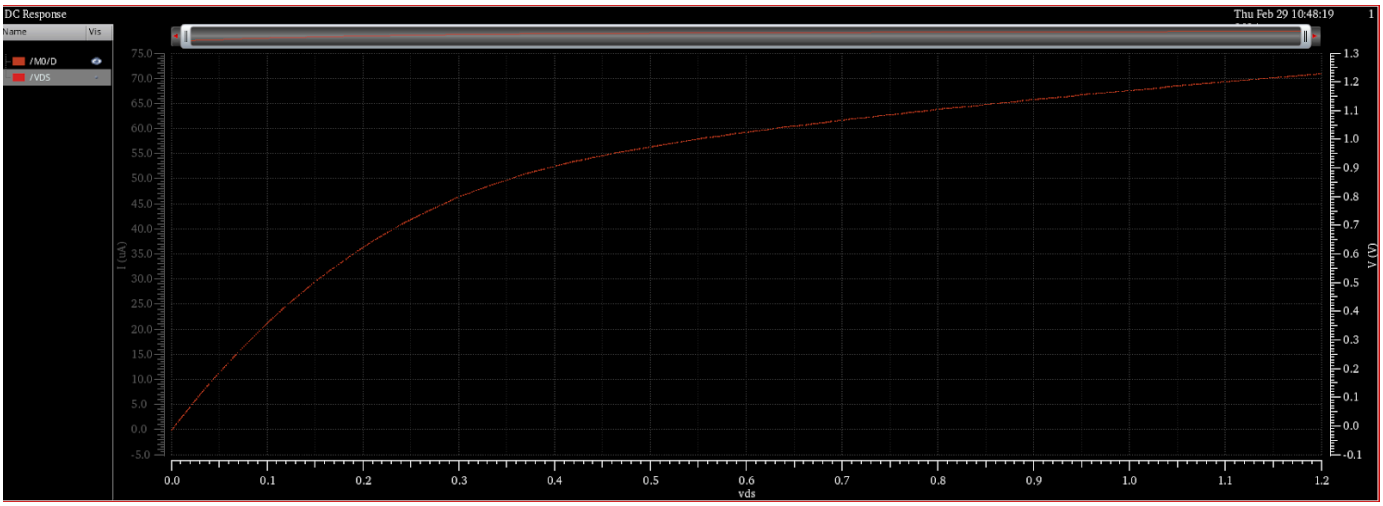


Figure 2. Waveform $I_{DS} = f(V_{DS})$

$V_{GS} = 1\ (V), V_{ov} = 1 - V_{TH}$

no cut-off

In triode region: $V_{DS} < V_{OV}$

$\Rightarrow V_{DS} < 1 - V_{TH}$

In saturation region

$V_{DS} \geq V_{OV}$

$\Rightarrow V_{DS} \geq 1 - V_{TH}\ (V)$

Based on the picture, at $V_{DS} = [0.4, 0.8]$, the I_D saturation phenomenon begins

$\Rightarrow V_{TH} \in [0.2, 0.6]\ (V)$

Draw a curve when fixing the value V_{DS} = 1.0V, and sweeping variable V_{GS} from 0V to 1.2V with step = 0.01V to characterize the change of I_{DS} with respect to V_{GS}.

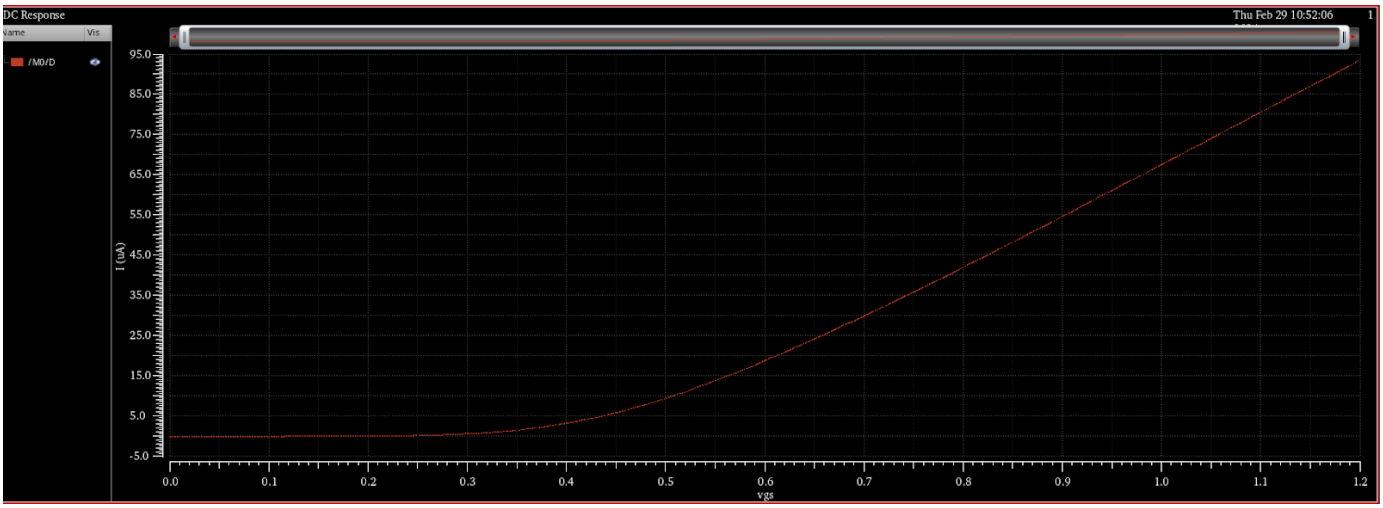


Figure 3. Waveform $I_{DS} = f(V_{GS})$

In cut off region $I_D \approx 0$ and $V_{GS} < V_{TH}$ until $V_{GS} \approx 0.3\ (V)$

$\Rightarrow V_{TH} \approx 0.3\ (V)$

In triode $V_{DS} < V_{OV}$

$\Rightarrow 1 < V_{GS} - 0.3$

$\Rightarrow V_{GS} > 0.7\ (V)$

In saturation region $V_{DS} > V_{OV}$

$\Rightarrow 0.3 < V_{GS} < 0.7\ (V)$

- ***Question:*** Propose ***at least one method*** to determine the threshold voltage of NMOS *nch_lvt* device.

At two distinct VGS levels, I assessed the FET's behavior (when the transistor was in its current saturation area)

$$\frac{I_{D1}}{I_{D2}} = \frac{K(V_{GS1} - V_T)^2}{K(V_{GS2} - V_T)^2}$$

$$\Rightarrow \frac{\sqrt{I_{D1}}}{\sqrt{I_{D2}}} = \frac{(V_{GS1} - V_T)}{(V_{GS2} - V_T)}$$

$$\Rightarrow \sqrt{I_{D1}}\,(V_{GS2} - V_T) = \sqrt{I_{D2}}\,(V_{GS1} - V_T)$$

$$\Rightarrow V_T\left(\sqrt{I_{D2}} - \sqrt{I_{D1}}\right) = \sqrt{I_{D2}}\,V_{GS1} - \sqrt{I_{D1}}\,V_{GS2}$$

$$\Rightarrow V_T = \frac{\sqrt{I_{D2}}\,V_{GS1} - \sqrt{I_{D1}}\,V_{GS2}}{\sqrt{I_{D2}} - \sqrt{I_{D1}}}$$

or we can get V_{TH} after determine cut off region as previous experiment

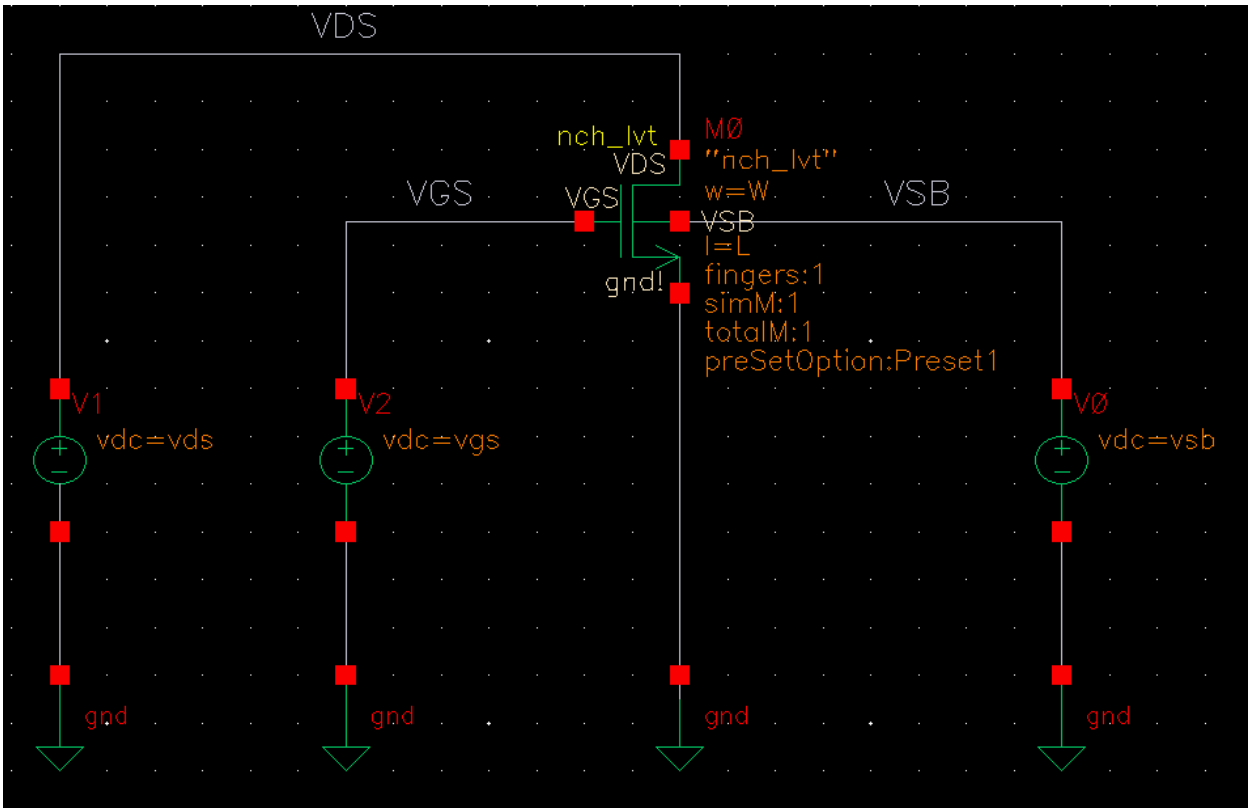
EXPERIMENT 2

Objective: The effects on I/V characteristics of NMOS when V_{GS}, width and length vary.

Requirements: Simulate and draw curves when V_{GS}, width and length vary.

Instruction:

- Setting parameters W, L, V_{GS}, V_{SB} and V_{DS} for convenience when characterizing the circuit shown in **Figure 1.**



- Sweep multiple variables in parallel using ADE-L: ***Tools*** → ***Parametric Analysis*** → ***Sweeps & Ranges Type*** (**Figure 4** is an example for setting multiple sweeping variables)
- You can refer to the setting in **Figure 4**, and observe the result shown in **Figures 5** and **6**.

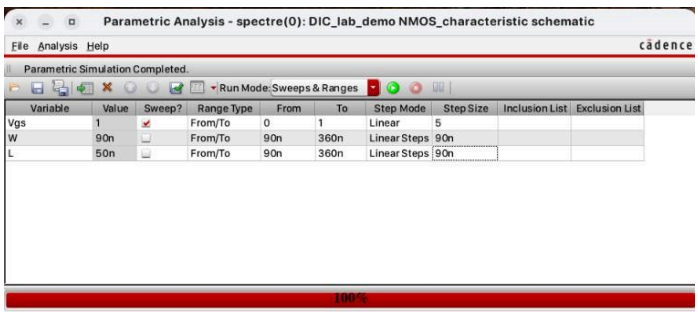


Figure 4. Setting parameters for characterizing $I_{DS} = f(V_{DS})$ at V_{GS} = {0, 0.25,0.5, 0.75,1.0} V

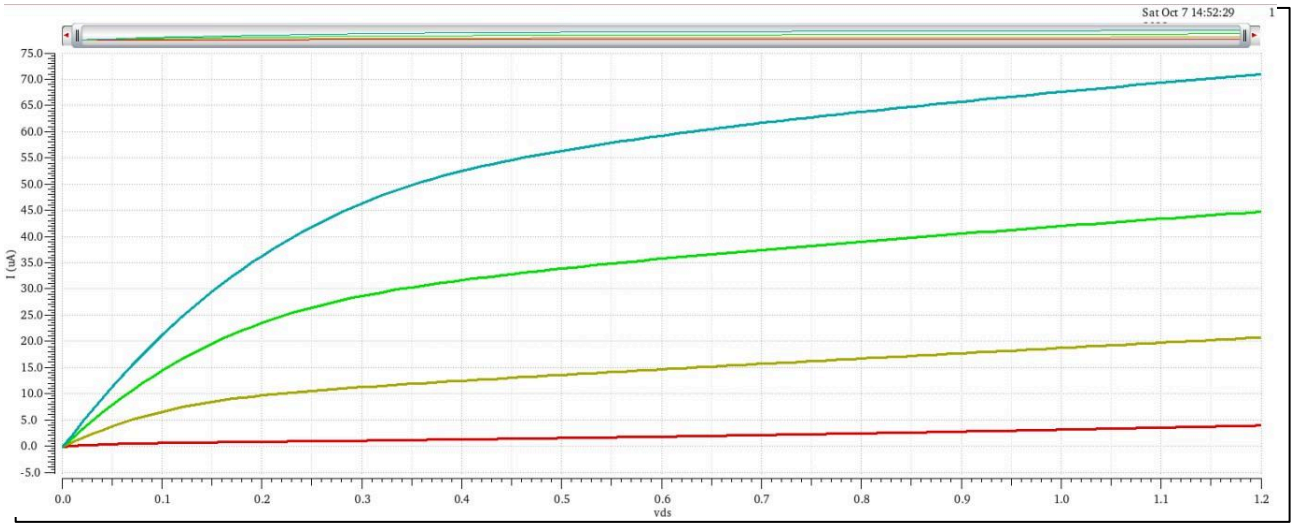


Figure 5. $I_{DS} = f(V_{DS})$ waveform with V_{GS} = {0, 0.25,0.5, 0.75,1.0} V

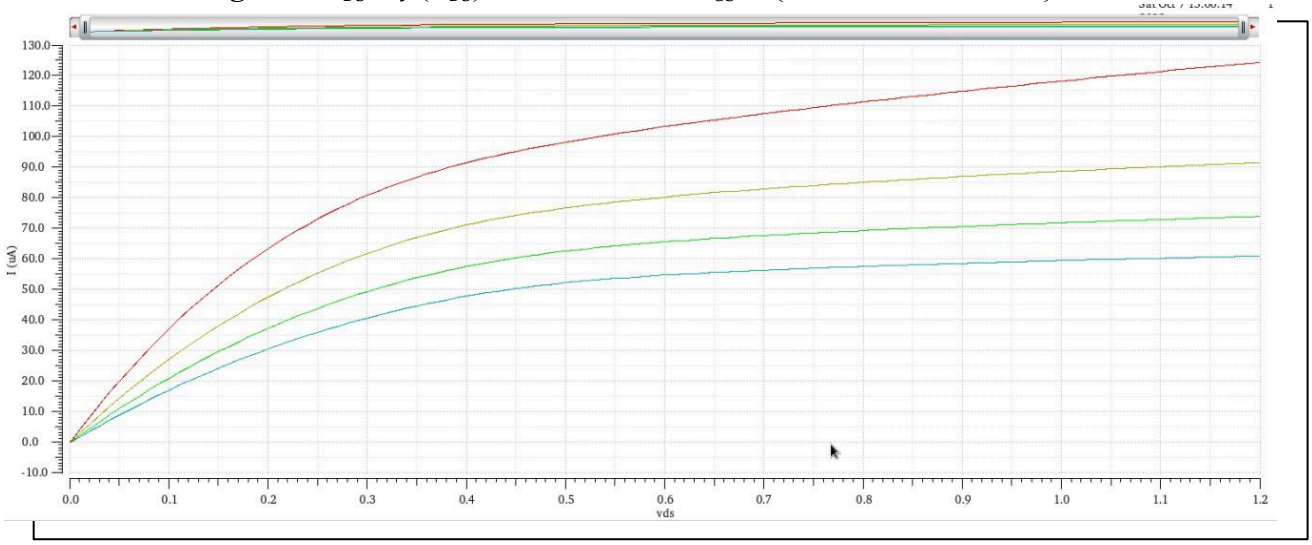
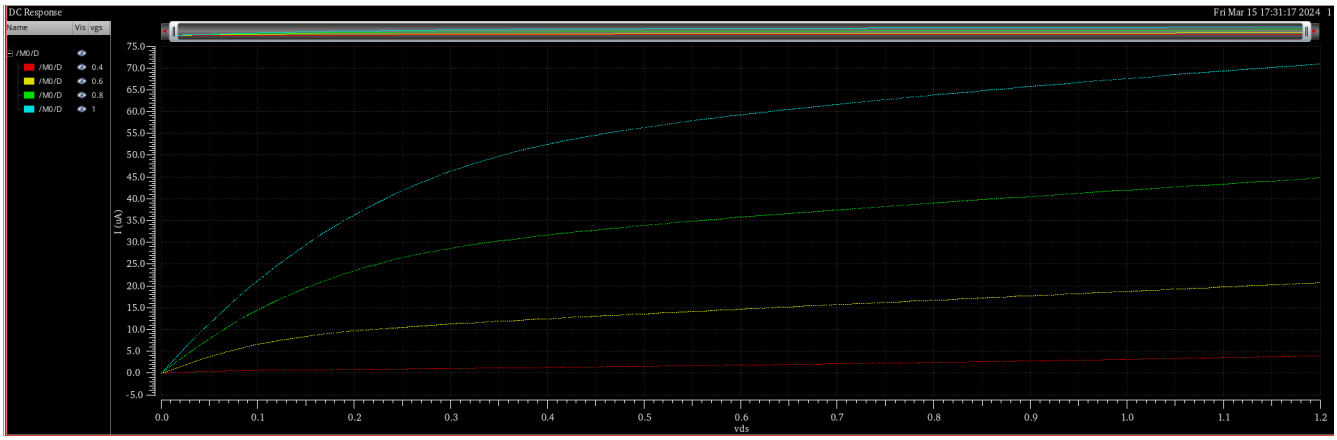


Figure 6. $I_{DS} = f(V_{DS})$ waveform with L = {90,180,270,360} nm

Check: Your result must show these results and summarize the conclusion of the current and operation region of NMOS with the width, length, and v_{gs} variation.

- Choose $L = 60nm$, $W = 120nm$ and $V_{SB} = 0V$. Draw curves $I_{DS} = f(V_{DS})$, sweeping variable V_{DS} from 0V to 1.2V with step = 0.01V and sweeping V_{GS} from 0.4V to 1.0V with step = 0.2V.



In cut off region $I_D \approx 0$ and $V_{GS} < V_{TH}$. Red line $I_{ds} \approx 0$

Get $V_{TH} = 0.3$ (Experiment 1)

In triode $V_{DS} < V_{OV}$

$\Rightarrow V_{DS} < V_{GS} - 0.3$

and $I_{DS} = k_n\left[(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\right]$

If $V_{GS} \uparrow$, $I_{DS} \uparrow$

In saturation region $V_{DS} > V_{OV}$

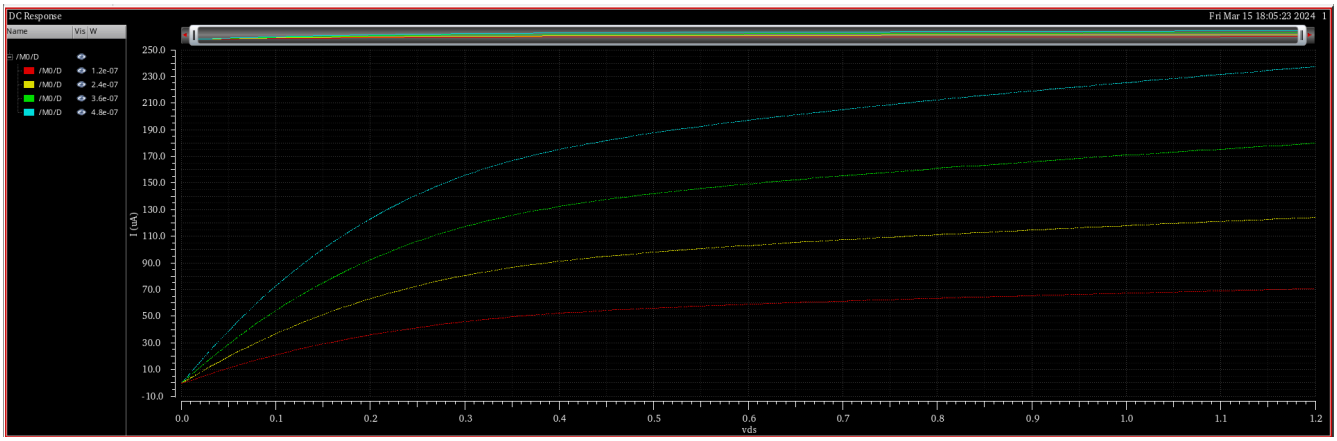
$\Rightarrow V_{DS} > V_{GS} - 0.3$

$\Rightarrow I_{DSsat} = 0.5\, k_n \left(V_{GS} - V_{TH}\right)^2$

If $V_{GS} \uparrow$, $I_{DSSsat} \uparrow$

with $k_n = \mu_n C_{ox} \frac{W}{L}$

- Choose $L = 60nm$, $V_{GS} = 1.0V$ and $V_{SB} = 0V$. Draw curves $I_{DS} = f(V_{DS})$ sweeping variable V_{DS} from 0V to 1.2V with step = 0.01V and $W = \{120, 240, 360, 480\}\ nm$



In triode $V_{DS} < V_{OV}$

$\Rightarrow V_{DS} < 1 - V_{TH}$

and $I_{DS} = k_n\left[(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\right]$

In saturation region $V_{DS} > V_{OV}$

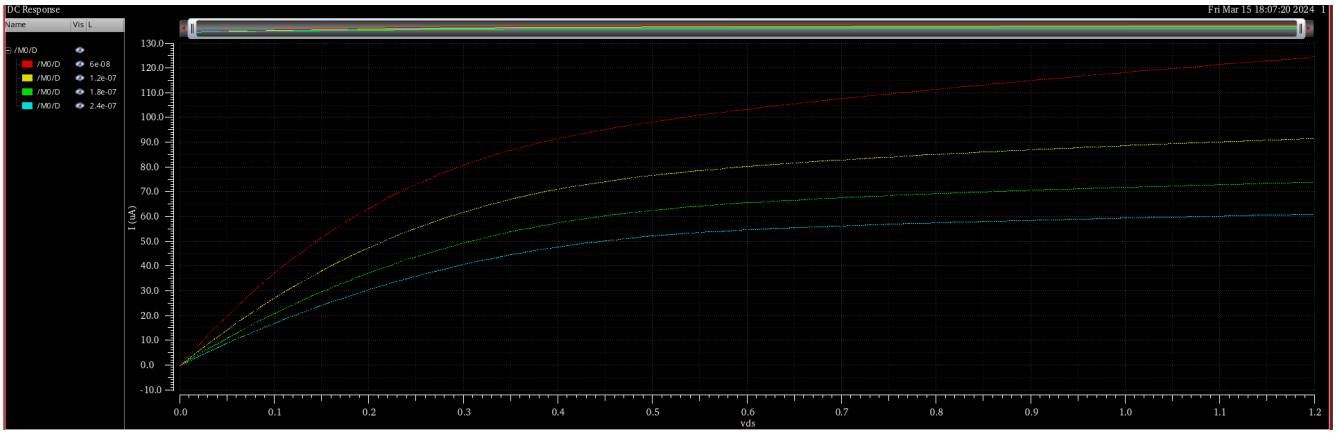
$\Rightarrow V_{DS} > 1 - V_{TH}$

and $I_{DSsat} = 0.5\, k_n\left(V_{GS} - V_{TH}\right)^2$

with $k_n = \mu_n C_{ox} \frac{W}{L}$

If $W \uparrow \Rightarrow I_{DS} \uparrow$

- Choose W = 240nm, V_{GS} = 1.0V and V_{SB} = $0V$. Draw curves $I_{DS} = f(V_{DS})$ sweeping variable V_{DS} from 0V to 1.2V with step = 0.01V and L = {60, 120, 180, 240} nm



In triode $V_{DS} < V_{OV}$

$\Rightarrow V_{DS} < 1 - V_{TH}$

and $I_{DS} = k_n\left[(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\right]$

In saturation region $V_{DS} > V_{OV}$

$\Rightarrow V_{DS} > 1 - V_{TH}$

and $I_{DSsat} = 0.5\, k_n\left(V_{GS} - V_{TH}\right)^2$

with $k_n = \mu_n C_{ox} \frac{W}{L}$

If $L \uparrow \Rightarrow I_{DS} \downarrow$

EXPERIMENT 3

Objective: Known second order effect of MOS transistor in library currently used.

The ideal I-V model neglects many effects that are important to modern device. It is useful to have a qualitative understanding of second order effects to predict their impact on circuit behavior and to be able to anticipate how devices will change in future process generations.

These effects are listed as follows.

No.	Name of second order effect (Nonlinear I-V Effects)	
1	Mobility degradation and Velocity saturation	
2	Channel length modulation	
3	Threshold voltage effect	Body effect
		Drain-Induced Barrier Lowering
		Short Channel Effect
4	Leakage	Subthreshold Leakage
		Gate Leakage
		Junction Leakage
5	Temperature Dependence	
6	Geometry Dependence	

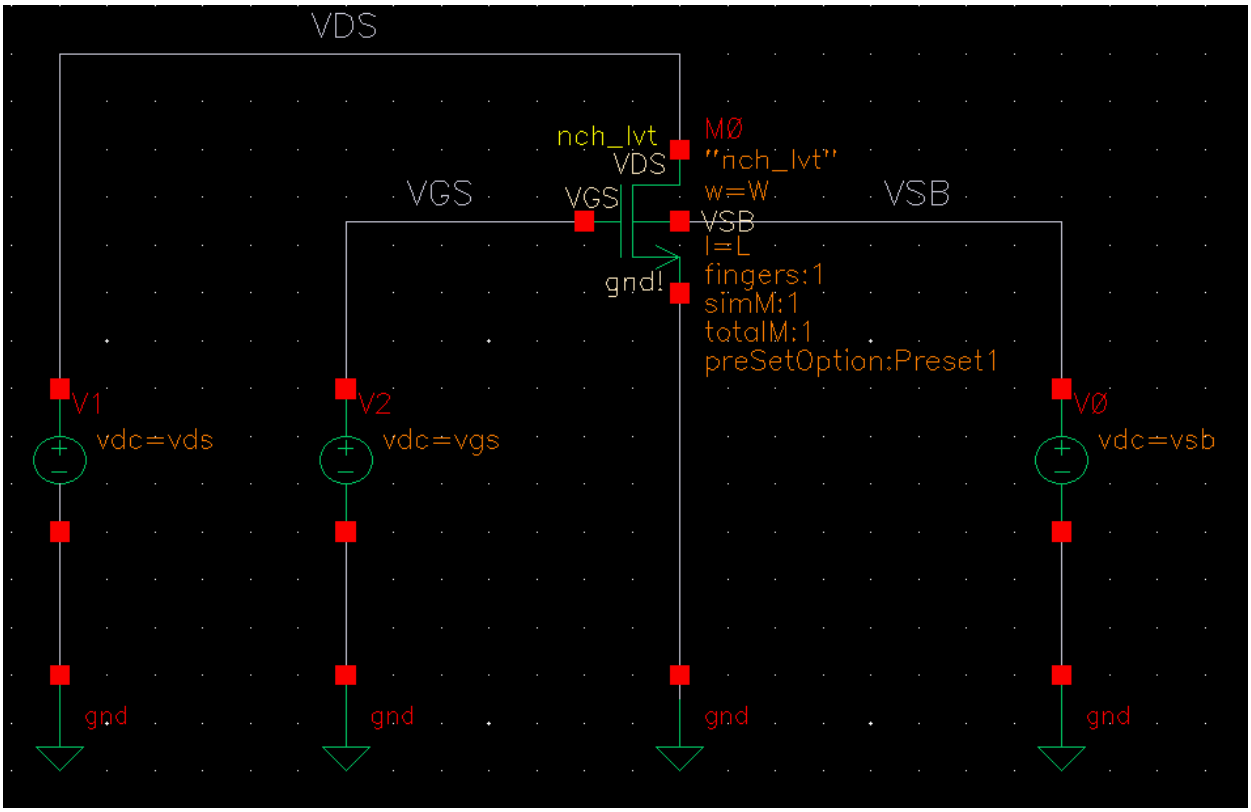
Table 1. Some second-order effects in MOS transistors.

In fact, body effect and channel length modulation are important when analyzing the small signal, and the expression determined I_{DS}. Assemble the testbench circuit as shown in Figure 1. In Experiment 2, we have already considered channel length modulation so in Experiment 3 we investigate the body effect of NMOS only.

Requirements:

Instruction:

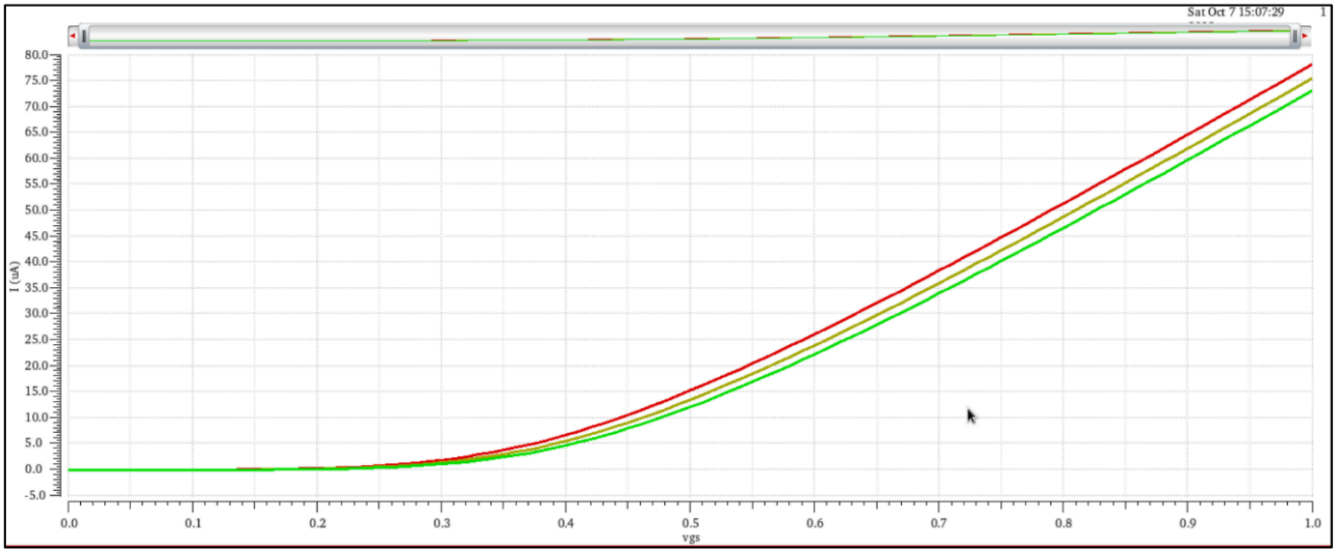
- Setting parameters W, L, V_{GS}, V_{SB} and V_{DS} for convenience when characterizing circuit shown in Figure 1.



- Sweep multiple variables in parallel using ADE-L: ***Tools → Parametric Analysis***

Check: Your report must show the results

- Draw curves $I_{DS} = f(V_{GS})$ when fixing $L = 60nm$, $W = 120nm$, $V_{DS} = 1.2V$, and sweeping V_{GS} from 0V to 1.0V at $V_{SB} = \{0.15,0.30,0.45\}\ V$



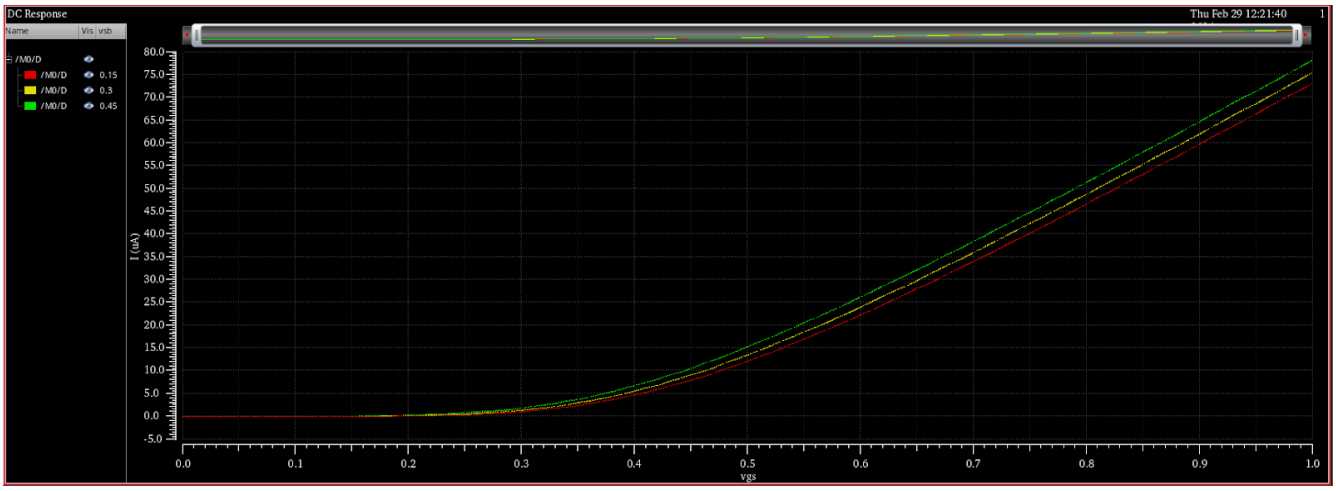


Figure 7. $I_{DS} = f(V_{GS})$ waveform with $V_{SB} = \{0.15, 0.30, 0.45\}\ V$

Questions:

- V_{TH} can also be obtained from Figure 7 or using DCOP report in DC analysis.

In cut off region $I_D \approx 0$ and $V_{GS} < V_{TH}$ until $V_{GS} \approx 0.3\ (V)$

$\Rightarrow V_{TH} \approx 0.3\ (V)$

In triode $V_{DS} < V_{OV}$

$\Rightarrow 1 < V_{GS} - 0.3$

$\Rightarrow V_{GS} > 0.7\ (V)$

$I_D = k_n\left[(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\right]$

In saturation region $V_{DS} > V_{OV}$

$\Rightarrow 0.3 < V_{GS} < 0.7\ (V)$

$I_{Dsat} = 0.5\ k_n\left(V_{GS} - V_{TH}\right)^2$

and if base voltage is given we can use the relationship $V_{GS} = V_{SB} - V_{TH}$

$\Rightarrow V_{SB} \uparrow \Rightarrow V_{GS} \uparrow \Rightarrow I_D \uparrow$

- Explain the body effect based on $I_{DS} = f(V_{GS})$ characteristic and V_{TH} measured in the previous step.

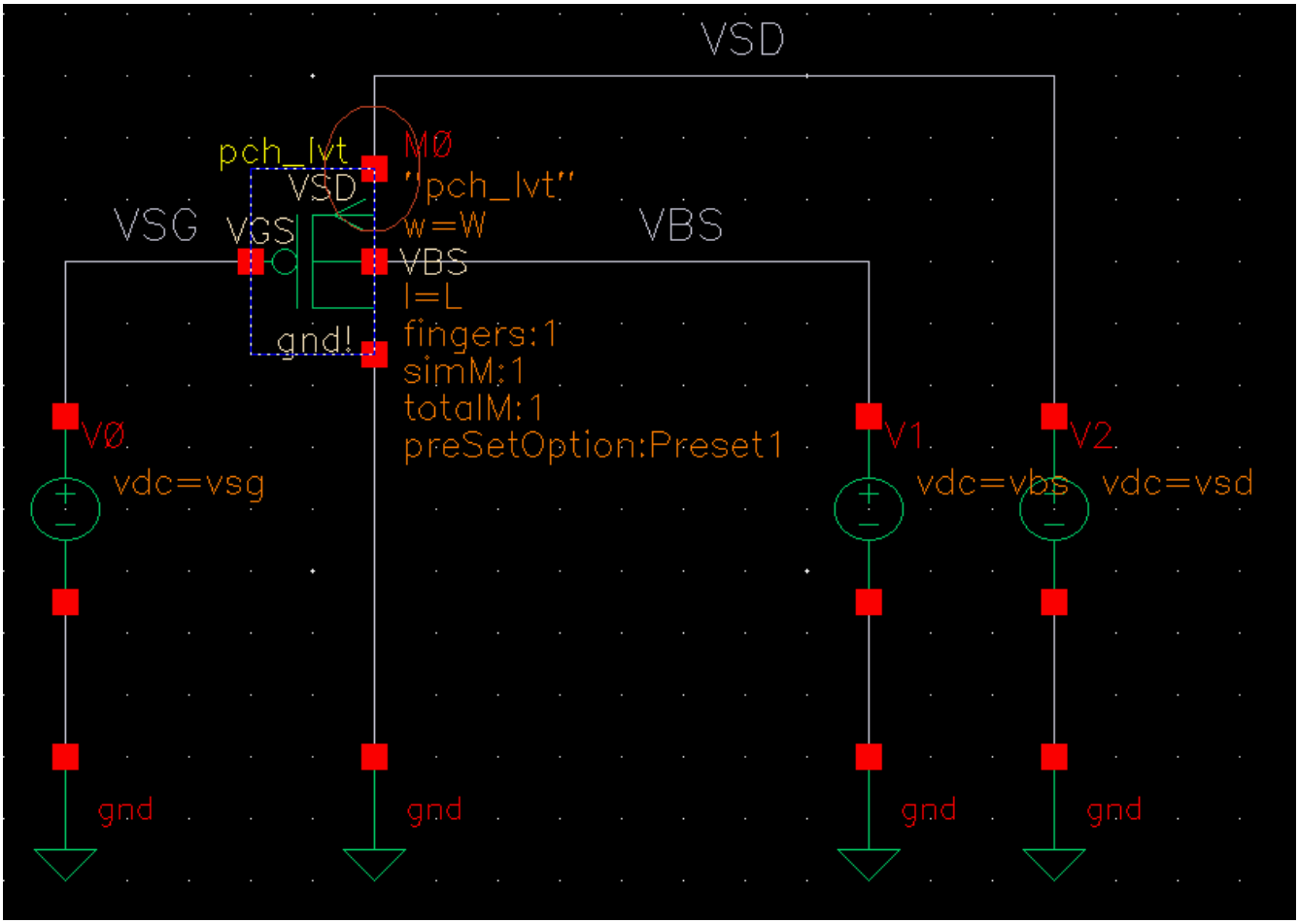
EXPERIMENT 4

Objective: The effects on I/V characteristics of PMOS when V_{SG}, width and length vary.

Requirements: Know how to create a testbench and consider the I/V characteristics of PMOS.

Instruction:

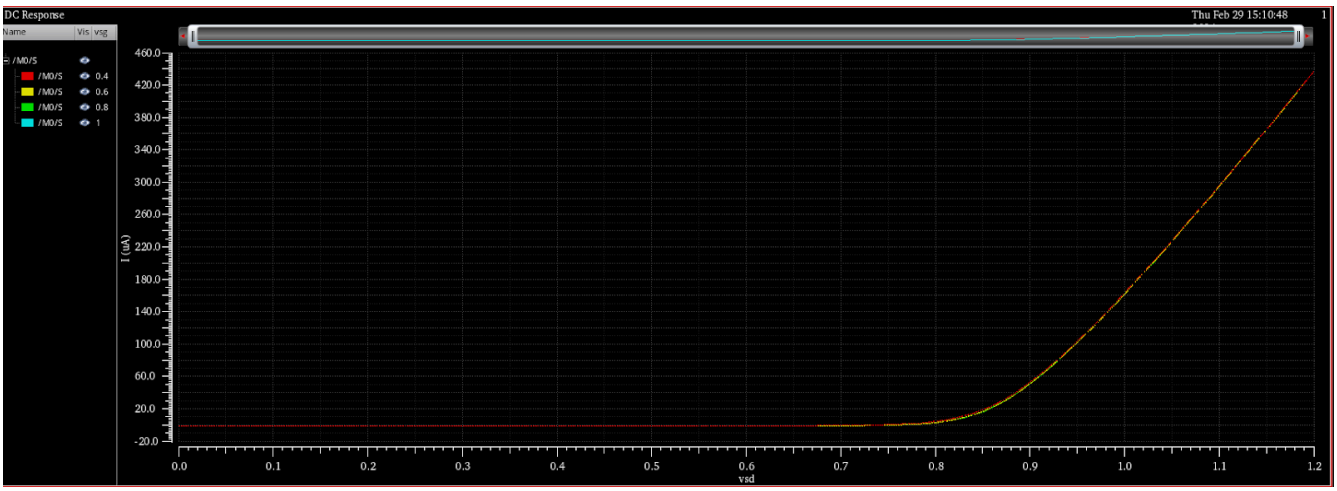
- Based on the NMOS I/V characteristics in ***Figure 1***, you propose a testbench to consider the I/V characteristics of ***PMOS pch_lvt device*** in tsmc65 technology.



Check: Your result must show these results and summarize the conclusion of the current and

operation region of PMOS with the width, length, and V_{SG} variation.

- Choose $L = 60nm$, $W = 120nm$ and $V_{BS} = 0V$. Draw curves $I_{SD} = f(V_{SD})$, sweeping variable V_{SD} from 0V to 1.2V with step = 0.01V and sweeping V_{SG} from 0.4V to 1.0V with step = 0.2V.



In cut off region $I_{SD} \approx 0$ and $V_{SG} \leq |V_{TP}|$ until $V_{SD} \approx 0.8\ (V)$

$\Rightarrow V_{TP} \approx -0.8\ (V); V_{SG} \leq 0.8$

In triode $V_{DS} > V_{SG} - |V_{TP}|$ and $V_{SG} \leq 0.8 \Leftrightarrow V_{DS} > V_{SG} - 0.8$

$I_{SD} = k_n\left[(V_{SG} - |V_{TP}|)V_{SD} - 0.5V_{SD}^2\right]$

$\Rightarrow V_{SD} \uparrow \quad \Rightarrow I_{SD} \uparrow$

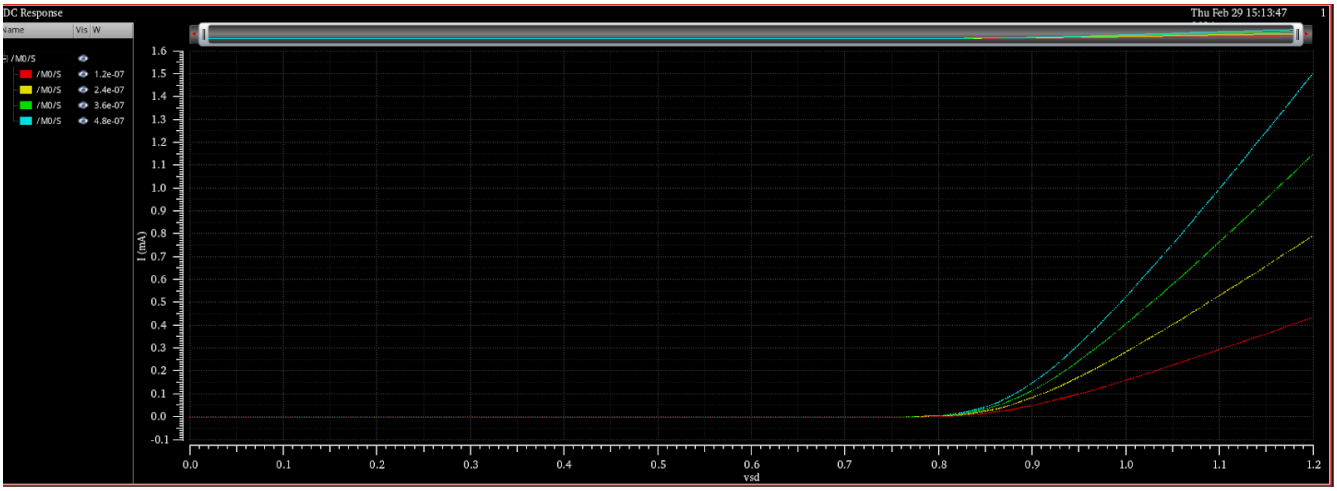
In saturation region $V_{DS} \leq V_{OV}$

$I_{SDsat} = 0.5\, k_n \left(V_{SG} - |V_{TP}|\right)^2$

$\Rightarrow V_{SD} \uparrow \quad \Rightarrow I_{SDsat}$ unchanged

In summary, in some cases, increasing V_{SD} in a PMOS transistor may not significantly change I_{SDsat} especially when the transistor is operating deep in saturation and the effect of channel-length modulation is minimal.

- Choose $L = 60nm$, $V_{SG} = 1.0V$ and $V_{BS} = 0V$. Draw curves $I_{SD} = f(V_{SD})$ sweeping variable V_{SD} from 0V to 1.2V with step = 0.01V and $W = \{120, 240, 360, 480\}\ nm$



In cut off region $I_{SD} \approx 0$ and $V_{SG} \leq |V_{TP}|$ until $V_{SD} \approx 0.8\ (V)$

$\Rightarrow V_{TP} \approx -0.8\ (V); V_{SG} \leq 0.8$

In triode $V_{DS} > V_{SG} - |V_{TP}|$ and $V_{SG} \leq 0.8 \Leftrightarrow V_{DS} > V_{SG} - 0.8$

$$I_{SD} = k_n\left[(V_{SG} - |V_{TP}|)V_{SD} - 0.5V_{SD}^2\right]$$

In saturation region $V_{DS} \leq V_{OV}$

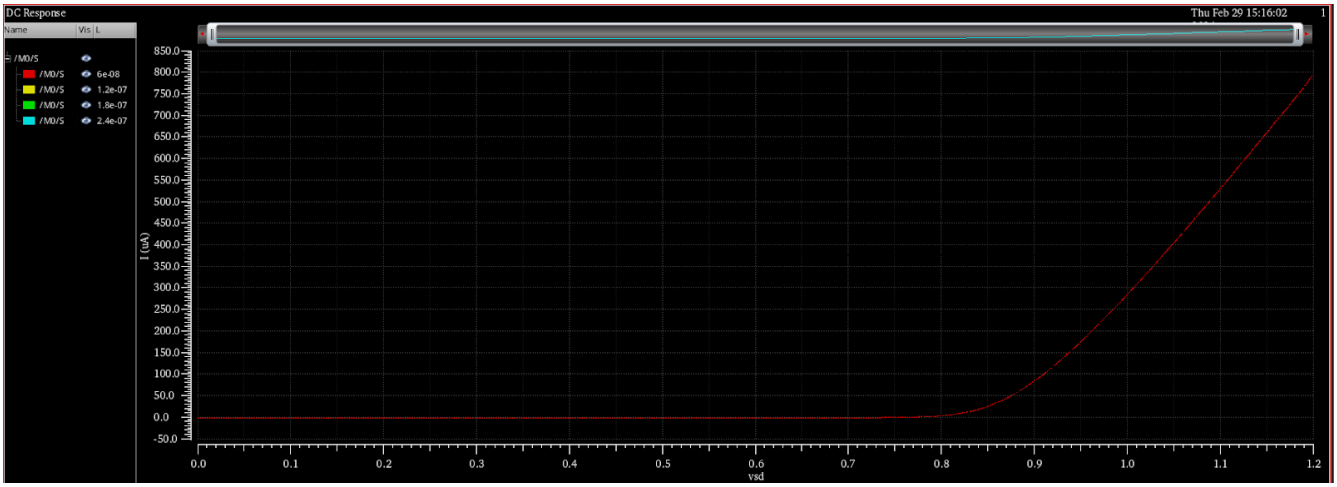
$$I_{SDsat} = 0.5\, k_n \left(V_{SG} - |V_{TP}|\right)^2$$

with

$$k_n = \mu_n C_{ox} \frac{W}{L}$$

If $W \uparrow \Rightarrow I_{SD} \uparrow$

- Choose W = 240nm, V_{SG} = 1.0V and V_{BS} = $0V$. Draw curves $I_{SD} = f(V_{SD})$ sweeping variable V_{SD} from 0V to 1.2V with step = 0.01V and L = {60, 120, 180, 240} nm



In cut off region $I_{SD} \approx 0$ and $V_{SG} \leq |V_{TP}|$ until $V_{SD} \approx 0.8\ (V)$

$\Rightarrow V_{TP} \approx -0.8\ (V); V_{SG} \leq 0.8$

In triode $V_{DS} > V_{SG} - |V_{TP}|$ and $V_{SG} \leq 0.8 \Leftrightarrow V_{DS} > V_{SG} - 0.8$

$$I_{SD} = k_n\left[(V_{SG} - |V_{TP}|)V_{SD} - 0.5V_{SD}^2\right]$$

In saturation region $V_{DS} \leq V_{OV}$

$$I_{SDsat} = 0.5\, k_n \left(V_{SG} - |V_{TP}|\right)^2$$

with

$$k_n = \mu_n C_{ox} \frac{W}{L}$$

If $L \uparrow \Rightarrow I_{SD} \downarrow$

However, V_{SG} or V_{TP}increase, it can offset the decrease in $\frac{W}{L}$

Overall, in certain cases, increasing in L a PMOS transistor might not lead to a significant change in I_{DS}, especially if other parameters are adjusted to compensate for the change in L