LABORATORY 3

CMOS INVERTER ANALYSIS WITH ADE-XL

OBJECTIVES

No.	Objectives	Requirements
1	Knowing how to setup ADE-XL simulation environment	▪ Find the trip-point of the inverter with ADE-XL simulation
2	Understand the calculator functions working	▪ Using calculator functions to measure some parameters of the inverter with transient analysis

PREPARATION FOR LAB 3

- Reading **Appendix 1** and **Appendix 2** about ADE-XL setting and using Calculator to measure the performance parameters of design.

LAB 3 INFORMATION

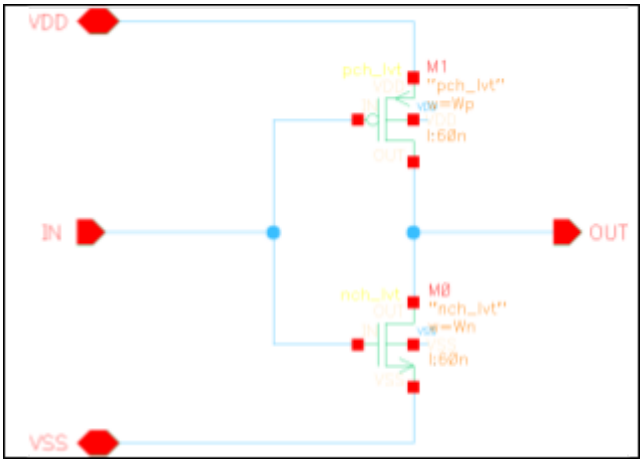
- Consider ***NMOS nch_lvt device, PMOS pch_lvt device*** and power supply ***vdd*** = **1**. **2*V***

EXPERIMENT 1

Objective: Build a testbench to measure the trip-point of the inverter. Setup and simulate design with ADE-XL environment.

Requirements: Simulate with dc analysis with ADE-XL environment.

Instruction: Assemble the circuit as shown in ***Figure 1*** and ***Figure 2***, setting parameters for power supplies (using ***vdc*** source), with $L_n = L_p = 60nm$, $C_{load} = 10fF$, $vdd = 1.2V$



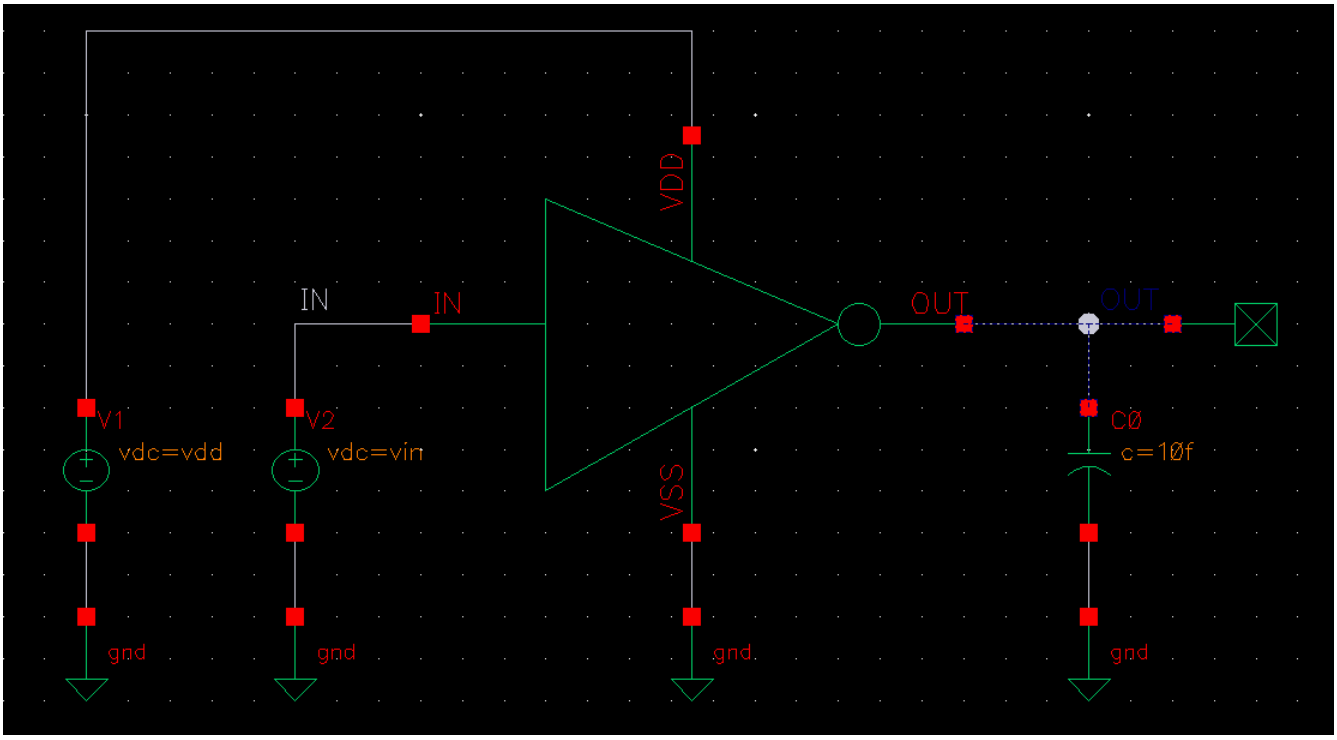
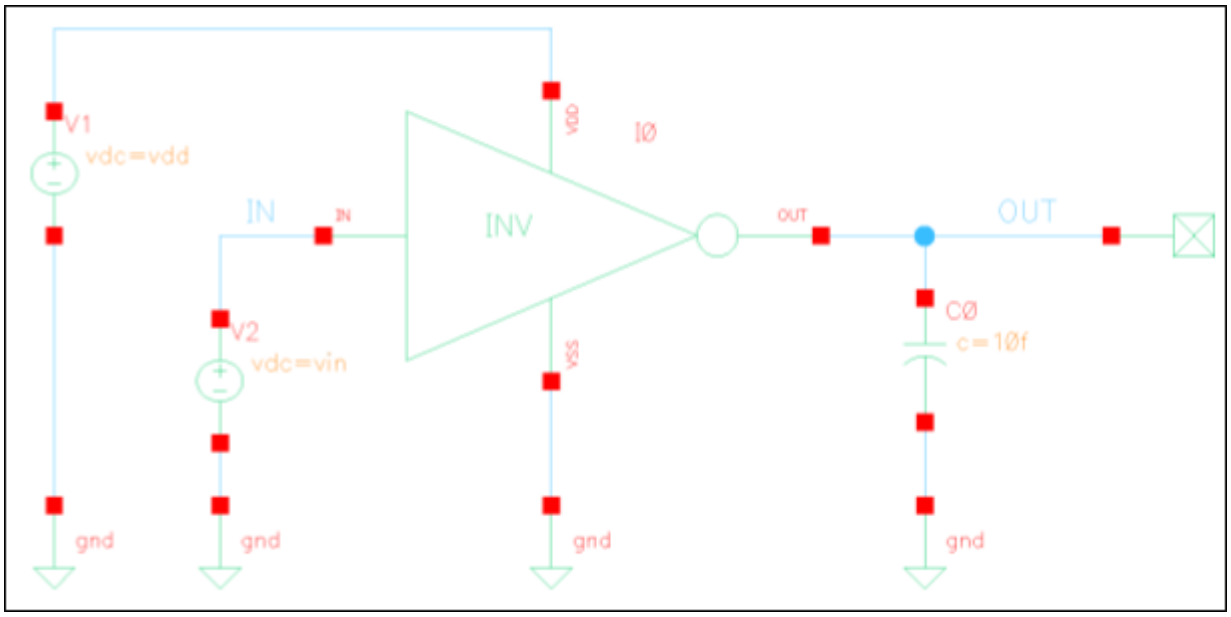


Figure 1. Schematic of INV



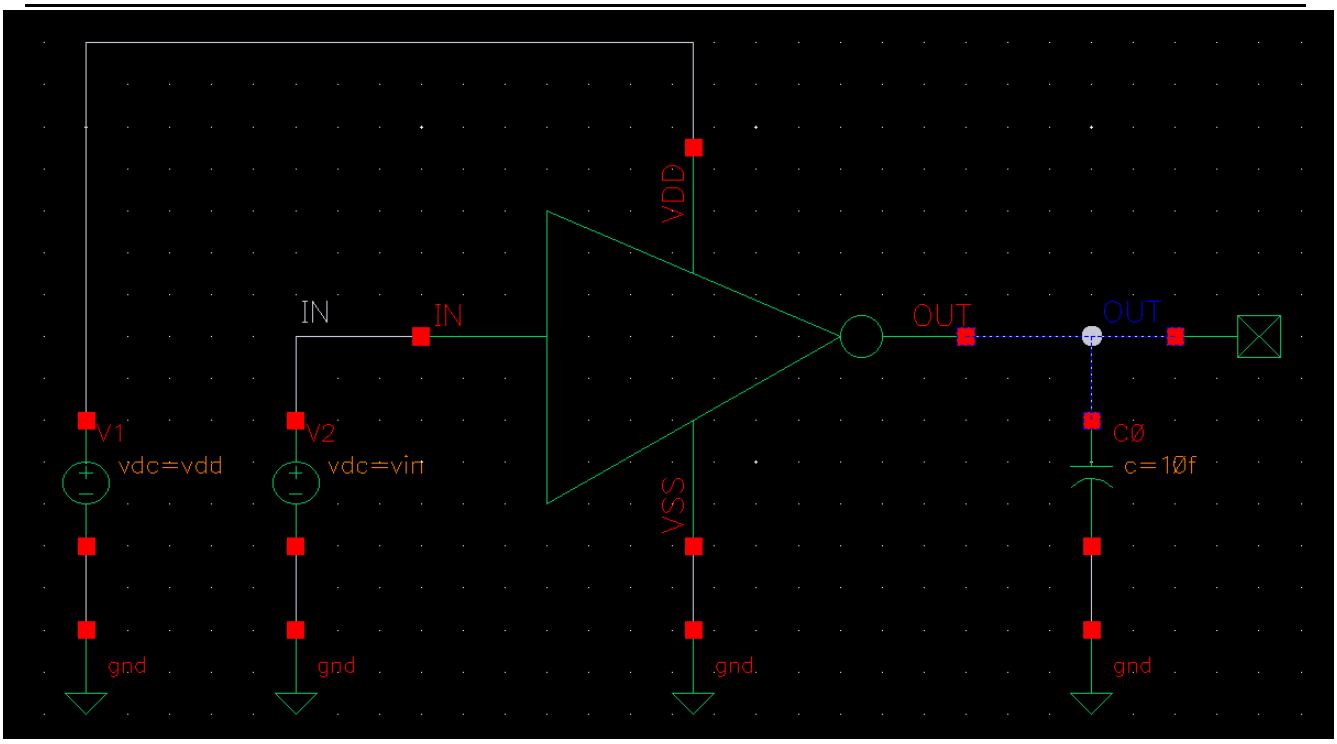


Figure 2. Testbench dc analysis of INV

Check:

- Trip point defines the input voltage that the output changes the state (from 0 to 1 / from 1 to 0).
- In switching state working, the inverter needs to balance between the rising and falling edge of the inverter to ensure stability. So, we need to find the P/N ratio size of PMOS and NMOS (W_N and W_P) to get the balanced state (or balance trip point).

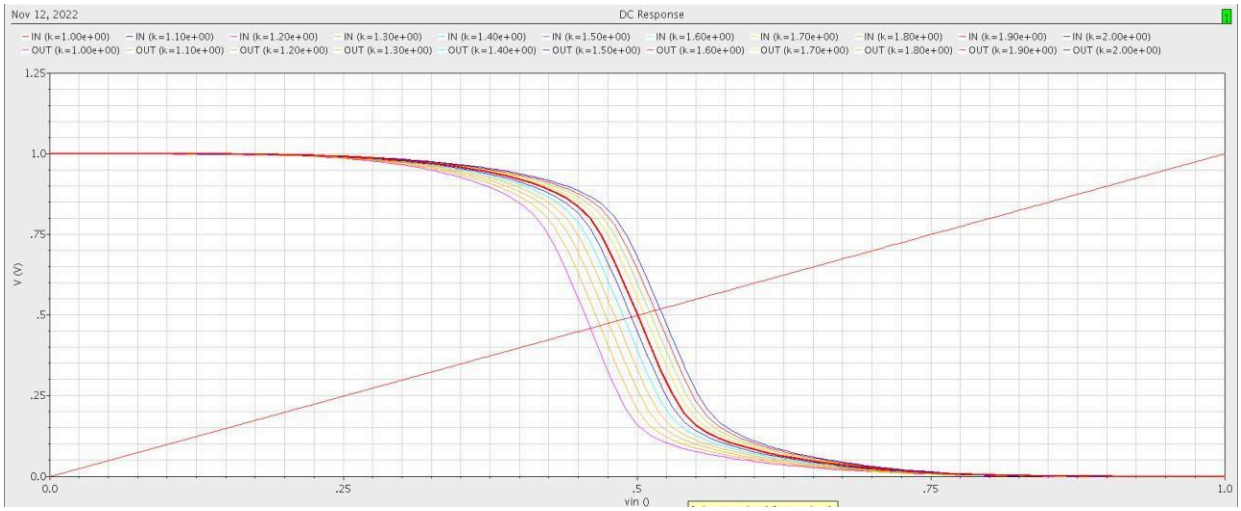
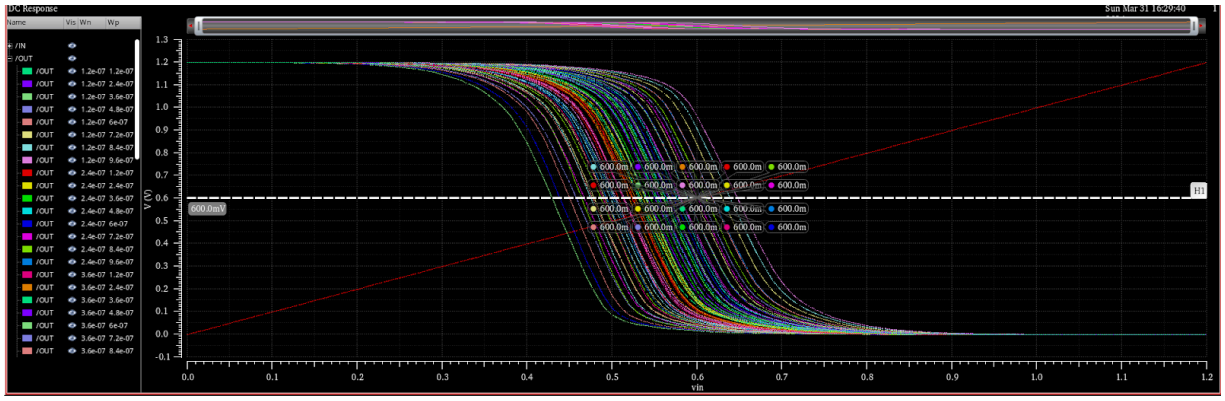
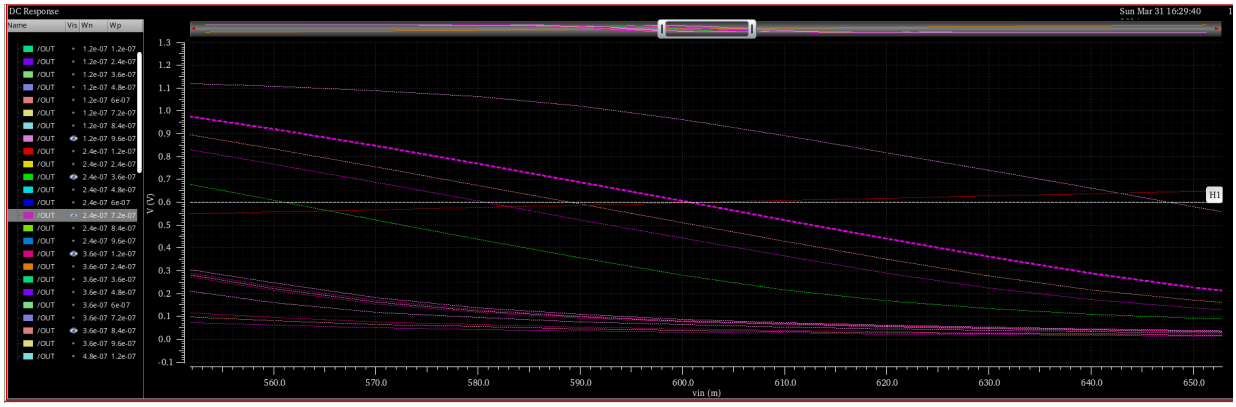


Figure 3. Example waveform finding the balance trip-point



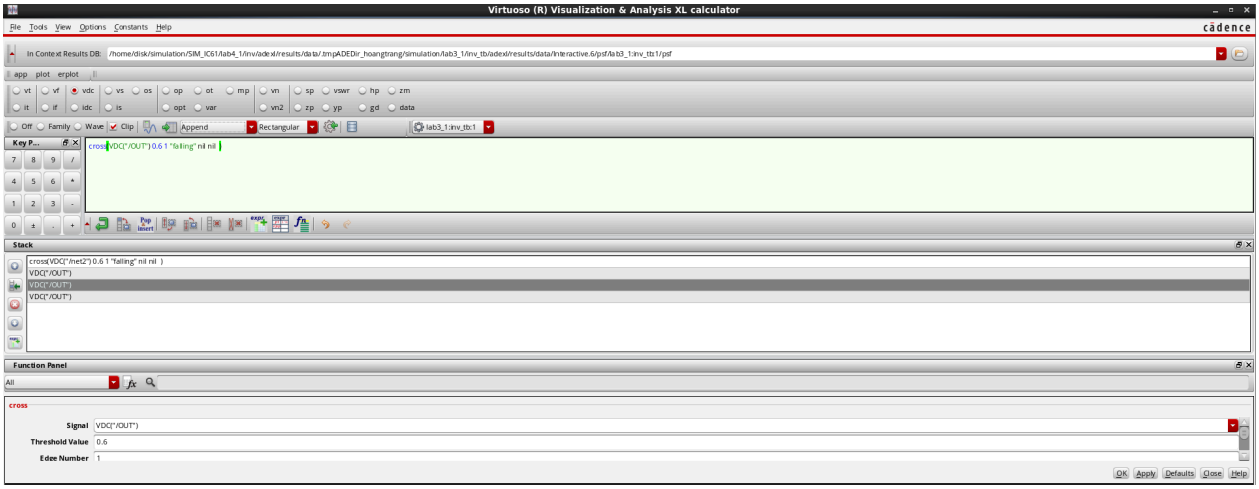


$W_n = 2.4 * 10^{-7}\ W_p = 7.2 * 10^{-7}$

or

$W_n = 240nm\ , W_p = 720nm$

- Writing a calculator function to measure the trip-point.



$tp = 600.6m$

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EXPERIMENT 2

Objective: Consider the variation of trip point with the changing of PVT

Requirements: Simulate dc analysis with ADE-XL enviroment.

Instruction: Assemble the circuit as shown in ***Figure 2***, setting parameters for power supplies (using ***vdc*** source), with $L_n = L_p = 60nm$, $C_{load} = 10fF$, $vdd = 1.2V$, $\boldsymbol{W_N}$, $\boldsymbol{W_P}$ **in Experiment 1.**

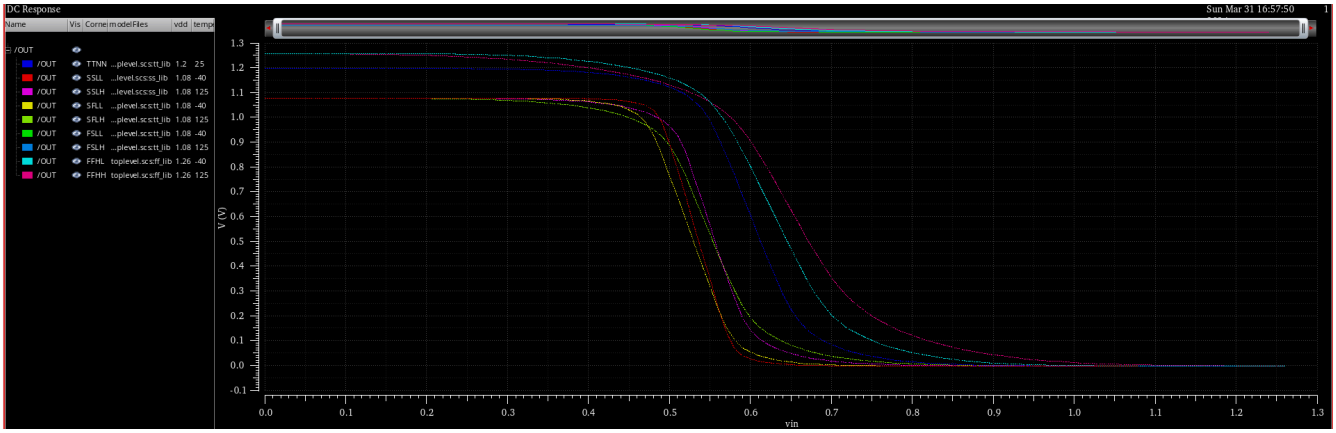
Check:

Check:

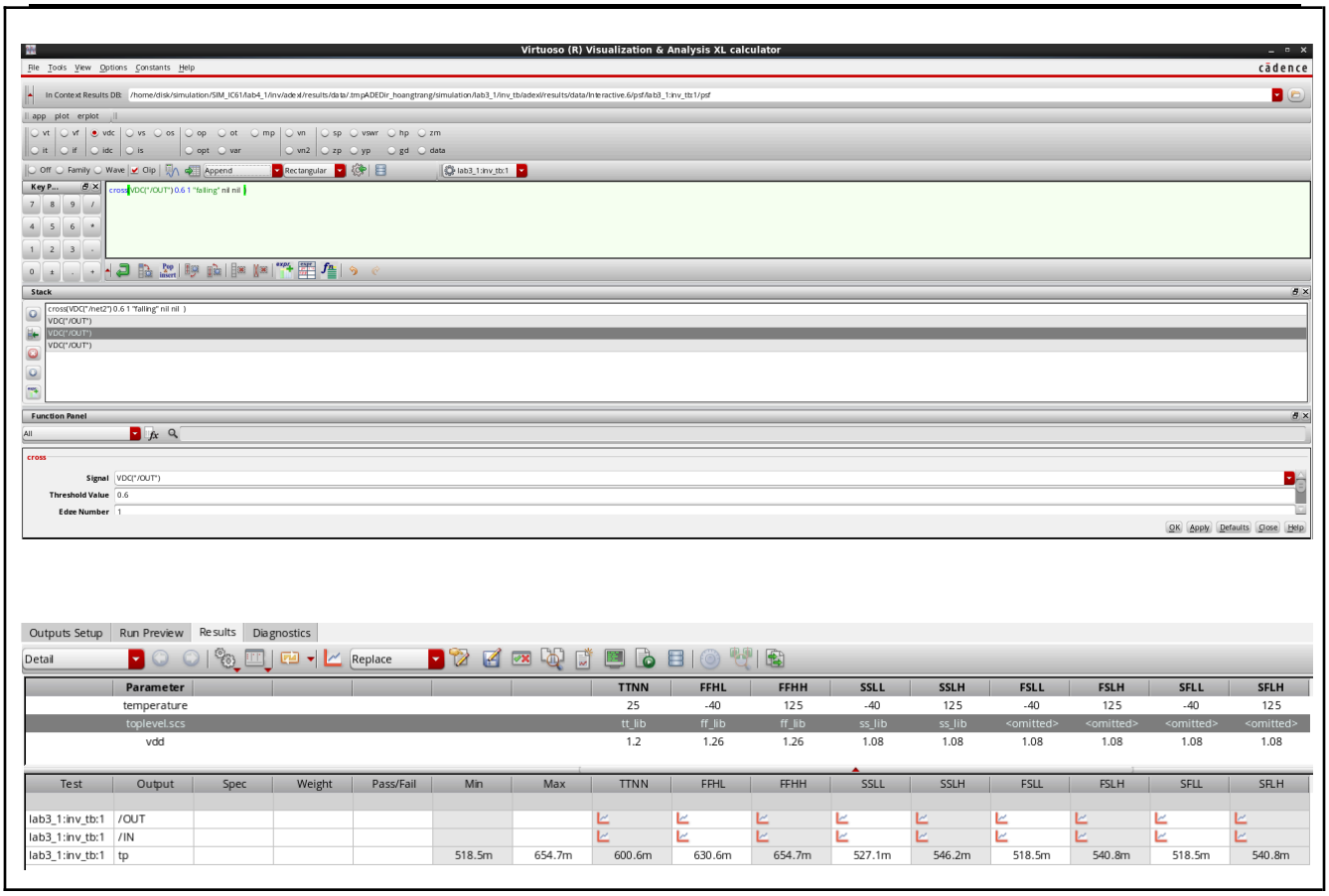
- Setup testbench with 9 PVT corners in ***Table 1*** with ADE-XL.

	TTNN	FFHL	FFHH	SSLL	SSLH	FSLL	FSLH	SFLL	SFLH
vdd	1.2	1.26	1.26	1.08	1.08	1.08	1.08	1.08	1.08
Temp	25	-40	125	-40	125	-40	125	-40	125

Table 1. PVT corner definition



- Evaluate the variation of trip-point with the vary of process, voltage and temperature.



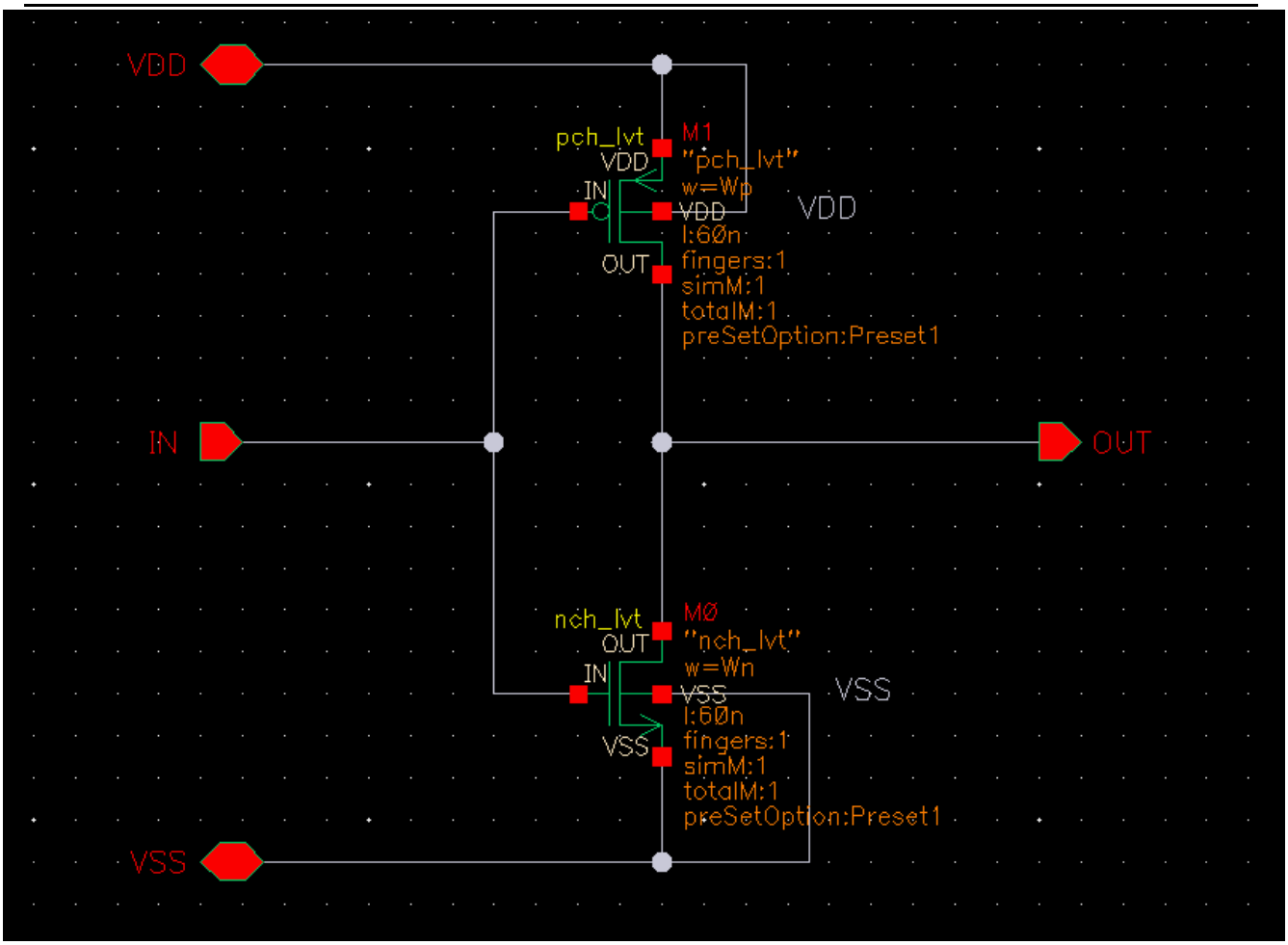
EXPERIMENT 3

Objective: Using the Calculator function to measure the performance of the inverter.

Requirements: Simulate tran analysis with ADE-XL environment.

Instruction:

- Assemble the circuit as shown in ***Figure 5***, setting parameters for power supplies (using ***vpulse*** source), with $L_n = L_p = 60nm$, $C_{load} = 10fF$, $vdd = 1.2V$ $\boldsymbol{W_N}$, $\boldsymbol{W_P}$ **in Experiment 1.**
- Set the variable for vpulse source parameter (voltage 1, voltage 2, period, rise time, fall time, pulse width) in ***Figure 6***.



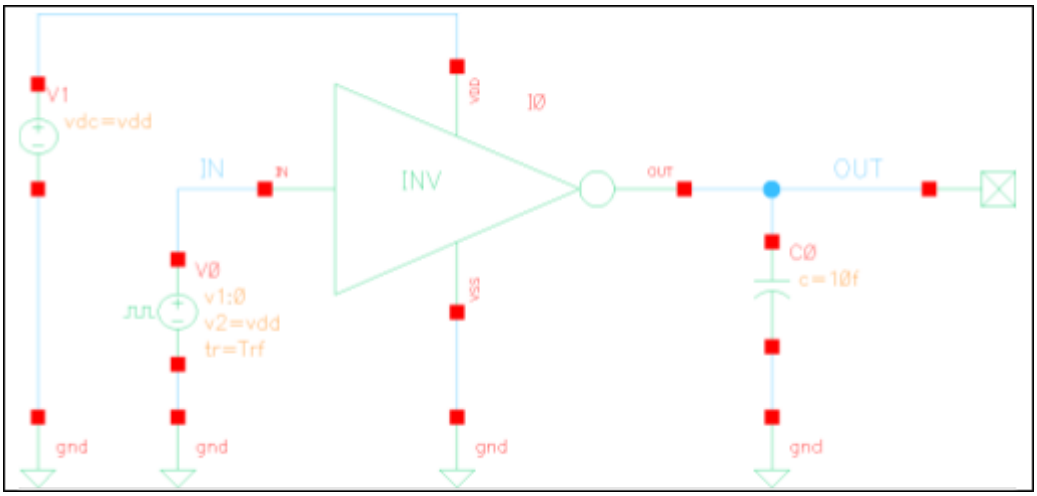


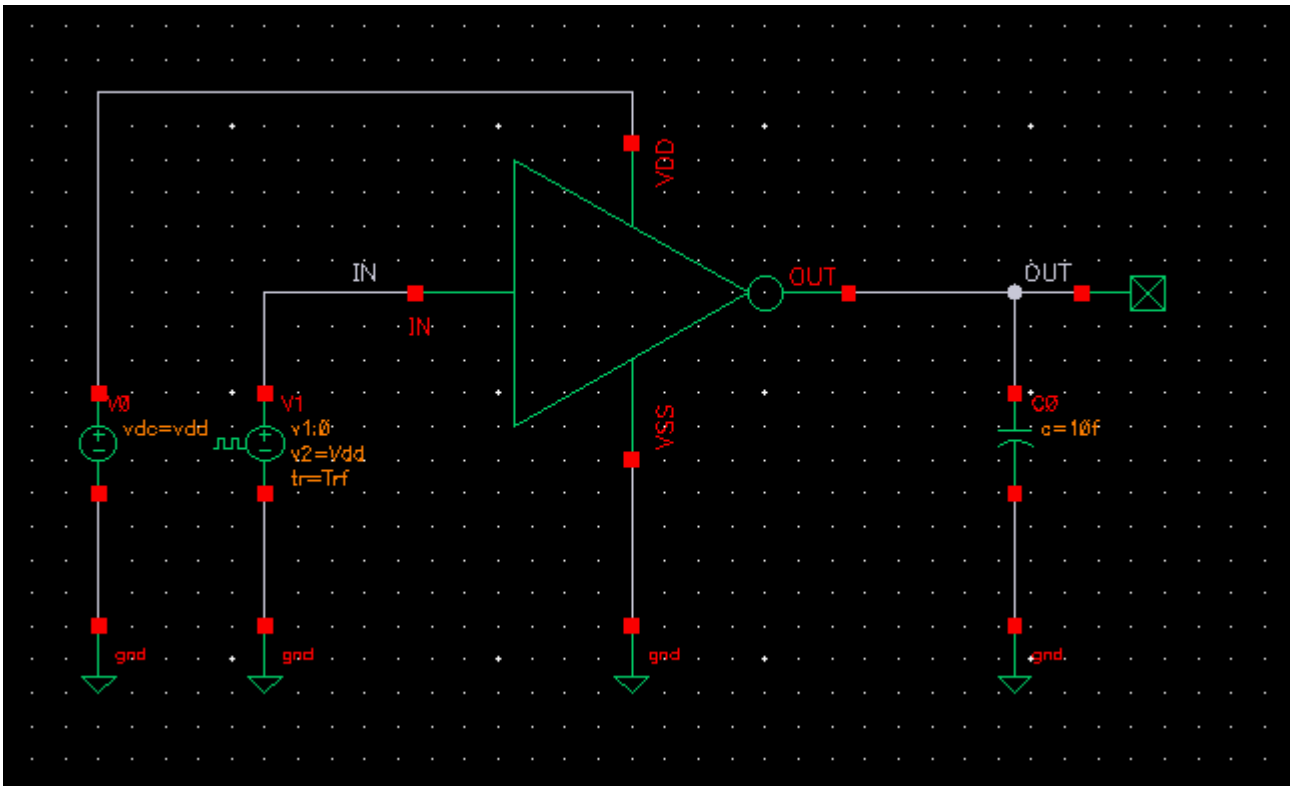
Figure 5. Testbench tran analysis of INV

Voltage 1	0 V
Voltage 2	Vdd V
Period	1/f s
Delay time	Td s
Rise time	Trf s
Fall time	Trf s
Pulse width	Pw s

Figure 6. Testbench tran analysis of INV

- Define the value of variable in the ADE-XL variable setting

$F = 10kHz,\ Td = 1ns,\ Trf = \frac{1}{10F},\ Pulse\_width = \frac{1}{2F} - Trf$



Check:

- Plot Input, Output and current at VDD pin of inverter as shown in **Figure 7** to check the function of inverter.

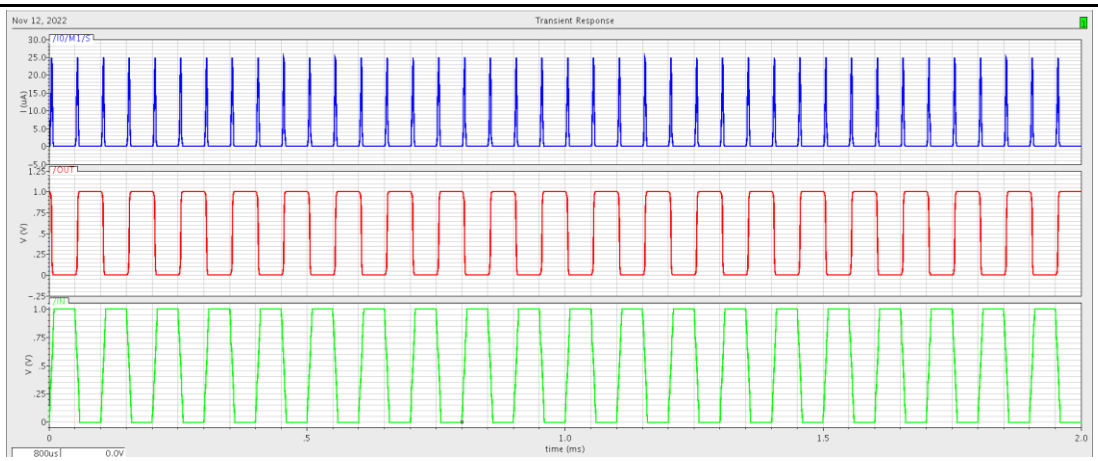
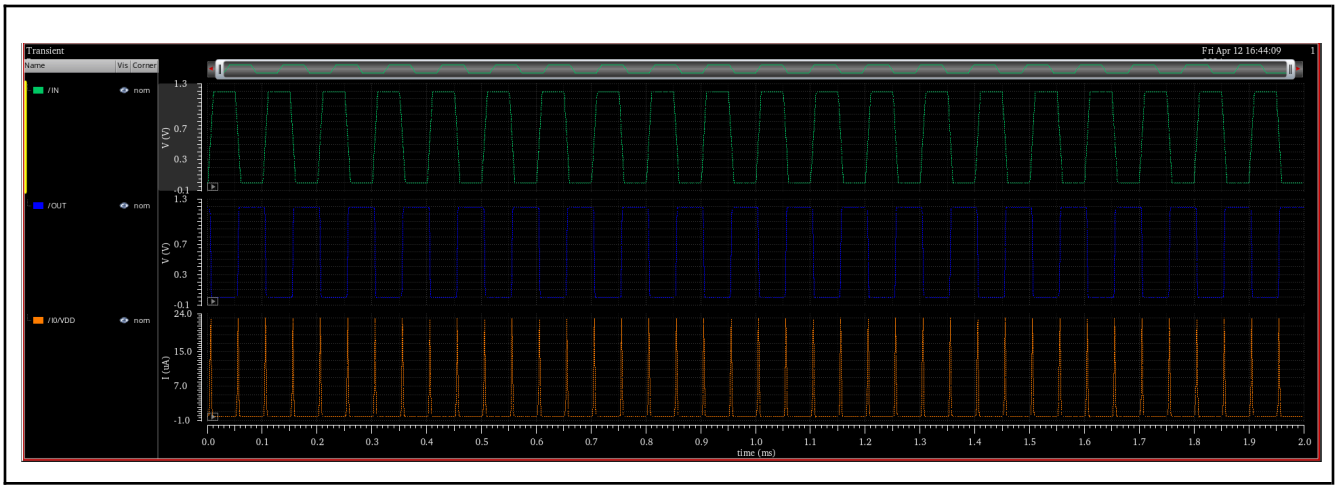


Figure 7. Result waveform of inverter simulation with transient analysis



Create the calculator function to measure rising time, falling time, duty cycle, delay from input to output, and current of inverter in **Table 2** with the guideline in **Figure 8**.

Name	Type	Expression/Signal/File
	signal	/Vin
	signal	/Vout
	signal	/M1/S
t_rise_avg	expr	riseTime(VT("/Vout") 0 nil VAR("Vdd") nil 10 90 nil "time")
t_fall_avg	expr	fallTime(VT("/Vout") VAR("Vdd") nil 0 nil 10 90 nil "time")
T_D_low	expr	(delay(VT("/Vout") (VAR("Vdd") / 2) 4 "falling" VT("/Vout") (VAR("Vdd") / 2) 4 "rising" 0 0 nil nil ?td1 0.0 ?td2 0.0 ?td2r0 nil ?stop nil) * VAR("f"))
T_D_high	expr	(delay(VT("/Vout") (VAR("Vdd") / 2) 5 "rising" VT("/Vout") (VAR("Vdd") / 2) 6 "falling" 0 0 nil nil ?td1 0.0 ?td2 0.0 ?td2r0 nil ?stop nil) * VAR("f"))
t_rise	expr	delay(VT("/Vout") (0.1 * VAR("Vdd")) 5 "rising" VT("/Vout") (0.9 * VAR("Vdd")) 5 "rising" 0 0 nil nil ?td1 0.0 ?td2 0.0 ?td2r0 nil ?stop nil)
t_fall	expr	delay(VT("/Vout") (0.9 * VAR("Vdd")) 5 "falling" VT("/Vout") (0.1 * VAR("Vdd")) 5 "falling" 0 0 nil nil ?td1 0.0 ?td2 0.0 ?td2r0 nil ?stop nil)

Figure 8. Guideline to configure the parameters for measurement functions

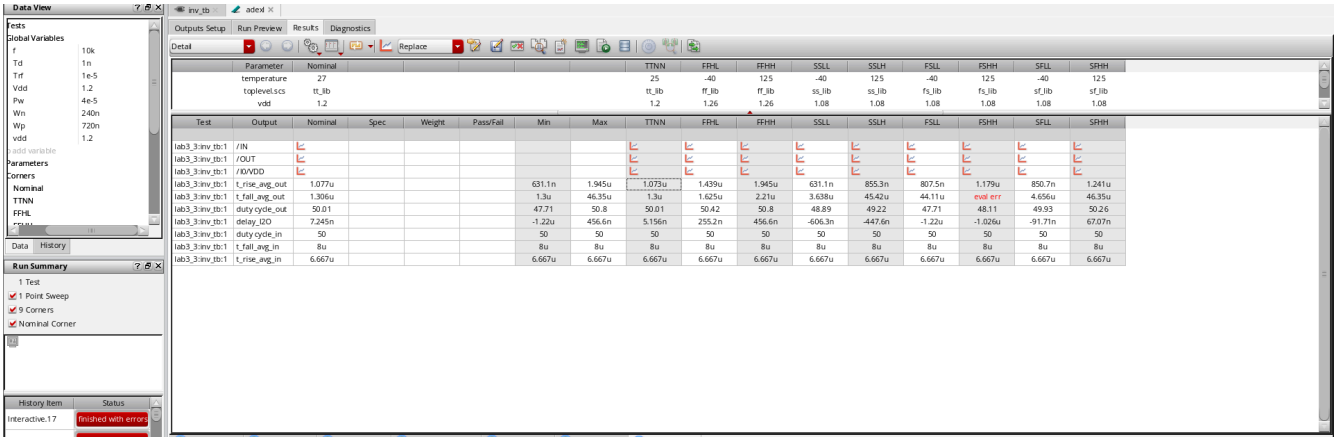
Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
lab3_3:inv_tb:1		signal	/I0/VDD	point	☑	☑						
lab3_3:inv_tb:1		signal	/IN	point	☑	☐						
lab3_3:inv_tb:1		signal	/OUT	point	☑	☐						
lab3_3:inv_tb:1	delay_I2O	expr	delay(?wf1 VT("/IN") ?value1 (VAR("Vdd") / 2) ?edge1 "rising" ?nth1 1 ?td1 0 ?wf2 VT("/OUT") ?value2 (VAR("Vdd") / 2) ?edge2 "falling"...	point	☑	☐						
lab3_3:inv_tb:1	duty cycle_out	expr	dutyCycle(VT("/OUT") ?mode "auto" ?threshold 0.0 ?xName "time" ?outputType "average")	point	☑	☐						
lab3_3:inv_tb:1	t_fall_avg_out	expr	fallTime(VT("/OUT") VAR("Vdd") nil 0 nil 10 90 nil "time")	point	☑	☐						
lab3_3:inv_tb:1	t_rise_avg_out	expr	riseTime(VT("/OUT") 0 nil 1 nil 10 90 nil "time")	point	☑	☐						
lab3_3:inv_tb:1	duty cycle_in	expr	dutyCycle(VT("/IN") ?mode "auto" ?threshold 0.0 ?xName "time" ?outputType "average")	point	☑	☐						
lab3_3:inv_tb:1	t_fall_avg_in	expr	fallTime(VT("/IN") VAR("Vdd") nil 0 nil 10 90 nil "time")	point	☑	☐						
lab3_3:inv_tb:1	t_rise_avg_in	expr	riseTime(VT("/IN") 0 nil 1 nil 10 90 nil "time")	point	☑	☐						

- Setup testbench with 9 PVT corners in ***Table 1.*** Explain the result with the PVT variation.

Parameter			TTNN	FFHL	FFHH	SSLL	SSLH	FSLL	FSHH	SFLL	SFHH
temperature			25	-40	125	-40	125	-40	125	-40	125
toplevel.scs			tt_lib	ff_lib	ff_lib	ss_lib	ss_lib	fs_lib	fs_lib	sf_lib	sf_lib
vdd			1.2	1.26	1.26	1.08	1.08	1.08	1.08	1.08	1.08

Output	Min	Max	TTNN	FFHL	FFHH	SSLL	SSLH	FSLL	FSHH	SFLL	SFHH
/OUT											
/IN											
/IO/VDD											
t_rise_avg	760.5n	2.384u	1.304u	1.725u	2.384u	760.5n	1.06u	979.7n	1.54u	1.014u	1.519u
t_fall_avg	774.8n	2.408u	1.302u	1.727u	2.408u	774.8n	1.101u	995.3n	1.537u	1.015u	1.528u
T_rise	776.7n	2.383u	1.304u	1.727u	2.383u	776.7n	1.055u	970.3n	1.538u	1.027u	1.519u
T_fall	760.6n	2.368u	1.305u	1.73u	2.368u	760.6n	1.074u	986.3n	1.53u	1.026u	1.535u

Figure 9. Example result of measurement parameter with transient analysis



Rising Time: the time taken for the output voltage of the inverter to transition from a low state to a high state in response to a change at the input. It typically measures the time it takes for the output to rise from 10% to 90% of its final value when the input changes.

Falling Time: Falling time is the time taken for the output voltage to transition from a high state to a low state in response to a change at the input. Similar to rising time, it measures the time it takes for the output to fall from 90% to 10% of its final value when the input changes.

Delay from Input to Output: This is the time delay experienced by a signal as it propagates from the input to the output of the inverter. It's the sum of rising time and falling time.

Current of the Inverter (MOSFET): The current in the inverter circuit depends on various factors including the supply voltage, load connected to the output, transistor characteristics, and input signal. In MOSFET-based inverters, the current flow mainly occurs during the transition periods (while the transistors are switching) and is primarily determined by the capacitance of the transistors and the load connected to the output.

- Annotate some measurement parameters

Item	Detail
T_rise_avg	Rising time from low voltage to high voltage (10%-90%) measured by risetime function
T_fall_avg	Falling time from high voltage to low voltage (90%-10%) measured by falltime function
DT_H	Duty cycle of high voltage measuring by delay function
DT_L	Duty cycle of low voltage measuring by delay function
Td_R2F	Delay from rising input to falling output measured by delay function
Td_F2R	Delay from rising input to falling output measured by delay function
T_rise	Rising time from low voltage to high voltage (10%-90%) measured by delay function
T_fall	Falling time from high voltage to low voltage (90%-10%) measured by delay function
I_static_0	Static current with low voltage input
I_static_1	Static current with high voltage input
I_dynamic	The average dynamic current of the inverter

Table 2. Parameter of inverter performance explanation