LABORATORY 2

COMMON SOURCE SINGLE STAGE AMPLIFIER

OBJECTIVES

No.	Objectives	Requirements
1	Knowing use dc, ac and transient analysis in Cadence virtuoso tool	▪ Using DC characteristic curve to determine the operation point for MOS device having the large gain. ▪ Determine gain, phase margin and bandwidth of amplifier using ac analysis
2	Knowing the advances and disadvances of resistor load, current load, and diode-connected load	▪ Explain the advances and disadvances of each topology based on waveform from dc, ac and transient analysis.

LAB 2 INFORMATION

- Consider ***NMOS nch_lvt device, PMOS pch_lvt device*** and power supply ***vdd*** = **1**. **2*V***

EXPERIMENT 1

Objective: Consider a common source single amplifier with resistor load topology.

Requirements: Simulate dc, ac and transient analysis.

Instruction: Assemble the circuit as shown in ***Figure 1***, setting parameters for power supplies (using ***vdc*** source), with $L_n = 60nm$, $W_n = 240nm$, $vdd = 1.2V$

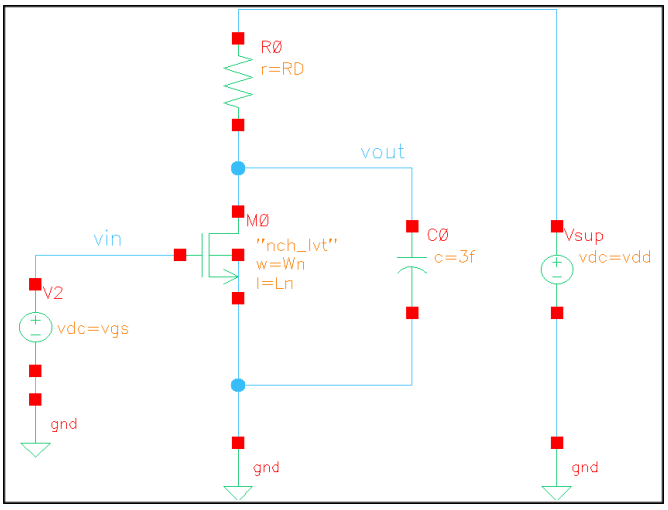
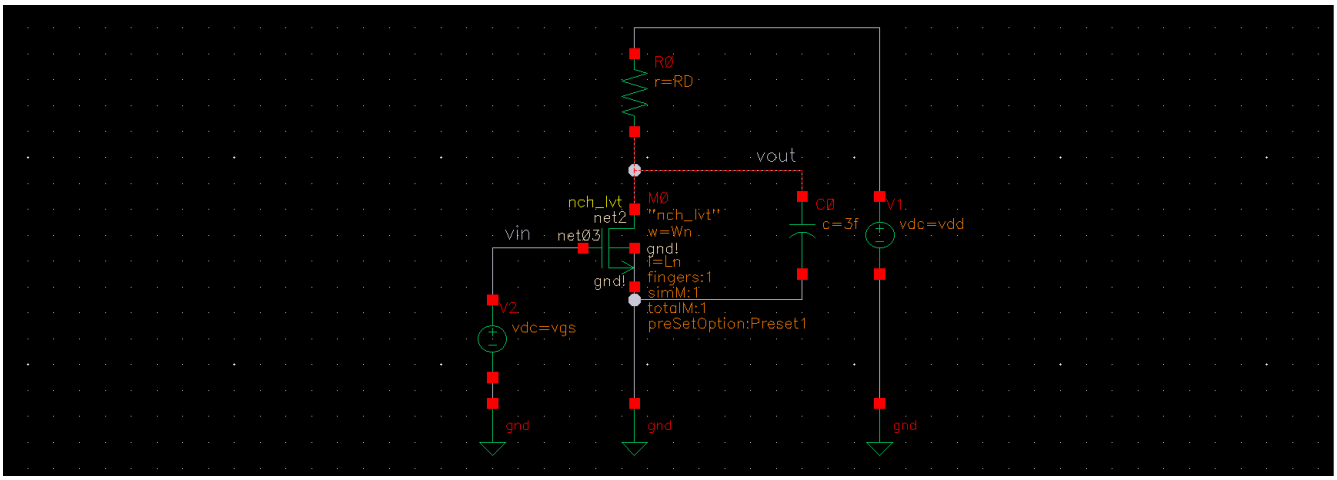


Figure 1. Common source stage with resistor load topology for DC and AC analysis

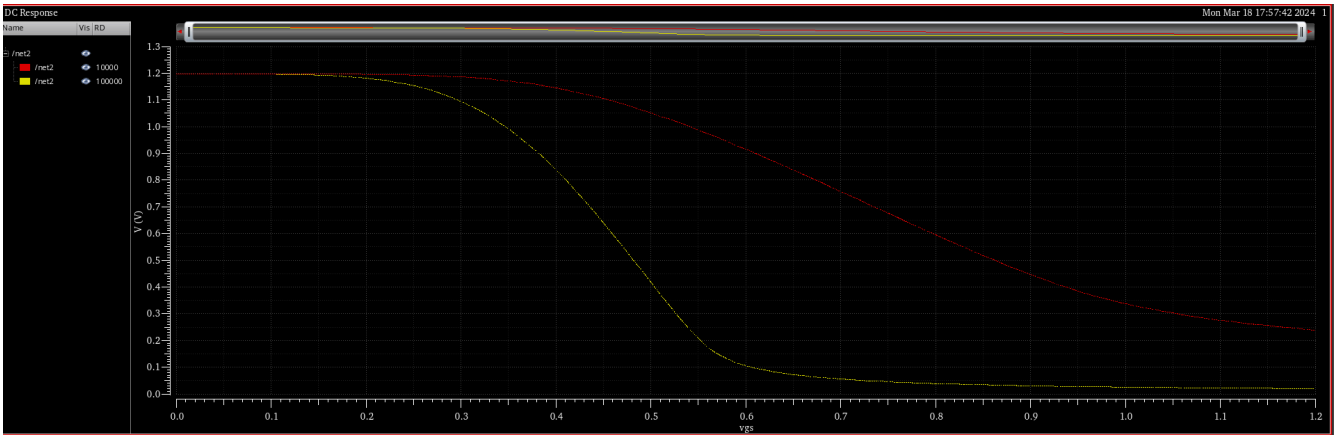
Check:

❖ **DC analysis:**

- Create testbench with V2 source is ***vdc type (in analogLib library)***, set value dc voltage is variable *vgs*.



- Consider $R_D = 10k\Omega$ and $R_D = 100k\Omega$, draw DC characteristic curve (using dc analysis, sweeping variable *vgs* from 0V to *vdd*)

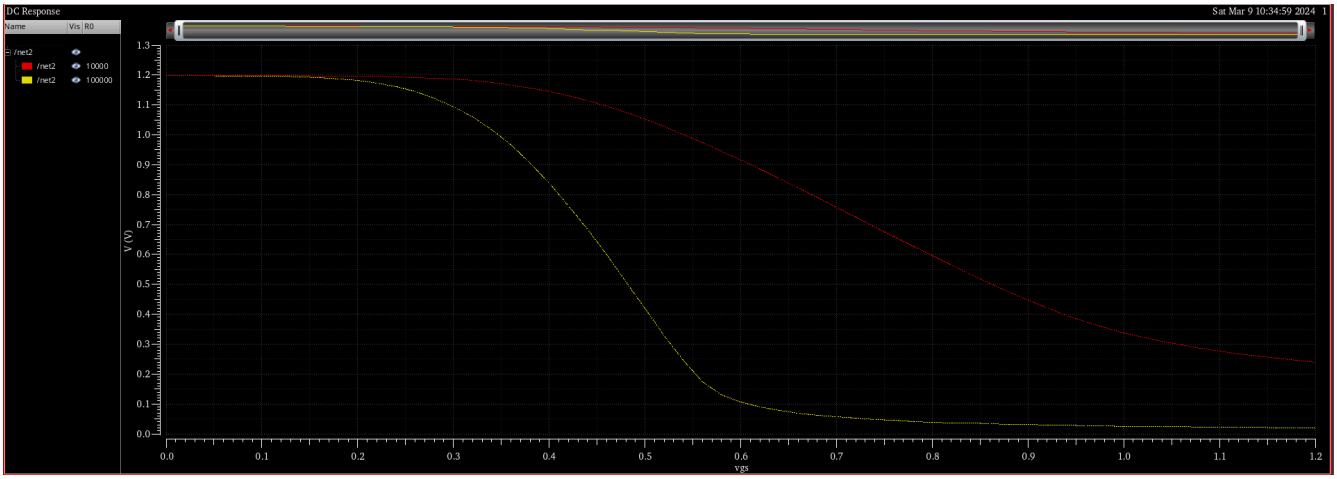


- Determine the operation point of NMOS device having the large gain. Choose the value of ***vgs* and R_D** has the better gain for the next consideration.

With $R_D = 100k\Omega$, the operation point of NMOS device having the large gain.
From the graph it can be seen that the largest gain value belongs to the range [0.3,0.55]
From 0.3 to 0.35: $\Delta = 0.1$
From 0.35 to 0.4: $\Delta = 0.19$
From 0.4 to 0.45: $\Delta = 0.195$
From 0.45 to 0.5: $\Delta = 0.215$
From 0.5 to 0.55: $\Delta = 0.19$
From 0.5 to 0.55: $\Delta = 0.19$
Consider:

From 0.45 to 0.47: $\Delta = 0.92\,mV$
From 0.47 to 0.49: $\Delta = 0.84\,mV$
operation point is nearly 450 mV
Gain $= \frac{V_{out}}{V_{in}} = \frac{0.637}{0.45} = 1.41$

Figure 2. DC characteristic curve with resistor load topology



- **Question:** Which value of R_D has the better gain? Explain the advanced and disadvantage with large and small R_D.

With $R_D = 100k\Omega$, the circuit has the better gain.

$I_D = \frac{V_{DD} - V_{out}}{R_D} = g_m V_{in} + r_o V_{out}$

$\Rightarrow V_{out}(r_o + \frac{1}{R_D}) = V_{in} g_m$

$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{g_m}{r_o + \frac{1}{R_D}}$

$A_V \uparrow \Rightarrow r_o + \frac{1}{R_D} \downarrow \Rightarrow R_D \uparrow$

Large R_D:	**Small R_D:**
Advantages: Improved Gain: A large RD can enhance the gain	**Advantages:** Faster Switching Speeds: With a small RD, the

of the transistor by allowing it to operate more efficiently in the saturation region, especially in amplifier circuits. Reduced Saturation Region Current Variation: With a large RD, the transistor operates more in the linear region rather than the saturation region. In the linear region, the drain current (ID) is less sensitive to changes in drain-source voltage (VDS). This reduces variations in ID due to VDS changes, which can improve stability in certain applications. Lower Power Dissipation: A large RD can help reduce power dissipation in the transistor because it limits the maximum current flow through the drain-source path. This can be advantageous in low-power designs where minimizing energy consumption is critical.	transistor operates more in the saturation region, where switching speeds are faster compared to the linear region. This is beneficial in applications where high-speed operation is essential, such as digital logic circuits or switching regulators.
Disadvantages: Slower Switching Speeds: Large RD slows down the charging and discharging of the drain-source capacitance (CDS). This results in slower switching speeds of the transistor, which can be detrimental in high-speed applications such as digital circuits or RF amplifiers. Increased Voltage Headroom: A large RD increases the voltage headroom required for the transistor to operate in the saturation region. This can limit the maximum achievable drain current and may necessitate higher supply voltages in certain applications.	**Disadvantages:** Increased Saturation Region Current Variation: With a small RD, the transistor is more prone to operate in the saturation region, where ID is highly sensitive to changes in VDS. This can result in larger variations in ID due to fluctuations in VDS, which may affect circuit performance and stability. Higher Power Dissipation: Small RD can lead to higher power dissipation in the transistor because it allows a larger drain current to flow, resulting in higher power losses, especially in applications where the transistor operates in the saturation region for extended periods.

- **AC analysis:**
  - Using DC analysis testbench as Figure 1, set the value of *vgs* equal to the value chosen in DC analysis. Set value ***ac voltage*** of V2 source equals to ***1V***.
  - Draw frequency response with ac analysis, frequency varies from 1Hz to 10GHz.

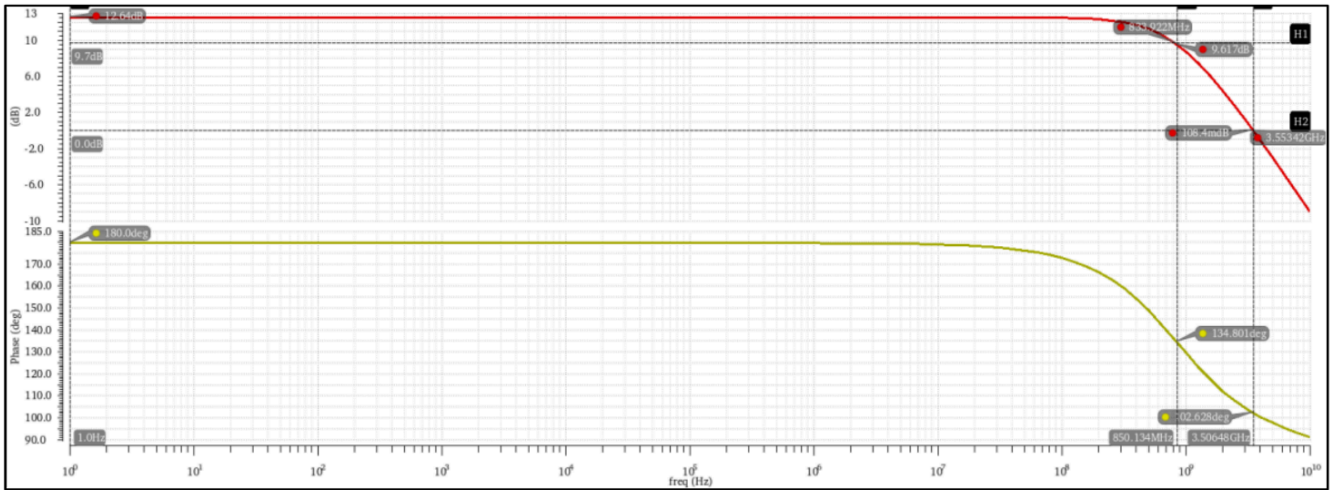
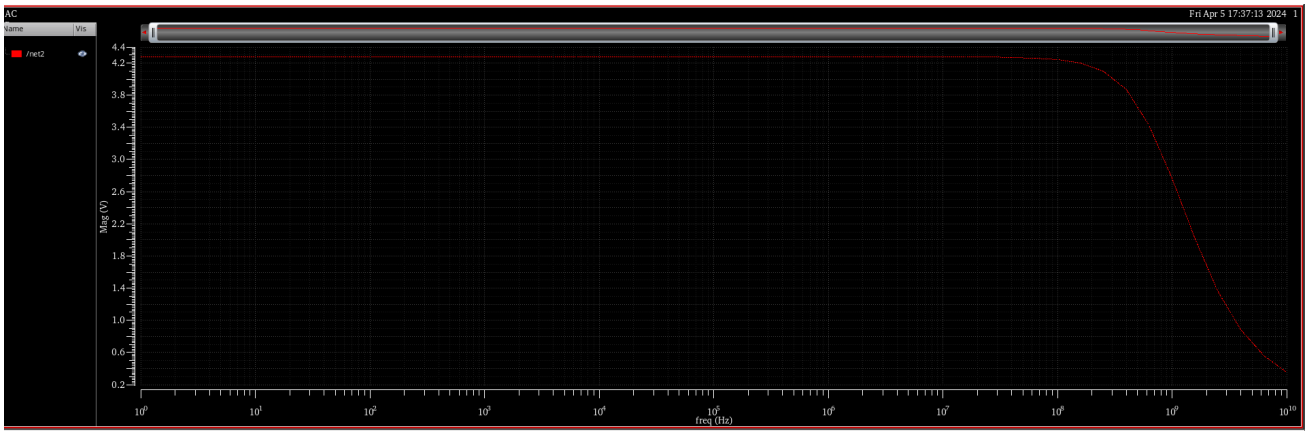
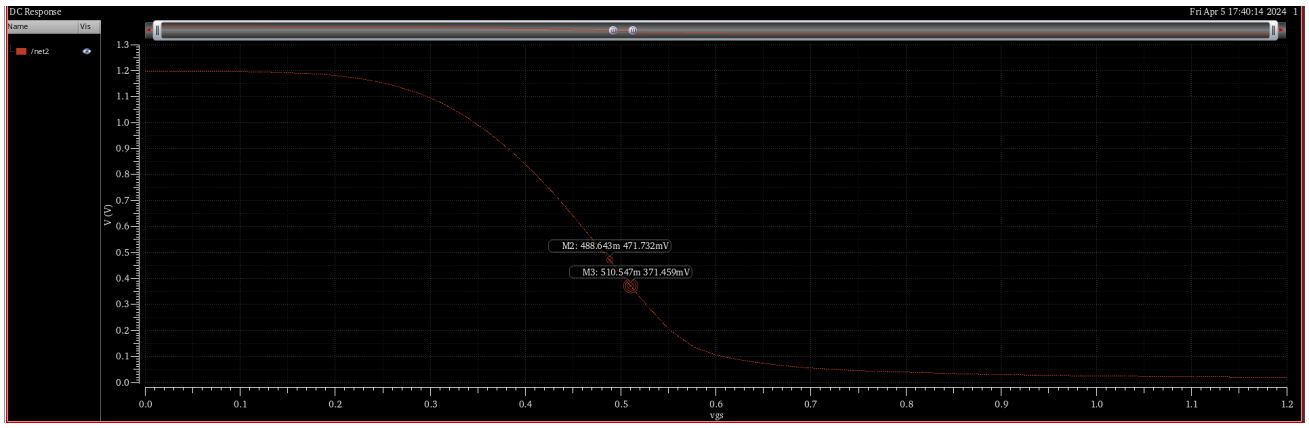


Figure 3. AC characteristic curve with resistor load topology

- Determine the DC gain, phase margin, and bandwidth.



AC analysis



DC analysis

$$A_v = \frac{371-471}{510-488} = -\ 4.5$$

The frequency at 0dB is bandwidth so gain bandwidth is nearly 3.6 GHz
The degree curve from 90 to 102.62 so phase margin is 12.62 degree

❖ **TRAN analysis:**

- Replace V2 source from ***vdc*** type to ***vsin*** type. Set the ***offset voltage equal to vgs*** equal to the value chosen in DC analysis, frequency = 1MHz, amplitude = 10mV.

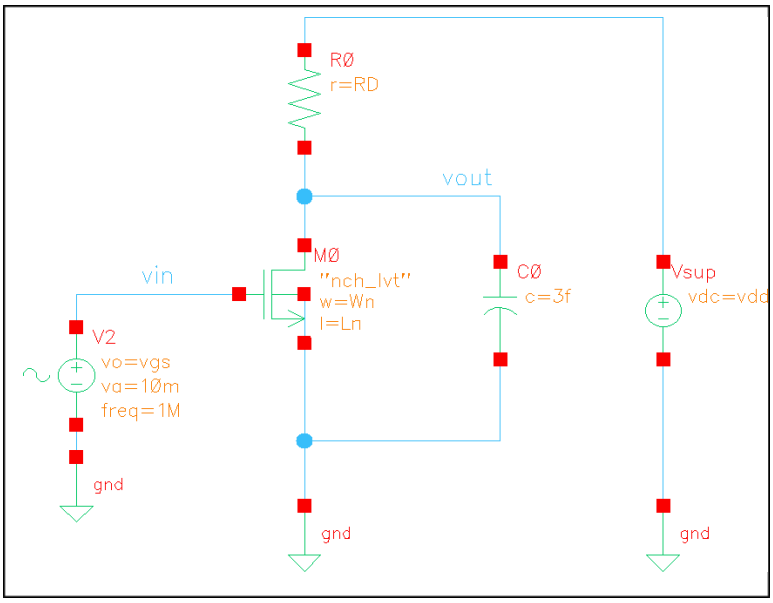


Figure 4. Common source stage with resistor load topology for TRAN analysis

- Draw the input and output waveform with transient analysis from 0s to 20us.

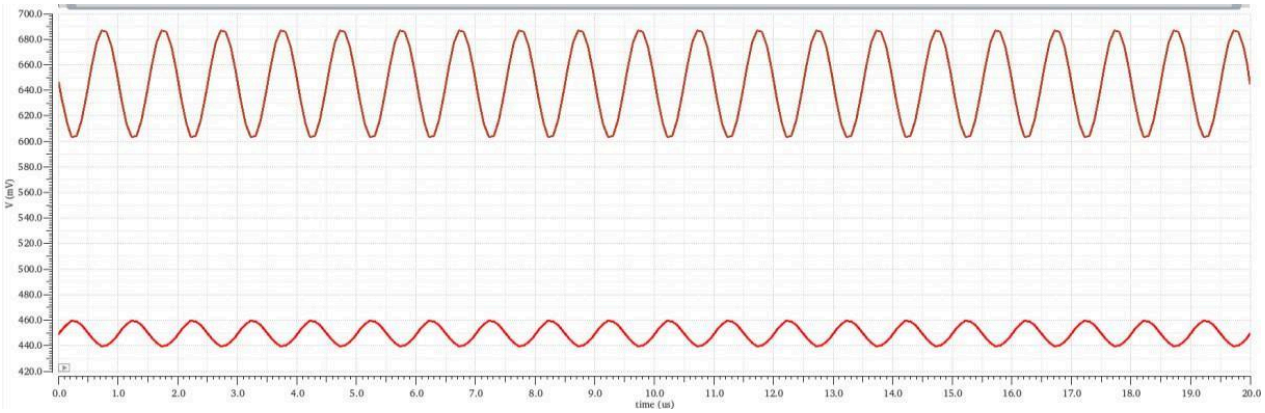
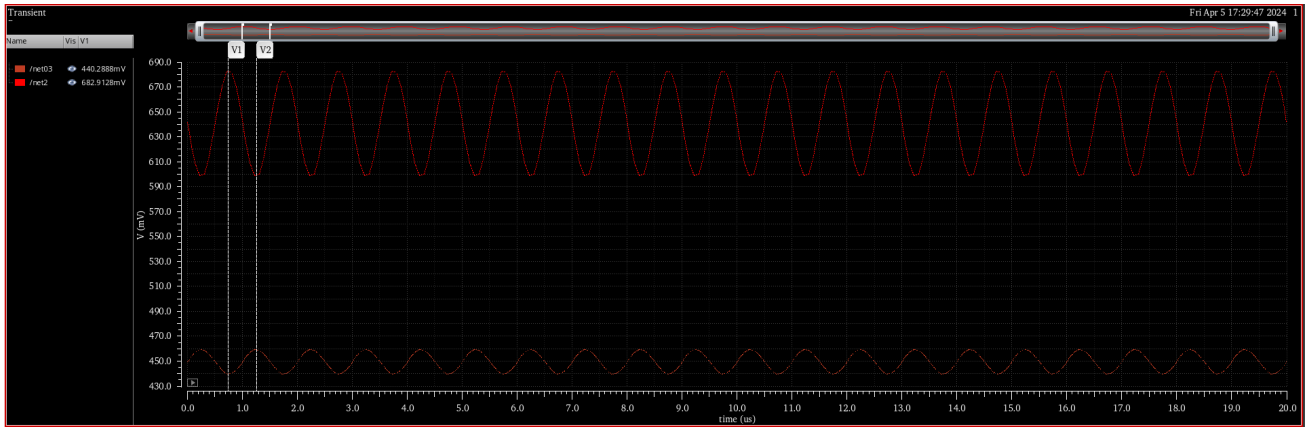


Figure 5. TRAN waveform with resistor load topology

- Determine the gain from the amplitude of input and output waveform. Compare to

result with DC and AC analysis.



$$A_v = \frac{600-682}{460-440} = -4.1$$

There is a slight difference between AC and TRANS analysis because when performing AV measurements in AC analysis, we choose to round the number and analyze by estimating

EXPERIMENT 2

Objective: Consider a common source single amplifier with diode-connected load topology.

Requirements: Simulate dc, ac and transient analysis

Instruction: Assemble the circuit as shown in ***Figure 6***, setting parameters for power supplies (using ***vdc*** source), with $L_n = 60nm$, $L_p = 60nm$, $vdd = 1.2V$

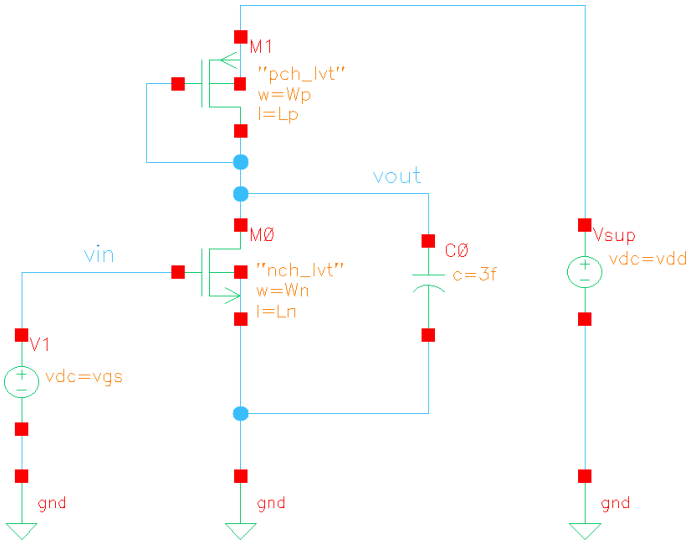
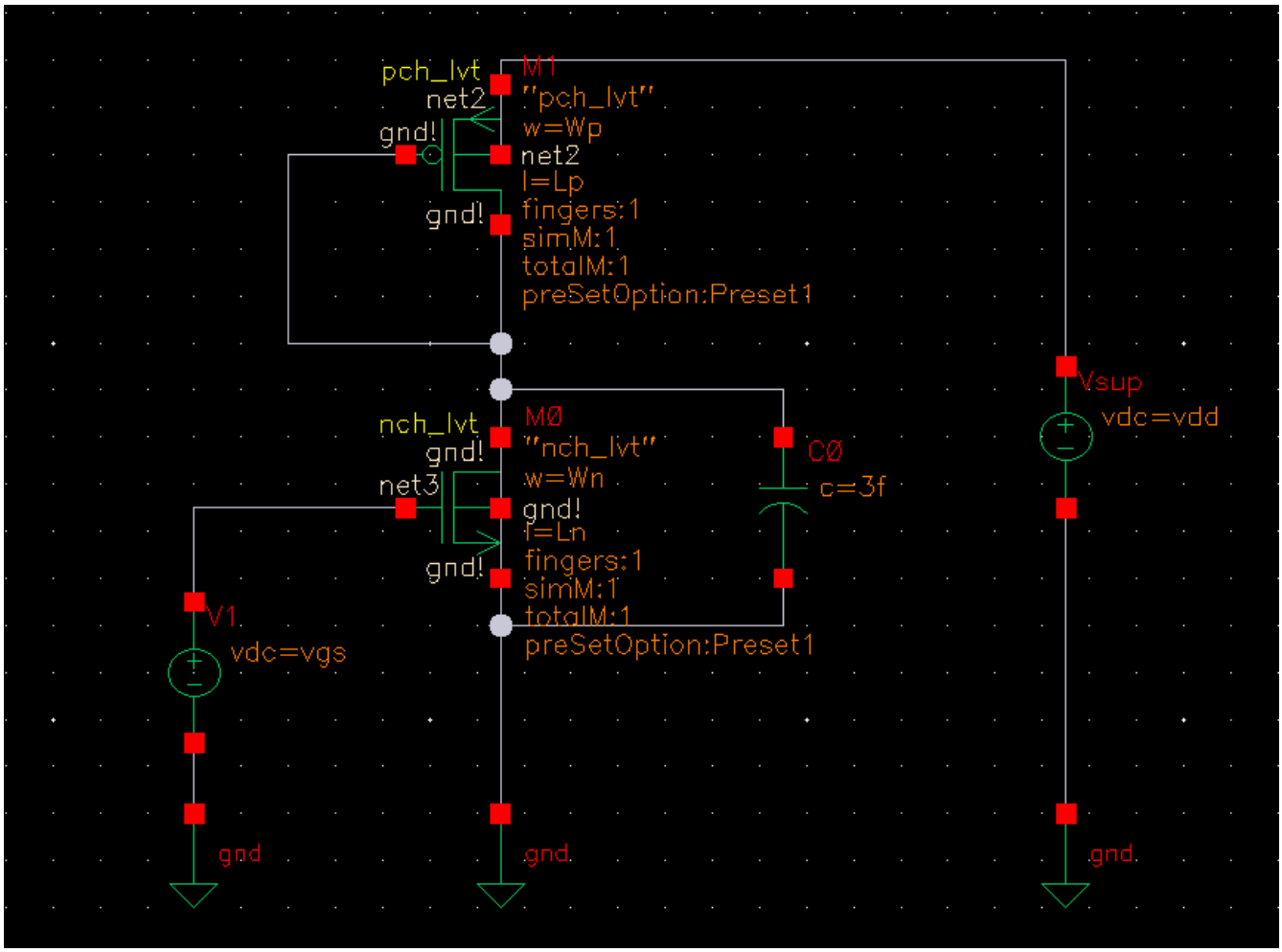


Figure 6. Common source stage with diode-connected load topology for DC and AC analysis



Check:

❖ **DC analysis:**

- Using DC analysis, you verify the W_n and W_p that the amplifier circuit has gain greater than 2 ($A_v > 2$). The method to determine the gain of amplifier circuit in DC analysis has proposed in Experiment 1.

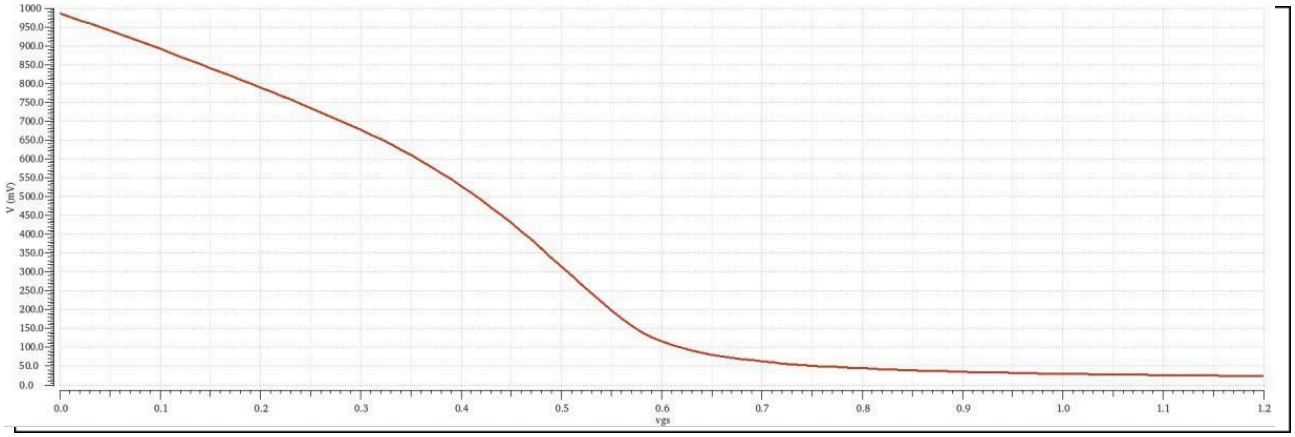
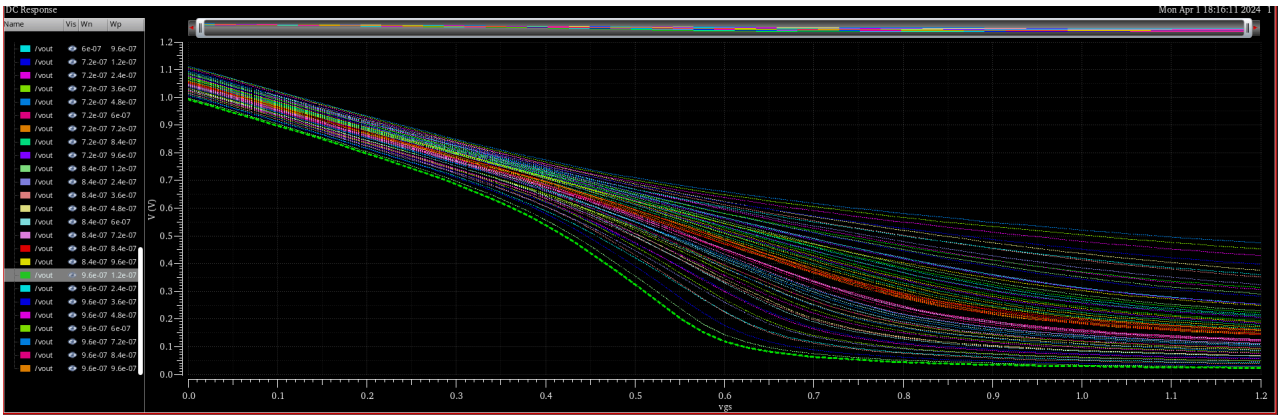
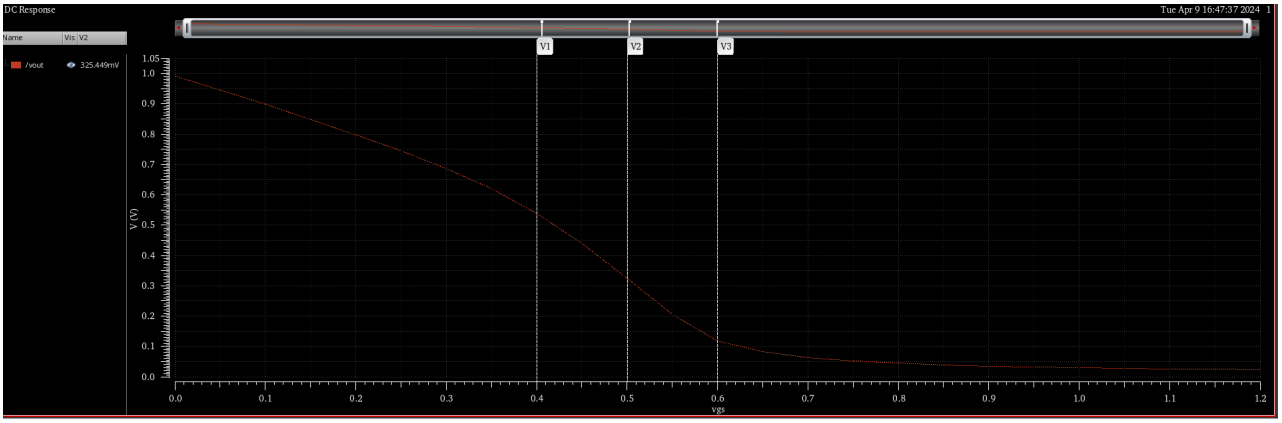


Figure 7. DC characteristic curve with diode-connected load topology



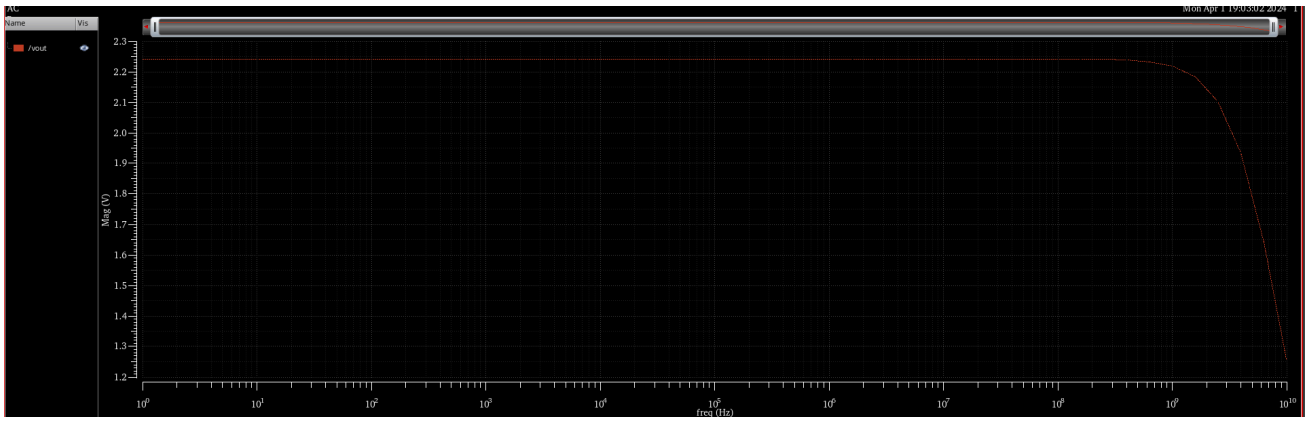
Can be seen that, A_v get the operation point around Vgs from 0.5V to 0.6V
with $Wn = 960\,nm;\ Wp = 120n$,A_v is largest

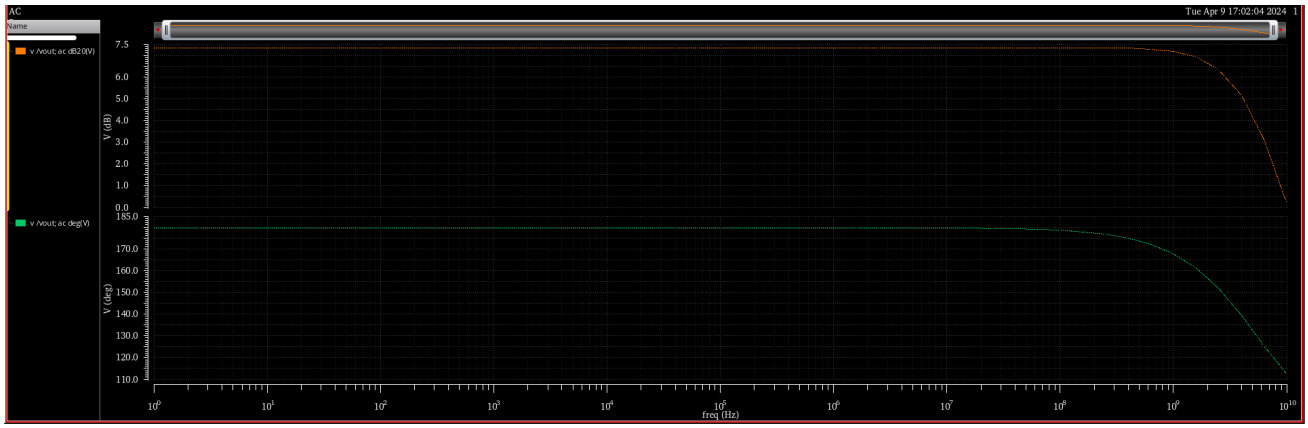


Av get largest when Vgs from 0.4 to 0.5
Operating point VGS= 0.45
A_v = -2.3

❖ **AC analysis:**

- Using DC analysis testbench as Figure 6, set the value of *vgs* equal to the value chosen in DC analysis. Set value ***ac voltage*** of V1 source equals to ***1V***.
- Draw frequency response with ac analysis, frequency varies from 1Hz to 10GHz.


AC
Mon Apr 1 19:03:02 2024
Name
Vis
/vout
Mag (V)
freq (Hz)


AC
Tue Apr 9 17:02:04 2024
Name
v /vout; ac dB20(V)
v /vout; ac deg(V)
V (dB)
V (deg)
freq (Hz)

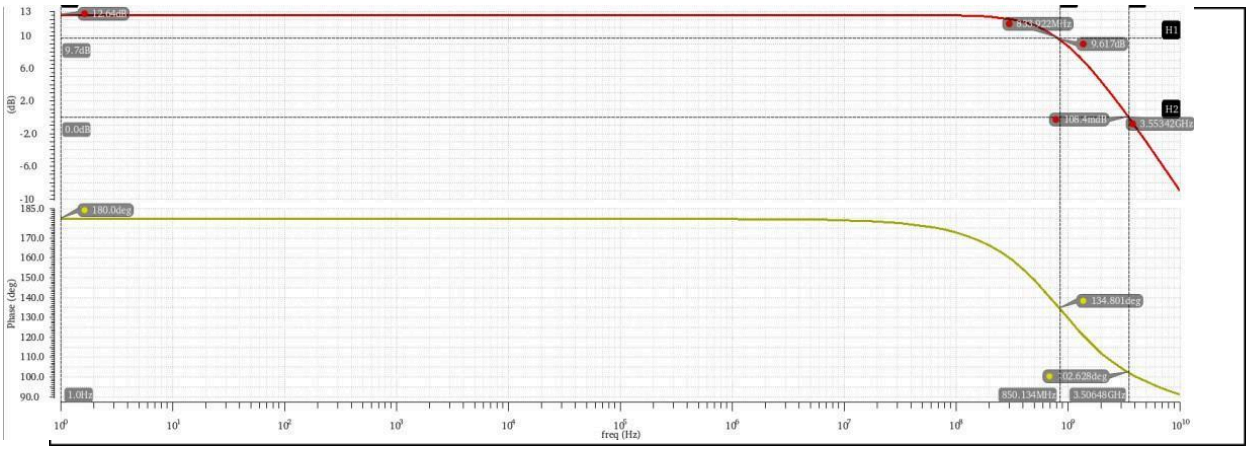
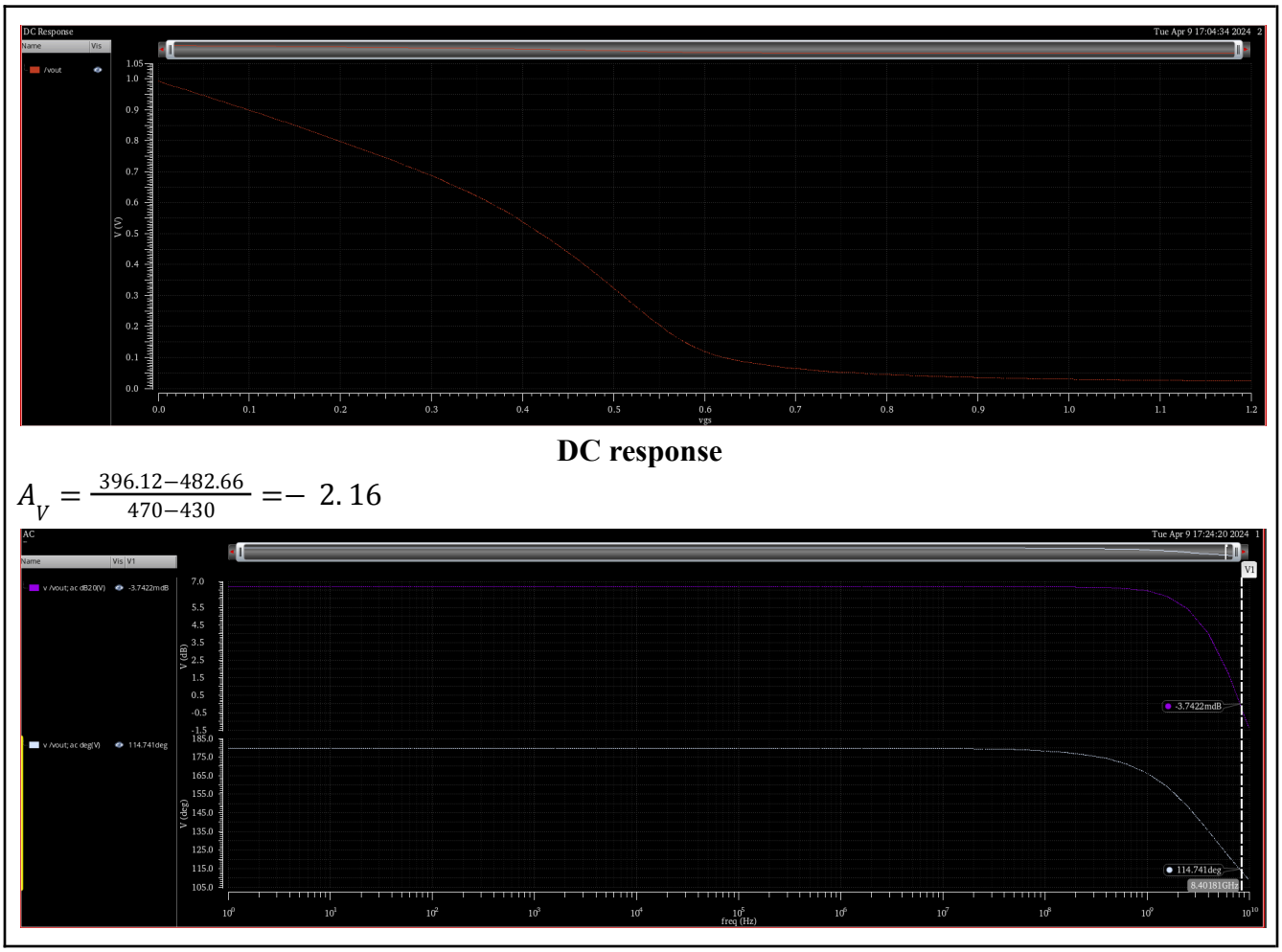


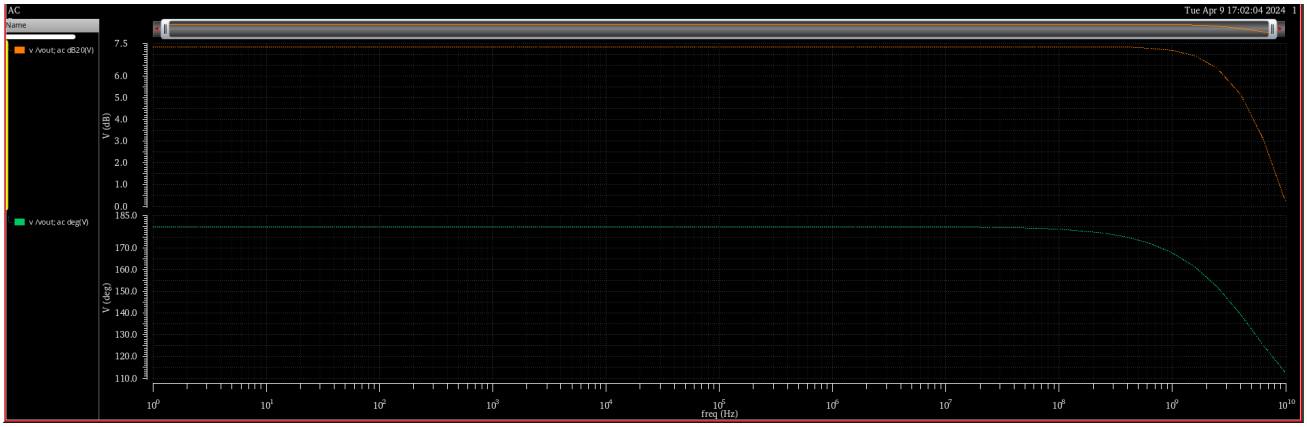
Figure 8. AC characteristic curve with diode-connected load topology

- Determine the DC gain, phase margin, and bandwidth.



DC response

$$A_V = \frac{396.12-482.66}{470-430} = -\ 2.16$$



The frequency at 0dB is bandwidth so gain bandwidth is nearly 8.4 GHz
The degree curve from 105 to 114.74 so phase margin is 9.74 degree

❖ TRAN analysis:

- Replace V1 source from ***vdc*** type to ***vsin*** type. Set the ***offset voltage equal to vgs*** equal to the value chosen in DC analysis, frequency = 1MHz, amplitude = 10mV.
- Draw the input and output waveform with transient analysis from 0s to 20us.

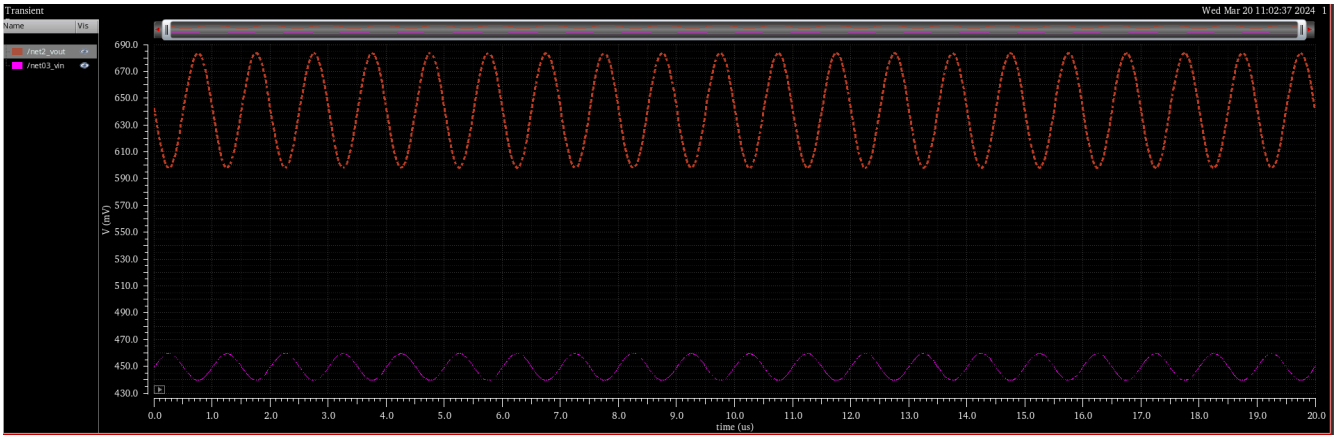
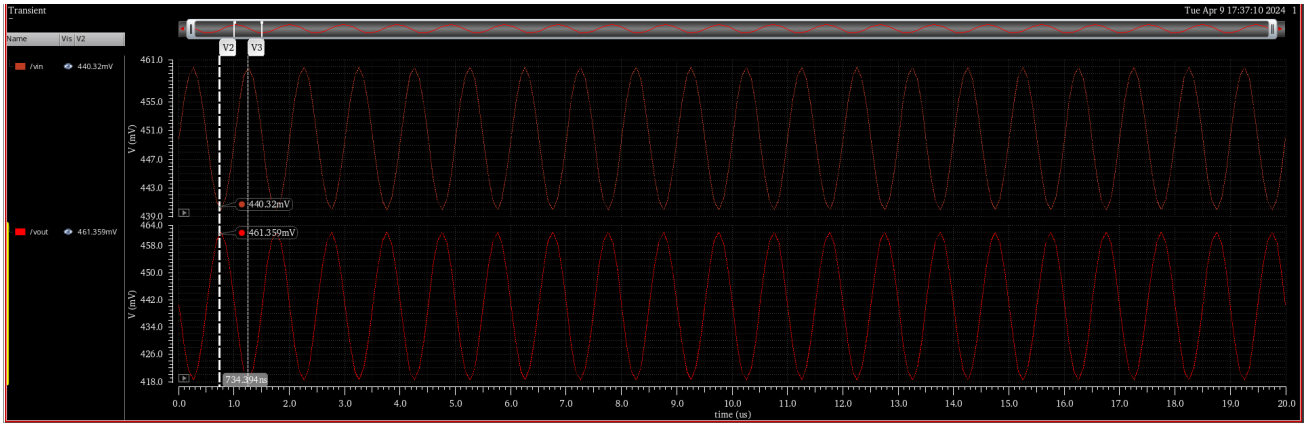


Figure 9. TRAN waveform with diode-connected load topology

- Determine the gain from the amplitude of the input and output waveform. Compare the result with DC and AC analysis.



$A_v = \frac{460-420}{440-460} = -2$

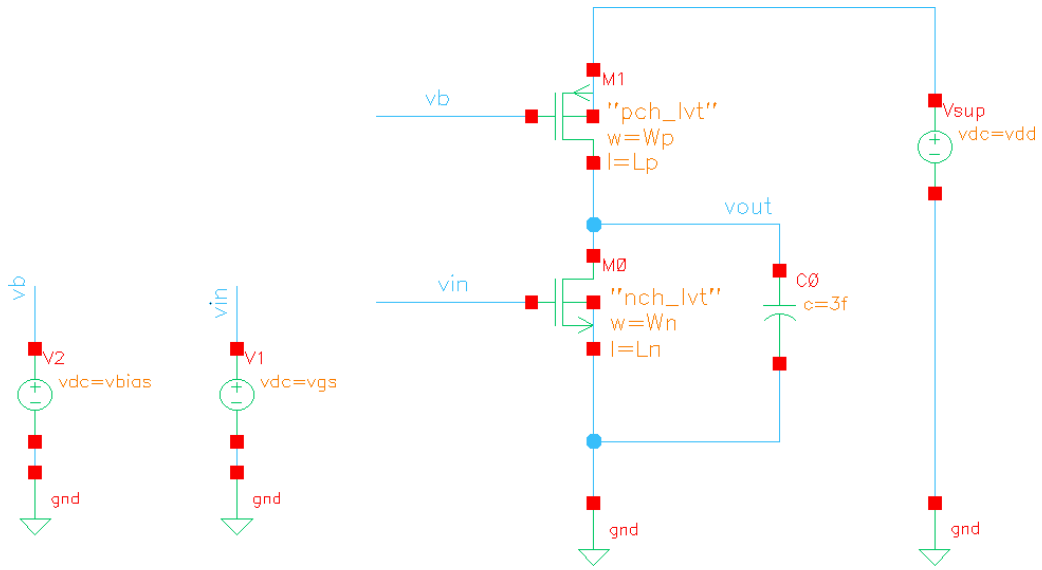
There is a slight difference between AC and TRANS analysis because when performing AV measurements in AC analysis, we choose to round the number and analyze by estimating

EXPERIMENT 3

Objective: Consider a common source single amplifier with current source load topology.

Requirements: Simulate dc, ac and transient analysis.

Instruction: Assemble the circuit as shown in ***Figure 10***, setting parameters for power supplies (using ***vdc*** source), with $L_n = 60nm$, $L_p = 60nm$, $vdd = 1.2V$



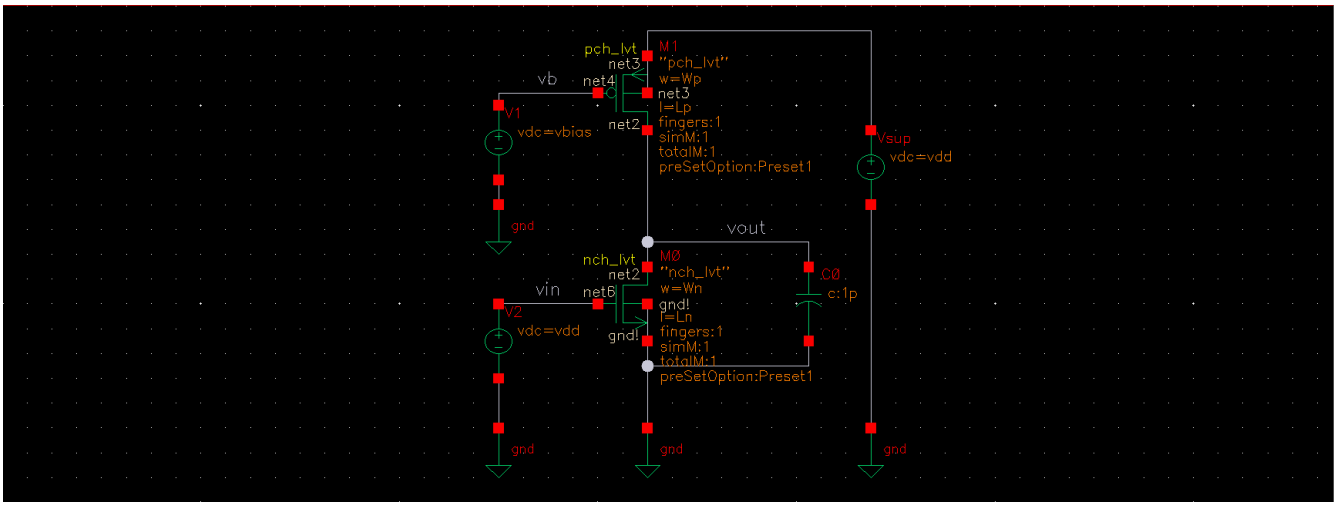


Figure 10. Common source stage with current source load topology for DC and AC analysis

Check:

❖ **DC analysis:**

- Using DC analysis, you verify the W_n, W_p and v_{bias} that the amplifier circuit has gain greater than 4 ($A_v > 4$). The method to determine gain of the amplifier circuit in DC analysis has been proposed in Experiment 1.

$$-\frac{V_{out}}{r_{o2}} = gm_1 V_{in} + \frac{V_{out}}{r_{o1}}$$

$$\Rightarrow A_v = -\frac{gm_1}{\frac{1}{r_{o2}}+\frac{1}{r_{o1}}}$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_N(1 + \lambda V_{out})I_D}$$

Assume I have λ_N,λ_P,$\mu_n C_{ox}$

$$r_{o1} = \frac{1}{\lambda_N I} = \frac{1}{0.1I} \; ; r_{o2} = \frac{1}{\lambda_p I} = \frac{1}{0.2I}$$

$$A_V > 4$$

$$\Rightarrow gm_1 > 4\left(\frac{1}{r_{o2}} + \frac{1}{r_{o1}}\right)$$

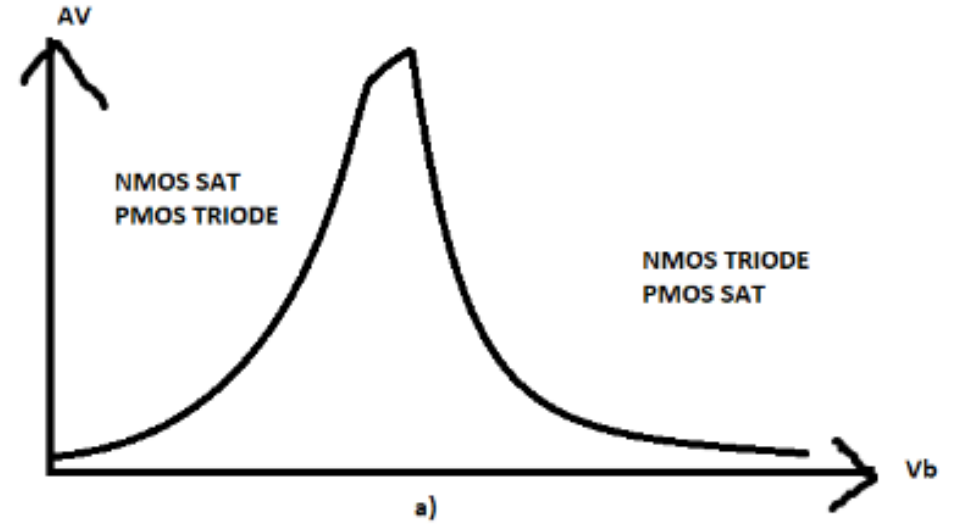
$$\Rightarrow gm_1 > 4(0.3I_D)$$

$$\Rightarrow 2\mu_n C_{ox}(\frac{W}{L})_N(1 + \lambda V_{out}) > 1.44I_D$$

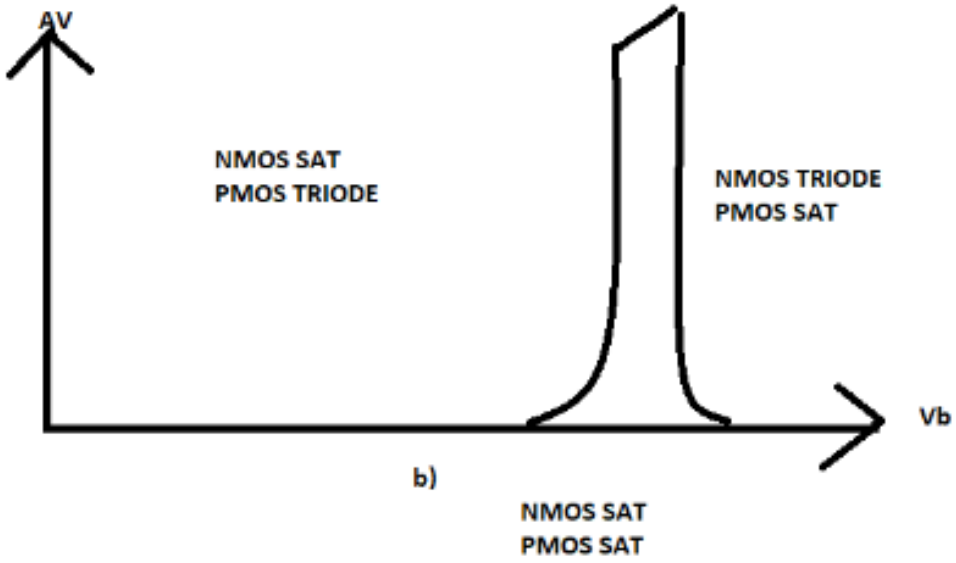
$$\Rightarrow 2 * 1.34225 * 10^{-4}\frac{W_N}{60n}(1 + 0.1V_{out}) > 1.44I_D$$

Consider in two case
NMOS enter the triode region before PMOS is saturated
NMOS enter the triode region after PMOS is saturated

at Vb = 0 small signal voltage gain in a) is higher than Vb in b). That is because gm1 in case 1 is higher than that in b). However, small signal voltage gain in a) is less than that in b because when Vb sweeps all the way from 0 to VDD, nowhere are both devices simultaneously in saturation region



a)



b)

NMOS SAT
PMOS SAT

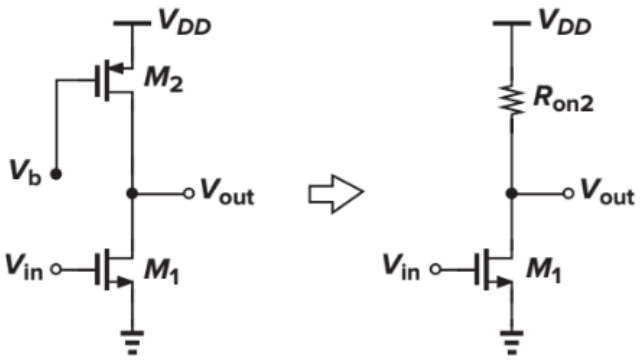
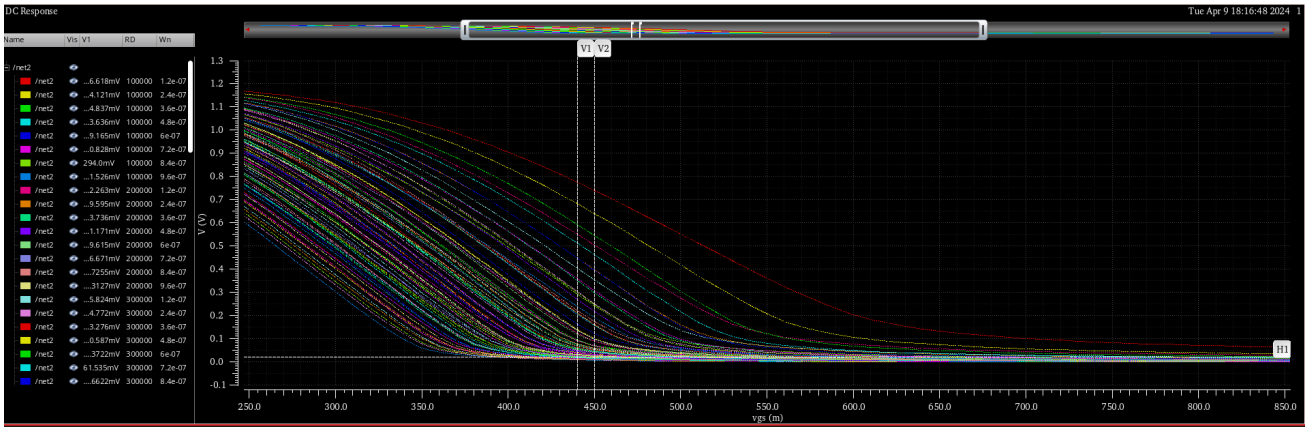
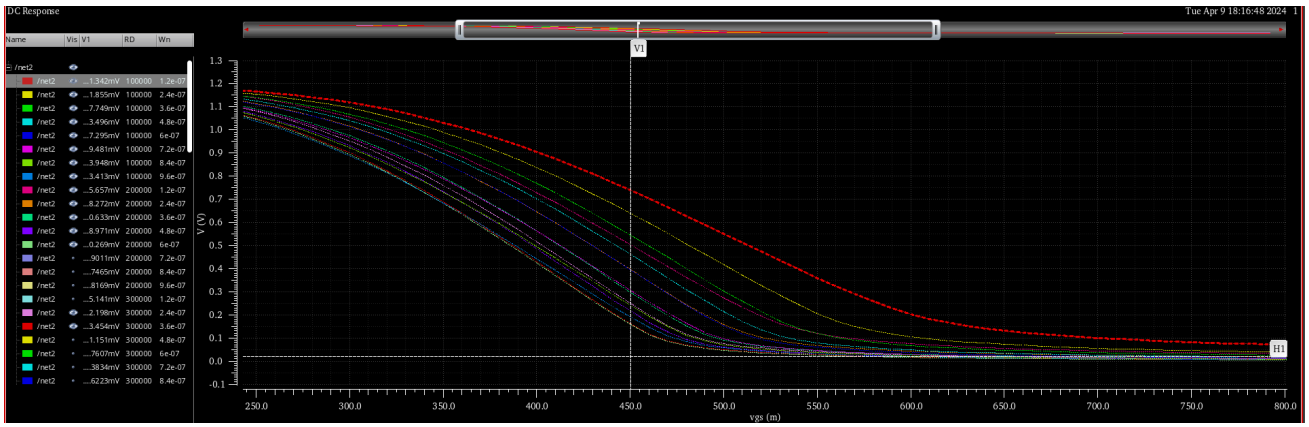
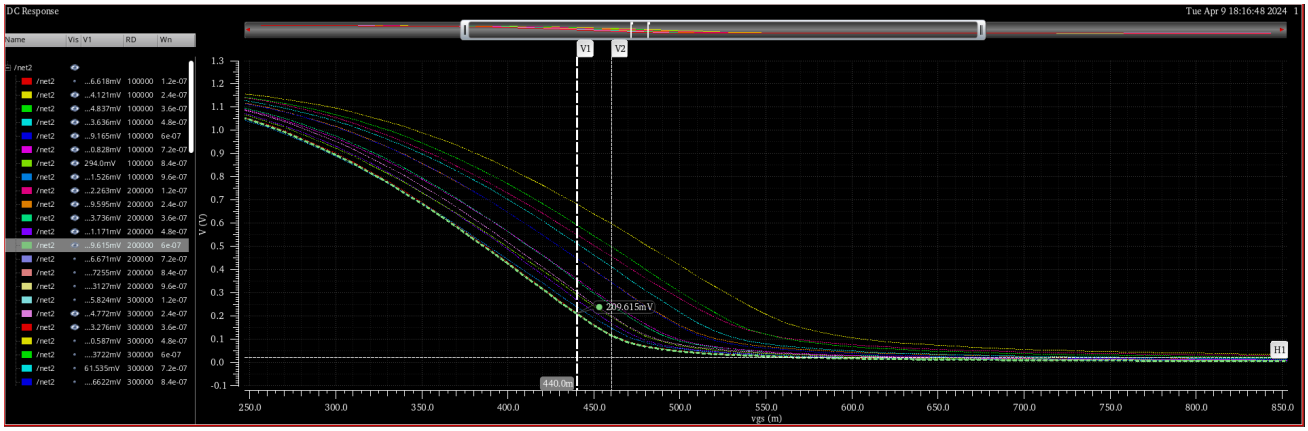


Figure 3.22 CS stage with triode load.

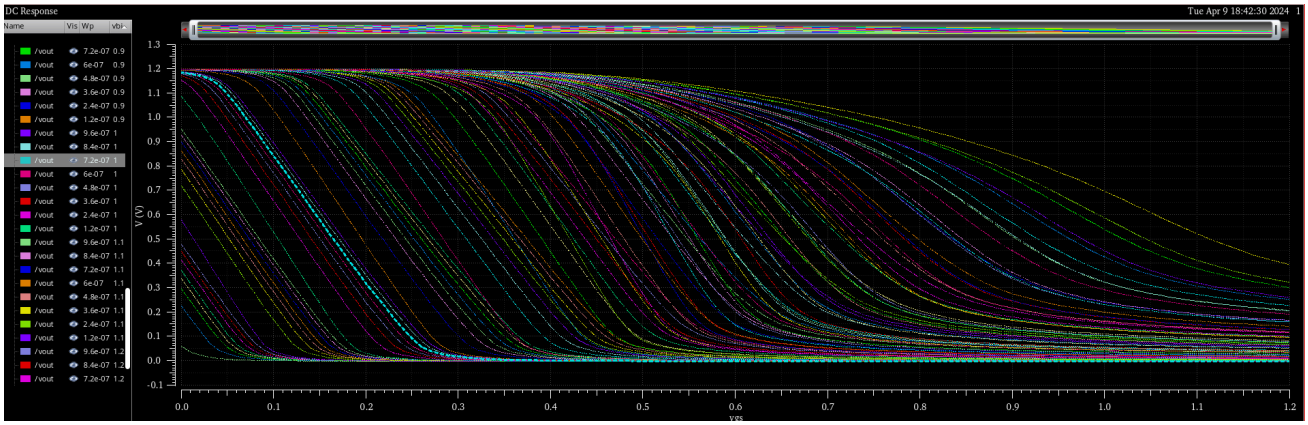




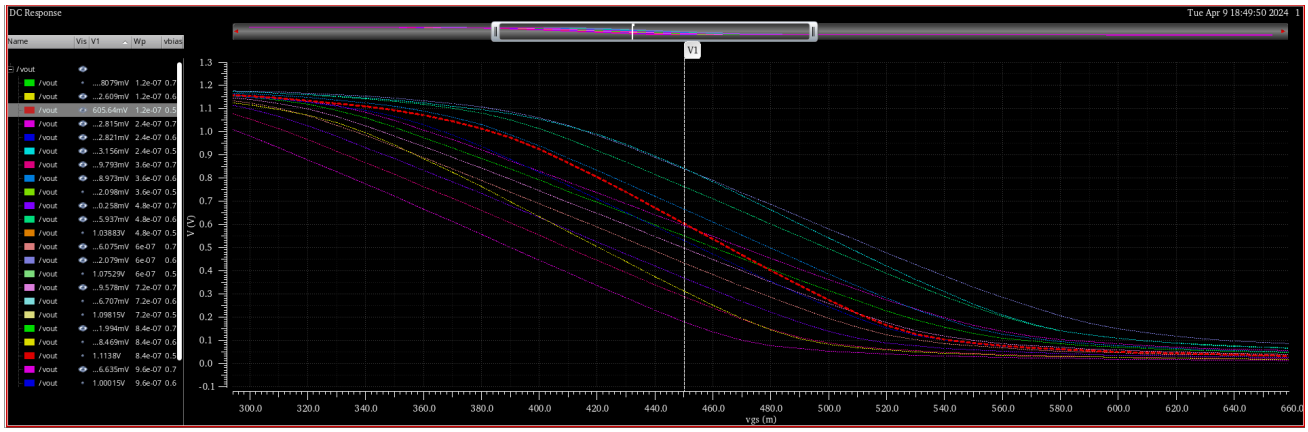
$R_{ON2} \in [10k - 20k]$



$R_{ON2} = 20k\ ; W_N = 600\ nm$



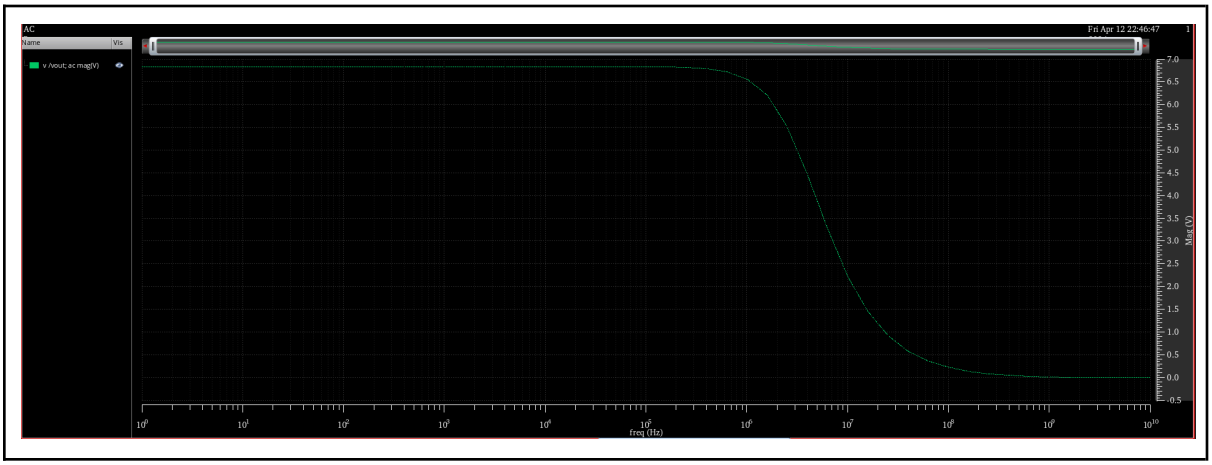
$V_{bias} \in [0.5, 0.6, 0.7]$



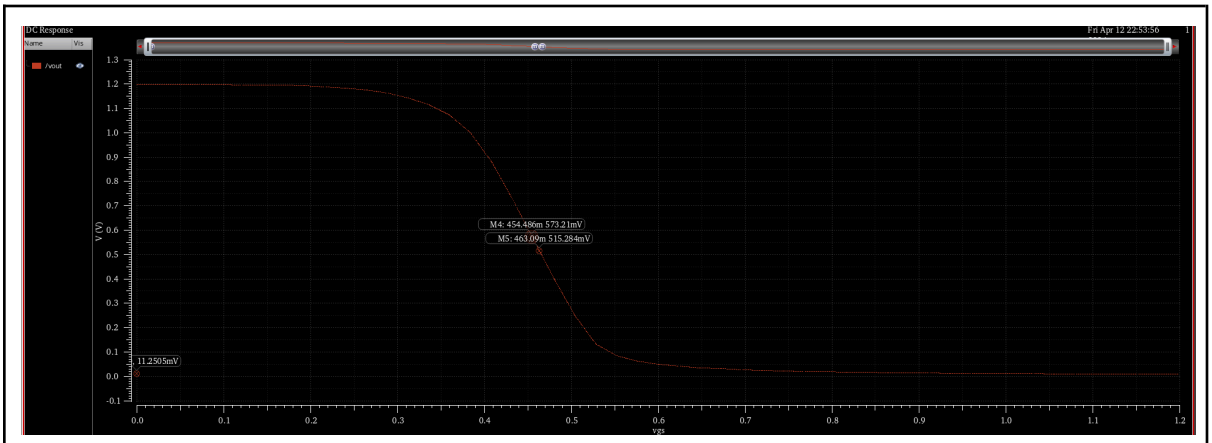
$V_{bias} = 0.5\,V\ ;\ W_p = 120\,nm;\ W_N = 600\,nm;\ V_{GS} = 0.45V$

❖ **AC analysis:**

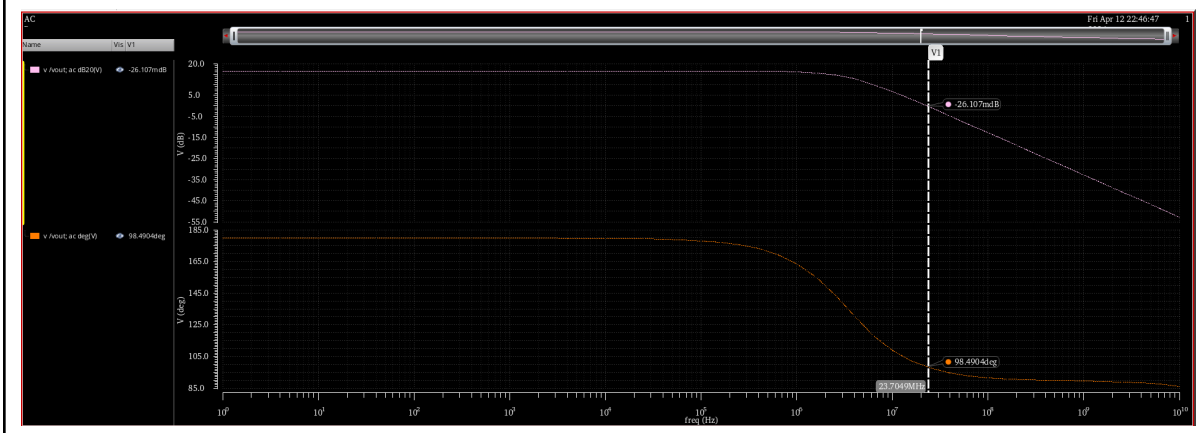
- Using DC analysis testbench as Figure 10, set the value of *vgs* equal to the value chosen in DC analysis. Set value ***ac voltage*** of V1 source equals to ***1V***.
- Draw frequency response with ac analysis, frequency varies from 1Hz to 10GHz.



- Determine the DC gain, phase margin, and bandwidth.



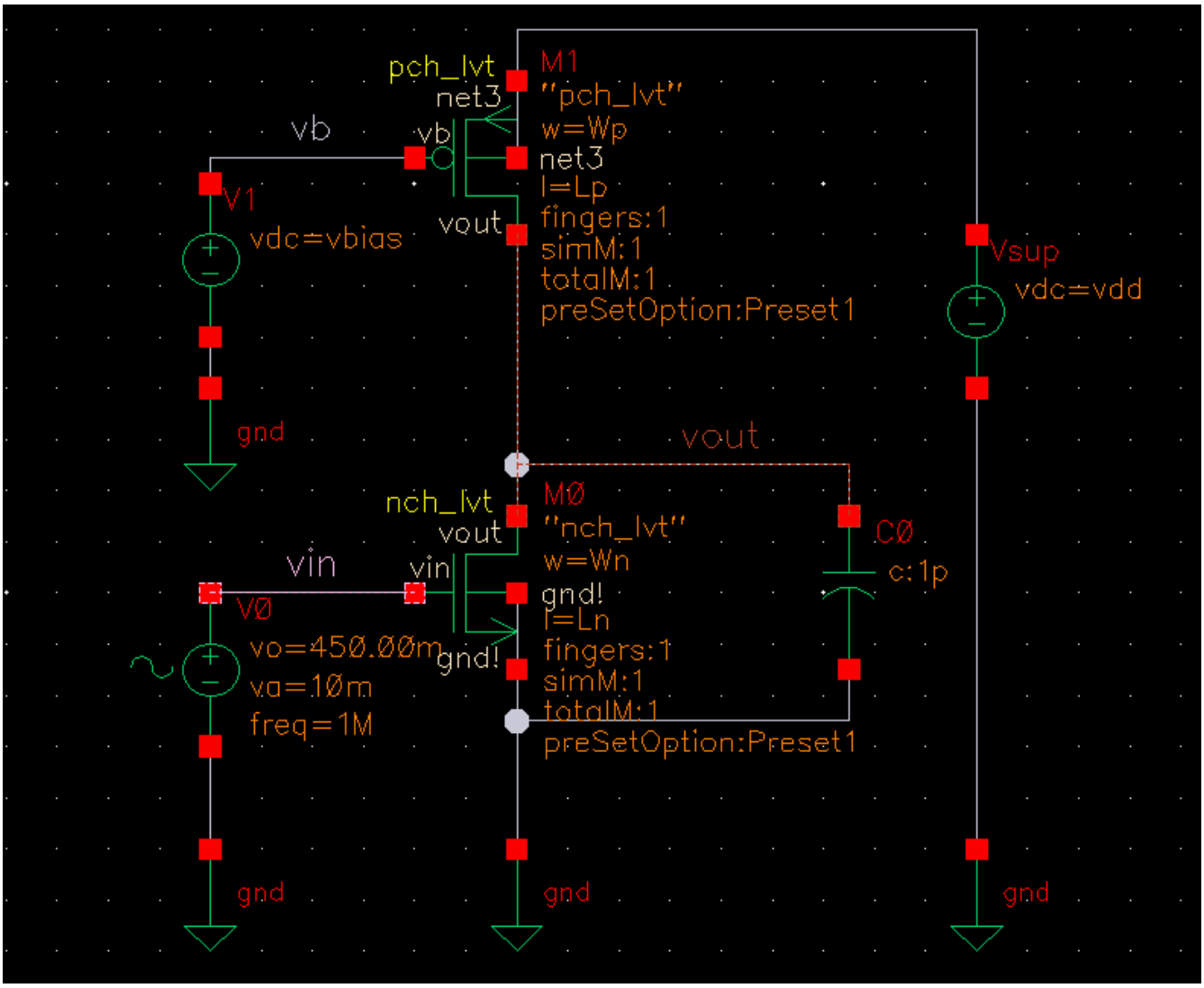
$A_V = -6.7$



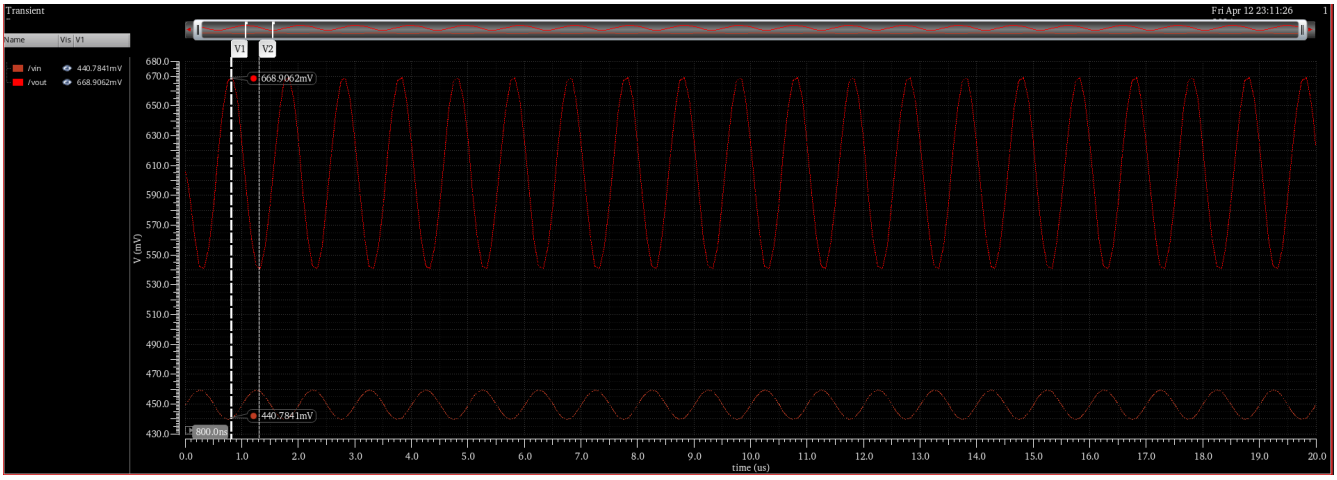
The frequency at 0dB is bandwidth so gain bandwidth is nearly 23.7MHz
The degree curve from 85 to 98 so phase margin is 13 degree

❖ **TRAN analysis:**

- Replace V1 source from ***vdc*** type to ***vsin*** type. Set the ***offset voltage equal to vgs*** equal to the value chosen in DC analysis, frequency = 1MHz, amplitude = 10mV.



- Draw the input and output waveform with transient analysis from 0s to 20us.



- Determine the gain from the amplitude of the input and output waveform. Compare the result with DC and AC analysis.

$A_V = -7$
There is a difference between AC and TRANS analysis because when performing AV measurements in AC analysis, we choose to round the number and analyze by estimating

- **Question:**

- Summary the method to increase the gain of amplifiers for 3 topologies considered in this LAB 2. What is the trade-off performance?

Common Source Amplifier:

- Increase the W/L (width/length) ratio of the MOSFET: By increasing the channel width (W) or decreasing the channel length (L) of the MOSFET, the transconductance gm and thus the gain can be increased.
- Increase the load resistance (RL): Increasing the load resistance connected to the drain of the MOSFET can also increase the voltage gain
- Trade-off: Increasing the W/L ratio increases the area of the MOSFET, which can lead to higher manufacturing costs and larger chip sizes. Increasing RL may reduce the bandwidth of the amplifier due to the increased RC time constant.

Trade-off Performance:

- Increasing gain often comes at the cost of bandwidth, power consumption, or stability.
- Higher gain may lead to reduced bandwidth due to increased pole-zero effects.
- Higher gain often requires larger bias currents, which can increase power consumption and heat dissipation.
- Increasing gain may also lead to decreased

- Summary the advances and disadvantages of 3 amplifier topologies.

Common Source Stage with Diode-Connected Load:
Advantages: High output impedance, simple biasing, good linearity.
Disadvantages: Limited voltage swing, limited gain, sensitivity to process variations.

Common Source Stage with Resistor Load:
Advantages: Wide voltage swing, high gain, simple implementation.
Disadvantages: Low output impedance, susceptibility to noise, limited linearity.

Common Source Stage with Current Source Load:
Advantages: High output impedance, improved linearity, better stability.
Disadvantages: Complex biasing, higher power consumption, slightly reduced gain