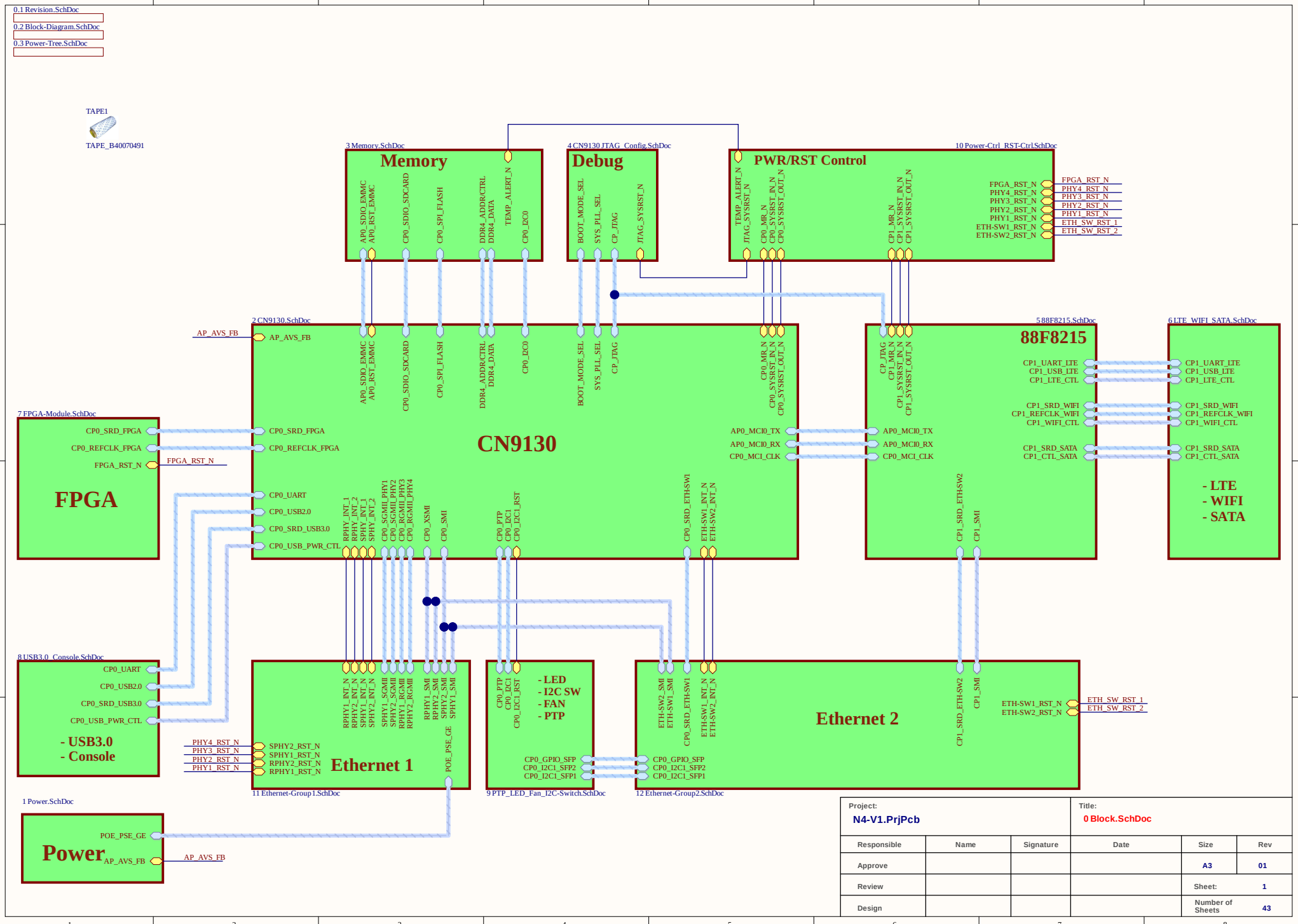

Project:			Title:		
N4-V1.PrjPcb			0 Block.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	1
Design				Number of Sheets	43

Project:			Title:		
N4-V1.PrjPcb			0.1 Revision.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	2
Design				Number of Sheets	43

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Project:			Title:		
N4-V1.PrjPcb			0.2 Block-Diagram.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	3
Design				Number of Sheets	43

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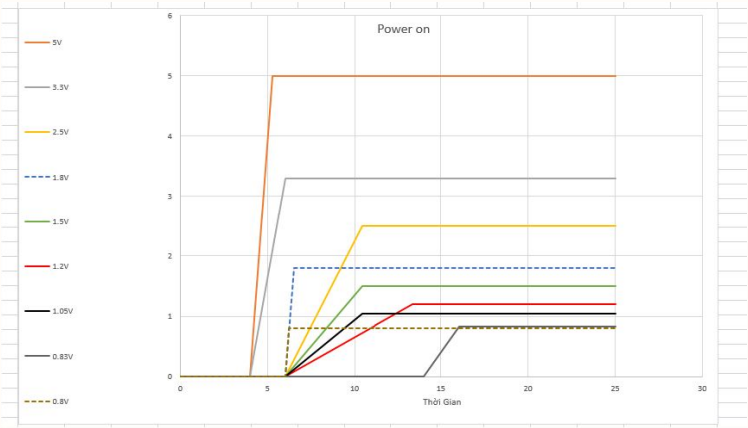

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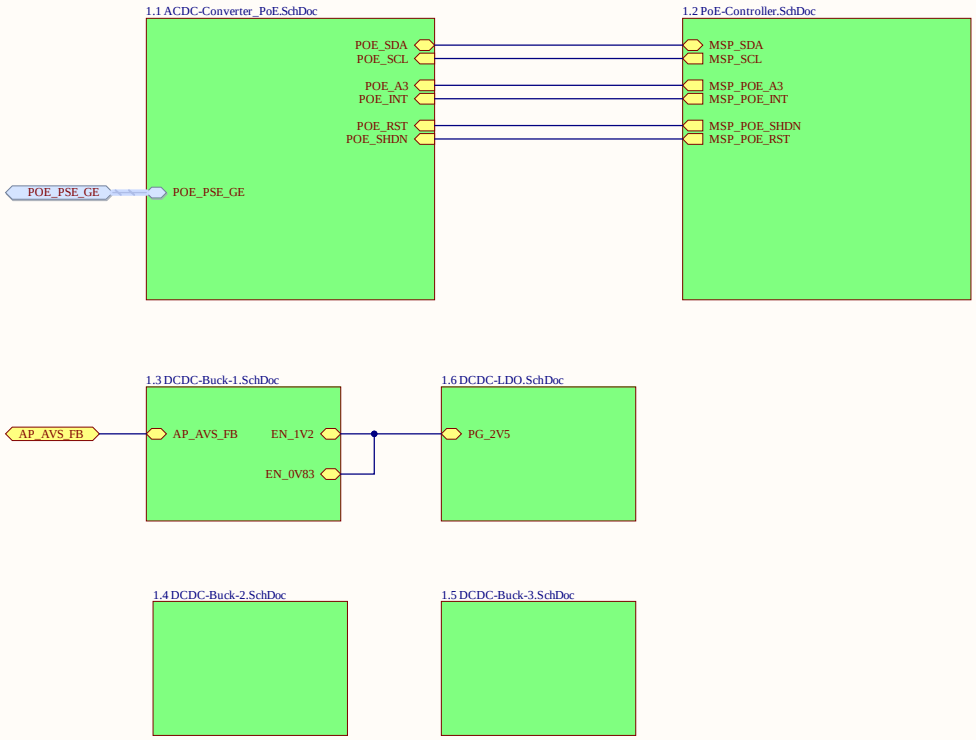
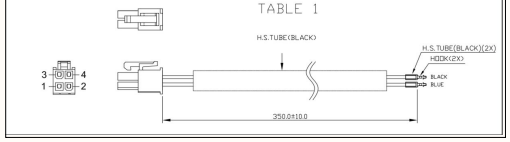
N4-V1.PrjPcb			0.3 Power-Tree.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	4
Design				Number of Sheets	43

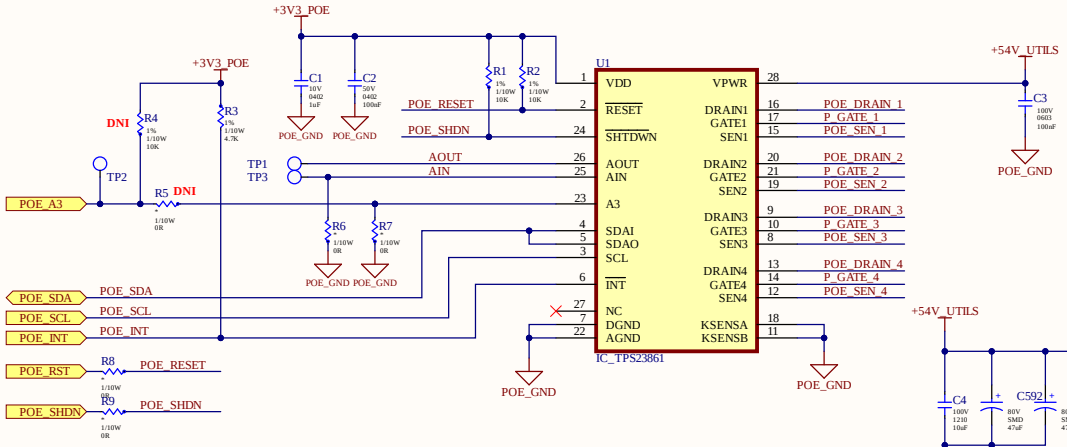


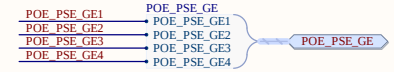
Project:			Title:		
N4-V1.PrjPcb			1 Power.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	5
Design				Number of Sheets	43

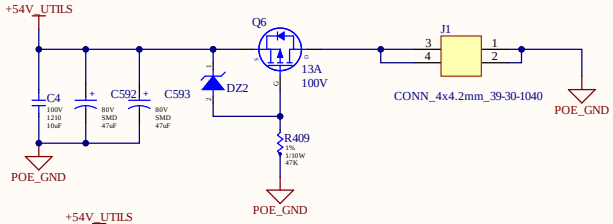
TABLE 1 :
HOUSING : MOLEX 39-01-2045 OR EQUIVALENT.
TERMINAL : MOLEX 39-00-0038 OR EQUIVALENT.
PLUG HOUSINGS : MOLEX, 5559
HEADER : MOLEX, 5566, 5569, 43810, 44068, 44281, 87427, 42404, 42440

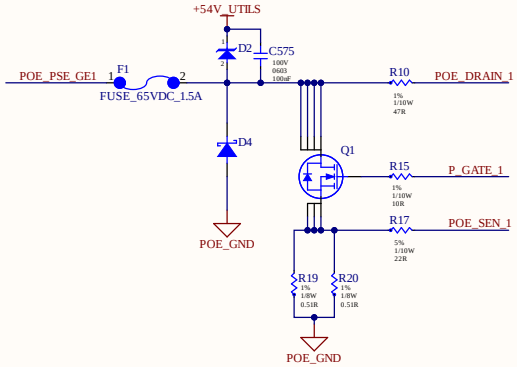
PIN	WIRE COLOR	PIN CONN
1	BLACK	54V RTN
2	BLACK	54V RTN
3	BLUE	54V
4	BLUE	54V

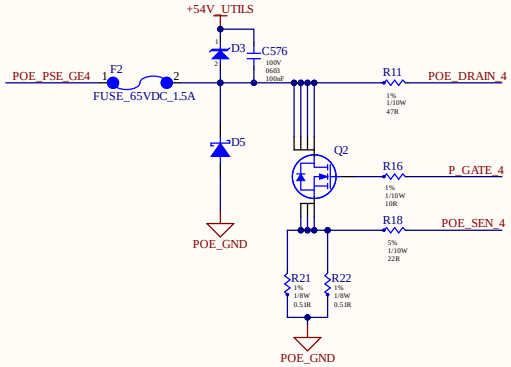


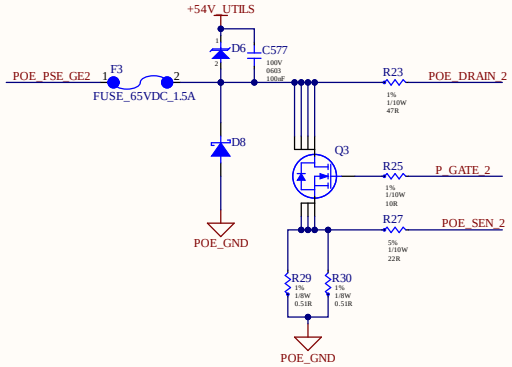


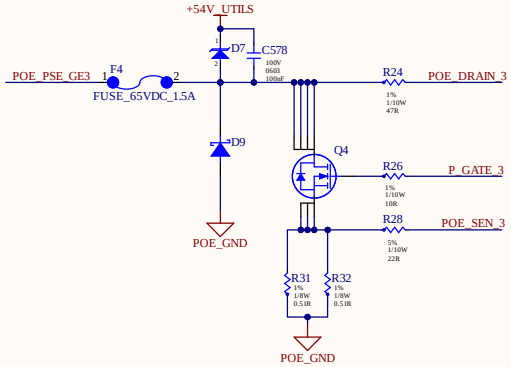


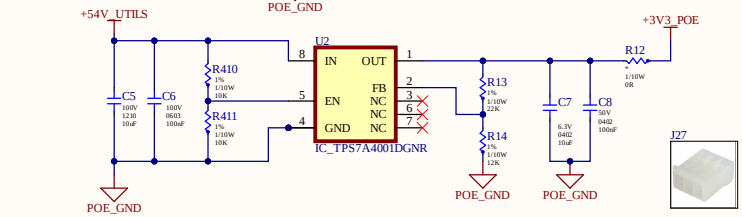


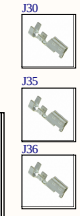


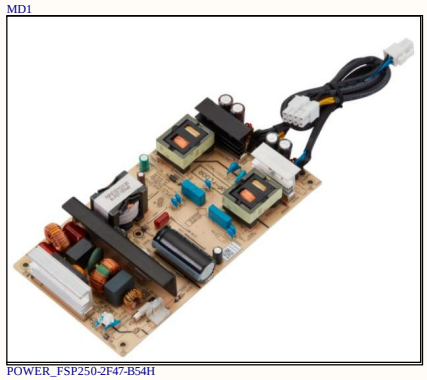


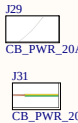












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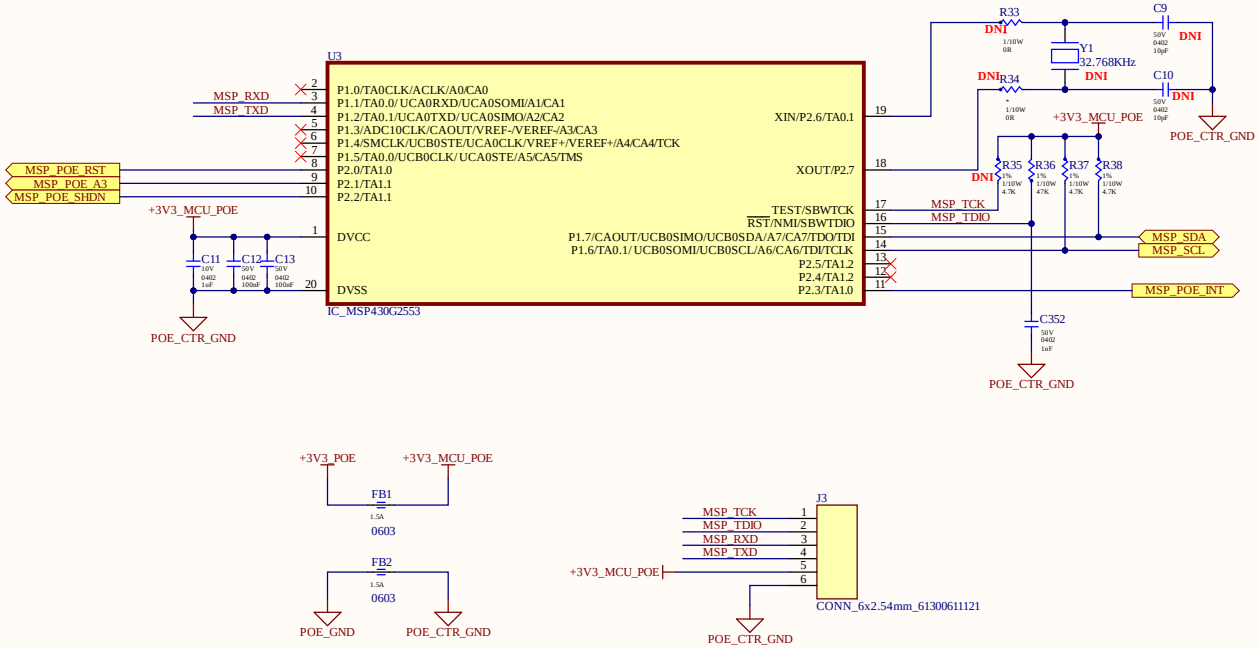
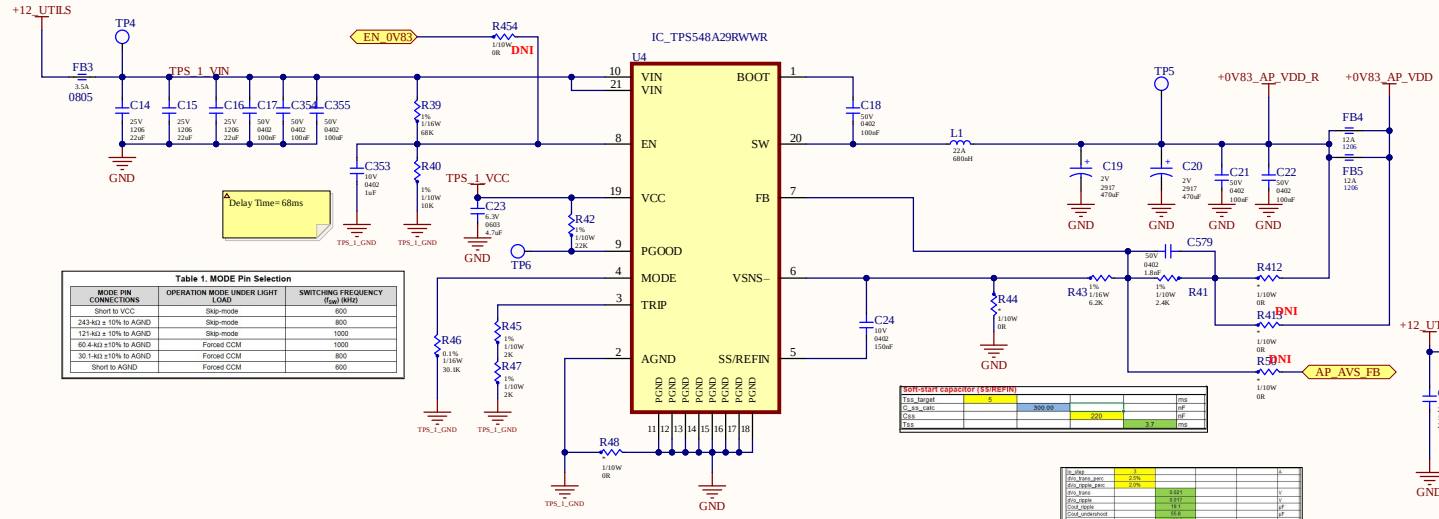
N4-V1.PrjPcb			1.1 ACDC-Converter_PoE.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	6
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			1.2 PoE-Controller.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	7
Design				Number of Sheets	43



PIN	WIRE COLOR	PIN CONN
1	YELLOW	12V
2	YELLOW	12V
3	YELLOW	12V
4	YELLOW	12V
5	BLACK	12V RTN
6	BLACK	12V RTN
7	BLACK	12V RTN
8	BLACK	12V RTN

Table 1. MODE Pin Selection

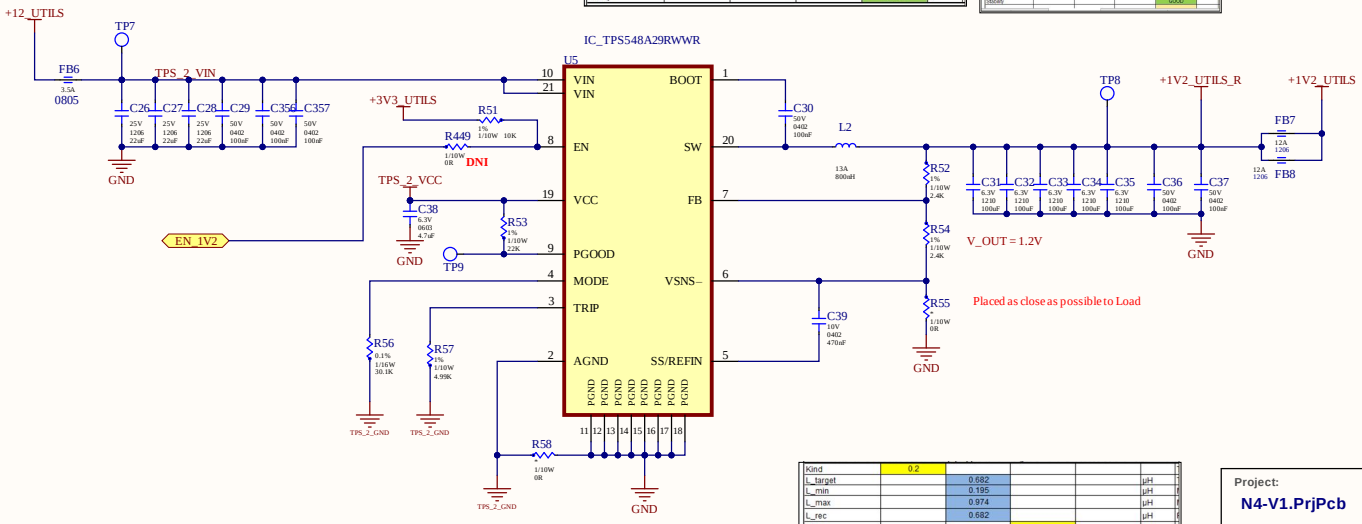
MODE PIN CONNECTIONS	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)
Short to VCC	Skip-mode	600
243-kΩ ± 10% to AGND	Skip-mode	800
121-kΩ ± 10% to AGND	Skip-mode	1000
60.4-kΩ ±10% to AGND	Forced CCM	1000
30.1-kΩ ±10% to AGND	Forced CCM	800
Short to AGND	Forced CCM	600

Soft-start capacitor (SS/REFIN)

Tss_target	5				ms
C_ss_calc		300.00			nF
Css			220		nF
Tss				3.7	ms

Iw_step	1				A
dvo_trans_perc	2.5%				
dVo_ripple_perc	20%				
dvo_trans		0.021			V
dVo_ripple		0.017			V
Cout_ripple		18.1			uF
Cout_undershoot		56.8			uF
Cout_overshoot		156.8			uF
Cout_stability		58.4			uF
Cout_min		155.0			uF
Cout_max		659.6			uF
ESR_trans		6.9			mΩ
ESR_ripple		8.2			mΩ
ESR_max		6.9			mΩ
Cout_single_cer			470		uF
Cer_derating			70%		
ESR_single_cer			2		mΩ
N_cer			2		
Cout_cer				658	uF
ESR_cer				1.0	mΩ
Cout_single_bulk			0.1		uF
Bulk_derating			30%		
ESR_single_bulk			2		mΩ
N_bulk			1		
Cout_bulk				0	uF
ESR_bulk				2.0	mΩ
Cout				658	uF
Vo_undershoot				18	mV
Vo_overshoot				49	mV
Zout_first				1.044	mΩ
Vo_ripple				21	mV
Stability				GOOD	

Kind	0.2				
L_target		0.324			µH
L_min		0.139			µH
L_max		0.694			µH
L_rec		0.324			µH
Lout			0.65		µH
DCR			2.3		mΩ
Tol_L			20%		
Iripple_max				1.870	A
Ipeak				15.935	A
Irms				15.010	A
Iripple_min				1.215	
Ivalley				14.392	A



Kind	0.2				
L_target		0.682			µH
L_min		0.195			µH
L_max		0.974			µH
L_rec		0.682			µH
Lout			0.8		µH
DCR			2.9		mΩ
Tol_L			20%		
Iripple_max				2.131	A
Ipeak				11.065	A
Irms				10.019	A
Iripple_min				1.367	
Ivalley				9.316	A

Project:			Title:		
N4-V1.PrjPcb			1.3 DCDC-Buck-1.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	8
Design				Number of Sheets	43

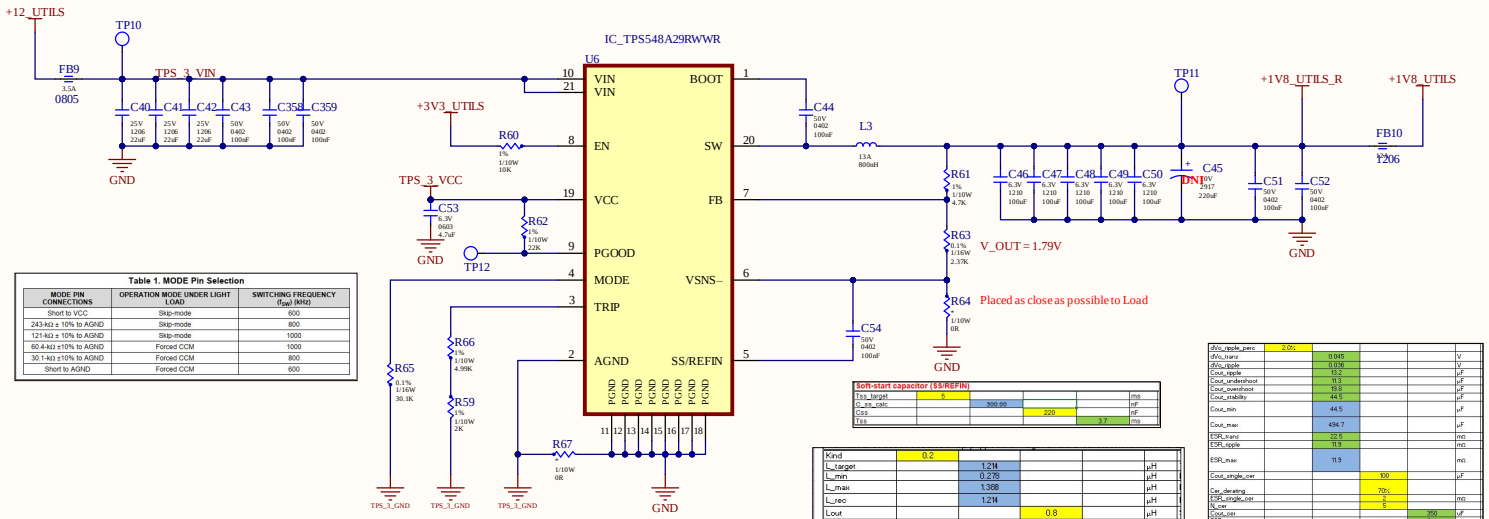


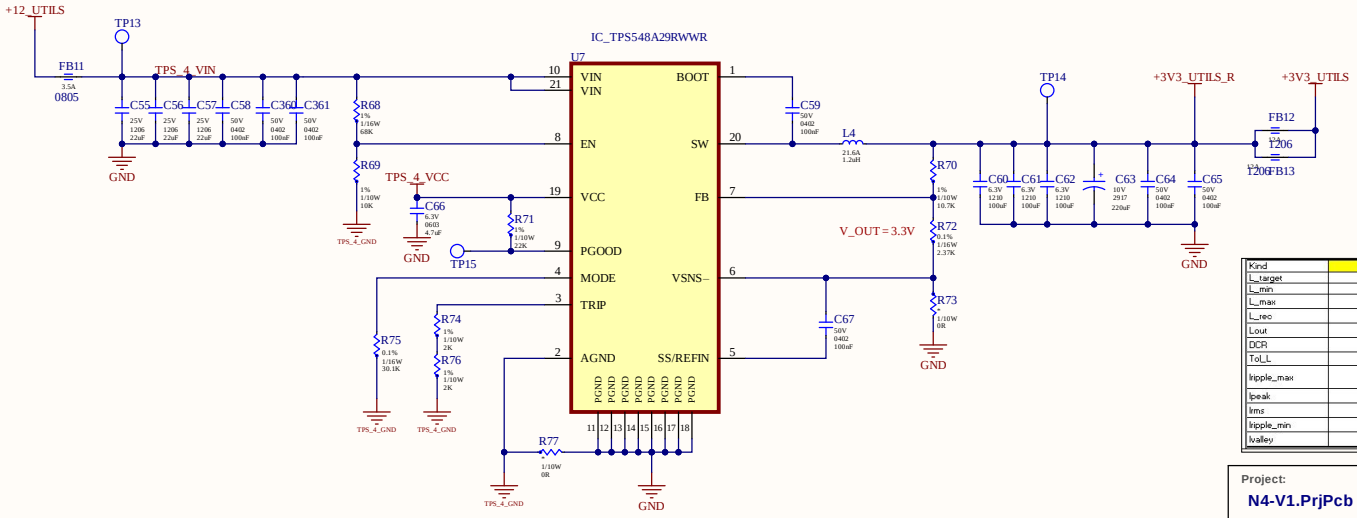
Table 1. MODE Pin Selection

MODE PIN CONNECTIONS	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)
Short to VCC	Skip-mode	600
243-kΩ ± 10% to AGND	Skip-mode	800
121-kΩ ± 10% to AGND	Skip-mode	1000
60.4-kΩ ±10% to AGND	Forced CCM	1000
30.1-kΩ ±10% to AGND	Forced CCM	800
Short to AGND	Forced CCM	600

Soft-start capacitor (SS/REFIN)					
Tss_target	5				ms
C_ss_calc		300.00			nF
Css			220		nF
Tss				3.7	ms

Kind	0.2				
L_target		1.214			µH
L_min		0.278			µH
L_max		1.388			µH
L_rec		1.214			µH
Lout			0.8		µH
DCR			2.9		mΩ
Tol_L			20%		
Iripple_max				3.036	A
Ipeak				3.518	A
Irms				8.048	A
Iripple_min				1.904	
Ivalley				7.048	A

dVo_ripple_perc	2.0%				
dVo_tranz		0.045			V
dVo_ripple		0.036			V
Cout_ripple		13.2			µF
Cout_undershoot		11.3			µF
Cout_overshoot		15.8			µF
Cout_stability		44.5			µF
Cout_min		44.5			µF
Cout_max		494.7			µF
ESR_tranz		22.5			mΩ
ESR_ripple		11.3			mΩ
ESR_max		11.3			mΩ
Cout_single_cer			100		µF
Cer_derating			70%		
ESR_single_cer			2		mΩ
N_cer			5		
Cout_cer				350	µF
ESR_cer				0.4	mΩ
Cout_single_bulk			0.1		µF
Bulk_derating			30%		
ESR_single_bulk			2		mΩ
N_bulk			1		
Cout_bulk				0	µF
ESR_bulk				2.0	mΩ
Cout				350	uF
Vo_undershoot				1.5	mV
Vo_overshoot				2.5	mV
Zout_tzw				0.695	mΩ
Vo_ripple				2.1	mV
Stability				GOOD	



Kind	0.2				
L_target		1.289			µH
L_min		0.442			µH
L_max		2.210			µH
L_rec		1.289			µH
Lout			1.2		µH
DCR			2.9		mΩ
Tol_L			20%		
Iripple_max				3.223	A
Ipeak				13.611	A
Irms				12.036	A
Iripple_min				1.880	
Ivalley				11.060	A

dVo_ripple_perc	2.0%				
dVo_tranz		0.083			V
dVo_ripple		0.056			V
Cout_ripple		7.0			µF
Cout_undershoot		9.5			µF
Cout_overshoot		8.8			µF
Cout_stability		29.7			µF
Cout_min		29.7			µF
Cout_max		329.8			µF
ESR_tranz		41.3			mΩ
ESR_ripple		20.5			mΩ
ESR_max		20.5			mΩ
Cout_single_cer			100		µF
Cer_derating			70%		
ESR_single_cer			2		mΩ
N_cer			5		
Cout_cer				350	uF
ESR_cer				0.4	mΩ
Cout_single_bulk			0.1		uF
Bulk_derating			30%		
ESR_single_bulk			2		mΩ
N_bulk			1		
Cout_bulk				0	µF
ESR_bulk				2.0	mΩ
Cout				350	uF
Vo_undershoot				2.2	mV
Vo_overshoot				3.1	mV
Zout_tzw				0.695	mΩ
Vo_ripple				2.2	mV
Stability				GOOD	

Project:			Title:		
N4-V1.PrjPcb			1.4 DCDC-Buck-2.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	9
Design				Number of Sheets	43

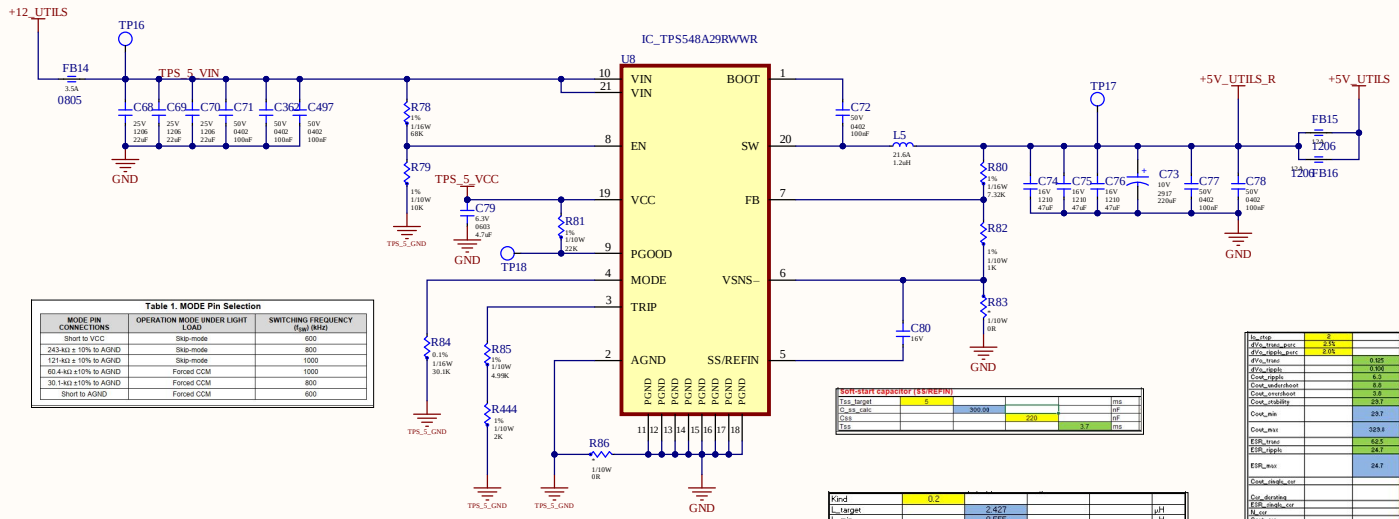


Table 1. MODE Pin Selection

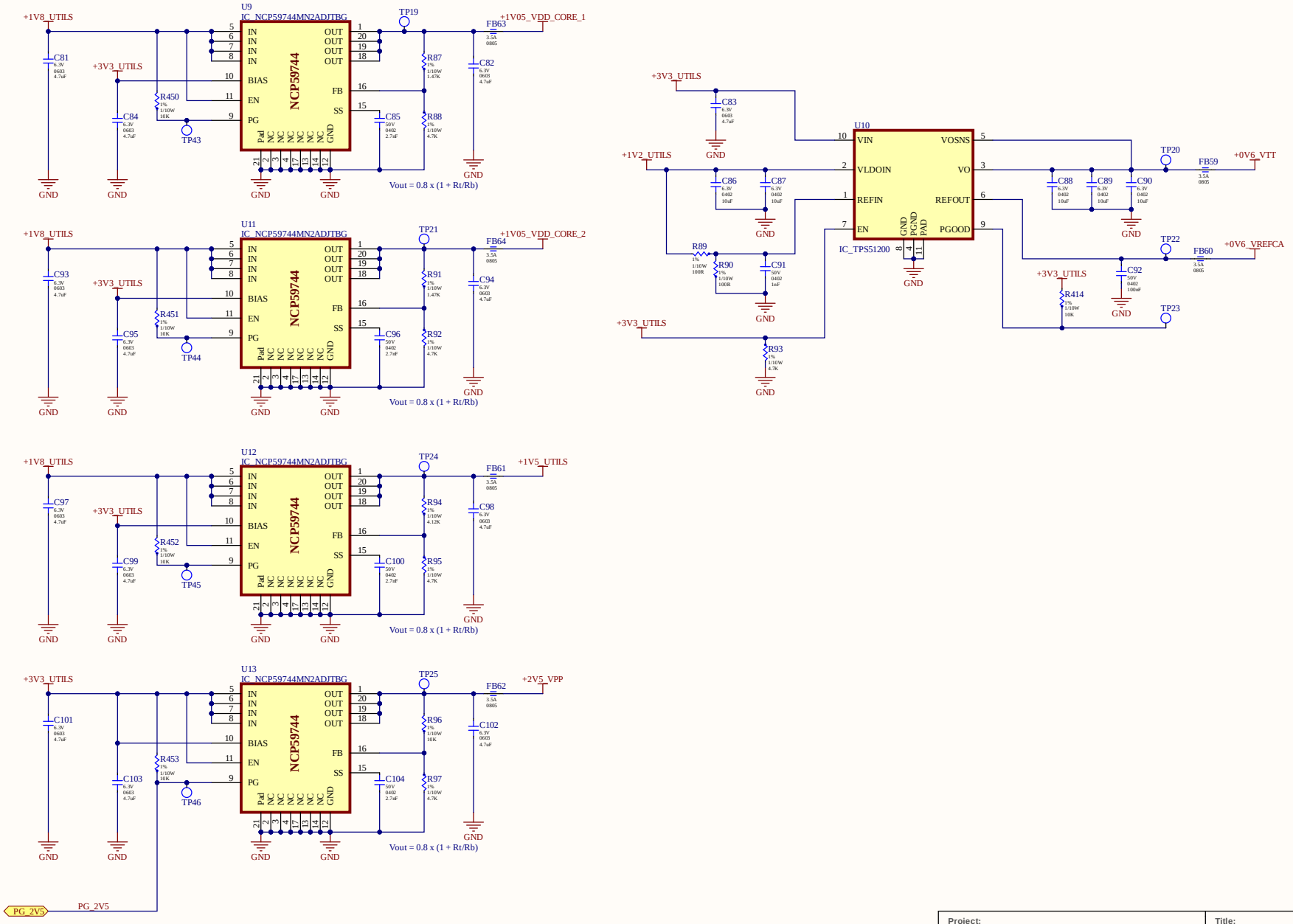
MODE PIN CONNECTIONS	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)
Short to VCC	Skip-mode	600
243-kΩ ± 10% to AGND	Skip-mode	800
121-kΩ ± 10% to AGND	Skip-mode	1000
60.4-kΩ ±10% to AGND	Forced CCM	1000
30.1-kΩ ±10% to AGND	Forced CCM	800
Short to AGND	Forced CCM	600

Soft-start capacitor (SS/REFIN)					
Tss_target	5				ms
C_ss_calc		300.00			nF
Css			220		nF
Tss				3.7	ms

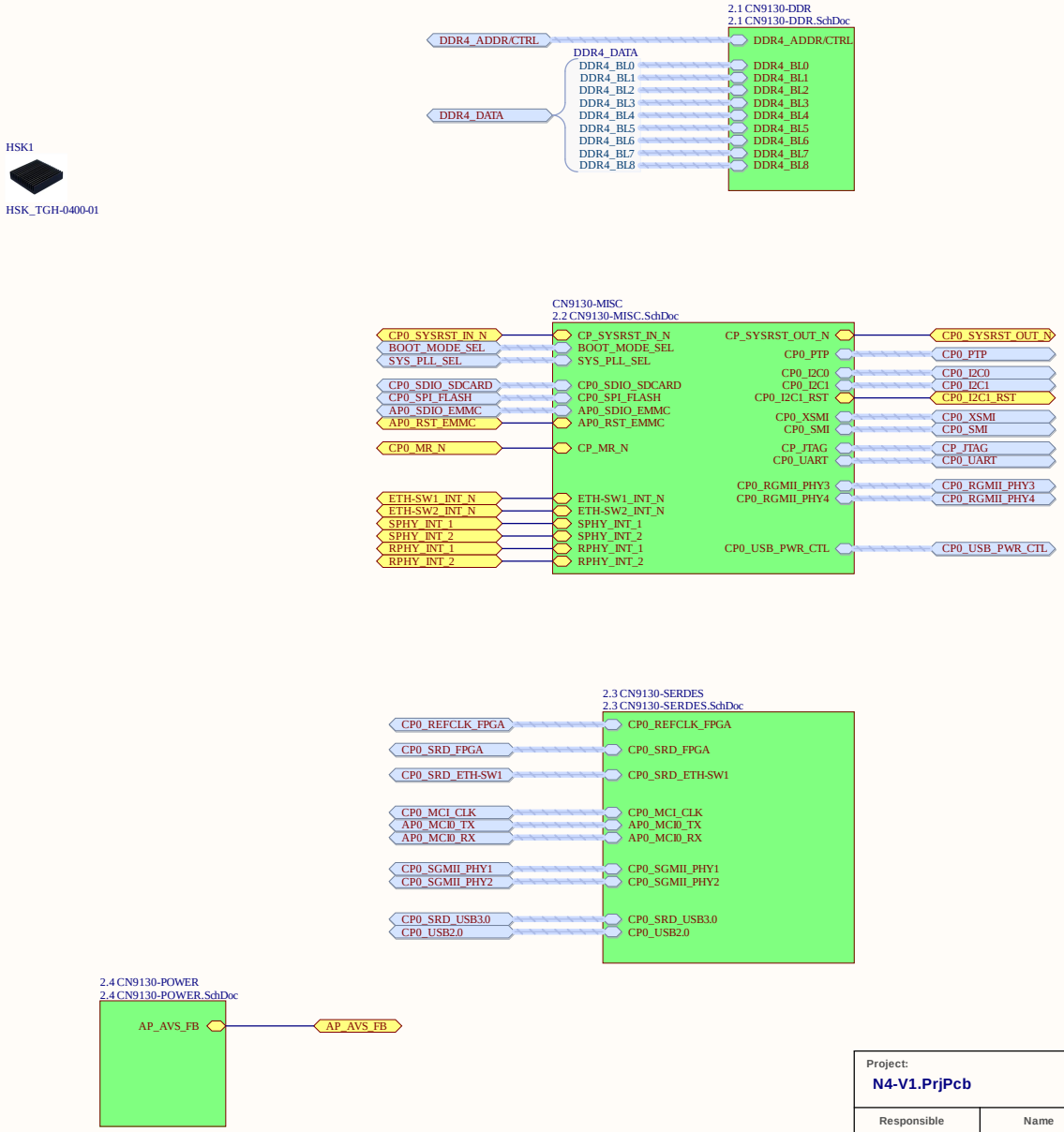
Kind	0.2				
L_target		2.427			µH
L_min		0.555			µH
L_max		2.773			µH
L_rec		2.427			µH
Lout			1.2		µH
DCR			2.9		mΩ
Tol_L			20%		
Ripple_max				4.044	A
Ipeak				10.022	A
Irms				8.085	A
Ripple_min				2.080	A
Ivalley				6.960	A

Io_step	5				A
dVo_transi_perc	2.5%				
dVo_ripple_perc	0.5%				
dVo_transi		0.125			V
dVo_ripple		0.100			V
Cout_ripple		6.3			µF
Cout_undershoot		8.8			µF
Cout_overshoot		3.5			µF
Cout_stability		23.7			µF
Cout_min		23.7			µF
Cout_max		325.8			µF
ESR_transi		62.5			mΩ
ESR_ripple		24.7			mΩ
ESR_max		24.7			mΩ
Cout_ripple_cer			100		µF
Cor_derating			70%		
ESR_ripple_cer			2		mΩ
N_cer			5		
Cout_cer				350	µF
ESR_cer				0.4	mΩ
Cout_ripple_bulk			0.1		µF
Bulk_derating			30%		
ESR_ripple_bulk			8		mΩ
N_bulk			1		
Cout_bulk				0	µF
ESR_bulk				8.0	mΩ
Cout				350	µF
Vo_undershoot				3.2	mV
Vo_overshoot				1.4	mV
Zout_tow				0.635	mΩ
Vo_ripple				2.8	mV
Stability				GOOD	
f_LC				1.6	kHz
f_ESR_cer				1136.8	kHz
f_ESR_bulk				804194.1	kHz

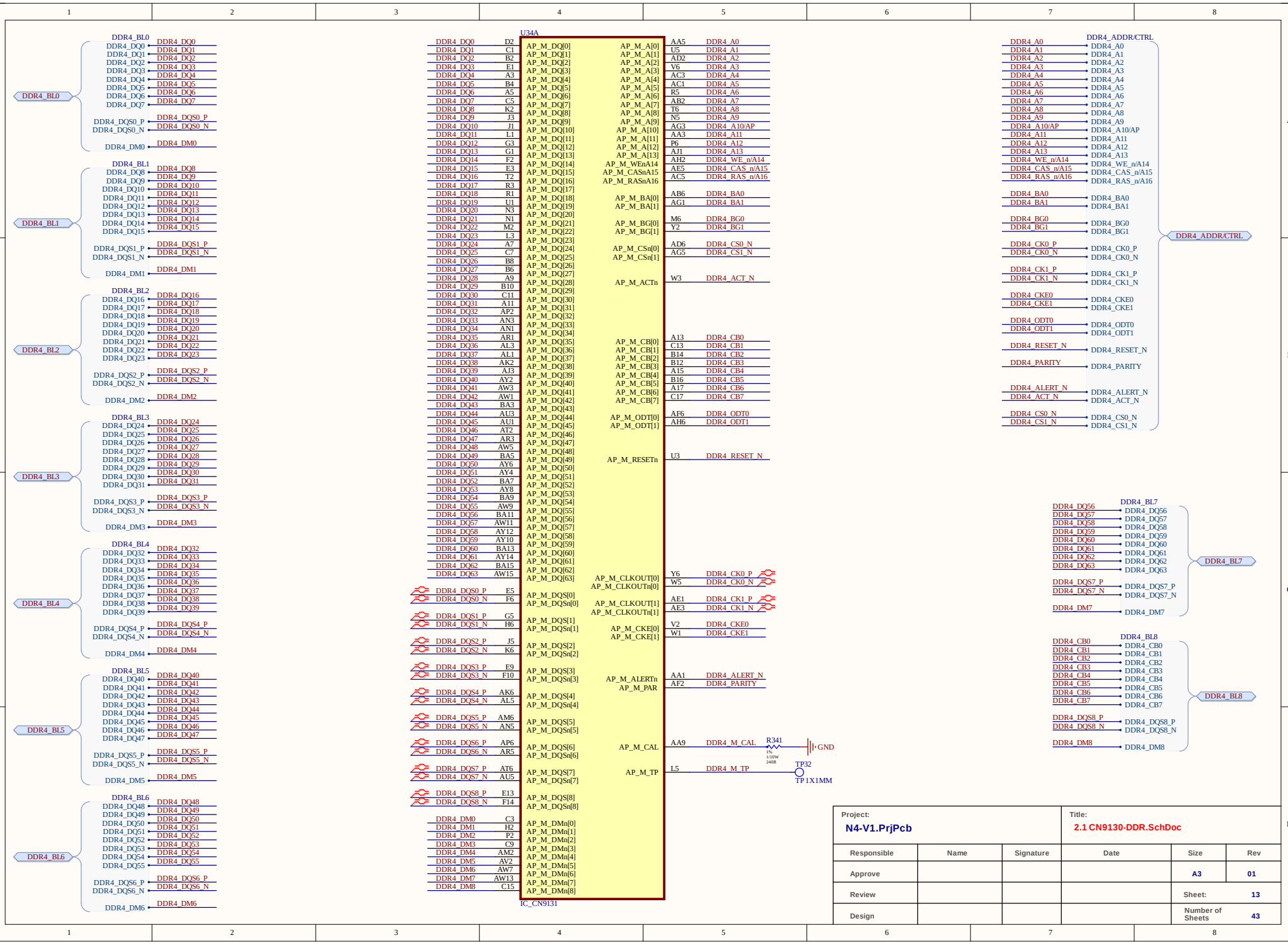
Project:			Title:		
N4-V1.PrjPcb			1.5 DCDC-Buck-3.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	10
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			1.6 DCDC-LDO.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	11
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			2 CN9130.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	12
Design				Number of Sheets	43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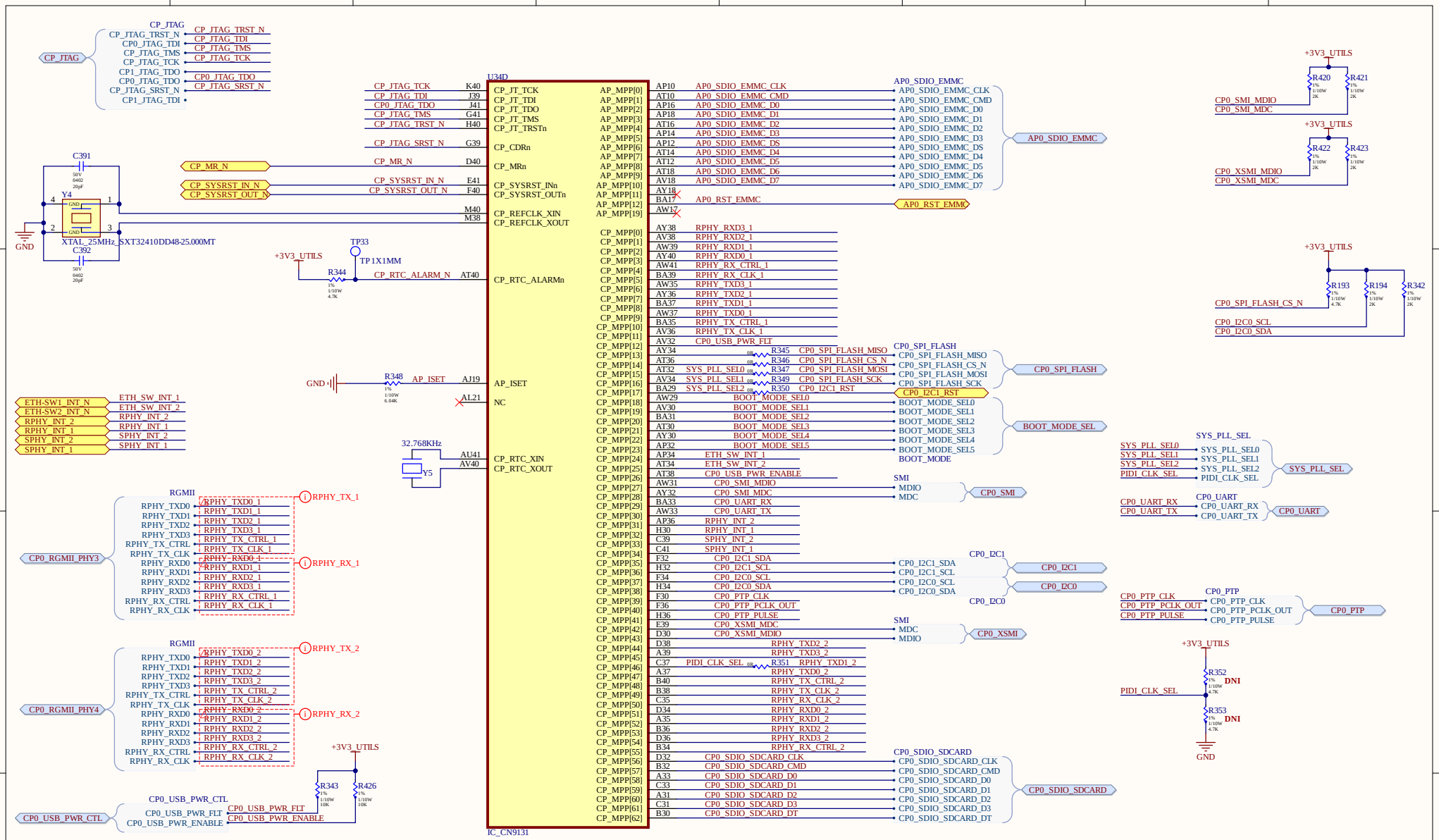
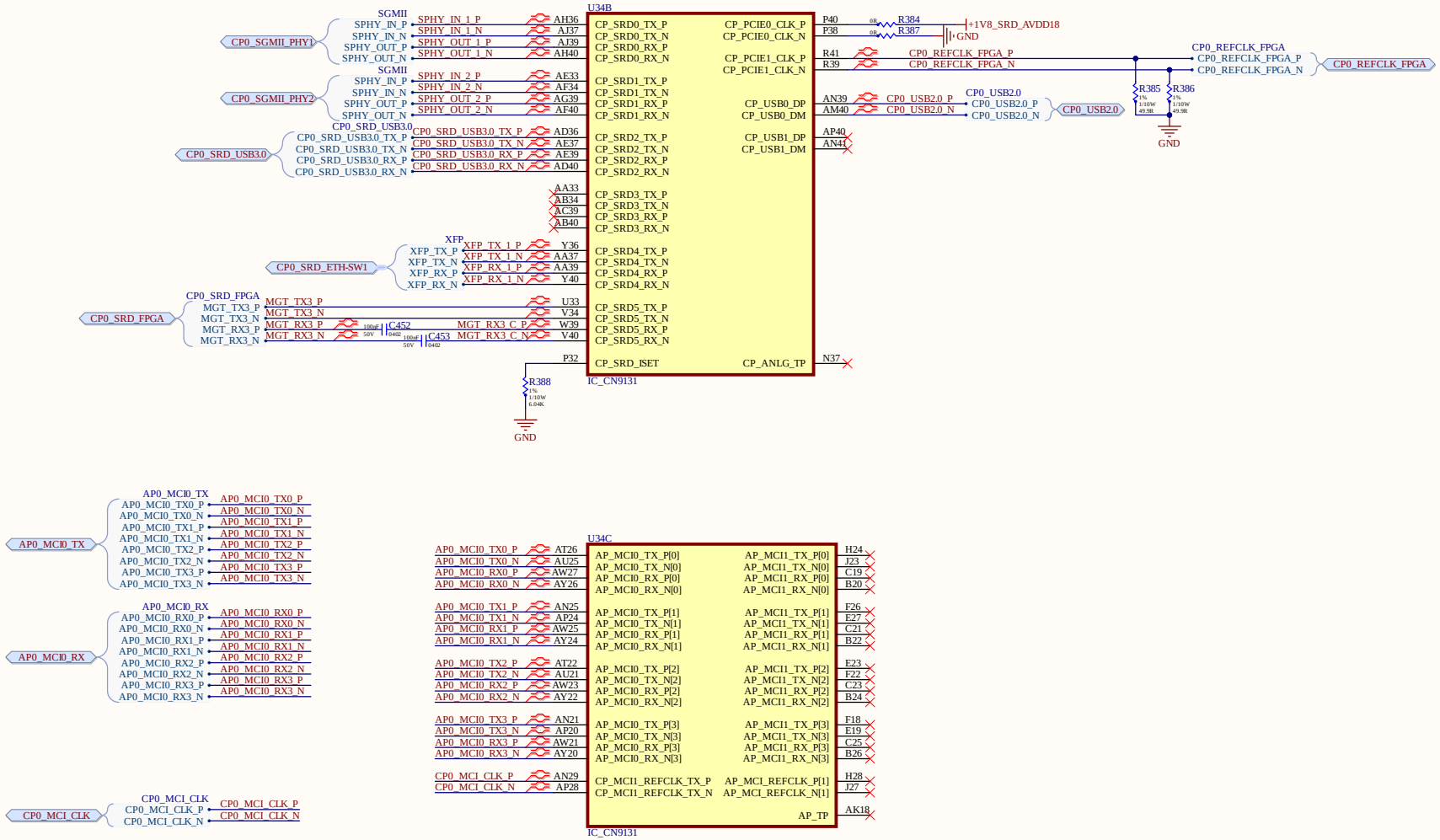
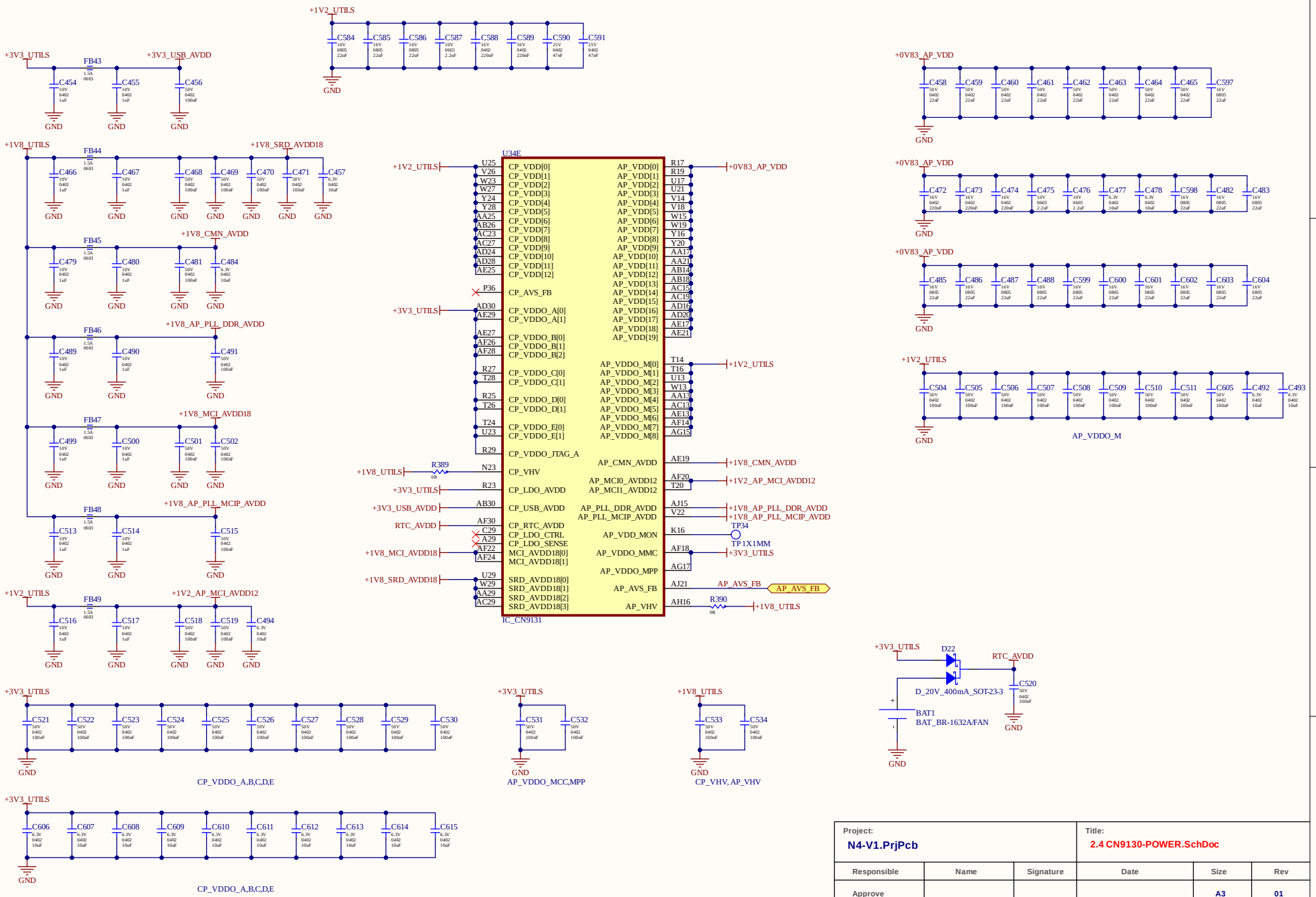
DDR4_BL2
DDR4_BL3
DDR4_BL4
DDR4_BL5
DDR4_BL6
DDR4_ADDR/CTRL
DDR4_BL7
DDR4_BL8
R341
1%
1/10W
240R
GND
TP32
TP 1X1MM
Project:
N4-V1.PrjPcb
Title:
2.1 CN9130-DDR.SchDoc
Responsible
Name
Signature
Date
Size
Rev
Approve
A3
01
Review
Sheet:
13
Design
Number of Sheets
43



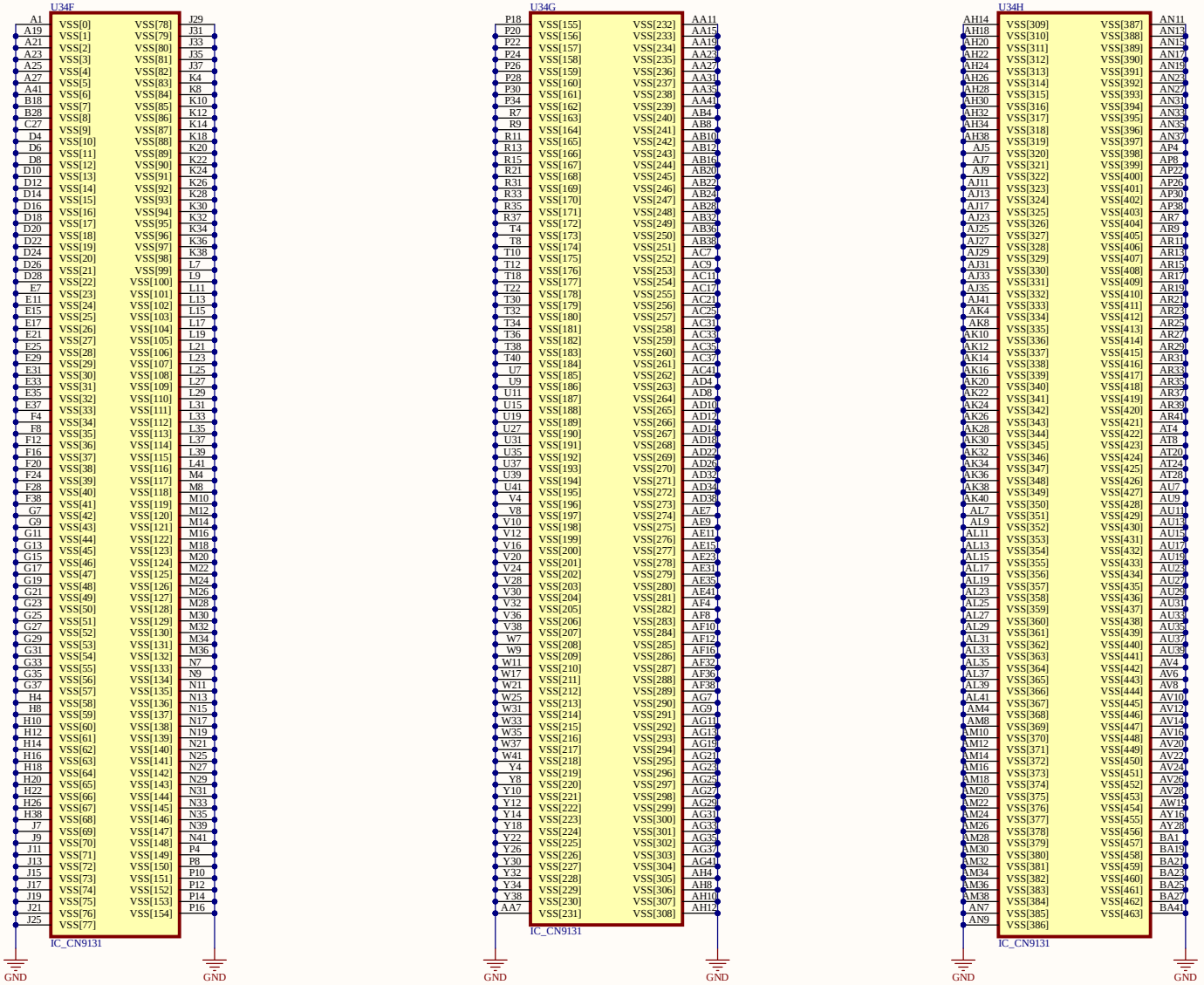
Project:			Title:		
N4-V1.PrjPcb			2.2 CN9130-MISC.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	14
Design				Number of Sheets	43



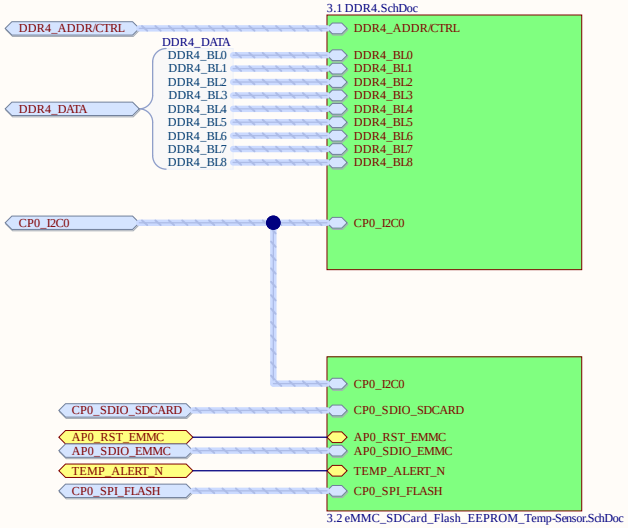
Project:			Title:		
N4-V1.PrjPcb			2.3 CN9130-SERDES.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	15
Design				Number of Sheets	43



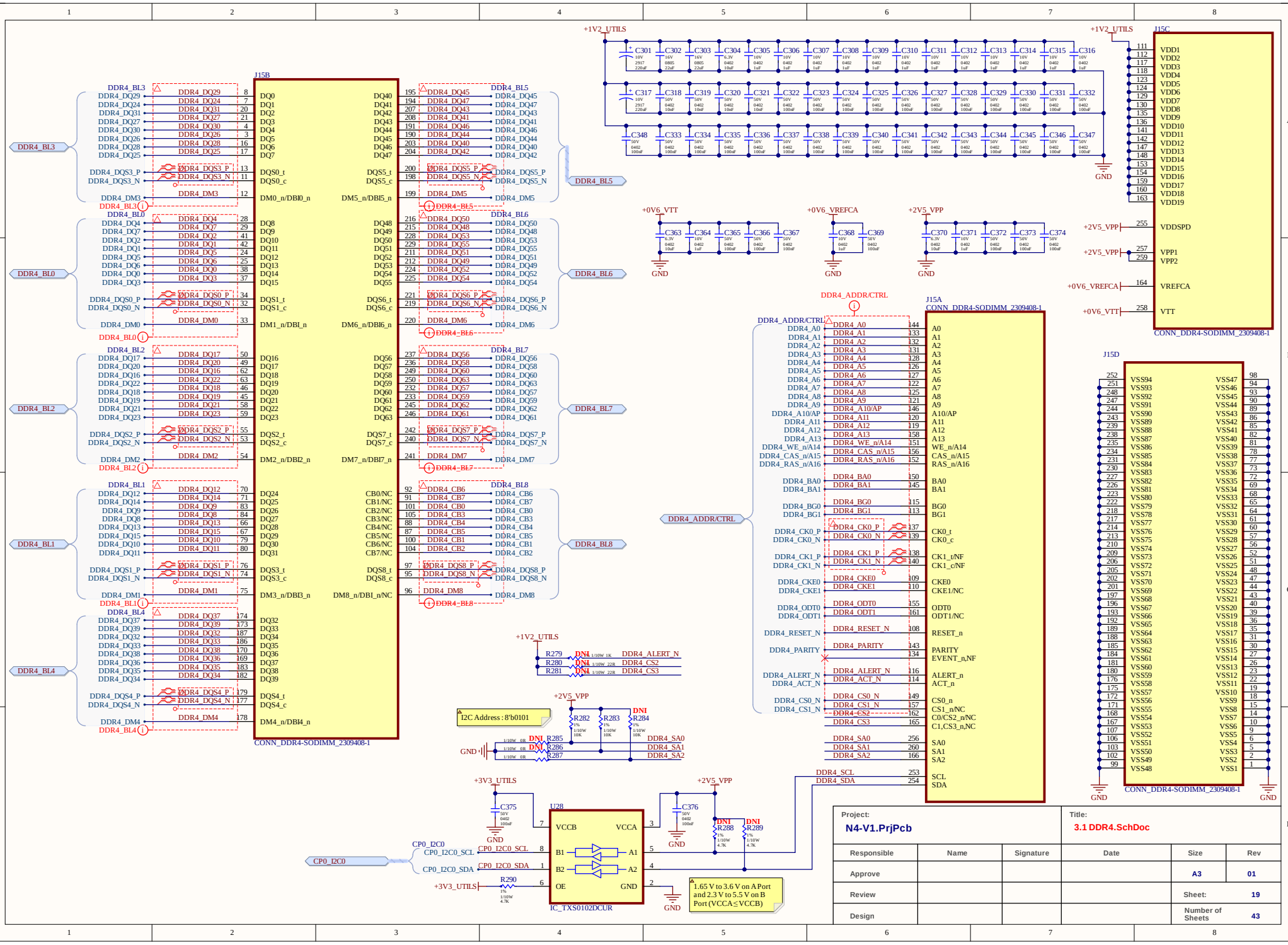
Project:			Title:		
N4-V1.PrjPcb			2.4 CN9130-POWER.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	16
Design				Number of Sheets	43

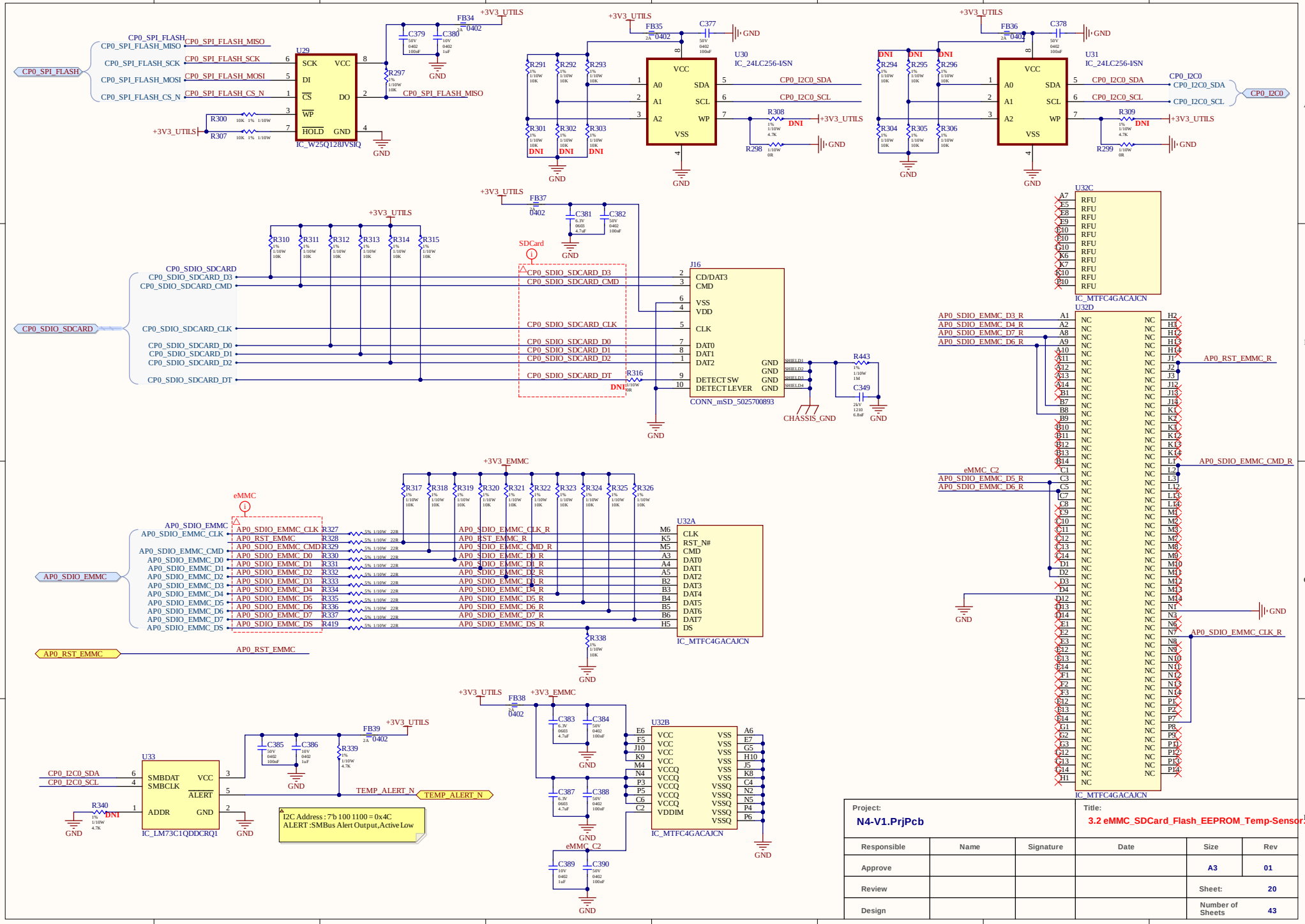


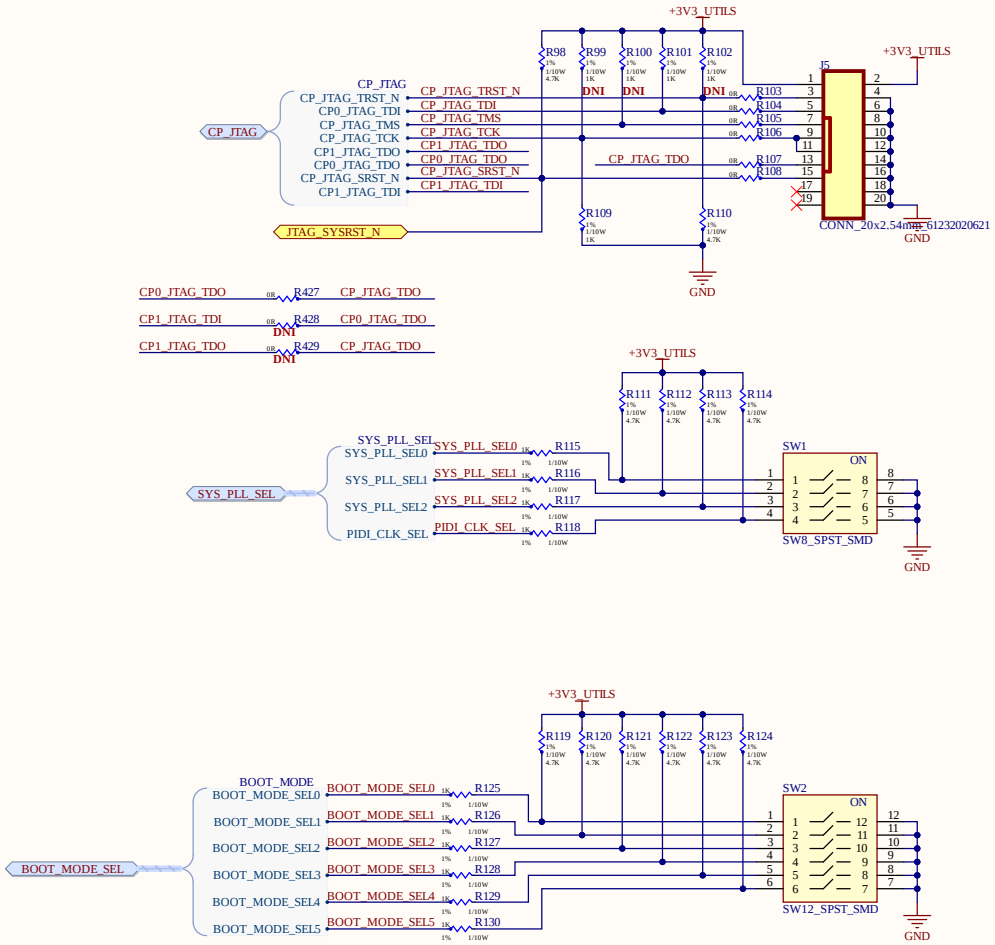
Project:			Title:		
N4-V1.PrjPcb			2.5 CN9130-GND.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	17
Design				Number of Sheets	43



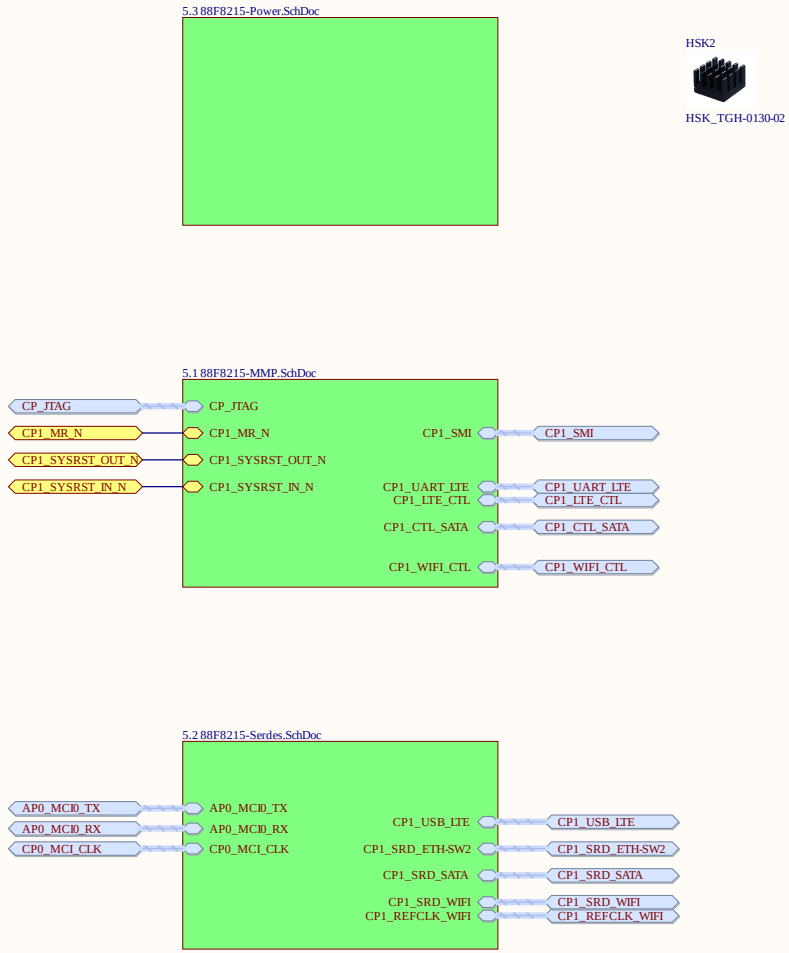
Project:			Title:		
N4-V1.PrjPcb			3 Memory.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	18
Design				Number of Sheets	43


J15B
CONN_DDR4-SODIMM_2309408-1
J15A
CONN_DDR4-SODIMM_2309408-1
J15C
CONN_DDR4-SODIMM_2309408-1
J15D
CONN_DDR4-SODIMM_2309408-1
U28
IC_TXS0102DCUR
+1V2_UTILS
+0V6_VTT
+0V6_VREFCA
+2V5_VPP
+3V3_UTILS
GND
DDR4_ADDR/CTRL
CP0_I2C0
I2C Address : 8'b0101
1.65 V to 3.6 V on A Port and 2.3 V to 5.5 V on B Port (VCCA≤VCCB)
Project:
N4-V1.PrjPcb
Title:
3.1 DDR4.SchDoc
Responsible
Name
Signature
Date
Size
Rev
Approve
A3
01
Review
Sheet:
19
Design
Number of Sheets
43

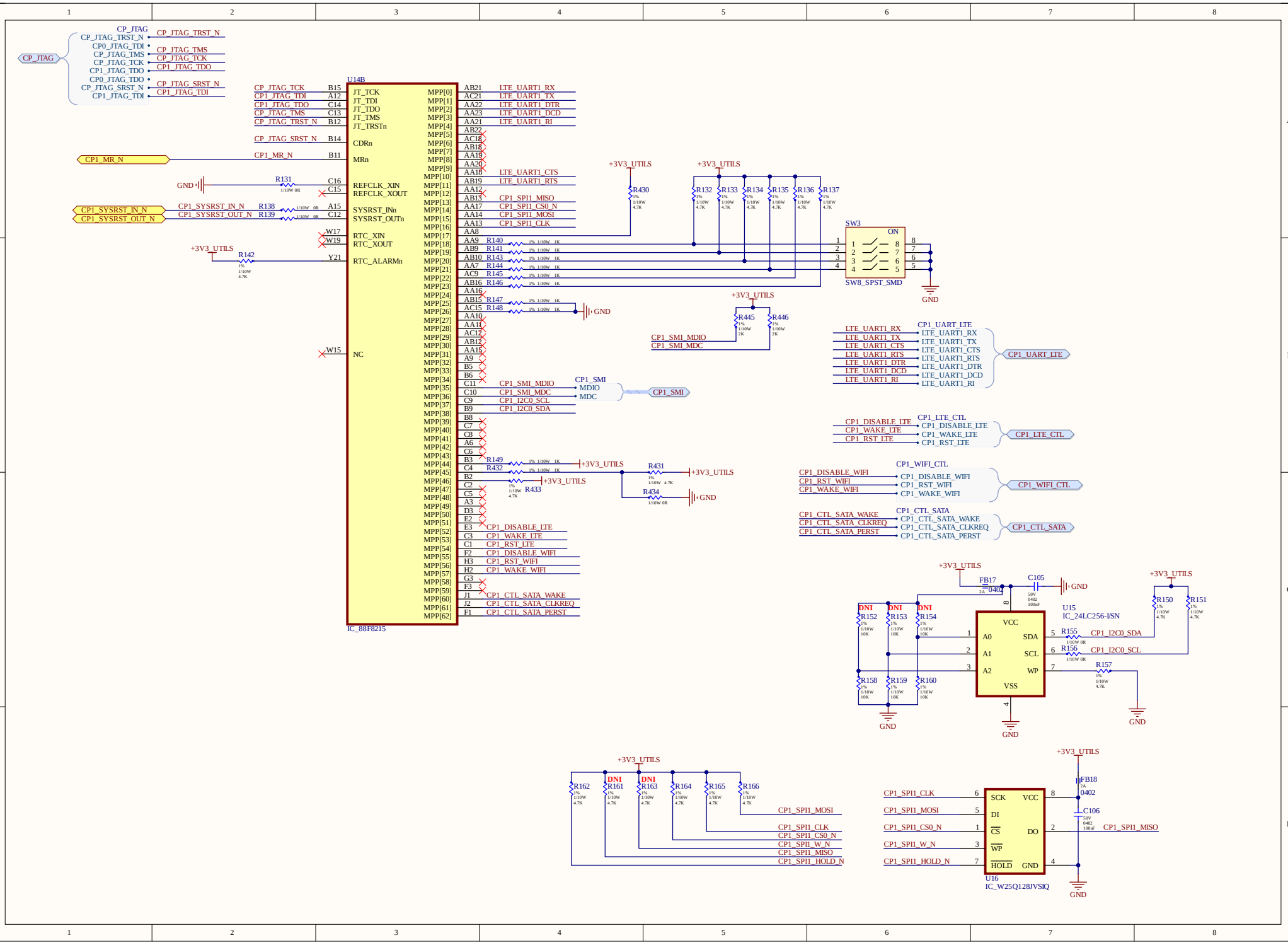

U29
IC_W25Q128JVSIQ
U30
IC_24LC256-I/SN
U31
IC_24LC256-I/SN
U32C
IC_MTFC4GACAJCN
U32D
IC_MTFC4GACAJCN
J16
CONN_mSD_5025700893
U32A
IC_MTFC4GACAJCN
U32B
IC_MTFC4GACAJCN
U33
IC_LM73C1QDDCRQ1
I2C Address : 7'b 100 1100 = 0x4C
ALERT :SMBus Alert Output,Active Low
Project:
N4-V1.PrjPcb
Title:
3.2 eMMC_SDCard_Flash_EEPROM_Temp-Sensor.SchDoc
Responsible
Name
Signature
Date
Size
Rev
Approve
A3
01
Review
Sheet:
20
Design
Number of Sheets
43

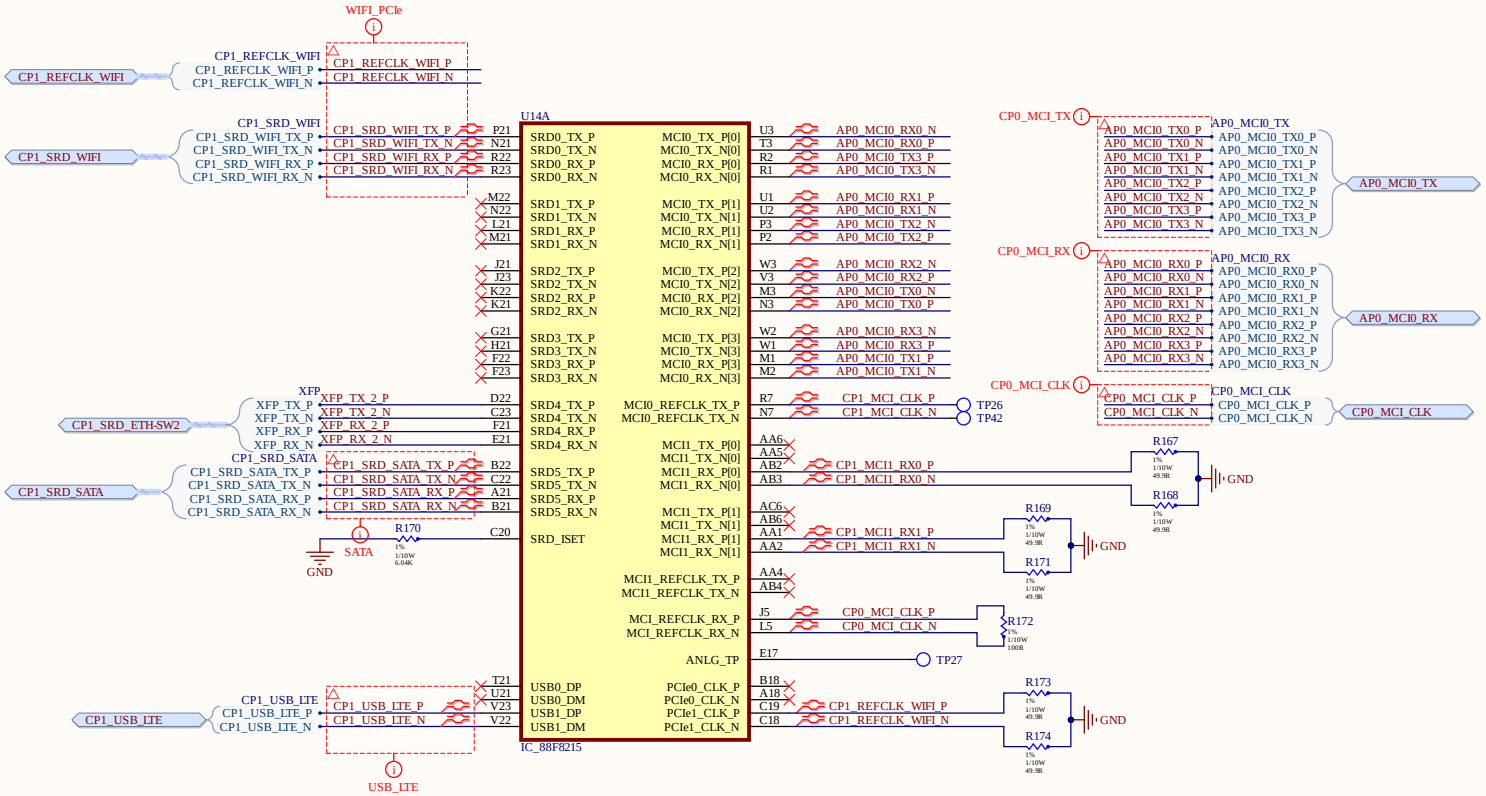


Project:			Title:		
N4-V1.PrjPcb			4 CN9130 JTAG_Config.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	21
Design				Number of Sheets	43

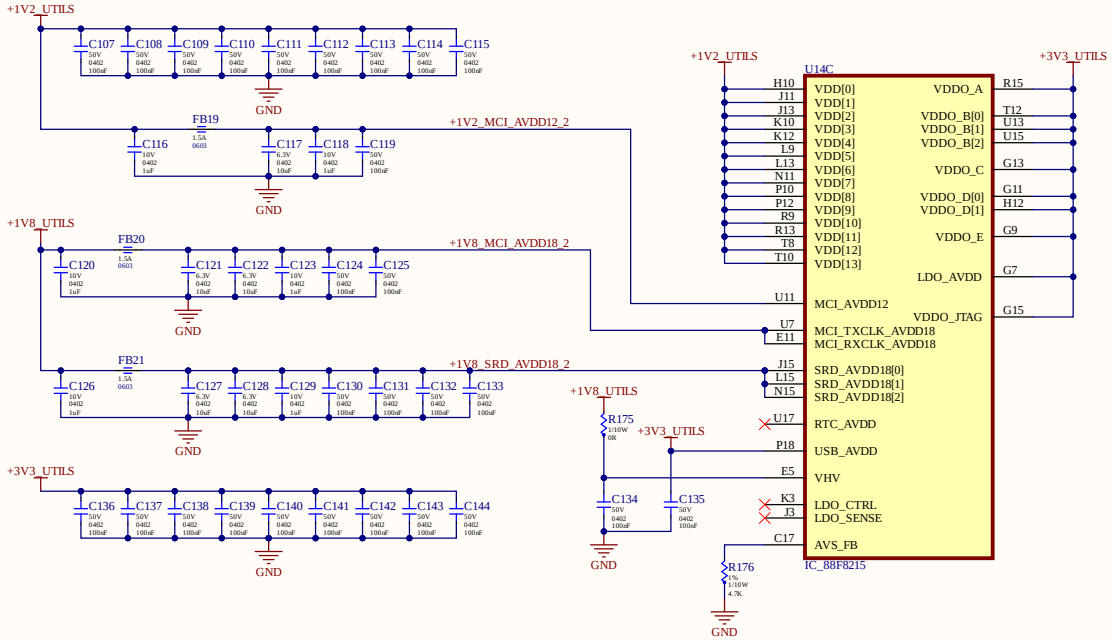


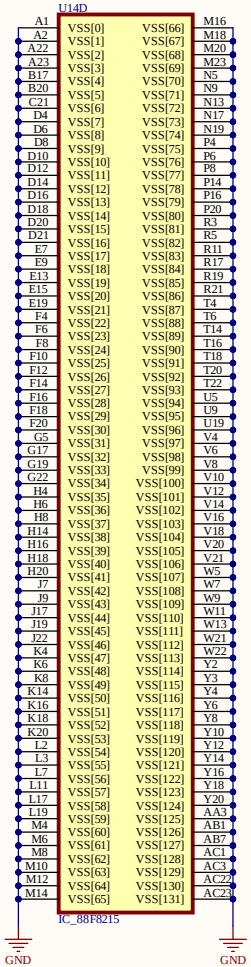
Project:			Title:		
N4-V1.PrjPcb			5 88F8215.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	22
Design				Number of Sheets	43


CP_JTAG
CP_JTAG_TRST_N
CP0_JTAG_TDI
CP_JTAG_TMS
CP_JTAG_TCK
CP1_JTAG_TDO
CP0_JTAG_TDO
CP_JTAG_SRST_N
CP1_JTAG_TDI
U14B
IC_88F8215
JT_TCK
JT_TDI
JT_TDO
JT_TMS
JT_TRSTn
CDRn
MRn
REFCLK_XIN
REFCLK_XOUT
SYSRST_INn
SYSRST_OUTn
RTC_XIN
RTC_XOUT
RTC_ALARMn
NC
CP1_MR_N
CP1_SYSRST_IN_N
CP1_SYSRST_OUT_N
GND
+3V3_UTILS
LTE_UART1_RX
LTE_UART1_TX
LTE_UART1_DTR
LTE_UART1_DCD
LTE_UART1_RI
LTE_UART1_CTS
LTE_UART1_RTS
CP1_SPI1_MISO
CP1_SPI1_CS0_N
CP1_SPI1_MOSI
CP1_SPI1_CLK
CP1_SMI_MDIO
CP1_SMI_MDC
CP1_I2C0_SCL
CP1_I2C0_SDA
CP1_DISABLE_LTE
CP1_WAKE_LTE
CP1_RST_LTE
CP1_DISABLE_WIFI
CP1_RST_WIFI
CP1_WAKE_WIFI
CP1_CTL_SATA_WAKE
CP1_CTL_SATA_CLKREQ
CP1_CTL_SATA_PERST
SW3
SW8_SPST_SMD
CP1_UART_LTE
CP1_LTE_CTL
CP1_WIFI_CTL
CP1_CTL_SATA
CP1_SMI
U15
IC_24LC256-I/SN
VCC
A0
A1
A2
VSS
SDA
SCL
WP
U16
IC_W25Q128JVSIQ
SCK
DI
CS
WP
HOLD
DO
FB17
FB18
C105
C106
DNI

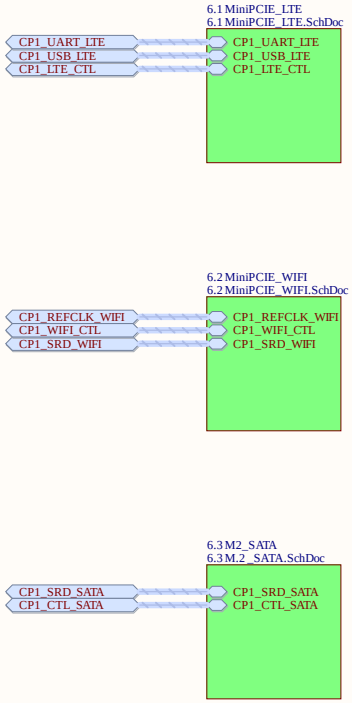


Project:			Title:		
N4-V1.PrjPcb			5.2 88F8215-Serdes.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	24
Design				Number of Sheets	43

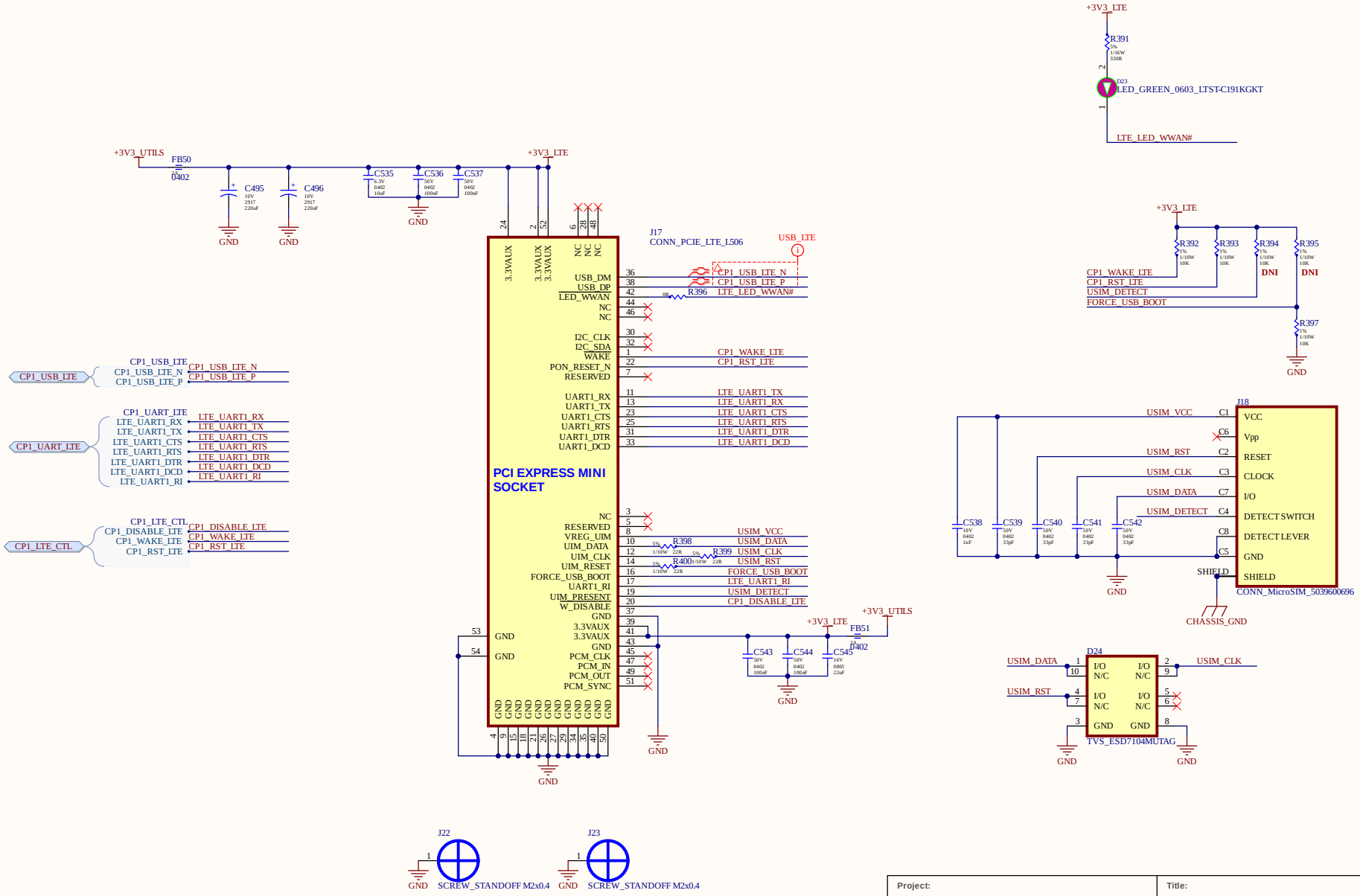




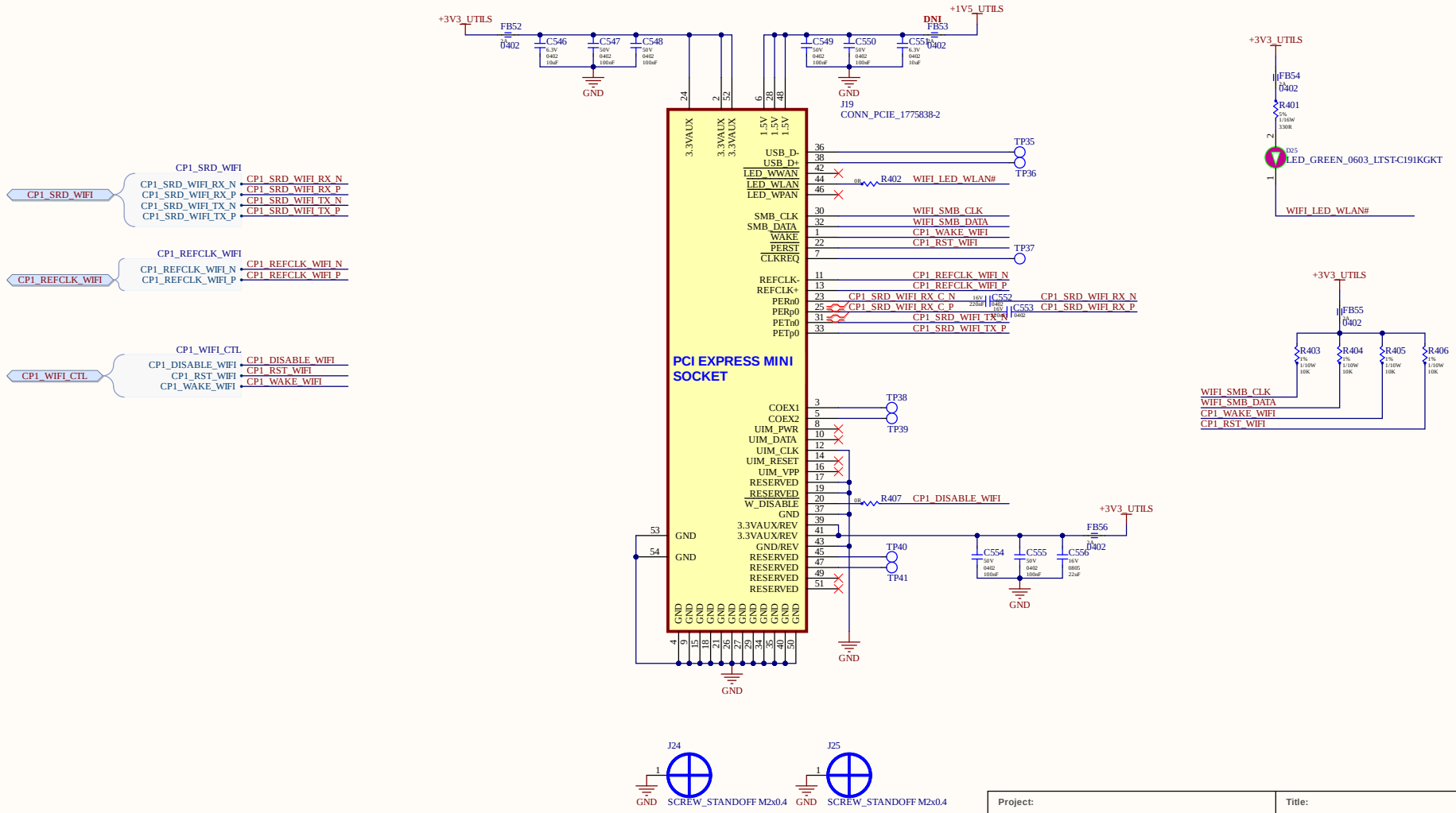
Project:			Title:		
N4-V1.PrjPcb			5.3 88F8215-Power.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	25
Design				Number of Sheets	43



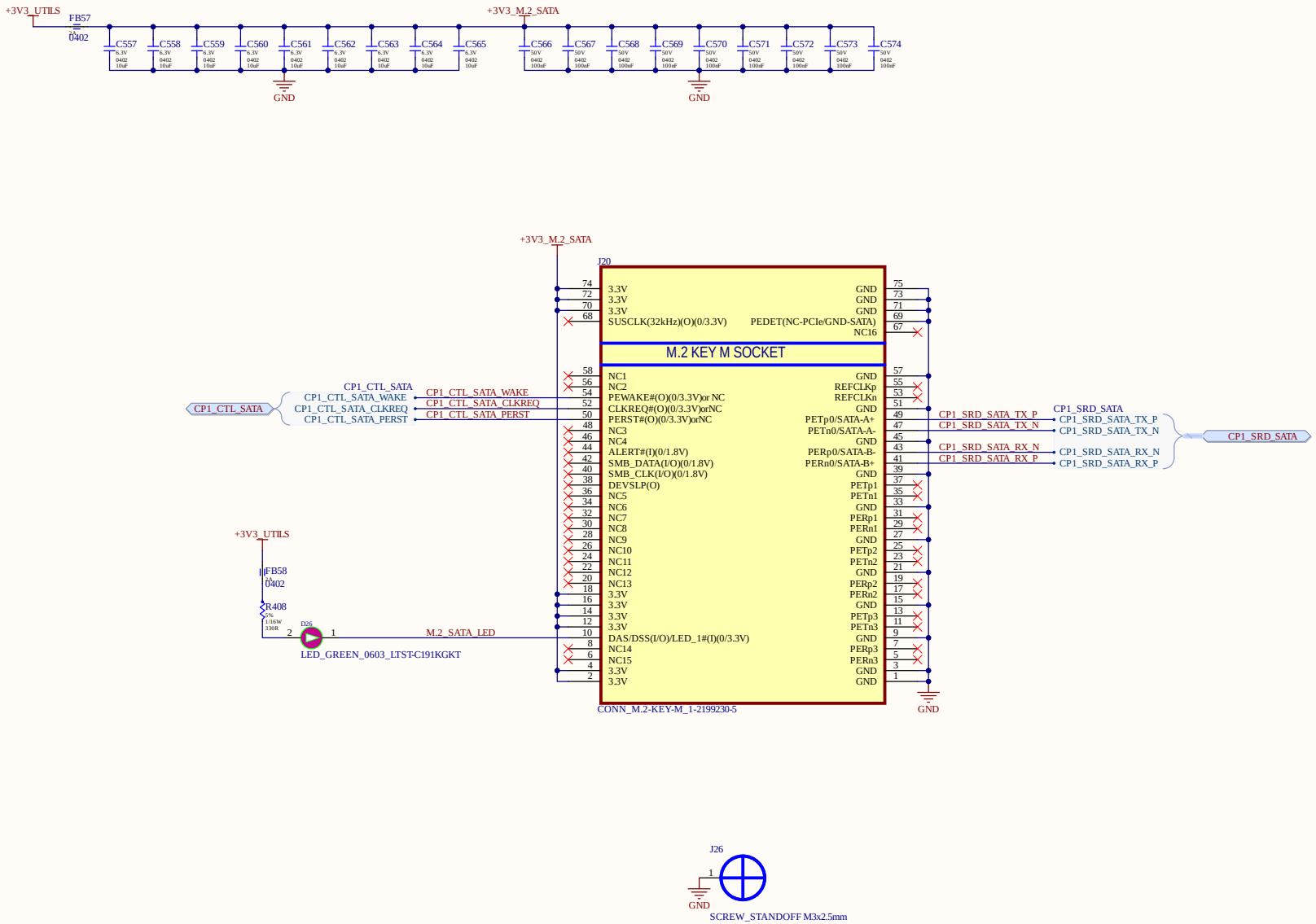
Project:			Title:		
N4-V1.PrjPcb			6 LTE_WIFI_SATA.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	26
Design				Number of Sheets	43



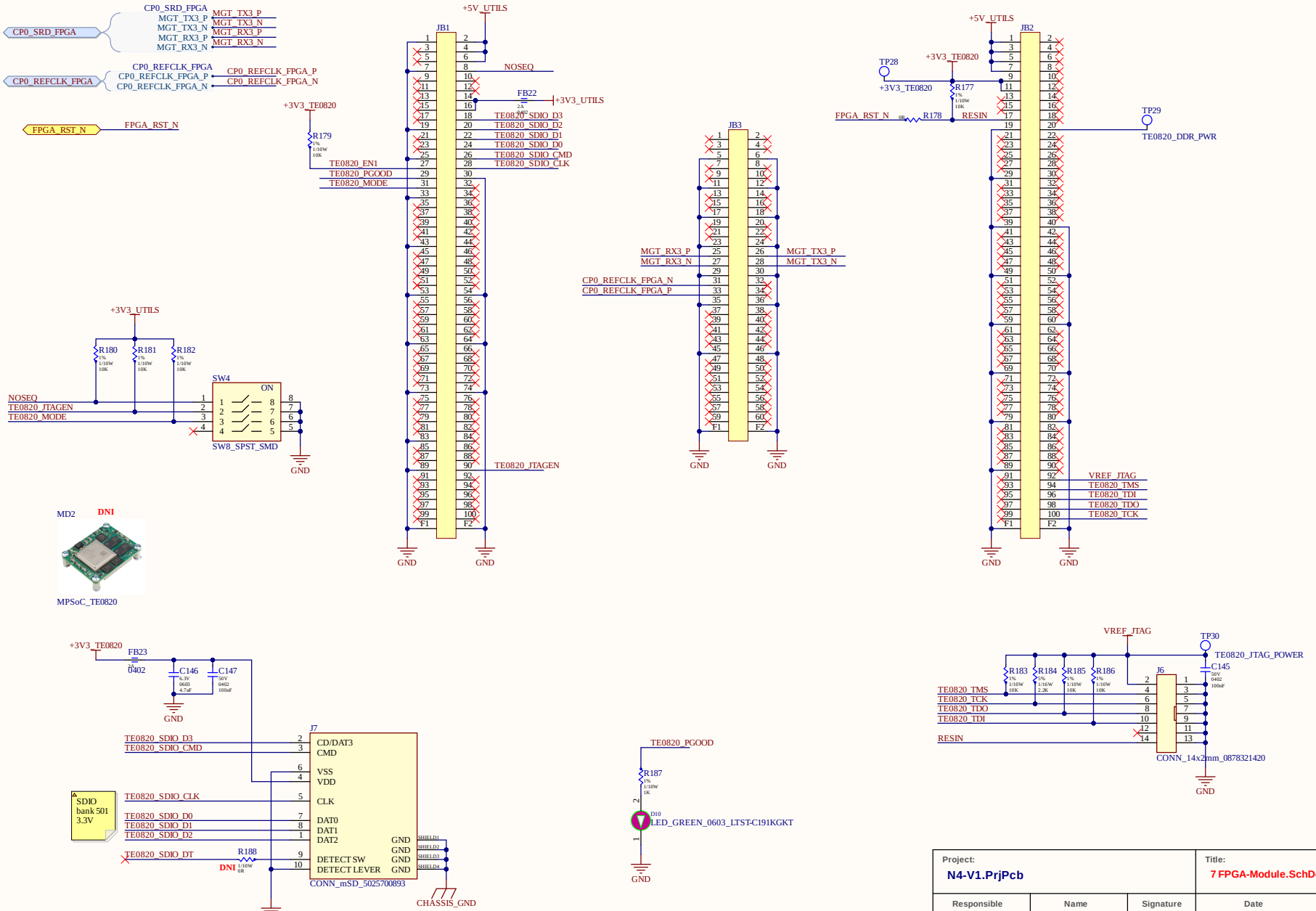
Project:			Title:		
N4-V1.PrjPcb			6.1 MiniPCIE_LTE.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	27
Design				Number of Sheets	43



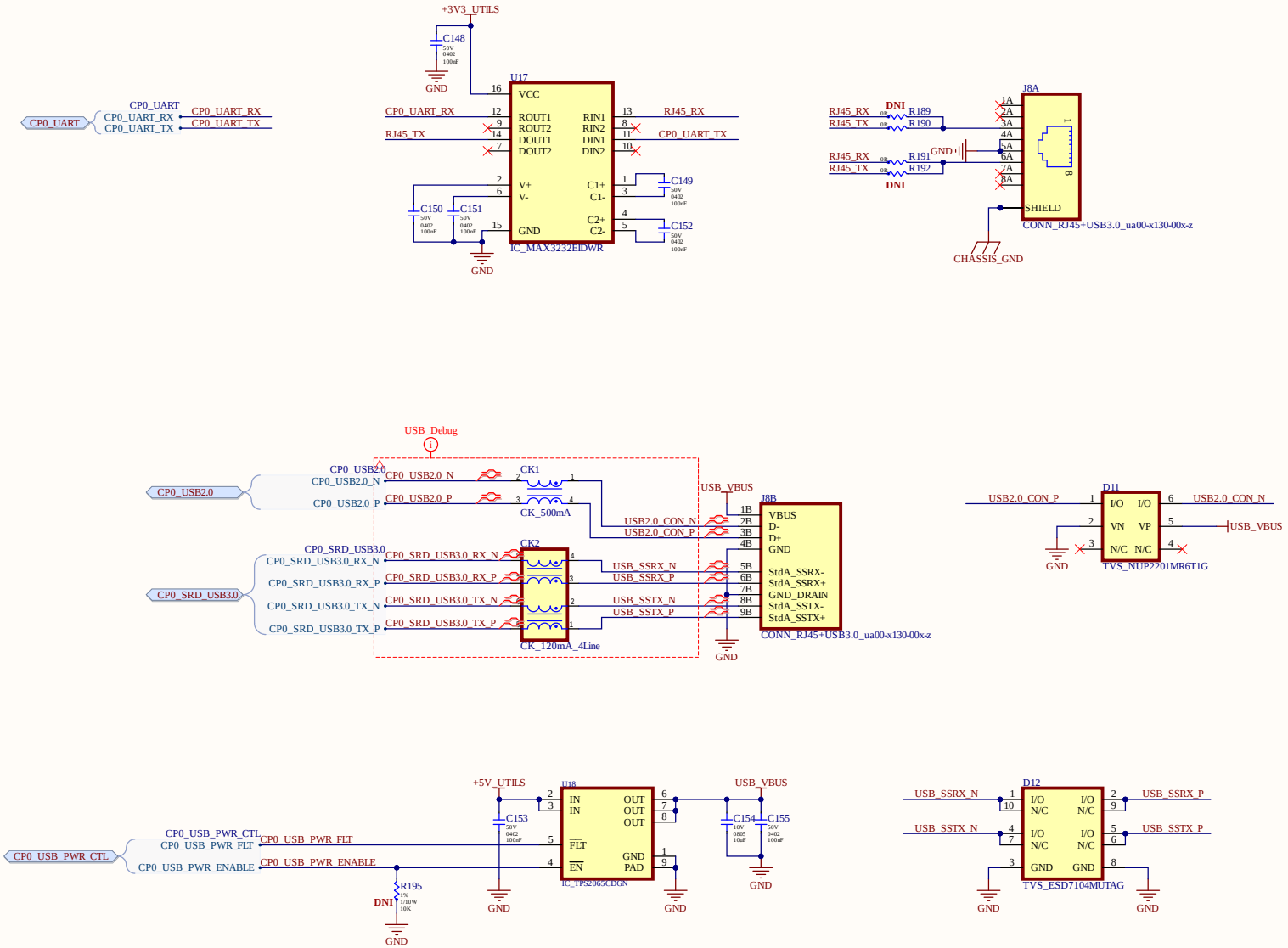
Project:			Title:		
N4-V1.PrjPcb			6.2 MiniPCIE_WIFI.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	28
Design				Number of Sheets	43



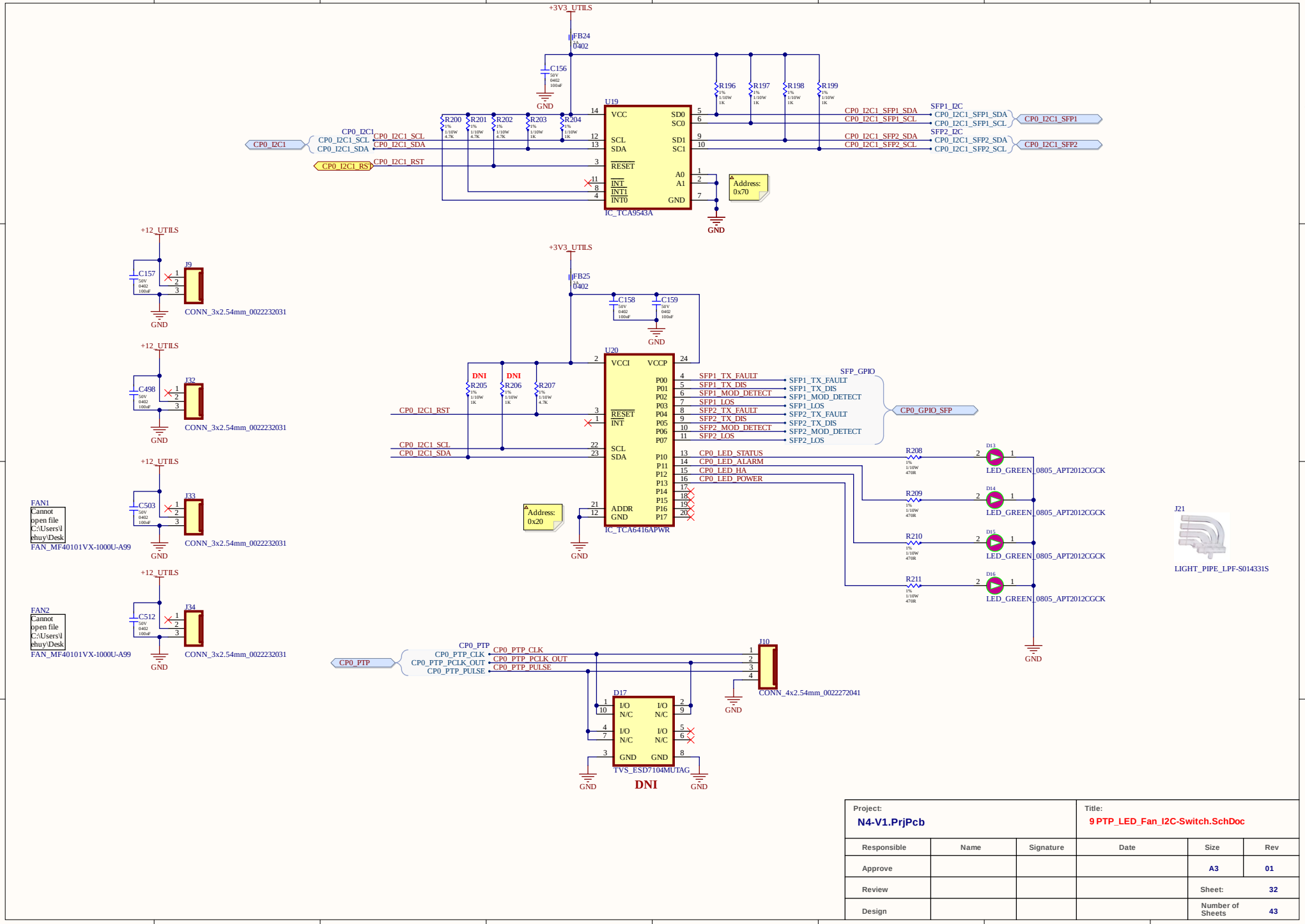
Project:			Title:		
N4-V1.PrjPcb			6.3 M.2 _SATA.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	29
Design				Number of Sheets	43



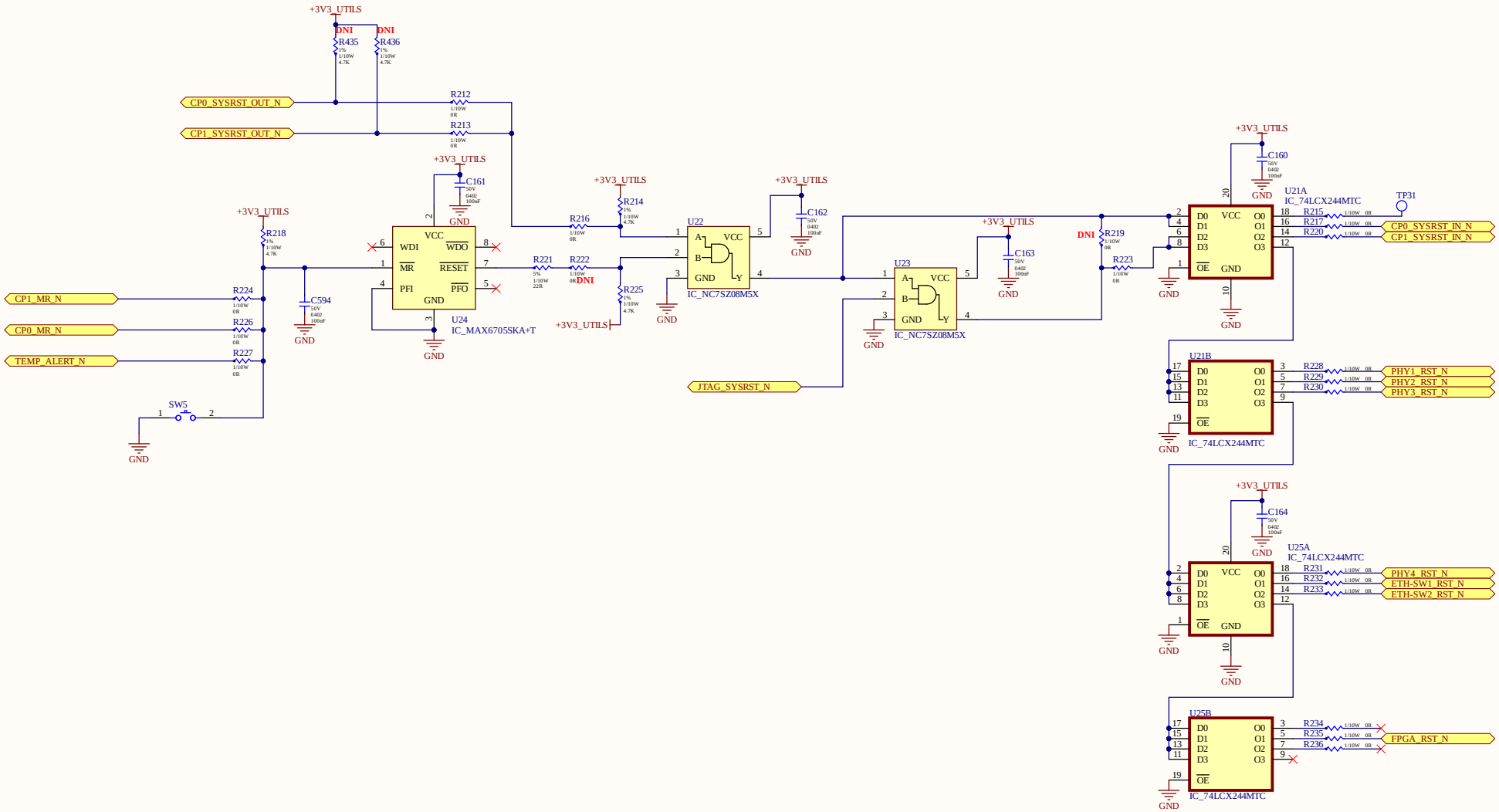
Project:			Title:		
N4-V1.PrjPcb			7 FPGA-Module.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	30
Design				Number of Sheets	43



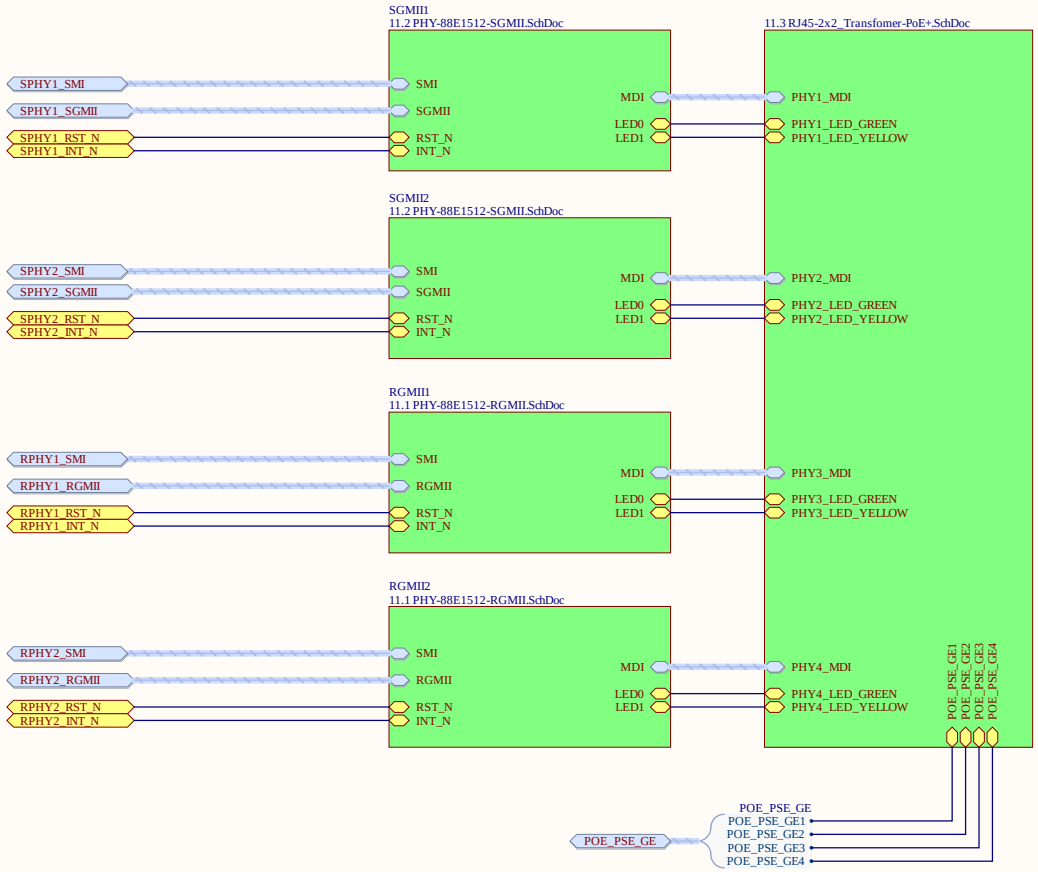
Project:			Title:		
N4-V1.PrjPcb			8 USB3.0_Console.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	31
Design				Number of Sheets	43



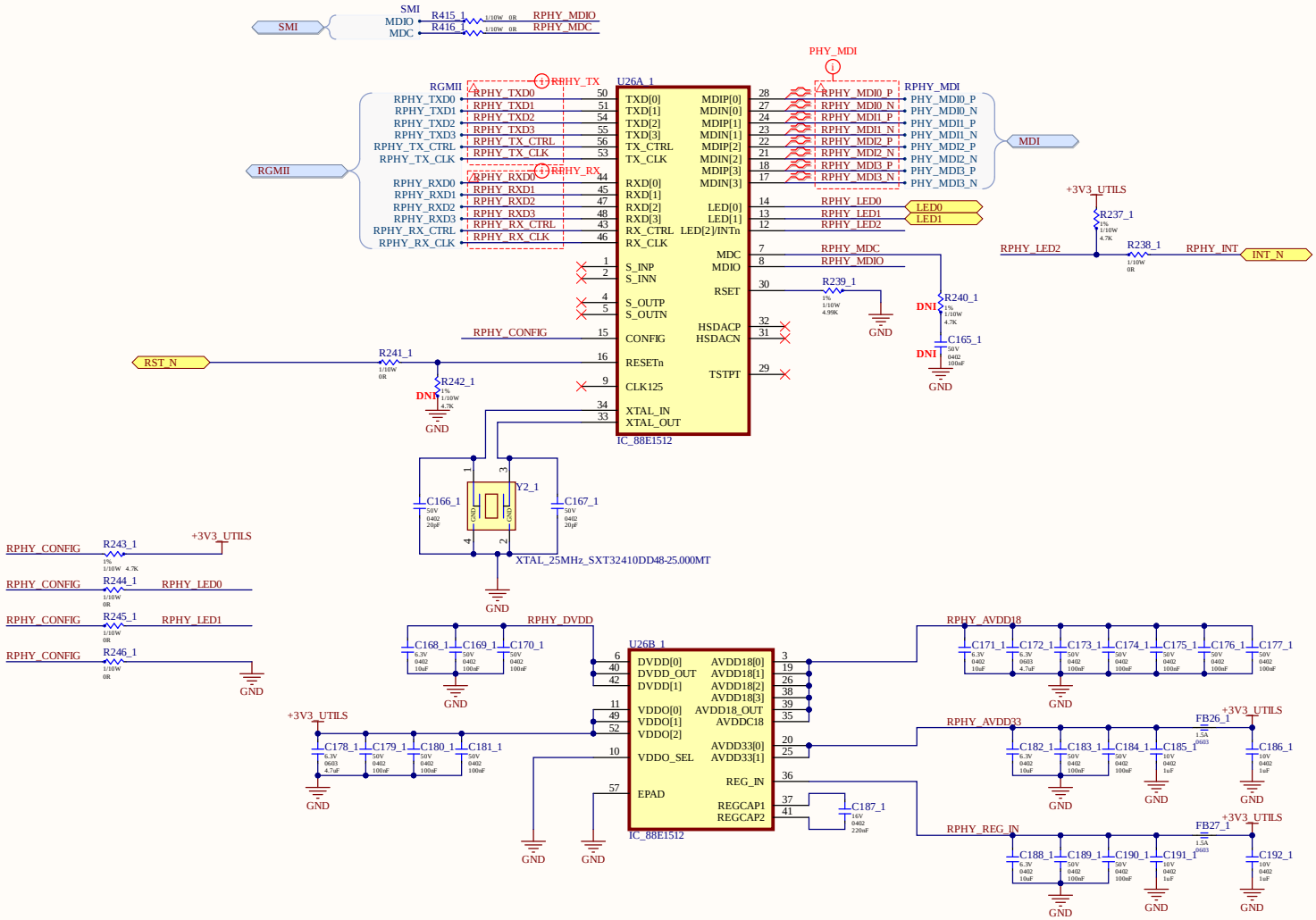
Project:			Title:		
N4-V1.PrjPcb			9 PTP_LED_Fan_I2C-Switch.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	32
Design				Number of Sheets	43



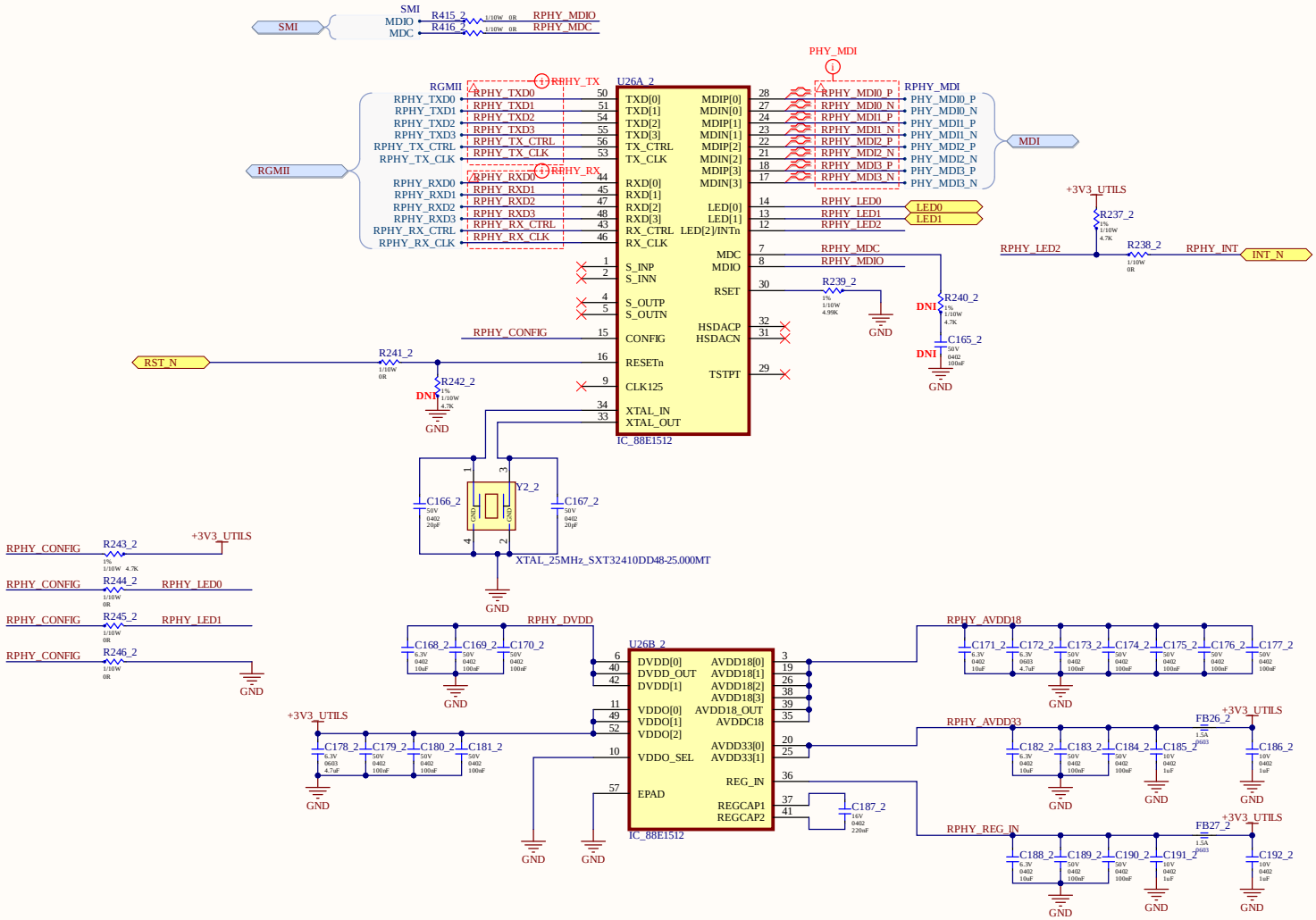
Project:			Title:		
N4-V1.PrjPcb			10 Power-Ctrl_RST-Ctrl.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	33
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			11 Ethernet-Group1.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	34
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			11.1 PHY-88E1512-RGMII.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	35
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			11.1 PHY-88E1512-RGMII.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	35
Design				Number of Sheets	43

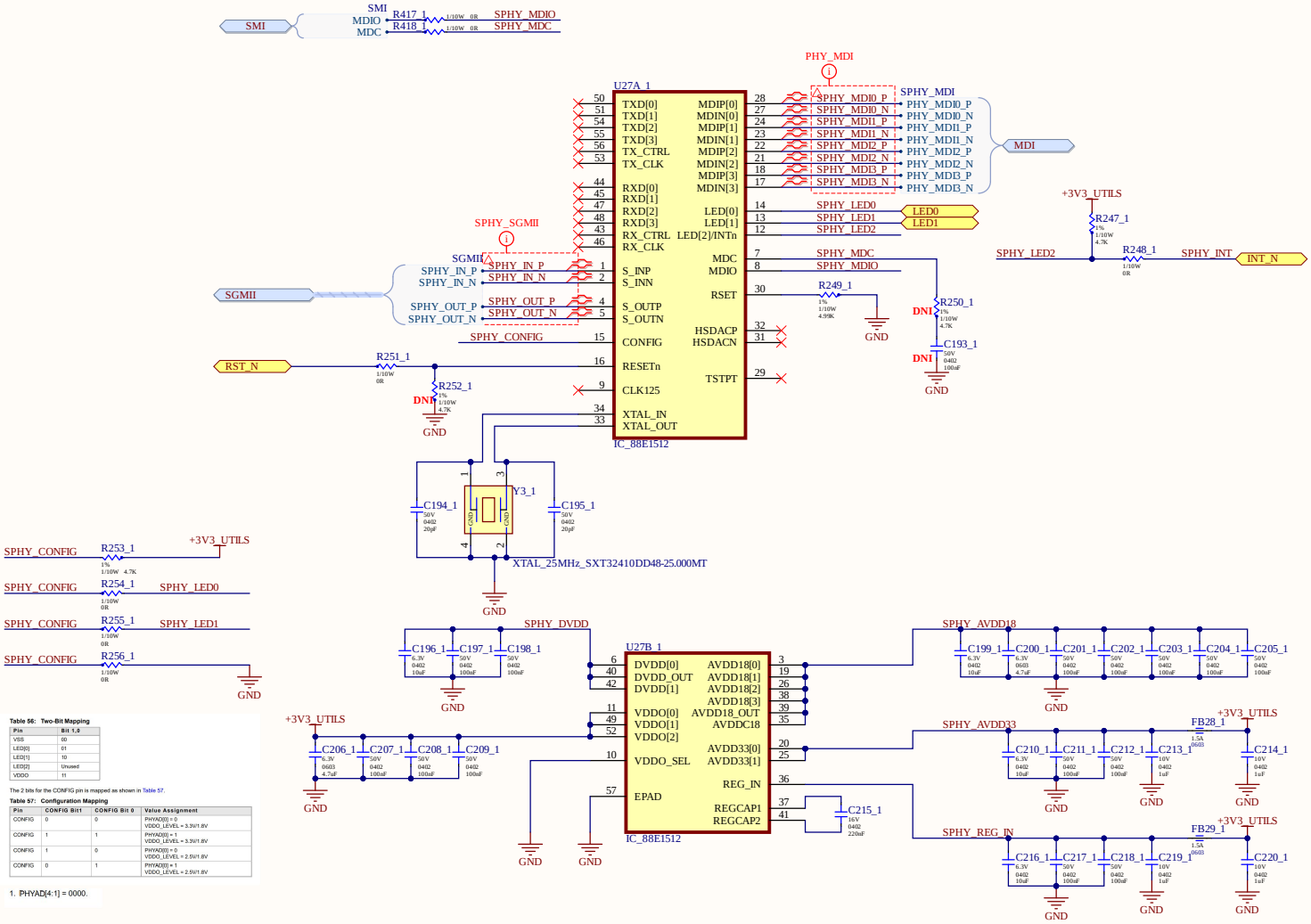


Table 56: Two-Bit Mapping

Pin	Bit 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

The 2 bits for the CONFIG pin is mapped as shown in Table 57.

Table 57: Configuration Mapping

Pin	CONFIG Bit1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYAD[0] = 0 VDDO_LEVEL = 3.3V/1.8V
CONFIG	1	1	PHYAD[0] = 1 VDDO_LEVEL = 3.3V/1.8V
CONFIG	1	0	PHYAD[0] = 0 VDDO_LEVEL = 2.5V/1.8V
CONFIG	0	1	PHYAD[0] = 1 VDDO_LEVEL = 2.5V/1.8V

1. PHYAD[4:1] = 0000.

Project:			Title:		
N4-V1.PrjPcb			11.2 PHY-88E1512-SGMII.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	36
Design				Number of Sheets	43

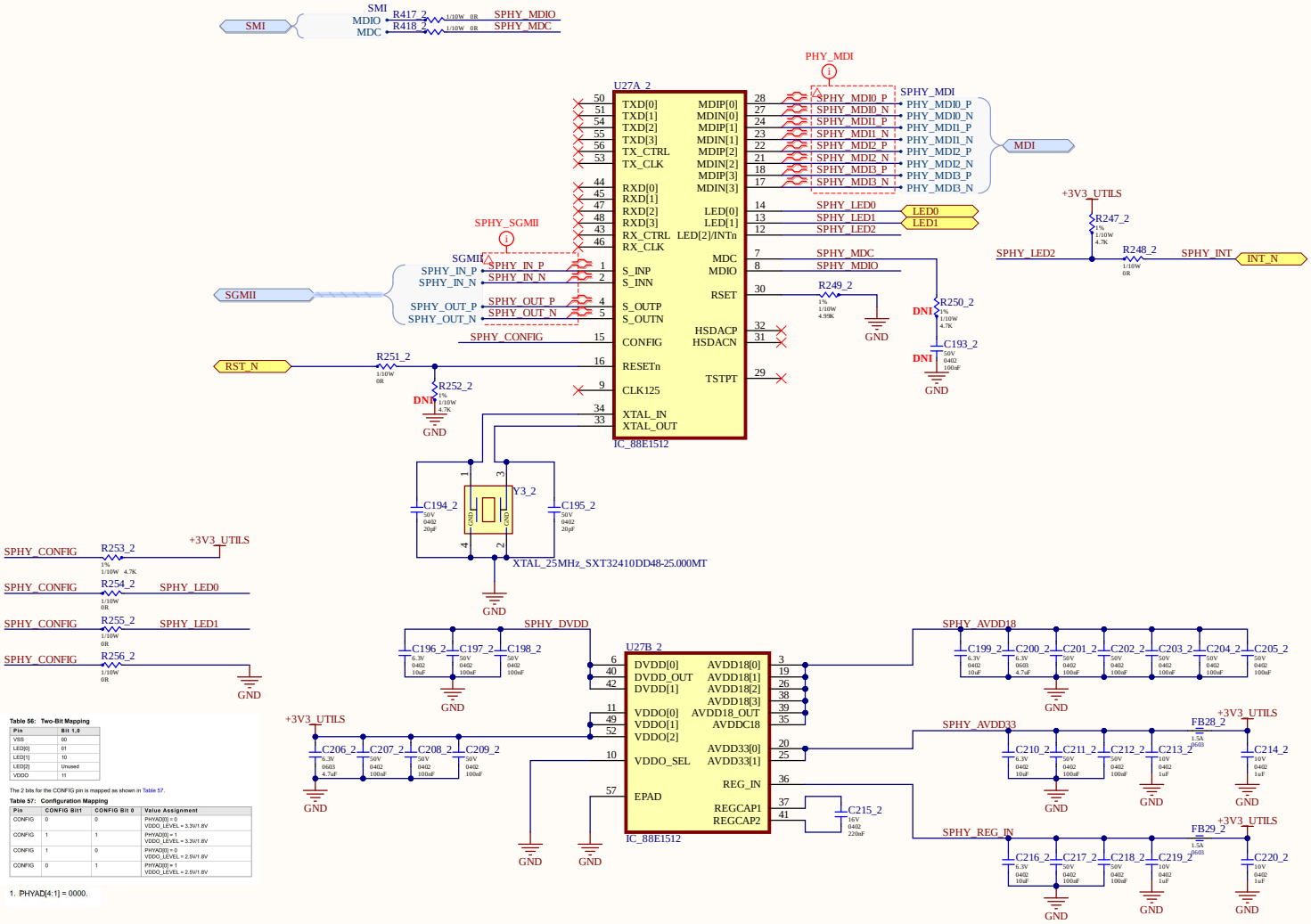


Table 56: Two-Bit Mapping

Pin	Bit 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
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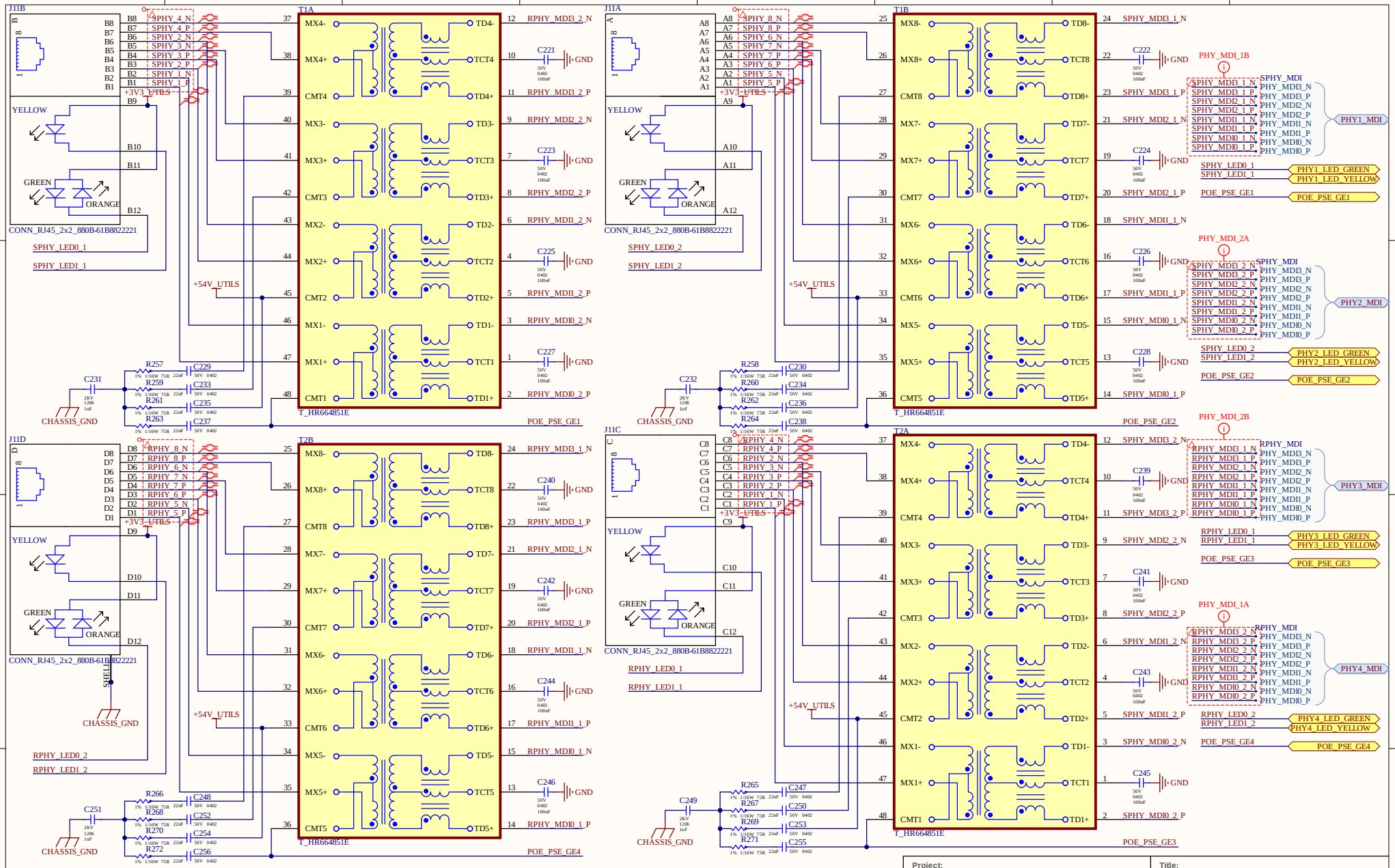
The 2 bits for the CONFIG pin is mapped as shown in Table 57.

Table 57: Configuration Mapping

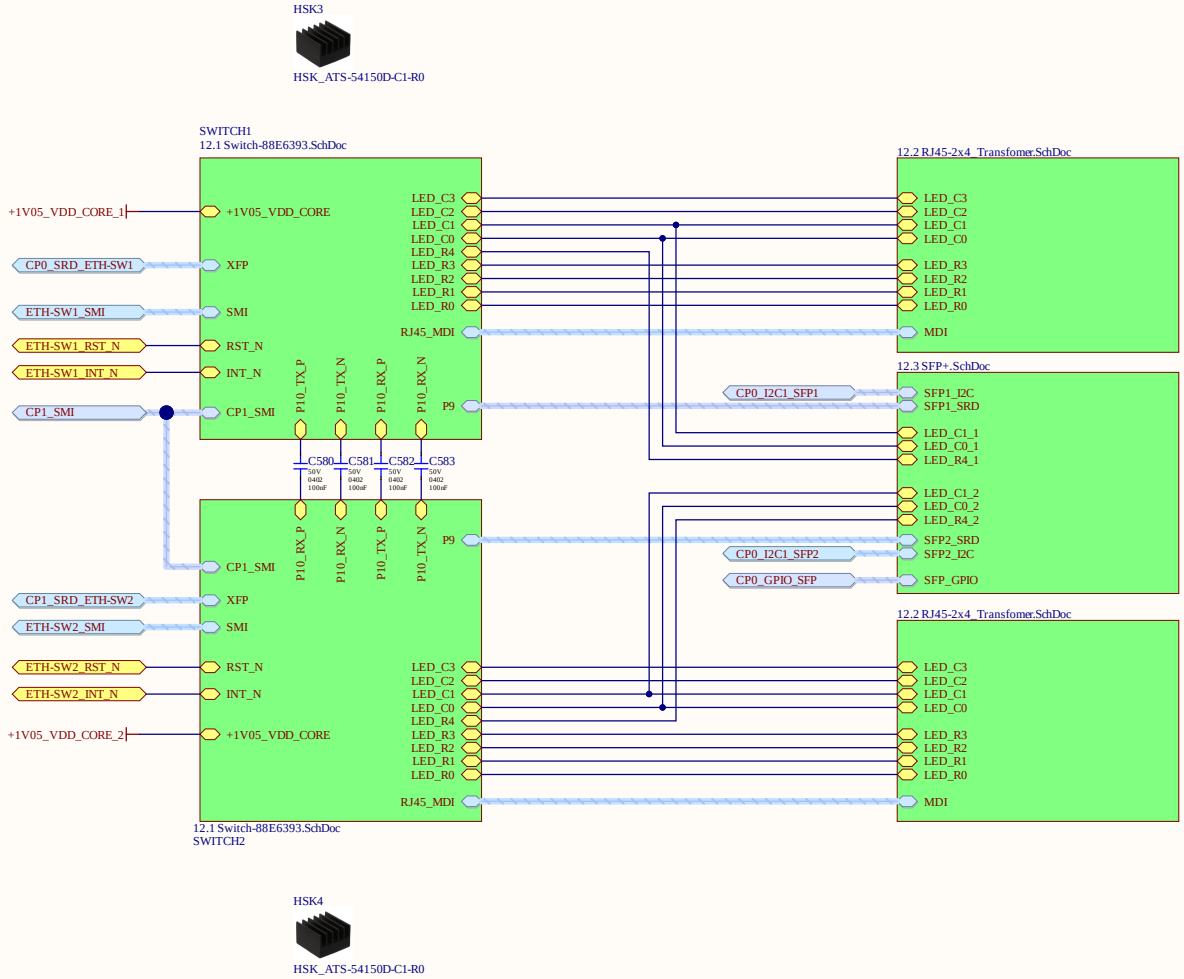
Pin	CONFIG Bit1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYAD[0] = 0 VDDO_LEVEL = 3.3V/1.8V
CONFIG	1	1	PHYAD[0] = 1 VDDO_LEVEL = 3.3V/1.8V
CONFIG	1	0	PHYAD[0] = 0 VDDO_LEVEL = 2.5V/1.8V
CONFIG	0	1	PHYAD[0] = 1 VDDO_LEVEL = 2.5V/1.8V

1. PHYAD[4:1] = 0000.

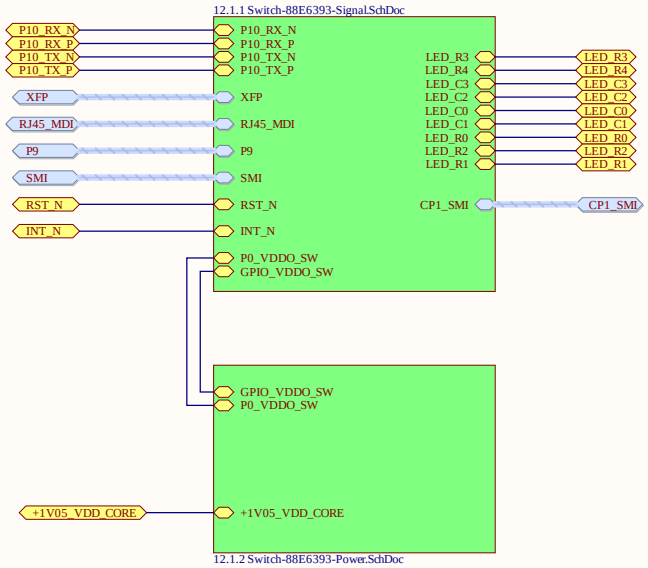
Project:			Title:		
N4-V1.PrjPcb			11.2 PHY-88E1512-SGMII.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	36
Design				Number of Sheets	43



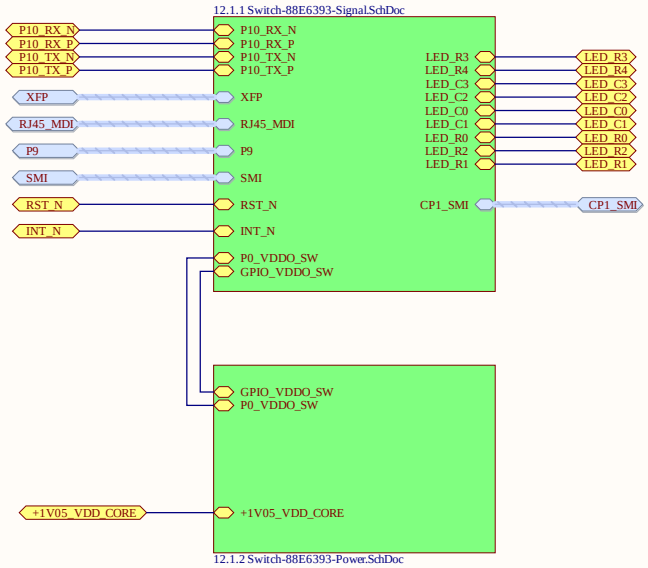
Project:			Title:		
N4-V1.PrjPcb			11.3 RJ45-2x2_Transfomer-PoE+.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	37
Design				Number of Sheets	43



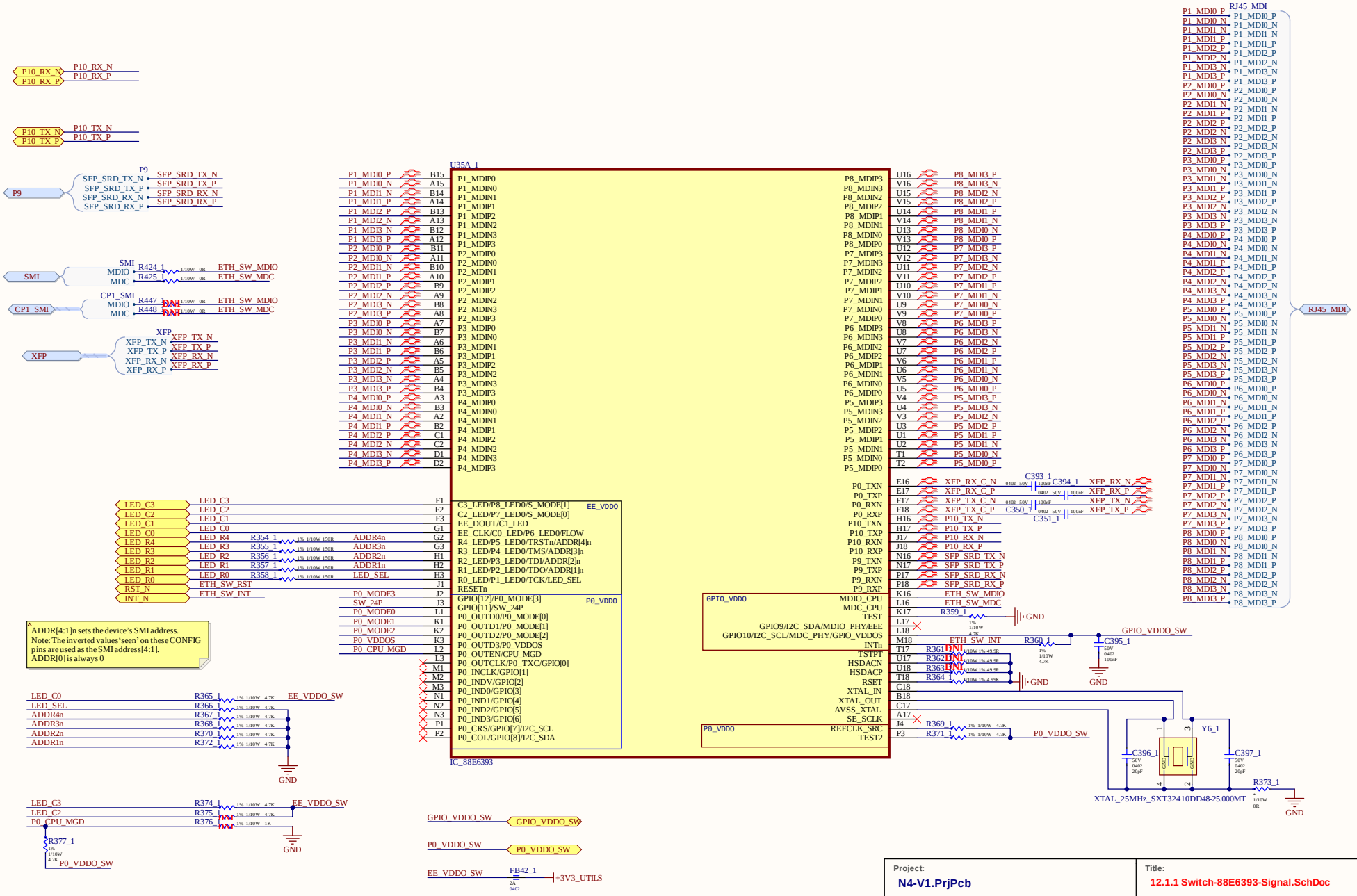
Project:			Title:		
N4-V1.PrjPcb			12 Ethernet-Group2.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	38
Design				Number of Sheets	43



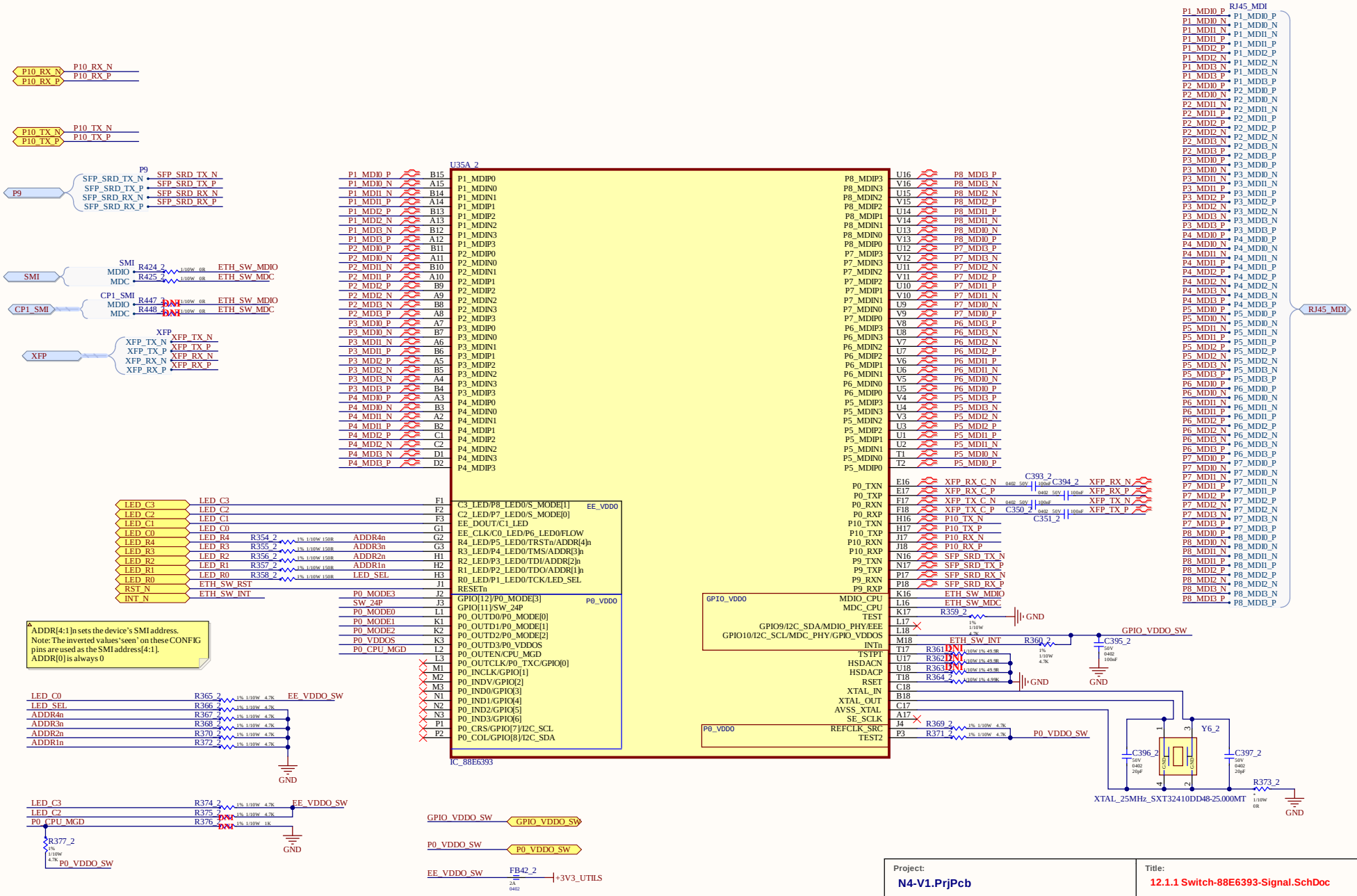
Project:			Title:		
N4-V1.PrjPcb			12.1 Switch-88E6393.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	39
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			12.1 Switch-88E6393.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	39
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			12.1.1 Switch-88E6393-Signal.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	40
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			12.1.1 Switch-88E6393-Signal.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
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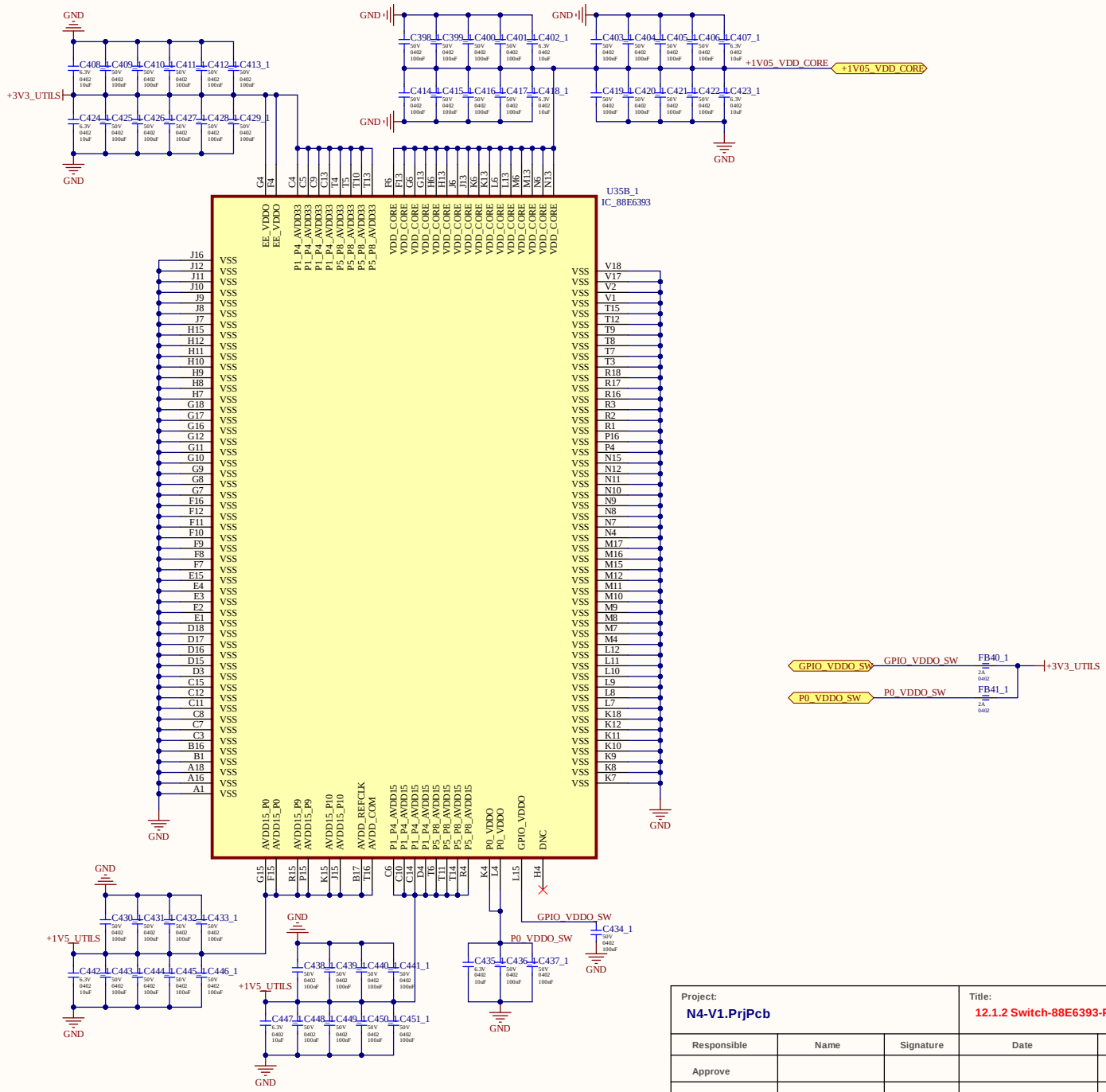

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Responsible	Name	Signature	Date	Size	Rev
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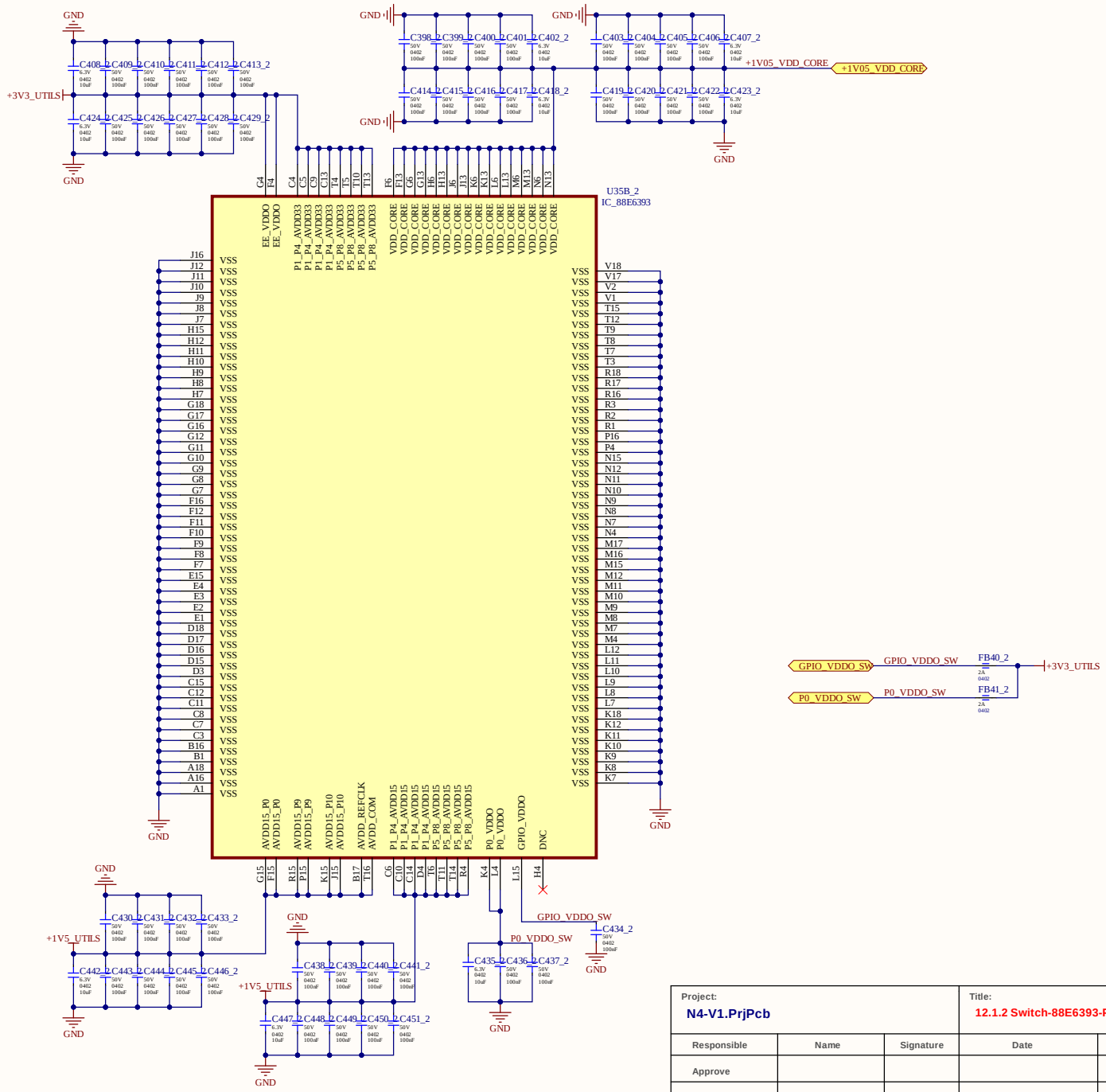
Review				Sheet:	41
Design				Number of Sheets	43



Project:			Title:		
N4-V1.PrjPcb			12.1.2 Switch-88E6393-Power.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
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Review				Sheet:	41
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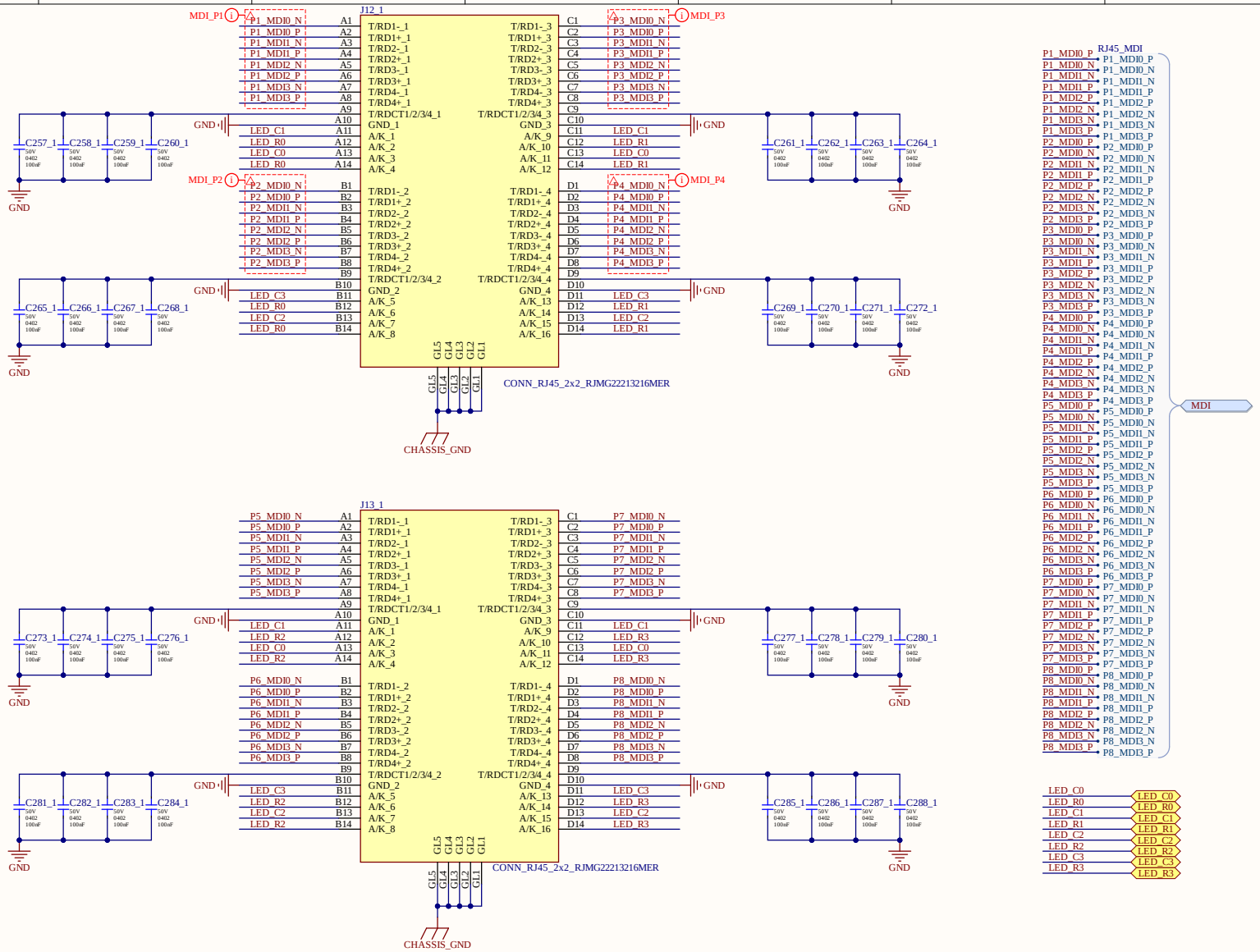
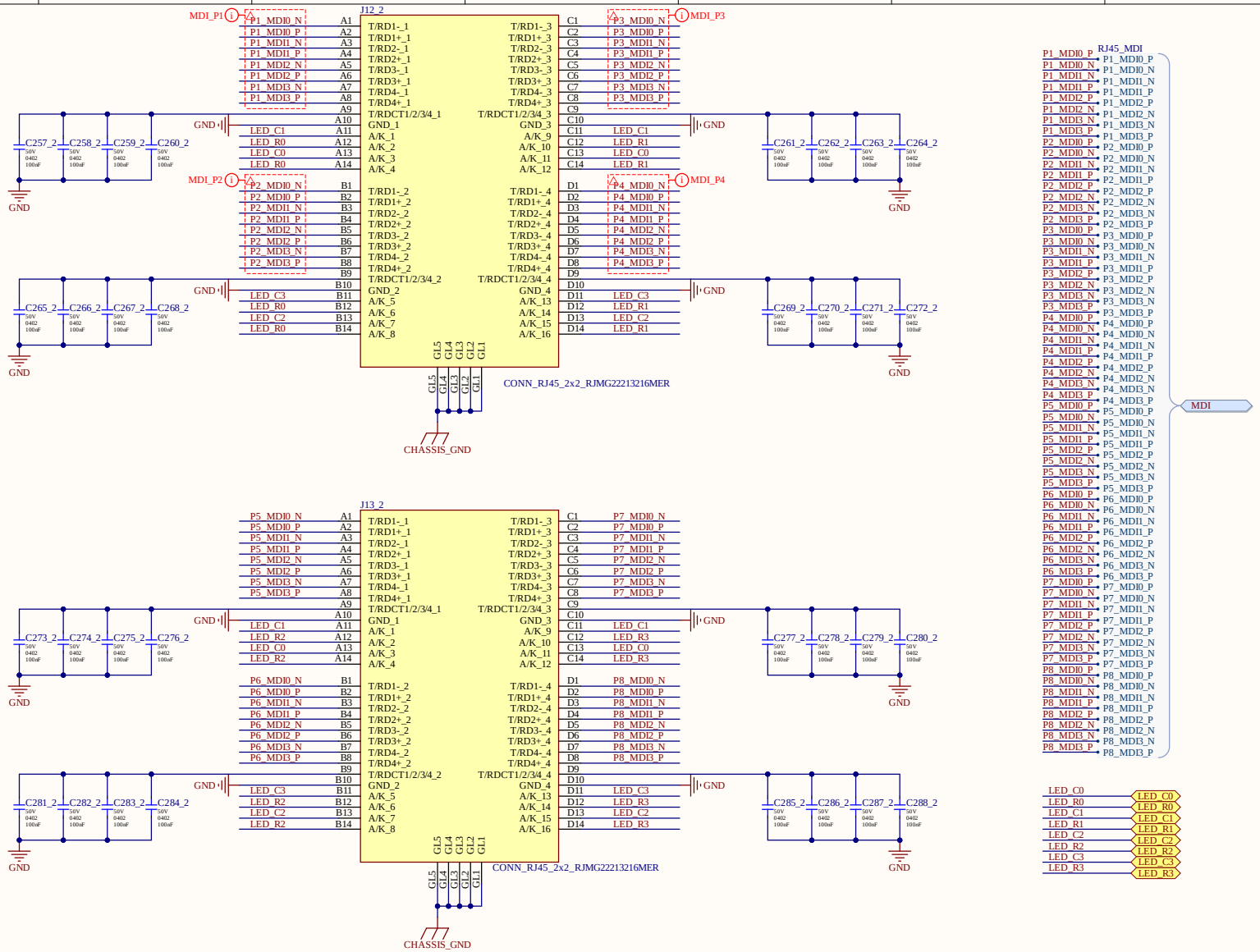


C3	R0	C2	R0	C3	R1	C2	R1	C3	R2	C2	R2	C3	R3	C2	R3
+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14	
B P2				D P4				B P6				D P8			
A P1				C P3				A P5				C P7			
+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14	
C1	R0	C0	R0	C1	R1	C0	R1	C1	R2	C0	R2	C1	R3	C0	R3

Project:			Title:		
N4-V1.PrjPcb			12.2 RJ45-2x4_Transfomer.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	42
Design				Number of Sheets	43



C3	R0	C2	R0	C3	R1	C2	R1	C3	R2	C2	R2	C3	R3	C2	R3
+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14	
B P2				D P4				B P6				D P8			
A P1				C P3				A P5				C P7			
+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14		+Y11 -Y12		+G13 -G14	
C1	R0	C0	R0	C1	R1	C0	R1	C1	R2	C0	R2	C1	R3	C0	R3

Project:			Title:		
N4-V1.PrjPcb			12.2 RJ45-2x4_Transfomer.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
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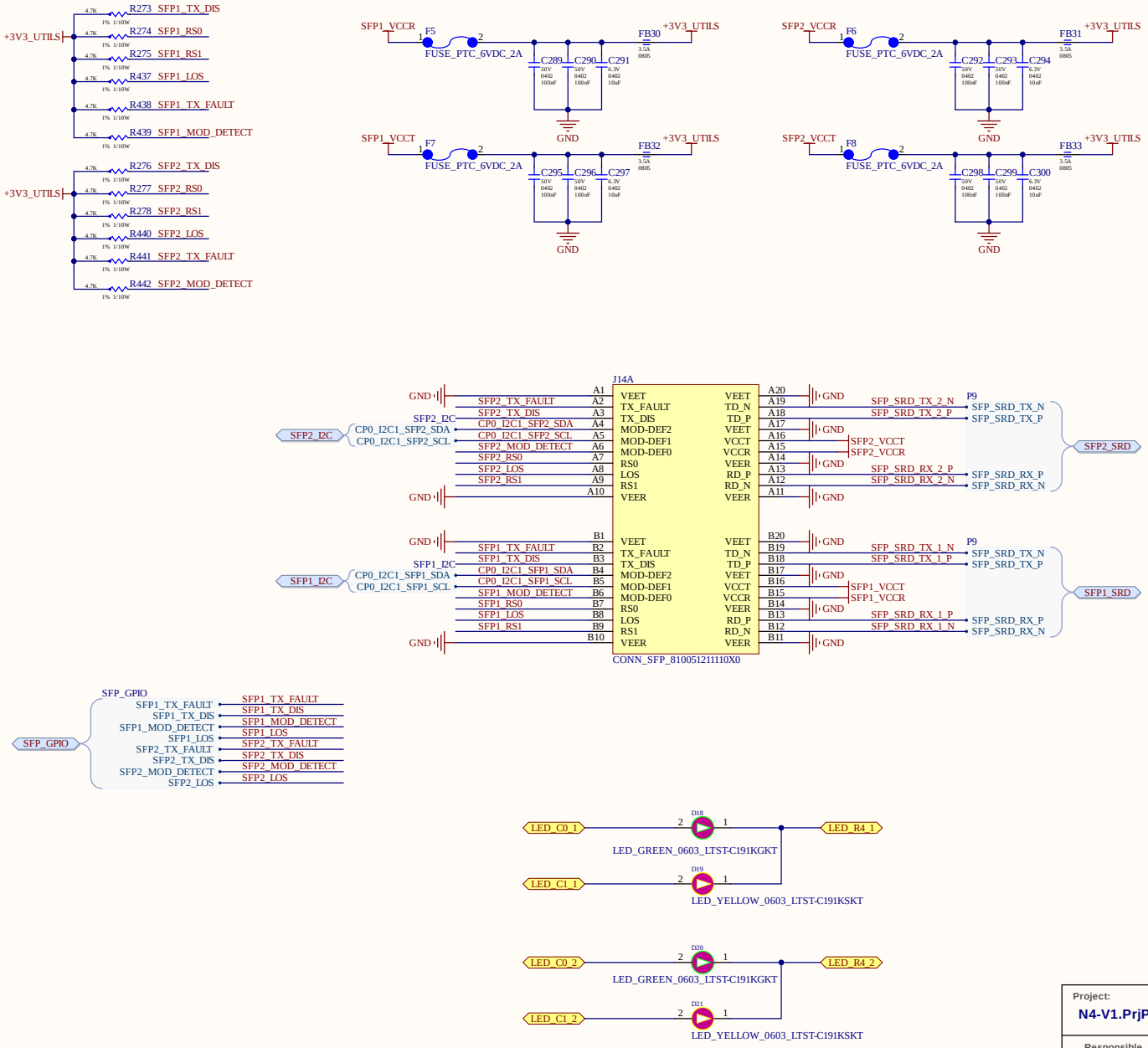

Project:			Title:		
N4-V1.PrjPcb			12.3 SFP+.SchDoc		
Responsible	Name	Signature	Date	Size	Rev
Approve				A3	01
Review				Sheet:	43
Design				Number of Sheets	43