Introduction to Vivado HLS

Lab#6 Report

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Introduction

This lab was to use Vivado HLS tools to create a custom hardware accelerated implementations in a reconfigurable hardware from high level representations of the application, and optimizing Vivado HLS applications to maximize statement and system level parallelism.

Procedure

1. Followed the instructions in lab6 tutorial.
2. Generated synthesis reports for no directive hardware implementation and the directives interfaced hardware implementations. Identified that the interface changed from memories to fifo.
3. Exported the the HLS design to XPS project and profiled the software code using software and hardware counters.

Comparison of Software only implementation (lab4) with Hardware/Software implementation (lab6)

Table1 specifies the comparison of software only implementation and hardware/software implementation done in this lab. Due to the utilization of hardware in the implementation of AES in this lab, the number of clock cycles utilized for the whole encrypt operation is reduced when compared to the software only implementation utilized in lab4. Later the amount of resources utilized by both the implantations are compared, due the custom hardware developed for encrypt function using Vivado HLS, we can see the difference in the number of FFs and LUTs utilized is increased in the hardware/software implementation. This increase is due to the implementation of co-processor and utilization of FSL links for data path. Thus it is evident that the performance is improved with utilization of the implemented custom hardware.

Table2 compares the software and hardware profiling results for Hardware/Software implementation of AES. The AES encryption was looped for 100 times and the profiling results were noted. It also compares the code size and data utilized in the software and hardware profiling of the AES implementation.

Table3 &Table4 shows the synthesis report of the hardware implementation of AES using HLS using different interfaces. Table3 refers to a no directive implementation where the inputs and outputs are read and written from the local memories. Whereas Table3 refers to the interfaced directive implementation where the inputs and outputs are read and written from the microblaze using an FSL link from a fifo buffer. Thus the interface is fifo in Table3.

Thus a custom hardware co-processor was built and connected it using a high speed FSL buses to software core processor on FPGA using Vivado HLS

Table1: Comparison of software only implementation with hardware/software implementation.

Function/Resources Utilized	Software only Implementation	Hardware/Software Implementation
Encrypt	6379420 Cycles	1231724 Cycles
No of FF used	5940	6338
No of LUTs used	5141	5562
No of BRAMs used	15	15
No of DSP48Es used	3	3

Table2: Comparison of gprof and hardware profiling in hardware/software implementation.

Function	Software Profiling	Hardware Profiling
Encrypt Execution Time	196.299ms	1231724 cycles
Code Size	7738	67560
Data	400	1552
Hardware_prof	12.76% time utilization	

Table3: Synthesis Report without interface directives

Parameter	Value
Estimated Clock Period	7.59ns
Worst case latency	2177 clock cycles
Number of DSP48A used	0
Number of BRAMs used	5
Number of FFs used	420
Number of LUTs used	777
IO Protocol used for	
-Encrypt	ap_ctrl_hs
-PlainText	ap_memory
-Key	ap_memory
-CipherText	ap_memory

Table4: Synthesis Report with interface directives

Parameter	Value
Estimated Clock Period	7.59ns
Worst case latency	2146 clock cycles
Number of DSP48A used	0
Number of BRAMs used	5
Number of FFs used	402
Number of LUTs used	773
IO Protocol used for	
-Encrypt	ap_ctrl_hs
-PlainText	ap_fifo
-Key	ap_fifo
-CipherText	ap_fifo