**Goblin-Core Architecture Specification**

Version 1.0.0

Legal Information

**Change Log**

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# Introduction

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# Architecture Overview

# Addressing Modes & Operand Conventions

The following section describes the local and global address mode conventions for the Goblin-Core architecture family. This includes local and global address modes as well as the associated operand conventions as they appear in the instruction set mnemonics.

# Addressing Modes

# Local Register Indirect with Displacement

# Global Register Indirect with Displacement

# Instruction Pointer [IP] Relative

# Operand Conventions

The architecture defines 8-bit byte word, 16-bit word, 32-bit double word, and 64-bit quad word. The architecture defines an IEEE-754 32-bit single precision floating point representation as well as an IEEE-754 64-bit double precision floating point representation. The architecture also defines a 128-bit global addressing format. The most significant quad word [64-bits] contains the address portion of the global address operand. The least significant quad word [64-bits] contains the interconnect locality portion of the address operand. However, 128-bit global address operands map to 64-bit quad word data payloads.

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Mnemonic | Size [bytes] | Notes |
| Unsigned Byte | UB | 1 |  |
| Unsigned Word | UW | 2 |  |
| Unsigned Double | UD | 4 |  |
| Unsigned Quad | UQ | 8 |  |
| Signed Byte | SB | 1 |  |
| Signed Word | SW | 2 |  |
| Signed Double | SD | 4 |  |
| Float Single | FS | 4 | IEEE-754 32-bit single precision floating point |
| Float Double | FD | 8 | IEEE-754 64-bit double precision floating point |
| Global Address | GA | 16 | Global Addressing operand mode. Most significant quad contains the address portion of the operand. Least significant quad contains the interconnect locality portion. |

**Figure 1. Operand Conventions**

# Exception Model

# Memory Management Units

# Local MMU

# Global MMU

# Interrupt Model

# Instruction Set

# Debug Model

# Application Binary Interface

# Appendix A. Instruction Set Table

# Appendix B. Performance Counters

# Appendix NNNN.