Read Request / Write Request

Copy-Back / Prefetch

L1a MSHR

L1b MSHR

L2 MSHR

Request	Answer
Find free MSHR Allocate Untreated Answer Low Latency (free package)	Find existing MSHR Set Untreated Answer High Latency (R/W/P Answer)
Find Next Untreated Request Directory->Request(package)	Find Next Untreated Answer Directory->Answer(package)
Dir: package->memory_operation=READ_REQUEST return memory_status=TRANSMIT	Dir: Coherence Answer(package) Coherence Access(package) package->memory_operation=READ_ANSWER Dir->release_lock() return memory_status=TRANSMIT
Find Next Transmit Send Package If Request: Directory->Wait(package)	Find Next Transmit Send Package Free Package
Dir: package->memory_operation=Read Answer return memory_status=wait	

Type		States Before			Details	States After		
		L1a	L1b	L2		L1a	L1b	L2
Cache Read	Read Miss L1, Read Miss L2	I	I	I		E	I	E
		I	I	I		I	I	E
	Read Hit L1	M	-	-		M	-	-
		O	-	-		O	-	-
		E	-	-		E	-	-
		S	-	-		S	-	-
	Read Miss L1, Read Hit L2	I	M	E		S	S	O
		I	O	E		S	S	O
		I	E	E		S	S	S
		I	S	S		S	S	S
		I	I	O		S	I	O
		I	I	E		E	I	E
		I	I	S		S	I	S

Type		States Before			Details	States After		
		L1a	L1b	L2		L1a	L1b	L2
Cache Write	Write Miss L1, Read Miss L2	I	I	I		M	I	E
		I	I	I		I	I	E
	Write Hit L1	M	-	-		M	I	E
		O	-	-		M	I	E
		E	-	-		M	I	E
		S	-	-		M	I	E
	Write Miss L1, Read Hit L2	I	M	E		M	I	E
		I	O	E		M	I	E
		I	E	E		M	I	E
		I	S	S		M	I	E
		I	I	O		M	I	E
		I	I	E		M	I	E
		I	I	S		M	I	E