**HAL VALIDATION RELEASE NOTES**

Release date: 19-Apr-2016

1. **Introduction**

This document describe the release information of Hardware abstraction firmware layer and Asic IPs validation.

1. **Release structure**

|  |  |
| --- | --- |
| ├── 02\_IT  │ └── platform  │ └── asic  │ └── hal  │ ├── app  │ │ ├── include  │ │ ├── linker  │ │ └── source  │ ├── release  │ │ ├── HAL\_Defects\_Analysis.xlsx  │ │ ├── HAL\_validation\_release\_notes.docx  │ │ ├── HAL\_Validation\_Status\_Report.xlsx  │ │ └── QC\_delivery\_checklist.xlsx  │ └── spec  ├── 03\_UT  ├── 04\_COMMON  │ ├── qc\_libs  │ └── qc\_tools  └── 05\_WORKSPACE  ├── Makefile  ├── qc\_platform.mak  └── swap\_mak  ├── AsicFwS1.mak  └── AsicFwS2.mak | - HAL integration test suits  - Test apps header files  - Swapping linker  - Test apps source files  - Release documents  - Defect analysis of  - Release notes (this document)  - Status tracking  - Delivery checklist  - Test specification and results  - Unit test suits  - QC common facilities  - QC library for IT, UT (c language)  - QC supporting tools (shell, python, \*.cmm)  - Workspace (build location)  - Makefile  - Makefile of integration test  - Swapping makefile to swap development’s makefiles |

1. **Inputs information**
2. **Hardware data sheets**

|  |  |  |  |
| --- | --- | --- | --- |
| **NO.** | **Module** | **Input** | **Revision** |
| 1 | UART | DW\_apb\_uart\_databook.pdf | 4.00a |
| 2 | GPIO | DW\_apb\_gpio\_databook.pdf | 2.11a |
| 3 | I2C | DW\_apb\_i2c\_databook.pdf | 2.00a |
| 4 | PWM | PWM\_uarch.pdf | 1.3 |
| 5 | SPI | DW\_apb\_ssi\_databook.pdf | 4.00a |
| 6 | QSPI | GUC-IGDAVI001A-QSPI-Datasheet.pdf | 1.0.0 |
| 7 | SYNCIO | Pulse\_Generator\_uArch\_v1.5.pdf | 1.5 |
| 8 | TIMER | DW\_apb\_timers\_databook.pdf | 2.10a |
| 9 | WDT | DW\_apb\_wdt\_databook.pdf | 1.09a |
| 10 | DMA | dw\_axi\_dmac\_db.pdf | 1.00a-ea01 |

1. **HAL firmware**

|  |  |  |  |
| --- | --- | --- | --- |
| **NO.** | **Module** | **Input** | **Revision** |
| 1 | UART | hal\_com.c  hal\_com.h | 1.0.0  1.0.0 |
| 2 | GPIO | hal\_gpio.c hal\_gpio.h | 1.0.0  1.0.0 |
| 3 | I2C | hal\_i2c.c  hal\_i2c.h | 1.0.0  1.0.0 |
| 4 | PWM | hal\_pwm.c  hal\_pwm.h | 1.0.0  1.0.0 |
| 5 | SPI | hal\_spi.c  hal\_spi.h | 1.0.0  1.0.0 |
| 6 | QSPI | hal\_qspi.c  hal\_qspi.h | On-going development |
| 7 | SYNCIO | hal\_syncio.c  hal\_syncio.h | 1.0.0  1.0.0 |
| 8 | TIMER | hal\_timer.c  hal\_timer.h | 1.0.0  1.0.0 |
| 9 | WDT | hal\_wdt.c  hal\_wdt.h | 1.0.0  1.0.0 |
| 10 | DMA | hal\_dma.c  hal\_dma.h | On-going development |
| 11 | VIC | hal\_vic.c  hal\_vic.h | 1.0.0  1.0.0 |
| 12 | MIPI | hal\_mipi.c  hal\_mipi.h | On-going development |

1. **System architecture**

|  |  |  |  |
| --- | --- | --- | --- |
| **NO.** | **Module** | **Input** | **Revision** |
| 1 | ASB | Lb-0023\_asb\_2015\_11\_06.pdf  SB0LFC6X05A\_assy.pdf | 1  1 |
| 2 | P2 | LightASICSystem.pdf | 1.5 |
| 3 | Config | synopsys\_general\_ip\_configuration\_0127\_2016\_v0.xlsx | NA |

1. **Outputs information**
2. **HAL test apps:**

|  |  |  |  |
| --- | --- | --- | --- |
| **NO.** | **Module** | **Input** | **Revision** |
| 1 | UART | it\_hal\_com.c  it\_hal\_com.h | 1.0.1  1.0.1 |
| 2 | GPIO | it\_hal\_gpio.c it\_hal\_gpio.h | 1.0.1  1.0.1 |
| 3 | I2C | it\_hal\_i2c.c  it\_hal\_i2c.h | 1.0.1  1.0.1 |
| 4 | PWM | it\_hal\_pwm.c  it\_hal\_pwm.h | 1.0.1  1.0.1 |
| 5 | SPI | it\_hal\_spi.c  it\_hal\_spi.h | 1.0.1  1.0.1 |
| 6 | QSPI | it\_hal\_qspi.c  it\_hal\_qspi.h | On-going development |
| 7 | SYNCIO | it\_hal\_syncio.c  it\_hal\_syncio.h | 1.0.1  1.0.1 |
| 8 | TIMER | it\_hal\_timer.c  it\_hal\_timer.h | 1.0.1  1.0.1 |
| 9 | WDT | it\_hal\_wdt.c  it\_hal\_wdt.h | 1.0.1  1.0.1 |
| 10 | DMA | Implicit covered in I2C and SPI | NA |
| 11 | VIC | Implicit covered in other modules | NA |
| 12 | MIPI | NA | On-going development |

1. **QC libraries**

|  |  |  |  |
| --- | --- | --- | --- |
| **NO.** | **Module** | **Input** | **Revision** |
| 1 | LOG | it\_log\_swapper.c  it\_log\_swapper.h | 1.0.1  1.0.1 |
| 2 | Assert | qc\_assert.c  qc\_assert.h | 1.0.1  1.0.1 |
| 3 | COMMON | qc\_common.h  qc\_common.c | 1.0.1  1.0.1 |

1. **HAL QC’s utilities**

|  |  |  |  |
| --- | --- | --- | --- |
| **NO.** | **Module** | **Input** | **Revision** |
| 1 | utilities | asic\_utilities.py  hal\_test.py | 1.0.1  1.0.0 |
| 2 | workspace | Makefile  qc\_platform.mak | 1.0.1  1.0.1 |
| 3 | swapper | AsicFwS1.mak  AsicFwS2.mak | 1.0.1  1.0.1 |

1. **Execution guideline**
   * + Download FTDI tool on google drive: [FTDI](https://drive.google.com/open?id=0B2TcdQ1KviMyWUhuTnMySFg3NGs)
     + Extract all files (keep folder structure) and create FTDI folder in atlantic\_fw repository to store them.
     + Download FPGA image on google drive: [FPGA-Rev0D](https://drive.google.com/open?id=0B5ni7VJ2qjKqdGRIS2lpdXBBaVE)
     + Create FPGA folder inside atlantic\_fw repository and store FPGA image in FPGA folder.
     + Unzip test suit Patch\_1\_0\_0\_19042016.zip inside atlantic\_fw repository
     + Jump to extracted folder named “19042016”:

$cd 19042016/05\_WORKSPACE

* + - Build test image:

$make

* + - Flashing FPGA via FTDI4222: (hardware wiring refers to [ASB bring-up guideline](https://drive.google.com/open?id=1CRnbnM5SwWvWciwWjGMCoyrylsDiVfzmUU5V3ud8l_Y))

(Just unplug J711)

$make FLASH\_FPGA FPGA=../../FPGA/bedrock\_full\_edif\_rev0D\_g.bit

Note: If there is not supported Quad mode on FTDI4222, use this command:

$make FLASH\_FPGA FLASH\_MODE=flash\_single FPGA=../../FPGA/bedrock\_full\_edif\_rev0D\_g.bit

* + - Unplug USB connector of FTDI4222 then connect to USB connect of FTDI2232
    - Flashing ASIC testing firmware: (hardware wiring refers to [ASB bring-up guideline](https://drive.google.com/open?id=1CRnbnM5SwWvWciwWjGMCoyrylsDiVfzmUU5V3ud8l_Y))

(Just unplug J721)

$make FLASH\_S2\_ASIC1

* + - Re-plug J721 back.
    - Open minicom in another terminal:

$sudo minicom -b 115200 -D /dev/ttyUSB1

* + - Reset ASB board:

$make reset

* + - Start execution.

1. **Known issues**

Sometime, the minicom is cursor is drifted because of timeout in ASIC’s UART HAL firmware.This will be fixed in automation execution.

1. **Limitation**

* Have not implementation the python or shell script to automate with minicom. This script will be release when do regression test.
* Regression test on FPGA-Rev0F have not been executed.
* DMA test scenario has not been defined yet.