

PDPTN5110_ConnectGetCC

```
graph LR; A[PDPTN5110_ConnectGetCC] --> B[PD_TimerCheckInvalidOrTimeOut]; A --> C[PDPTN5110_RegCacheSynC];
```

The diagram illustrates a branching logic flow. A single source node, 'PDPTN5110_ConnectGetCC', is shown on the left. Two arrows originate from its right side, pointing to two separate destination nodes on the right: 'PD_TimerCheckInvalidOrTimeOut' (top) and 'PDPTN5110_RegCacheSynC' (bottom).

PD_TimerCheckInvalidOrTimeOut

PDPTN5110_RegCacheSynC