

ModelSim Intel FPGA Starter Edition

KAIST, School of EE

Computer Architecture and Memory systems Laboratory

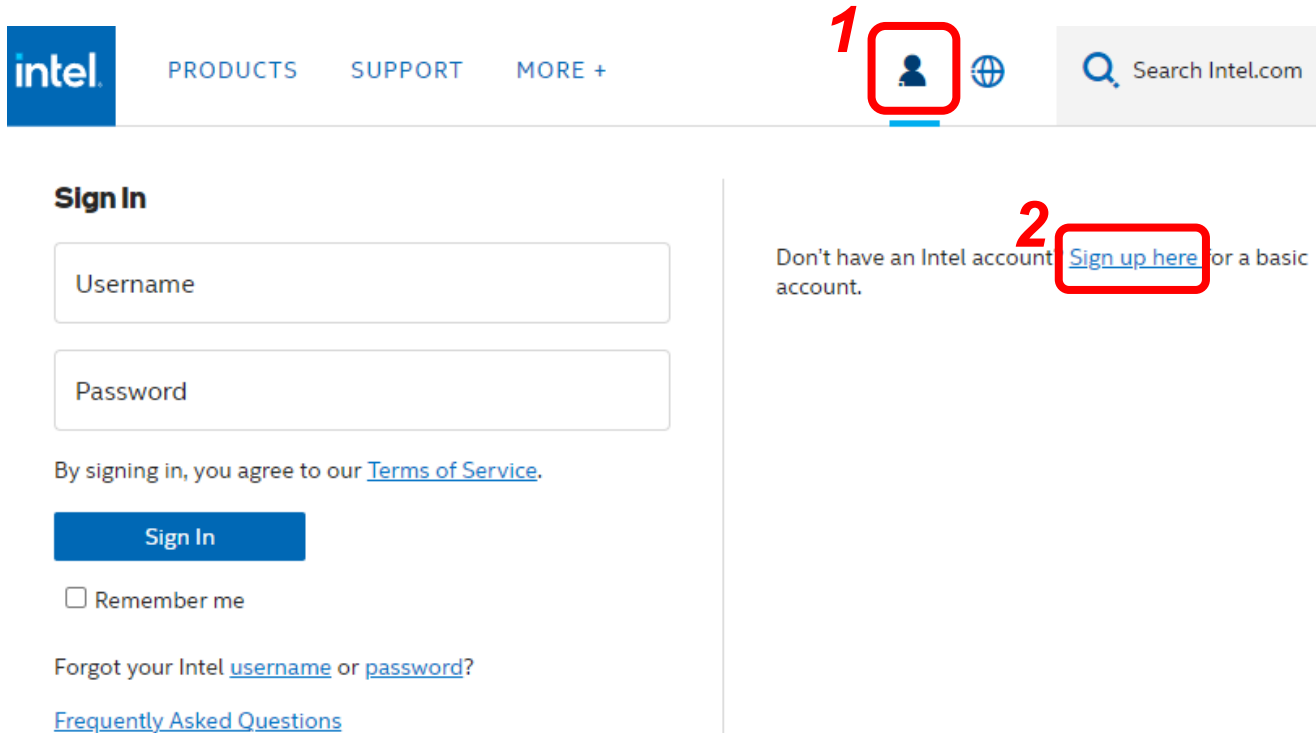
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Sign up Intel Website

- <https://www.intel.com/content/www/us/en/homepage.html#>



The screenshot shows the Intel website's sign-up page. At the top, the Intel logo is on the left, and navigation links for 'PRODUCTS', 'SUPPORT', and 'MORE +' are in the center. On the right, there is a user icon (labeled with a red '1' and a red box), a globe icon, and a search bar labeled 'Search Intel.com'. Below the navigation bar, the 'Sign In' section is on the left, featuring input fields for 'Username' and 'Password', a 'Sign In' button, a 'Remember me' checkbox, and links for 'Forgot your Intel username or password?' and 'Frequently Asked Questions'. On the right, a message says 'Don't have an Intel account' followed by a link 'Sign up here' (labeled with a red '2' and a red box) and 'or a basic account'.

intel. PRODUCTS SUPPORT MORE +

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Sign In

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By signing in, you agree to our [Terms of Service](#).

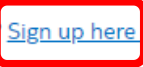
Sign In

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Forgot your Intel [username](#) or [password](#)?

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2 

Sign up Intel Website

- <https://www.intel.com/content/www/us/en/homepage.html#>

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Sign up for a Basic Intel® Account to be able to login to My Intel and start your journey with Intel. You will still need to register for specific programs in order to gain additional privileges. You can look at some other programs we offer [here](#).

Personal Information

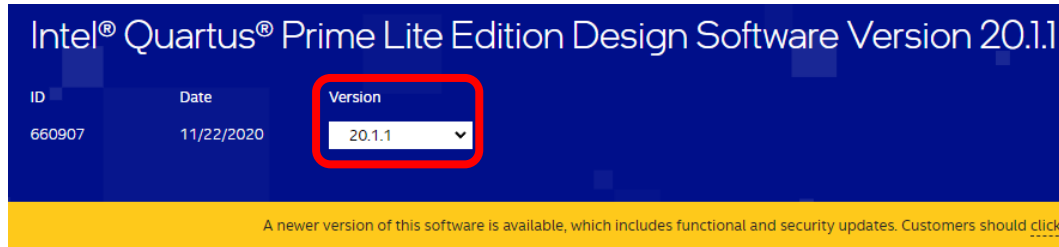
First Name	Last Name	
Business Email Address	Username	
Password	Confirm Password	
Country/Region		
Profession		
Country/Region Code	Phone	Extension (optional)

Next Step

Fill out the registration form

Download

- <https://www.intel.com/content/www/us/en/collections/products/fpga/software/downloads.html?s=Newest&q=lite>



Intel® Quartus® Prime Lite Edition Design Software Version 20.1.1

ID	Date	Version
660907	11/22/2020	20.1.1

A newer version of this software is available, which includes functional and security updates. Customers should [click here](#) to learn more.

Users should upgrade to the latest version of the Intel® Quartus® Prime Design Software. The selected version does not include the latest functional and the [technical recommendations](#) to help improve security. For critical support requests, please contact our [support team](#).

The Intel® Quartus® Prime Lite Edition Design Software, Version 20.1.1 is subject to removal from the web when support for all devices in this release a version are obsolete. If you would like to receive customer notifications by e-mail, please subscribe to our [subscribe to our customer notification mail](#).

[Critical Issues and Patches for the Intel® Quartus® Prime Lite Edition Software, Version 20.1.](#)

[Knowledge Base: Search for Errata](#). Also see [Critical Issues and Patches](#).

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Note that we select “Lite” version
(It does not require a license.)

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Intel® Quartus® Software

ModelSim-Intel® FPGA Edition (includes Starter Edition)

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ModelSimSetup-20.1.1.720-windows.exe

Size: 1.2 GB
SHA1: d484e4c7882fca584a9b0243cbbd74953a4aeb25

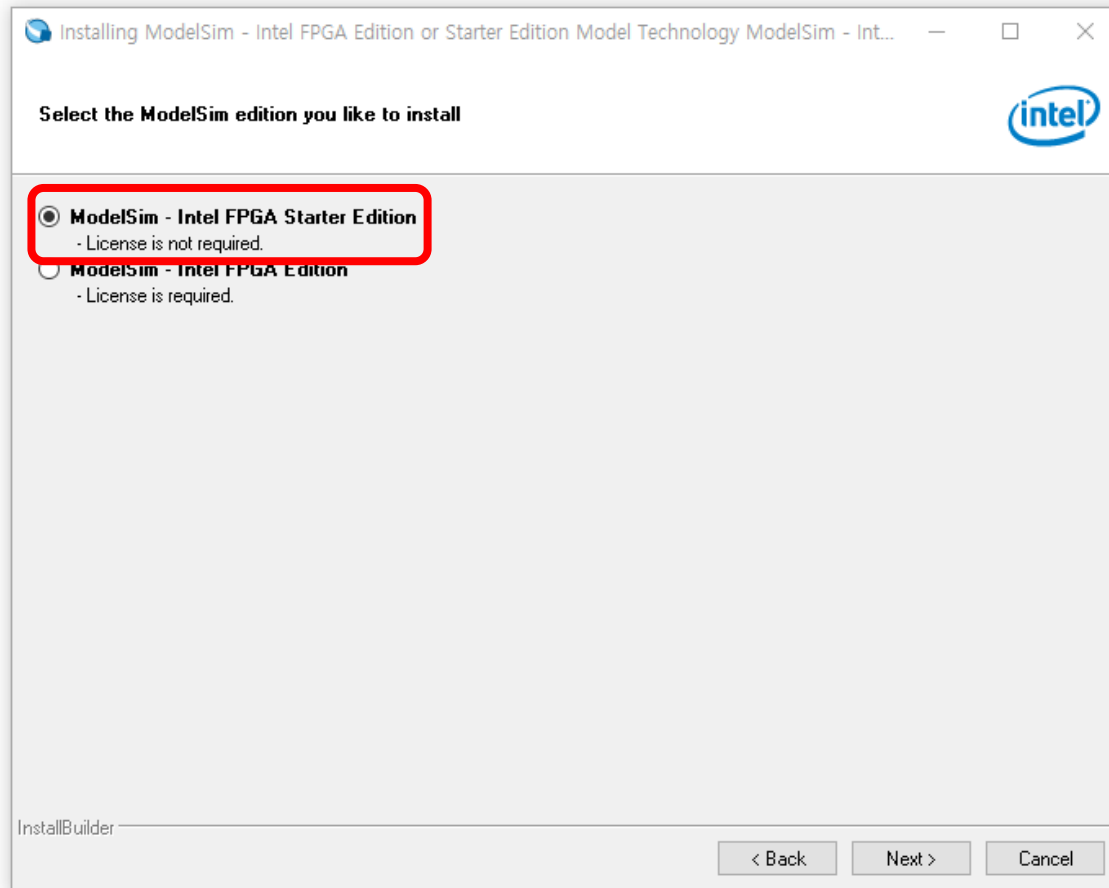
Intel® Quartus® Prime (includes Nios® II EDS)

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QuartusLiteSetup-20.1.1.720-windows.exe

Size: 1.6 GB
SHA1: 5edd76fcafa2a6a40077bc3eeed5bdc95cacdc8

ModelSim Installation

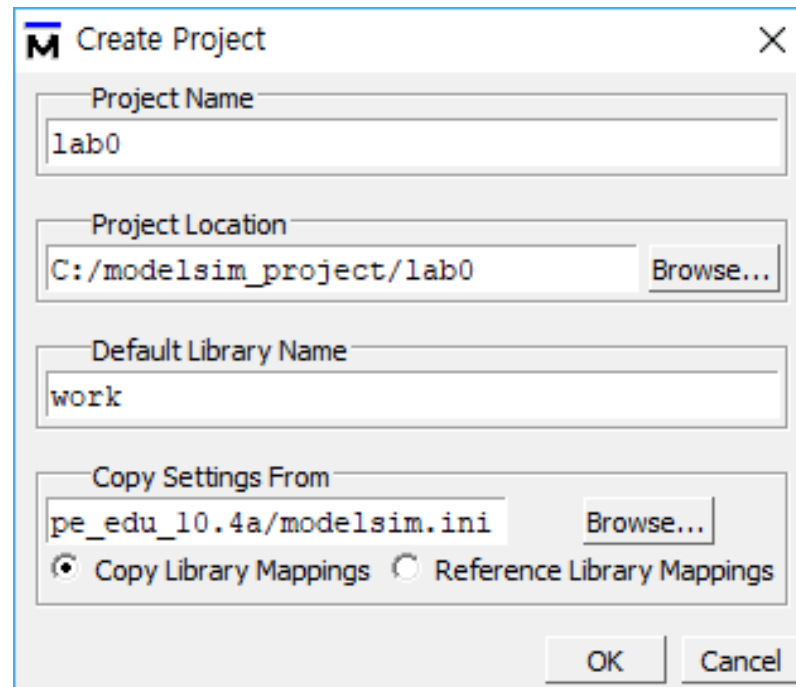
- Select “Intel FPGA Starter Edition” and click next, next, ... until it finishes the installation



[illegible]

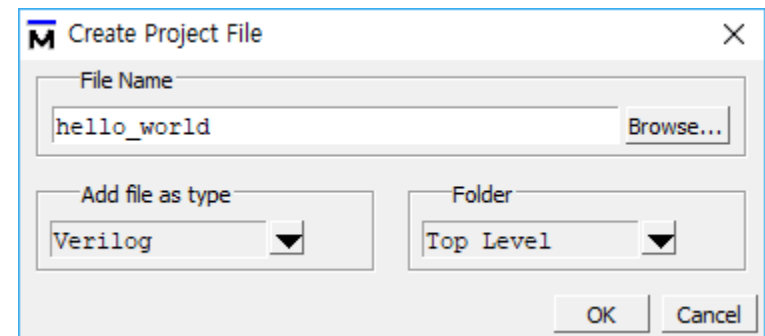
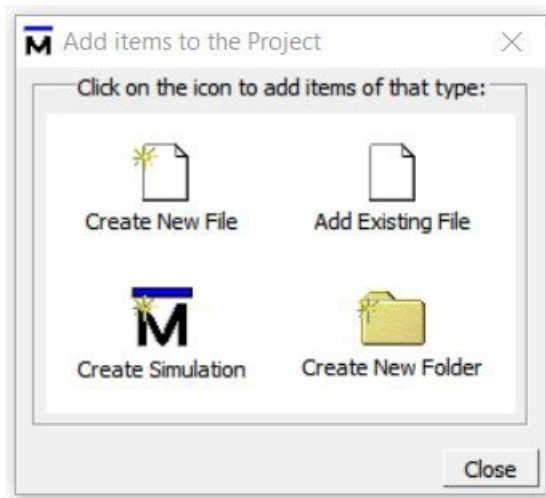
Create new project

- #1. Create “lab0” directory in C:\modelsum_project
- #2. Run ModelSim
- #3. File → New → project



Create new project

- #1. “Add items to the Project” window will pop up
- #2. Click “Create New File”
- #3. Create “hello_world” file with the type of Verilog



Hello World!

- 4-bit synchronous up counter
- Update at clock posedge



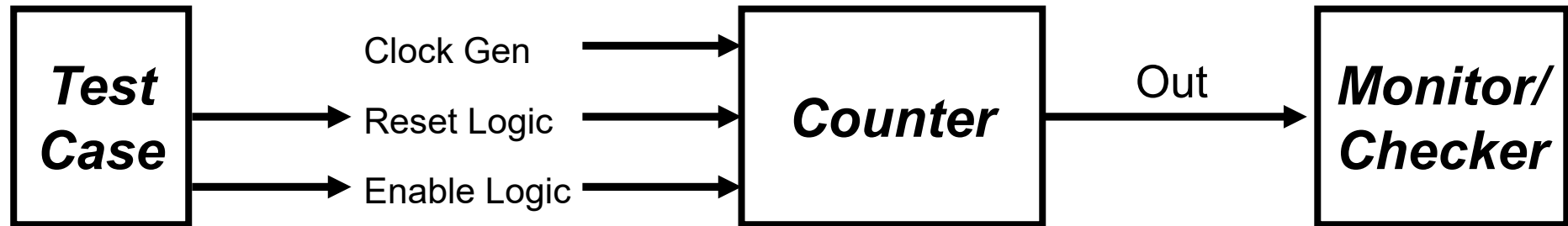
Hello World!

- Copy & Paste Compile!

```
`timescale 1ns / 100ps
module counter (clock, reset, enable, out);
    input      clock;
    input      reset;
    input      enable;
    output [0:3] out;
    reg [0:3] out;
    initial begin
    end
    always @(posedge clock) begin
        if (enable == 1'b1) begin
            if (reset == 1'b1)
                out <= 4'b0000;
            else begin
                out <= out+1;
            end
        end
    end
end
endmodule
```

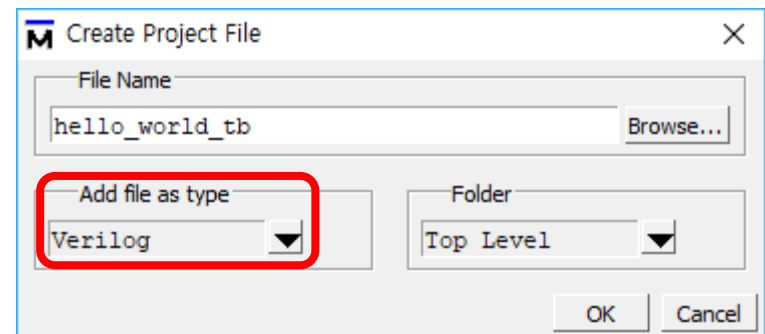
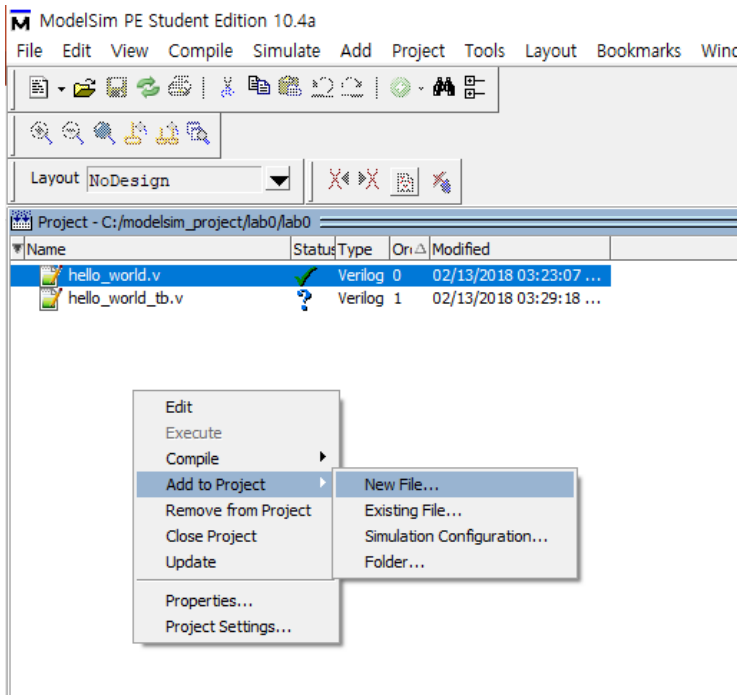
Hello World!

- We need testbench to test our module



Hello World!

- Add new file for testbench to the project, and don't forget the type is Verilog



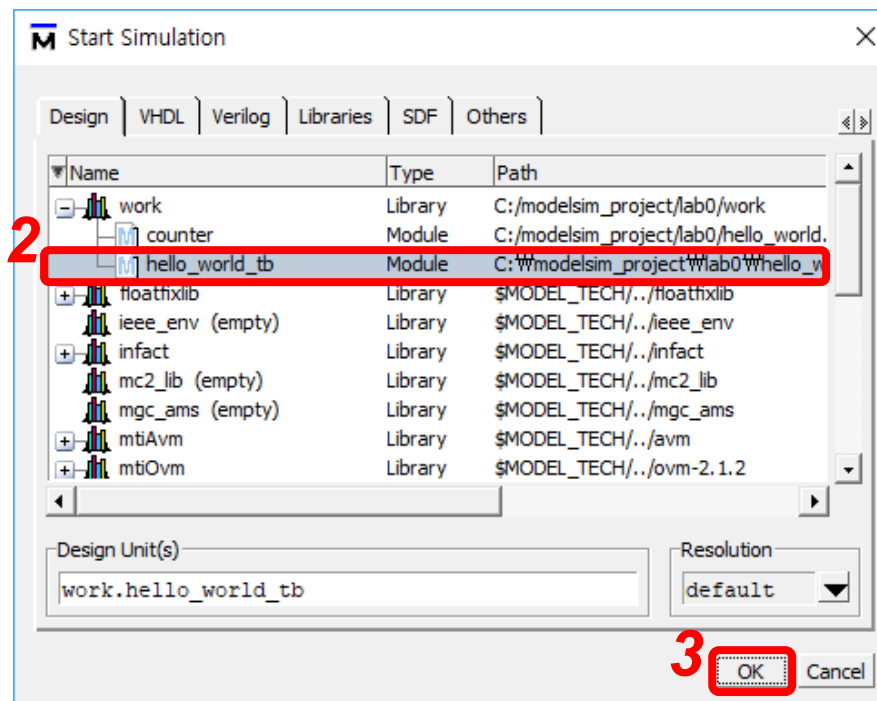
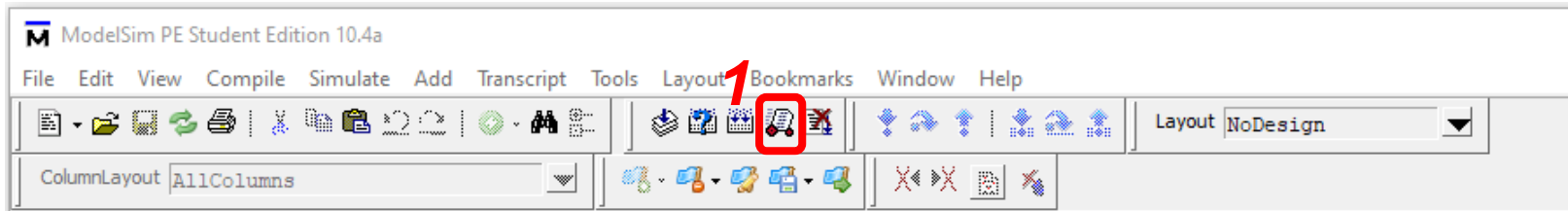
Hello World!

- Copy & Paste Compile!

```
`include "hello_world.v"
module hello_world_tb();
    reg clock_r, reset_r, enable_r;
    wire [0:3] counter_out;
    initial begin
        $display ("time\t clk reset enable counter");
        $monitor ("%T\t %b  %b  %b  %b", $time, clock_r, reset_r, enable_r, counter_out);
        clock_r <= 1;
        reset_r <=0;
        enable_r <= 0;
        #5 enable_r <= 1;
        #5 reset_r <=1;
        #10 reset_r <= 0;
        #100 enable_r <= 0;
        #5 $finish;
    end
    always begin
        #5 clock_r <= ~clock_r;
    end
    counter U_counter (clock_r, reset_r, enable_r, counter_out);
endmodule
```

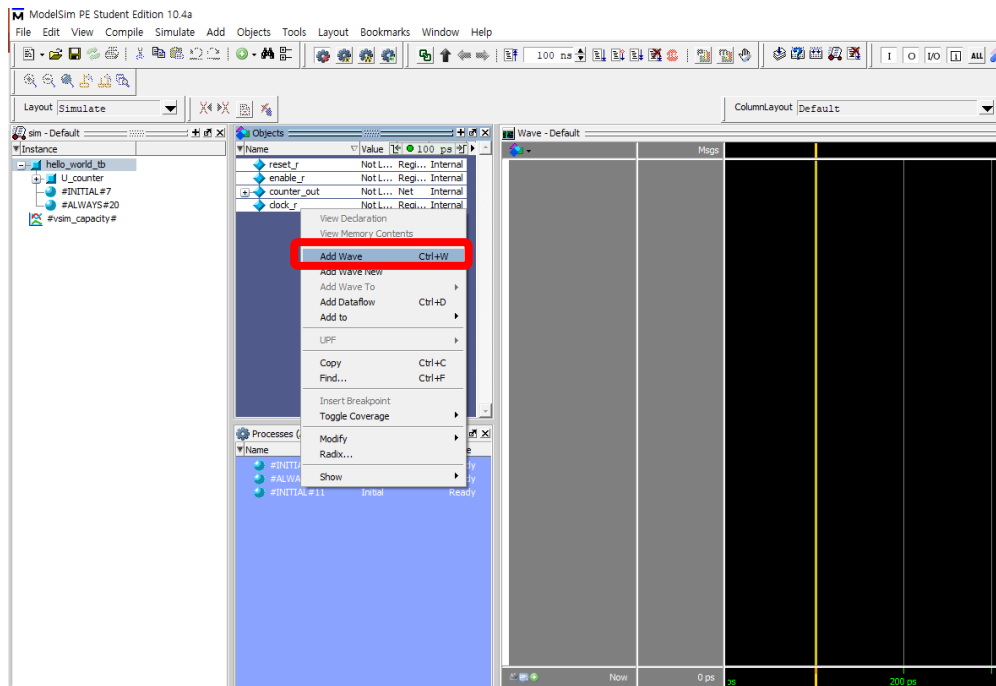
Simulation

- After compile, let's simulate your code

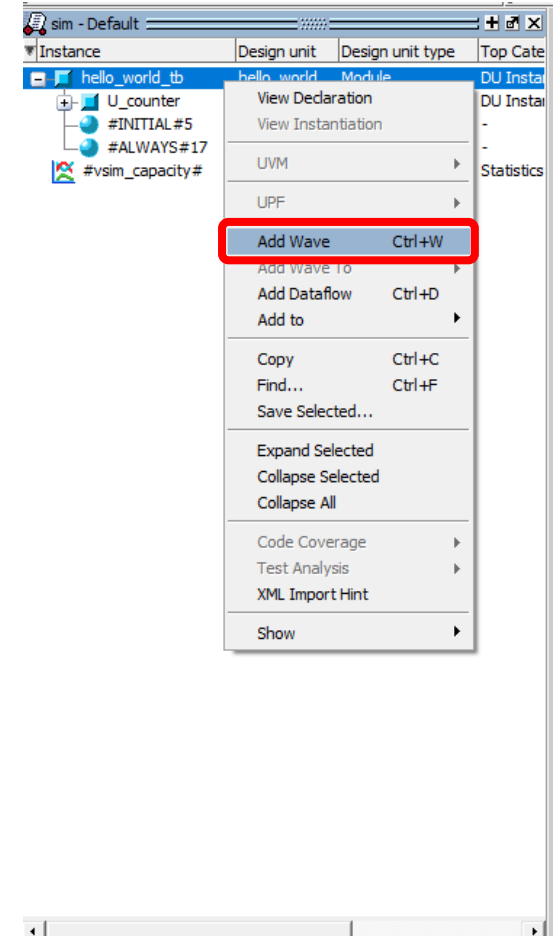


Simulation

- Add waveform using one of the following ways



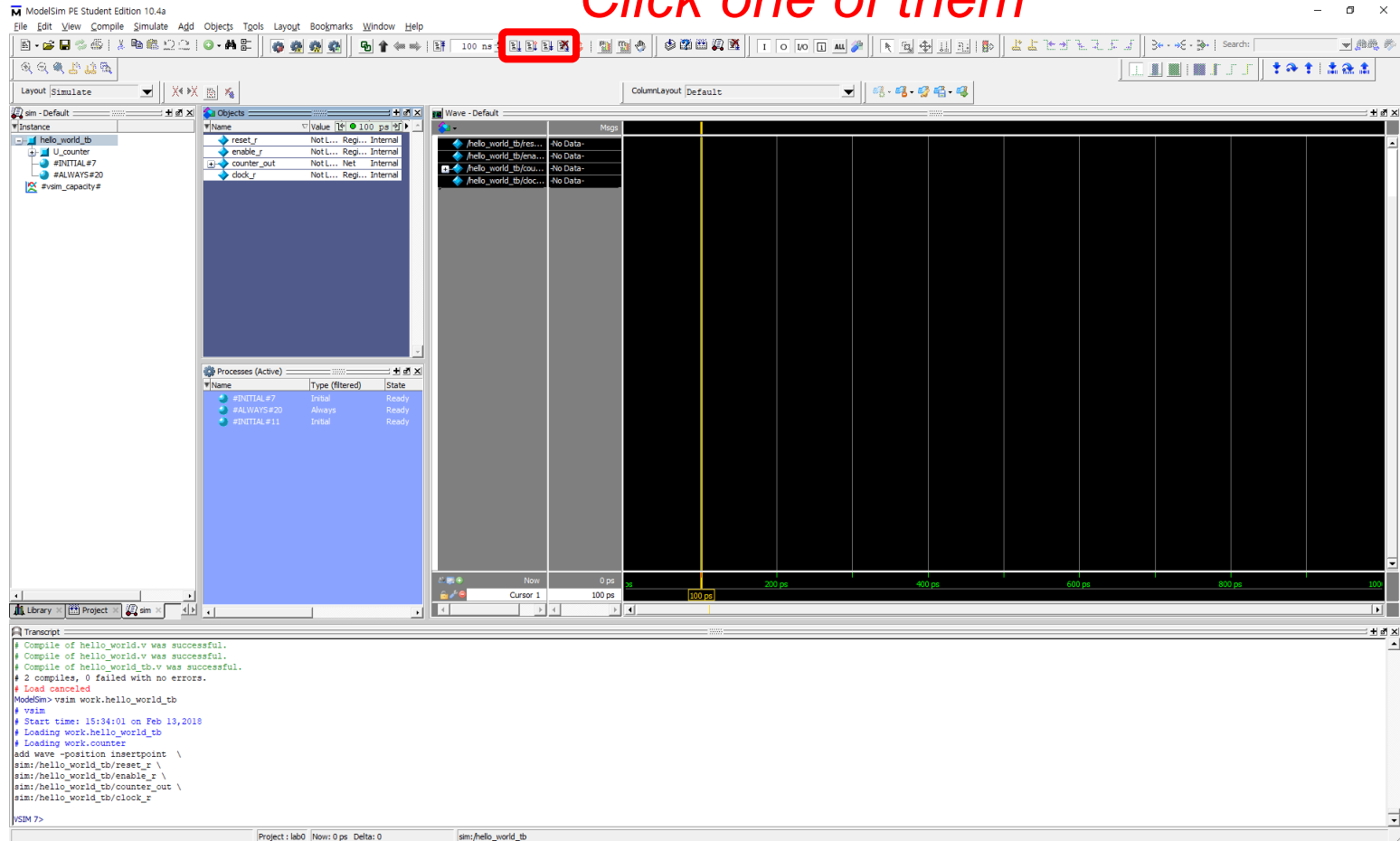
or



Simulation

- Click one of buttons to run or break the simulation

Click one of them



Simulation

- Now, you can see the waveform and output on the “Transcript” tab

