2017 IEEE 24th International Conference on High Performance Computing (HiPC)

Characterization of data movement requirements for sparse matrix computations on GPUs

Süreyya Emre Kurt, Vineeth Thumma, Changwan Hong, Aravind Sukumaran-Rajam, P. Sadayappan
Department of Computer Science and Engineering
The Ohio State University
Columbus, Ohio, USA
{*kurt.29, thumma.6, hong.589, sukumaranrajam.1, sadayappan.1*}*@osu.edu*

***Abstract*—Tight data movement lower bounds are known for dense matrix-vector multiplication and dense matrix-matrix multiplication and practical implementations exist on GPUs that achieve performance quite close to the roofline bounds based on operational intensity. For large dense matrices, matrix-vector multiplication is bandwidth-limited and its performance is significantly lower than matrix-matrix multiplication. However, in contrast, the performance of sparse matrix-matrix multiplication (SpGEMM) is generally much lower than that of sparse matrix-vector multiplication (SpMV).**

In this paper, we use a combination of lower-bounds and upper-bounds analysis of data movement requirements, as well as hardware counter based measurements to gain insights into the performance limitations of existing implementations for SpGEMM on GPUs. The analysis motivates the development of an adaptive work distribution strategy among threads and results in performance enhancement for SpGEMM code on GPUs.

***Keywords*-data-movement bounds, sparse matrix-vector multiplication (SpMV), sparse matrix-matrix multiplication (SpGEMM), graph analytics, hypergraph partitioning, GPU computing**

I. Introduction

Sparse matrix computations are at the core of many compute-intensive applications, both in scientific/engineering modeling/simulation as well as large-scale data analytics. A large number of graph algorithms can also be formulated in the language of sparse linear algebra on semi-rings [1]. The GraphBLAS consortium [2] is defining a sparse linear algebra API intended for such use in developing portable implementations of graph algorithms using efficient implementations of key sparse matrix operations.

The wide ranging uses for sparse matrix operations has resulted in significant recent interest in developing efficient GPU implementations for sparse matrix-vector (MV) multiplication [3], [4], [5], [6], [7] and sparse general matrix-matrix (MM) multiplication [8], [9], [10], [11], [12], [4], [13]. We note that several variants of sparse matrix operations are used, depending on which operands are sparse/dense. In this paper we only consider the following variants for sparse MV and MM: i) sparse-matrix times dense-vector (SpMV), and ii) sparse-matrix times sparse-matrix (SpGEMM).

A surprising fact is that the performance (in GFLOPs) of efficient GPU SpMV implementations [5], [6], [7] is much higher than that achieved by the best current GPU SpGEMM implementations [13]. This is in stark contrast to the dense case, where the performance of matrix-matrix multiplication (a BLAS3 operation) is typically orders of magnitude higher than matrix-vector multiplication (a BLAS2 operation). A primary goal of this work is to attempt to gain insights into why this is the case. *Is the low performance of SpGEMM because of some inherent fundamental bottleneck, such as data movement requirements? If not, is there scope for performance improvement?*

We begin (**Sec. III**) by first documenting performance of dense/sparse MV/MM on an Nvidia Kepler K20c GPU, using a variety of sparse matrices from the Suite Sparse collection [14], [15], drawn from different application domains. We confirm that SpGEMM performance is consistently much lower than SpMV performance.

Focusing on data movement requirements for SpMV and SpGEMM computations, we seek lower bounds as well as upper bounds based on hypergraph partitioning (**Sec. IV**). We explicitly enumerate the complete set of arithmetic operations needed to perform sparse matrix-matrix multiplication as vertices of a hypergraph, with each data element being modeled as a hyperedge incident on all arithmetic operations (hypergraph vertices) that use that data element. By performing hypergraph partitioning, we determine upper bounds for data movement for SpGEMM computation. We find that upper bounds are quite close to lower bounds, while actual data movement in SpGEMM implementations is orders of magnitude higher.

A challenge to gleaning insights into performance bottlenecks for SpGEMM is the fact that data elements from three sparse matrices are used in each elementary operation. Even if two of the matrices are kept the same to perform C = A*A, different rows of A (with different sparsity patterns) are involved. In order to better control the variability and gain insights, we devised a set of experiments to perform SpGEMM on banded matrices, but represented in the CSR representation used in all SpGEMM implementations (**Sec. VI**). Further, each banded matrix was also randomized via a random symmetric permutation of rows/columns.

The experiments with synthetic banded matrices provide useful insights that insufficient concurrency is likely a factor contributing to lowered performance. Using this insight, we devise an adaptive work distribution strategy using virtual warps (**Sec. VII**) for SpGEMM. Experimental results demonstrate that the new SpGEMM implementation achieves better performance than existing GPU SpGEMM codes, including Nvidia's cuSPARSE [3], [4], bhSPARSE [8], [9], KKMEM [16] and HybridSparse [13].

0-7695-6326-0/17/$31.00 ©2017 IEEE
DOI 10.1109/HiPC.2017.00040

The paper makes the following contributions:

- It undertakes a systematic exploration of the data movement requirements for general sparse matrix-matrix multiplication, using a range of matrices drawn from different application domains.
- It uses hypergraph partitioning on explicitly enumerated graphs of the computational operations and data dependences in multiplying various sparse matrices, and demonstrates that there is not some inherent lower bound on data movement that forces SpGEMM to incur much higher data movement than SpMV.
- It uses experimentation with synthetic banded matrices to gain insights into SpGEMM using the scatter-vector approach, and diagnoses inadequate thread-level concurrency as a likely cause of performance loss.
- It devises an adaptive work distribution strategy among threads for a scatter-vector based GPU SpGEMM implementation, resulting in enhanced performance for SpGEMM on GPUs.

II. Background: Sparse MV/MM on GPUs

In this section, we provide background information on challenges in achieving high performance sparse matrix-matrix (SpGEMM) multiplication on GPUs.

A. Dense versus sparse MV

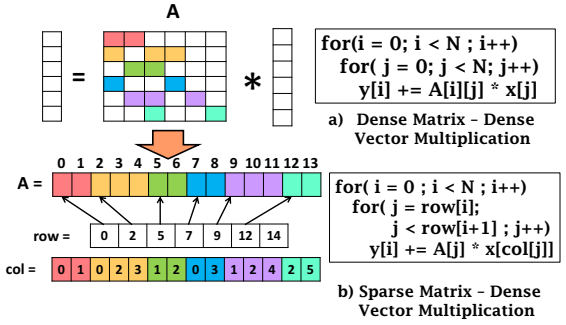

Figure 1. Dense Matrix Vector vs Sparse Matrix Vector Multiplication

Fig. 1 shows code for dense MV (top) and sparse MV (bottom). The overall loop structure is very similar, with an outer loop running over rows of the matrix, and the inner loop performing a dot product of the input vector with one row of the matrix. The main difference is in the representation and access of the rows of the matrix. The figure also shows an example of a sparse matrix in the CSR (Compressed Sparse Row) representation. The non-zero elements are grouped by row and compacted into a long 1-D vector (A) and a parallel 1-D vector (col) holds the column position of the corresponding data element. A third vector (row) holds indexes that point to the start of elements corresponding to each row. In the SpMV code, for processing row i, the inner loop runs over contiguously located data elements in A, from index row[i] to index row[i+1]-1. The needed element of the vector is obtained indirectly using col. Thus, the overall code structure is not very different between dense and sparse MV, with about double the data volume being needed in the sparse case because both the column index and the nonzero element value must be read in from memory; in contrast with dense MV, only the matrix elements need to be read in.

B. Dense versus sparse MM

Algorithm 1: Dense Matrix-Matrix Multiplication

```
   input : DenseMatrix A[M][N], DenseMatrix B[N][P]
   output: DenseMatrix C[M][P]
1  for i = 0 to M-1 do
2      for j = 0 to P-1 do
3          C[i][j] = 0
4          for k = 0 to N-1 do
5              C[i][j] += A[i][k] * B[k][j]
```

Next let us consider dense MM. Simple code for it is shown in Alg. 1, with three nested loops. Two of the three loop indices directly index the row/column of each of the three matrices. Each of the N^2 result elements C_{ij} is computed by accumulating N partial products $A_{ik} * B_{kj}$, for k ranging from 0 to N-1. This code does not show aspects like multi-level tiling necessary to achieve high performance, but illustrates a key characteristic that enables high performance: it is feasible to efficiently index and access the elements of the three matrices due to the simple direct relationship between indices of interacting data elements. Alg. 2 shows

Algorithm 2: Sparse-Matrix Sparse-Matrix Multiplication

```
   input : SparseMatrix A[M][N], SparseMatrix B[N][P]
   output: SparseMatrix C[M][P]
1  for each A[i][*] in matrix A do
2      for each non-zero entry A[i][k] in A[i][*] do
3          for each non-zero entry B[k][j] in B[k][*] do
4              value = A[i][k] * B[k][j]
5              if C[i][j] ∉ C[i][*] then
6                  Insert C[i][j] in C[i][*]
7                  C[i][j] = value
8              else
9                  C[i][j] += value
```

high-level pseudocode for SpGEMM. If the sparse matrices are represented in CSR format, efficient contiguous access to elements in any row is possible, but access to the elements in a column is not efficient. In order to compute the elements of a row i of C, all nonzero elements $A_{i,*}$ must be accessed, and for each such nonzero A_{ik}, all elements $B_{k,*}$ need to be accessed. For each such nonzero element B_{kj}, the product A_{ik}*B_{kj} must be computed and it contributes to a nonzero element C_{ij}.

A significant challenge in computing the sparse matrix product is in efficiently gathering together the various additive contributions to an element C_{ij} from different rows of B. Several approaches have been used to address this "index-matching" problem. One option is to use a hash table to store non-zero elements of C, and the implementation

in the Nvidia cuSPARSE library [3], [4] and a recent implementation by Anh et al. [10] use this approach. An alternate approach has been to implement efficient "row-merge" functionality to merge contributions from two sparse rows. This approach has been used by the implementation of Gremse et al. [11] and the bhSPARSE code from Liu and Vinter [8], [9]. To form row i of the result matrix C, the nonzeros A_{ik} first form vectors of partial products by multiplying with the nonzeros in B_{kj}, and then these sparse vectors of partial products are merged to form the result row $C_{i,*}$. Yet another approach, labeled ESC (Expand-Sort-Compress), was first developed for the Nvidia CUSP library [12], [17]. With this approach, all nonzero partial products $A_{ik}*B_{kj}$ are first formed in parallel and written out as key-value pairs (i,j,value). The huge vector of key-value pairs is then sorted so that key-value pairs with the same row/column indices become adjacent. This is followed by a segmented prefix-sum computation to "compress" the key-value pairs by accumulating the values corresponding to the same row/column index. Finally, yet another approach is to use a dense "scatter-vector" of size N to address the "index-matching" problem. This approach was first proposed by Gustavson [18] for the sequential context. Our prior work in developing the HybridSparse [13] SpGEMM implementation used a combination of the scatter-vector approach and the ESC approach. The scatter-vector approach is a focus also in this paper, and is described in greater detail later on in Sec. VII.

III. Performance of Dense/Sparse MV/MM

In this section, we present experimental data on achieved performance with state-of-the-art GPU implementations of dense/sparse matrix-vector (MV) and matrix-matrix (MM) multiplication. The surprising observation is the consistent reversal in relative performance of the two operations when considering the dense versus the sparse case: For dense matrices, performance of MM is much higher than MV, while the opposite is true for the sparse case.

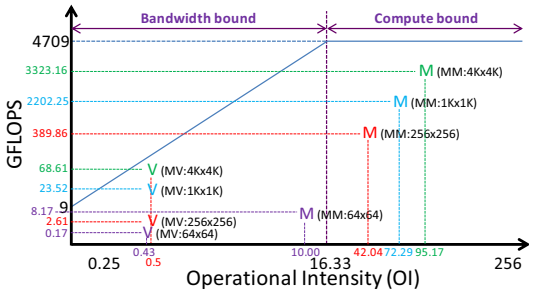

Figure 2. Roofline plot: Dense MV vs Dense MM

A. Performance of Dense MV vs. MM

Fig. 2 shows a roofline plot [19] for an Nvidia Kepler K20c GPU, with data-points for single-precision dense matrix-vector and dense matrix-matrix multiplication using Nvidia's cuBLAS library. A roofline plot provides insightful visual illustration of the extent to which algorithms are constrained by the data-movement bandwidth limits of a system. It contains two asymptotic lines that represent upper bounds on performance: i) the maximum computational rate of processor cores and, ii) the bandwidth from main memory to cores. The horizontal line represents peak computational performance (in GFLOPS), and the inclined line has a slope corresponding to the memory bandwidth (in Gbytes/sec). The y-axis of the roofline plot represents performance (in GFLOPs), while the x-axis represents the "operational intensity" (*OI*) of a computation, defined as the ratio of number of computational operations performed per byte of data moved between main memory and the processor cores. A code will be memory-bandwidth limited unless *OI* is sufficiently high, greater than a "critical intensity" corresponding to the point of intersection of the two rooflines. This is because the product of the *OI* and the peak memory-bandwidth (slope of the inclined roofline) imposes an upper-bound on the number of computational operations that can be performed per second due to the amount of data moved from/to main-memory.

Hardware counters were profiled using the Nvprof profiler for execution of dense MV and MM computations with cuBLAS library calls. For each problem size, the achieved performance in GFLOPS and *OI* (ratio of number of floating-point operations and measured data volume) were computed. The displayed points on the roofline plot show two clusters, one for the MV instances and another for the MM instances. For MV, since two floating point operations are performed per matrix element, the upper-bound on *OI* is 2 operations for 4 bytes transferred for single-precision computation, i.e., 0.5. The achieved *OI* is 0.43, very close to the theoretical limit.

Two conclusions that can be drawn from the roofline plot:

- Dense MV is bandwidth-bound, with achieved performance being quite close to the asymptotic sloping roofline representing the memory-bandwidth-based performance limit.
- Dense MM achieves over 30x performance than dense MV for large matrices, and the computation is clearly compute-bound – for large enough problem sizes, the plotted points are far to the right of the machine balance point where the rooflines intersect.

B. SpMV vs. SpGEMM Performance

We next present similar roofline data for sparse matrix-vector (SpMV) and sparse matrix-matrix (SpGEMM) multiplication using a collection of 25 sparse matrices from the Suite Sparse Matrix Collection [14], [15]. These matrices are drawn from a range of application domains and have been used in recent publications on optimizing SpGEMM [8], [9], [10], [13]. Characteristics of these matrices are provided in Table I. For SpMV, an implementation using the CSR5 variant [5] of the compressed sparse row (CSR) data structure was used. For SpGEMM, we used the HybridSparse [13] code. The matrix product C = A*A was performed using each of the 25 test matrices.

Since plotting the achieved performance at the measured *OI* for these 25 matrices on a roofline plot like Fig. 2 would make it very cluttered, we instead present the same information in a different form in Fig. 3. In the upper

portion of the figure, the achieved performance for SpMV and SpGEMM are shown for all the sparse matrices. In contrast to the dense case, it may be seen that for every matrix the performance (in GFLOPS) achieved by SpMV is higher than that achieved by SpGEMM, with SpMV performance often being over an order of magnitude higher. The lower portion of Fig. 3 displays the achieved *OI* by SpMV and SpGEMM for each matrix (here operations-per-word, rather than operations-per-byte). A theoretical upper-bound for SpMV is 2 flops for two words (value and col-index in CSR format), or an OI_UB of 1.0. Again, the trend is the opposite of that seen for the dense case: the achieved *OI* is always significantly higher for SpMV than SpGEMM. This indicates that many more words of data are moved between main-memory and the cores for each FLOP with the SpGEMM code than the SpMV code. This is so although the theoretical OI upper-bound (ratio of number of operations to the sum of sizes of input and output matrices) is generally larger 0 for SpGEMM than SpMV's OI_UB of 1.0, as seen in Table I.

The following conclusions can be drawn regarding SpMV versus SpGEMM:

- In contrast to the dense case, performance of SpGEMM is considerably lower than performance of SpMV across all tested sparse matrices.
- The measured *OI* for SpGEMM is much lower than the measured *OI* for SpMV, which already is more memory bandwidth bound than dense MV. This is very different from the relative operational intensities achieved by dense MM versus MV.

The above observations raise the following important question: *Is SpGEMM inherently much more constrained than SpMV due to fundamental data movement requirements, or is it the case that even the best existing SpGEMM implementations on GPUs are very far from optimal in terms of data movement?* We begin to address this question in the next section.

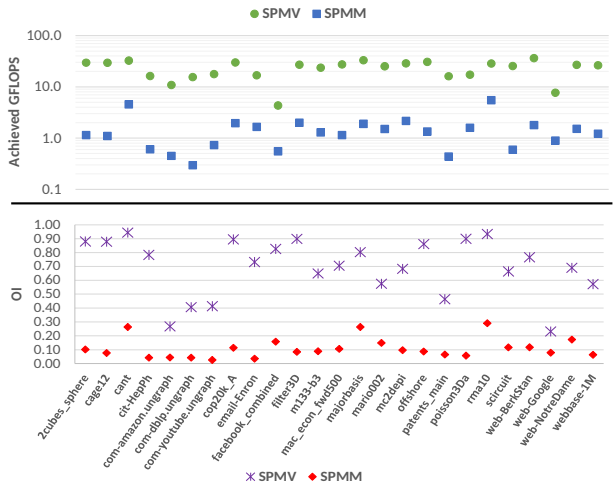

Figure 3. SpMM vs SpMV: Performance and Operational Intensity

Table I
CHARACTERISTICS OF SPARSE MATRICES: C=A*A

Matrix Name	NZ_A (K)	NZ_C (K)	#ops (M)	*OI* _UB
2cubes_sphere	1647	8975	55	2.237
cage12	2033	15232	69	1.794
cant	4007	17440	539	10.587
cit-HepPh	422	3713	13	1.468
com-amazon.ungraph	926	2531	6	0.816
com-dblp.ungraph	1050	4909	14	1.066
com-youtube.ungraph	2988	154931	373	1.166
cop20k_A	2624	18705	160	3.335
email-Enron	368	30492	103	1.649
facebook_combined	88	338	5	5.277
filter3D	2707	20162	172	3.361
m133-b3	801	3183	6	0.670
mac_econ_fwd500	1273	6705	15	0.817
majorbasis	1750	8243	38	1.633
mario002	2101	6450	26	1.204
mc2depi	2100	5246	17	0.888
offshore	4243	23356	143	2.241
patents_main	561	2281	5	0.813
poisson3Da	353	2958	24	3.213
rma10	2374	7901	313	12.371
scircuit	959	5223	17	1.215
web-BerkStan	7601	78351	445	1.213
web-Google	5105	29710	121	2.404
web-NotreDame	1497	16801	129	1.563
webbase-1M	3106	51112	139	3.311

IV. DATA MOVEMENT BOUNDS FOR SPMV AND SPGEMM

For any computation, such as dense matrix-matrix multiplication of a given pair of input matrices, there are many valid schedules for the elementary arithmetic operations that collectively achieve the matrix multiplication. All equivalent schedules perform exactly the same number of arithmetic operations, but can differ very significantly in the number of cache misses incurred. Cache misses cause data to be moved across the levels of the cache/memory hierarchy. For very large problems that cannot fit even in the last level cache (LLC) in the memory hierarchy, the overheads for data movement between main memory and the last-level cache tend to be the most significant for sparse matrix computations. We therefore focus our attention on the data movement between a GPUs global memory and the L2 cache, which is the last-level cache in current Nvidia GPUs.

A. Data Movement Lower Bounds for SpMV and SpGEMM

Consider the execution of an algorithm for matrix-matrix multiplication of a pair of sparse matrices A and B to produce a resulting matrix C. The execution can be viewed in terms of a collection of elementary floating-point additions and multiplications. There will generally be many valid execution schedules corresponding to temporal reordering of the elementary operations. Each non-zero element C_{ij} of the result matrix requires additive accumulation of a number of contributions of the form $A_{ik} \times B_{kj}$ for matching non-zero elements in A and B. These operations can be interleaved in many ways to produce the same final result.

All such valid schedules require exactly the same number of arithmetic operations, but can differ greatly in the number of data movements between the large but slow main memory and the fast but small cache/scratchpad store. It is of great interest to efficiently find valid schedules that minimize the total movement of data between the slow large memory and fast small cache. However, this is in general an open and unsolved problem for most algorithms.

Techniques have been developed to find data movement lower bounds for dense matrix-matrix multiplication [20], which generalizes to sparse matrix-matrix multiplication: $1.72 \times N_{Ops}/\sqrt{C}$, where N_{Ops} is the number of update (multiply-add) operations executed and C is the size of fast memory. However, this bound turns out to be extremely loose compared to a simple data-footprint lower bound - total number of words needed to represent the input and output matrices. Since a CSR representation of a sparse matrix uses two words per nonzero (one for the column index and another for the value of the nonzero element), a lower bound on data volume for $C = A \times B$ is $2*(nnz_A + nnz_B + nnz_C)$.

For SpMV, the data footprint is $2 * nnz$ for the sparse matrix, and $2 * N$ for the two vectors. This data footprint is a lower bound on the minimum possible data movement between main-memory and cache for execution of SpMV.

B. Upper Bounds for SpGEMM

In this section we describe our approach for determining a data movement upper bound for matrix multiplication $C = A \times B$, for specific matrices A and B. The main idea is to "tile" an explicitly enumerated large graph with one vertex for each elementary multiply-add operation needed for the matrix multiplication, and a hyperedge corresponding to each data element in A, B, and C, incident upon all operations using that data element. Loop tiling (also called loop blocking) is a well known optimization for nested loop computations, which changes the order of execution of the instances of the statements from the natural order specified by the iterators of the nested loops to a different one that groups contiguous blocks of statement instances in the multidimensional iteration space. The rationale for tiling is that often statement instances close to each other in the multidimensional iteration space exhibit data reuse. By performing the reordering to execute multidimensional blocks together, data reuse in a limited cache/scratchpad store is enhanced.

In the case of sparse matrices, simply tiling the 3D iteration space for sparse matrix-matrix multiplication with uniform sized tiles is not expected to be effective since different tiles will have highly varied operation counts. Instead, a hypergraph is formed that captures data reuse characteristics and operation reordering is achieved by performing hypergraph partitioning [21]. A hypergraph partitioner such as PaToH [21] places each graph vertex into a partition, with roughly equal number of vertices in each partition and a minimization of the number of inter-partition hyperedges. Thus, wherever possible a hyperedge is fully "internalized" to avoid an edge cut by placing all operations involving the corresponding data element within a single vertex-partition. The hypergraph partition is used to reorder the operations for sparse matrix multiplication to be executed in partition order: first execute all operations in the first partition, followed by all operation in the second partition, and so on. All multiply-add operations for the entire sparse matrix multiplication can be arbitrarily reordered. This is because i) the result elements in C can be formed completely independently of each other, allowing arbitrary interleaving in the multiply-add operations for different C_{ij}, and ii) associativity of addition means that the various multiply-add operations for a specific C_{ij} can also be arbitrarily reordered. Hence, the reordered execution after hypergraph partitioning is a valid execution order for the matrix multiplication.

Ballard et al. [22] used a form of "optimal" hypergraph partitioning of a graph comprised of the elementary arithmetic operations for sparse matrix-matrix multiplication to model data movement lower bounds. In this paper, we use a similar hypergraph partitioning approach, but we use it instead to form data movement upper bounds.

We first define the hypergraph for sparse matrix-matrix multiplication $C = A \times B$. The hypergraph construction is a modified version of the hypergraph construction of Ballard et al. [22]. Let A and B be $I \times K$ and $K \times J$ matrices, respectively. Let S_A and S_B be the sets containing the data elements of matrices A and B. The data elements of S_C are defined as the set containing elements:

$$S_C = \{(i,j) : (i,k) \in S_A \wedge (k,j) \in S_B)\}$$

Vertices $\mathcal{V}$ and Nets $\mathcal{N}$ of the hypergraph are defined as follows:

$$\mathcal{V} = \{v_{ikj} : (i,k) \in S_A \wedge (k,j) \in S_B\}$$
$$\mathcal{N} = \mathcal{N}^A \cup \mathcal{N}^B \cup \mathcal{N}^C$$
$$\mathcal{N}^A = \{n^A_{ik} : (i,k) \in S_A\} \quad n^A_{ik} = \{v_{ikj} : (k,j) \in S_B\}$$
$$\mathcal{N}^B = \{n^B_{kj} : (k,j) \in S_B\} \quad n^B_{kj} = \{v_{ikj} : (i,k) \in S_A\}$$
$$\mathcal{N}^C = \{n^C_{ij} : (i,j) \in S_C\} \quad n^C_{ij} = \{v_{ikj} : (i,k) \in S_A \wedge (k,j) \in S_B\}$$

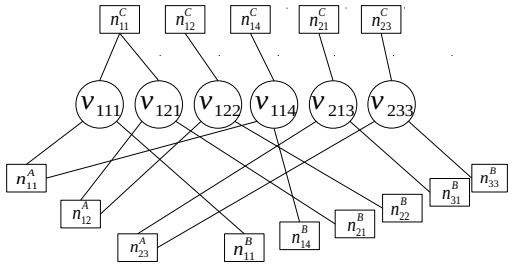

Figure 4. Hypergraph $\mathcal{H}(A,B)$ for $C = A \times B$ where S_A = {(1,1),(1,2),(2,3)} and S_B={(1,1),(1,4),(2,1),(2,2),(3,1),(3,3)}

Figure 4 shows an example of a hypergraph for SpGEMM. Each vertex in the hypergraph represents a multiply-add operation in $C = A \times B$ and each net represents a data element, either in A, B or C, and connects together all elementary operations that use that data element.

A key parameter to a hypergraph partitioner is the number of partitions. Our goal is to perform a partition such that the number of data elements touched by a partition (the

number of incident hyperedges) does not exceed the cache capacity. We use an iterative strategy of performing repeated hypergraph partitions with increasing partition counts until this condition is satisfied.

A data-movement upper bound is computed by adding necessary store and load operations for each partition. With a CSR representation, for each element of A or B, we need to load 2 elements for it (1 load for column index and 1 load for element value). Similarly, for each element of C we associate 3 memory transactions for it (1 load for column index, 1 load for previous element value and 1 store for write-out of final value.

Alg 3 presents the algorithm for upper-bound computation. It partitions the hypergraph $\mathcal{H}(A, B)$ into $\mathcal{P}$ partitions. The minimum possible number of partitions satisfying the cache-size limit for their data footprint is unknown. So we start with $\mathcal{P} = 2$ partitions, and successively double the number of partitions until the cache capacity constraint is met. The loop at line 8 runs through each of the partitions to check for violations of the cache-capacity constraint. The loops at line 9, 12, and 15 accumulate data-footprint counts for each partition, for array A, B, and C, respectively. Two words are accounted for each accessed data element (column index and element value).

Algorithm 3: Find Upper Bound SpGEMM

input : Hypergraph $\mathcal{H}(A, B)$, size of fast memory M
output: Data movement upper bound UB

1 $\mathcal{V} = \mathcal{H}(A, B).getVertices()$
2 $numPar$ = 2
3 $pass$ = false
4 **while** $\neg pass$ **do**
5 $pass$ = true
6 $W_a[*] = W_b[*] = W_c[*] = 0$
7 par = Partition($\mathcal{H}(A, B)$,$numPar$)
8 **for** $0 < p \leq numPar$ **do**
9 **for** $(i, k) \in S_A$ **do**
10 **if** $\exists j, par(v_{ikj}) = p$ **then**
11 $W_a[p] = W_a[p] + 2$
12 **for** $(k, j) \in S_B$ **do**
13 **if** $\exists i, par(v_{ikj}) = p$ **then**
14 $W_b[p] = W_b[p] + 2$
15 **for** $(i, j) \in S_C$ **do**
16 **if** $\exists k, par(v_{ikj}) = p$ **then**
17 $W_c[p] = W_c[p] + 2$
18 **if** $\exists p, W_a[p] + W_b[p] + W_c[p] > M$ **then**
19 $pass$ = false
20 $numPar = 2 \times numPar$
21 **for** $0 < i \leq numPar$ **do**
22 $UB = UB + 2 \times W_a[i] + 2 \times W_b[i] + 3 \times W_c[i]$
23 $UB = UB - |S_C|$

A similar hypergraph partitioning was also performed for the SpMV computation to determine data movement upper bounds.

Fig. 5 presents data-movement upper-bound (UB) data

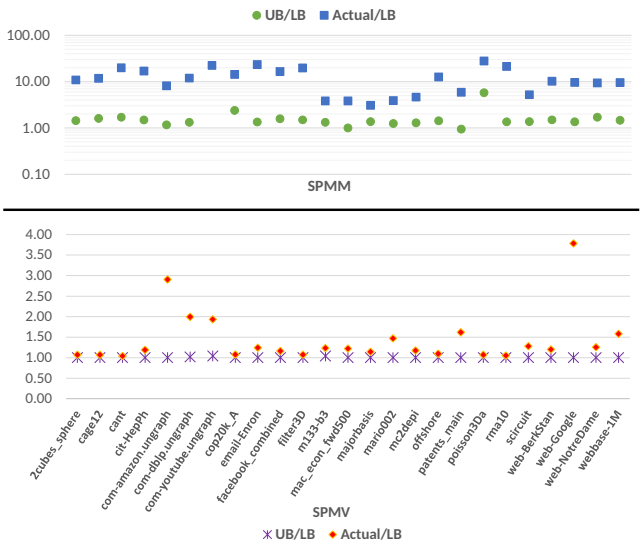

Figure 5. Ratios of Upper Bound and Measured Data Movement to Lower Bound, for SpGEMM and SpMV

from hypergraph partitioning, for SpGEMM and SpMV. Instead of absolute data-movement volume, ratios with respect to lower-bounds on data volume are presented. In addition to the UB/LB ratio, we also present the ratio of actual measured data volume (presented previously in Sec. III in the form of operatonal intensity) to LB.

For SpMV (lower portion of Fig. 5), the UB/LB ratio is very close to 1.0 for all matrices. The measured-volume/LB ratio is also close to 1 for the majority of matrices, indicating that close to the minimal possible data movement is being achieved by the CSR5 SpMV implementation. For a few matrices drawn from social-network domains (e.g., com.amazon-ungraph and web-Google), the measured/LB ratio is very high. This is likely due to multiple uncoalesced accesses to the input vector elements during SpMV.

For SpGEMM too, surprisingly the UB/LB ratio is very close to 1.0 for the majority of matrices. This suggests that the capacity of L2 cache (around 1.5 Mbytes) in the Kepler GPU is sufficient to almost fully reuse data elements in cache, if a suitable reordering of the operations is performed. However, as observed previously, the measured/LB ratio for data volume is very high for most matrices for SpGEMM.

V. Reordering Matrices

We can see from Figure 5 that the data-movement upper-bounds are significantly lower than the measured data movement for SpGEMM. This suggests that a reordered schedule of execution of the elementary operations (operations within a partition performed contiguously) has the potential to greatly reduce the total data movement between main-memory and cache. However, this would require the generation of an explicit schedule of all operations, i.e., a completely unrolled program with as many statements as the total number of arithmetic operations to perform the SpGEMM computation. Instead, we take the following approach: 1) Use the results of the hypergraph partitioning to assign each

row/column of the input matrix A to one of the hypergraph partitions, based on maximum affinity, i.e., the partition containing the most arithmetic operations associated with that row/column; 2) Renumber the rows/column of A based on the partition mapping, so that row/column mapped to a partition are contiguously numbered in the new numbering; 3) Perform a symmetric row/column permutation of A based on the renumbering in the previous step and execute the SpGEMM code to perform the sparse matrix product of the reordered matrix.

Thus, we use the results of the hypergraph partitioning to reorder the original matrix, in the expectation that it could lead to better data locality and improved performance.

Alg. 4 shows pseudocode for the symmetric row/column reordering of a matrix based on hypergraph partitioning. After partitioning of hypergraph $\mathcal{H}(A, A)$, each vertex is assigned to a partition. Majority-voting is then performed for each row/column of the matrix to assign it to a partition. For row/column u, this is done by tallying total counts for each hypergraph partition, of the number of multiply-add operations associated with row/column u (lines 3-7), and assigning it to the partition with the highest tally. The renumbering of row/column indexes is performed by contiguously numbering row/column assigned to each partition, and ordering across the partitions in order of partition id. The count of rows/columns assigned to each partition is first accumulated into vector ptr (lines 9-10), prefix-sum computed (lines 11-12), the permutation vector $reorder$ populated (lines 13-15), and the permuted matrix A_R generated (lines 16-17).

Similarly, matrix reordering was also performed for SpMV, based on partitioning of the corresponding hypergraph.

Algorithm 4: Reorder Matrix For SpGEMM

input : Hypergraph $\mathcal{H}(A, A')$,// A' is deep copy of A
Num. Partitions $numPar$, SparseMatrix A[N][N]
output: SparseMatrix A_R[N][N]

1 par = Partition($\mathcal{H}(A, A)$,$numPar$)
2 **for** $1 \leq u \leq N$ **do**
3 **for** $(u, k) \in S_A \wedge (k, j) \in S_A$ **do**
4 vote[$par[v_{ukj}]$] = vote[$par[v_{ukj}]$] + 1
5 **for** $(k, u) \in S_A \wedge (i, k) \in S_A$ **do**
6 vote[$par[v_{iku}]$] = vote[$par[v_{iku}]$] + 1
7 $index[u]$ = s such that $\forall p$, vote[p] $\leq$ vote[s]
8 ptr[*] = 0
9 **for** $1 \leq u \leq N$ **do**
10 ptr[$index[u] + 1$] = ptr[$index[u] + 1$] + 1
11 **for** $1 < u \leq P$ **do**
12 ptr[u] = ptr[u] + ptr[u-1]
13 **for** $1 \leq u \leq N$ **do**
14 $reorder[u]$ = ptr[$index[u]$]
15 ptr[$index[u]$] = ptr[$index[u]$] +1
16 **for** $\forall (i, j) \in S_A$ **do**
17 $A_R[reorder[i]][reorder[j]] = A$[i][j]

Fig. 6 presents experimental results comparing achieved performance and measured data volume to/from global memory, for both SpMV and SpGEMM. For most matrices, the reordering produces a slight improvement in data volume and performance, with significant changes in a few cases. It is interesting to note that the cases of significant improvement are usually not the same matrices for SpMV and SpGEMM. Overall, these experiments suggest that matrix reordering may potentially have a significant performance impact and exploration of alternate matrix reordering approaches is planned in future work.

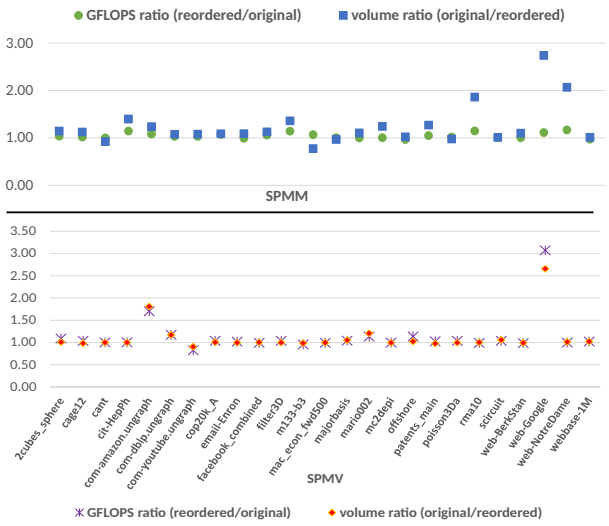

Figure 6. GFLOPS and data volume comparison for SPMM/SPMV on original/reordered matrices

VI. Experiments with Synthetic Banded Matrices

With all previous experiments, with or without matrix reordering, we can make the following observations:

- The actual measured data movement volume for SpGEMM is much higher than the upper bound determined via hypergraph partitioning.
- Even considering the actual measured data movement volume for SpGEMM, the achieved performance in GFLOPs is far from the roofline based on the achieved OI.

The latter observation suggests that inadequate overall concurrency may be a significant factor in low SpGEMM performance. A challenge to gleaning insights into performance bottlenecks for SpGEMM is the fact that data elements from three sparse matrices are used in each elementary operation. Even if two of the matrices are kept the same to perform C = A*A, different rows of A (with different sparsity patterns) are involved. In order to better control the variability and gain insights, we devised a set of experiments to perform SpGEMM on banded matrices, but represented using a CSR representation. Further, a random symmetric row/column permutation was performed for each tested banded matrix, and the randomized variant was also tested.

Fig. 7 presents the results of these experiments. The set of matrices had half-band sizes of 15, 31, 47, 63, 79, 95, and 111. For each matrix and its randomized variant, the stacked

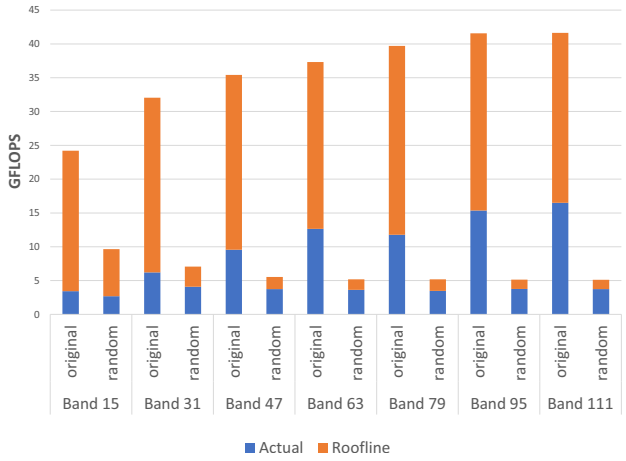

Figure 7. Banded Original vs Randomized

bar-chart shows actual achieved performance (blue) as well as the roofline performance bound based on measured data volume to/from global memory. The main observations are as follows:

- The randomized variants achieve significantly lower performance than the contiguously represented banded matrices. This is a consequence of the significantly worse temporal locality in accessing rows of B for the randomized variant, as well as worse data coalescing for accesses to elements of C with the scatter-vector approach.
- As the band size increases (going from right to left in the chart), the ratio of roofline to actual performance decreases noticeably. This is more prominent for the randomized variants, which have a much higher data volume than the corresponding contiguous variants. This trend is suggestive that inadequate thread-level concurrency is a factor in the low performance of the SpGEMM implementation. As the band size increases, the average degree of concurrency with the scatter-vector approach increases, proportionally with the band size. At high band sizes, execution is closer to a bandwidth-limited regime, as indicated by the lower ratio of roofline performance bound to actual achieved performance.

The latter observation suggests the development of an adaptive work distribution scheme across virtual warps of a thread block, as developed in the next section.

VII. Enhancing Concurrency for SpGEMM

Scatter Vector Approach: Using a "scatter vector" is one approach to solve the index matching problem in SpGEMM. With the scatter-vector approach, a vector of size *n* (where *n* is the number of columns in B) is used to store the pointers to compacted elements in a row of the result matrix "C". The rows of A are processed sequentially. Before processing each row of A, the entire scatter-vector is initialized to a null value. For each element of A in the current row, the corresponding elements of B are identified and partial products are formed. For each such partial product, the corresponding column in the scatter-vector is accessed. If the

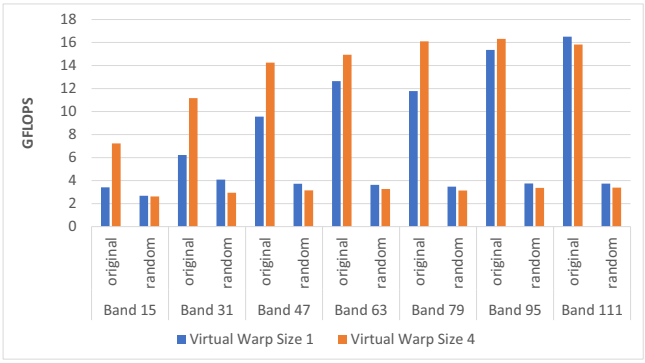

Figure 8. Performance variation with virtual-warp size

scatter-vector contains a non-null value, the current partial contribution is added to the location pointed by the scatter-vector. If the value is null, a new location is obtained from a memory pool and is initialized with the current partial product. The index of the obtained unique location is written to the corresponding column of the scatter-vector. In the rest of this section, we describe enhancements to the scatter-vector implementation in HybridSparse.

As shown in Figure 8, for many matrices SpGEMM performance is far from the roofline limit, indicating that the code may be latency limited. Latency effects can be mitigated by enhancing parallelism. The amount of available parallelism in GPUs is limited by the total number of warps that can be simultaneously active. The "achieved occupancy" metric from "Nvprof" indicates that the kernels achieve near-optimal occupancy. This suggests that even with high occupancy, the effective parallelism is low. We observed that in Figure 8, the gap between achieved GFLOPS and the roofline limit is smaller for larger bands. The reason for this effect is as follows. For each element in a row of matrix A, we assign all the threads in a thread block to process the corresponding elements of B. The number of threads assigned to process each element in a given row of A depends on the total number of operations corresponding to that row (bin id). For example, consider a row of A assigned 128 threads. It may happen that even though the total number of operations to process a row of A is high, the number elements in each accessed row of B is low. Since we process the elements of each row of A sequentially, if the number of elements in the corresponding rows of B is low, many threads will be idle. Note that even though the threads are idle, they have not exited the kernel and so Nvprof reports high occupancy. When compared to matrices with narrower bands, matrices with wider bands have a larger number of non-zeros in each row of B. Hence, fewer threads are idle, resulting in higher performance.

In order to improve effective concurrency, we implemented "virtual-warping". Instead of using all threads in a thread-block in the processing of each row of A, the thread-block is divided into a number of "virtual-warps", and only threads within a virtual-warp participate in processing a row of A. For example, for a thread block of size 128, and virtual-warp-count of 4, each thread block will process 4 rows of A simultaneously. For each row of A, a virtual-warp of 32 (128/4) threads are assigned to cyclically process the

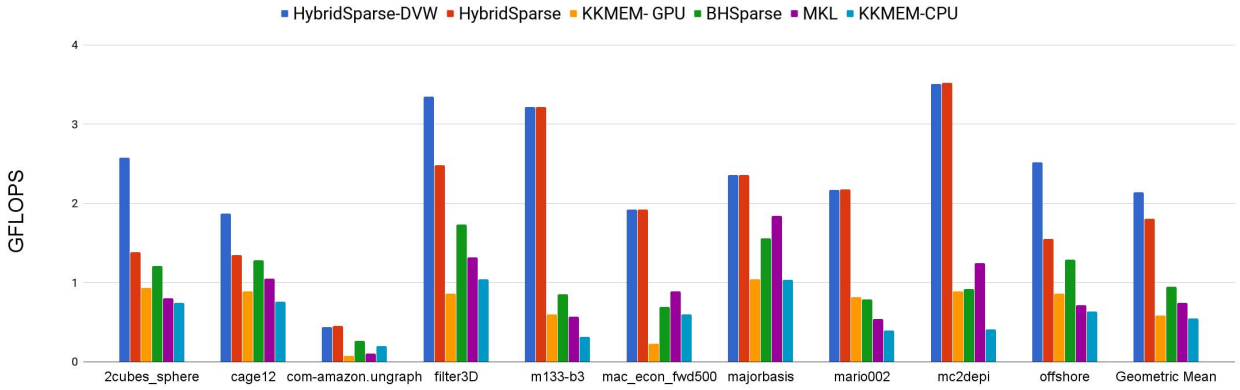

Figure 9. Performance comparision: low-throughput matrices

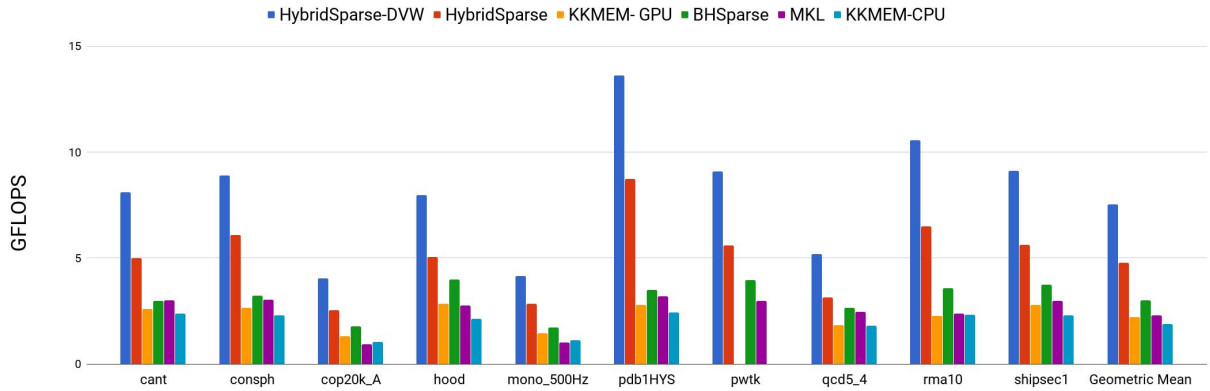

Figure 10. Performance comparision: high-throughput matrices

Table II
HYBRIDSPARSE_DVW VERSUS BHSPARSE FOR 8 PRUNED MATRICES WITH 100K ROWS/COLUMNS

	2cubes_sphere	cage12	filter3D	hood	majorbasis	mario002	mc2depi	pwtk	shipsec1
2cubes_sphere	6.38	3.29	4.16	7.57	2.41	3.8	3.91	7.51	7.14
cage12	4.13	4.27	4.44	-	3.14	4.47	4.45	7.88	-
filter3D	-	-	7.53	7.38	4.11	3.16	3.59	7.43	6.8
hood	6.9	6.81	5.66	10.65	6.51	1.93	1.81	8.63	8.9
majorbasis	3.1	3.6	4.37	9.92	4.2	4.88	5.21	12.49	10.72
mario002	5.41	5.81	4.71	4.42	6.14	5.86	5.87	5.27	5.1
mc2depi	5.53	5.93	4.63	4.02	5.47	6.02	7.17	4.45	4.6
pwtk	8.23	7.71	5.39	9.21	9.02	2.18	2.19	13.88	10.39
shipsec1	7.32	7.25	5.44	8.12	8.28	2.48	2.48	10.18	12.11

corresponding elements in B.

Figure 8 compares performance for virtual-warp-counts of 1 and 4. We note that virtual-warping is not beneficial for all band sizes, which motivates an adaptive scheme. If the virtual-warp-count is greater than 4, then accesses to B elements may be partially uncoalesced. For example, if the virtual-warp-count is 8, then a virtual-warp of 16 (128/8) threads will work on each row of A. The 32 elements of B (corresponding to two rows of A) that are simultaneously processed by a physical warp may not be contiguous, resulting in uncoalesced accesses. If the average number of non zeros in B is greater than 32, then the latter choice may not be beneficial. Consider another example when the average number of non-zeros in B is 128. In this case, a virtual-warp-count of 4 or 1 can achieve fully coalesced access; however the performance of virtual-warp-count of 1 can be better due to the following reason. When the virtual-warp-count is 1, each thread block processes one row of A at a time. In contrast, when the virtual-warp-count is 4, four rows of A are processed at the same time, which increases cache pressure and reduces cache hit rate.

The adaptive virtual-warping scheme determines virtual-

warp-count based on the average number of non-zeros in B for a given row of A. For a given "C" row, the average number of non-zeros in B is determined by dividing the total operations by the number of elements in corresponding row of A.

Fig. 9, 10 present a performance comparison of the new SpGEMM code (HypridSparse_dvw) with other publicly available SpGEMM codes for GPUs (HybridSparse [13], bhSPARSE [8], cuSPARSE [3], KKMEM [16]) and multi-core CPUs (Intel MKL and KKMEM [16]). The GPU was an Nvidia GTX TITAN (14 Kepler SMs, 192 cores/MP, 6 GB Global Memory, 876MHz, 1.5 MB L2 cache, ECC off). The multi-core CPU was a quad-core (8 thread) Intel Core i7-6700K CPU @ 4.00GHz, 8MB L3 cache. We use the set of sparse matrices used in recent GPU-SpGEMM studies, dividing the set into a low-throughput group (Fig. 9) and a high-throughput group (Fig. 10). We do not compare with Nvidia's CUSP or cuSPARSE libraries, since the implementations we compare have shown to be consistently superior to CUSP and cuSPARSE.

The leftmost two bars in the graphs show performance of HybridSparse_dvw and HybridSparse, respectively. HybridSparse_dvw is consistently better than HybridSparse for all high-throughput matrices ((Fig. 10). It is also superior for about half of the low-throughput matrices (Fig. 9) and equal in performance for the other half. The middle two bars in the charts show performance of KKMEM-GPU (third bar from left) and bhSPARSE (fourth bar from left). For all matrices, HybridSparse_dvw is consistently and often significantly faster than either KKMEM-GPU or bhSPARSE. The rightmost two bars show performance on the multicore CPU for KKMEM-CPU (rightmost bar) and Intel MKL (second bar from the right). Again, for all tested matrices, HybridSparse_dvw is consistently faster. However, we note that the peak performance of the multi-core CPU is considerably lower than that of the GPU.

It has been customary in SpGEMM studies to report SpGEMM performance for A*A, where both the matrices are the same. It is more challenging to perform tests for A*B where A and B are selected from a suite like Suite Sparse [15] because the number of columns of A must exactly match the number of rows in B. In order to test performance across differing left/right matrices, we selected eight of the test matrices and extracted the top-left 100K x 100K submatrices, which all have matching sizes but sparsity structure representative of the real matrices. We performed A*B for all combinations, and compared the speedup of HybrisSparse_dvw with bhSPARSE. These results are presented in Table II. It may be seem that while the speedups vary across the test set, HybridSparse_dvw is consistently much faster.

VIII. Related Work

A. Bounds on Data Movement

Techniques have been developed to find schedule-independent lower bounds on the minimal amount of data movement between slow and fast memory [23] for computations abstracted as computational directed acyclic graphs (CDAGs). For dense matrix-matrix multiplication of $N \times N$ matrices on a processor with a cache capacity of C words, a tight lower bound for data movement between main-memory and cache was shown to be $O(N^3/\sqrt{C})$. Scaling constants for the lower bounds on matrix-matrix multiplication were provided by Irony et al. [24] and later improved by Dongarra et al. [20] to $1.72N^3/\sqrt{C}$. This lower bound is also generalizable for sparse matrix-matrix multiplication: $1.72 \times N_{Ops}/\sqrt{C}$, where N_{Ops} is the number of update (multiply-add) operations executed. However this bound is much lower than the simple data-footprint lower bound that we use, as discussed in Sec. IV.

Ballard et al. [22] modeled data movement requirements for SpGEMM using a hypergraph, as we do in this paper. However they model data movement lower bounds for SpGEMM in terms of a minimal-partition hypergraph partitioning that satisfies some constraints, while we use a heuristic-based hypergraph partitioner (PaToH [21]) to determine *upper bounds* on data movement for SpGEMM, as elaborated in Sec. IV.

B. SpMV and SpGEMM on GPUs

Over the last few years, there has been significant interest in developing efficient SpMV and SpGEMM implementations for GPUs, in part because they are key kernels for data analytics.

Nvidia's cuSPARSE library [3], [4] implements multiple SpMV implementations, for a number of sparse matrix formats, including CSR, COO (coordinate format), ELL (ELLPAck format), HYB (hybrid of ELL and COO). The multiplicity of formats is due to the fact that none of CSR, COO, ELL, HYB is uniformly superior in performance; the best format is dependent on the sparsity structure of the sparse matrix [25]. Recent developments have resulted in SpMV implementations that are quite consistently better than all variants in cuSPARSE, including CSR5 [5], Merge-CSR [6], and Hola [7]. In this paper, we use the CSR5 SpMV implementation for our experiments.

As discussed in Sec. II, a significant challenge with SpGEMM relative to SpMV is that of efficient load-balanced "index-matching" and accumulation of multiple additive contributions from products $A_{ik} * B_{kj}$ to form C_{ij}. Different approaches have been devised for this. The earliest efficient SpGEMM implementation was by Gustavson [18], who proposed the use of a scatter-vector for it. HybridSparse [13] is based on a combination of the scatter-vector approach and the ESC (Expand-Sort-Compress) approach. Nvidia's open-source CUSP library [12], [17] also uses the ESC approach. Nvidia's closed-source library cuSPARSE uses hashing to address index-combining [3], [4]. A more recent GPU SpGEMM implementation by Anh et al. [10] also uses hashing. Deveci et al. have developed a performance-portable SpGEMM implementation based on hashing, which can execute on single or multiple GPUs and also on multi-core CPUs [16]. Another approach to index-combining is "row-merging" (discussed in Sec. II), used by an implementation by Gremse et al. [11] and by Liu and Vinter for their bhSPARSE implementation [8], [9]. In this paper, we improve upon the HybridSparse implementation to create the HybridSparse-DVW variant with improved performance. Its

performance is compared with cuSPARSE and bhSPARSE, whose implementations are publicly available.

IX. Conclusion

This paper has attempted to gain insights into the cause of relatively low performance of GPU implementations of general sparse matrix-matrix multiplication relative to sparse matrix-vector multiplication. A significant challenge with the former in comparison to the latter is the challenge of efficiently combining the various additive contributions to result data elements. All devised approaches to this problem cause additional data movement and/or introduce other sources of performance loss, such as hashing/sorting/merging operations, atomics, uncoalesced data access, thread divergence, etc.

An attempt was made to identify any fundamental inherent data-movement bottlenecks for sparse matrix-matrix multiplication. A main conclusion are that the current low performance of SpGEMM implementations cannot be attributed to any fundamental data movement requirements (as is the case for sparse matrix-vector multiplication). Inadequate operation-level concurrency was identified as a cause of performance loss for a scatter-vector based SpGEMM implementation and an improved implementation was devised.

Acknowledgment

This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under Contract D16PC00183, and the National Science Foundation (NSF) through awards 1404995, 1440749, 1513120 and 1629548.

References

[1] J. Kepner, P. Aaltonen, D. Bader, A. Bulu, F. Franchetti, J. Gilbert, D. Hutchison, M. Kumar, A. Lumsdaine, H. Meyerhenke, S. McMillan, C. Yang, J. D. Owens, M. Zalewski, T. Mattson, and J. Moreira, "Mathematical foundations of the graphblas," in *2016 IEEE High Performance Extreme Computing Conference (HPEC)*, Sept 2016.

[2] Graph BLAS Forum. [Online]. Available: http://www.graphblas.org

[3] NVIDIA. (2017) Nvidia cuSPARSE library. [Online]. Available: http://developer.nvidia.com/cuSPARSE

[4] J. Demouth, "Sparse matrix-matrix multiplication on the gpu," in *Proceedings of the GPU Technology Conference*, 2012.

[5] W. Liu and B. Vinter, "Csr5: An efficient storage format for cross-platform sparse matrix-vector multiplication," in *Proceedings of the 29th ACM on International Conference on Supercomputing*. New York, NY, USA: ACM, 2015, pp. 339–350. [Online]. Available: http://doi.acm.org/10.1145/2751205.2751209

[6] D. Merrill and M. Garland, "Merge-based parallel sparse matrix-vector multiplication," in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*. Piscataway, NJ, USA: IEEE Press, 2016, pp. 58:1–58:12.

[7] M. Steinberger, R. Zayer, and H.-P. Seidel, "Globally homogeneous, locally adaptive sparse matrix-vector multiplication on the gpu," in *Proceedings of the International Conference on Supercomputing*. New York, NY, USA: ACM, 2017, pp. 13:1–13:11.

[8] W. Liu and B. Vinter, "An efficient gpu general sparse matrix-matrix multiplication for irregular data," in *2014 IEEE 28th International Parallel and Distributed Processing Symposium*, 2014, pp. 370–381.

[9] ——, "A framework for general sparse matrix–matrix multiplication on gpus and heterogeneous processors," *Journal of Parallel and Distributed Computing*, vol. 85, pp. 47–61, 2015.

[10] P. N. Q. Anh, R. Fan, and Y. Wen, "Balanced hashing and efficient gpu sparse general matrix-matrix multiplication," in *2016 International Conference on Supercomputing*. New York, NY, USA: ACM, 2016, pp. 36:1–36:12.

[11] F. Gremse, A. Hofter, L. O. Schwen, F. Kiessling, and U. Naumann, "Gpu-accelerated sparse matrix-matrix multiplication by iterative row merging," *SIAM Journal on Scientific Computing*, vol. 37, no. 1, pp. C54–C71, 2015.

[12] S. Dalton, L. Olson, and N. Bell, "Optimizing sparse matrixmatrix multiplication for the gpu," *ACM Transactions on Mathematical Software (TOMS)*, vol. 41, no. 4, p. 25, 2015.

[13] R. Kunchum, A. Chaudhry, A. Sukumaran-Rajam, Q. Niu, I. Nisa, and P. Sadayappan, "On improving performance of sparse matrix-matrix multiplication on gpus," in *Proceedings of the International Conference on Supercomputing*. New York, NY, USA: ACM, 2017, pp. 14:1–14:11.

[14] T. A. Davis and Y. Hu, "The university of florida sparse matrix collection," *ACM Transactions on Mathematical Software (TOMS)*, vol. 38, no. 1, p. 1, 2011.

[15] T. Davis. (2017) The suitesparse matrix collection. [Online]. Available: https://sparse.tamu.edu/about

[16] M. Deveci, C. Trott, and S. Rajamanickam, "Performance-portable sparse matrix-matrix multiplication for many-core architectures," in *2017 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, May 2017, pp. 693–702.

[17] S. Dalton, N. Bell, L. Olson, and M. Garland, "Cusp: Generic parallel algorithms for sparse matrix and graph computations," 2014, version 0.5.0. [Online]. Available: http://cusplibrary.github.io/

[18] F. G. Gustavson, "Two fast algorithms for sparse matrices: Multiplication and permuted transposition," *ACM Trans. Math. Softw.*, vol. 4, no. 3, pp. 250–269, Sep. 1978.

[19] S. Williams, A. Waterman, and D. Patterson, "Roofline: an insightful visual performance model for multicore architectures," *Communications of the ACM*, vol. 52, no. 4, pp. 65–76, 2009.

[20] J. Dongarra, J.-F. Pineau, Y. Robert, and F. Vivien, "Matrix product on heterogeneous master-worker platforms," in *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, 2008, pp. 53–62.

[21] Ü. Çatalyürek and C. Aykanat, "Patoh (partitioning tool for hypergraphs)," pp. 1479–1487, 2011.

[22] G. Ballard, A. Druinsky, N. Knight, and O. Schwartz, "Hypergraph partitioning for sparse matrix-matrix multiplication," *ACM Transactions on Parallel Computing (TOPC)*, vol. 3, no. 3, p. 18, 2016.

[23] J.-W. Hong and H. T. Kung, "I/O complexity: The red-blue pebble game," in *Proceedings of the thirteenth annual ACM symposium on Theory of computing*, 1981, pp. 326–333.

[24] D. Irony, S. Toledo, and A. Tiskin, "Communication lower bounds for distributed-memory matrix multiplication," *J. Parallel Distrib. Comput.*, vol. 64, no. 9, pp. 1017–1026, 2004.

[25] N. Sedaghati, T. Mu, L.-N. Pouchet, S. Parthasarathy, and P. Sadayappan, "Automatic selection of sparse matrix representation on gpus," in *Proceedings of the 29th ACM on International Conference on Supercomputing*. New York, NY, USA: ACM, 2015, pp. 99–108.