ECE 425
Lab 1
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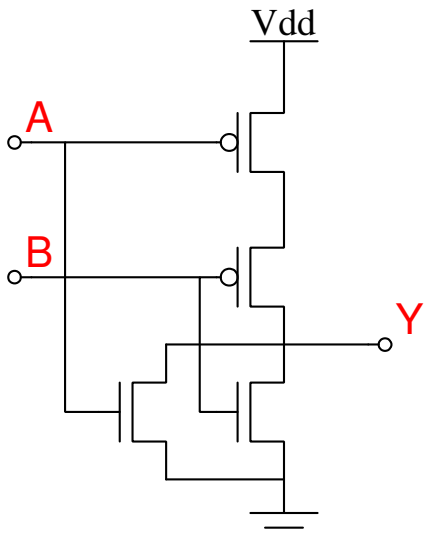


**Fig. 1:** *2 Input CMOS NOR Gate*

This circuit (fig. 1) was simulated in IRSIM to obtain the following waveform (fig. 2):

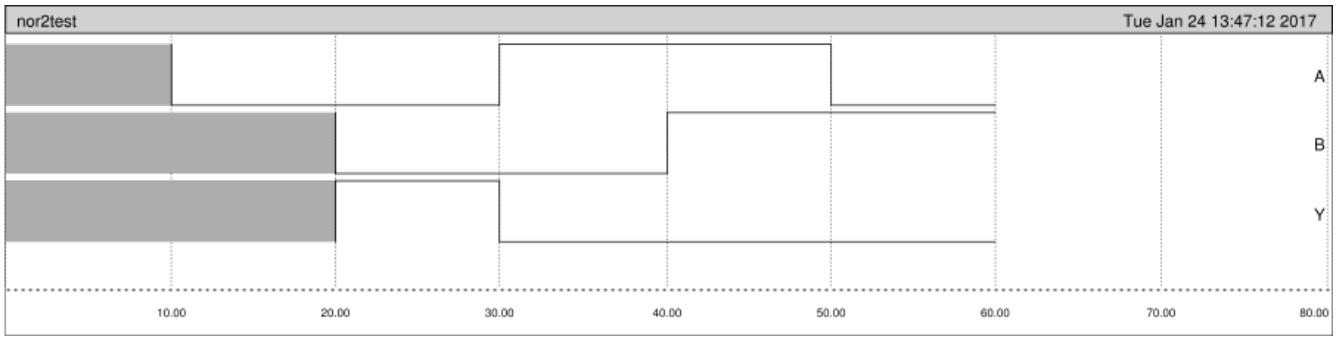


**Fig. 2:** *Simulation Waveform for 2 Input NOR Gate*

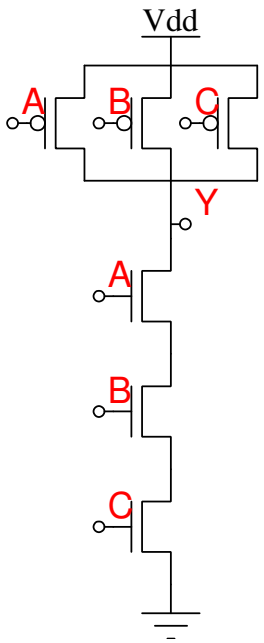


**Fig. 3:** *3 Input CMOS NAND Gate*

This circuit (fig. 3) was simulated using the following IRSIM command file:

```
h Vdd
l GND
vector in A B C
setvector in 000
s
setvector in 001
s
setvector in 010
s
setvector in 011
s
setvector in 100
s
setvector in 101
s
setvector in 110
s
setvector in 111
s
```

The simulation results are shown in fig. 4.

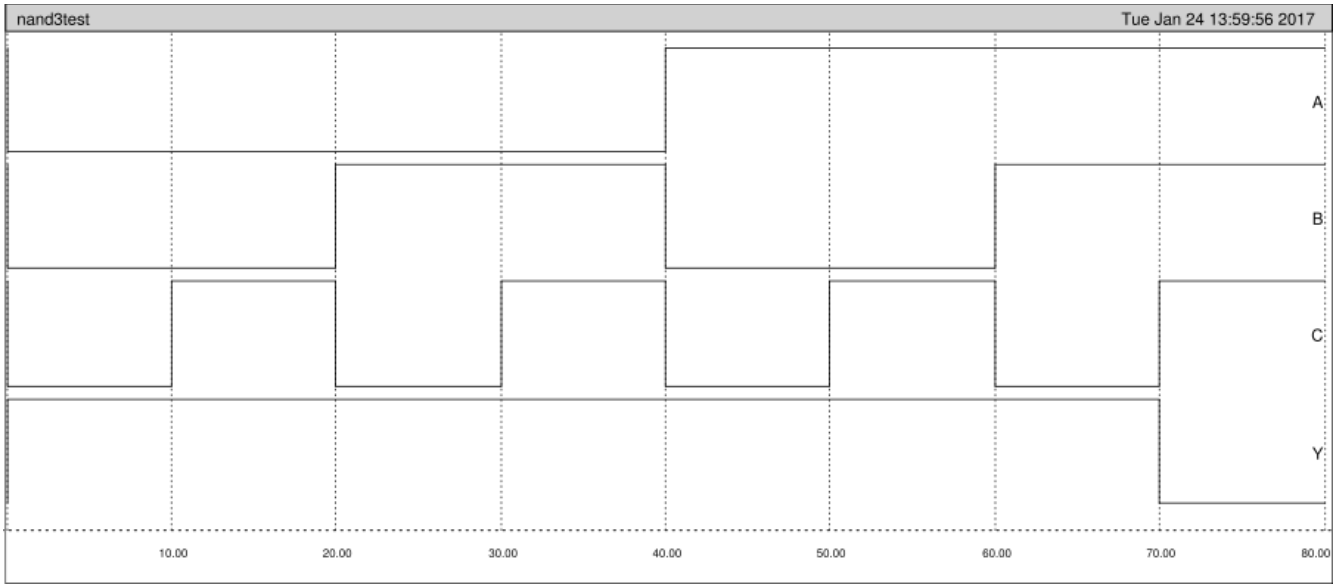


**Fig. 4:** *Simulation waveform for 3 Input NAND gate*

As can be seen, the logical behavior of the gate is consistent with expected NAND behavior (high except when all the inputs are high).