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ECE 425 Final Project
Report 1
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Chip Floorplan

Our proposed floorplan is shown in Fig. 1. It is roughly the same as the original MIPS floorplan, but with some modifications. The first part of the datapath with the instruction registers has been moved to sit on top of the register array. This shortens the overall datapath by 750λ so it can fit within 3000λ. The Controller and ALU Decoder have been replaced with the (approximate) sizes from the synthesized decoders in previous labs. Note that the final version's ALU decoder will also have to handle shift operations, and will therefore need to be somewhat larger than shown.

We have chosen to use a logarithmic shifter, which fits nicely into the datapath slices, though it needs to have twice as many slices, making it have twice the height. Its width was calculated by taking the width of the source generation logic plus the width of 3 2 input muxes. Also, there is interconnect needed, with 4 wiring tracks on the first stage, 3 on the second, and 2 on the third. The source generation logic requires 2 NAND2 gates, a NAND3 gate, and an inverter. The width is then 2(24)+32+16+[4(8)+4]+[3(8)+4]+[2(8)+4]+3(64) which is approximately 375λ.

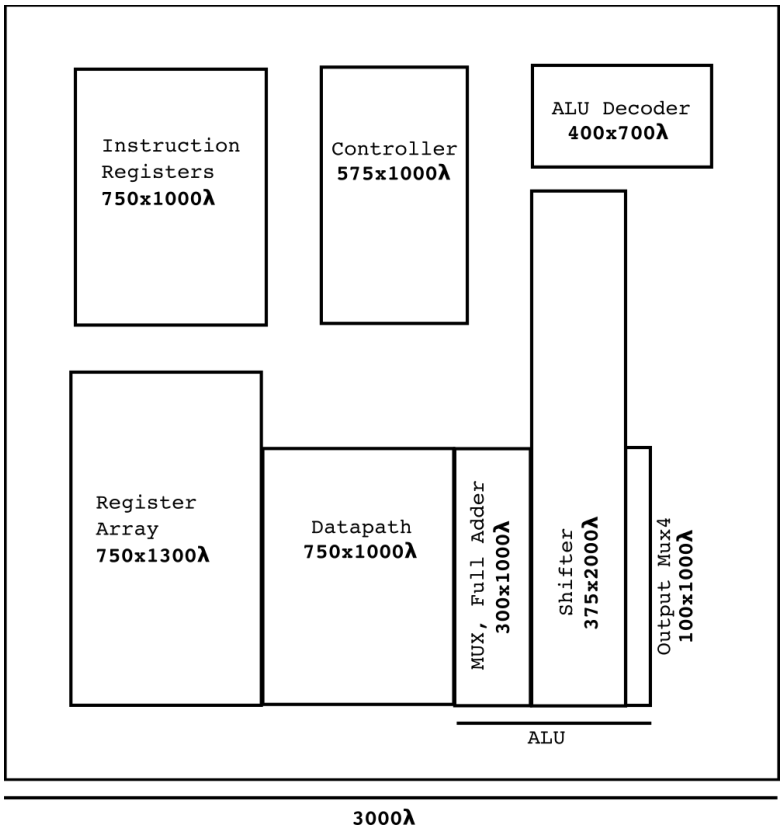

Figure 1: Top Level Floorplan

Below is the updated slice plan of the datapath. The existing signals going into the register file slice were extended and routed into the new location. The updated ALU from Lab4 was added with the current outputs passing over the shifter that we will create. The slices from the shifter were spaced apart to account for the wire tracks that will run between the slices for ease of wiring.

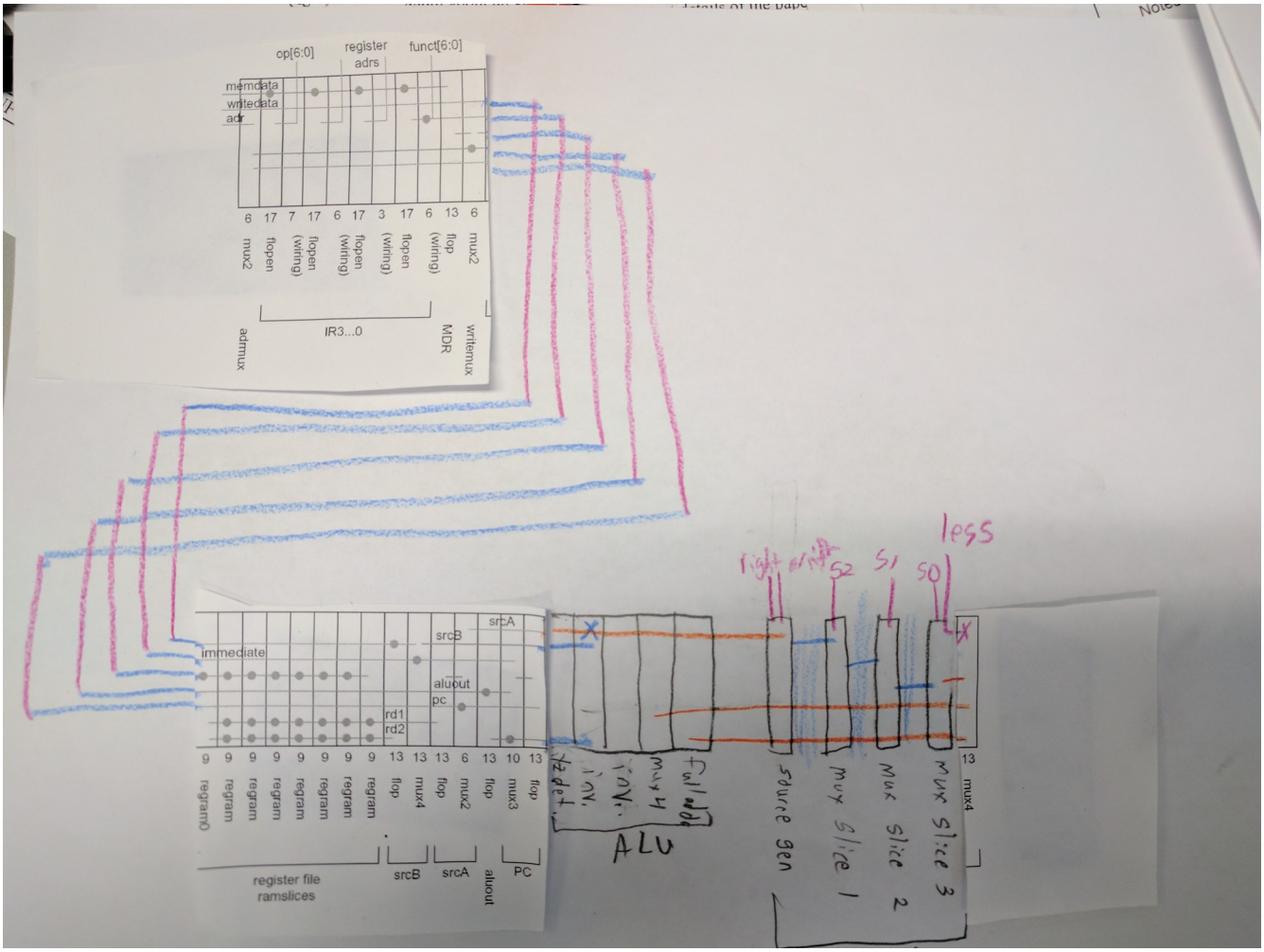

Figure 2: Updated Slice Plan of Datapath