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ECE 425
Lab06
3/7/2017

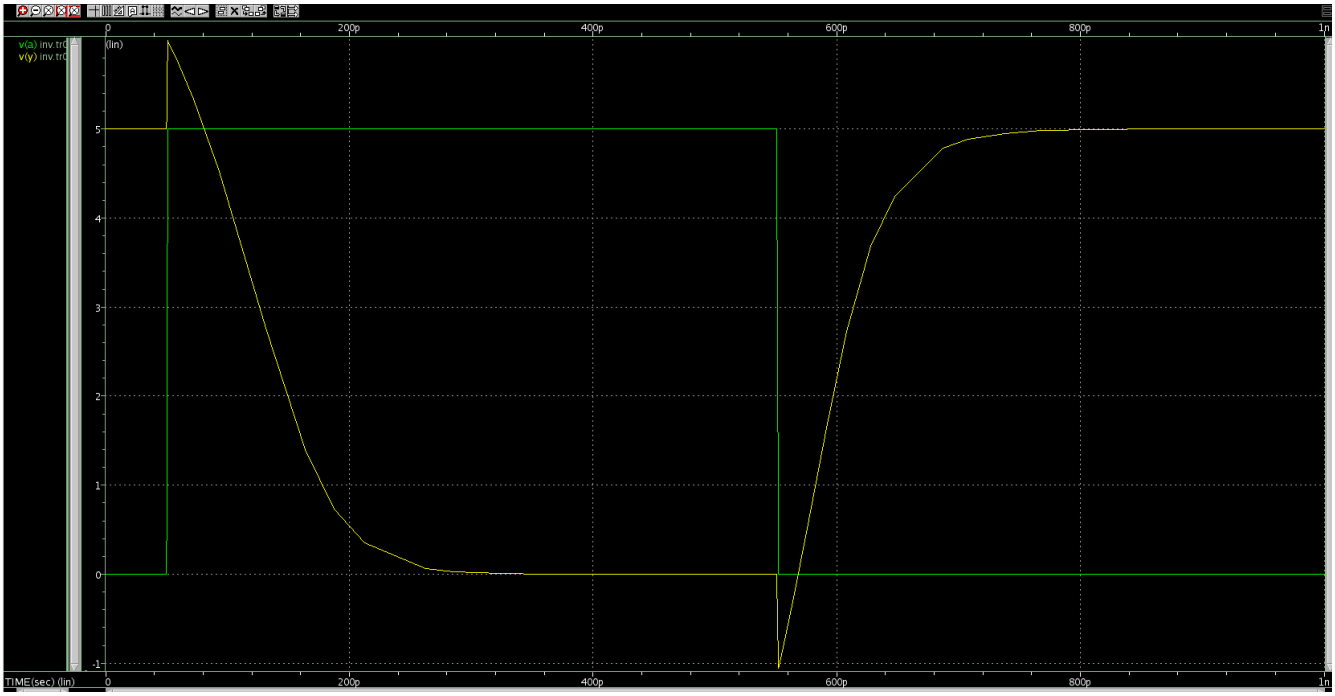

Figure 1: Inv Transient Simulation

This is the waveform for the inverter that was provided in the lecture slides. We tested the switching of HIGH to LOW and then LOW to HIGH.

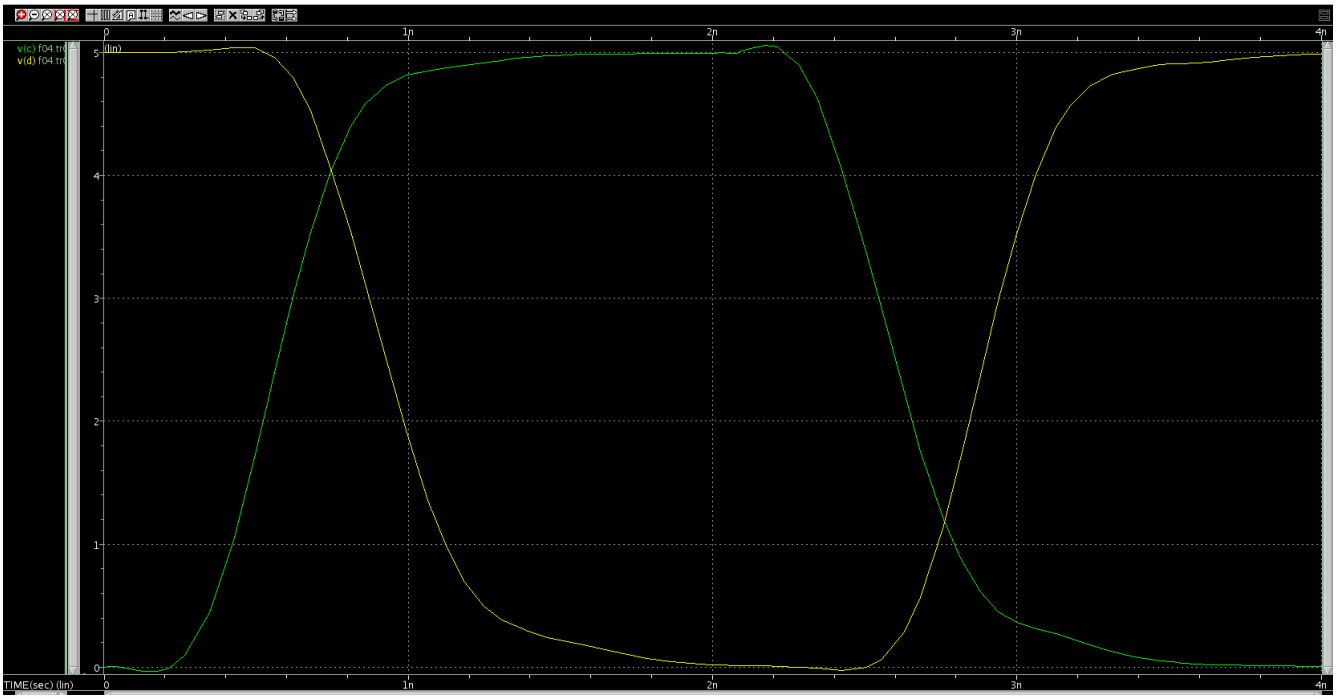

Figure 2: f04 Transient Simulation

This is the simulation for the inverter with realistic driving and loading conditions using other inverters. The yellow signal is the input to the Device Under Test and the green is the output of that inverter. Below we have included the measured rise and fall times along with the propagation delays.

F04.sp transient rise and fall times

tpdr= 291.3731p
tpdf= 355.7412p
tpd= 323.5572p
trise= 323.1150p
tfall= 369.0093p

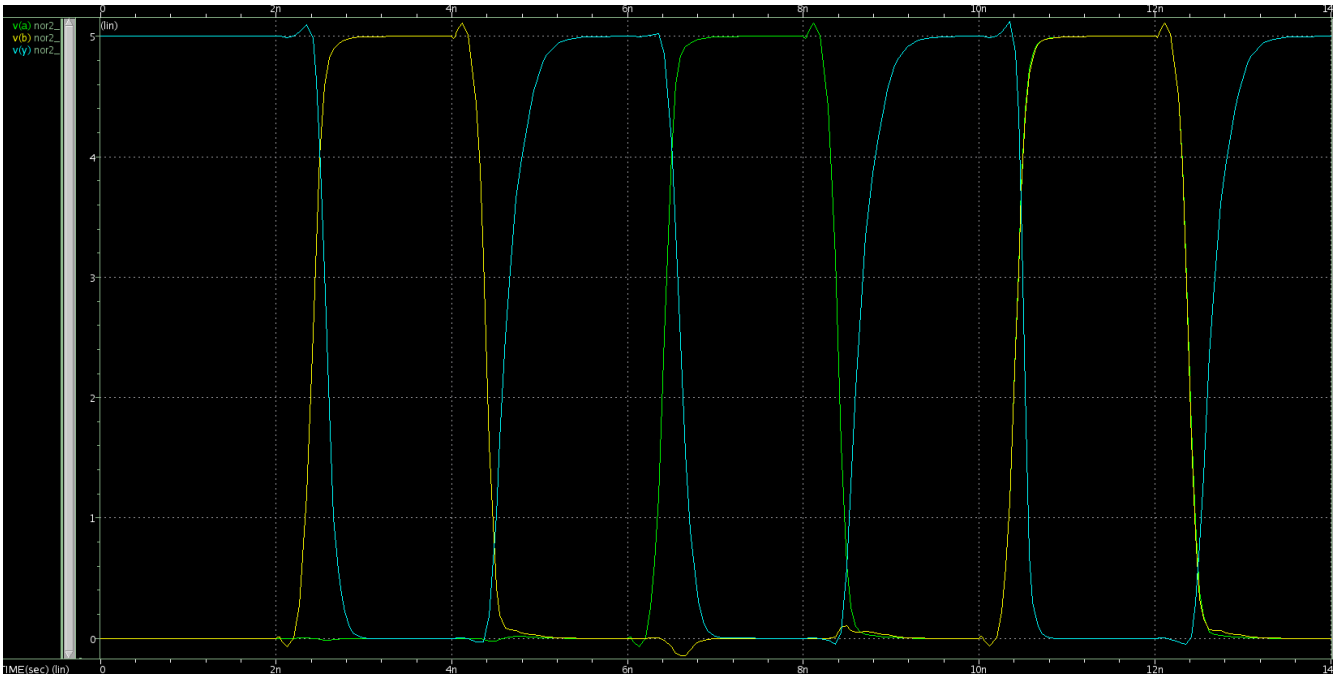

Figure 3: nor Transient Simulation

This is the simulation for the provided nor gate generated by Magic. Each input to the nor gate was loaded with two inverters, the second being four times as large as the first. The yellow signal corresponds to the a input while green is the b input. Blue is the output of the nor gate before the simulated load using a unit inverter. Below are the rise and fall times and propagation delays of the switching signals.

NOR transient rise and fall

00→01→00 transition

tpdf1= 155.1463p targ= 2.5760n trig= 2.4209n
tpdr1= 220.3718p targ= 4.6107n trig= 4.3903n
tpd1= 187.7591p
tfall1= 152.7677p targ= 2.6561n trig= 2.5033n
trise1= 291.4195p targ= 4.7947n trig= 4.5033n

00→10→00 transition

tpdf2= 181.7060p targ= 6.6027n trig= 6.4210n
tpdr2= 238.9959p targ= 8.6319n trig= 8.3929n
tpd2= 210.3509p
tfall2= 194.4458p targ= 6.7033n trig= 6.5089n
trise2= 293.6220p targ= 8.8172n trig= 8.5236n

00→11→00 transition

delay with respect to a

tpdf3a= 90.8924p targ= 10.5115n trig= 10.4207n
tpdr3a= 249.9227p targ= 12.6372n trig= 12.3873n
tpd3a= 170.4075p

delay with respect to b

tpdf3b= 90.0279p targ= 10.5115n trig= 10.4215n
tpdr3b= 252.9185p targ= 12.6372n trig= 12.3843n
tpd3b= 171.4732p

tfall3= 99.0936p targ= 10.5620n trig= 10.4629n
trise3= 293.7825p targ= 12.8214n trig= 12.5276n

Maxes and Mins
Max pdf: 181.7060p (a from 0 to 1)
Min pdf: 90.0279p (a and b from 0 to 1) (b input)

Max pdr: 252.9185p (a and b from 1 to 0) (b input)
Min pdr: 220.3718p (b from 1 to 0)

Max trise: 293.7825p (a and b from 1 to 0)
Min trise: 291.4195p (b from 1 to 0)

Max tfall: 194.4458p (a from 0 to 1)
Min tfall: 99.0936p (a and b from 0 to 1)

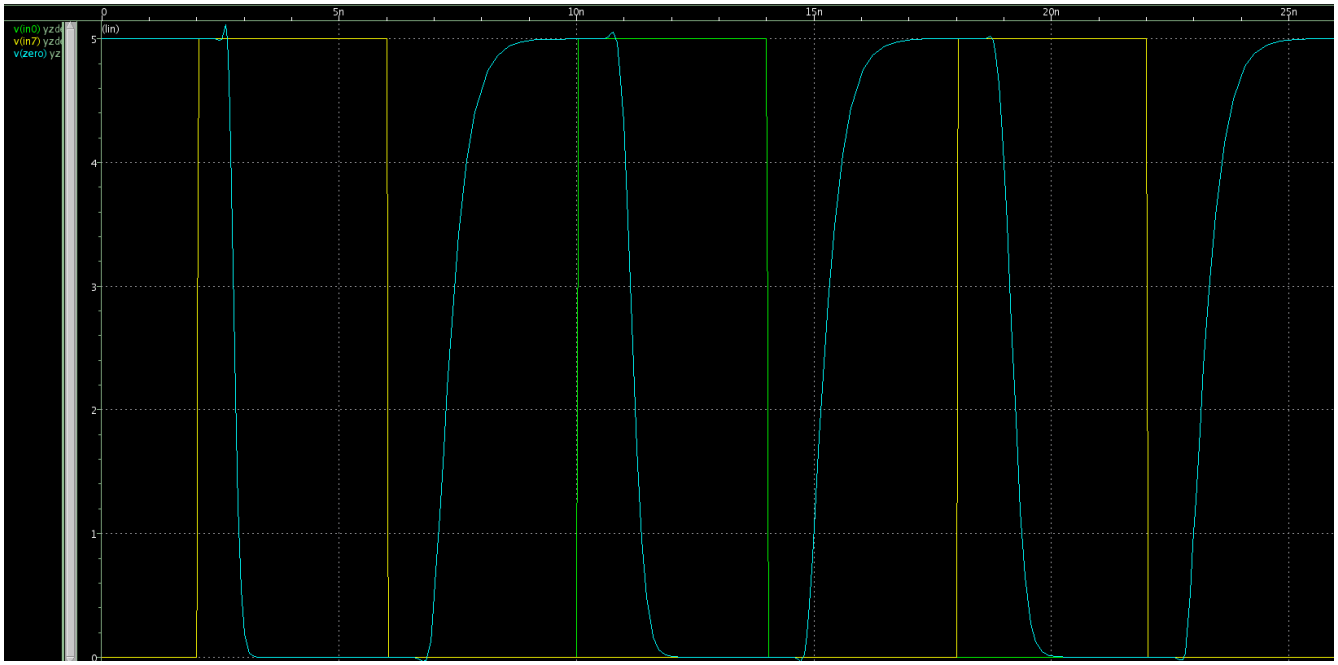

Figure 4: yzdetect Transient Simulation

This is the simulation for the yzdetect circuit. Through the results from the previous part, we hypothesized that changing the a input of one nor gate would cause the max fall time for the output while changing all of the inputs would cause the max rise time. We tested three cases that would result in the extreme cases for verification. The green signal is the a_7 input while yellow is the a_0 input. Blue is the output of the yzdetect. Through analysis of the circuit, we determined that changing one of the inputs while all others remain zero would cause the output to change with only one path driving the output. With all inputs changing, the output would again change but with all paths driving the output. All other cases between these would be intermediate and we would not expect them to be maxes or mins.

yzdetect

00000000→11111111→00000000 transition
tpdf1= 383.6665p targ= 2.8038n trig= 2.4201n
tpdr1= 949.7964p targ= 7.3351n trig= 6.3853n
tpd1= 666.7314p
tfall1= 169.7229p targ= 2.8953n trig= 2.7256n
trise1= 593.0496p targ= 7.6860n trig= 7.0930n
00000000→00000001→00000000 transition
tpdf2= 771.1142p targ= 11.1884n trig= 10.4173n
tpdr2= 845.2096p targ= 15.2339n trig= 14.3886n
tpd2= 808.1619p
tfall2= 336.2699p targ= 11.3630n trig= 11.0267n
trise2= 593.3065p targ= 15.5874n trig= 14.9941n
00000000→10000000→00000000 transition
tpdf3= 763.9977p targ= 19.1813n trig= 18.4173n
tpdr3= 848.5642p targ= 23.2330n trig= 22.3844n

tpd3= 806.2810p
tfall3= 379.0049p targ= 19.3768n trig= 18.9978n
trise3= 597.6559p targ= 23.5914n trig= 22.9937n

Maxes and Mins
max pdf: 771.1142p (a0 from 0 to 1)
min pdf: 383.6665p (everything 0 to 1)

max pdr: 949.7964p (everything 1 to 0)
min pdr: 845.2096p (a0 from 1 to 0)

max trise: 597.6559p (a7 1 to 0)
min trise: 593.0496p (everything 1 to 0)

max tfall: 379.0049p (a7 0 to 1)
min tfall: 169.7229p (everything 0 to 1)

Problems Encountered:
We had a difficult time initially determining the syntax for the PWL voltage source in SPICE. We were seeing linear changes of signals instead of plateaus. All other issues encountered were user error syntax mistakes in SPICE code. We spent approximately 3 hours on this lab and the report.