Ian Miller, Christer Hoeflinger
ECE 425 Lab 8\
Mar 28 2017

Part 1: Counter

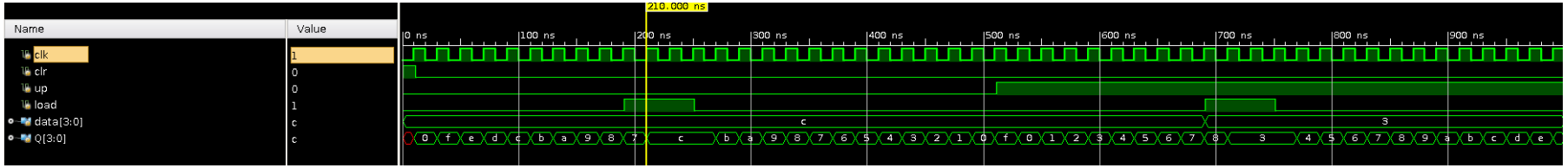


Figure 1: Modified Counter Simulation

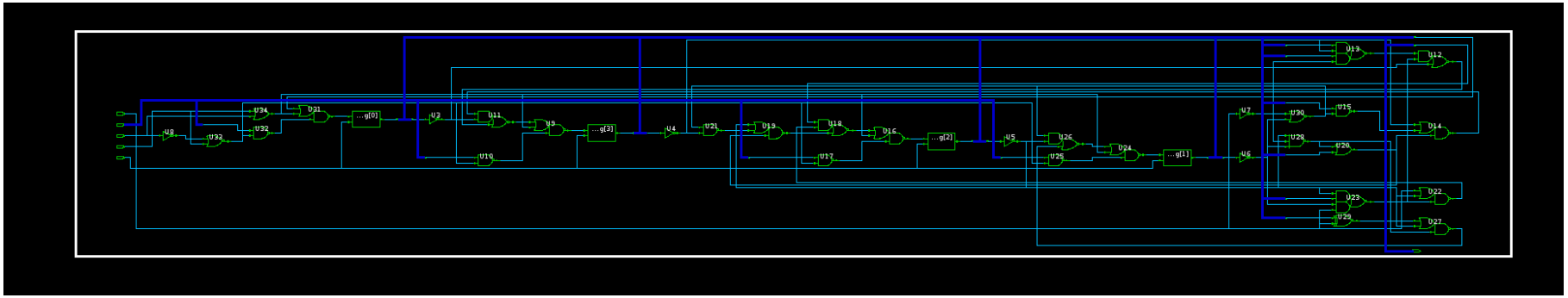


Figure 2: Modified Counter Circuit Diagram

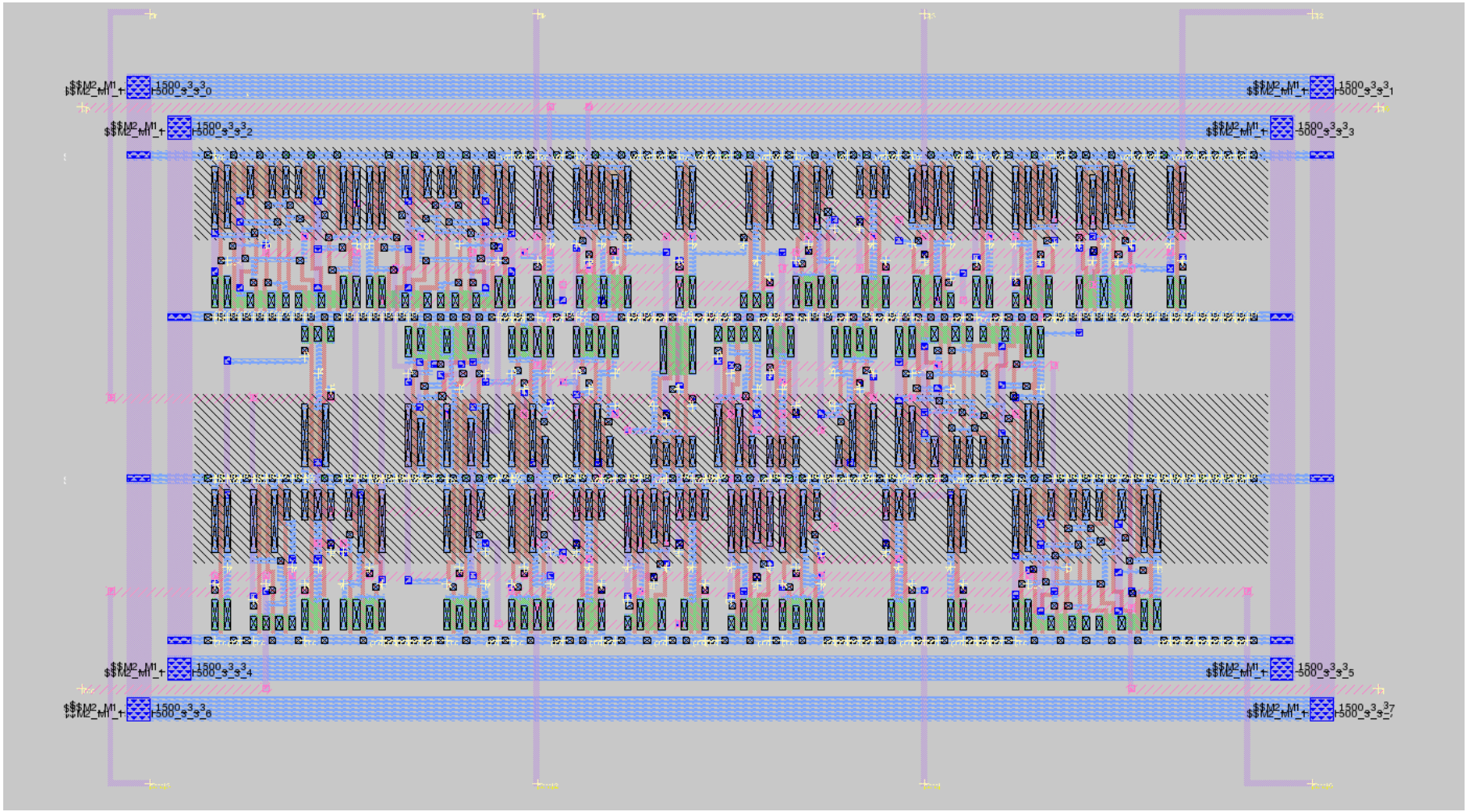
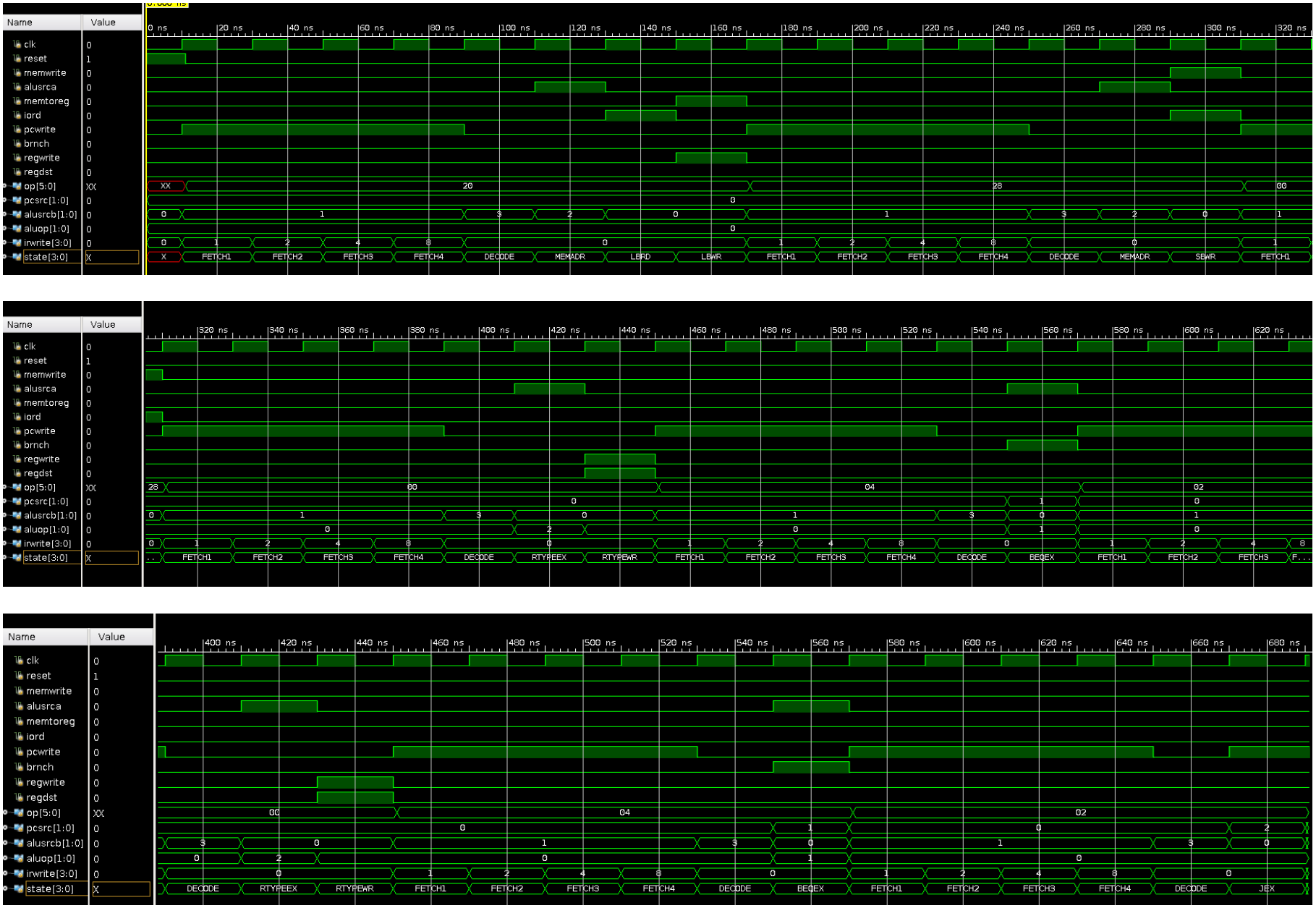


Figure 3: Modified Counter Layout

Part 2: MIPS FSM



MIPS FSM Simulations (note there is some overlap in the waveforms)

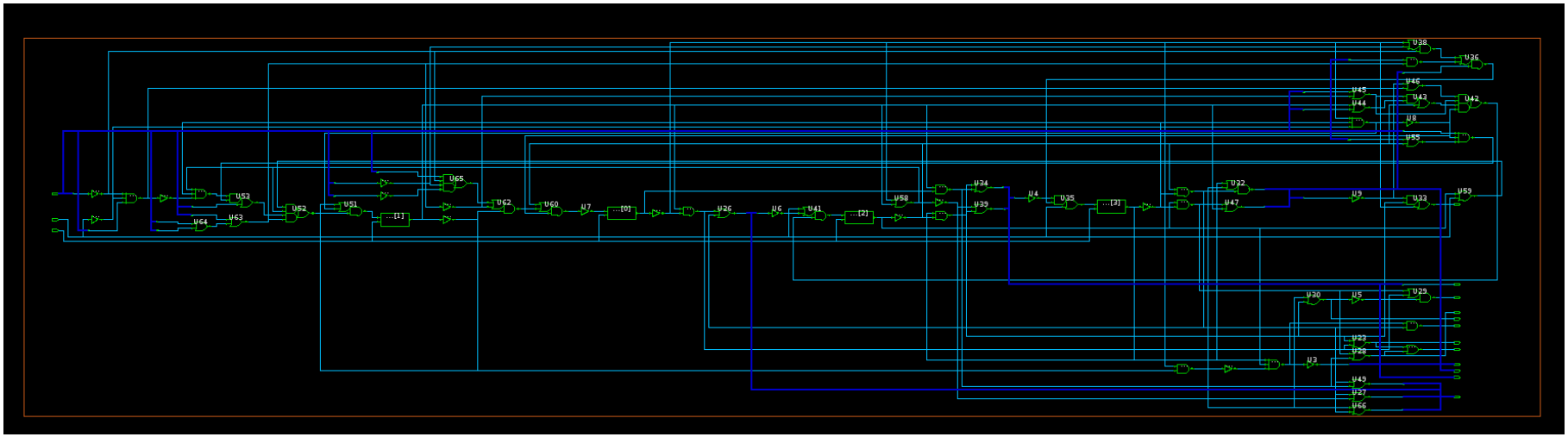


Figure 4: MIPS FSM Circuit Diagram

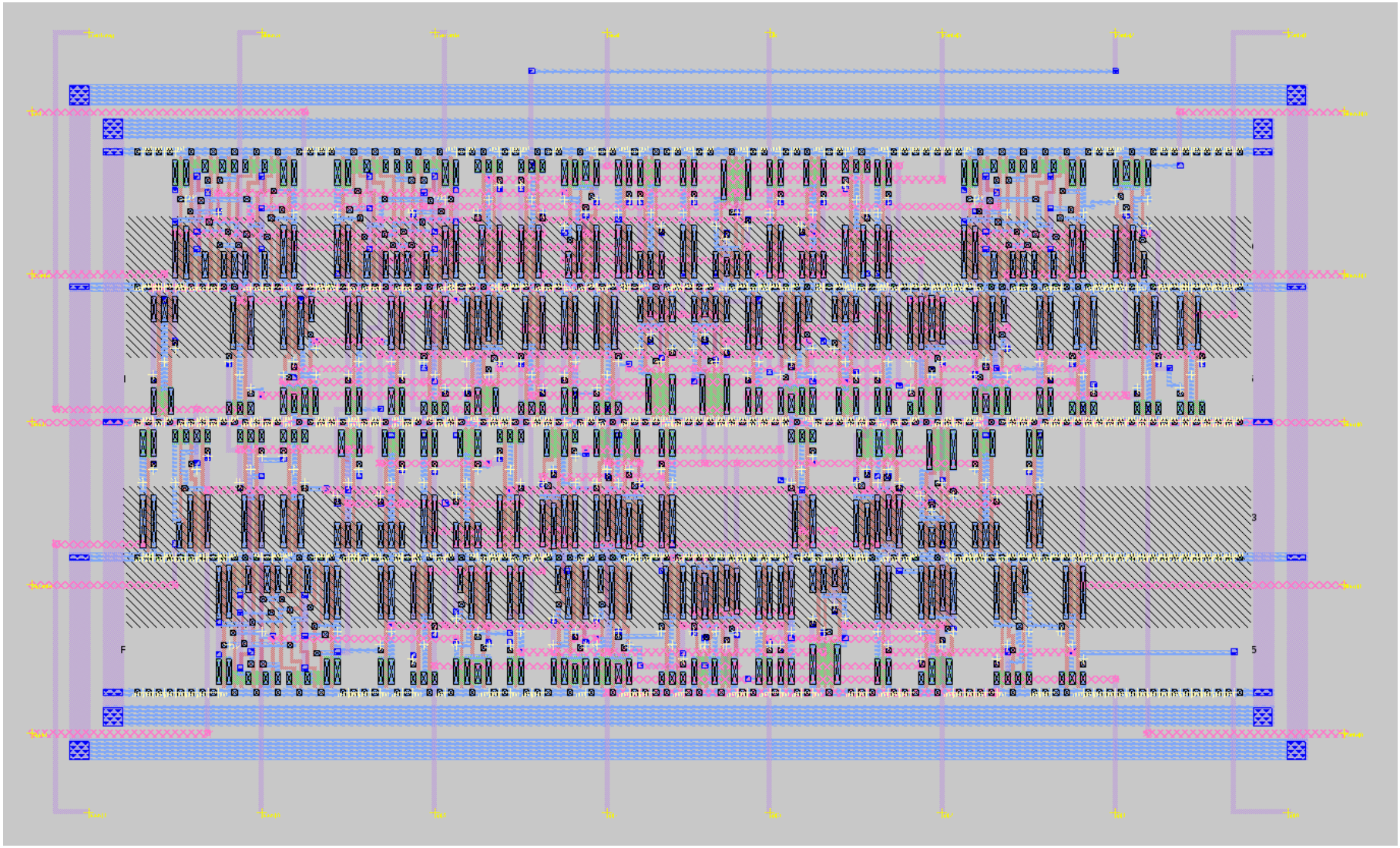


Figure 5: MIPS FSM Layout

The area of the layout was 291.9x173.4 um or 973x578 lambda (50615 um^2 or 562394 $lambda^2$)

This lab took about 2.5 hours. No major obstacles were encountered, as in fact our FSM ended up working in simulation without issue, once we refreshed our memory of SystemVerilog.