

Christer Hoeflinger
Ian Miller
ECE 425
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Lab07

Transistor Sizing

Stage	1	2	3
Pmos Size (lambda)	2x16	2x20	2x42
Nmos Size (lambda)	2x8	2x20	2x21
Capacitance	6C	10C	15.75C

The first stage was kept the same size as stated in the lab description. To calculate the other stages, we completed worksheet 2 in the pre-lab and found our G, B, H, P, and F values to calculate the optimal delay, which was 14.2. Using these calculations, we found the capacitance of each stage and found ideal sizing of transistors. The only stage that was too large was the third one with pmos being 2x64 lambda and nmos being 2x32 lambda. The maximum size that would fit in our current yzdetect was 76 lambda; however, the diffusion needed to be 12 lambda apart, leaving us with 64 lambda of work space. Pmos needed to be twice as large as the nmos for a NOR gate, giving the sizes in the table. When the delay was computed with the modified sizing, it was found to be 14.67, which meets the spec of 10% within the ideal delay.

High Speed

```
***** transient analysis tnom= 25.000 temp= 70.000 *****
tpdf1= 312.3326p targ= 2.7324n trig= 2.4200n
tpdr1= 762.6127p targ= 7.1472n trig= 6.3846n
tpd1= 537.4727p
tfall1= 81.0529p targ= 2.7752n trig= 2.6942n
trise1= 285.0431p targ= 7.3151n trig= 7.0300n
tpdf2= 630.3187p targ= 11.0475n trig= 10.4172n
tpdr2= 659.6481p targ= 15.0473n trig= 14.3876n
tpd2= 644.9834p
tfall2= 175.1916p targ= 11.1369n trig= 10.9617n
trise2= 277.7035p targ= 15.2105n trig= 14.9328n
tpdf3= 618.5923p targ= 19.0357n trig= 18.4171n
tpdr3= 658.8622p targ= 23.0433n trig= 22.3844n
tpd3= 638.7273p
tfall3= 200.7281p targ= 19.1315n trig= 18.9308n
trise3= 279.3903p targ= 23.2103n trig= 22.9310n
```

Low Speed

***** transient analysis tnom= 25.000 temp= 70.000 *****

tpdf1= 383.6665p targ= 2.8038n trig= 2.4201n
tpdr1= 949.7964p targ= 7.3351n trig= 6.3853n
tpd1= 666.7314p
tfall1= 169.7229p targ= 2.8953n trig= 2.7256n
trise1= 593.0496p targ= 7.6860n trig= 7.0930n
tpdf2= 771.1142p targ= 11.1884n trig= 10.4173n
tpdr2= 845.2096p targ= 15.2339n trig= 14.3886n
tpd2= 808.1619p
tfall2= 336.2699p targ= 11.3630n trig= 11.0267n
trise2= 593.3065p targ= 15.5874n trig= 14.9941n
tpdf3= 763.9977p targ= 19.1813n trig= 18.4173n
tpdr3= 848.5642p targ= 23.2330n trig= 22.3844n
tpd3= 806.2810p
tfall3= 379.0049p targ= 19.3768n trig= 18.9978n
trise3= 597.6559p targ= 23.5914n trig= 22.9937n

Speed Comparison

Design	Low Speed	High Speed	% Change
Tpdr (max)	949.8	762.6	80.29
Tpdr (min)	845.2	658.9	77.96
Tpdf (max)	771.1	630.3	81.74
Tpdf (min)	383.7	312.3	81.39
Tr (max)	597.7	285.0	47.68
Tr (min)	593.0	277.7	46.83
Tf (max)	379.0	200.7	52.96
Tf (min)	169.7	85.1	50.15

Note that the predicted speeds from the method of logical effort were 14.67 vs 20, or a 73.4% change. Logical effort is a very approximate method, but the actual speed reduction is on a similar order of magnitude.

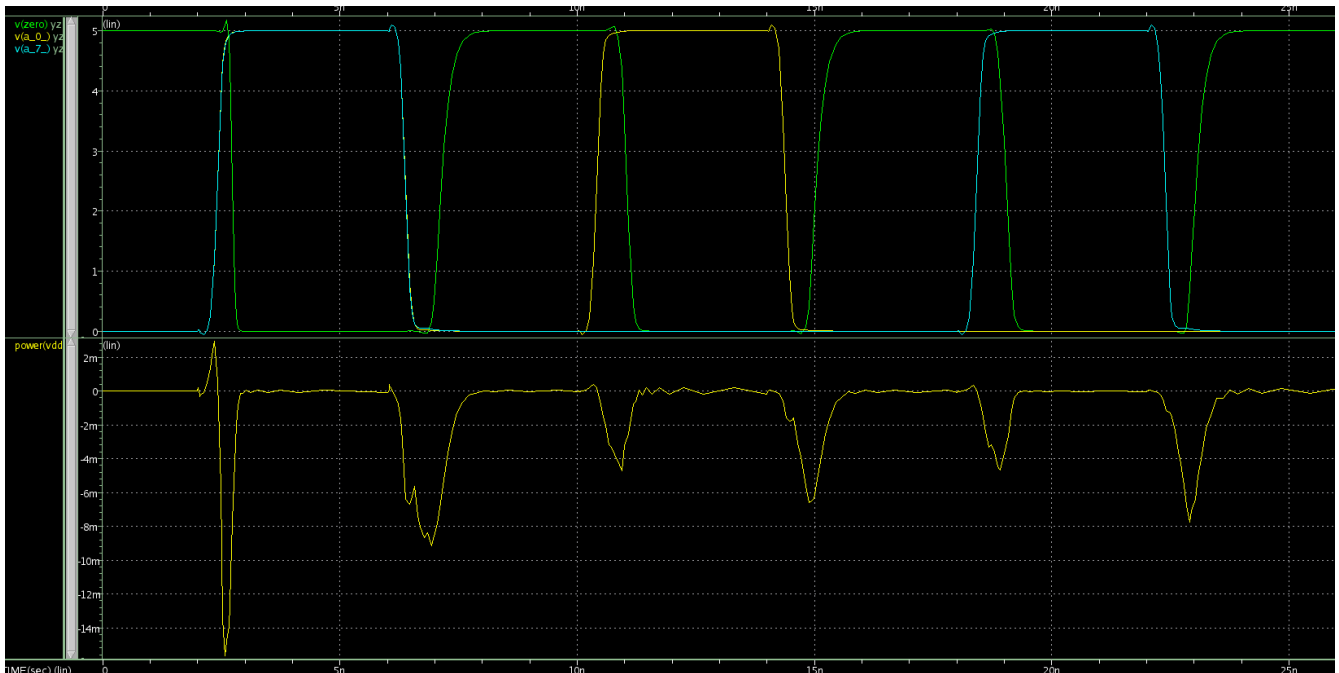


Figure 1: High Speed yzdetect Transient Simulation

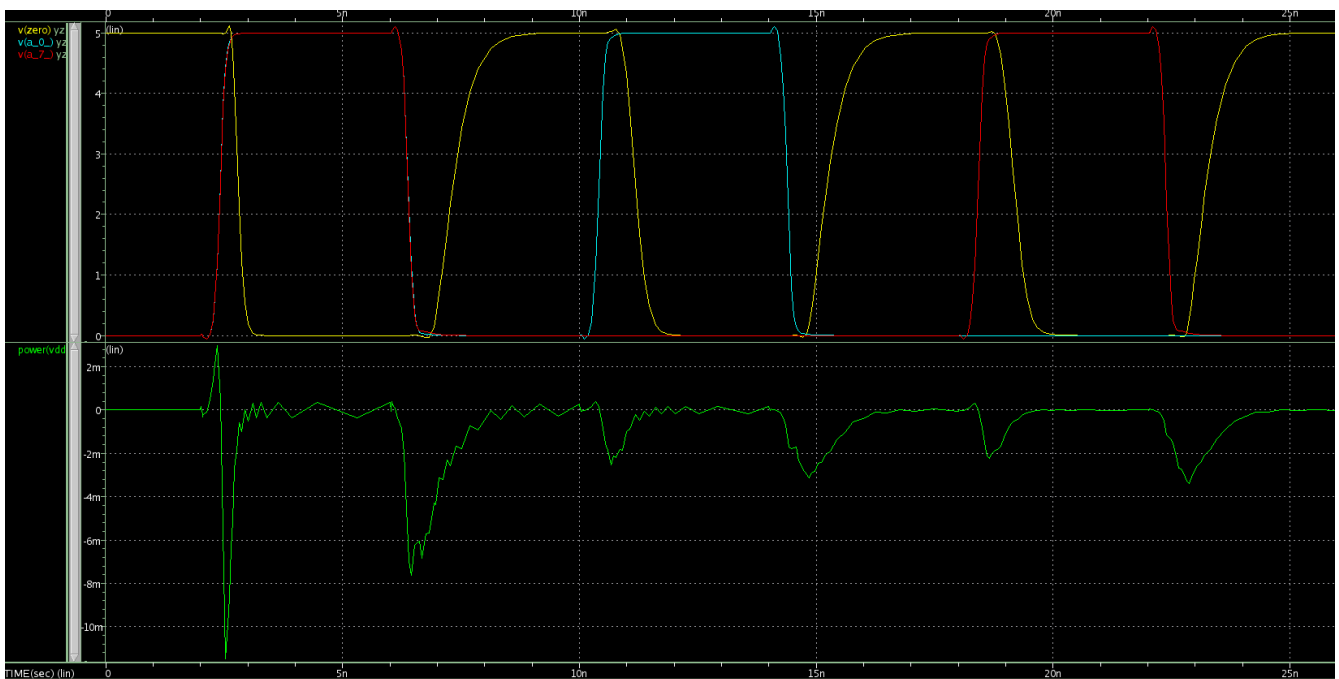


Figure 2: Low Speed yzdetect Transient Simulation

On these plots, the power consumption is the bottom plot, and the I/O voltages are on top (yellow is output).

High Speed

pwridle1=-717.8794p from= 0. to= 2.0000n
pwrsw1= -3.4192m from= 2.0000n to= 3.0000n
pwridle2= -1.7831u from= 3.0000n to= 6.0000n
pwrsw2= -3.7673m from= 6.0000n to= 8.0000n

Low Speed

pwridle1=-702.6534p from= 0. to= 2.0000n
pwrsw1= -1.9020m from= 2.0000n to= 3.0000n
pwridle2= -5.7917u from= 3.0000n to= 6.0000n
pwrsw2= -2.8957m from= 6.0000n to= 8.0000n

High Speed		Low Speed	
Idle	Switching	Idle	Switching
717.8pW	3.42mW	702.6pW	1.90mW
1.78uW	3.76mW	5.79uW	2.90mW

Note that there are two values for each of the high and low switching transition (the first and second switches on the plots). Also, as expected, note that the switching power is 56% or 77% for the low speed version over the high speed when switching (the difference is due to whether it is the rising or falling transition).

This lab took about 3 hours.